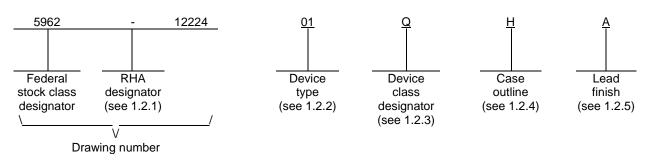
LTR								ŀ	REVISI	ONS										
						DESCR	RIPTIO	N					DA	ATE (YI	R-MO-I	DA)		APPR	OVED	
A	Add	device	type 02	2. Upda	ite elec	trical te	est limit	s and a	add life	test de	lta limi	ts jt	t 14-01-13				C. SA	\FFLE		
В	Add Add	radiatio	n hard	ened d	evice ty .2.3jt	ype 03.	Add c	ase ou	utline X.				14-12-18			C. SAFFLE				
С					pendix .									15-0	08-19			C. SAFFLE		
D	Make	e correc mA to	ction to	the un	it of the	∍ dropo	ut volta	ige tes	t (V <sub>OUT</sub>	=19.3 \	/) in Ta	able I		16-0	)2-04			C. SAFFLE		
																				* •
REV							<u></u>	<u></u>				T	1		1		T	1		
REV								<u> </u>		<u> </u>				<u> </u>		<u> </u>				
SHEET	D	D		D	D															
	D 15	D 16	D 17	D 18	D 19	D 20	D 21													
SHEET REV	15				19			D	D	D	D	D	D	D	D	D	D	D		
SHEET REV SHEET	15			18	19 /		21	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A		16 RD CUIT		18 REV SHE PRE Jet	19 / EET PAREE ffery T CKED	20 D BY Tunstal	21 D 1	_		_		6 CC	DLA I	8 LAND	9 0 ANE , OHI0	_	11 RITIMI 218-39	12 E 990	13	_
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A STA MICR DR THIS DRAW FOR U	IS NDAF OCIRC AWIN JSE BY ARTMEN ING IS A JSE BY	16 RD CUIT G VAILAI ALL ITS DF THE	3LE	18 REV SHE Jet CHE R APPI	19 / EET PAREE ffery T CKED ckED charles	20 D BY Tunstal BY Pithac D BY S Saffle	21 D 1	2		4 MIC TR/ LOV	5 CROC ANSI W-DF	6 CC http: CIRCI ENT-	DLA I DLUM CLUM UIT, I RES	LINE/ PON	9 9 0 ANE , OHIO dand dand AR, L SE, 1 -AGE	10 D MAF O 432	11 RITIMI 218-39 ime.d	12 <b>E</b> 990 <u>Ia.mil</u> SE, F <i>A</i> STAE	13 AST- BLE	_
SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A MICR MICR DR THIS DRAW FOR U DEP/ AND AGE DEPARTME	IS NDAF OCIRC AWIN JSE BY ARTMEN ING IS A JSE BY	16 RD CUIT G VAILAI ALL ITS DF THE DEFEN	3LE	18 REV SHE Jet CHE R APPI C DRA	19 / EET PAREE ffery T CKED tajesh ROVEE charles	20 D BY Funstal D BY D BY S Saffle 13-0 LEVEL	21 D 1 dia	2		4 MIC TRA LOV MO	5 CROC ANSI W-DF	6 CC http: CIRCI ENT- ROPC ITHIC	DLA I DLUM CLUM UIT, I RES	LAND MBUS W.lan UINE PON VOLT ICON	9 9 0 ANE , OHIO dand dand AR, L SE, 1 -AGE	10 0 MAF 0 432 mariti	11 RITIMI 218-39 ime.d	12 E 990 Ia.mil SE, F <i>I</i> STAE TOR,	AST- BLE	_

## 1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device class Q and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 <u>PIN</u>. The PIN is as shown in the following example:



1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type</u>. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7A4501M	Low-noise, fast transient-response, 1.5 A adjustable low-dropout voltage regulator
02	TPS7A4501-SP	Low-noise, fast transient response, 750 mA, adjustable low-dropout voltage Regulator
03	TPS7A4501-RHA	Radiation hardened, low-noise, fast transient response,1.5 A adjustable low-dropout voltage regulator

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class		Device requirement	nts documentation							
Q or V	Certi	fication and qualifica	tion to MIL-PRF-38535							
1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:										
Outline letter [	Descriptive designator	Terminals	Package style							
H GE	DFP1-F10 or CDFP2-F10	10	Flat pack							
X Se	e Figure 2	10	Flat pack							
1.2.5 Lead finish. The lead fini	ish is as specified in MIL-PR	RF-38535 for device	classes Q and V.							
STANDARD MICROCIRCUIT DRAWING		SIZE A		5962-12224						
DLA LAND AND I COLUMBUS, OHIO			REVISION LEVEL D	SHEET 2						

	resses above the absolute maximum rating may cause f aximum levels may degrade performance and affect reli- bosolute maximum input-to-output differential voltage can n voltages. With the IN pin at 22 V, the OUT pin may no JT can not exceed ± 22V. The manufacturer supplying RHA device type 03 has perfe- ethod 1019 paragraph 3.13.1.1. The radiation end point ethod 1019, condition A and condition D to a maximum to STANDARD MICROCIRCUIT DRAWING	ability. not be achieved v ot be pulled below formed characteriz limits for the conc	vith all combinations of rate 0 V. The total measured v ration testing in accordance litions are as specified in M	d IN pin and OUT oltage from IN to with MIL-STD-883
	aximum levels may degrade performance and affect reli- psolute maximum input-to-output differential voltage can in voltages. With the IN pin at 22 V, the OUT pin may no UT can not exceed ± 22V. The manufacturer supplying RHA device type 03 has perfected thod 1019 paragraph 3.13.1.1. The radiation end point ethod 1019, condition A and condition D to a maximum to	ability. not be achieved v ot be pulled below ormed characteriz limits for the cond total dose of 100 l	vith all combinations of rate 0 V. The total measured v ration testing in accordance litions are as specified in M	d IN pin and OUT oltage from IN to with MIL-STD-883
1.5 <u>F</u> M The ma	Operating temperature range (T <sub>A</sub> = T <sub>J</sub> ) Radiation features. Naximum total dose available (dose rate = 50-300 rads(S Device type 03 nufacturer supplying RHA part device type 03 has perfo 1019 paragraph 3.13.1.1 to a maximum total dose of 10	Si)/s): rmed characteriza	100 krads(Si) <u>3</u> /	with MIL-STD-883
	Recommended operating conditions		- 55°C to +125°C	
Ĺ	case outline X Thermal resistance, junction-to-case (bottom) ( $\theta_{JC}$ bot) Thermal resistance, junction-to-ambient ( $\theta_{JA}$ )			
_	case outline H Thermal resistance, junction-to-case (bottom) $(\theta_{JC})$ Thermal resistance, junction-to-ambient $(\theta_{JA})$			
S	ead temperature (10s soldering time) operating junction temperature (T <sub>J</sub> ) torage temperature range, T( <sub>STG)</sub>		125°C	
	Input-to-output differential <u>2</u> / ADJ SHDN		- 22 V to 22 V - 7 V to 7 V	
	IN OUT			

## 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

# DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

# DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits. MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

# DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <u>http://quicksearch.dla.mil/</u> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Radiation exposure circuit</u>. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein .

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-12224
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Test	Symbol	Conditions -55° $\leq$ T <sub>A</sub> $\leq$ +125°C <u>1</u> / T <sub>A</sub> =T <sub>J</sub>	Group A subgroups	Device type	Limits		Unit
		unless otherwise specified			Min	Max	
Minimum input voltage <u>2/3/</u>	V <sub>IN</sub>	$I_{load} = 0.5 \text{ A}, T_A = 25^{\circ}\text{C}$	1	01, 02		2.3	V
		I <sub>load</sub> = 1.5 A	1, 2, 3	01		2.5	
		I <sub>load</sub> = 750 mA	1, 2, 3	02		2.5	
		I <sub>load</sub> = 1.5 A	1, 2, 3	03		2.9	
	$V_{\text{ADJ}}$	$V_{IN}$ = 2.21 V, $I_{LOAD}$ = 1mA,	1	01	1.197	1.222	
ADJ pin voltage <u>2/ 4</u> /		$T_A = 25^{\circ}C$	1	02	1.196	1.224	V
		$V_{IN} = 2.5 \text{ V to } 20 \text{ V}$ $I_{LOAD} = 1 \text{ mA to } 1.5 \text{ A}$	1,2, 3	01	1.174	1.246	
		$V_{IN} = 2.5 V \text{ to } 20 V$ $I_{LOAD} = 1 \text{ mA to } 750 \text{ mA}$	1, 2, 3	02	1.174	1.246	
		$V_{IN} = 2.9 V$ to 20 V I <sub>LOAD</sub> = 1 mA to 1.5 A	1, 2, 3	03	1.174	1.246	
Line regulation <u>2</u> /	V <sub>RLINE</sub>	$\Delta V_{IN} = 2.21 \text{ V to } 20 \text{ V},$	1, 2, 3	01		3	mV
		I <sub>LOAD</sub> = 1mA	1, 2, 3	02		4.5	
		$\Delta V_{IN} = 2.9 V$ to 20 V, I <sub>LOAD</sub> = 1mA	1, 2, 3	03		6.5	
Load regulation <u>2</u> /	V <sub>RLOAD</sub>	V <sub>IN</sub> = 2.5 V,	1	01		8	
		$\Delta I_{LOAD} = 1 \text{ mA to } 1.5 \text{ A}$	2, 3			18	
		VIN = 2.5 V,	1	02		8	
		$\Delta I_{LOAD} = 1 \text{ mA to } 750 \text{ mA}$	2, 3			18	
		VIN = 2.9 V,	1	03		10	
		$\Delta I_{LOAD} = 1 \text{ mA to } 1.5 \text{ A}$	2, 3			18	
Drop out voltage	V <sub>DO</sub>	I <sub>LOAD</sub> = 1 mA	1	01, 02		.05	V
$V_{OUT} = 2.4 V$			2, 3	01, 02		.07	
<u>5</u> / <u>6</u> /		I <sub>LOAD</sub> = 100 mA	1	01, 02		.10	
			2, 3	01, 02		.13	
		I <sub>LOAD</sub> = 500 mA	1	01, 02		.21	
			2, 3	01, 02		.27	

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Test	Symbol	$\begin{array}{l} \text{Conditions}  \underline{1} / \\ \textbf{-55^{\circ}} \leq T_{\text{A}} \leq \textbf{+125^{\circ}C} \\ T_{\text{A}} = T_{\text{J}} \end{array}$	Group A subgroups	Device type	Limits		Unit
		unless otherwise specified			Min	Max	
Drop out voltage	V <sub>DO</sub>	I <sub>LOAD</sub> = 750 mA	1	01, 02		.27	V
$V_{OUT} = 2.4V$			2, 3	01, 02		.33	
<u>5/ 6</u> /		I <sub>LOAD</sub> = 1.5 A	1	01		.50	
			2, 3	01		.75	
Dropout voltage $V_{OUT} = 19.3 V$ <u>5</u> / <u>7</u> /	V <sub>DO</sub>	I <sub>LOAD</sub> = 1 mA	1	03		.32	V
			2, 3	03		.40	
		$I_{LOAD} = 100 \text{ mA}$	1	03		.40	
			2, 3	03		.58	
		$I_{LOAD} = 500 \text{ mA}$	1	03		.40	
			2, 3	03		.60	
		I <sub>LOAD</sub> = 750 mA	1	03		.40	
			2, 3	03		.62	
		$I_{LOAD} = 1.0 \text{ A}$	1	03		.45	
			2, 3	03		.65	
		I <sub>LOAD</sub> = 1.25 A	1	03		.50	
			2, 3	03		.68	
		$I_{LOAD} = 1.5 \text{ A}$	1	03		.60	
			2, 3	03		.75	

 TABLE I.
 Electrical performance characteristics – Continued.

See footnotes at end of table.

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Test	Symbol		tions <u>1</u> / <sup>7</sup> <sub>A</sub> ≤ +125°C ,=T <sub>J</sub>	Group A subgroups	Device type	Lim	iits	Unit
			wise specified			Min	Max	
GND pin current		$I_{LOAD} = 0 \text{ mA}$		1, 2, 3	01, 02		1.5	mA
V <sub>IN</sub> = 2.5 V		$I_{LOAD} = 1 \text{ mA}$		1, 2, 3	01, 02		1.6	
<u>6/ 8</u> /		$I_{LOAD} = 100 \text{ mA}$		1, 2, 3	01, 02		7.0	
		$I_{LOAD} = 500 \text{ mA}$		1, 2, 3	01, 02		30	
		$I_{LOAD} = 750 \text{ mA}$		1, 2, 3	02		45	
		$I_{LOAD} = 1.5 A$		1, 2, 3	01		130	
GND pin current		$I_{LOAD} = 0 \text{ mA}$		1, 2, 3	03		1.5	mA
V <sub>IN</sub> = 2.9 V		I <sub>LOAD</sub> = 1 mA		1, 2, 3	03		1.6	
<u>6/ 9/</u>		I <sub>LOAD</sub> = 100 mA		1, 2, 3	03		7.0	
		I <sub>LOAD</sub> = 500 mA		1, 2, 3	03		30	
		I <sub>LOAD</sub> = 750 mA		1, 2, 3	03		45	
		I <sub>LOAD</sub> = 1 A		1, 2, 3	03		50	
		I <sub>LOAD</sub> = 1.25 A		1, 2, 3	03		80	
		I <sub>LOAD</sub> = 1.5 A 1, 2, 3		03		105		
Output voltage noise <u>10</u> /	E <sub>N</sub>	$C_{OUT} = 10\mu$ F, $I_{LC}$ B <sub>W</sub> = 10Hz to 10 T <sub>A</sub> = 25°C		4	01		55	μV <sub>RMS</sub>
I <sub>ADJ</sub> pins bias current <u>2</u> / <u>11</u> /	I <sub>ADJ</sub>			1	01, 02, 03		7	μA
				2, 3	03		15	
Shutdown threshold		$V_{OUT} = OFF$ to C	DN	1, 2, 3	01, 02, 03		2	V
		$V_{OUT} = ON$ to O	FF	1, 2, 3	01, 02, 03	0.15		
SHDN pin current		$V_{\overline{SHDN}} = 0 V,$		1	01, 02		1	μA
				1, 2, 3	03		10	
		$V_{SHDN} = 20 V,$		1	01, 02		20	
				1, 2, 3	03		20	
Quiescent current in shutdown		$V_{IN} = 6 V,$		1	01, 02		1	μA
		$V_{SHDN} = 0V,$		1, 2, 3	03		10	
			M, D, P, L, R	1	03		50	

TABLE I. <u>Electrical performance characteristics</u> – Continued.

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-12224
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	TABLE	I. Electrical performance character	<u>istics</u> – Conti	nuea.			
Test	Symbol	Conditions $\frac{1}{}$ -55° ≤ T <sub>A</sub> ≤ + 125°C	Group A subgroups	Device type	Lir	nits	Unit
		$T_A = T_J$ Unless otherwise specified			Min	Max	
Ripple rejection <u>12</u> /		$V_{IN}-V_{OUT} = 1.5 V (avg),$ $V_{RIPPLE} = 0.5 V_{P-P},$	4	01,02, 03	60		db
		$F_{RIPPLE} = 120HZ, I_{LOAD} = 0.75 A$	5,6	03	58		
	$V_{IN}$ - $V_{OUT} = 1.5 V (avg),$	4	03	54		db	
		$V_{RIPPLE} = 0.5 V_{P-P},$ $F_{RIPPLE} = 120HZ, I_{LOAD} = 1.5 A$	5, 6	03	44		
Current limit <u>12</u> /	ILIMIT	$V_{IN} = 7 V$ , $Vout = 0V$	1	01, 02,	1.7		А
			1, 2, 3	03			
		V <sub>IN</sub> = 2.5 V, Vout = 0V	1, 2, 3	01, 02	1.6		
		V <sub>IN</sub> = 2.9 V, Vout = 0V	1, 2, 3	03	1.6		
Input reverse leakage current	I <sub>IL</sub>	$V_{IN} = -20 V, V_{out} = 0 V$	1, 2, 3	01, 02, 03		300	μA
Reverse output current 13/	I <sub>RO</sub>	$V_{OUT} = 1.21 \text{ V}, V_{IN} < 1.21 \text{ V}$	1	01, 02		500	μA
			1, 2, 3	03		500	

TABLE | Electrical performance characteristics - Continued

<u>1</u>/ Device type 03 supplied to this drawing have been characterized through all levels P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level,  $T_A = +25$ °C (see1.5 herein).

The manufacturer supplying RHA device type 03 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1. The radiation end point limits for the conditions are as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si).

2/ The device is tested and specified for these condition with the ADJ pin connected to the OUT pin.

3/ Dropout voltage are limited by the minimum input voltage specification under some output voltage/load conditions.

- <u>4</u>/ Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
- 5/ Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to:  $V_{IN} V_{DROPOUT}$ .
- <u>6</u>/ To satisfy requirements for minimum input voltage, the device is tested and specified for these conditions with an external resistor divider (two 4.12kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300µA DC load on the output.
- <u>7</u>/ To satisfy requirements for minimum input voltage, the device is tested and specified for these conditions with an external resistor divider (one 4.12- kΩ resistor and one 61.9) for an output voltage of 19.3 V. The external resistor divider adds a 300- µA dc load on the output.
- 8/ GND pin current is tested with V<sub>IN</sub> = 2.5 V and a current source load. The GND pin current decreases at higher input voltages.
- $\underline{9}$ / GND pin current is tested with V<sub>IN</sub> = 2.9 V and a current source load. The GND pin current deceases at high input voltages.

10/ Not production tested parameter, guaranteed by characterization.

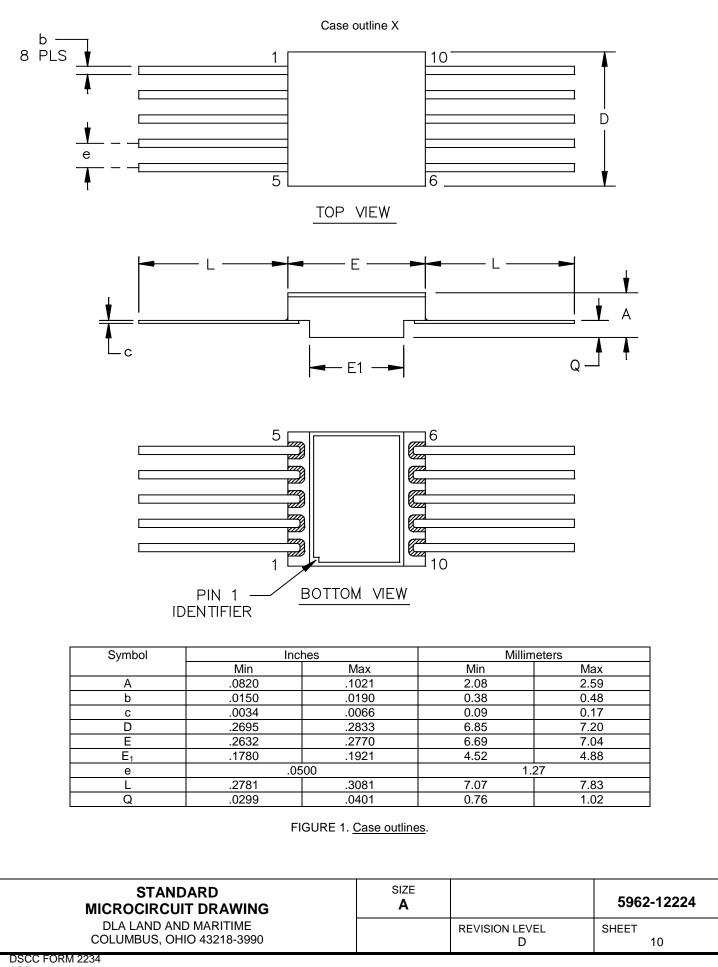
STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-12224
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TABLE I.	Electrical	performance	characteristics	- Continued.

 $\underline{11}$ / ADJ pin bias current flows into the ADJ pin.

- <u>12</u>/ Specification is guaranteed by characterization for KGD and is not tested in production.
- 13/ Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows Into the OUT pin and out the GND pin.

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	24, 22, 22
Device type	01, 02, 03
Case outline	H, X
Terminal number	Terminal symbol
1	SHDN
2	IN
3	IN
4	IN
5	N/C
6	OUT
7	OUT
8	OUT
9	SENSE/ADJ
10	GND

FIGURE 2. Terminal connections.

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PIN		DESCRIPTION		
NO.	NAME			
1	SHDN	Shutdown. SHDN is used to put the regulator into a low-power shutdown state. The output is off when SHDN is pulled low. SHDN can be driven by 5-V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and SHDN current, typically 3 $\mu$ A. If unused, SHDN must be connected to V <sub>IN</sub> . The device is in the low-power shutdown state if SHDN is not connected.		
2, 3, 4	IN	Input. Power is supplied to the device through IN. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1µF to 10µF is sufficient. The regulator is designed to withstand reverse voltage on IN with respect to ground and on OUT. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.		
5	NC	Not Connected.		
6, 7, 8	OUT	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10µF is required to prevent oscillations. Larger output capacitors are required for application with large transient loads to limit peak voltage transients.		
9	ADJ	Adjust. This is the input to the error amplifier. ADJ is internally clamped to $\pm$ 7 V. It has a bias current of 3 µA that flows into the pin. ADJ voltage is 1.21 V references to ground, and the output voltage range is 1.21 V to 20V.		
10	GND	Ground.		
Thermal Vias (Case outline )	тX)	The exposed thermal vias of the case outline X should be connected to a wide ground plane for effective heat dissipation.		

FIGURE 2. <u>Terminal connections</u> – Continued.

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3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

# 4. VERIFICATION

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

# 4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

### 4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5, 6, 7, 8, 9, 10 and 11 in table I method 5005 of MIL-STD-883 shall be omitted.

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Test requirements	Subgroups		
	(in accordance with		
	MIL-PRF-38535, table III)		
	Device	Device	
	class Q	class V	
Interim electrical	1, 2, 3	1, 2, 3	
parameters (see 4.2)			
Final electrical	1, 2, 3, 4 <u>1</u> /	1, 2, 3, 4	
parameters (see 4.2)		<u>1/ 2</u> /	
Group A test	1, 2, 3, 4	1, 2, 3, 4	
requirements (see 4.4)			
Group C end-point electrical	1, 2, 3, 4	1, 2, 3, 4	
parameters (see 4.4)		<u>2</u> /	
Group D end-point electrical	1	1	
parameters (see 4.4)			
Group E end-point electrical	1, 4	1, 4	
parameters (see 4.4)			

TABLE IIA. Electrical test requirements.

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

TABLE IIB. <u>240 burn-in and group C life test delta parameters</u>. ( $T_A = +25^{\circ}$  C). <u>1</u>/

Parameters	Symbol	Min	Max	Units
ADJ pin voltage	V <sub>ADJ</sub>	-0.012	+0.012	V
Line Regulation	V <sub>RLINE</sub>	-0.24	+0.24	mV

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

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4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}C \pm 5^{\circ}C$ , after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 <u>Total dose irradiation testing</u>. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and condition D as specified herein for device type 03.

4.4.4.1.1 <u>Accelerated annealing test</u>. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

# 5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

# 6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

## 6.6 Sources of supply.

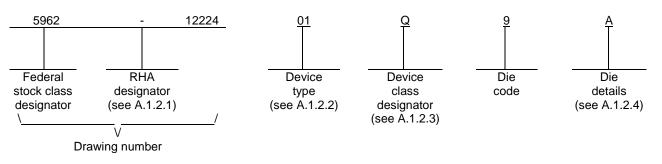
6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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# A.1 SCOPE

A.1.1 <u>Scope</u>. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 <u>PIN</u>. The PIN is as shown in the following example:



A.1.2.1 <u>RHA designator</u>. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 <u>Device type</u>. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7A4501M	Low-noise, fast transient-response, 1.5 A adjustable low-dropout voltage regulator
02	TPS7A4501-SP	Low-noise fast transient-response 750 mA adjustable low-dropout voltage regulator
03	TPS7A4501-RHA	Radiation hardened, low-noise, fast transient response, 1.5 A adjustable low-dropout voltage regulator

### A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 <u>Die details</u>. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.	
<u>Die type</u>	Figure number
01, 02, 03	A-1
A.1.2.4.2 Die bonding pad locations and electric	al functions.
<u>Die type</u>	Figure number
01, 02, 03	A-1
A.1.2.4.3 Interface materials.	
Die type	Figure number
01, 02, 03	A-1
A.1.2.4.4 Assembly related information.	
<u>Die type</u>	Figure number
01, 02, 03	A-1

A.1.3 <u>Absolute maximum ratings</u>. See paragraph 1.3 herein for details.

A.1.4 <u>Recommended operating conditions</u>. See paragraph 1.4 herein for details.

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## A.2 APPLICABLE DOCUMENTS.

A.2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

#### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <u>http://quicksearch.dla.mil/</u>or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

#### A.3 REQUIREMENTS

A.3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 <u>Design, construction and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 <u>Die bonding pad locations and electrical functions</u>. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.3 <u>Electrical performance characteristics and post-irradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 <u>Electrical test requirements</u>. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 <u>Marking</u>. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 <u>Certification of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

## A.4 VERIFICATION

A.4.1 <u>Sampling and inspection</u>. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

### A.4.3 Conformance inspection.

A.4.3.1 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.1.1 herein.

## A.5 DIE CARRIER

A.5.1 <u>Die carrier requirements</u>. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

## A.6 NOTES

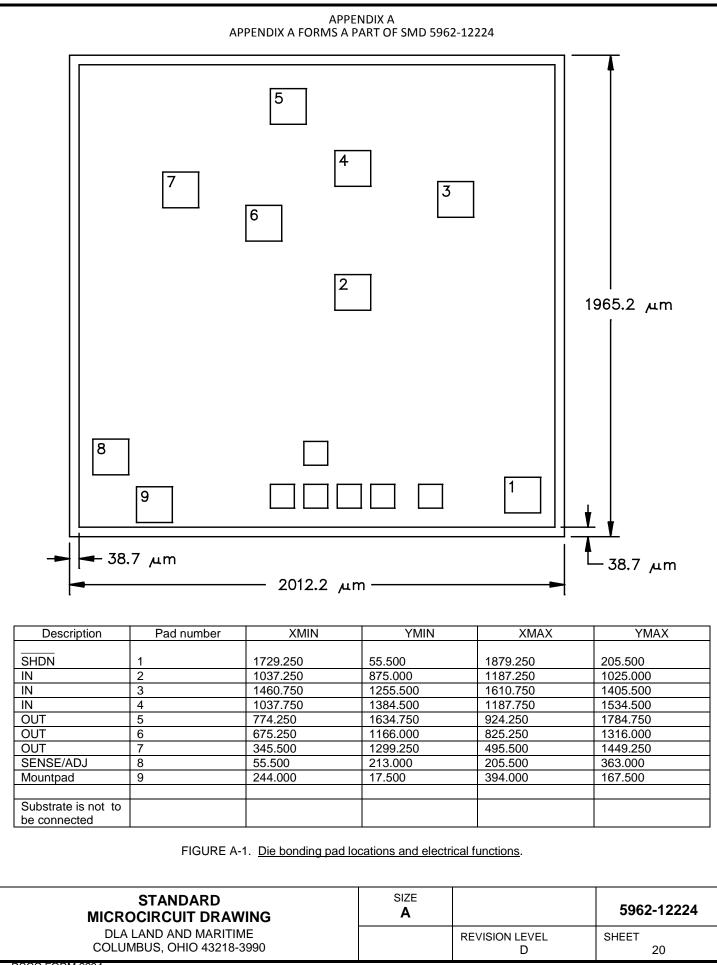
A.6.1 <u>Intended use</u>. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 <u>Comments</u>. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime VA and have agreed to this drawing.

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Die bonding pad locations and electrical functions

Die physical dimensions. Die size: 1964.00  $\mu m$  x 2012.00  $\mu m$  Die thickness: 15  $\pm$  1 mils

Interface materials. Top metallization: TiW/AICu2(1627 nm) Backside metallization: None

Glassivation. Type: SIN Thickness: 10 kA

Substrate: P(111) 10-21 ohm-cm

Assembly related information. Substrate potential: Insulated (backside of the die is left floating in factory package assembly) Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

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#### STANDARD MICROCIRCUIT DRAWING BULLETIN

### DATE: 16-02-04

Approved sources of supply for SMD 5962-12224 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <a href="http://www.landandmaritime.dla.mil/Programs/Smcr/">http://www.landandmaritime.dla.mil/Programs/Smcr/</a>.

Standard	Vendor	Vendor
microcircuit drawing	CAGE	similar
PIN <u>1</u> /	number	PIN <u>2</u> /
5962-1222401QHA	01295	TPS7A4501MUB
5962-1222401Q9A	01295	TPS7A4501MKGD1
5962-1222402VHA	01295	TPS7A4501-SP
5962-1222402V9A	01295	TPS7A4501KGD-SP
5962R1222403VXC	01295	TPS7A4501-RHA
5962R1222403V9A		TPS7A4501RHAKGD

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- <u>2</u>/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number Vendor name and address

01295

Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243

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