REF5025-HT Low-Noise, Very-Low-Drift, Precision Voltage Reference

1 Features

- Low Temperature Drift: 40 ppm/°C
- Low Noise: 3 μV_{PP}/V
- High Output Current: ±7 mA
- Low Temperature Drift: 5 ppm/°C (Maximum)
- Available in Military (–55°C to +210°C) Temperature Range (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

2 Applications

- 16-Bit Data Acquisition Systems
- ATE Equipment
- Industrial Process Control
- Medical Instrumentation
- Optical Control Systems
- Precision Instrumentation
- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site

(1) Custom temperature ranges available

3 Description

The REF5025-HT is a low-noise, very low-drift, very high precision voltage references. This reference is capable of both sinking and sourcing, and is very robust with regard to line and load changes.

Excellent temperature drift and high accuracy are achieved using proprietary design techniques. These features, combined with very low noise, make the REF5025-HT suitable for use in high-precision data acquisition systems.

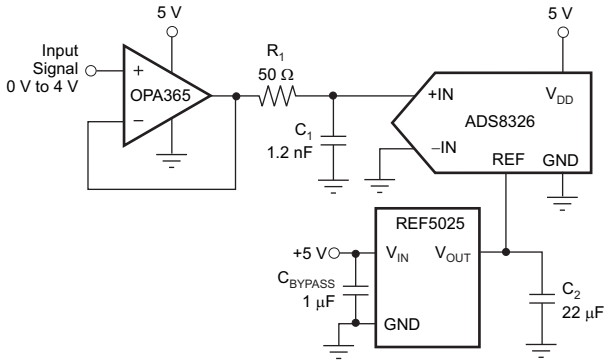
The device is offered in HKJ and HKQ packages, as well as Known-Good-Die (KGD) form, and is specified from –55°C to +210°C.

Device Information(a)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF5025-HT	CFP (HKJ)(8)	6.9 mm × 5.65 mm
	CFP (HKQ) (8)	6.9 mm × 5.65 mm
	XCEPT (KGD) (0)	2.04 mm × 1.676 mm

(a) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2013) to Revision F — **Page**

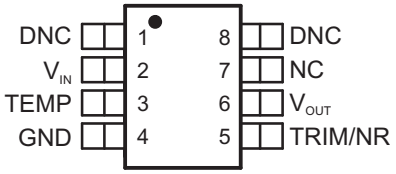
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table, see POA at the end of the data sheet ... 1

Changes from Revision D (April 2012) to Revision E — **Page**

- Added KGD2 package option ... 1

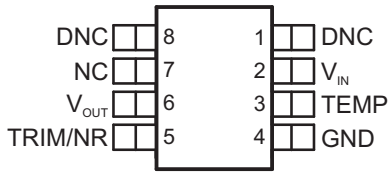
5 Pin Configuration and Functions

HKJ Package
8-Pin CFP
Top View



DNC = Do not connect
NC = No internal connection

HKQ Package
8-Pin CFP
Top View



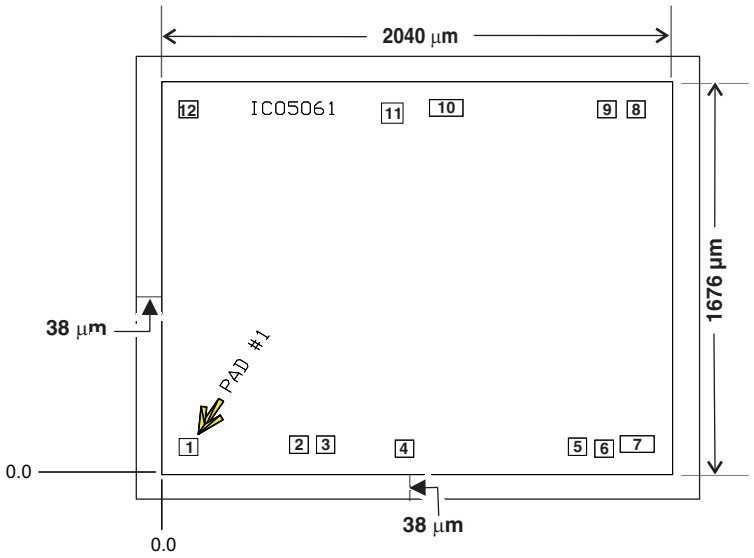
HKQ is a dead bug performed version of HKJ

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	1, 8	—	Do not connect
GND	4	Power	System ground
NC	7	—	No internal connection
TEMP	3	O	Temperature monitoring pin provides a temperature-dependent voltage output
TRIM/NR	5	I	Output adjustment and noise reduction input. Connecting 1 μF to this pin creates a low-pass filter at the bandgap and reduce output noise
V_{IN}	2	Power	Power supply voltage. Range from V_{OUT} + 0.2 V up to 18 V. TI recommends a bypass capacitor with a value from 1 μF up to 10 μF
V_{OUT}	6	O	Very accurate, factory-trimmed voltage output. TI recommends a bypass capacitor with a value from 1 μF up to 50 μF with ESR between 1 and 1.5 Ω

Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	GND	Al-Cu (0.5%)	598 nm



Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
NC	1	35.45	46.55	111.45	122.55
NC	2	496.75	56.55	572.75	132.55
VIN	3	607.45	56.55	683.45	132.55
NC	4	637.9	39.4	1013.9	115.4
TEMP	5	1660.1	47.2	1736.1	123.2
GND	6	1770.9	38.85	1847.05	115
GND	7	1877.1	59.6	2016.8	135.6
TRIM/NR	8	1904.65	1553.4	1980.65	1629.4
NC	9	1782.15	1553.4	1858.15	1629.4
VOUT	10	1080.2	1559.85	1219.9	1636
VOUT	11	880.25	1543.55	956.25	1619.55
NC	12	35.45	1553.45	111.45	1629.45

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}		18	V
Output short-circuit			30	mA
Operating temperature		–55	210	°C
Junction temperature, T_J			210	°C
Storage temperature, T_{stg}		–65	210	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	3.25	18	V
I_{OUT}	–7	7	mA

6.4 Thermal Information

THERMAL METRIC(1)		REF5025-HT HJK, HKQ (CFP) 8 PINS	UNIT
$R_{\theta JC}$ Junction-to-case thermal resistance	To ceramic side of case	5.7	°C/W
	To top of case lid (metal side of case)	13.7	

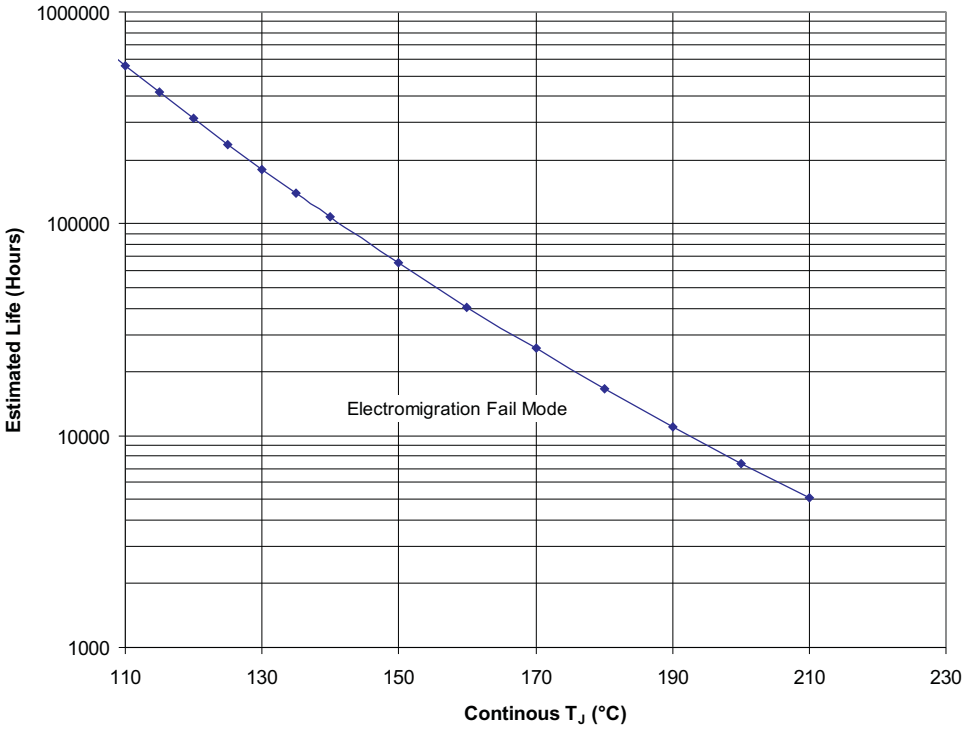
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

at T_A = 25°C, I_{LOAD} = 0, C_L = 1 µF, V_{IN} = 3.25 V to 18 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A = –55 to +125°C			T_A = 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE (2.5 V)									
V_{OUT}	Output voltage			2.5			2.5		V
	Initial accuracy(1)	V_{IN} = 3.25 V	0%		0.9%		0.14%		
NOISE									
	Output voltage noise	f = 0.1 Hz to 10 Hz		7.5					μV_{PP}
OUTPUT VOLTAGE TEMPERATURE DRIFT									
dV_{OUT}/dT	Output voltage temperature drift(2)	Calculated from –55°C to +210°C						40	ppm/°C
LINE REGULATION									
dV_{OUT}/dV_{IN}	Line regulation	From V_{IN} = 3.25 V to V_{IN} = 18 V		1	2.2		63	215	ppm/V
LOAD REGULATION									
dV_{OUT}/dI_{LOAD}	Load regulation	–7 mA < I_{LOAD} < 10 mA, V_{IN} = 3.25 V		20	50		20	75	ppm/mA
SHORT-CIRCUIT CURRENT									
I_{SC}	Short-circuit current	V_{OUT} = 0 V		25			11		mA
TEMP PIN									
	Voltage output	At T_A = 25°C		575					mV
Temperature sensitivity(3)				2.64					mV/°C
TURN-ON SETTLING TIME									
	Turn-on settling time	To 0.1% with C_L = 1 µF		200					µs
POWER SUPPLY									
V_S	Supply voltage		3.25		18	3.25		18	V
	Quiescent current			0.8	1.2			1.5	mA
TEMPERATURE RANGE									
	Specified range	–55°C to +210°C							
	Operating range	–55°C to +210°C							

(1) See Figure 5.
(2) See Figure 4.
(3) See Figure 10.



(1) See *Absolute Maximum Ratings* and *Recommended Operating Conditions*.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. REF5025SKGD1 and REF5025SKGD2 Operating Life Derating Chart

6.6 Typical Characteristics

at T_A = 25°C, I_{LOAD} = 0, V_S = 3.25 V (unless otherwise noted).

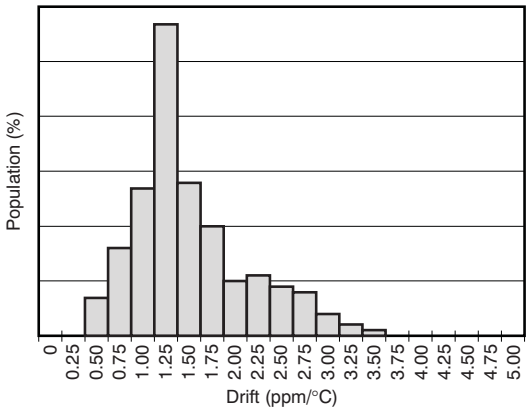


Figure 2. Temperature Drift (0°C to 85°C)

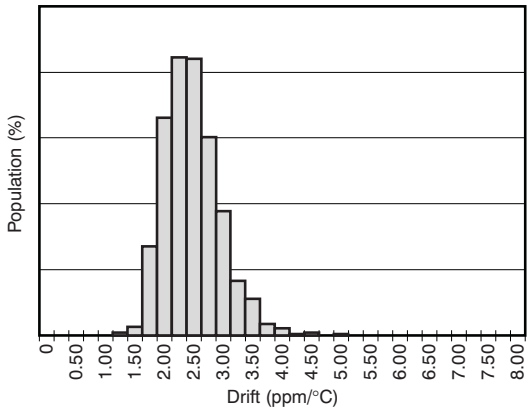


Figure 3. Temperature Drift (–40°C to +125°C)

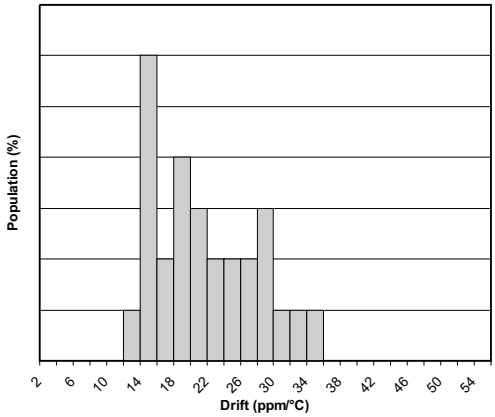


Figure 4. Temperature Drift (–55°C to +210°C)

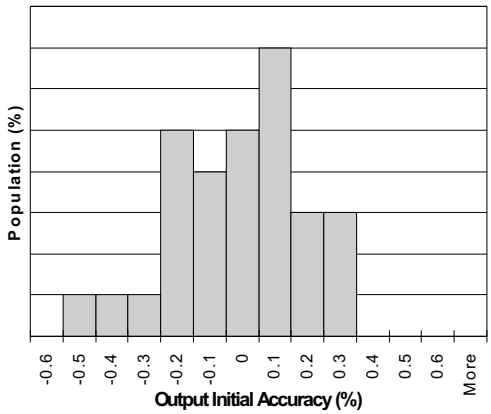


Figure 5. Output Voltage and Initial Accuracy (210°C)

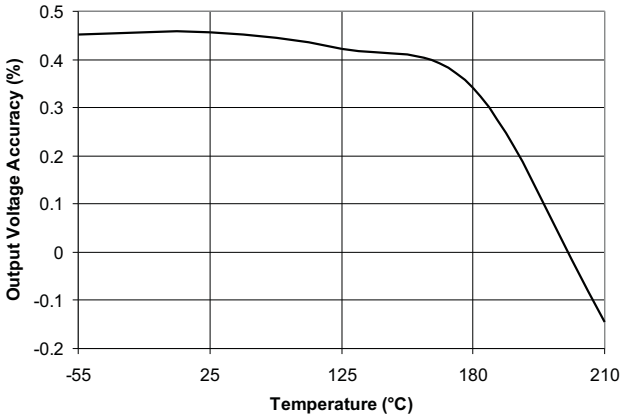


Figure 6. Output Voltage Accuracy vs Temperature

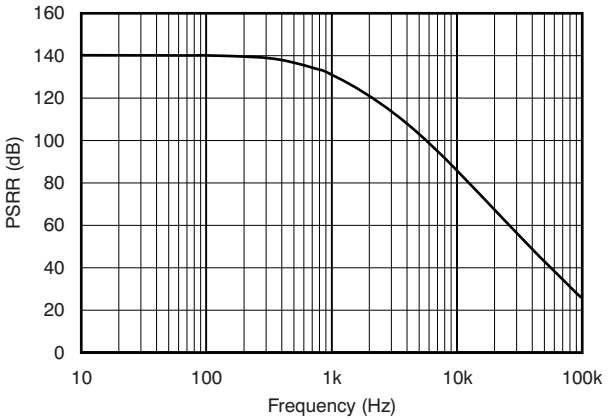


Figure 7. Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, I_{LOAD} = 0, V_S = 3.25 V (unless otherwise noted).

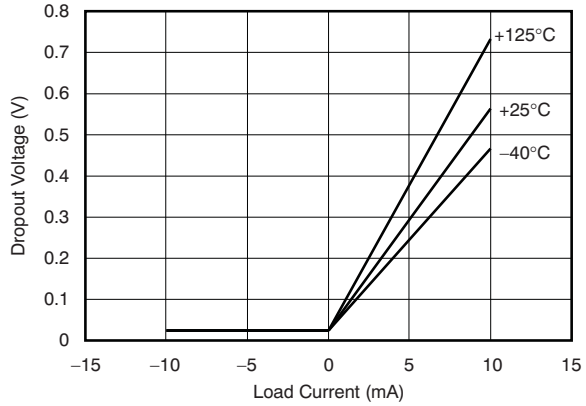


Figure 8. Dropout Voltage vs Load Current

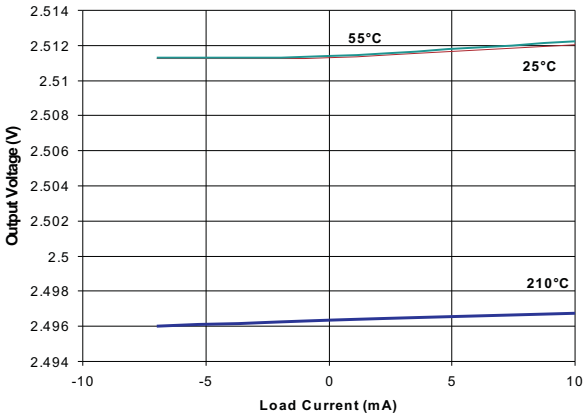


Figure 9. Output Voltage vs Load Current

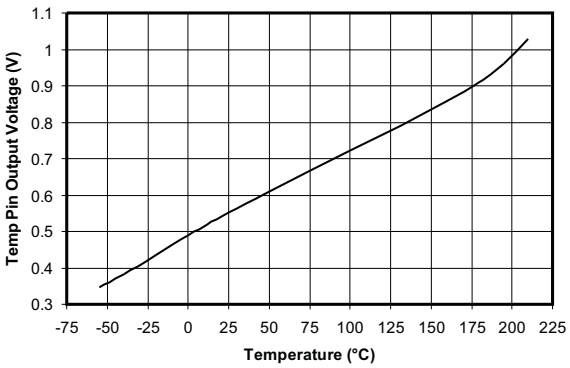


Figure 10. Temperature Pin Output Voltage vs Temperature

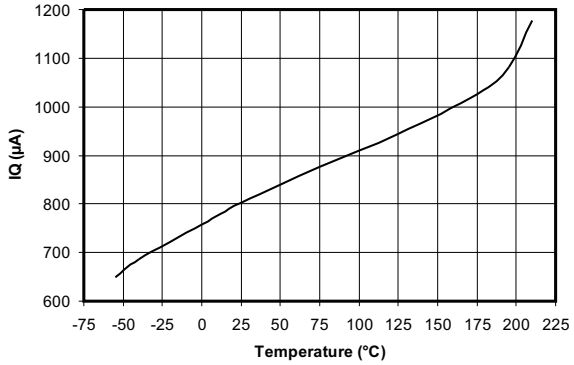


Figure 11. Quiescent Current vs Temperature

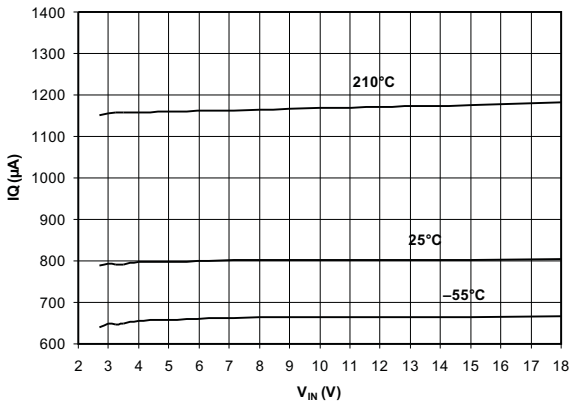


Figure 12. Quiescent Current vs Input Voltage

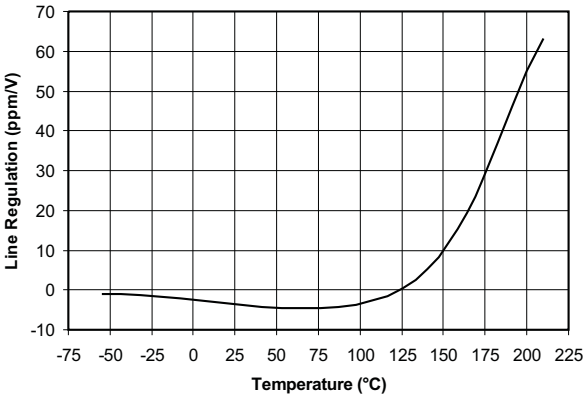


Figure 13. Line Regulation vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, I_{LOAD} = 0, V_S = 3.25 V (unless otherwise noted).

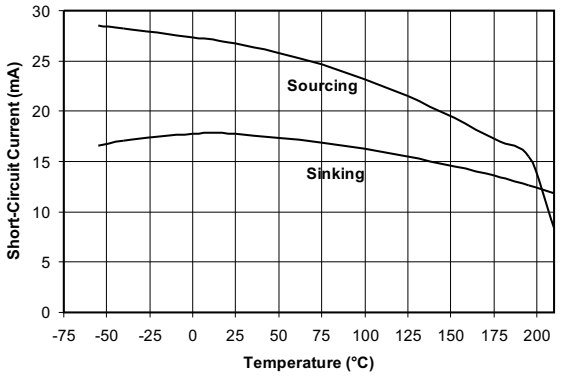


Figure 14. Short-Circuit Current vs Temperature

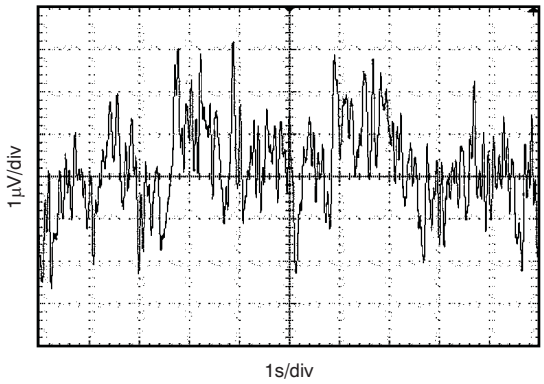
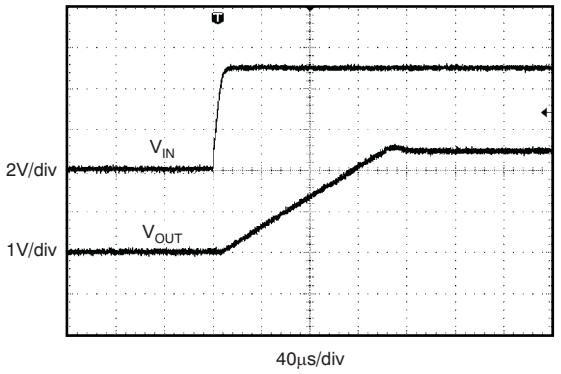
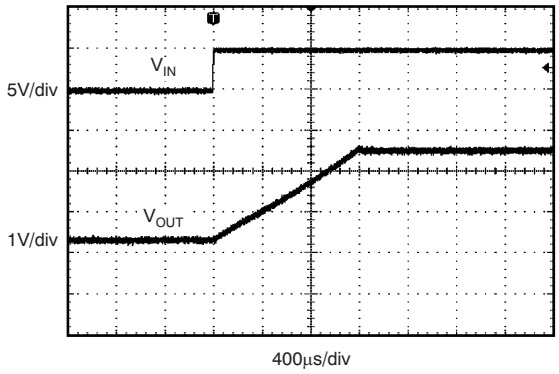


Figure 15. Noise



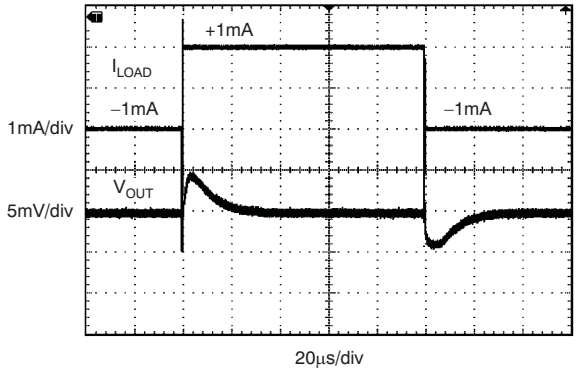
C_L = 1 µF

Figure 16. Start-Up (REF5025)



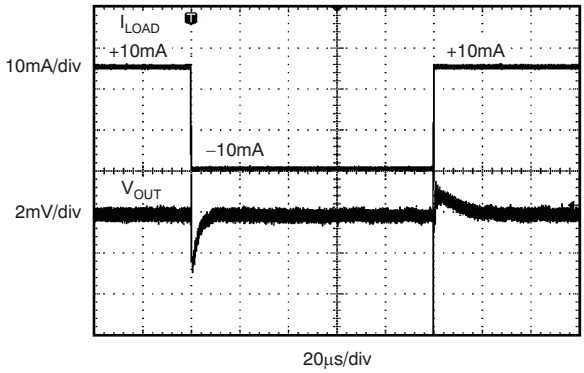
C_L = 10 µF

Figure 17. Start-Up (REF5025)



I_{OUT} = 1 mA C_L = 1 µF

Figure 18. Load Transient

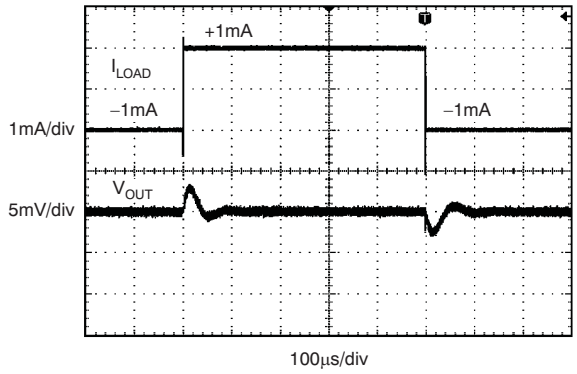


I_{OUT} = 10 mA C_L = 1 µF

Figure 19. Load Transient

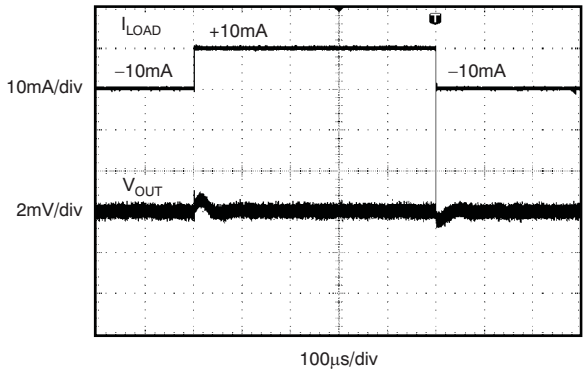
Typical Characteristics (continued)

at T_A = 25°C, I_{LOAD} = 0, V_S = 3.25 V (unless otherwise noted).



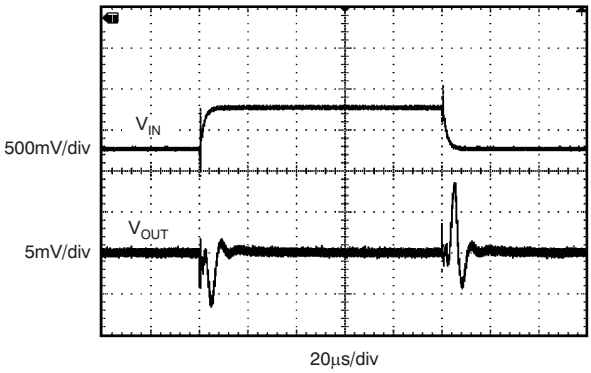
C_L = 10 µF I_{OUT} = 1 mA

Figure 20. Load Transient



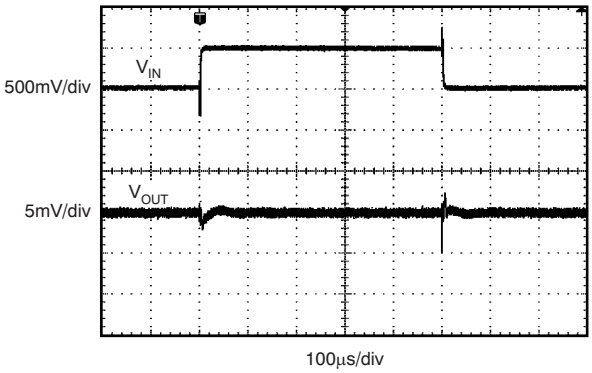
C_L = 10 µF I_{OUT} = 10 mA

Figure 21. Load Transient



C_L = 1 µF

Figure 22. Line Transient



C_L = 10 µF

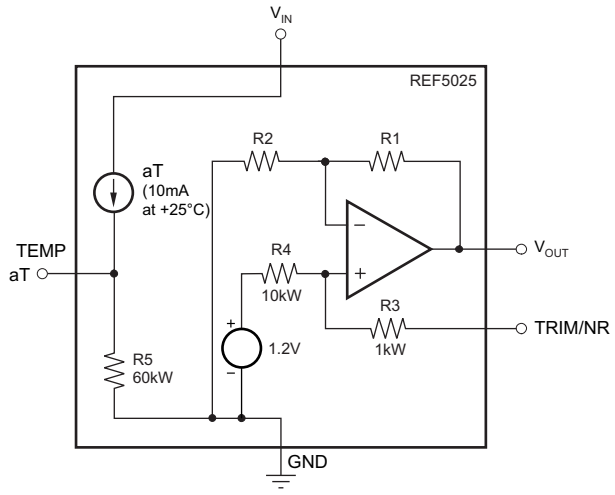
Figure 23. Line Transient

7 Detailed Description

7.1 Overview

The REF5025-HT devices are low-noise, low-drift, very high precision voltage references. These references can both sink and source, and are very robust with regard to line and load changes.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Adjustment Using the TRIM/NR Pin

The REF5025-HT provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 24 shows a typical circuit that allows an output adjustment of ±15 mV.

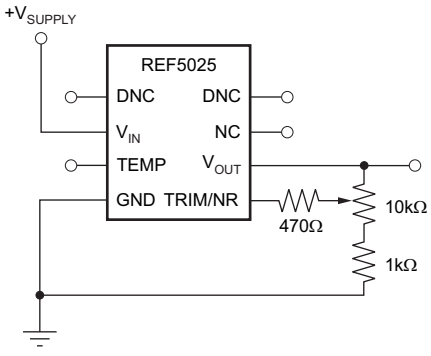


Figure 24. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF5025-HT allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see Figure 26) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1 μF creates a low-pass filter with the corner frequency between 10 Hz and 20 Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Use of this capacitor increases start-up time.

Feature Description (continued)

7.3.2 Low Temperature Drift

The REF5025-HT is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 1:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

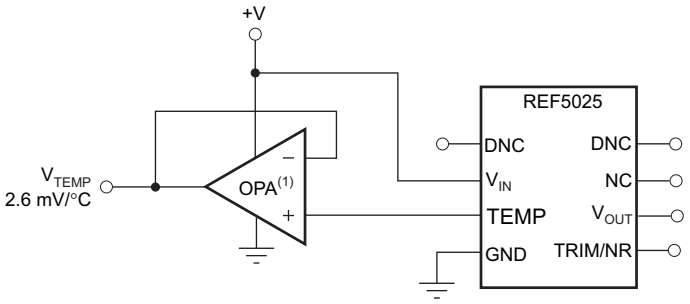
7.3.3 Temperature Monitoring

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As seen in Figure 10, the output voltage follows the nominal relationship:

$$V_{TEMP\ PIN} = 509\ \text{mV} + 2.64 \times T(°C) \quad (2)$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79 mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see *Functional Block Diagram*). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift operational amplifiers, such as the OPA333, OPA335, or OPA376, as shown in Figure 25.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 25. Buffering the TEMP Pin Output

7.3.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise the REF5025-HT is specified in the *Electrical Characteristics* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can improve output noise levels, although take care to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, see *Analog Applications Journal* articles entitled *How a Voltage Reference Affects ADC Performance. Part 1* (SLYT331), *How the Voltage Reference Affects ADC Performance, Part 2* (SLYT339), and *How the Voltage Reference Affects ADC Performance, Part 3* (SLYT355). This three-part series is available for download from the TI website.

Feature Description (continued)

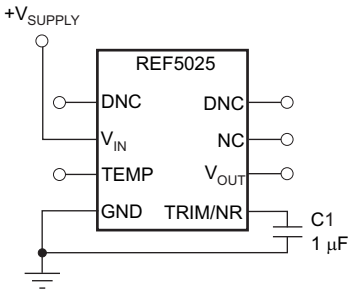


Figure 26. Noise Reduction Using the TRIM/NR Pin

7.4 Device Functional Modes

The REF5025-HT is powered on when the voltage on the VIN pin is greater than 3.25 V. The maximum input voltage for the REF5025-HT is 18 V. Use a supply bypass capacitor with a value ranging from 1 µF to 10 µF. The total capacitive load at the output must be between 1 µF to 50 µF to ensure the best output stability.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The REF5025-HT device is a low-noise, precision bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. See the *Functional Block Diagram*.

When designing circuits with a voltage reference, output noise is one of the main concerns. The main source of voltage noise in the reference voltages originates from the bandgap and output amplifier, which contribute significantly to the overall noise. During the design process, it is important to minimize these sources of voltage noise.

8.2 Typical Applications

8.2.1 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF5025-HT and OPA735 can provide a dual-supply reference from a 5-V supply. Figure 27 shows how the REF5025-HT provides a 2.5-V supply reference voltage. The low-drift performance of the REF5025-HT complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R_1 and R_2.

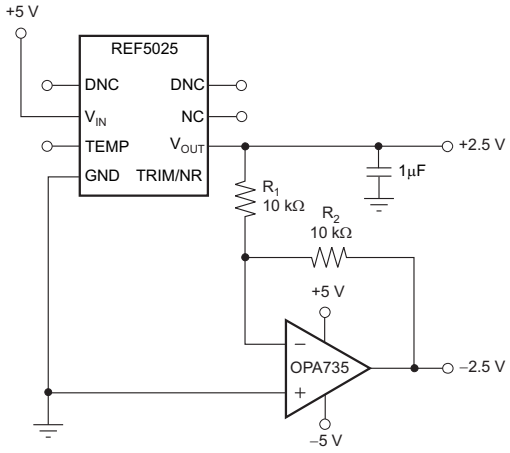


Figure 27. The REF5025-HT and OPA735 Create Positive and Negative Reference Voltages

8.2.1.1 Design Requirements

When using REF5025-HT in the design, it is important to select a proper capacitive load that do not create gain peaking adding noise to the output voltage. At the same time, the capacitor must be selected to provide required filtering performance for the system. Input bypass capacitor and noise reduction capacitors must be added for optimum performances.

8.2.1.2 Detailed Design Procedure

Proper design procedure will require first to select output capacitor. If the ESR of the capacitor is not in 1-Ω range additional resistor must be added in series with the load capacitor. Next, add a 1-µF capacitor to the NR pin to reduce internal noise of the REF5025-HT. Measuring output noise will confirm if the design has met the initial target.

Typical Applications (continued)

8.2.1.3 Application Curves

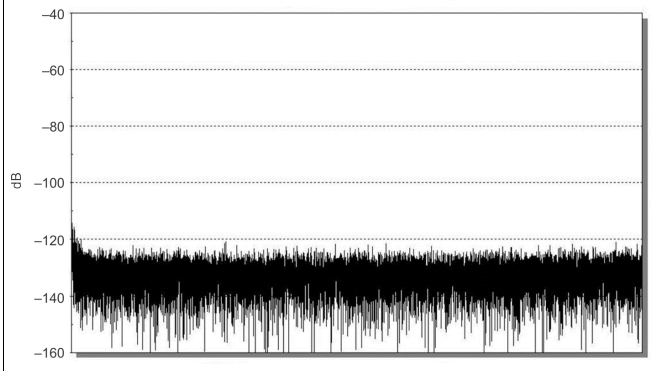


Figure 28. Noise Measurements of Properly Design REF5025 Data Acquisition System From Figure 35

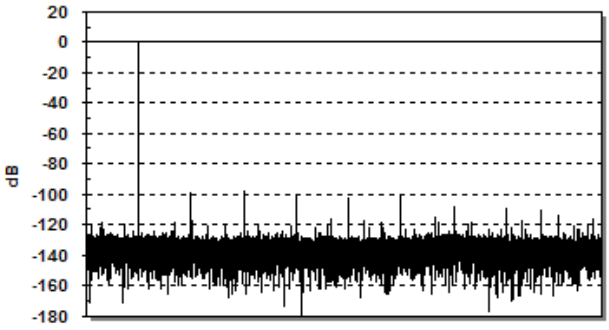


Figure 29. FFT of Data Acquisition System Design With REF5025 From Figure 35

8.2.2 Positive Reference Voltage

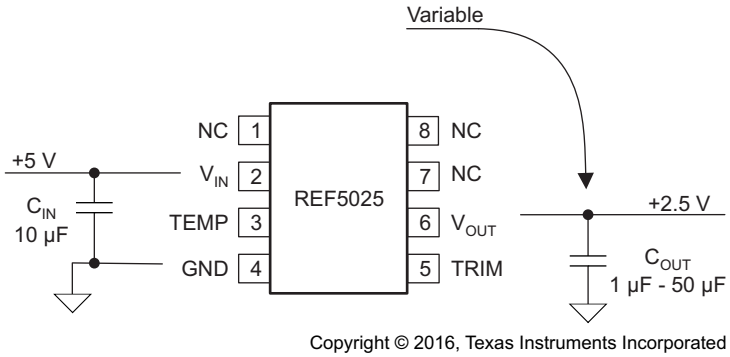


Figure 30. REF5025-HT With Load Capacitor

8.2.2.1 Detailed Design Procedure

8.2.2.1.1 Load Capacitance

To determine how much noise the reference voltage is contributing in a real application, this design uses the circuit presented in Figure 30. For the same conditions as power supply, input decoupling, and load current, measure the output noise for different output decoupling or load capacitors. The load capacitor type will change the low-pass filter frequency that is created on the output. This filter is determined by an added capacitor value and two parasitic components: the open-loop output impedance of the internal amplifier to the reference voltage, and the ESR of the external capacitor.

Figure 31 shows a fast-Fourier-transform (FFT) plot of the output signal of the reference voltage circuit with a 10-µF ceramic capacitor load. The output noise level peaks at around 9 kHz because of the response of the internal amplifier of the circuit to the capacitive load (C_L).

This peaking is the main contributor to the overall measured noise. This output noise, measured with an analog meter over a frequency range of up to 80 kHz, is approximately 16.5 µVRMS. If the voltage-reference circuit was connected to the input of an ADC, the measured noise across a 65-kHz frequency range would be 138 µVPP. This noise level makes this solution adequate for 8- to 14-bit converters.

Typical Applications (continued)

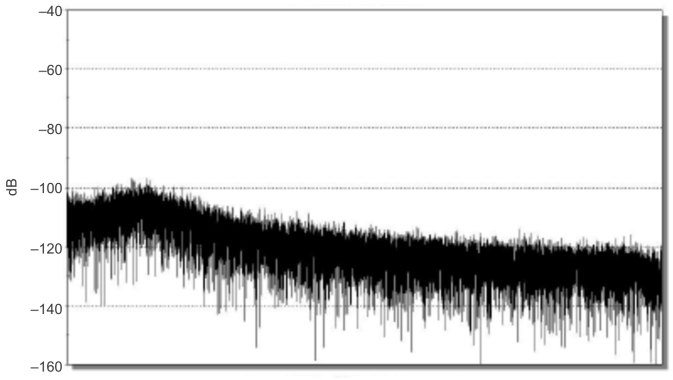
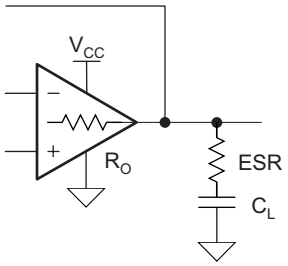


Figure 31. REF5025 FFT Plot of the Noise With 10-µF Load Capacitor and 10-µΩ ESR

Every capacitor can be represented with a complicated equivalent model, which is voltage and frequency dependent with a large number of passive components. For the purposes of this design, this model is limited to the few components. The biggest impact on the creation of the low-pass filter and stability analysis is the simplified model of equivalent series inductance and resistance. Considering good layout practice and inherently low equivalent series inductance of today's components, this model in the future analysis will be presented only by equivalent capacitance and series resistance.



$$f_P = \frac{1}{2\pi \bullet (R + ESR) \bullet C_L}$$

$$f_Z = \frac{1}{2\pi \bullet ESR \bullet C_L}$$

Figure 32. Equivalent SCH of REF5025 With Load Capacitor for Stability Analysis

When evaluating the impact of ESR and C_L on the performance the reference voltage, it is important to include the effect of the open-loop output resistance (R_O) of the output amplifier. The combination of R_O, ESR, and C_L modifies the open-loop response curve by introducing one pole (f_P) and one zero (f_Z). The values R_O, ESR, and C_L determine the corner frequency of the added pole f_P; and the values of ESR and C_L determine the corner frequency of the added zero.

The introduction of the external ESR-CL on the output of the reference voltage modifies the output amplifier open-loop gain curve. The added pole modifies the open-loop gain curve of the reference voltage output amplifier by introducing a –20 dB/decade change at the frequency f_P to the already –20 dB/decade slope of the open-loop gain curve, making the slope equal to –40 dB/decade. The added zero at frequency f_Z changes the open-loop gain curve back to –20 dB/decade.

Typical Applications (continued)

Table 1. Noise Measurement Results for Different Load Capacitors

NOISE	22 kHz LP-5P	30 kHz LP-3P	80 kHz LP-3P	> 500 kHz	UNIT
GND	0.8	1	1.8	4.9	μV_{RMS}
1 µF	37.8	41.7	53.7	9017	
2.2 µF (cer)	41.7	46.2	55.1	60.8	
10 µF	33.4	33.4	35.2	38.5	
10 µF (cer)	37.1	37.2	37.8	39.1	
20 µF (cer)	33.1	33.1	33.2	34.5	
47 µF	23.2	23.8	24.1	26.5	

Table 1 shows the measured noise values for different frequency bandwidths as well as different values and types of external capacitors. These measurements show that low-ESR (approximately 100-mΩ) ceramic capacitors tend to increase the noise, compared to normal-ESR (approximately 2-Ω) tantalum capacitors. This tendency is caused by a stability issue with the output amplifier and gain peaking in the amplifier frequency response.

8.2.2.1.2 Bandgap Noise Reduction

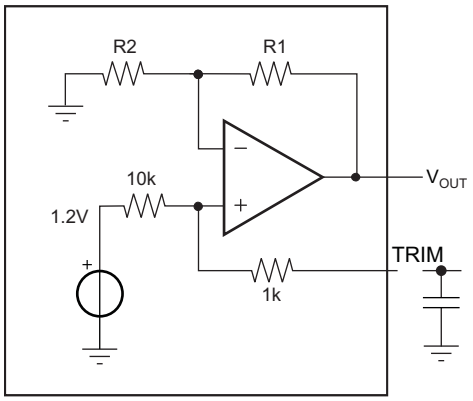


Figure 33. REF5025-HT Internal Structure of Trim/NR Pin

The internal schematic of the REF5025-HT device shows that the trim pin allows direct access to the bandgap output. Figure 33 shows the trim pin connection to the internal bandgap circuit through a resistor. Adding a capacitor on the trim pin creates a lowpass filter that has a broadband attenuation of −21 dB.

For example, a small 1-µF capacitor adds a pole at 14.5 Hz and a zero at 160 Hz. If more filtering is needed, a larger value capacitor can be added, which will lower the filter cutoff frequency and the noise contributed by the bandgap.

Table 2. Measured Noise (μV_{RMS}) for Four Bandwidths

NOISE	22 kHz (LOW-PASS 5-POLE)	30 kHz (LOW-PASS 3-POLE)	80 kHz (LOW-PASS 3-POLE)	> 500 kHz	UNIT
GND	0.8	1	1.8	4.6	μV_{RMS}
2.2 µF (ceramic)	42.5	47.2	61.2	68.3	
2.2 µF + 1 µF	17.5	19.4	22.6	24.5	
10 µF (ceramic)	34.4	35.6	37.7	44.5	
10 µF + 1 µF	14.1	14.4	14.9	16.4	
20 µF (ceramic)	34.8	34.9	35.1	35.2	
20 µF + 1 µF	14.4	14.4	14.7	15.1	

Adding a 1-µF capacitor in this example filters the noise contribution of the bandgap and lowers the total noise by a factor of 2.5 times.

8.3 System Example

8.3.1 Data Acquisition

Data acquisition systems often require stable voltage references to maintain accuracy. The REF5025-HT family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 34 shows the REF5040 as an example in a basic data acquisition system. The same principle can be applied when designing with REF5025-HT.

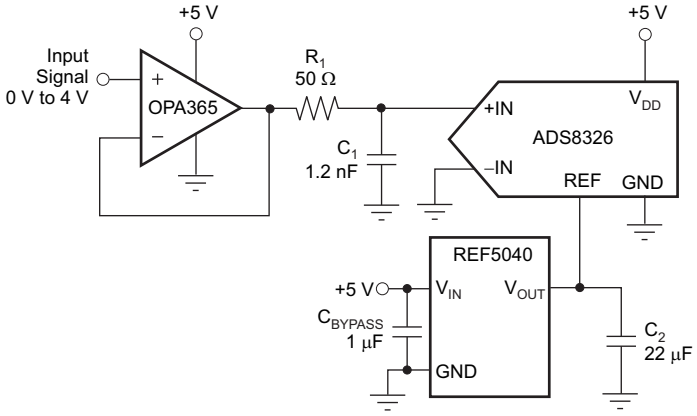


Figure 34. Basic Data Acquisition System

During the design of the data acquisition system, equal consideration must be given to the buffering analog input signal as well as the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement, but does not ensure the maximum performance.

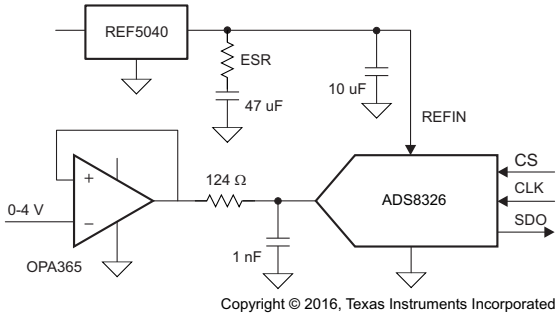


Figure 35. Complete Data Acquisition System Using REF50xx

System Example (continued)

Three measurements using different components of the output are shown for this data acquisition system.

Table 3 shows improvements on the FFT for a properly designed system.

Table 3. Data Acquisition Measurement Results for Different Conditions

OPA365 REF5040 TRIM	124 Ω, 1 nF 10 µF 0 µF	124 Ω, 1 nF 10 µF + 47 µF 1 µF	124 Ω, 100 µF 10 µF + 47 µF 1 µF	UNIT
Resolution	16	16	16	Bits
States	65536	65536	65536	
V_{REF}	4.096	4.096	4.096	V
LSB	62.5	62.5	62.5	µV
V_{IN}	4.02	4.02	4.02	V
Data Std	1.07	0.53	0.41	LSB
Noise	67.0	33.4	25.8	μV_{RMS}
Noise	442.3	220.5	170.2	μV_{PP}
SNR	86.7	92.8	95.0	dB
FTT Points	32768	32768	32768	
Noise Flor	–128.8	–134.9	–131.7	dB

Once the correct components for data acquisition system from Figure 35 are selected, measurement results can be compared to the ADS8326 data sheet specifications.

Table 4. AC Performance for Data Acquisition System From Figure 35

REF5040 TRIM	ADS8326 DATA SHEET	ADS8326B DATA SHEET	SYSTEM LOW ESR	SYSTEM 10 µF + 47 µF 1µF	UNIT
SNR	91	91.5	90.6	92.2	dB
SINAD	87.5	88	85.7	89.5	dB
SFDR	94	95	88.3	98.4	dB
THD	–90	–91	–87.3	–92.9	dB
ENOB	14.28	14.35	13.94	14.58	Bits

9 Power Supply Recommendations

The minimum recommended power supply voltage for REF5025-HT is 3.25 V. The maximum power supply voltage for the REF5025-HT is 18 V. TI recommends adding a bypass capacitor of 1 μF to 10 μF at the input to compensate for the layout and power supply source impedance.

Figure 36 shows the typical connections for the REF5025-HT. TI recommends a supply bypass capacitor with a value ranging from 1 μF to 10 μF. A 1-μF to 50-μF output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value of C_L must be less than or equal to 1.5-Ω to ensure output stability. To minimize noise, TI recommends the ESR value of the of C_L is between 1-Ω and 1.5-Ω.

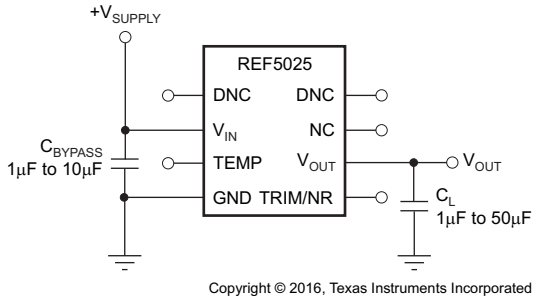


Figure 36. Basic Connections

10 Layout

10.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the VIN pin and ground pins. TI recommends a bypass capacitor value of 1 µF to 10 µF. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Place a 1-µF noise filtering capacitor between the NR pin and ground.
- The output must be decoupled with a 1-µF to 50-µF capacitor. In series with the load capacitor, add an ESR of 1-Ω for the best noise performance.
- A high-frequency, 1-µF capacitor can be added in parallel between the output and ground to filter noise and help with switching loads as data converters.

10.2 Layout Example

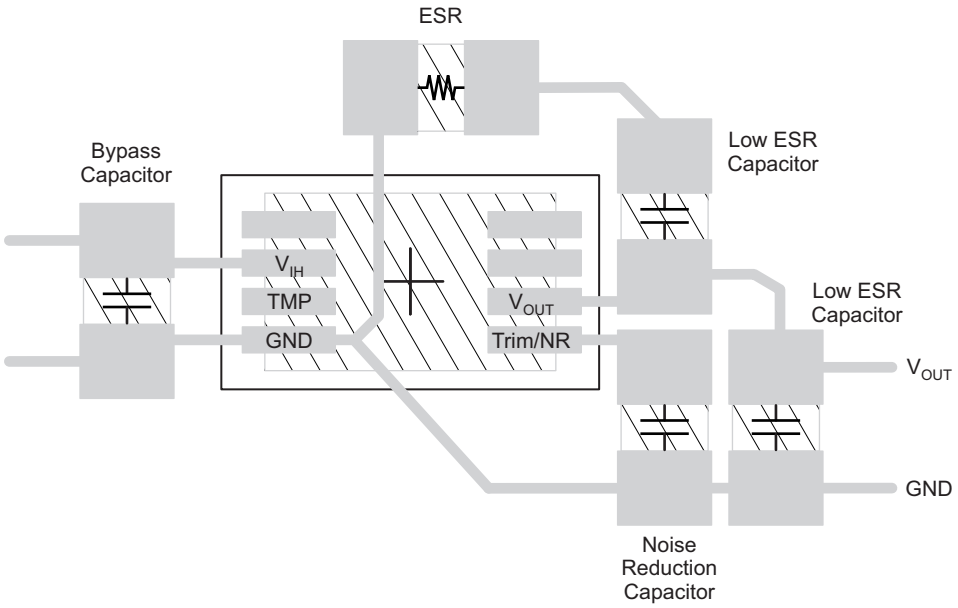


Figure 37. Recommended Layout for REF5025-HT

10.3 Power Dissipation

The REF50xx family is specified to deliver current loads of ±10-mA over the specified input voltage range. The temperature of the device increases according to Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

Where:

- T_J = Junction temperature (°C)
- T_A = Ambient temperature (°C)
- P_D = Power dissipated (W)
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of +150°C.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *0.05uV/degC (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier* (SBOS282)
- *REF5020 PSpice Model* (SLIM160)
- *REF5020 TINA-TI Reference Design* (SLIM159)
- *REF5020 TINA-TI Spice Model* (SLIM158)
- *INA270 PSpice Model* (SBOM485)
- *INA270 TINA-TI Reference Design* (SBOC246)
- *INA270 TINA-TI Spice Model* (SBOM306)
- *How a Voltage Reference Affects ADC Performance* (SLYT331)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5025SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	REF5025S HKJ	Samples
REF5025SHKQ	ACTIVE	CFP	HKQ	8	25	TBD	AU	N / A for Pkg Type	-55 to 210	REF5025S HKQ	Samples
REF5025SKGD1	ACTIVE	XCEPT	KGD	0	195	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples
REF5025SKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

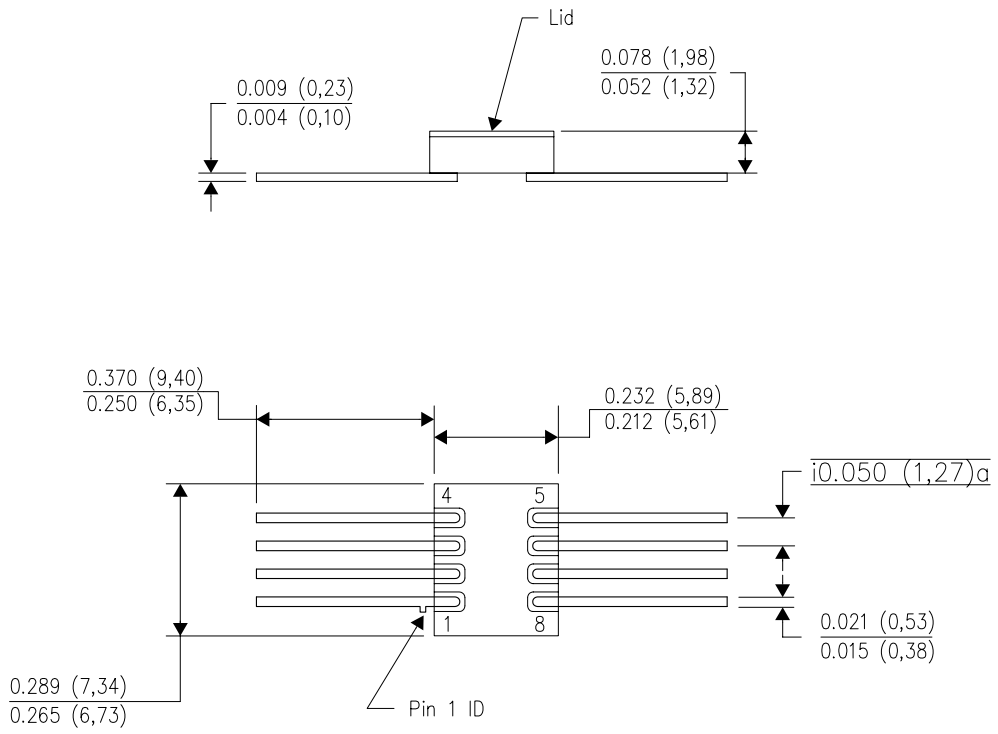
OTHER QUALIFIED VERSIONS OF REF5025-HT :

- Catalog: REF5025
- Enhanced Product: REF5025-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
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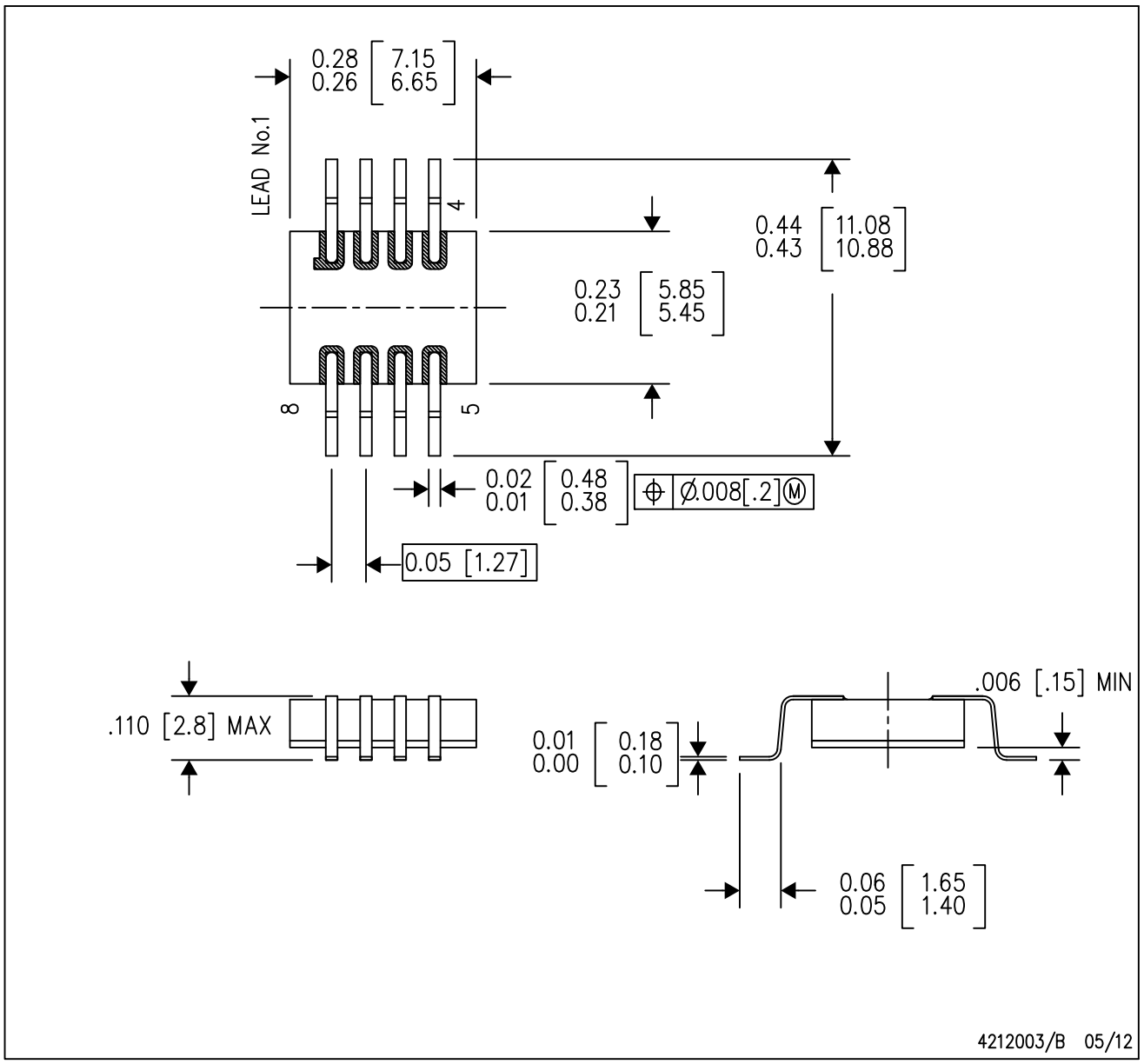
D. The terminals will be gold plated.

HKQ (R–CDFP–G8) CERAMIC GULL WING



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D. The terminals will be gold plated.
E. Lid is not connected to any lead.

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