集成 VCO 的高性能宽带 PLLatinum™ RF 合成器 LMX2592

1 特性

- 输出频率范围从 20 至 9800MHz
- 相位噪声性能行业领先
  - 压控振荡器 (VCO) 的相位噪声：在 1MHz 偏移时为 –134.5dBc/Hz（对于 6GHz 输出）
  - 标准化锁相环 (PLL) 噪底：–231dBc/Hz
  - 标准化 PLL 闪烁噪声：-126dBc/Hz
  - 49fs 均方根 (RMS) 抖动（12kHz 至 20MHz）（对于 6GHz 输出）
- 输入时钟频率高达 1400MHz
- 相位检测器频率高达 200MHz，在整数 N 模式中高达 400MHz
- 支持分数 N 和整数 N 模式
- 双差分输出
- 减少毛刺的创新型解决方案
- < 25µs 快速校准模式
- 可编程相位调整
- 可编程电荷泵电流
- 可编程输出功率水平
- 串行外设接口 (SPI) 或 uWire（4 线制串行接口）
- 单电源供电：3.3V

2 应用

- 测试/测量设备
- 国防和雷达
- 微波回程
- 高速数据转换器的高性能时钟源
- 卫星通信

3 说明

LMX2592 是一款集成 VCO 的低噪声、宽带射频 (RF) PLL，支持的频率范围为 20MHz 至 9.8GHz。该器件支持分数 N 和整数 N 模式，具有一个 32 位小数分频器，可提供精确频率选择。其积分噪声为 49fs 的噪声（对于 6GHz 输出），是理想的低噪声源。该器件融入了一流的 PLL 和 VCO 积分噪声与集成的低压线性稳压器 (LDO)，从而无需高性能系统中的多个分立器件。

该器件可接受高达 1.4GHz 的输入频率，与分频器及可编程低噪声乘法器相结合，可灵活设置频率。增加可编程低噪声乘法器可帮助用户去除整数边界毛刺的影响。在分数 N 模式下，该器件可将输出相位调整 32 位分辨率。对于 需要快速切换频率的应用， 该器件支持耗时小于 25us 的快速校准选项。

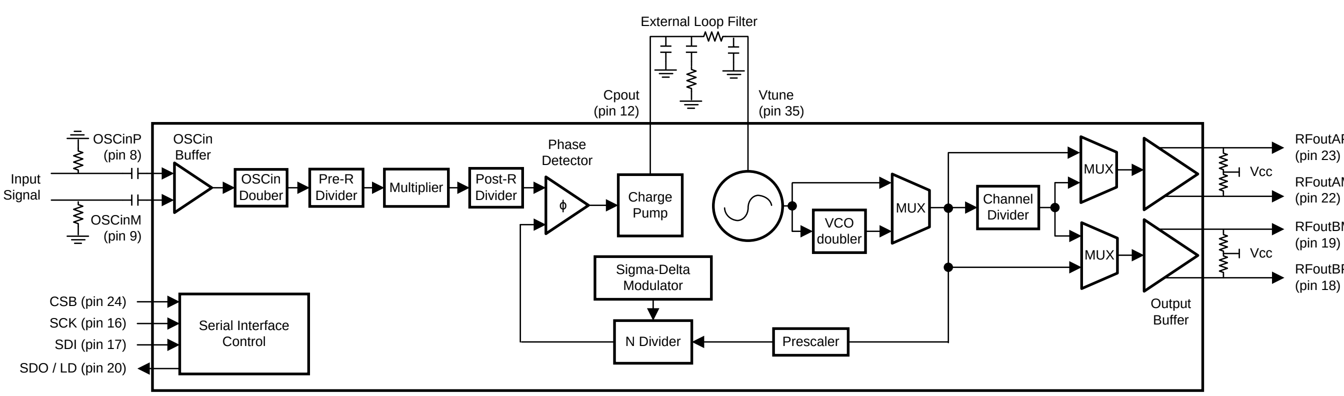
使用一个 3.3V 电源即可能实现此性能。该器件支持 2 个差分输出，这两个输出也可灵活配置为单端输出。用户可选择将其中一个编程为从 VCO （或倍压器）输出，另一个从通道分配器输出。若不想使用，可分别禁用每个输出。

器件信息 (1)

部件号	说明	封装尺寸（标称值）
LMX2592RHAT LMX2592RHAR	WQFN (40)	6mm x 6mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。
(2) T = 带；R = 卷

简化电路原理图



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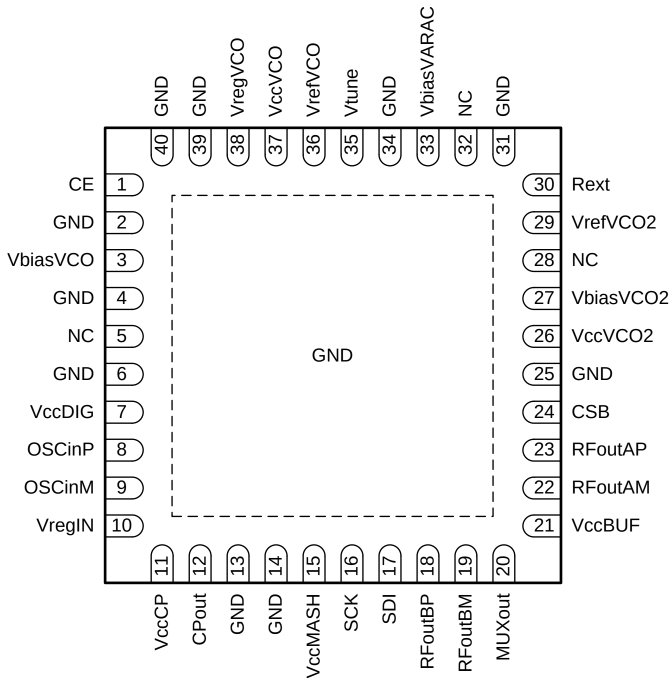
4 修订历史记录

Changes from Original (December 2015) to Revision A — **Page**

- 已将器件状态从产品预览更改为量产数据，并且已发布完整数据表 1

5 Pin Configuration and Functions

RHA Package
40-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CE	1	Input	Chip Enable input. Active high powers on the device.
GND	2	Ground	VCO ground.
VbiasVCO	3	Bypass	VCO bias internal voltage, access for bypass. Requires connecting 10-µF capacitor to VCO ground. Place close to pin.
GND	4	Ground	VCO ground.
NC	5	—	Not connected.
GND	6	Ground	Digital ground.
V_{CC}DIG	7	Supply	Digital supply. Recommend connecting 0.1-µF capacitor to digital ground.
OSCinP	8	Input	Differential reference input clock (+). High input impedance. Requires connecting series capacitor (0.1-µF recommended).
OSCinM	9	Input	Differential reference input clock (-). High input impedance. Requires connecting series capacitor (0.1-µF recommended).
VregIN	10	Bypass	Input reference path internal voltage, access for bypass. Requires connecting 1-µF capacitor to ground. Place close to pin.
V_{CC}CP	11	Supply	Charge pump supply. Recommend connecting 0.1-µF capacitor to charge pump ground.
CPout	12	Output	Charge pump output. Recommend connecting C1 of loop filter close to pin.
GND	13	Ground	Charge pump ground.
GND	14	Ground	Digital ground.
V_{CC}MASH	15	Supply	Digital supply. Recommend connecting 0.1-µF and 10-µF capacitor to digital ground.
SCK	16	Input	SPI or uWire clock. High impedance CMOS input. 1.8 to 3.3-V logic.
SDI	17	Input	SPI or uWire data. High impedance CMOS input. 1.8 to 3.3-V logic.
RFoutBP	18	Output	Differential output B (+). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RFoutBM	19	Output	Differential output B (-). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
MUXout	20	Output	Programmable with register MUXOUT_SEL to be readback SDO or lock detect indicator (active high).
V_{CC}BUF	21	Supply	Output buffer supply. Requires connecting 0.1-µF capacitor to RFout ground.
RFoutAM	22	Output	Differential output A (-). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
RFoutAP	23	Output	Differential output A (+). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
CSB	24	Input	SPI chip select bar or uWire latch enable. High impedance CMOS input. 1.8 to3.3-V logic.
GND	25	Ground	VCO ground.
V_{CC}VCO2	26	Supply	VCO supply. Recommend connecting 0.1-µF and 10-µF capacitor to VCO ground.
VbiasVCO2	27	Bypass	VCO bias internal voltage, access for bypass. Requires connecting 1-µF capacitor to VCO ground.
NC	28	—	Not connected.
VrefVCO2	29	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 10-µF capacitor to VCO ground.
Rext	30	Bypass	External resistor connection. Requires connecting 680-Ω resistor to ground.
GND	31	Ground	VCO ground.
NC	32	—	Not connected.
VbiasVARAC	33	Bypass	VCO varactor internal voltage, access for bypass. Requires connecting 10-µF capacitor to VCO ground.
GND	34	Ground	VCO ground.
Vtune	35	Input	VCO tuning voltage input. This signal should be kept away from noise sources.
VrefVCO	36	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 10-µF capacitor to ground.
V_{CC}VCO	37	Supply	VCO supply. Recommend connecting 0.1-µF and 10-µF capacitor to ground.
VregVCO	38	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 1-µF capacitor to ground.
GND	39	Ground	VCO ground.
GND	40	Ground	VCO ground.
GND	DAP	Ground	RFout ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
V_{IN}	Input voltage to pins other than V_{CC} pins	–0.3	V_{CC} + 0.3	V
V_{OSCin}	Voltage on OSCin (pin 8 and pin 9)	≤1.8 with V_{CC} Applied, ≤1 with V_{CC}=0		Vpp
T_L	Lead temperature (solder 4 sec.)		260	°C
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1250	
		Machine model (MM) ESD stress voltage	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1250 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.15		3.45	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMX2592 RHA (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C.
Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{CC}	Supply voltage			3.3		V
I_{CC}	Supply current	Single 6-GHz, 0-dBm output(1)		250		mA
I_{PD}	Power down current			3.7		mA
Output Characteristics						
F_{out}	Output frequency		20		9800	MHz
P_{out}	Typical high output power	Output = 3 GHz, 50-Ω pull-up, single ended(2)		8		dBm
Input Signal Path						
REFin	Maximum reference input frequency		5		1400	MHz
REFv	Reference input voltage	AC coupled, differential(3)	0.2		2	Vppd
MULin	Input signal path multiplier input frequency		40		70	MHz
MULout	Input signal path multiplier output frequency		180		250	MHz
Phase Detector and Charge Pump						
PDF	Phase detector frequency		5		200	MHz
		Extended range mode(4)	0.25		400	MHz
CPI	Charge pump current	Programmable		0 to 12		mA
PLL Phase Noise						
PLL_flicker_Norm	Normalized PLL Flicker Noise(5)			–126		dBc/Hz
PLL_FOM	Normalized PLL Noise Floor (PLL Figure of Merit)(5)			–231		dBc/Hz
VCO						
$\|\Delta T_{CL}\|$	Allowable temperature drift(6)	VCO not being re-calibrated			125	°C

(1) For typical total current consumption of 250 mA: 100 MHz input frequency, OSCin doubler bypassed, pre-R divider bypassed, multiplier bypassed, post-R divider bypassed, 100MHz phase detector frequency, 0.468mA charge pump current, channel divider off, one output on, 6GHz output frequency, 50-Ω output pull-up, 0 dBm output power (differential). See Applications section for more information.
(2) For a typical high output power for a single-ended output, with 50-Ω pull-up on both M and P side, register OUTx_POW = 63. Un-used side terminated with 50-Ω load.
(3) There is internal voltage biasing so the OSCinM and OSCinP pins should always be AC coupled (capacitor in series). Vppd is differential peak-to-peak voltage swing. If there is a differential signal (two are negative polarity of each other), the total swing is one subtracted by the other, each should be 0.1 to 1-Vppd. If there is a single-ended signal, it can have 0.2 to 2Vppd. See Detailed Description and Applications section for more information.
(4) To use phase detector frequencies lower than 5 MHz set register FCAL_LPFD_ADJ = 3. To use phase detector frequencies higher than 200MHz, you must be in integer mode, set register PFD_CTL = 3 (to use single PFD mode), set FCAL_HPFD_ADJ = 3. To see more information go to Detailed Description section.
(5) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20*log(Fvco/Fpd) + 10*log(Fpd / 1Hz). PLL_flicker (offset) = PLL_flicker_Norm + 20*log(Fvco / 1GHz) – 10*log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = $10 \cdot \log(10^{PLL\_Flat / 10} + 10^{PLL\_flicker / 10})$.
(6) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift without reprogramming the device, and still have the device stay in lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.

Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C.
Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$PN_{open\ loop}$	Output = 3 GHz	100 kHz			–118.8		dBc/Hz
		1 MHz			–140.3		
		10 MHz			–155.1		
		100 MHz			–156.3		
	Output = 6 GHz	100 kHz			–112.6		
		1 MHz			–134.2		
		10 MHz			–152.6		
		100 MHz			–156.2		
	Output = 9.8 GHz	100 kHz			-108.2		
		1 MHz			-129.1		
		10 MHz			-140.5		
		100 MHz			-141.1		
Harmonic Distortion(7)							
HD_fund	Harmonic Distortion fundamental feed-through with doubler enabled	8 GHz, VCO doubler enabled	Fundamental (4 GHz)		–26		
Digital Interface							
V_{IH}	High level input voltage			1.8		V_{CC}	V
V_{IL}	Low level input voltage			0		0.4	V
I_{IH}	High level input current			-25		25	uA
I_{IL}	Low level input current			-25		25	uA
V_{OH}	High level output voltage	Load/Source Current of –350 µA			V_{CC} - 0.4		V
V_{OL}	Low level output voltage	Load/Sink Current of 500 µA			0.4		V
SPIW	Highest SPI write speed				75		MHz
SPIR	SPI read speed				50		MHz

(7) Not tested in production. Typical numbers from characterization with output settings: 50-Ω pull-up, OUTA_POW=15, channel divider off.

6.6 Timing Requirements

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C, except as specified. Typical values are at V_{CC} = 3.3 V, T_A = 25°C

			MIN	TYP	MAX	UNIT
Microwire Timing						
tES	Clock to enable low time	See Figure 1		5		ns
tCS	Data to clock setup time			2		ns
tCH	Data to clock hold time			2		ns
tCWH	Clock pulse width high			5		ns
tCWL	Clock pulse width low			5		ns
tCES	Enable to clock setup time			5		ns
tEWH	Enable pulse width high			2		ns

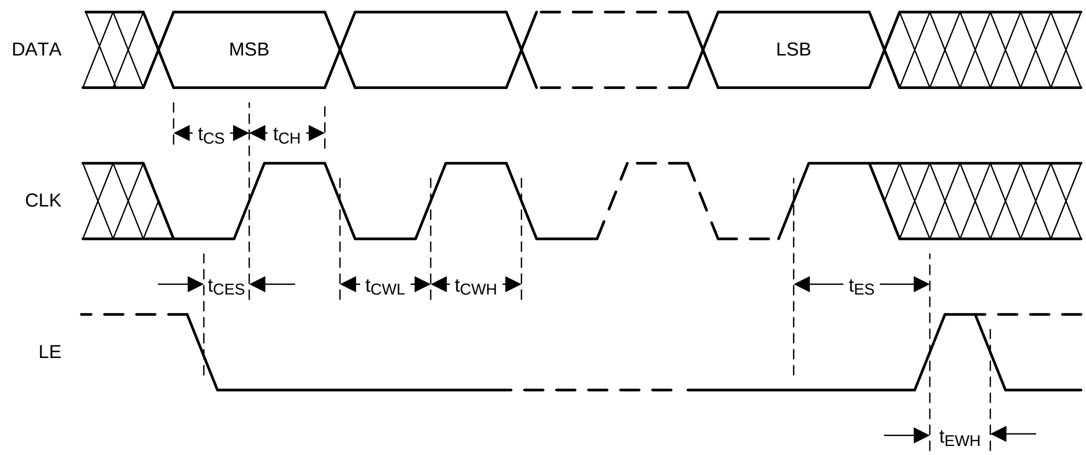


Figure 1. Serial Data Input Timing Diagram

There are several considerations for programming:

- A slew rate of at least 30 V/µs is recommended for the CLK, DATA, LE
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter
- The LE pin may be held high after programming and clock pulses will be ignored
- The CLK signal should not be high when LE transitions to low
- When CLK and DATA lines are shared between devices, it is recommended to divide down the voltage to the CLK, DATA and LE pins closer to the minimum voltage. This provides better noise immunity
- If the CLK and DATA lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming

6.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

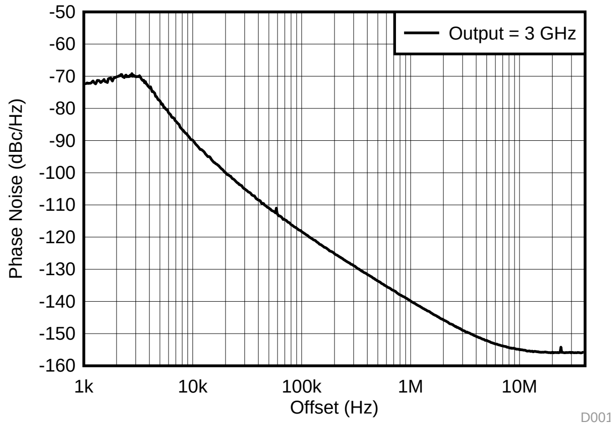


Figure 2. 3-GHz Output - Closed Loop Phase Noise

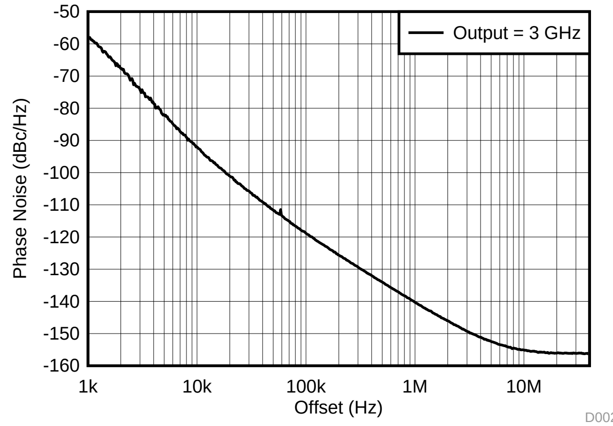


Figure 3. 3-GHz Output - Open Loop Phase Noise

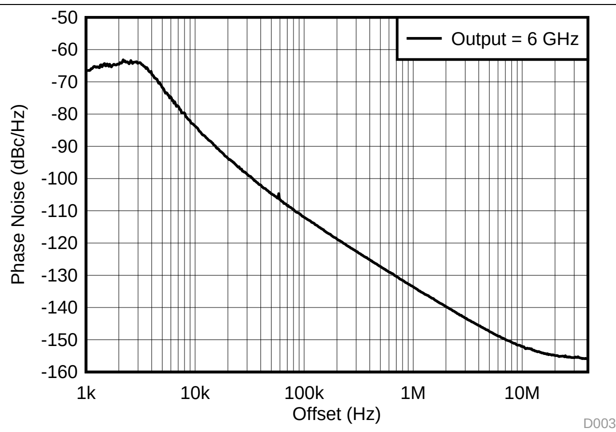


Figure 4. 6-GHz Output - Closed Loop Phase Noise

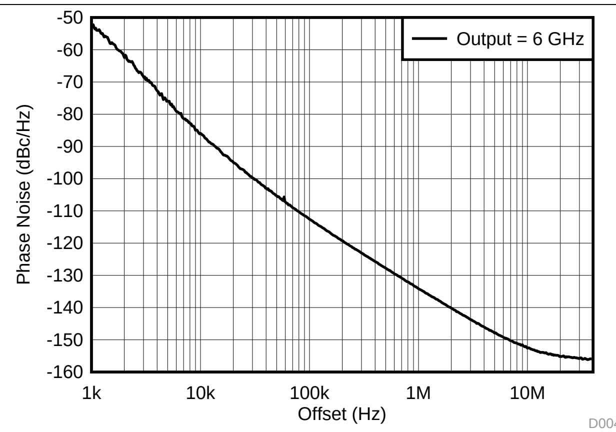


Figure 5. 6-GHz Output - Open Loop Phase Noise

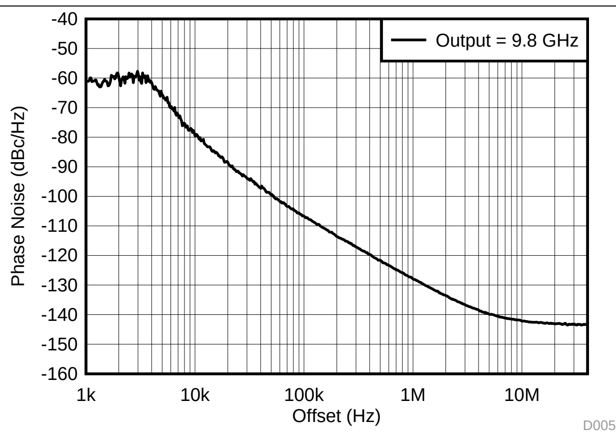


Figure 6. 9.8-GHz Output - Closed Loop Phase Noise

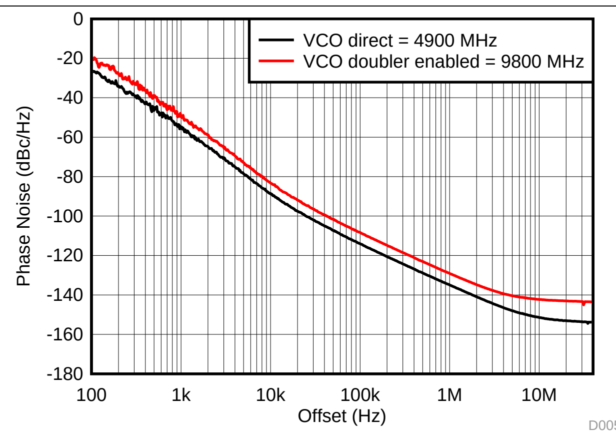


Figure 7. 9.8-GHz Output - Open Loop Phase Noise

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

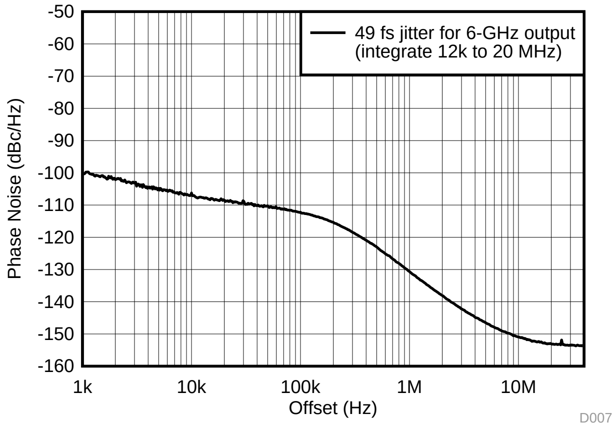


Figure 8. Integrated Jitter (49 fs) - 6-GHz Output

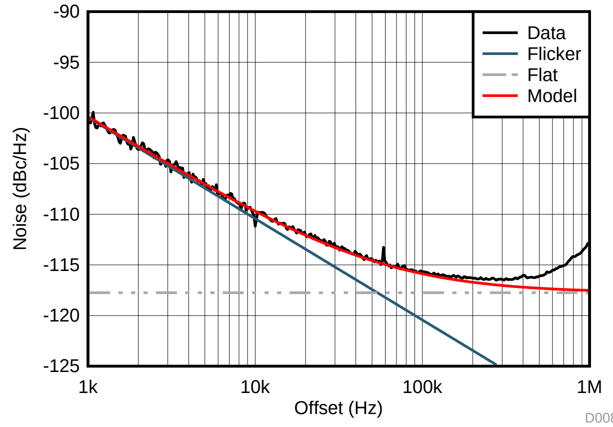


Figure 9. 6-GHz Output Wide Loop Bandwidth – Showing PLL Performance

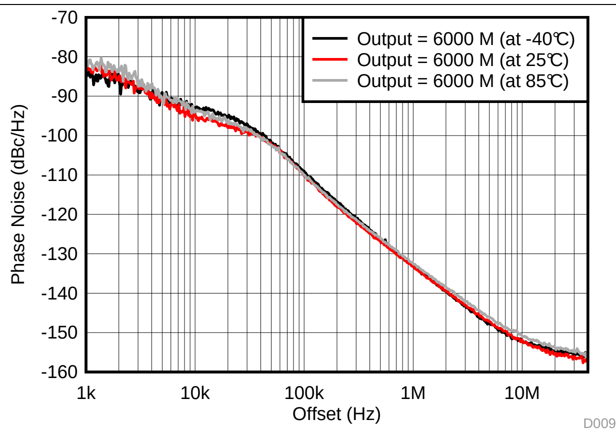


Figure 10. Variation of Phase Noise Across Temperature

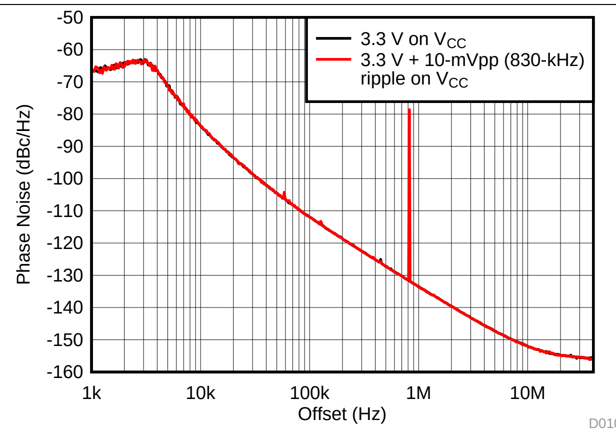


Figure 11. Impact of Supply Ripple on 6-GHz Output Phase Noise

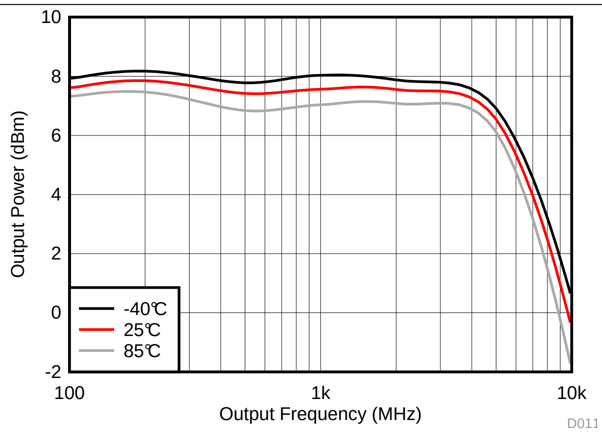


Figure 12. High Output Power (50-Ω Pull-Up, Single-Ended) vs Output Frequency

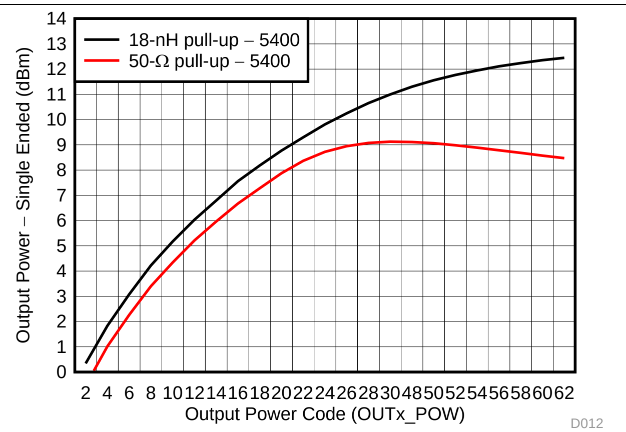


Figure 13. Output Power at 5.4-GHz Output vs OUTx_POW Code (1 - 31, 48 - 63)

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

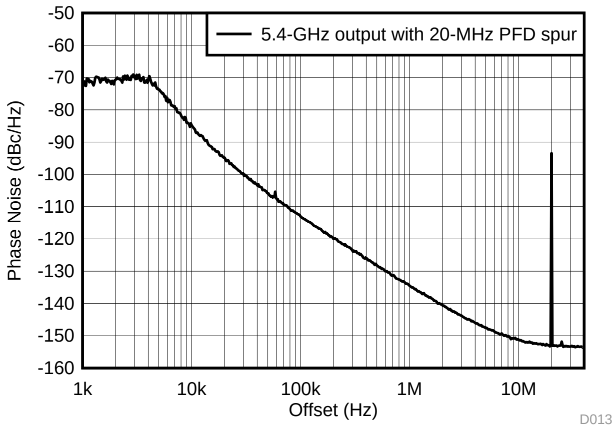


Figure 14. Typical PFD Spur for 5.4 GHz Output

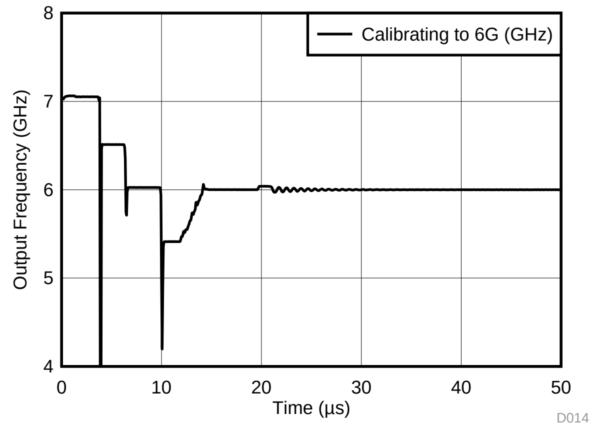


Figure 15. 20-µs Frequency Change Time to 6 GHz with Fast Calibration

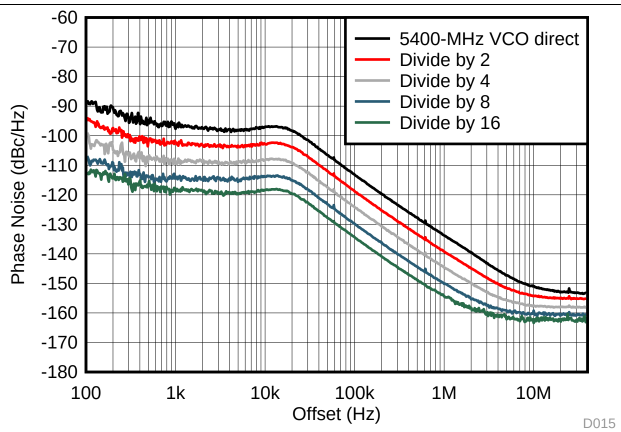


Figure 16. Impact of Channel Divider Settings on Phase Noise

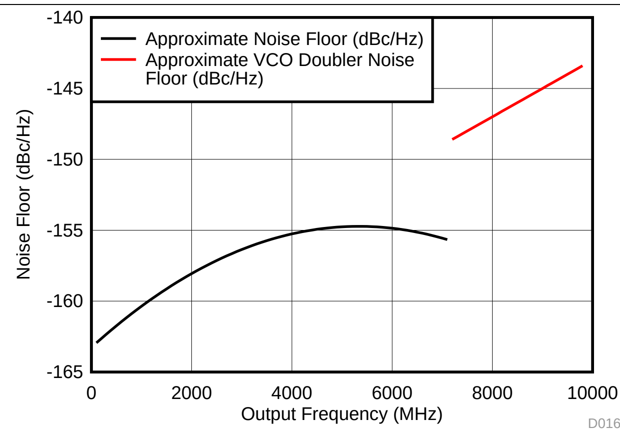


Figure 17. Noise Floor Variation with Output Frequency

7 Detailed Description

7.1 Overview

The LMX2592 is a high performance wideband synthesizer (PLL with integrated VCO). The output frequency range is from 20 MHz to 9.5 GHz. The VCO core covers an octave from 3.55 to 7.1 GHz. The output channel divider covers the frequency range from 20MHz to the low bound of the VCO core. The VCO-doubler covers the frequency range from the upper bound of the VCO to 9800MHz.

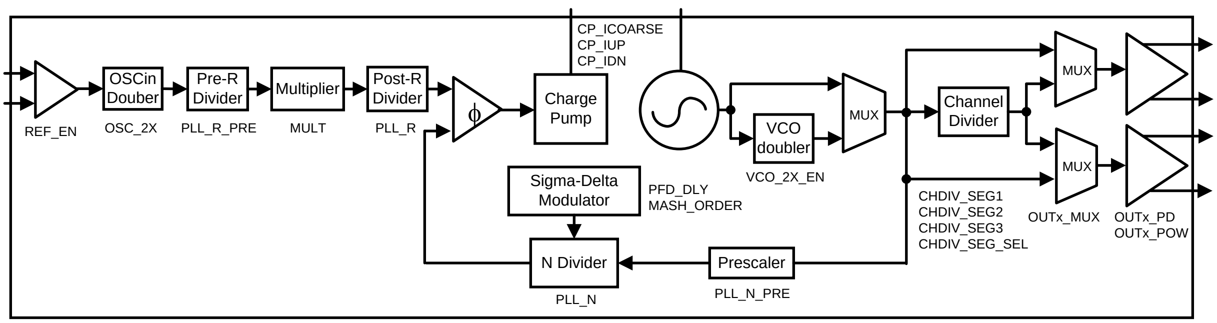
The input signal frequency has a wide range from 5 to 1400MHz. Following the input, there is an programmable OSCin doubler, a pre-R divider (previous to multiplier), a multiplier, and then a post-R divider (after multiplier) for flexible frequency planning between the input (OSCin) and the phase detector.

The phase detector (PFD) can take frequencies from 5 to 200 MHz, but also has extended modes down to 0.25 MHz and up to 400 MHz. The phase-lock loop (PLL) contains a Sigma-Delta modulator (1st to 4th order) for fractional N-divider values. The fractional denominator is programmable to 32-bit long, allowing a very fine resolution of frequency step. There is a phase adjust feature that allows shifting of the output phase in relation to the input (OSCin) by a fraction of the size of the fractional denominator.

The output power is programmable and can be designed for high power at a specific frequency by the pull-up component at the output pin.

The digital logic is a standard 4-wire SPI or uWire interface and is 1.8-V and 3.3-V compatible.

7.2 Functional Block Diagram



7.3 Functional Description

7.3.1 Input Signal

An input signal is required for the PLL to lock. The input signal is also used for the VCO calibration, so a proper signal needs to be applied before the start of programming. The input signal goes to the OSCinP and OSCinM pins of the device (there is internal biasing which requires AC-coupling caps in series before the pin). This is a differential buffer so the total swing is the OSCinM signal subtracted by the OSCinP signal. Both differential signals and single-ended signal can be used. Below is an example of the max signal level in each mode. It is important to have proper termination and matching on both sides (see *Application and Implementation*).

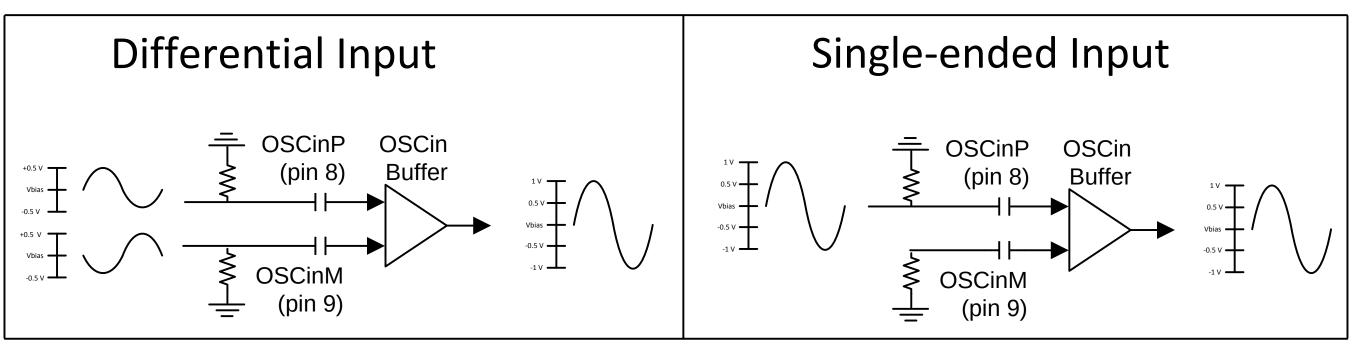


Figure 18. Differential vs Single-Ended Mode

Functional Description (continued)

7.3.2 Input Signal Path

The input signal path contains the components between the input (OSCin) buffer and the phase detector. The best PLL noise floor is achieved with a 200-MHz input signal for the highest dual phase detector frequency. In order to address a wide range of applications, the input signal path contains the below components for flexible configuration before the phase detector. Each component can be bypassed. See the table below for usage boundaries if engaging a component.

- OSCin doubler: This is low noise frequency doubler which can be used to multiply input frequencies by two. The doubler uses both the rising and falling edge of the input signal so the input signal must have 50% duty cycle if enabling the doubler. The best PLL noise floor is achieved with 200-MHz PFD, thus the doubler is useful if, for example, a very low noise 100-MHz input signal is available instead.
- Pre-R divider: This is a frequency divider capable of very high frequency inputs. Use this to divide any input frequency up to 1400-MHz, and then the post-R divider if lower frequencies are needed.
- Multiplier: This is a programmable, low noise multiplier. In combination with the Pre-R and Post-R dividers, the multiplier offers the flexibility to set a PFD away from frequencies that may create critical integer boundary spurs with the VCO and output frequencies. See *Application and Implementation* for an example. The user should not use the doubler while using the low noise programmable multiplier.
- Post-R divider: Use this divider to divide down to frequencies below 5 MHz in extended PFD mode.

Table 1. Boundaries for Input Path Components

	INPUT		OUTPUT	
	LOW (MHz)	HIGH (MHz)	LOW (MHz)	HIGH (MHz)
Input signal	5	1400		
OSCin doubler	5	700	10	1400
Pre-R divider	10	1400	5	700
Multiplier	40	70	180	250
Post-R divider	5	250	0.25	125
PFD	0.25	400		

7.3.3 PLL Phase Detector and Charge Pump

The PLL phase detector, also known as phase frequency detector (PFD), compares the outputs of the post-R divider and N divider and generates a correction current with the charge pump corresponding to the phase error until the two signals are aligned in phase (the PLL is locked). The charge pump output goes through external components (loop filter) which turns the correction current pulses into a DC voltage applied to the tuning voltage (Vtune) of the VCO. The charge pump gain level is programmable and allow to modify the loop bandwdith of the PLL.

The default architecture is a dual-loop PFD which can operate between 5 to 200 MHz. To use it in extended range mode the PFD has to be configured differently:

- Extended low phase detector frequency mode: For frequencies between 250 kHz and 5 MHz, low PFD mode can be activated (FCAL_LPFD_ADJ = 3). PLL_N_PRE also needs to be set to 4.
- Extended high phase detector frequency mode: For frequencies between 200 and 400 MHz, high PFD mode can be activated (FCAL_HPFD_ADJ = 3). The PFD also has to be set to single-loop PFD mode (PFD_CTL = 3). This mode only works if using integer-N, and PLL noise floor will be about 6-dB higher than in dual-loop PFD mode.

7.3.4 N Divider and Fractional Circuitry

The N divider (12 bits) includes a multi-stage noise shaping (MASH) sigma-delta modulator with prgrammable order from 1st to 4th order, which performs fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). Using programmable registers, PLL_N is the integer portion and PLL_NUM / PLL_DEN is the fractional portion, thus the total N divider value is determined by PLL_N + PLL_NUM / PLL_DEN. This allows the output frequency to be a fractional multiplication of the phase detector frequency. The higher the denominator the finer the resolution step of the output. There is a N divider prescalar (PLL_N_PRE) between the VCO and the N divider which performs a division of 2 or 4. 2 is selected typically for higher performance in fractional mode and 4 may be desirable for lower power operation and when N is approaching max value.

Fvco = Fpd × PLL_N_PRE × (PLL_N + PLL_NUM / PLL_DEN)

Minimum output frequency step = Fpd / PLL_DEN

Typically, higher modulator order pushes the noise out in frequency and may be filtered out with the PLL. However, several tradeoff needs to be made. table below shows the suggested minimum N value while in fractional mode as a function of the sigma-delta modulator order. It also describe the recommended register setting for the PFD delay (register PFD_DLY_SEL).

Table 2. MASH order and N Divider

	INTEGER-N	1st ORDER	2nd ORDER	3rd ORDER	4th ORDER
Minimum N divider (low bound)	9	11	16	18	30
PFD delay recommended setting (PFD_DLY_SEL)	1	1	2	2	8

7.3.5 Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) is fully integrated. The frequency range of the VCO is from 3.55 to 7.1 GHz so it covers one octave. Output dividers allow the generation of all other lower frequencies. The VCO-doubler allow the generation of all other higher frequencies. The output frequency of the VCO is inverse proportional to the DC voltage present at the tuning voltage point on pin Vtune. The tuning range is 0 V to 2.5 V. 0 V generates the maximum frequency and 2.5 V generates the minimum frequency. This VCO requires a calibration procedure for each frequency selected to lock on. Each vco calibration will force the tuning voltage to mid value and calibrate the VCO circuit. The VCO is designed to remained locked over the entire temperature range the device can support. Table 3 shows the VCO gain as a function of frequency.

Table 3. Typical kVCO

VCO FREQUENCY (MHz)	kVCO (MHz/V)
3700	28
4200	30
4700	33
5200	36
5700	41
6200	47
6800	51

7.3.6 VCO Calibration

The VCO calibration is responsible of setting the VCO circuit to the target frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. A valid input (OSCin) signal to the device must present before the VCO calibration begins. To see how to reduce the calibration time, refer to *Application and Implementation*.

7.3.7 VCO Doubler

To go above the VCO upper bound, the VCO-doubler must be used (VCO_2X_EN=1). The doubling block can be enabled while the VCO is between 3.55 GHz (lowest VCO frequency) and 4.9 GHz. When VCO doubler is enabled, the N divider prescalar is automatically forced to divide by 4.

7.3.8 Channel Divider

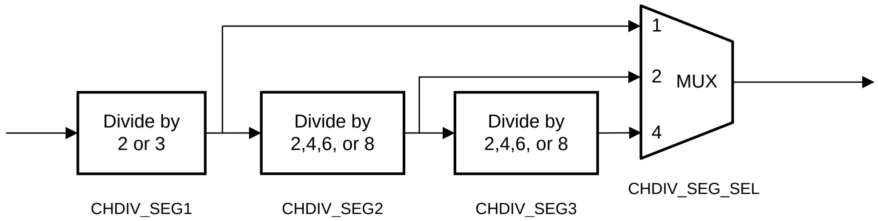


Figure 19. Channel Divider Diagram

To go below the VCO lower bound, the channel divider must be used. The channel divider consists of three programmable dividers controlled by the registers CHDIV_SEG1, CHDIV_SEG2, CHDIV_SEG3. The Multiplexer (programmed with register CHDIV_SEG_SEL) selects which divider is included in the path. The minimum division is 2 while the maximum division is 192. Un-used dividers can be powered down to save current consumption. The entire channel divider can be powered down with register CHDIV_EN = 0 or selectively setting registers CHDIV_SEG1_EN = 0, CHDIV_SEG2_EN = 0 ,CHDIV_SEG3_EN = 0. Unused buffers may also be powered down with registers CHDIV_DISTA_EN and CHDIV_DIST_EN. See Table 4 for a guideline of what channel divider setting to use when below a specific output frequency.

Table 4. Channel Divider Setting as a Function of the Desired Output Frequency

OUTPUT FREQUENCY	CHANNEL DIVIDER SEG1	CHANNEL DIVIDER SEG2	CHANNEL DIVIDER SEG3	TOTAL DIVISION	VCO FREQ
3600	2	1	1	2	7200
1840	3	1	1	3	5520
1240	2	2	1	4	4960
930	3	2	1	6	5580
610	2	4	1	8	4880
460	2	6	1	12	5520
300	2	8	1	16	4800
230	3	8	1	24	5520
150	2	8	2	32	4800
110	3	6	2	36	3960
100	3	8	2	48	4800
70	2	8	4	64	4480
50	2	8	6	96	4800
30	2	8	8	128	3840
20	3	8	8	192	3840

7.3.9 Output Distribution

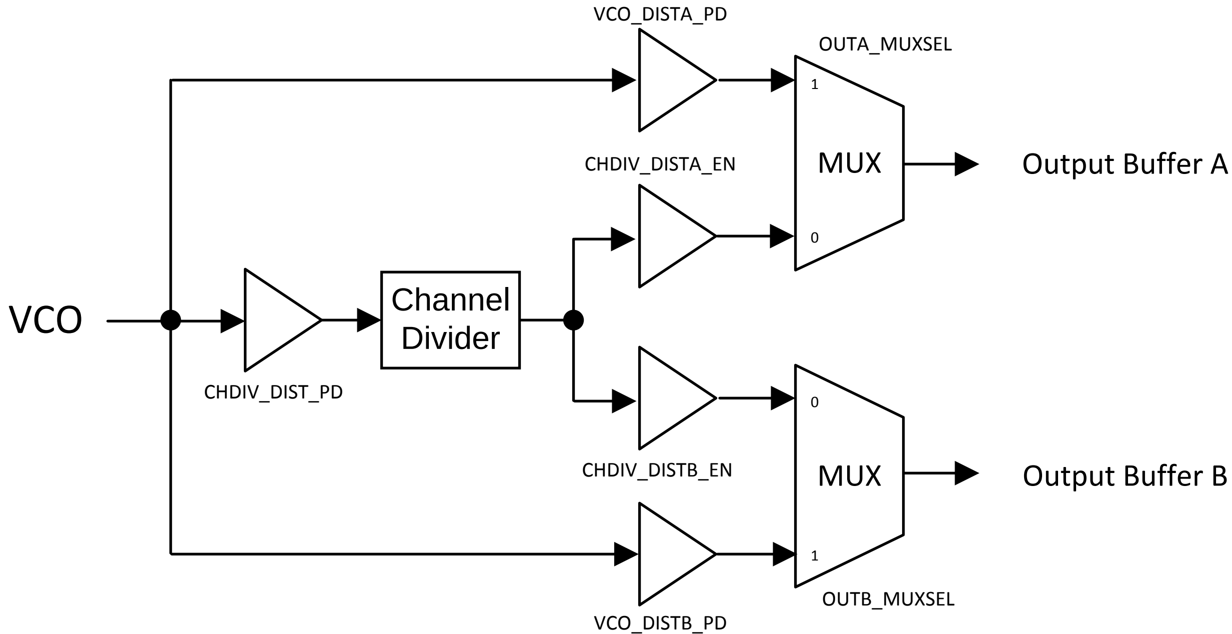


Figure 20. Output Distribution Diagram

For each output A or B, there is a mux which select the VCO output directly or the channel divider output. Before these selection MUX there are several buffers in the distribution path which can be configured depending on the route selected. By disabling unused buffers, unwanted signals can be isolated and unneeded current consumption can be eliminated.

7.3.10 Output Buffer

Each output buffer (A and B) have programmable gain with register OUTA_POW and OUTB_POW. The RF output buffer configuration is open collector and requires an external pull-up from RFout pin to V_{CC}. There are two pull-up options that can be used with either resistor or inductor. Refer to the applications section for design considerations.

1. Resistor pull-up: placing a 50-Ω resistor pull-up matches the output impedance to 50-Ω. However, maximum output power is limited. Output buffer current settings should be set to a value before output power is saturated (output power increases less for every step increase in output current value).
2. Inductor pull-up: placing an inductor pull-up creates a resonance at the frequency of interest. This offers higher output power for the same current and higher maximum output power. However, the output impedance will be higher and additional matching may be required..

7.3.11 Phase Adjust

In fractional mode, the phase relationship between the output and the input can be changed with very fine resolution. Writing the register MASH_SEED will trigger this shift. The seed value should be less then the fractional-N denominator register PLL_N_DEN. The actual phase shift can be obtained with the following equation:

Phase shift (degrees) = 360 × MASH_SEED / PLL_N_DEN / [Channel divider value]

7.4 Device Functional Modes

7.4.1 Powerdown

Power up and down can be achieved using the CE pin (logic HIGH or LOW voltage) or the POWERDOWN register bit (0 or 1). When the device comes out of the powered down state, either by pulling back CE pin HIGH (if it was powered down by CE pin) or by resuming the POWERDOWN bit to 0 (if it was powered down by register write), it is required that register R0 be programmed again to re-calibrate the device.

Device Functional Modes (continued)

7.4.2 Lock Detect

The MUXout pin can be configured to output a signal that gives an indication for the PLL being locked. If lock detect is enabled (LD_EN = 1) and the MUXout pin is configured as lock detect output (MUXOUT_SEL = 1), when the device is locked, the MUXout pin output is a logic HIGH voltage, and when the device is unlocked, MUXout output is a logic LOW voltage.

7.4.3 Register Readback

The MUXout pin can be programmed (MUXOUT_SEL = 0) to use register readback serial data output. To read back a certain register value, use the following steps:

1. Set the R/W bit to 1; the data field contents are ignored.
2. Program this register to the device, readback serial data will be output starting at the 9th clock.

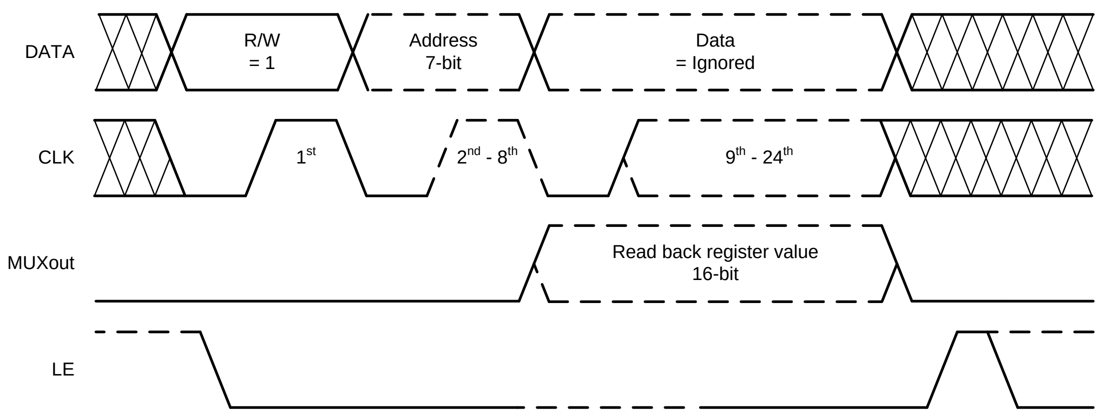


Figure 21. Register Readback Timing Diagram

7.5 Programming

The programming using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W (bit 23), 1 is read and 0 is write. The address field ADDRESS (bits 22:16) is used to decode the internal register address. The remaining 16 bits form the data field DATA (bits 15:0). While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank.

7.5.1 Recommended Initial Power on Programming Sequence

When the device is first powered up, the device needs to be initialized and the ordering of this programming is very important. After this sequence is completed, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the V_{CC} pins are at the proper levels
2. Ensure that a valid reference is applied to the OSCin pin
3. Soft reset the device (write R0[1] = 1)
4. Program the remaining registers
5. Frequency calibrate (write R0[3] = 1)

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Set the new N divider value (write R38[12:1])
2. Set the new PLL numerator (R45 and R44) and denominator (R41 and R40)
3. Frequency calibrate (write R0[3] = 1)

7.6 Register Maps

7.6.1 LMX2592 Register Map

Figure 22. Register Table

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	ADDRESS[6:0]							DATA [15:0]															
0	R/W	0	0	0	0	0	0	0	0	0	LD_EN	0	0	0	1	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_SEL	RESET	POWERDOWN
1	R/W	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
7	R/W	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	0
8	R/W	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
9	R/W	0	0	0	1	0	0	1	0	0	0	0	OSC_2X	0	REF_EN	1	0	0	0	0	0	0	1	0
10	R/W	0	0	0	1	0	1	0	0	0	0	1	MULT					1	0	1	1	0	0	0
11	R/W	0	0	0	1	0	1	1	0	0	0	0	PLL_R								1	0	0	0
12	R/W	0	0	0	1	1	0	0	0	1	1	1	PLL_R_PRE											
13	R/W	0	0	0	1	1	0	1	0	CP_EN	0	0	0	0	PFD_CTL		0	0	0	0	0	0	0	0
14	R/W	0	0	0	1	1	1	0	0	0	0	0	CP_IDN					CP_IUP					CP_ICOARSE	
19	R/W	0	0	1	0	0	1	1	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	1
23	R/W	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0
24	R/W	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1
28	R/W	0	0	1	1	1	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0
29	R/W	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
30	R/W	0	0	1	1	1	1	0	0	0	0	0	0	MASH_DITHER	0	0	0	0	1	1	0	1	0	VCO_2X_EN
31	R/W	0	0	1	1	1	1	1	0	0	0	0	0	VCO_DISTB_PD	VCO_DISTA_PD	0	CHDIV_DIST_PD	0	0	0	0	0	0	1
32	R/W	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0
33	R/W	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0
34	R/W	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	1	1	CHDIV_EN	1	0	0	0	0

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	**ADDRESS[6:0]**							**DATA [15:0]**															
35	R/W	0	1	0	0	0	1	1	0	0	0	CHDIV_SEG2				CHDIV_SEG3_EN	CHDIV_SEG2_EN	0	0	1	1	CHDIV_SEG1	CHDIV_SEG1_EN	1
36	R/W	0	1	0	0	1	0	0	0	0	0	0	CHDIV_DISTB_EN	CHDIV_DISTA_EN	0	0	0	CHDIV_SEG_SEL			CHDIV_SEG3			
37	R/W	0	1	0	0	1	0	1	0	1	0	PLL_N_PRE	0	0	0	0	0	0	0	0	0	0	0	0
38	R/W	0	1	0	0	1	1	0	0	0	0	PLL_N												
39	R/W	0	1	0	0	1	1	1	1	0	PFD_DLY						0	0	0	0	0	1	0	0
40	R/W	0	1	0	1	0	0	0	PLL_DEN[31:16]															
41	R/W	0	1	0	1	0	0	1	PLL_DEN[15:0]															
42	R/W	0	1	0	1	0	1	0	MASH_SEED[31:16]															
43	R/W	0	1	0	1	0	1	1	MASH_SEED[15:0]															
44	R/W	0	1	0	1	1	0	0	PLL_NUM[31:16]															
45	R/W	0	1	0	1	1	0	1	PLL_NUM[15:0]															
46	R/W	0	1	0	1	1	1	0	0	0	OUTA_POW						OUTB_PD	OUTA_PD	MASH_EN	1	0	MASH_ORDER		
47	R/W	0	1	0	1	1	1	1	0	0	0	OUTA_MUX		0	0	0	1	1	OUTB_POW					
48	R/W	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	OUTB_MUX	
64	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	ACAL_FAST	FCAL_FAST	1	0	1	0	1	1	1	1

7.6.1.1 Register Descriptions

Table 5. R0 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14		R/W		Program to default
13	LD_EN	R/W	1	Lock detect enable 1: enable 0: disable
12:9		R/W		Program to default
8:7	FCAL_HPFD_ADJ	R/W	0	Used for when PFD freq is high 3: PFD > 200 MHz 2: PFD > 150 MHz 1: PFD > 100 MHz 0: not used
6:5	FCAL_LPFD_ADJ	R/W	0	Used for when PFD freq is low 3: PFD < 5 MHz 2: PFD < 10 MHz 1: PFD < 20 MHz 0: not used
4		R/W		Program to default
3	FCAL_EN	R/W	1	Enable frequency calibration 1: enable (writing 1 to this register triggers the calibration sequence) 0: disable
2	MUXOUT_SEL	R/W	1	Signal at MUXOUT pin 1: Lock Detect (3.3V if locked, 0V if unlocked) 0: Readback (3.3V digital output)
1	RESET	R/W	0	Reset Write with a value of 1 to reset device (this register will self-switch back to 0)
0	POWERDOWN	R/W	0	Powerdown whole device 1: power down 0: power up

Table 6. R1 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:3		R/W		Program to default
2:0	CAL_CLK_DIV	R/W	3	Divides down the OSCin signal for calibration clock Calibration Clock = OSCin / 2^CAL_CLK_DIV Set this value so that calibration clock is less than but as close to 200MHz as possible if fast calibration time is desired.

Table 7. R7 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 8. R8 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 9. R9 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11	OSC_2X	R/W	0	Reference path doubler 1: enable 0: disable
10		R/W		Program to default
9	REF_EN	R/W	1	Enable reference path 1: enable 0: disable
8:0		R/W		Program to default

Table 10. R10 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11:7	MULT	R/W	1	Input signal path multiplier (input range from 40 - 70 MHz, output range from 180 - 250 MHz)
6:0		R/W		Program to default

Table 11. R11 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11:4	PLL_R	R/W	1	R divider after multiplier and before PFD
3:0		R/W		Program to default

Table 12. R12 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11:0	PLL_R_PRE	R/W	1	R divider after OSCin doubler and before multiplier

Table 13. R13 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15		R/W		Program to default
14	CP_EN	R/W	1	Enable charge pump 1: enable 0: disable
13:10		R/W		Program to default
9:8	PFD_CTL	R/W	0	PFD mode 0: Dual PFD (default) 3: Single PFD (ONLY use if PFD freq is higher than 200MHz)
7:0		R/W		Program to default

Table 14. R14 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11:7	CP_IDN	R/W	3	Charge pump current (DN) – must equal to charge pump current (UP). Can activate any combination of bits. <bit 4>: 1.25 mA <bit 3>: 2.5 mA <bit 2>: 0.625 mA <bit 1>: 0.312 mA <bit 0>: 0.156 mA
6:2	CP_IUP	R/W	3	Charge pump current (UP) – must equal to charge pump current (DN). Can activate any combination of bits. <bit 4>: 1.25 mA <bit 3>: 2.5 mA <bit 2>: 0.625 mA <bit 1>: 0.312 mA <bit 0>: 0.156 mA
1:0	CP_ICOARSE	R/W	1	charge pump gain multiplier - multiplies charge pump current by a given factor: 3: multiply by 2.5 2: multiply by 1.5 1: multiply by 2 0: no multiplication

Table 15. R19 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 16. R23 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 17. R24 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 18. R28 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 19. R29 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 20. R30 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11		R/W		Program to default
10	MASH_DITHER	R/W	0	MASH dithering: toggle on/off to randomize
9:1		R/W		Program to default
0	VCO_2X_EN	R/W	0	Enable VCO doubler 1: enable 0: disable

Table 21. R31 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11		R/W		Program to default
10	VCO_DISTB_PD	R/W	1	Power down buffer between VCO and output B 1: power down 0: power up
9	VCO_DISTA_PD	R/W	0	Power down buffer between VCO and output A 1: power down 0: power up
8		R/W		Program to default
7	CHDIV_DIST_PD	R/W	0	Power down buffer between VCO and channel divider
6:0		R/W		Program to default

Table 22. R32 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 23. R33 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 24. R34 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6		R/W		Program to default
5	CHDIV_EN	R/W	1	Enable entire channel divider 1: enable 0: power down
4:0		R/W		Program to default

Table 25. R35 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to default
12:9	CHDIV_SEG2	R/W	1	Channel divider segment 2 8: divide-by-8 4: divide-by-6 2: divide-by-4 1: divide-by-2 0: PD
8	CHDIV_SEG3_EN	R/W	0	Channel divider segment 3 1: enable 0: power down (power down if not needed)
7	CHDIV_SEG2_EN	R/W	0	Channel divider segment 2 1: enable 0: power down (power down if not needed)
6:3		R/W		Program to default
2	CHDIV_SEG1	R/W	1	Channel divider segment 1 1: divide-by-3 0: divide-by-2
1	CHDIV_SEG1_EN	R/W	0	Channel divider segment 1 1: enable 0: power down (power down if not needed)
0		R/W		Program to default

Table 26. R36 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to default
11	CHDIV_DISTB_EN	R/W	0	Enable buffer between channel divider and output B 1: enable 0: disable
10	CHDIV_DISTA_EN	R/W	1	Enable buffer between channel divider and output A 1: enable 0: disable
9:7		R/W		Program to default
6:4	CHDIV_SEG_SEL	R/W	1	Channel divider segment select 4: includes channel divider segment 1,2 and 3 2: includes channel divider segment 1 and 2 1: includes channel divider segment 1 0: PD
3:0	CHDIV_SEG3	R/W	1	Channel divider segment 3 8: divide-by-8 4: divide-by-6 2: divide-by-4 1: divide-by-2 0: PD

Table 27. R37 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to default
12	PLL_N_PRE	R/W	0	N-divider pre-scalar 1: divide-by-4 0: divide-by-2
11:0		R/W		Program to default

Table 28. R38 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to default
12:1	PLL_N	R/W	27	Integer part of N-divider
0		R/W		Program to default

Table 29. R39 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14		R/W		Program to default
13:8	PFD_DLY	R/W	2	PFD Delay 32: Not used 16: 16 clock cycle delay 8: 12 clock cycle delay 4: 8 clock cycle delay 2: 6 clock cycle delay 1: 4 clock cycle delay
7:0		R/W		Program to default

Table 30. R40 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_DEN[31:16]	R/W	1000	Denominator MSB of N-divider fraction

Table 31. R41 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_DEN[15:0]	R/W	1000	Denominator LSB of N-divider fraction

Table 32. R42 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	MASH_SEED[31:16]	R/W	0	MASH seed MSB

Table 33. R43 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	MASH_SEED[15:0]	R/W	0	MASH seed LSB

Table 34. R44 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_NUM[31:16]	R/W	0	Numerator MSB of N-divider fraction

Table 35. R45 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_NUM[15:0]	R/W	0	Numerator LSB of N-divider fraction

Table 36. R46 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15		R/W		Program to default
13:8	OUTA_POW	R/W	15	Output buffer A power increase power from 0 to 31 extra boost from 48 to 63
7	OUTB_PD	R/W	1	Output buffer B power down 1: power down 0: power up
6	OUTA_PD	R/W	0	Output buffer A power down 1: power down 0: power up
5	MASH_EN	R/W	1	Enable sigma-delta modulator
4:3		R/W		Program to default
2:0	MASH_ORDER	R/W	3	Sigma-delta modulator order 4: fourth order 3: third order 2: second order 1: first order 0: integer mode

Table 37. R47 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to default
12:11	OUTA_MUX	R/W	0	Selects signal to the output buffer 2,3: reserved 1: Selects output from VCO 0: Selects the channel divider output
10:6		R/W		Program to default
5:0	OUTB_POW	R/W	0	Output buffer B power increase power from 0 to 31 extra boost from 48 to 63

Table 38. R48 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:2		R/W		Program to default
1:0	OUTB_MUX	R/W	0	Selects signal to the output buffer 2,3: reserved 1: Selects output from VCO 0: Selects the channel divider output

Table 39. R64 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10		R/W		Program to default
9	ACAL_FAST	R/W	0	Enable fast amplitude calibration 1: enable 0: disable
8	FCAL_FAST	R/W	0	Enable fast frequency calibration 1: enable 0: disable
7:0		R/W		Program to default

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Optimization of Spurs

8.1.1.1 Understanding Spurs by Offsets

The first step in optimizing spurs is to be able to identify them by offset. Figure 23 gives a good example that can be used to isolate the following spur types.

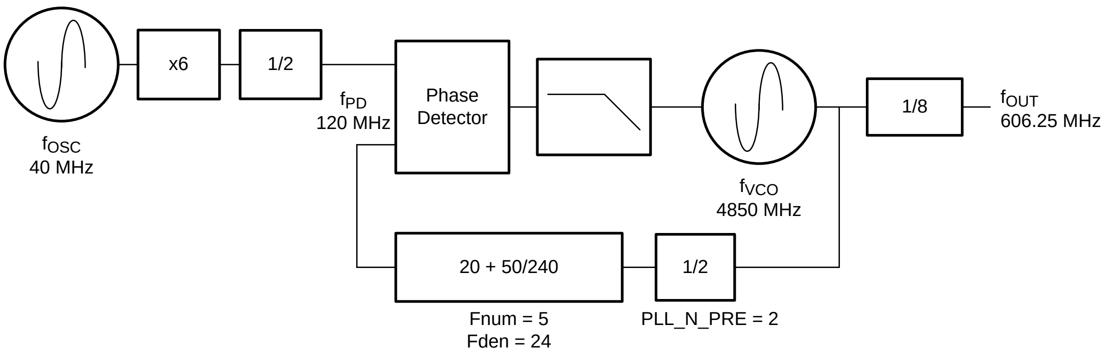


Figure 23. Spur Offset Frequency Example

Based on the above figure, the most common spurs can be calculated from the frequencies. Note that the **%** is the modulus operator and is meant to mean the difference to the closest integer multiple. Some examples of how to use this operator are: 36 % 11 = 3, 1000.1 % 50 = 0.1, and 5023.7 % 122.88 = 14.38. Applying this concept, the spurs at various offsets can be identified from Figure 23.

Table 40. Spur Definition Table

SPUR TYPE	OFFSET	OFFSET IN Figure 23	COMMENTS
OSCin	f_{OSC}	40 MHz	This spur occurs at harmonics of the OSCin frequency.
Fpd	f_{PD}	120 MHz	The phase detector spur has many possible mechanisms and occurs at multiples of the phase detector frequency.
f_{OUT} % f_{OSC}	f_{OUT} % f_{OSC}	606.25 % 40 = 6.25 MHz	This spur is caused by mixing between the output and input frequencies.
f_{VCO}% f_{OSC}	f_{VCO} % f_{OSC}	4850 % 40 = 10 MHz	This spur is caused by mixing between the VCO and input frequencies.
f_{VCO}% f_{PD}	f_{VCO} % f_{PD}	4850 % 120 = 50 MHz	This spur would be the same offset as the integer boundary spur if PLL_N_PRE=1, but can be different if this value is greater than one.
Integer Boundary	f_{PD} *(Fnum%Fden)/ Fden)	120 × (5%24)/24 = 25 MHz	This is a single spur
Primary Fractional	f_{PD} / Fden	120 / 24 = 5 MHz	The primary fractional

Application Information (continued)

Table 40. Spur Definition Table (continued)

SPUR TYPE	OFFSET	OFFSET IN Figure 23	COMMENTS
Sub-Fractional	f_{PD} / Fden / k k=2,3, or 6	First Order Modulator: None 2nd Order Modulator: 120/24/2 = 2.5 MHz 3rd Order Modulator: 120/24/6 = 0.83333 MHz 4th Order Modulator: 120/24/12 = 0.416666 MHz	To Calculate k: 1st Order Modulator: k=1 2nd Order Modulator: k=1 if Fden is odd, k=2 if Fden is even 3rd Order Modulator: k=1 if Fden not divisible by 2 or 3, k=2 if Fden divisible by 2 not 3, k=3 if Fden divisible by 3 but not 2, Fden = 6 if Fden divisible by 2 and 3 4th Order Modulator: k=1 if Fden not divisible by 2 or 3. k=3 if Fden divisible by 3 but not 2, k=4 if Fden divisible by 2 but not 3, k=12 if Fden divisible by 2 and 3 Sub-Fractional Spurs exist if k>1

In the case that two different spur types occur at the same offset, either name would be correct. Some may name this by the more dominant cause, while others would simply name by choosing the name that is near the top of Table 40.

8.1.1.2 Spur Mitigation Techniques

Once the spur is identified and understood, there will likely be a desire to try to minimize them. The following table gives some common methods.

Table 41. Spurs and Mitigation Techniques

SPUR TYPE	WAYS TO REDUCE	TRADE-OFF
OSCin	1. Use PLL_N_PRE = 2 2. Use an OSCin signal with low amplitude and high slew rate (like LVDS).	
Phase Detector	1. Decrease PFD_DLY 2. To pin 11, use a series ferrite bead and a shunt 0.1-µF capacitor.	
f_{OUT} % f_{OSC}	Use an OSCin signal with low amplitude and high slew rate (like LVDS)	
f_{VCO}% f_{OSC}	1. To pin 7, use a series ferrite bead and a shunt 0.1-µF capacitor. 2. Increase the offset of this spur by shifting the VCO frequency 3. If multiple VCO frequencies are posslble that yield the same spur offset, choose the higher VCO frequency. .	
f_{VCO}% f_{PD}	Avoid this spur by shifting the phase detector frequency (with the programmable input multiplier or R divider) or shifting the VCO frequency. This spur is better at higher VCO frequency.	
Integer Boundary	**Methods for PLL Dominated Spurs** 1. Avoid the worst case VCO frequencies if possible. 2. Strategically choose which VCO core to use if possible. 3. Ensure good slew rate and signal integrity at the OSCin pin 4. Reduce the loop bandwidth or add more filter poles for out of band spurs 5. Experiment with modulator order and PFD_DLY	Reducing the loop bandwidth may degrade the total integrated noise if the bandwidth is too narrow.
	Methods for VCO Dominated Spurs 1. Avoid the worst case VCO frequencies if possible. 2. Reduce Phase Detector Frequency 3. Ensure good slew rate and signal integrity at the OSCin pin 4. Make the impedance looking outwards from the OSCin pin close to 50 Ω.	Reducing the phase detector may degrade the phase noise and also reduce the capacitance at the Vtune pin.

Table 41. Spurs and Mitigation Techniques (continued)

SPUR TYPE	WAYS TO REDUCE	TRADE-OFF
Primary Fractional	1. Decrease Loop Bandwidth 2. Change Modulator Order 3. Use Larger Unequivalent Fractions	Decreasing the loop bandwidth too much may degrade in-band phase noise. Also, larger unequivalent fractions only sometimes work
Sub-Fractional	1. Use Dithering 2. Use MASH seed 3. Use Larger Equivalent Fractions 4. Use Larger Unequivalent Fractions 5. Reduce Modulator Order 6. Eliminate factors of 2 or 3 in denominator (see AN-1879, SNAA062)	Dithering and larger fractions may increase phase noise. MASH_SEED can be set between values 0 and Fden, which will change the sub-fractional spur behavior. This is a deterministic relationship and there will be one seed value that will give best result for this spur.

8.1.2 Configuring the Input Signal Path

The input path is considered the portion of the device between the OSCin pin and the phase detector, which includes the input buffer, R dividers, and programmable multipliers. The way that these are configured can have a large impact on phase noise and fractional spurs.

8.1.2.1 Input Signal Noise Scaling

The input signal noise scales by 20*log(output frequency / input signal frequency), so always check this to see if the noise of the input signal scaled to the output frequency is close to the PLL in-band noise level. When that happens, the input signal noise is the dominant noise source, not the PLL noise floor.

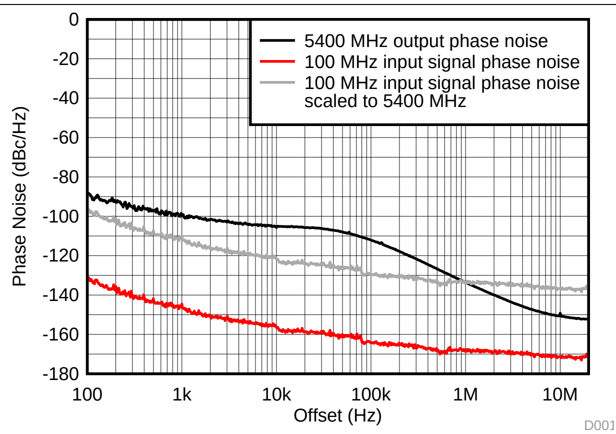


Figure 24. Phase Noise of 5.4-GHz Output with Low Noise Input Signal

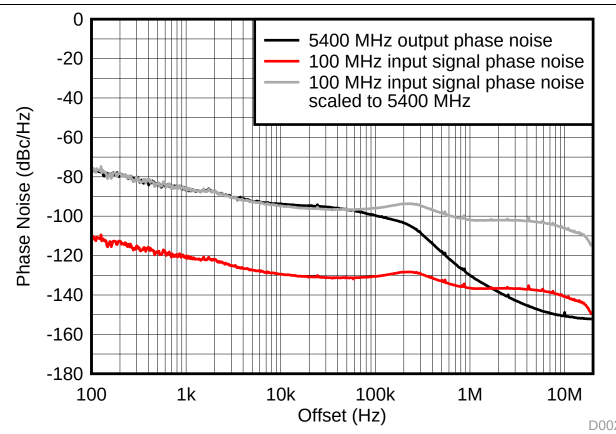


Figure 25. Phase Noise of 5.4-GHz Output with High Noise Input Signal

8.1.3 Input Pin Configuration

The OSCinM and OSCinP can be used to support both a single-ended or differential clock. In either configuration, the termination on both sides should match for best common-mode noise rejection. The slew rate and signal integrity of this signal can have an impact on both the phase noise and fractional spurs. Standard clocking types, LVDS, LVPECL, HCSL, and CMOS can all be used.

8.1.4 Using the OSCin Doubler

The lowest PLL flat noise is achieved with a low noise 200-MHz input signal. If only a low noise input signal with lower frequency is available (for example a 100-MHz source), you can use the low noise OSCin doubler to attain 200-MHz phase detector frequency. Since PLL_flat = PLL_FOM + 20*log(Fvco/Fpd) + 10*log(Fpd / 1Hz), doubling Fpd theoretically gets –6 dB from the 20*log(Fvco/Fpd) component, +3 dB from the 10*log(Fpd / 1Hz) component, and cumulatively a –3-dB improvement.

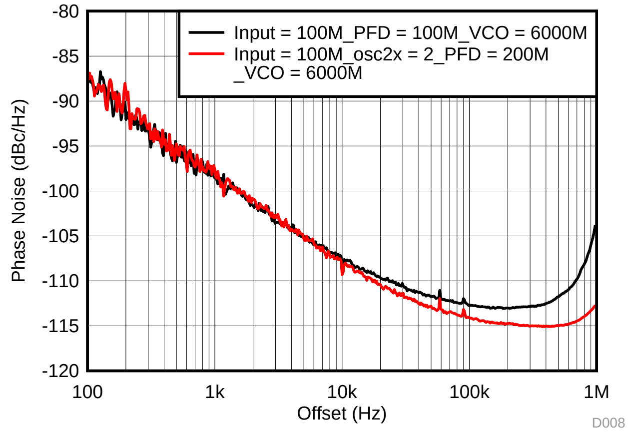


Figure 26. 100MHz Input with OSCin Doubler

8.1.5 Using the Input Signal Path Components

The ideal input is a low noise 200-MHz (or multiples of it) signal and 200-MHz phase detector frequency (highest dual PFD frequency). However, if spur mechanisms are understood, certain combinations of the R-divider and Multiplier can help. Refer to the optimization of spurs section for understanding spur types and their mechanisms first, then try this section for these specific spurs.

8.1.5.1 Moving Phase Detector Frequency

Engaging the multiplier in the reference path allows more flexibility in setting the PFD frequency. One example use case of this is if Fvco % Fpd is the dominant spur. This method can move the PFD frequency and thus the Fvco % Fpd.

Example: Fvco = 3720.12 MHz, Fosc = 300 MHz, Pre-R divider = 5, Fpd = 60 MHz, Fvco%Fosc = 120.12 MHz (Far out), Fvco%Fpd = 120 kHz (dominant). There is a Fvco%Fpd spur at 120 kHz (refer to Figure 27).

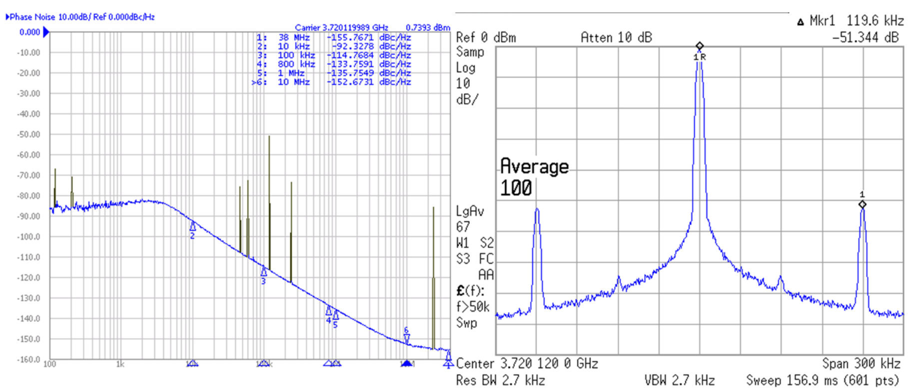


Figure 27. Fvco % Fpd Spur

Then second case, using divider and multiplier, we make Fpd = 53.57 MHz away from 120-kHz spur. Fvco = 3720.12MHz, Fosc = 300MHz, Pre-R divider = 7, Multiplier = 5, Post-R divider = 4, Fpd = 53.57 MHz, Fvco%Fosc = 120.12 MHz (Far out). Fvco % Fpd = 23.79 MHz (far out). There is a 20–dB reduction for the Fvco % Fpd spur at 120 kHz (refer to Figure 28).

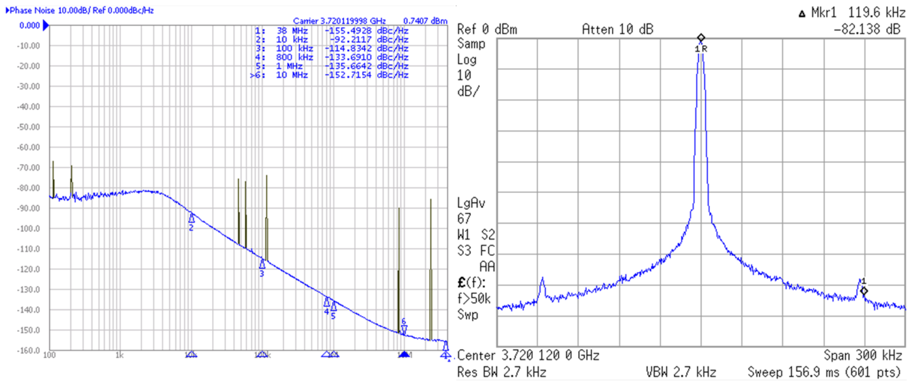


Figure 28. Moving Away from Fvco % Fpd Spur

8.1.5.2 Multiplying and Dividing by the Same Value

Although it may not seem like the first thing to try, the Fvco%Fosc and Fout%Fosc spur can sometimes be improved engaging the OSC_2X bit and then dividing by 2. Although this gives the same phase detector frequency, the spur can be improved.

8.1.6 Designing for Output Power

If there is a desired frequency for highest power, use an inductor pull-up and design for the value so that the resonance is at that frequency. Use the formula SRF = 1 / (2π× sqrt[L × C]).

Example: C = 1.4 pF (characteristic). If max power is targeted at 1 GHz, L = 18 nH. If max power is targeted at 3.3 GHz, L = 1.6 nH

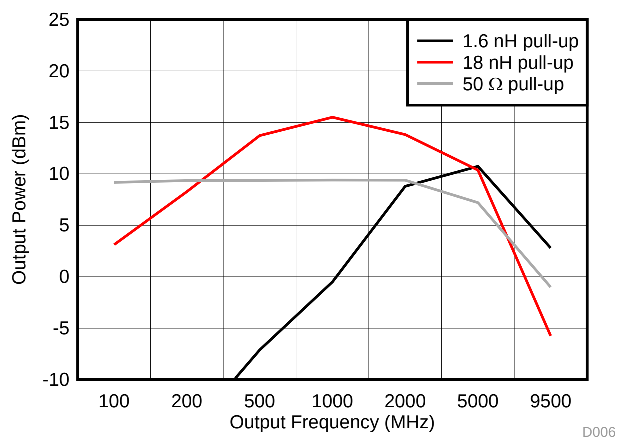


Figure 29. Output Power Versus Pull-Up Type

8.1.7 Current Consumption Management

The starting point is the typical total current consumption of 250 mA: 100-MHz input frequency, OSCin doubler bypassed, Pre-R divider bypassed, multiplier bypassed, post-R divider bypassed, 100-MHz phase detector frequency, 0.468-mA charge pump current, channel divider off, one output on, 6000-MHz output frequency, 50-Ω output pull-up, 0-dBm output power (differential). To understand current consumption changes due to engaging different fuctional blocks , refer to Table 42.

Table 42. Typical Current Consumption Impact By Function

ACTION	STEPS	PROGRAMMING	INCREASE IN CURRENT (mA)
Use input signal path	Enable OSCin doubler	OSC_2X = 1	7
	Enable multiplier	MULT = 3,4,5, or 6	10

Table 42. Typical Current Consumption Impact By Function (continued)

ACTION	STEPS	PROGRAMMING	INCREASE IN CURRENT (mA)
Add an output	Route VCO to output B	VCO_DISTB_PD = 0	8
	Enable output B buffer	OUTB_PD = 0	54
Increase output power from 0 to +10dBm (differential)	Set highest output buffer current	OUTA_POW = 63	53
Use channel divider	Route channel divider to output	CHDIV_DISTA_EN = 1	5
	Enable channel divider	CHDIV_EN = 1	18
	Enable chdiv_seg1	CHDIV_SEG1_EN = 1	2
	Enable chdiv_seg2	CHDIV_SEG2_EN = 1	5
	Enable chdiv_seg3	CHDIV_SEG3_EN = 1	5
Using VCO doubler	Enable VCO doubler	VCO2X_EN	16

8.1.8 Decreasing Lock Time

Lock time consists of the calibration time (time for internal algorithm to set to desired output frequency) plus the analog settling time (time to settle to the final Vtune value). For fast calibration set registers FCAL_FAST = 1 and ACAL_FAST = 1. Also set the calibration clock (input frequency / 2^CAL_CLK_DIV) close to the maximum (200 MHz). For fast analog settling time, design loop filter for very wide loop bandwidth (MHz range).

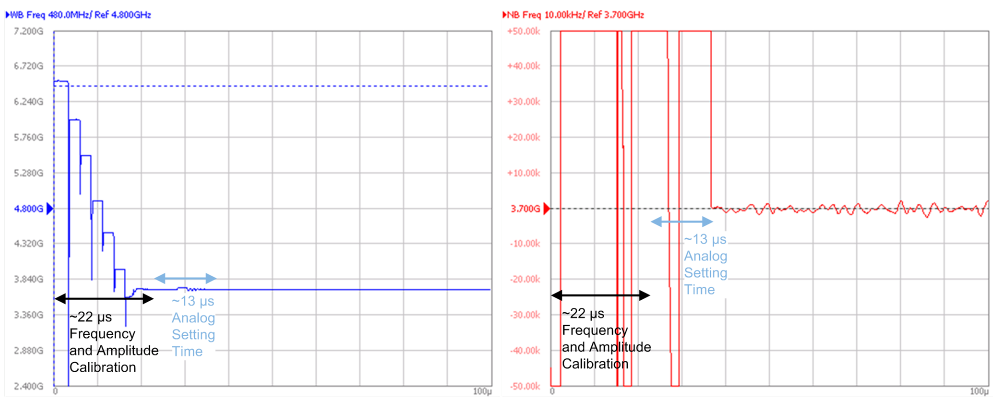


Figure 30. Lock Time Screenshot

The calibration sweeps from the top of the VCO frequency range to the bottom. This example does a calibration to lock at 3.7 GHz (which is the worst case). For the left screenshot (Wideband Frequency view), see the sweeping from top to bottom of the VCO range. On the right screenshot (Narrowband Frequency view), see the analog settling time to the precise target frequency.

8.1.9 Modeling and Understanding PLL FOM and Flicker Noise

Follow these recommended settings to design for wide loop bandwidth and extract FOM and flicker noise. The flat model is the PLL noise floor modeled by: PLL_flat = PLL_FOM + 20*log(Fvco/Fpd) + 10*log(Fpd / 1 Hz). The flicker noise (also known as 1/f noise) which changes by -10dB / decade, is modeled by: PLL_flicker (offset) = PLL_flicker_Norm + 20*log(Fvco / 1 GHz) – 10*log(offset / 10k Hz). The cumulative model is the addition of both components: PLL_Noise = 10*log(10PLL_Flat / 10 + 10PLL_flicker / 10). This is adjusted to fit the the measured data to extract the PLL_FOM and PLL_flicker_Norm spec numbers.

Table 43. Wide Loop Filter Design

PARAMETER	VALUE
PFD (MHz)	200
Charge pump (mA)	12
VCO frequency (MHz)	5400
Loop bandwidth (kHz)	2000

Table 43. Wide Loop Filter Design (continued)

PARAMETER	VALUE
Phase margin (degrees)	30
Gamma	1.4
Loop filter (2nd order)	
C1 (nF)	0.01
C2 (nF)	0.022
R2 (kohms)	4.7

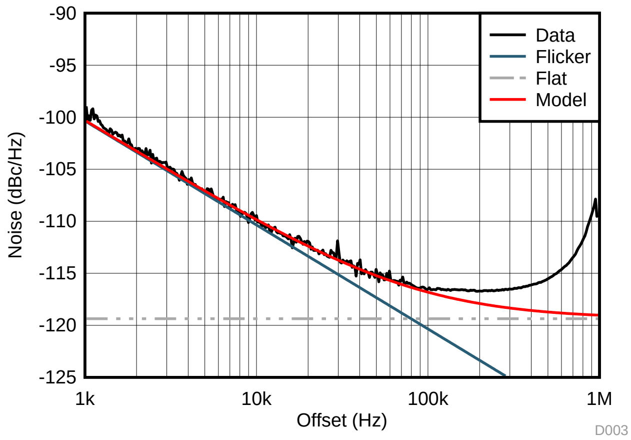


Figure 31. FOM and Flicker Noise Modeling

8.2 Typical Application

8.2.1 Design for Low Jitter

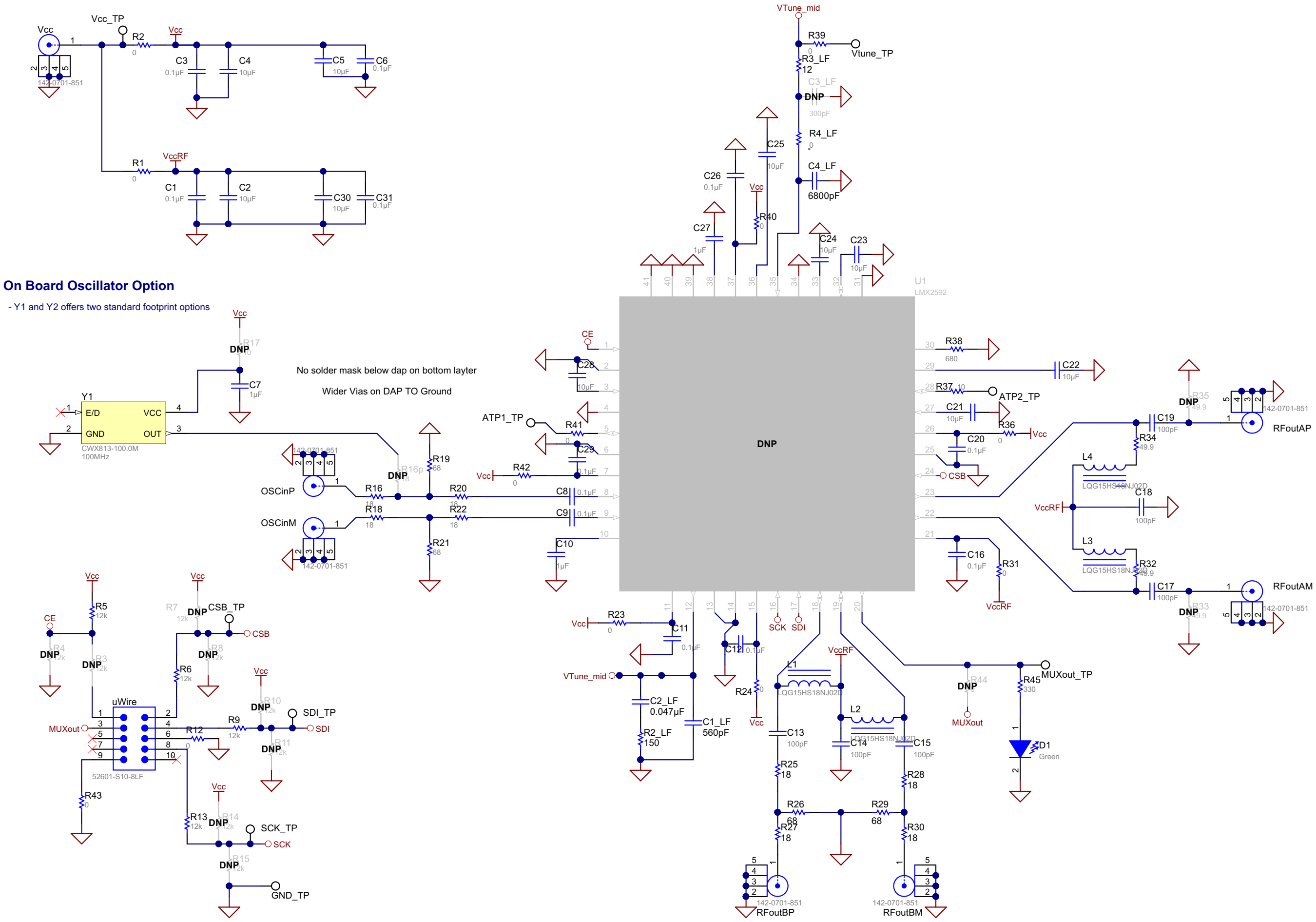


Figure 32. Typical Application Schematic

8.2.1.1 Design Requirements

Refer to the design parameters shown in Table 44.

Table 44. Design Information

PARAMETER	VALUE
PFD (MHz)	200
Charge pump (mA)	4.8
VCO frequency (MHz)	6000
Loop bandwidth (kHz)	210
Phase margin (degrees)	70
Gamma	3.8
Loop filter (2nd order)	
C1 (nF)	4.7
C2 (nF)	100
R2 (ohms)	0.068

8.2.1.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. As a rule of thumb, jitter will be lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design will have less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this as longer lock times and spurs should be considered in design as well.

8.2.1.3 Application Curves

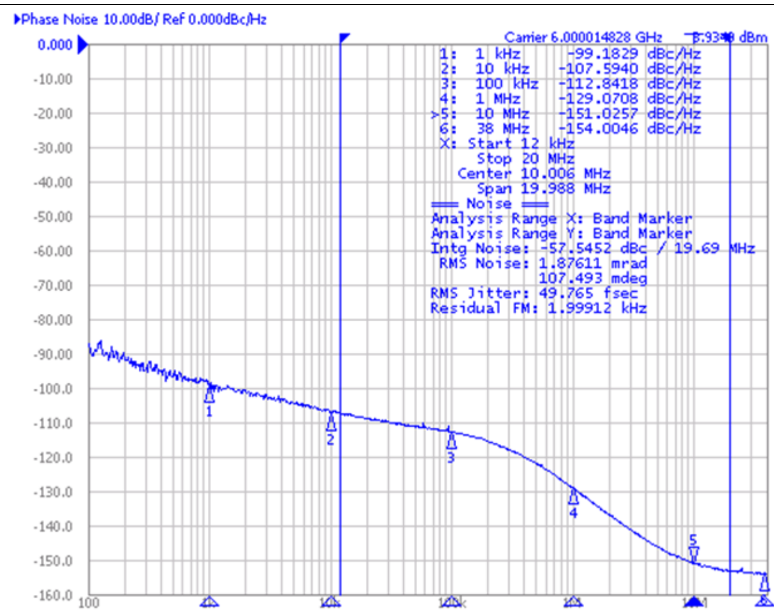


Figure 33. Typical Jitter

9 Power Supply Recommendations

It is recommended to place 100 nF close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree.

10 Layout

10.1 Layout Guidelines

See EVM instructions for details. In general, the layout guidelines are similar to most other PLL devices. The followings are some outstanding guidelines.

- Place output pull up components close to the pin.
- Place capacitors close to the pins.
- Make sure input signal trace is well matched.
- Do not route any traces that carrying switching signal close to the charge pump traces and external VCO.

10.2 Layout Example

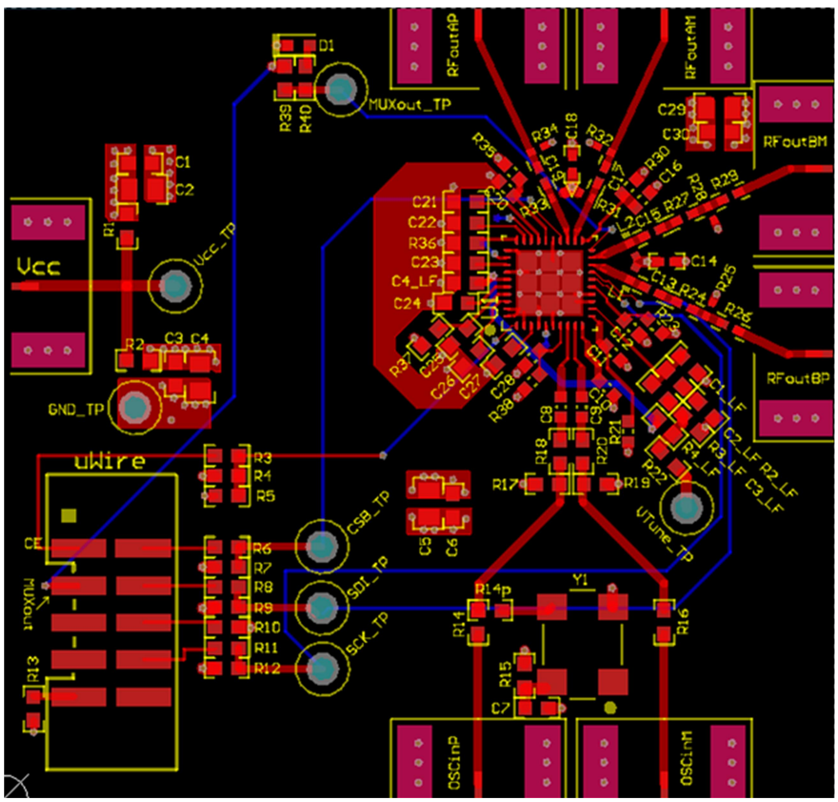


Figure 34. Recommended Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

德州仪器 (TI) 在 www.ti.com 提供了多种辅助开发的软件工具。其中包括：

- Codeloader，通过该工具可以了解如何编程 EVM 板。
- 时钟设计工具，用于设计回路滤波器、相位噪声仿真以及毛刺仿真。
- EVM 板说明，用于了解典型测量数据、详细测量条件以及完整设计的信息。
- 时钟架构，用于了解器件设计和仿真以及如何与其他器件搭配使用的信息。

11.2 文档支持

11.2.1 相关文档

以下为推荐读物。

- AN-1879*《分数 N 频率合成》*（文献编号：SNAA062）
- *《PLL 性能、仿真和设计手册》*（文献编号SNAA106）

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2592RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2592	Samples
LMX2592RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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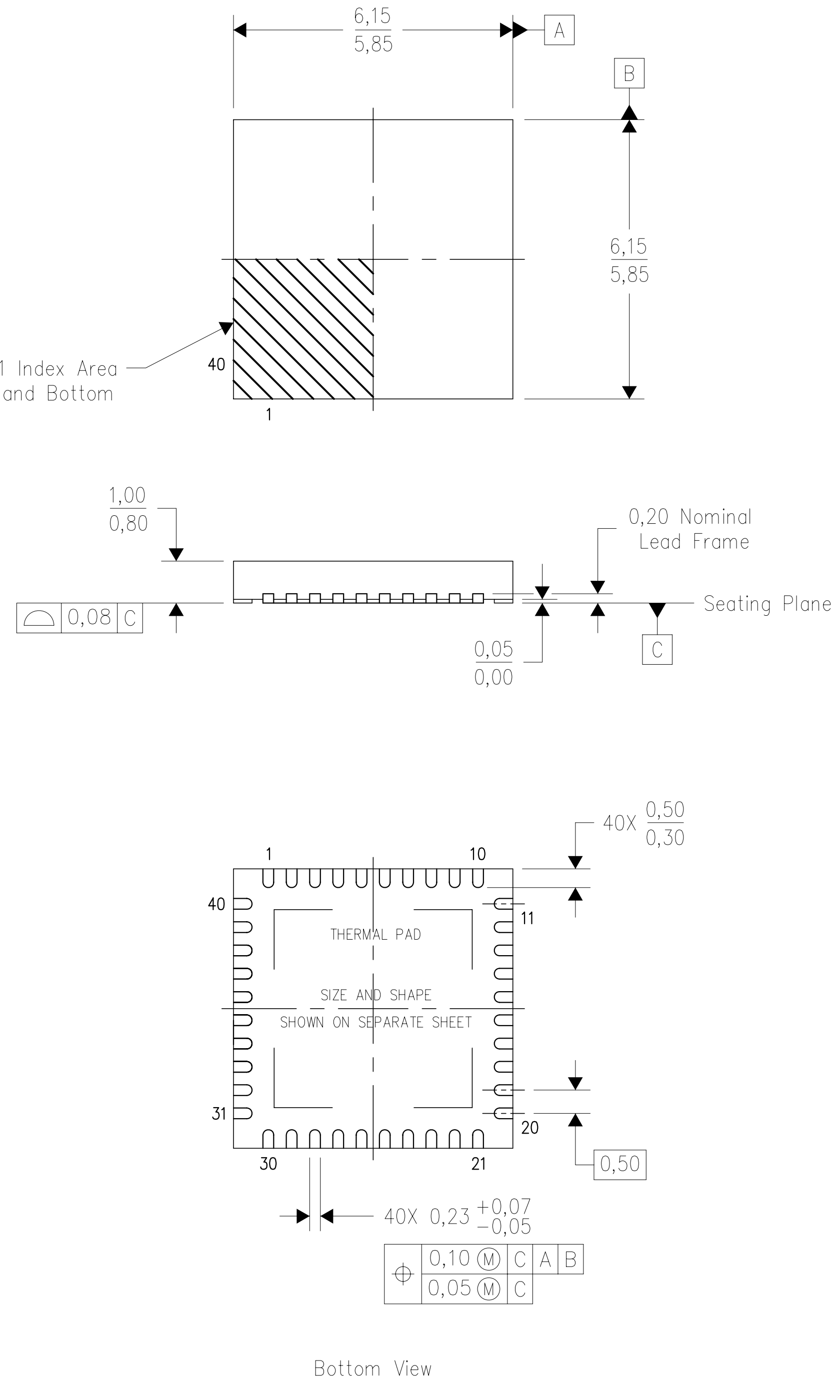
RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No−Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Package complies to JEDEC MO−220 variation VJJD−2.

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