TPS1H100-Q1 40-V, 100-mΩ Single-Channel Smart High-Side Power Switch

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C4B
- Single-Channel Smart High-Side Power Switch With Full Diagnostics
  - Version A: Open-Drain Status Output
  - Version B: Current Sense Analog Output
- Wide Operating Voltage 3.5 to 40 V
- Very-Low Standby Current, <0.5 µA
- Operating Junction Temperature, –40 to 150°C
- Input Control, 3.3-V and 5-V Logic Compatible
- High-Accuracy Current Sense, ±30 mA at 1 A, ±4 mA at 5 mA
- Programmable Current Limit With External Resistor, ±20% at 0.5 A
- Diagnostic Enable Function for Multiplexing of MCU Analog or Digital Interface
- Tested According to AECQ100-12 Grade A, 1 Million Times Short to GND Test
- Electrical Transient Disturbance Immunity Certification of ISO7637-2 and ISO16750-2
- Protection
  - Overload and Short-Circuit Protection
  - Inductive Load Negative Voltage Clamp
  - Undervoltage Lockout (UVLO) Protection
  - Thermal Shutdown/Swing With Self Recovery
  - Loss of GND, Loss of Supply Protection
  - Reverse Battery Protection With External Circuitry
- Diagnostic
  - On/Off State Output Open/Short to Battery Detection
  - Overload and Short to Ground Detection and Current Limit
  - Thermal Shutdown/Swing Detection
- 14-Pin Thermally-Enhanced PWP Package

2 Applications

- High-Side Power Switch for Sub-Module
- Low-Wattage Lamp Power Switch
- High-Side Relay/Solenoids
- PLC Digital Output Power Switch
- General Resistive, Inductive, and Capacitive Loads

3 Description

The TPS1H100-Q1 is a fully protected high-side power switch, with integrated NMOS power FET and charge pump, targeted for the intelligent control of the variable kinds of resistive, inductive, and capacitive loads. Accurate current sense and programmable current limit features differentiate it from the market.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS1H100-Q1	HTSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Schematic

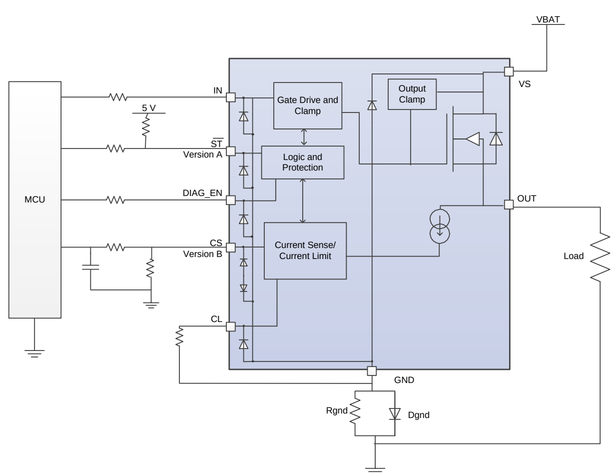


Table of Contents

5 Revision History

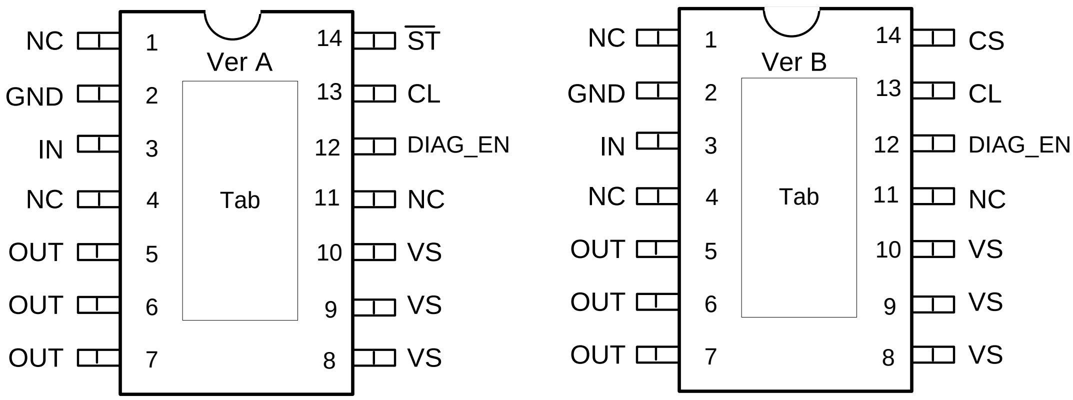
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2015) to Revision B	Page
• Updated Figure 6 and Figure 7	10
• Updated Figure 38	25
• Updated Figure 39	26
• Updated Figure 40	27
• Added *Community Resources*	39

Changes from Original (October 2014) to Revision A	Page
• Updated device status from preview to production data	1

6 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Top View



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION	
NC	1, 4, 11	—	No connect pin	Floating
GND	2	—	Ground pin	
IN	3	I	Input control for channel activation	
OUT	5, 6, 7	O	Output, connected to load (NMOS source)	
VS	8, 9, 10	I	Power supply; battery voltage	
DIAG_EN	12	I	Enable/disable pin for diagnostic functions	Connect to device GND if not used
CL	13	O	Programmable current limit pin	Connect to device GND if external current limit is not used
CS	14 (1)	O	Current sense output	Floating if not used
$\overline{\text{ST}}$	14 (2)	O	Open-drain diagnostic status output	Floating if not used
Tab	—	—	Thermal pad	Connect to device GND or floating

(1) Version B
(2) Version A

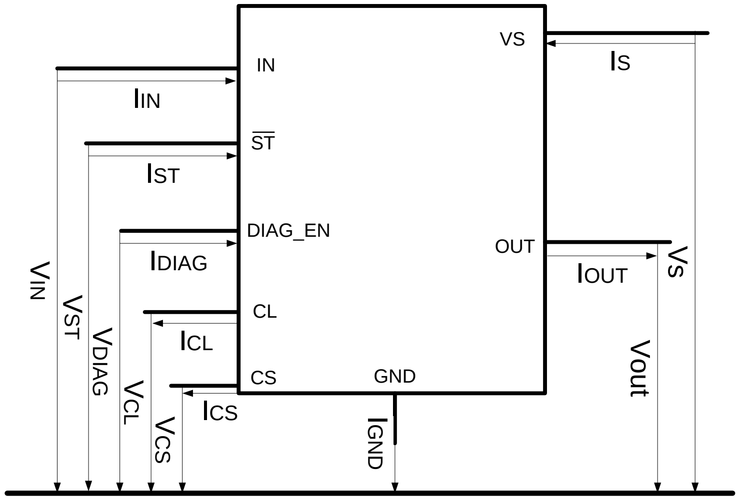


Figure 1. Pin Current and Voltage Conventions

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Supply voltage(4), t < 400 ms		48	V
Reverse polarity voltage(5)	–18		V
Continuous drain current	Internally limited		A
Reverse current on GND	–50	20	mA
Reverse current on GND, t < 120 s	–250	20	mA
Voltage on IN/DIAG_EN pin	–0.3	7	V
Current on IN /DIAG_EN pin	–30	2	mA
Voltage on $\overline{ST}$ pin	–0.3	7	V
Current on $\overline{ST}$ pin	–30	10	mA
IN pin PWM frequency		2	KHz
Voltage on CL pin	–0.3	7	V
Current on CL pin	–2	30	mA
Voltage on CS pin	–2.7	6.5	V
Current on CS pin	–2	30	mA
Inductive load switch-off energy dissipation single pulse(6)		70	mJ
Operating ambient temperature	–40	125	°C
Operating junction temperature	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute negative voltage on these terminals is not to go below –0.3 V.
(4) Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.
(5) Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-kΩ resistor in parallel with diode.
(6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-µm Cu, 2- × 35-µm Cu. 600-mm^2 thermal pad copper area.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) AEC-Q100 Classification Level H3A(1)	VS, OUT, GND	±5000	V
		Human body model (HBM) AEC-Q100 Classification Level H2(1)	Other pins	±4000	
		Charged device model (CDM), per AEC Q100-011(2)		±750	

(1) The human-body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
(2) The charged-device model is tested according to AEC_Q100-011C.

7.3 Recommended Operating Conditions

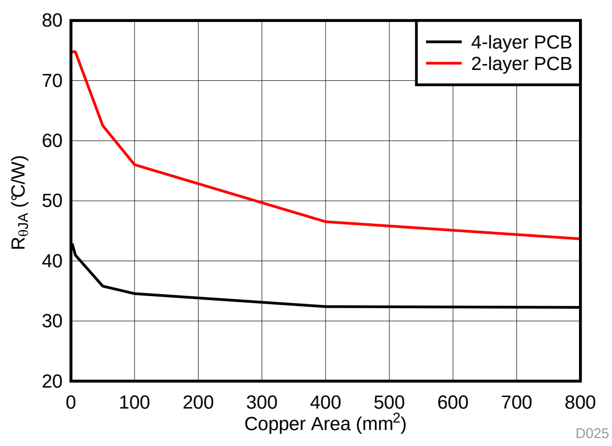
over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Operating voltage	5	40	V
	Voltage on IN/DIAG_EN pin	0	5	V
	Voltage on $\overline{ST}$ pin	0	5	V
$I_{o,nom}$	Nominal DC load current	0	4	A
T_J	Operating junction temperature range	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS1H100-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	41	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.



(1) 4-layer board: FR4 2s2p board, 2.8-mil copper (top/bottom), 1.4-mil copper (internal layers). 76.4- × 114.3- × 1.5-mm board size.
(2) 2-layer board: FR4 2s0p board, 2.8-mil copper (top/bottom). 76.4- × 114.3- × 1.5-mm board size.

Figure 2. $R_{\theta JA}$ Value vs Copper Area

7.5 Electrical Characteristics

5 V < V_S < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{S,nom}$	Nominal operating voltage		5		40	V
$V_{S,op}$	Extended operating voltage	$R_{DS\text{-}ON}$ value increases maximum 20%, compared to 5 V, see $R_{DS\text{-}ON}$ parameter	3.5		5	V
$V_{S,UVR}$	Undervoltage restart	V_S rises up, $V_S > V_{S,UVR}$, device turn on	3.5	3.7	4	V
$V_{S,UVF}$	Undervoltage shutdown	V_S falls down, $V_S < V_{S,UVF}$, device shuts off	3	3.2	3.5	V
$V_{UV,hys}$	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
I_{nom}	Nominal operating current	V_{IN} = 5 V, V_{DIAG_EN} = 0 V, no load			5	mA
		V_{IN} = 5 V, V_{DIAG_EN} = 0 V, 10-Ω load			10	mA
I_{off}	Standby current	V_S = 13.5 V, $V_{IN} = V_{DIAG\_EN} = V_{CS} = V_{CL} = V_{OUTPUT}$ = 0 V, T_J = 25°C			0.5	µA
		V_S = 13.5V, $V_{IN} = V_{DIAG\_EN} = V_{CS} = V_{CL} = V_{OUTPUT}$ = 0 V, T_J = 125°C			5	µA
$I_{off,diag}$	Standby current with diagnostic enabled	V_{IN} = 0 V, V_{DIAG_EN} = 5 V			1.2	mA
$t_{off,deg}$	Standby mode deglitch time(1)	IN from high to low, if deglitch time > $t_{off,deg}$, enters into standby mode.		2		ms
$I_{leak,out}$	Off-state output leakage current	V_S = 13.5 V, $V_{IN} = V_{OUTPUT}$ = 0, T_J = 25°C			0.5	µA
		V_S = 13.5 V, $V_{IN} = V_{OUTPUT}$ = 0, T_J = 125°C			3	µA
POWER STAGE						
$R_{DS\text{-}ON}$	On-state resistance	V_S > 5 V, T_J = 25°C		80	100	mΩ
		V_S > 5 V, T_J = 150°C			166	mΩ
		V_S = 3.5 V, T_J = 25°C			120	mΩ
$I_{lim,nom}$	Internal current limit		7		13	A
$Il_{im,tsd}$	Current limit during thermal shutdown	Internal current limit, thermal cycling condition		5		A
		External current limit, thermal cycling condition; Percentage of current limit set value		50%		
V_{DS}	Clamp drain-to-source voltage internally clamped		50		70	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain-to-source diode voltage	V_{IN} = 0, I_{OUT} = −0.2 A		0.7		V
I_{rev1}	Continuous reverse current when reverse polarity(2)	t < 60 s, V_S = 13.5 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. See I_{rev1} test condition (Figure 6).		4		A
I_{rev2}	Continuous reverse current when $V_{OUT} > V_S + V_{diode}$(2)	t < 60 s, V_S = 13.5 V. T_J = 25°C. See I_{rev2} test condition (Figure 7).		2		A
LOGIC INPUT (IN AND DIAG_EN)						
$V_{logic,h}$	Input/Diag_En high level voltage		2			V
$V_{logic,l}$	Input/Diag_En low level voltage				0.8	V
$V_{logic,hys}$	Input/Diag_En Hysteresis voltage			250		mV
$R_{pd,in}$	Input pulldown resistor			500		kΩ
$R_{pd,diag}$	Diag pulldown resistor			150		kΩ

(1) Value is specified by design, not subject to production test.
(2) Value are based on the minimum value of the 10 pcs/3 lots samples.

Electrical Characteristics (continued)

5 V < V_S < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
$I_{loss,gnd}$	Loss of ground output leakage current				100	µA
$V_{ol,off}$	Open load detection threshold in off state	V_{IN} = 0 V, When V_S – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.	1.4	1.8	2.6	V
$I_{ol,off}$	Off-state output sink current when open load	V_{IN} = 0 V, V_S = V_{OUT} = 13.5 V, T_J = 125°C.			–50	µA
$t_{ol,off}$	Open load detection threshold deglitch time in off state	V_{IN} = 0 V, When V_S – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.		600		µs
$I_{ol,on}$	Open load detection threshold in on state	V_{IN} = 5 V, when I_{OUT} < $I_{ol,on}$, duration longer than $t_{ol,on}$. Open load detected. Version A only	2	6	10	mA
$t_{ol,on}$	Open load detection threshold deglitch time in on state	V_{IN} = 5 V, when I_{OUT} < $I_{ol,on}$, duration longer than $t_{ol,on}$. Open load detected. Version A only		700		µs
V_{ST}	Status low output voltage	I_{ST} = 2 mA Version A only			0.4	V
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD,rst}$	Thermal shutdown status reset			155		°C
T_{sw}	Thermal swing shutdown threshold			60		°C
Thys	Hysteresis for resetting the thermal shutdown and swing			10		°C
CURRENT SENSE (VERSION B) AND CURRENT LIMIT						
K	Current sense current ratio			500		
K_{CL}	Current limit current ratio			2000		
dK/K	Current sense accuracy	I_{load} ≥ 5 mA	–80%		80%	
		I_{load} ≥ 25 mA	–10%		10%	
		I_{load} ≥ 50 mA	–7%		7%	
		I_{load} ≥ 0.1 A	–5%		5%	
		I_{load} ≥ 1 A	–3%		3%	
dK_{CL}/K_{CL}	External current limit accuracy	I_{limit} ≥ 0.5 A	–20%		20%	
		I_{limit} ≥ 1.6 A	–14%		14%	
$V_{CS,lin}$	Linear current sense voltage range (1)	V_S ≥ 5 V	0		4	V
$I_{OUT,lin}$	Linear output current range (1)	V_S ≥ 5 V, $V_{CS,lin}$ ≤ 4 V	0		4	A
$V_{CS,H}$	Current sense fault high voltage	V_S ≥ 7 V	4.3	4.75	4.9	V
		V_S ≥ 5 V	Min(V_S – 0.8, 4.3)		4.9	
$I_{CS,H}$	Current sense fault condition current	V_{CS} = 4.3 V, V_S > 7 V	10			mA
$V_{CL,th}$	Current limit internal threshold voltage (1)			1.233		V
$I_{CS,leak}$	Current sense leakage current in disabled mode	V_{IN} = 5 V, R_{load} = 10 Ω, V_{DIAG_EN} = 0 V, T_J = 125°C			1	µA
		V_{IN} = 0 V, V_{DIAG_EN} = 0 V, T_J = 125°C			1	µA

7.6 Timing Requirements – Current Sense Characteristics(1)

			MIN	NOM	MAX	UNIT
$t_{CS,off1}$	CS settling time from DIAG disabled	V_{IN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 5 to 0 V. CS to 10% of sense value.			10	µs
$t_{CS,on1}$	CS settling time from DIAG enabled	V_{IN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 0 to 5 V. CS to 90% of sense value.			10	µs
$t_{CS,off2}$	CS settling time from IN falling edge	V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. IN from 5 to 0 V. CS to 10% of sense value.			10	µs
		V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. IN from 5 to 0 V. Current limit triggered.			180	µs
$t_{CS,on2}$	CS settling time from IN rising edge	V_S = 13.5 V, V_{DIAG_EN} = 5 V, I_{load} ≥ 100 mA. V_{IN} from 0 to 5 V. CS to 90% of sense value.			150	µs

(1) Value specified by design, not subject to production test.

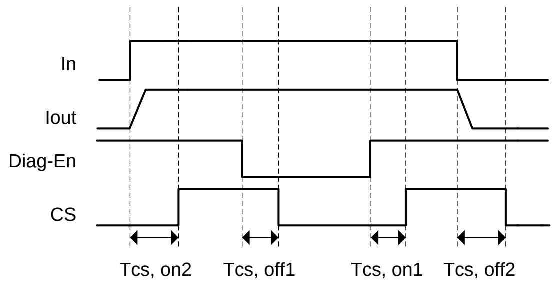


Figure 3. CS Delay Characteristics

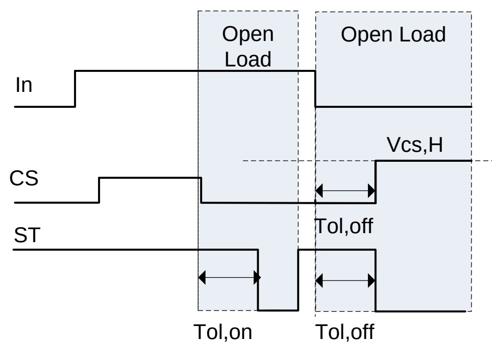


Figure 4. Open Load Blanking Time Characteristics

7.7 Switching Characteristics

V_S = 13.5 V, R_{load} = 10 Ω, over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d,ON}$	Turn-on delay time	IN rising edge to V_{OUT} = 10%, DIAG_EN high	20		50	µs
$t_{d,OFF}$	Turn-off delay time	IN falling edge to V_{OUT} = 90%, DIAG_EN high	20		50	µs
dV/dt_{ON}	Slew rate on	V_{OUT} = 10% to 90%, DIAG_EN high	0.1		0.5	V/µs
dV/dt_{OFF}	Slew rate off	V_{OUT} = 90% to 10%, DIAG_EN high	0.1		0.5	V/µs
	Slew rate on and off matching		–0.15		0.15	V/µs

(1) Value specified by design, not subject to production test.

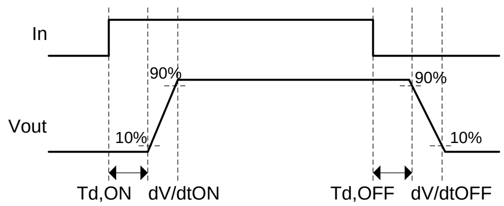


Figure 5. Switching Characteristics Diagram

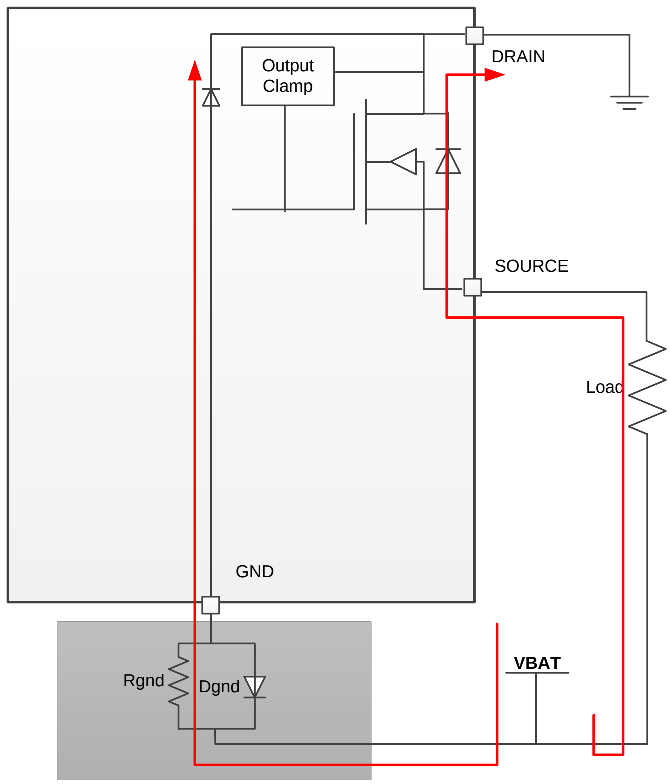


Figure 6. I_{rev1} Test Condition

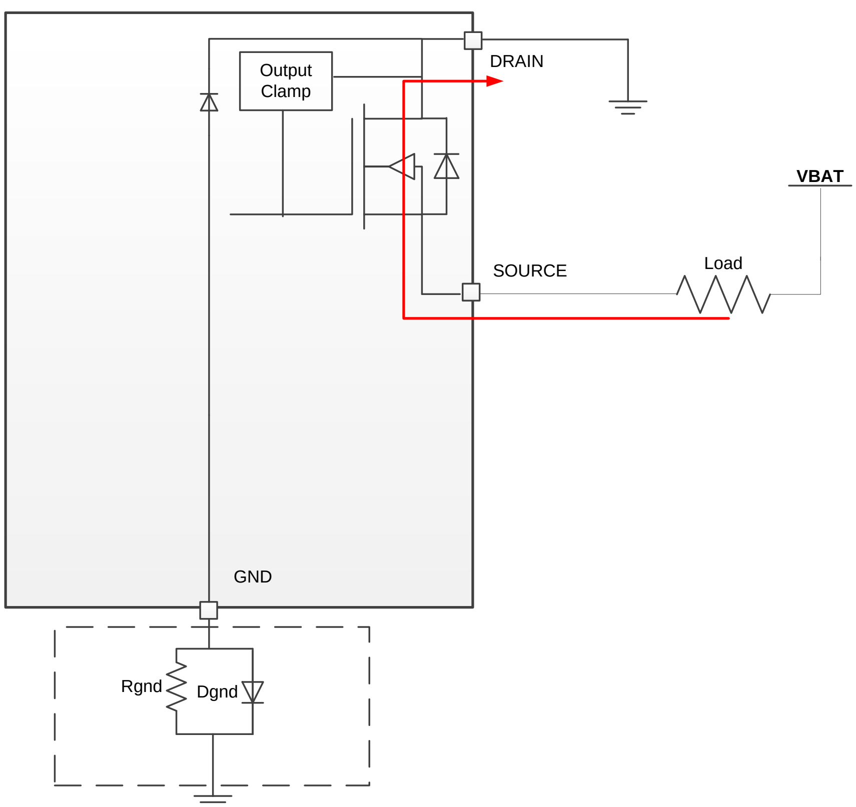


Figure 7. I_{rev2} Test Condition

7.8 Typical Characteristics

All the below data are based on the mean value of the three lots samples, V_S = 13.5 V if not specified.

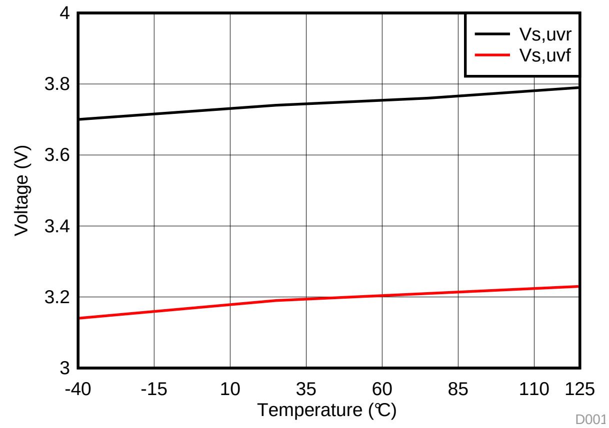


Figure 8. $V_{S,UVR}$ and $V_{S,UVF}$

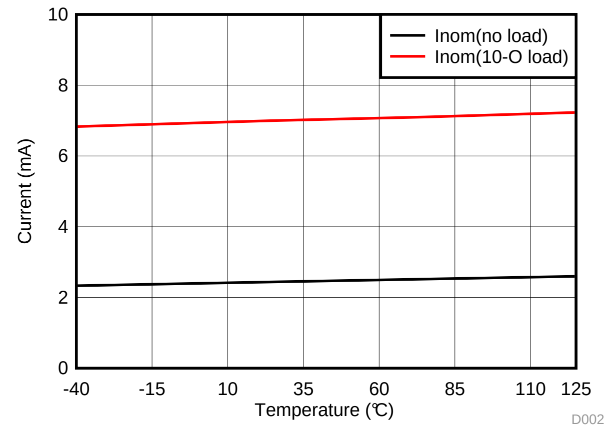


Figure 9. I_{nom} With No Load and 10-Ω Load

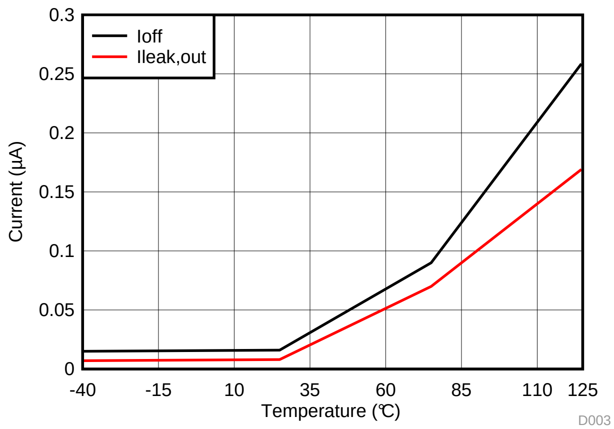


Figure 10. I_{off} and $I_{leak,out}$

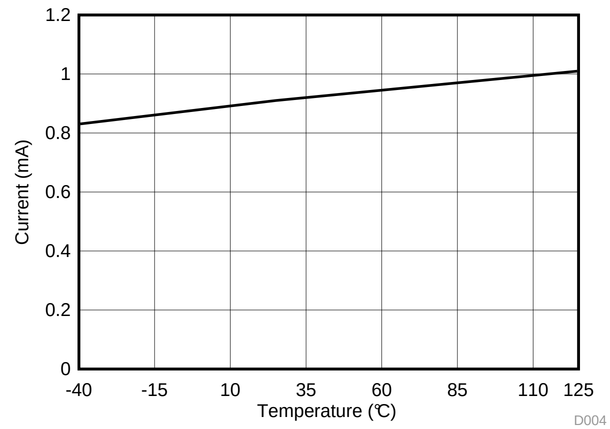


Figure 11. $I_{off,diag}$

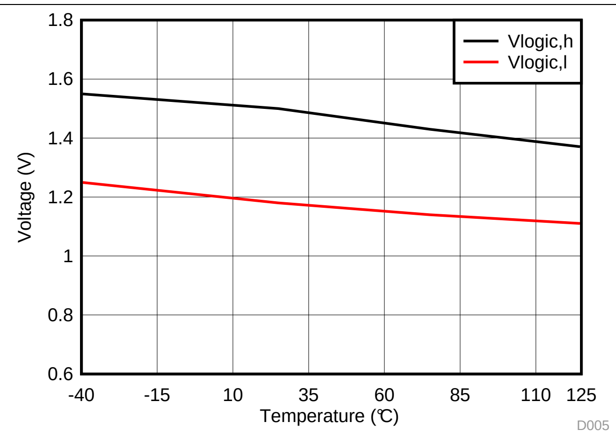


Figure 12. $V_{logic,h}$ and $V_{logic,l}$

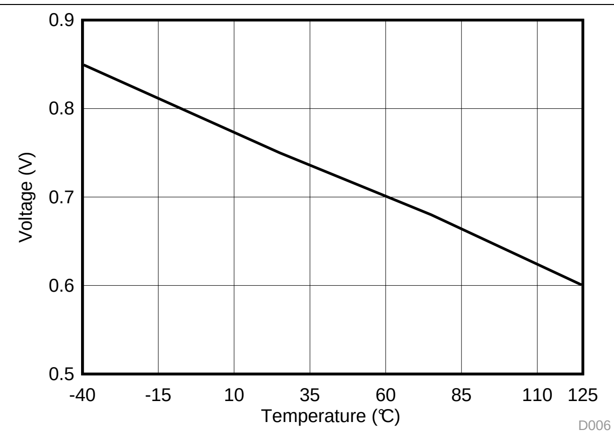


Figure 13. VF

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_S = 13.5 V if not specified.

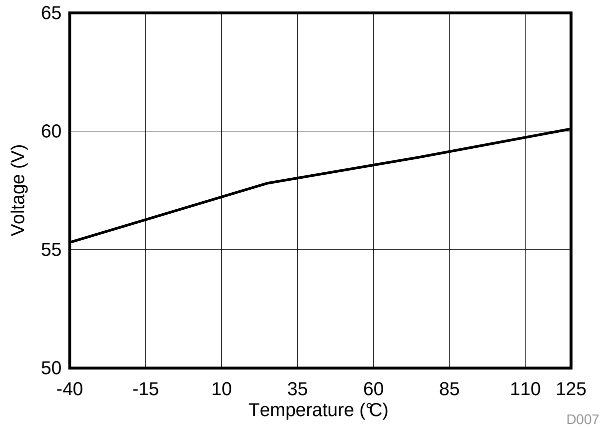


Figure 14. $V_{DS,\ clamp}$

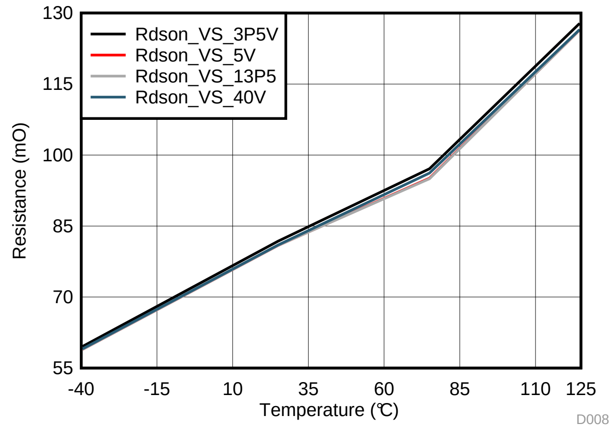


Figure 15. R_{DSON}

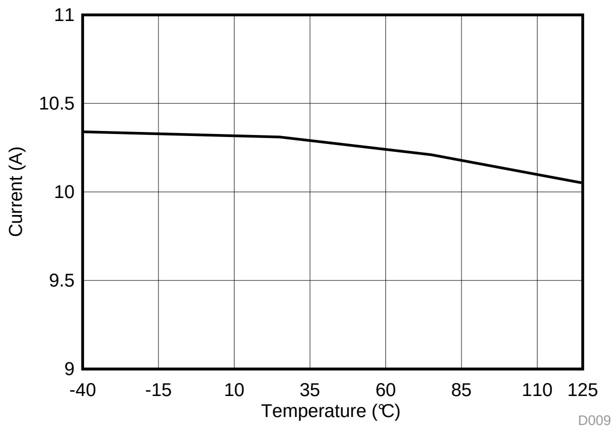


Figure 16. $I_{lim,nom}$

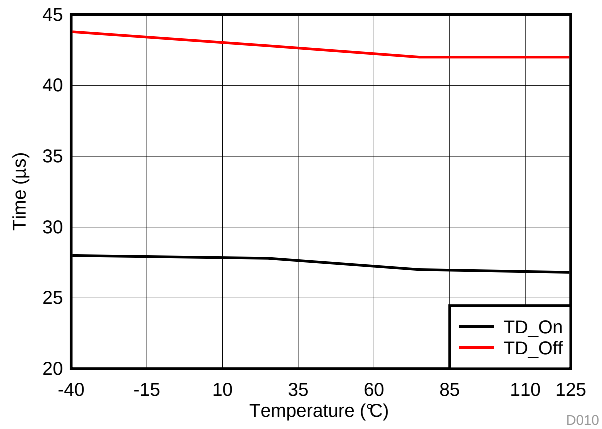


Figure 17. TDon and TDoff

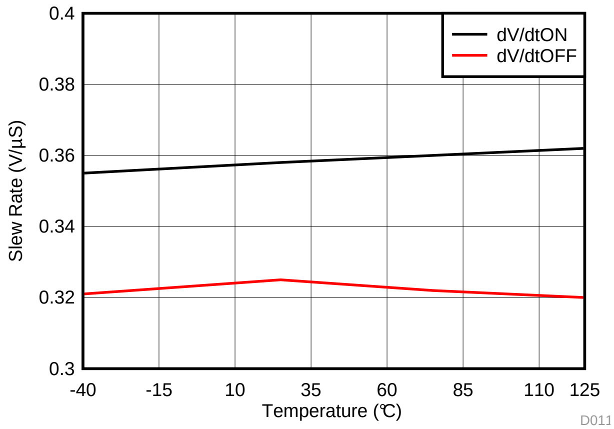


Figure 18. dV/dtON and dV/dtOFF

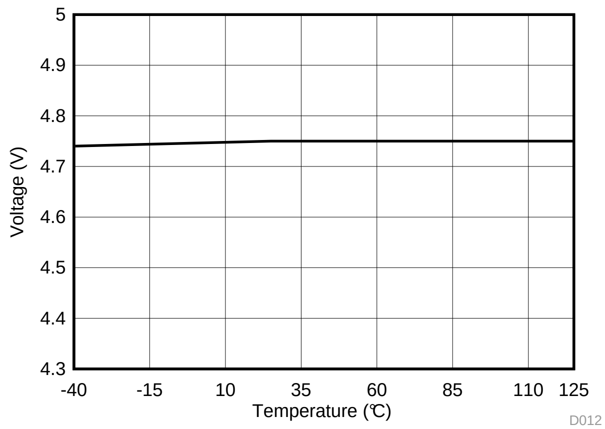


Figure 19. $V_{CS,h}$

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_S = 13.5 V if not specified.

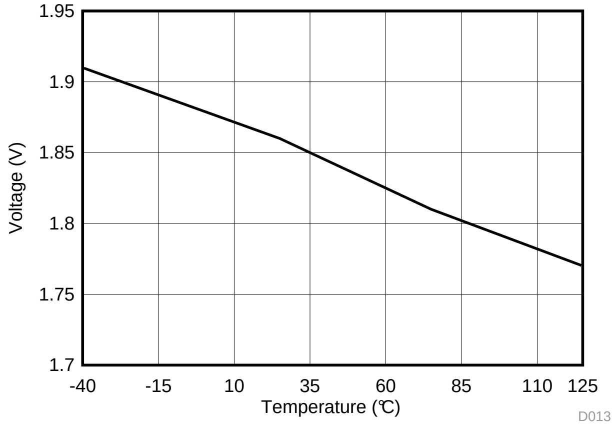


Figure 20. $V_{ol,off}$

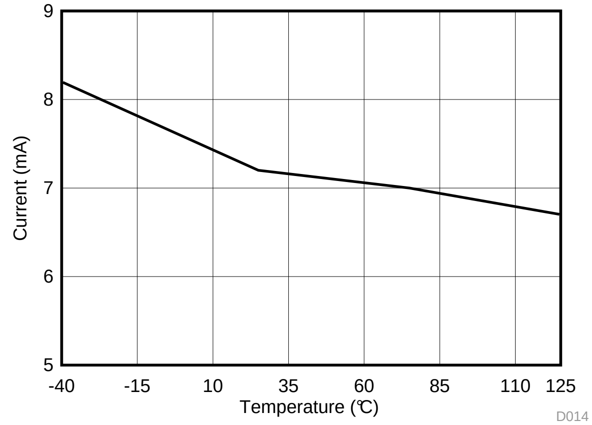


Figure 21. $I_{ol,on}$

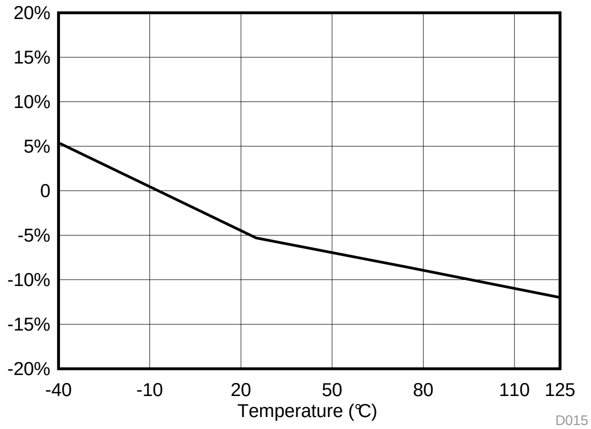


Figure 22. K_{CS} = 5 mA, 13.5 V

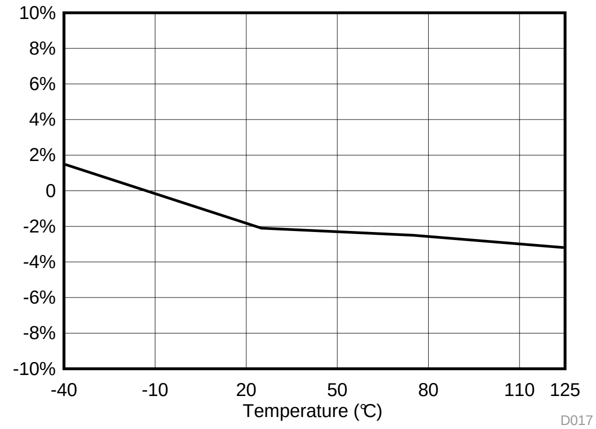


Figure 23. K_{CS} = 25 mA, 13.5 V

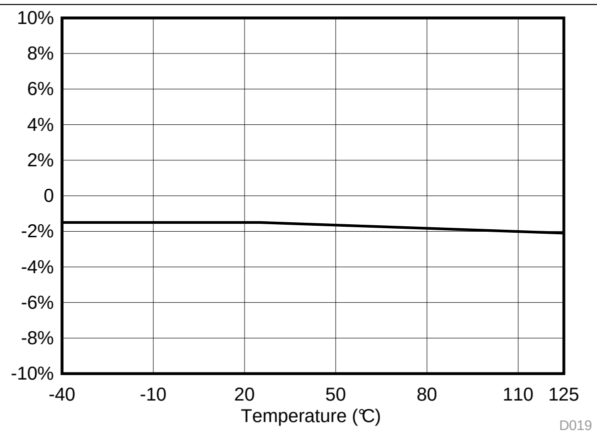


Figure 24. K_{CS} = 50 mA, 13.5 V

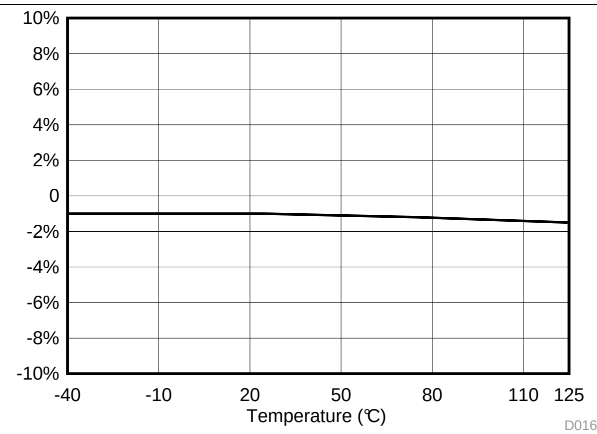


Figure 25. K_{CS} = 100 mA, 13.5 V

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_S = 13.5 V if not specified.

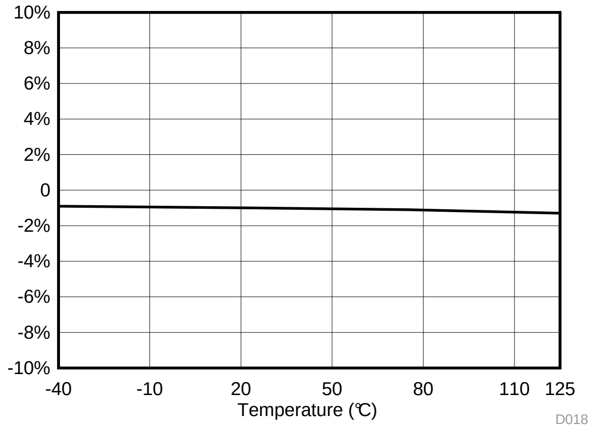


Figure 26. K_{CS} = 1 A, 13.5 V

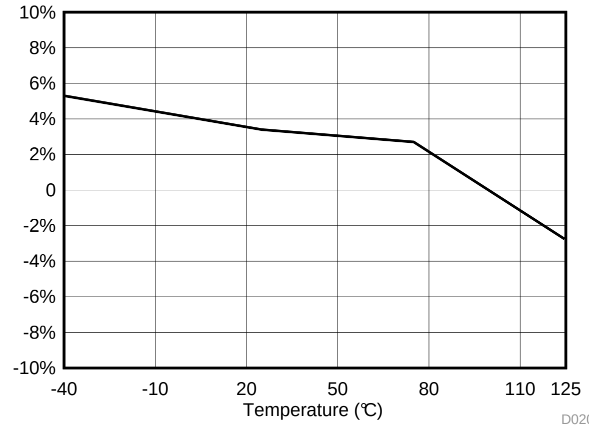


Figure 27. K_{CL} = 0.5 A, 13.5 V

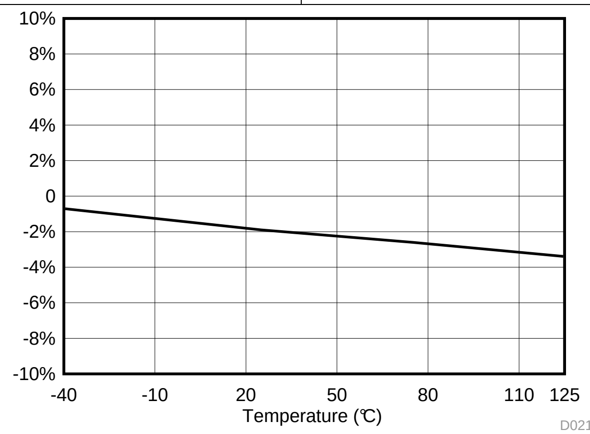


Figure 28. K_{CL} = 1.6 A, 13.5 V

8 Detailed Description

8.1 Overview

The TPS1H100-Q1 is a high-side power switch that is fully protected and single channel, with integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current sense features enable intelligent control of the load. Programmable current limit function greatly improves the whole system's reliability. The device diagnostic reporting has two versions to support both digital status and analog current sense output, both of which can be set as high impedance when diagnostics are disabled, for multiplexing the MCU analog or digital interface among devices.

For version A, the digital status report is implemented with an open-drain structure. When a fault condition happens, it pulls down to GND. 3.3- or 5-V external pullup is required to match the microcontroller's supply level. For version B, high-accuracy current sensing allows better real-time monitoring effect and more accurate diagnostics without further calibration. A current mirror is used to source 1 / K of the load current, which is reflected as voltage on the CS pin. K is a constant value across the temperature and supply voltage. Wide linear region from 0 to 4 V is presented for normal operation current sensing function. The CS pin can also report a fault with pulled up voltage of $V_{CS,h}$.

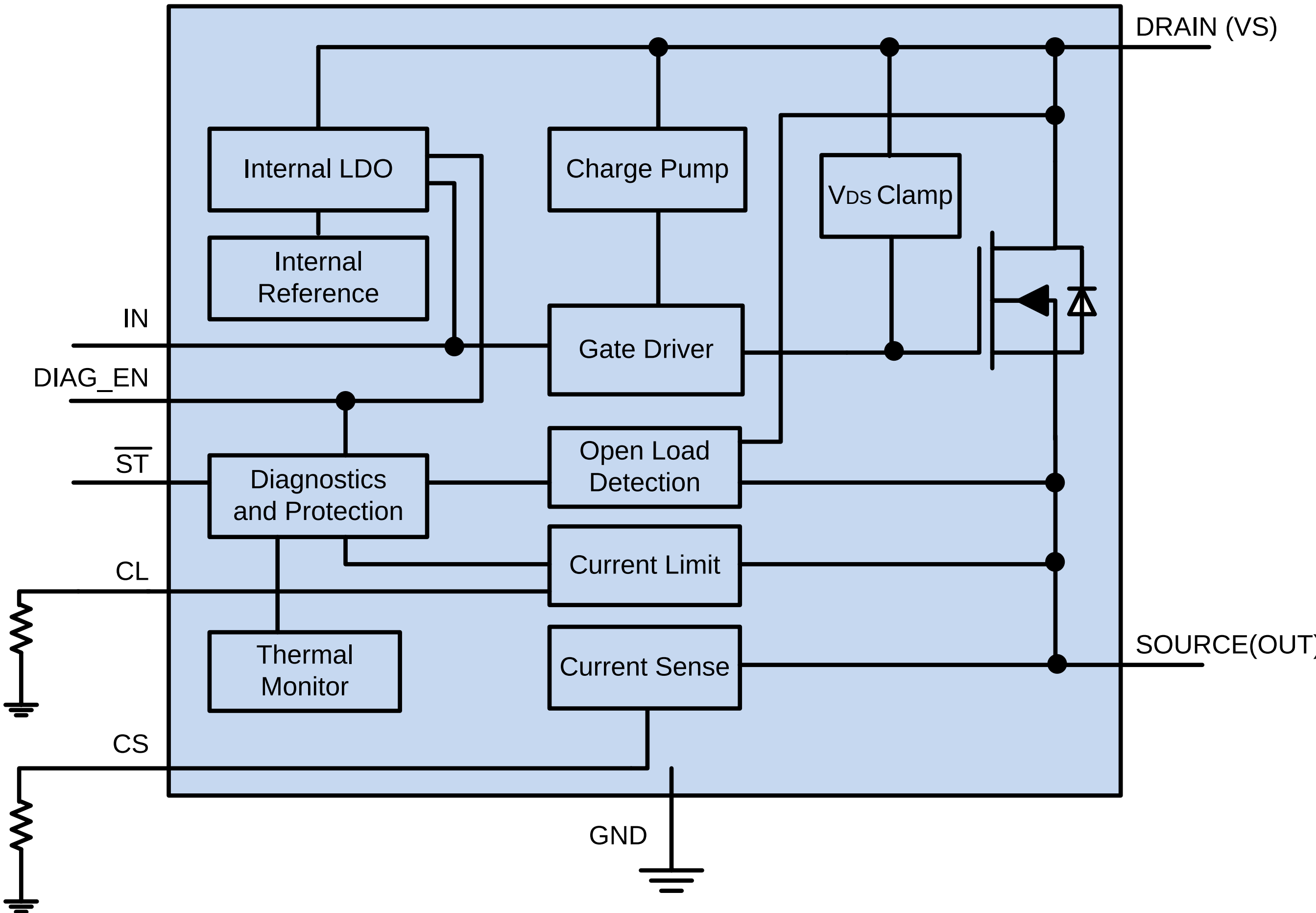
The external high-accuracy current limit allows setting the current limit value by application. It highly improves the system's reliability by clamping the inrush current effectively under start-up or short-circuit conditions. Also, it can save system costs by reducing PCB trace, connector size, and the preceding power stage capacity. Internal current limit is also implemented in this device. The smaller value of the external or internal current limit value is applied.

An active drain and source voltage clamp is built in to address switching off energy of inductive load, including the relays, solenoids, pumps, motors, and so forth. During the inductive switching off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, TPS1H100-Q1 can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. Refer to *Inductive Load Switching-Off Clamp* for more details.

Short circuit reliability is critical for smart high-side power switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short to GND certification.

TPS1H100-Q1 can be used as a high-side power switch a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Accurate Current Sense

For version B, the high-accuracy current sense function is internally implemented, which allows a better realtime monitoring effect and more accurate diagnostics without further calibration. A current mirror is used to source 1 / K of the load current, flowing out to the external resistor between the CS pin and GND, and reflected as voltage on CS pin.

K is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

Feature Description (continued)

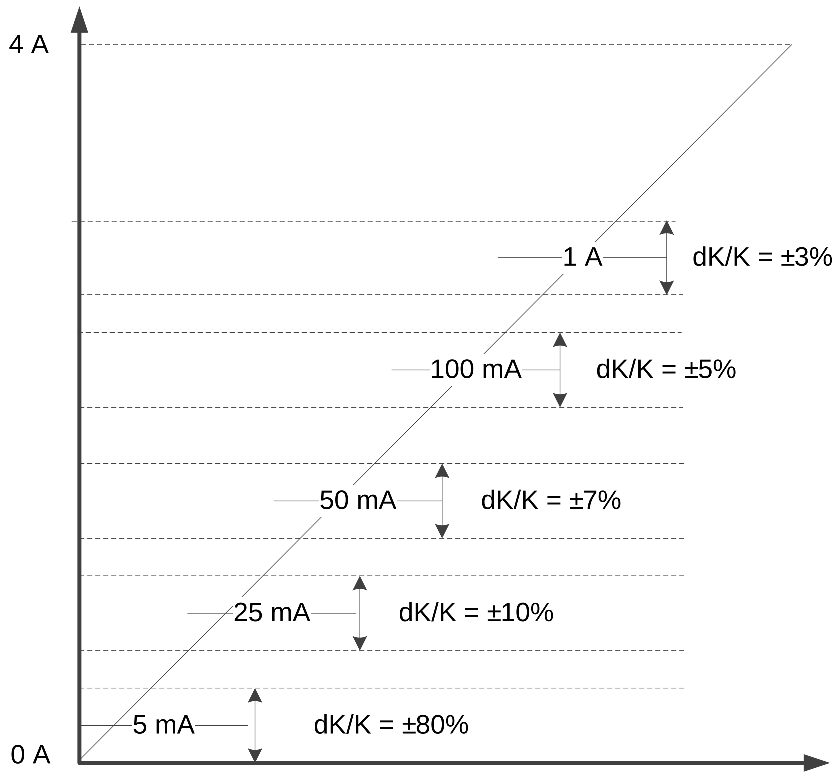


Figure 29. Current Sense Accuracy

Ensure the CS voltage is in the linear region (0 to 4 V) during normal operation. Calculate the R_{CS} with Equation 1.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K}{I_{out}} \quad (1)$$

Also, when a fault condition happens, CS works as a diagnostics report pin. When open load/short to battery happens in the on-state, V_{CS} almost equals 0. When current limit, thermal shutdown/swing, open load/short to battery in the off-state happens, the voltage is pulled up to $V_{CS,h}$. Figure 30 shows a typical current sense voltage according to the operating conditions, including fault conditions.

Feature Description (continued)

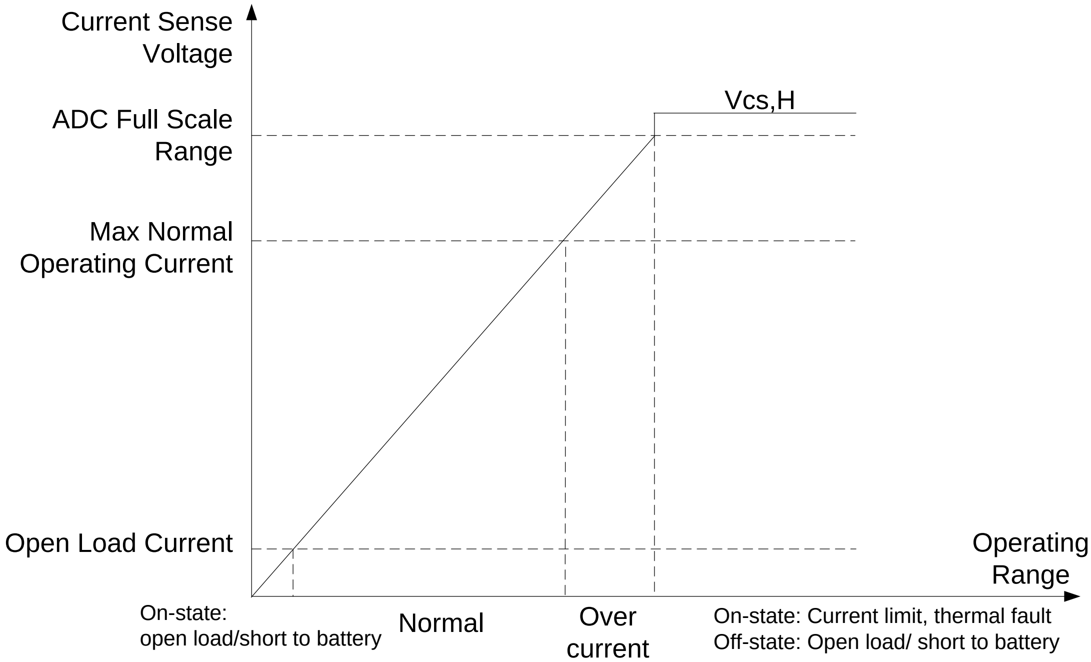


Figure 30. Current Sense Pin Voltage Indication

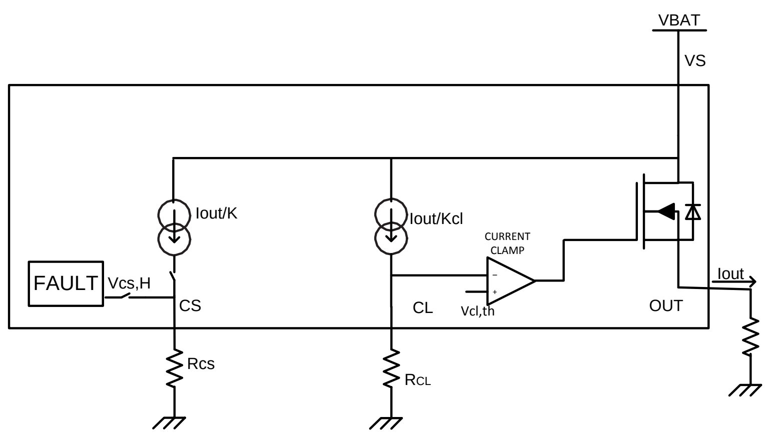


Figure 31. Current Sense and Current Limit Block Diagram

8.3.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power-up. Also, it can save system costs, by reducing PCB traces, connector size, and the preceding stage power capacity.

Current limit offers the protection to the load and integrated power FET from over stressing. It holds at the set value, and pulls up the CS pin to $V_{CS,h}$ as a diagnostic report. The two current limit thresholds are:

- External programmable current limit -- An external resistor is used to convert a proportional load current into a voltage, which is compared with an internal reference voltage, $V_{th,cl}$. When the voltage on the CL pin exceeds $V_{th.cl}$, a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{ds} voltage regulation. When the closed loop is set up, the current is clamped at the set value finally. The external programmable current limit enhances the flexibility to set the current limit value by application.
- Internal current limit -- Internal current limit is fixed and typically 10 A. To use internal current limit for large

Feature Description (continued)

current applications, the CL pin should be tied directly to the device GND.

Both internal current limit ($I_{lim,nom}$) and external programmable current limit are always active when V_S is powered and IN is high level. The smaller one (of $I_{lim,nom}$ and external programmable current limit) is applied as the actual current limit.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the CL pin must be connected with device GND. Calculate the R_{CL} with Equation 2.

$$I_{CL} = \frac{V_{CL,th}}{R_{CL}} = \frac{I_{out}}{K_{CL}} \rightarrow R_{CL} = \frac{V_{CL,th} \times K_{CL}}{I_{out}} \quad (2)$$

For better protection from the hard short to GND condition (when V_S and input are high and a short to GND happens suddenly), an open loop fast-response behavior is set to turn off the channel, before the current limit closed loop is set-up. The open loop response time is around 1 µs. With this fast response, the device can achieve better inrush suppression performance.

8.3.3 Inductive Load Switching-Off Clamp

When inductive load is switching off, output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the demagnetization. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,clamp}$, the clamp diode between the drain and gate.

$$V_{DS,clamp} = V_{BAT} - V_{OUT} \quad (3)$$

During the duty of demagnetization (T_{DECAY}), the power FET is turned on for inductance energy dissipation. Both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy will be dissipated on the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \quad (4)$$

From the high-side power switch's view, E_{HSD} equals the integration value during the demagnetization duty.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \quad (5)$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \quad (6)$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (7)$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (8)$$

Feature Description (continued)

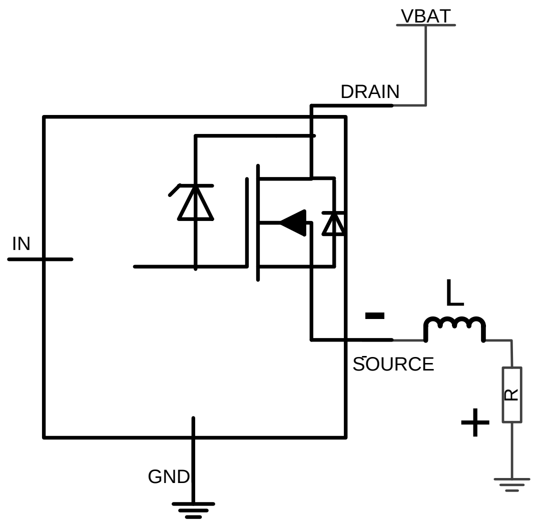


Figure 32. Driving Inductive Load

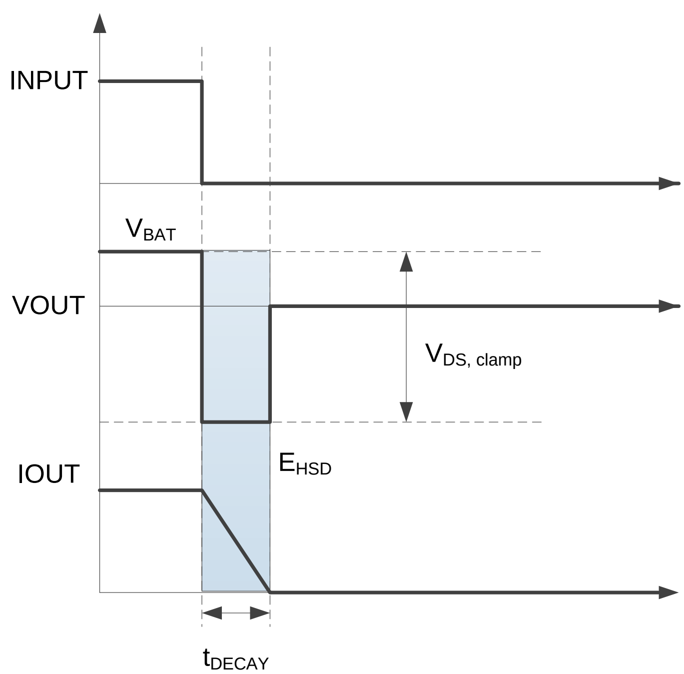


Figure 33. Inductive Load Switching Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition. TI provides the upper limit of the maximum single pulse energy that devices can tolerant under the test condition: V_S = 13.5 V, inductance from 0.1 to 400 mH, R = 0 Ω, FR4 2s2p board, 2- × 70-µm copper, 2- × 35-µm copper, thermal pad copper area 600 mm^2.

For one dedicated inductance, users can refer to Figure 34. If the maximum switching off current is smaller than the current value shown on the curve, the internal clamp function can be used for the demagnetization energy dissipation. If not, the external free-wheeling circuitry is necessary for device protection.

Feature Description (continued)

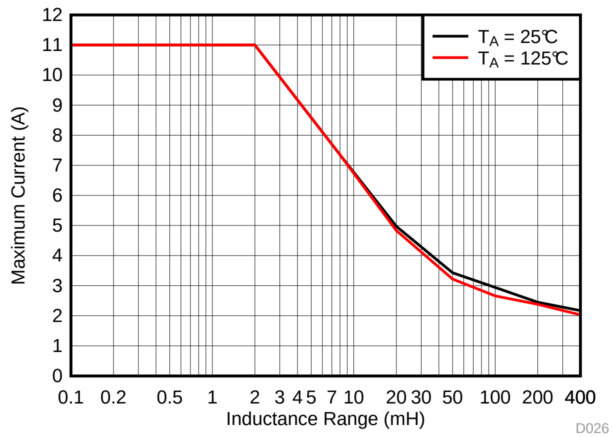


Figure 34. Maximum Current vs Inductance Range

8.3.4 Full Protections and Diagnostics

Table 1 is when DIAG_EN enabled. When DIAG_EN is low, current sense or ST is disabled accordingly. The output is in high-impedance mode. Refer to Table 2 for details.

Table 1. Fault Table

CONDITIONS	IN	OUT	CRITERION	$\overline{ST}$ (Version A)	CS (Version B)	Diagnostics Recovery
Normal	L	L		H	0	
	H	H		H	In linear region	
Short to GND	H	L	Current limit triggered.	L	$V_{CS,h}$	AUTO
Open load (1) Short to battery Reverse polarity	H	H	Version A: Output current < $I_{ol,on}$ Version B: Judged by users	L (deglitch)	Almost 0	AUTO
	L	H	$V_S - V_{OUT} < V_{ol,off}$	L (deglitch)	$V_{CS,h}$ (deglitch)	AUTO
Thermal shutdown	H		TSD triggered	L	$V_{CS,h}$	Recovery when temp < $T_{SD,rst}$
Thermal swing	H		T_{sw} triggered	L	$V_{CS,h}$	AUTO

(1) Need external pullup resistor during off-state

Table 2. DIAG_EN Logic Table

DIAG_EN	IN Condition	Protections and Diagnostics
HIGH	ON	See Table 1
	OFF	See Table 1
LOW	ON	Diagnostics disabled, protection normal CS or $\overline{ST}$ is high Impedance
	OFF	Diagnostics disabled, no protections CS or $\overline{ST}$ is high impedance

8.3.4.1 Short to GND/Overload Detection

In the on state, the short to GND fault is reported as the low status output or $V_{CS,h}$ on CS, when current limit is triggered. The smaller one of the internal or external set value is applied for the actual current limit. It is in auto-recovery when the fault condition is cleared. If not cleared, thermal shutdown triggers to protect the power FET.

8.3.4.2 Open Load Detection

In the on state, for version A, if the current flowing through the output is less than $I_{ol,on}$, the device recognizes an open load fault. For version B, diagnostics are diagnosed by reading the voltage on the CS pin, it is judged by the user. As a benefit from high accuracy current sense down to very-small current range, this device can achieve very-low open load detection threshold, which respectively expands the normal operation region. TI suggests 10 mA as the upper limit for the open-load detection threshold and 25 mA as the lower limit for the normal operation current. In Figure 35, the recommended open load detection region is shown as the dark-shaded region and the light-shaded region is for normal operation. As a guideline, do not overlap these two regions.

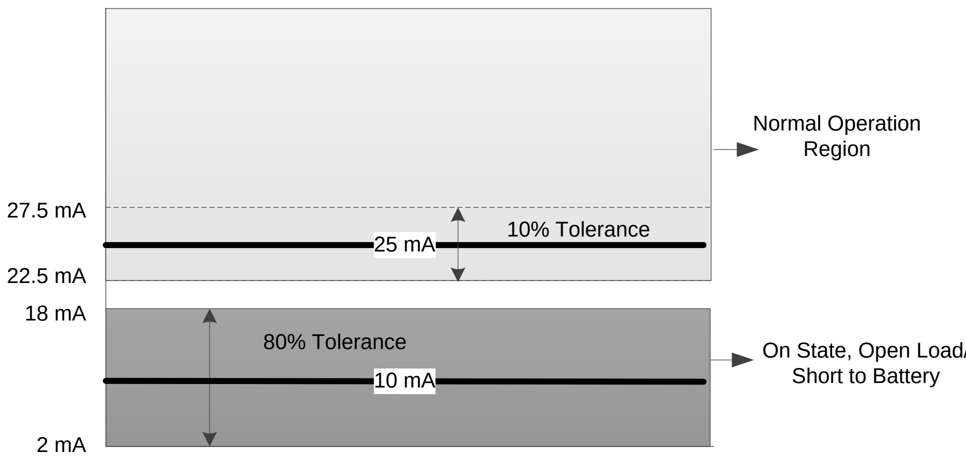


Figure 35. On-State Open Load Detection and Normal Operation Diagram

In the off state, if a load is connected, the output voltage is pulled to 0 V. When open load, the output voltage is close to the supply voltage, $V_S - V_{OUT} < V_{ol,off}$. For version A, the ST pin will go low to indicate the fault to MCU. For version B, the CS pin will be pulled up to $V_{CS,h}$. There is always a leakage current $I_{ol,off}$ present on the output, due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current. This pullup current should be less than output load current to avoid misdetection in the normal operation mode. To reduce the standby current, TI recommends to always use a switch for the pullup resistor. TI recommends $R_{pu} \leq 15$ kΩ.

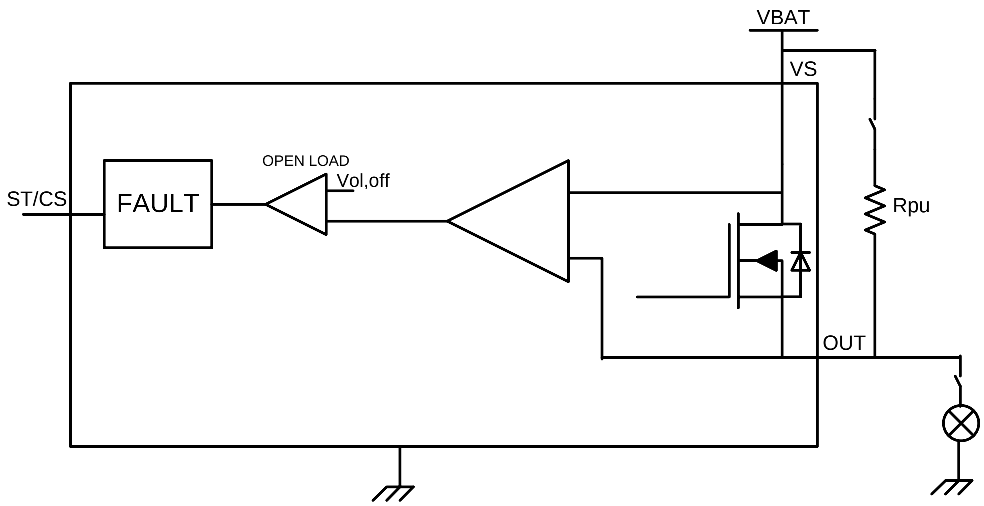


Figure 36. Open Load Detection Circuit

8.3.4.3 Short to Battery Detection

Short to battery has the same detection mechanism and behavior as open load both in the on-state and off-state. Refer to the fault truth table, Table 1, for more details. In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case for off-state is when reverse current occurs. In the off-state, if $V_{OUT} – V_S < V_F$, short to battery can be detected. (V_F is the body diode forward voltage and typically 0.7 V.) However, the reverse current will not occur. If $V_{OUT} – V_S > V_F$, short to battery can be detected, and the reverse current should be smaller than I_{rev2} to ensure the survival of the device. TI recommends switching on the input for lower power dissipation or the reverse block circuitry for the supply. Refer to *Reverse Current Protection* for more external protection circuitry information.

8.3.4.4 Reverse Polarity Detection

Reverse polarity has the same detection mechanism and behavior as open load both in the on-state and off-state. Refer to the fault truth table, Table 1, for more details. In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case off-state is when reverse current occurs. In off-state, the reverse current should be smaller than I_{rev1} to ensure the survival of the device. Refer to *Reverse Current Protection* for more external protection circuitry information.

8.3.4.5 Thermal Protection Behavior

Both the absolute temperature thermal shutdown and the dynamic temperature thermal swing diagnostic and protection are built in to the device to increase the max reliability of the power FET. Thermal swing is active when the temperature of the power FET is increasing sharply, that is $\Delta T = T_{DMOS} – T_{Logic} > T_{sw}$, then the output is shut down, and the ST pin goes low, or the CS pin is pulled up to $V_{CS,h}$. It auto-recovers and clears the fault signal until $\Delta T = T_{DMOS} – T_{Logic} < T_{sw} – T_{hys}$. Thermal swing function improves the device's reliability against repetitive fast thermal variation, as shown in Figure 37. Multiple thermal swings are triggered before thermal shutdown happens. Thermal shutdown is active when absolute temperature $T > T_{SD}$. When active, the output is shut down, and the ST pin goes low, or the CS pin pulled up to $V_{CS,h}$. The output is auto-recovered when $T < T_{SD} – T_{hys}$; the current limit is reduced to $I_{lim,tsd}$, or half of the programmable current limit value, to avoid repeated thermal shutdown. However, the thermal shutdown fault signal and half current limit value are not cleared until the junction temperature decreases to less than $T_{SD,rst}$.

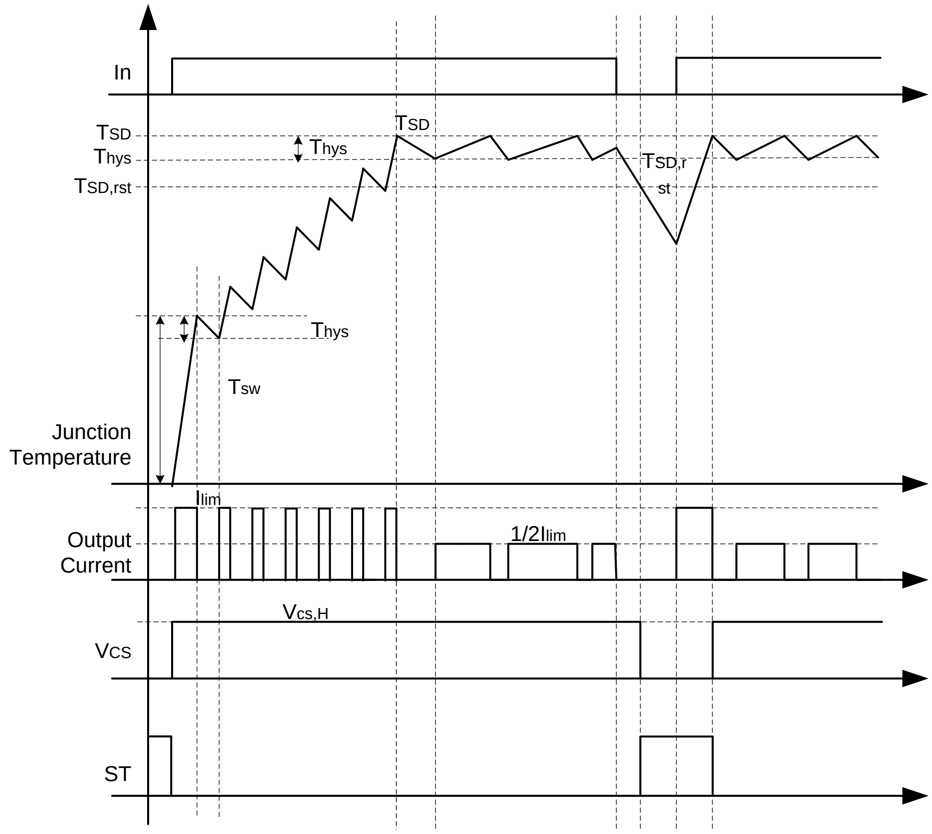


Figure 37. Thermal Behavior

8.3.4.6 UVLO Protection

The device monitors the supply voltage V_S to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to $V_{S,UVF}$, the output stage is shut down automatically. When the supply rises up to $V_{S,UVR}$, the device turns on.

8.3.4.7 Loss of GND Protection

When loss of GND happens, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of device GND): Loss of GND protection is active when the Tab, I_{C_GND}, and current limit GND are one trace connected to the board GND, as shown in Figure 38. Tab floating is also a choice.

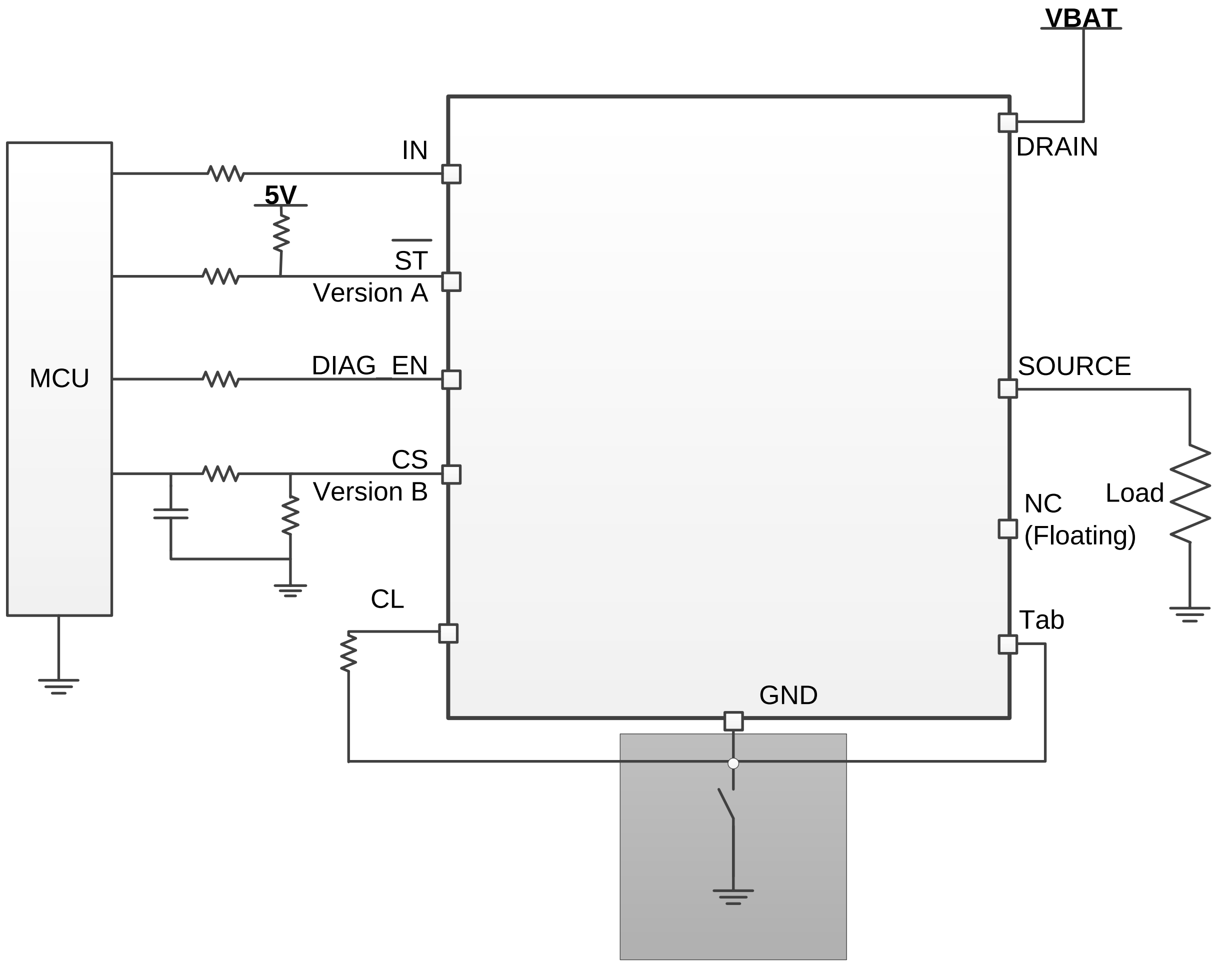


Figure 38. Loss of Device GND

Case 2 (loss of module GND): When the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

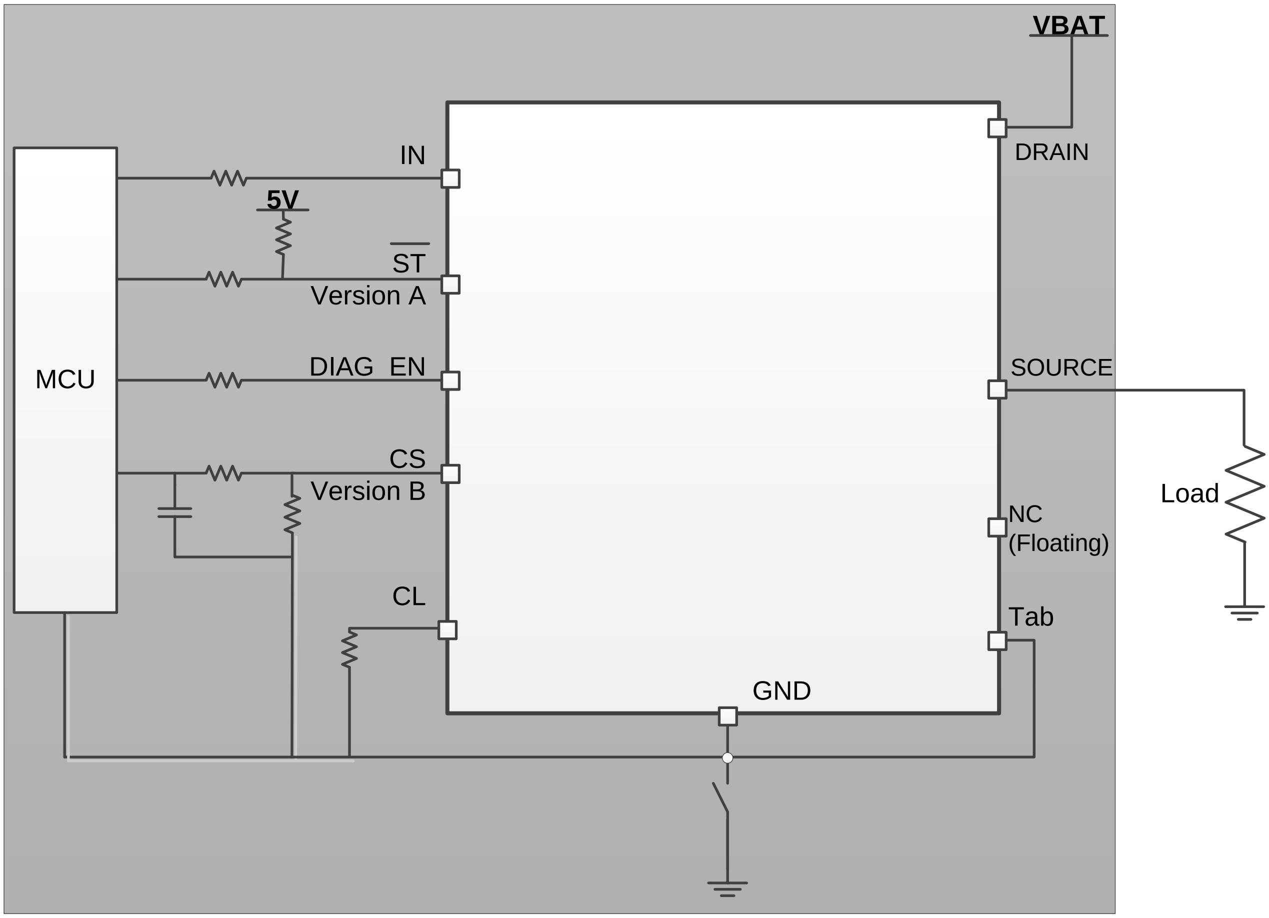


Figure 39. Loss of Module GND

8.3.4.8 Loss of Power Supply Protection

When loss of supply happens, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

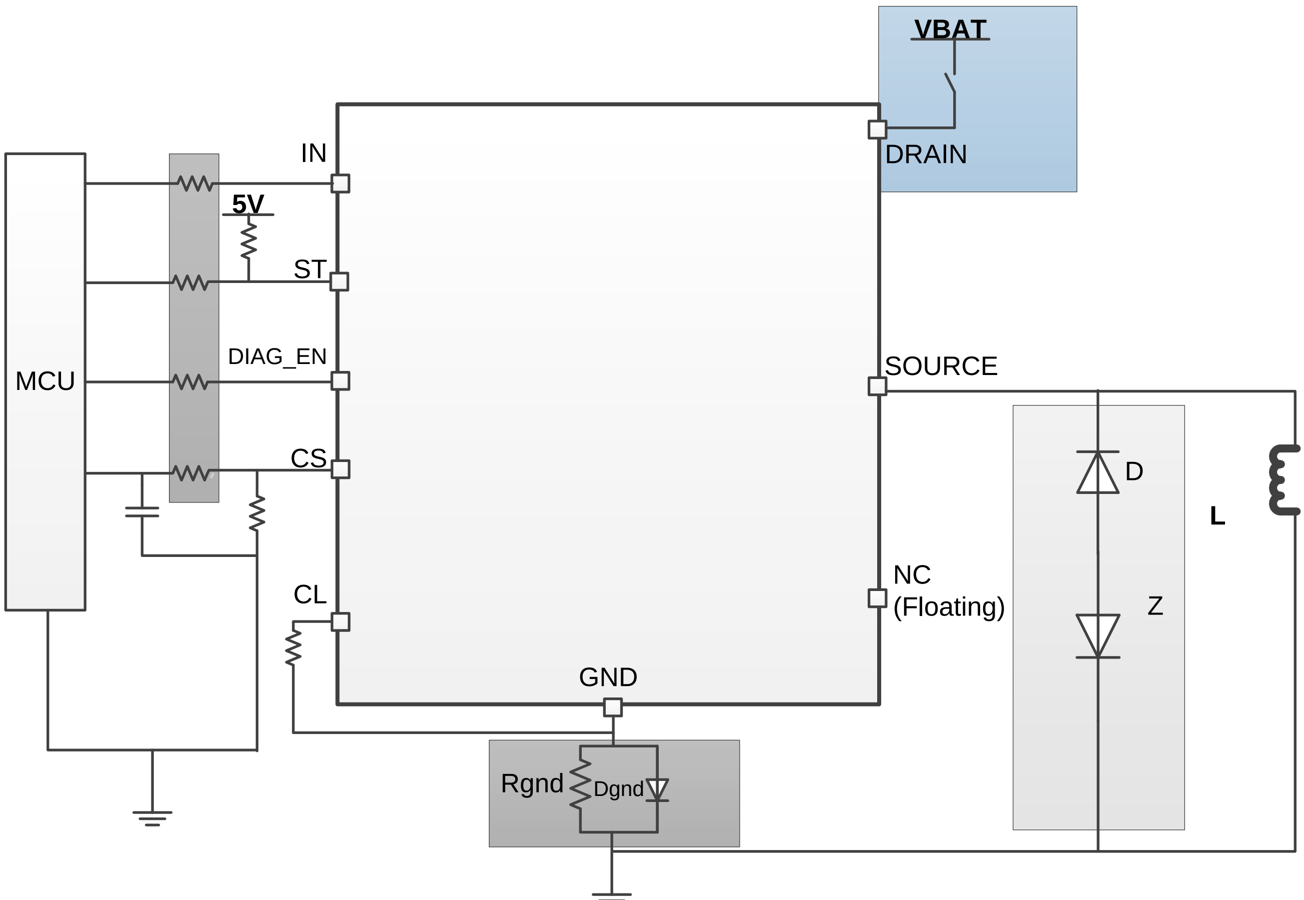


Figure 40. Loss of Battery

8.3.4.9 Reverse Current Protection

Method 1: Block diode connected with V_S. Both the IC and load are protected when in reverse polarity.

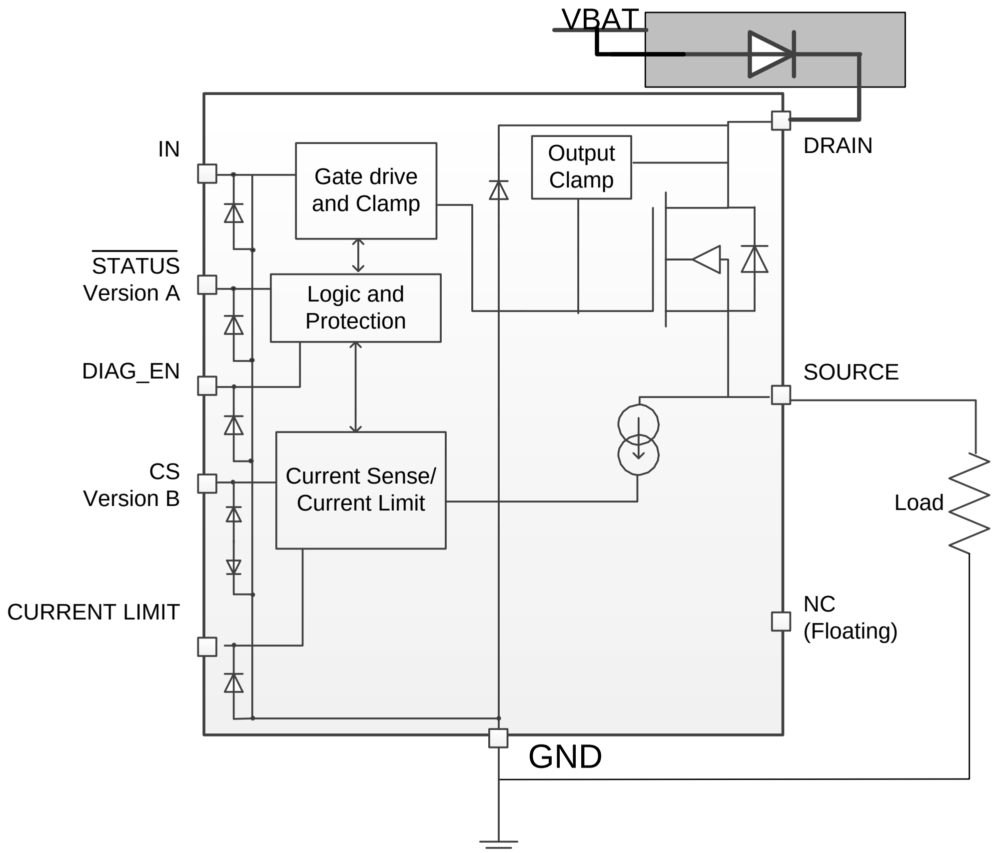


Figure 41. Reverse Protection With Block Diode

Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse loop is limited by the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET should be less than I_{rev}. Of the three types of ground pin networks, TI strongly recommends type 3 (the resistor and diode in parallel). No matter what types of connection are between IC GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Leave the NC pin floating or connect to the IC GND. TI recommends to leave floating.
- Connect the current limit programmable resistor to IC GND.

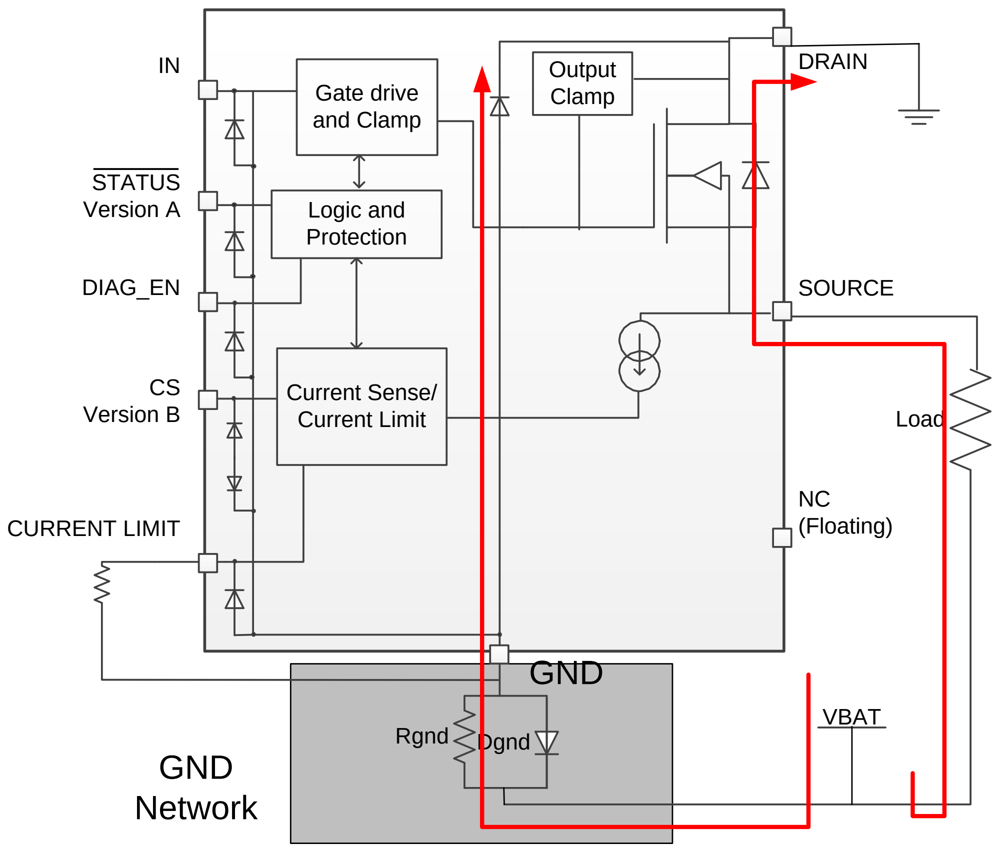


Figure 42. Reverse Protection With GND Network

- **Type 1 (resistor):** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses. However, it leads to higher GND shift during normal operation mode. Also, consider the resistor's power dissipation.

$$R_{GND} \leq \frac{V_{GNDshift}}{I_{nom}} \quad (9)$$

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \quad (10)$$

where

  - $V_{GNDshift}$ is the maximum value for the GND shift, determined by the HSD and microcontroller. TI suggests a value ≤ 0.6 V.
  - I_{nom} is the nominal operating current.
  - $–V_{CC}$ is the maximum reverse voltage seen on the battery line.
  - $–I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Type 2 (diode):** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600 mV).

However, an inductive load is not acceptable to avoid an abnormal status when switching off.

- **Type 3 (resistor and diode in parallel (recommended)):** A peak negative spike may occur when the inductive load is switching off, which may damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are 1-kΩ resistor in parallel with an I_F > 100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

8.3.4.10 MCU IOs Protection

In many conditions, such as the negative ISO pulse, or the loss of battery when inductive load, a negative potential on the IC GND pin may damage the MCU's I/O pins. Therefore, the serial resistors between MCU and HSD are required.

Also, for the proper protection of loss of GND, TI recommends 4.7 kΩ when using 3.3-V MCU I/Os; 10 kΩ is for 5-V applications.

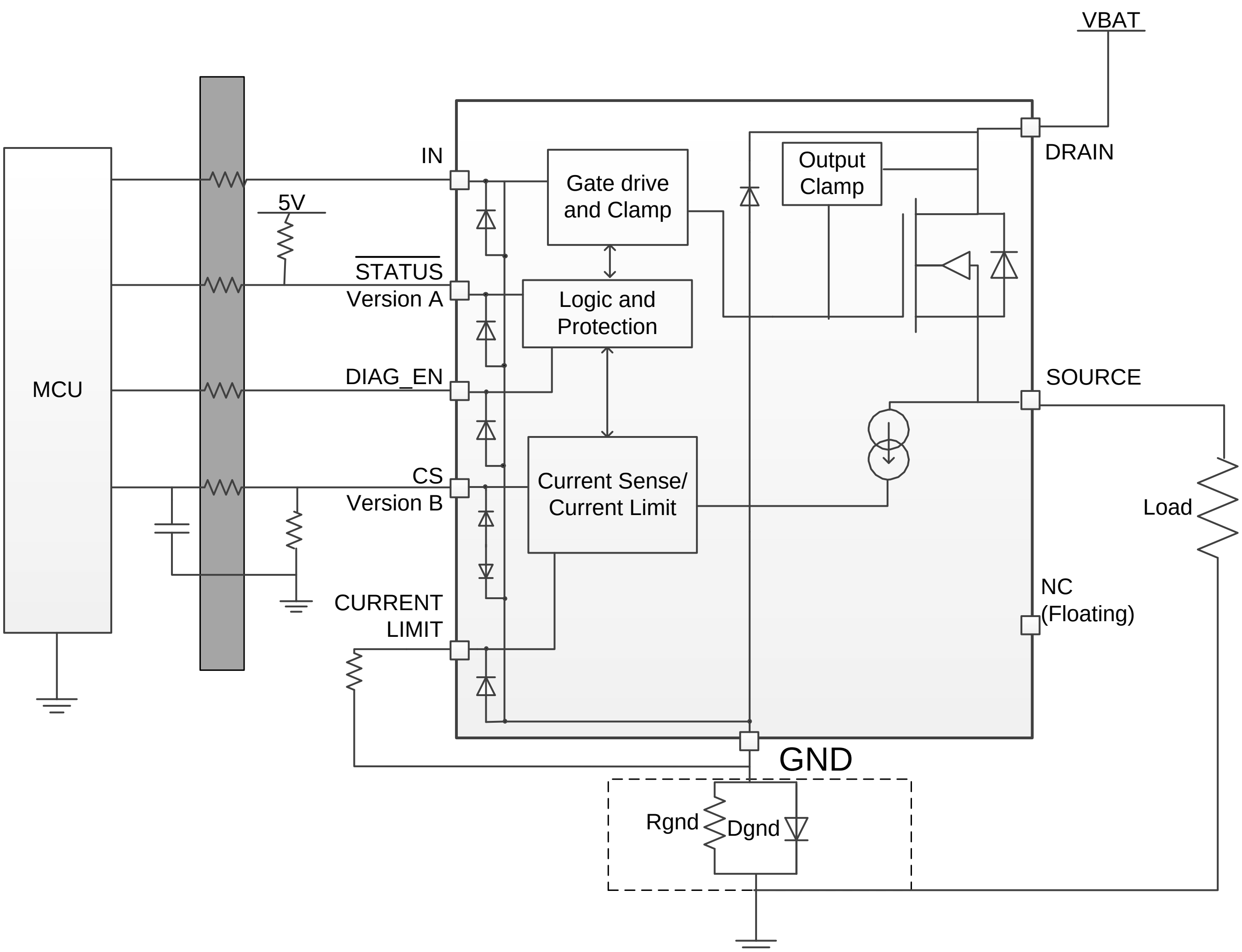


Figure 43. MCU IO Protections

8.3.5 Diagnostic Enable Function

The diagnostic enable pin, DIAG_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, during the output off period, diagnostic disable function lowers the current consumption for the standby condition. The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If an off-state power saving is required in the system, the standby current is <500 nA with DIAG_EN low. If the off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high.

8.4 Device Functional Modes

8.4.1 Working Mode

The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If an off-state power saving is required in the system, the standby current is less than 500 nA with DIAG_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high. Note that to enter standby mode requires IN low and $t > t_{off,deg}$. $t_{off,deg}$ is the standby mode deglitch time, which is used to avoid false triggering. Figure 44 shows a work mode state machine block diagram.

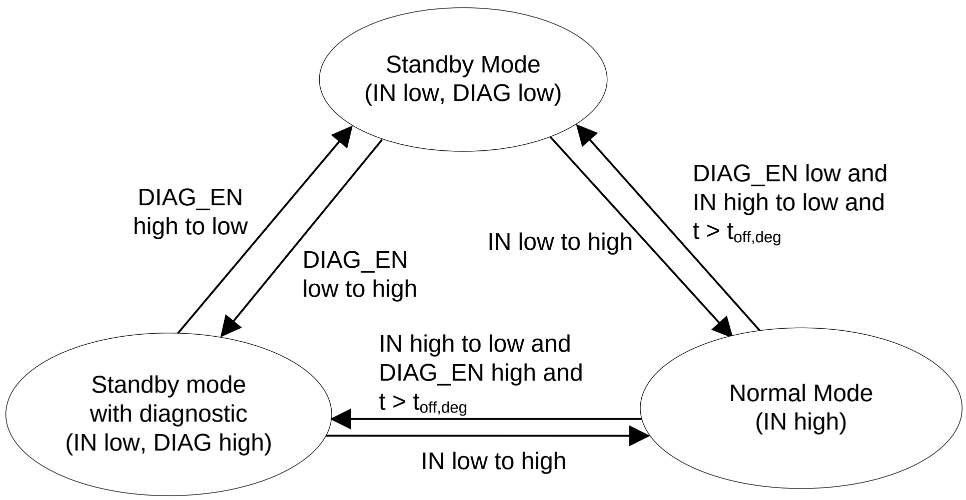


Figure 44. Work Mode State Machine

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following discussion notes how to implement the device such as distinguish the different fault modes and transient pulse immunity test.

In some applications, open load, short to battery, and short to GND are required to distinguish from each other. This requires two steps.

9.2 Typical Application

Figure 45 shows an example of how to design the external circuitry parameters.

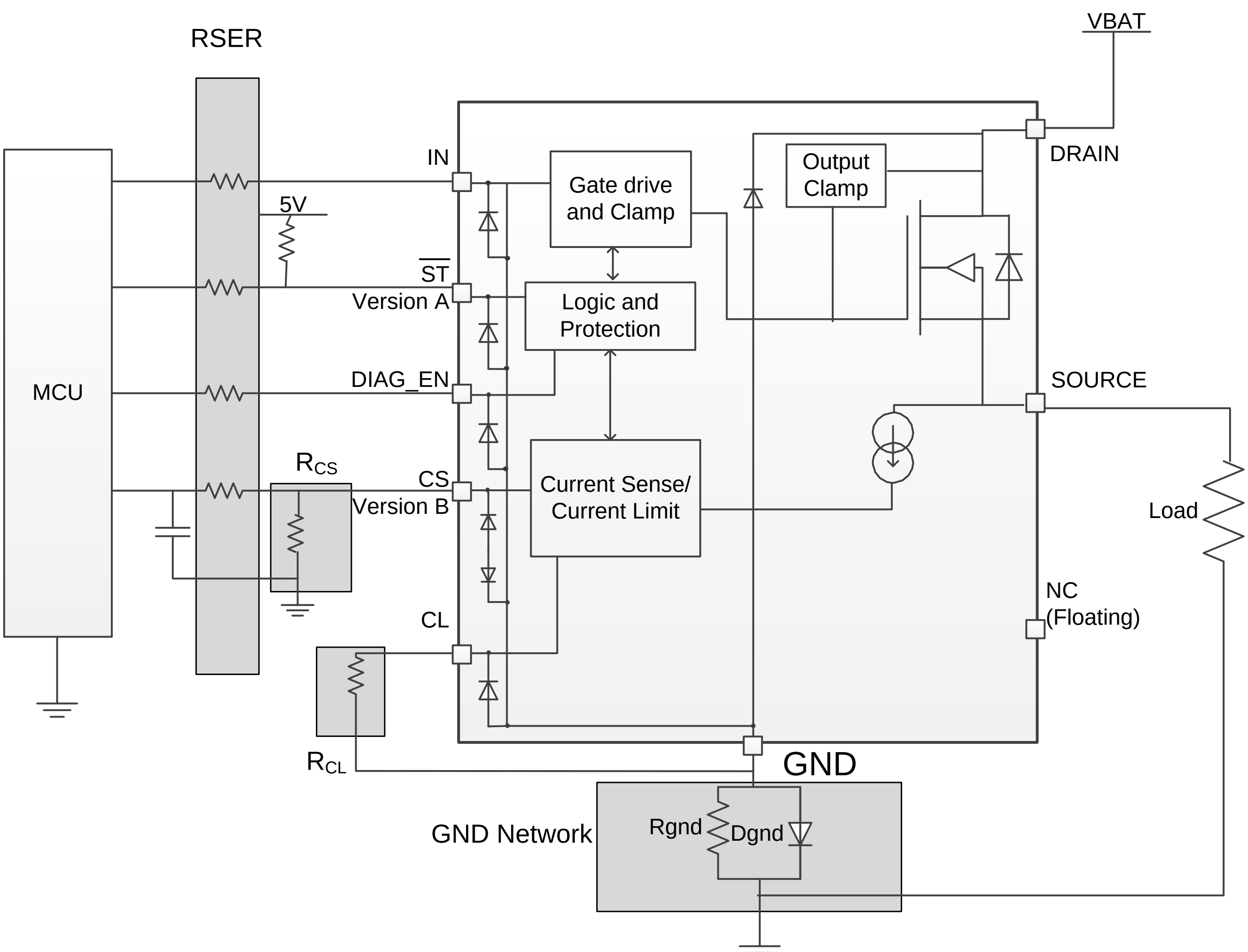


Figure 45. Typical Application Circuitry

Typical Application (continued)

9.2.1 Design Requirements

- V_S range from 9 to 16 V
- Nominal current of 2 A
- Current sense for fault monitoring
- Expected current limit value of 5 A
- Full diagnostic with 5-V MCU
- Reverse protection with GND network

9.2.2 Detailed Design Procedure

The R_{CS}, V_{CS} linear region is from 0 to 4 V. To keep the 2-A nominal current in the 0- to 3-V range, calculate the R_{CS} as in Equation 11. To achieve better current sense accuracy, 1% accuracy or an even higher resistor is preferred.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K}{I_{OUT}} = \frac{3 \times 500}{2} = 750\ \Omega \tag{11}$$

R_{CL}, $V_{CL,th}$ is the current limit internal threshold 1.233 V. To set the programmable current limit value at 5 A, calculate the R_{CL} as in Equation 12.

$$R_{CL} = \frac{V_{cl,th} \times K_{CL}}{I_{OUT}} = \frac{1.233 \times 2000}{5} = 493.2\ \Omega \tag{12}$$

TI recommends R_{SER} = 10 kΩ for 5-V MCU.

TI recommends R_{GND} = 1 kΩ, 200 V / 0.2 A D_{GND} for the GND network.

9.2.2.1 Distinguishing of Different Fault Modes

Some applications require that open load, short to battery, and short to GND can be distinguished from each other. This requires two steps:

1. In the on state, for current sense version device (version B), on-state open load/ short to battery are recognized as an extremely-low voltage level in current sense pin, while short to GND is reported as a pulled-up voltage $V_{CS,h}$. Therefore, the user can find a short to GND (see Figure 46).
2. If reported as an on-state open load or short to battery fault in the first step, turn off the input signal. In the off state, with an external pulldown resistor, open load and short to battery can be easily distinguished. When the output pulls down, the short to battery is still reported as an off-state fault condition, while the open load is ignored.

Typical Application (continued)

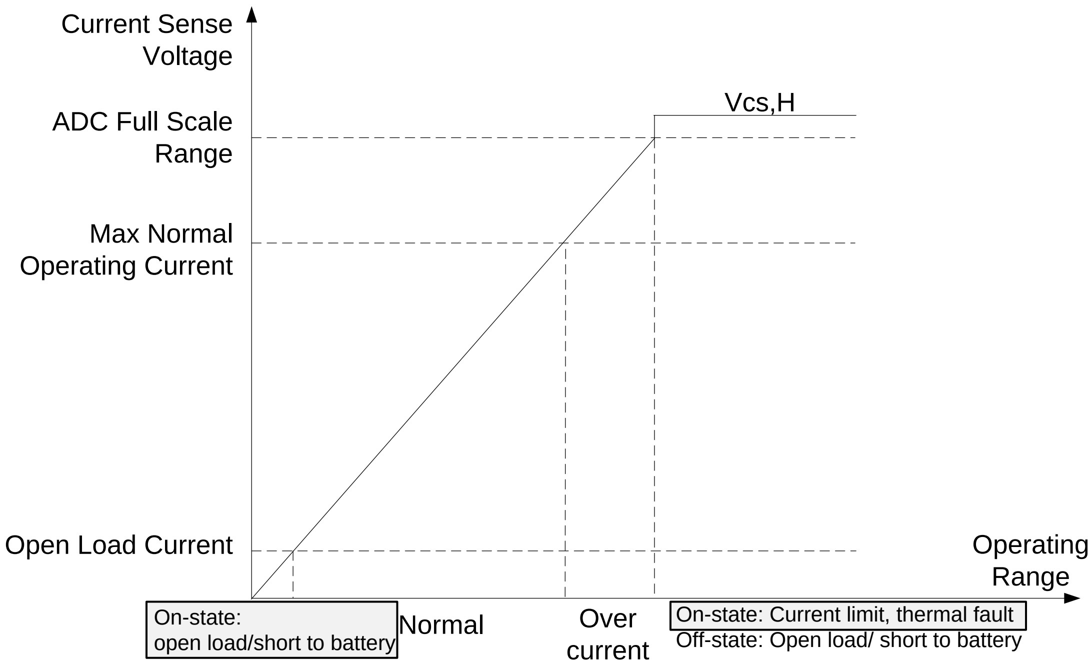


Figure 46. Step 1: Distinguish Short to GND in On-State

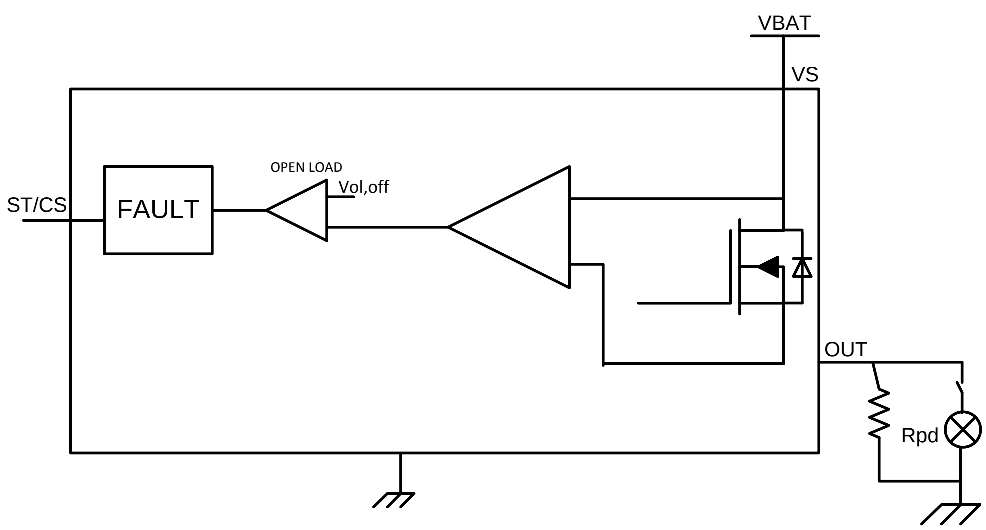


Figure 47. Step 2: Distinguish Short to Battery in Off-State

9.2.2.2 AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short to GND certification.

Three test modes are defined in the AEC Q100-012. See Table 3 for cold repetitive SCT – long pulse, cold repetitive SCT – short pulse, and hot repetitive SCT.

Typical Application (continued)

Table 3. Tests

Test Items	Test Condition	Test Cycles
Cold repetitive short circuit test – short pulse	–40°C, 10-ms pulse, cool down	1M
Cold repetitive short circuit test – long pulse	–40°C, 300-ms pulse, cool down	1M
Hot repetitive short circuit test	25°C, keeping short	1M

Different grade levels are specified according to the pass cycles. The TPS1H100 gets the certification of Grade A level, 1 million times short to GND, which is the highest test standard in the market.

Table 4. Grade Levels

Grade	Number of Cycles	Lots/Samples Per Lot	Number of Fails
A	>1000000	3/10	0
B	>300000 to 1000000	3/10	0
C	>100000 to 300000	3/10	0
D	>30000 to 100000	3/10	0
E	>10000 to 30000	3/10	0
F	>3000 to 10000	3/10	0
G	>1000 to 3000	3/10	0
H	300 to 1000	3/10	0
O	<300	3/10	0

9.2.2.3 EMC Transient Disturbances Test

Due to the severe electrical condition in the automotive, the immunity capacity against electrical transient disturbances is required, especially for a high-side power switch, which is connected to the battery directly. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010. TPS1H100-Q1 part is tested and certificated by a third-party organization.

Table 5. ISO 7637-2:2011(E) in 12-V System(1)(2)(3)(4)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst Cycle/Pulse Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN	MAX		
1	III	–112	2 ms	500 pulses	0.5 s	e s	10	Status II
2a	III	55	50 µs	500 pulses	0.2 s	5 s	2	Status II
2b	IV	10	0.2 to 2 s	10 pulses	0.5 s	5 s	0 to 0.05	Status II
3a	IV	–220	0.1 µs	1h	90 ms	100 ms	50	Status II
3b	IV	150	0.1 µs	1h	90 ms	100 ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, it is tested without any filter capacitors in V_S and V_{OUT}.
(3) GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

Table 6. ISO 16750-2:2010(E) Load Dump Test B in 12-V System(1)(2)(3)(4)(5)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst Cycle/Pulse Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN (s)	MAX (s)		
Test B		45	40 to 400 ms	5 pulses	60	e	0.5 to 4	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, it is tested without any filter capacitors in V_S and V_{OUT}.
(3) GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.
(5) Select 45-V external suppressor

9.2.3 Application Curves

Figure 48 shows a test example of initial short circuit inrush current limit. Test condition: V_S = 13.5 V, input is from low to high, load is short to GND or with 470-µF capacitive load, external current limit is 2 A. CH1 is the output current. CH3 is the input step.

Figure 49 shows a test example of a hard short-circuit inrush current limit. Test condition: V_S= 13.5 V, input is high, load is 5 µH + 100 mΩ, external current limit is 1 A. A short to GND suddenly happens.

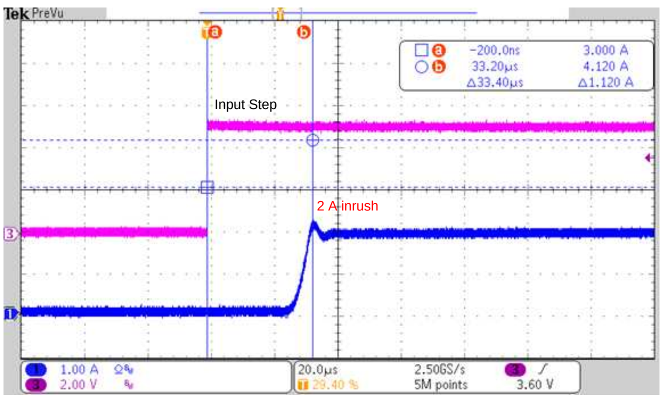


Figure 48. Initial Short to GND Waveform

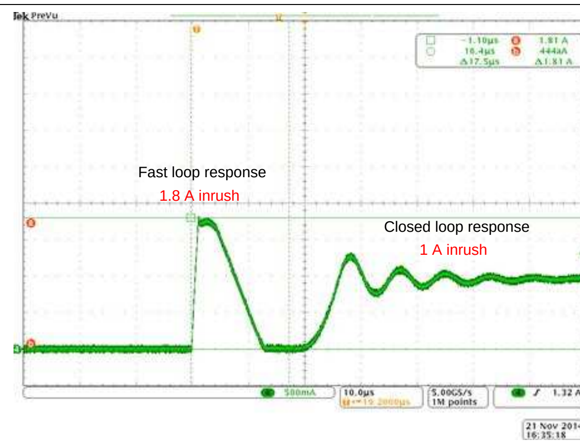


Figure 49. Hard Short to GND Waveform

10 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. Detailed supply voltage should be within the range specified in the *Recommended Operating Conditions*.

11 Layout

11.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

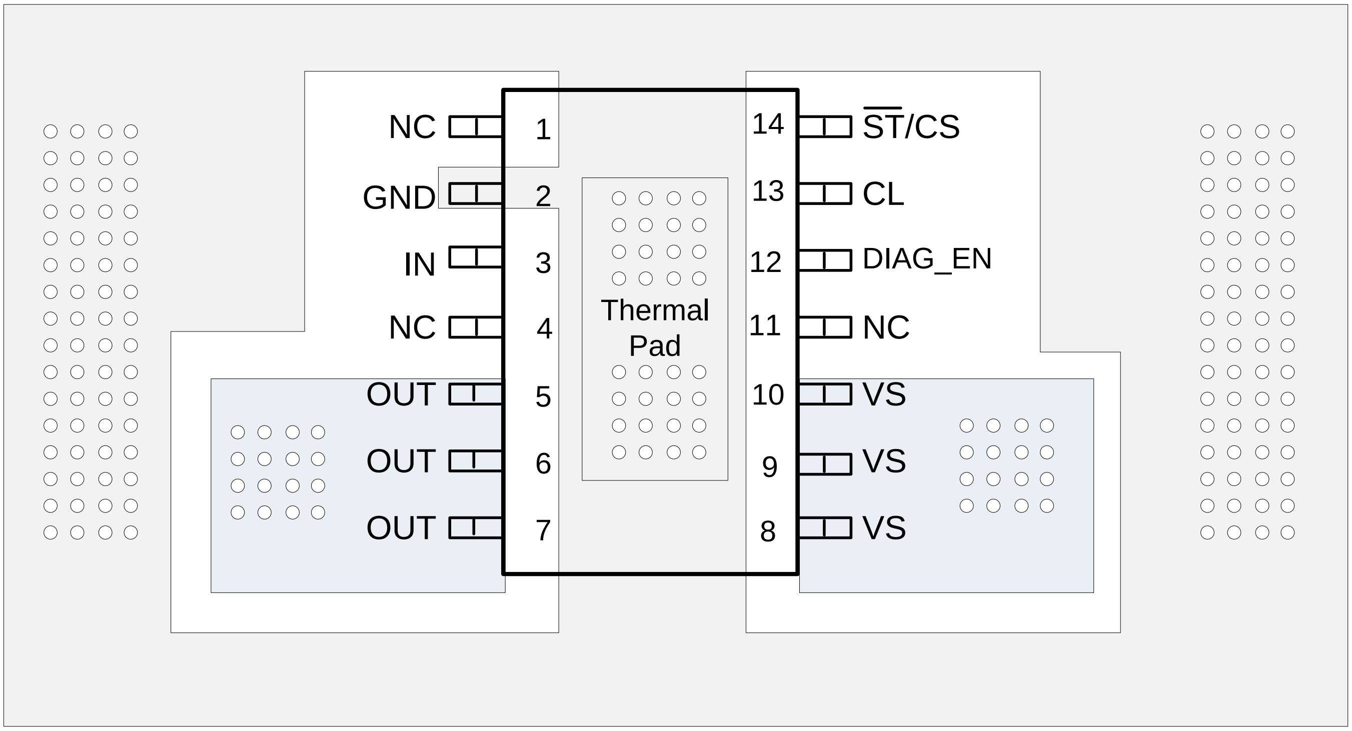


Figure 50. Without a GND Network Layout

Layout Example (continued)

11.2.2 With a GND Network

With a GND network, tie the thermal pad as one trace to the board GND copper after the GND network.

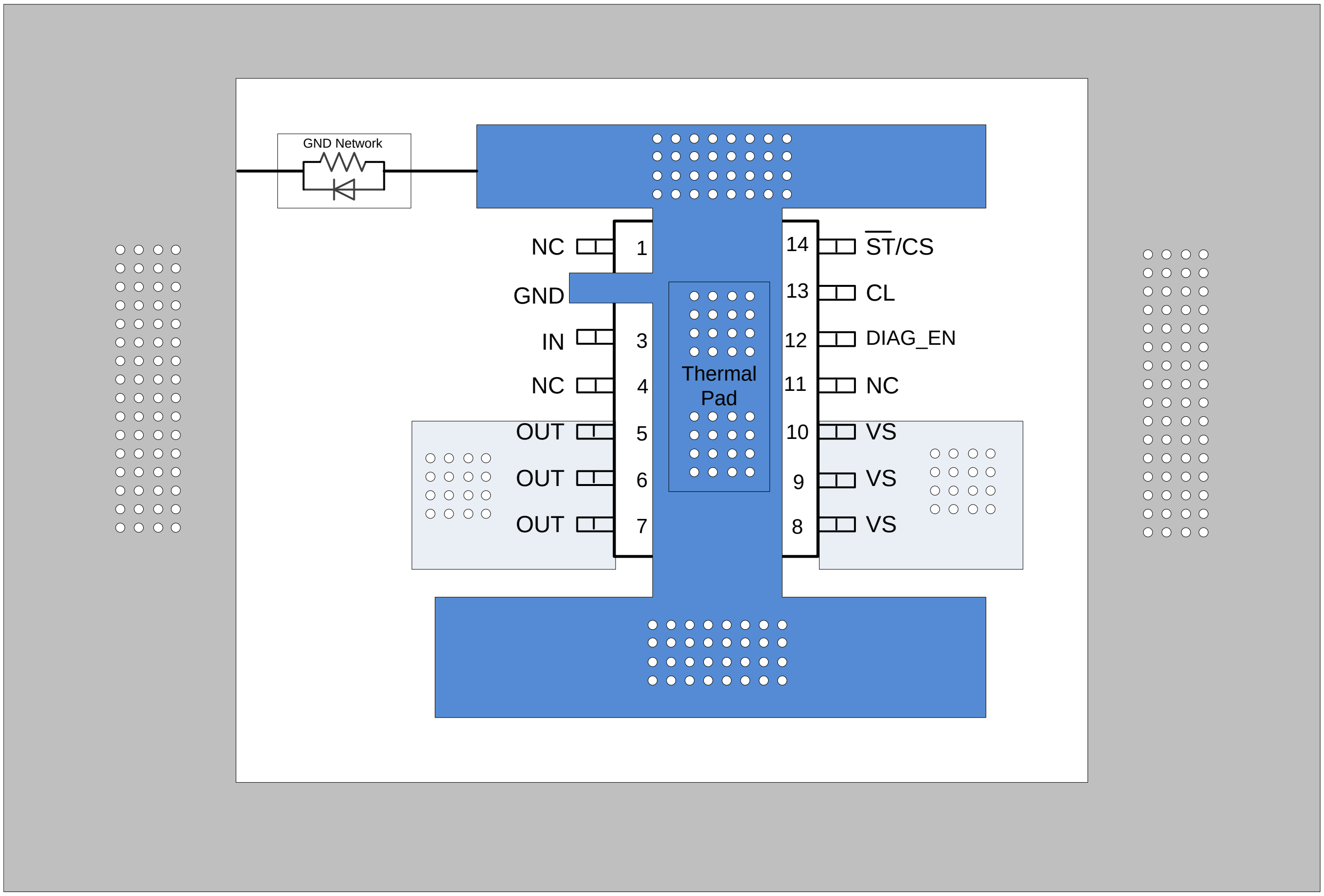


Figure 51. With a GND Network Layout

11.3 Thermal Considerations

This device possesses thermal shutdown (TSD) circuitry as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to Equation 13.

$$P_T = I_{OUT}^2 \times R_{DSON} + V_S \times I_{nom}$$

where

- P_T = Total power dissipation of the device (13)

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (14)$$

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1H100AQPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100AQ	Samples
TPS1H100BQPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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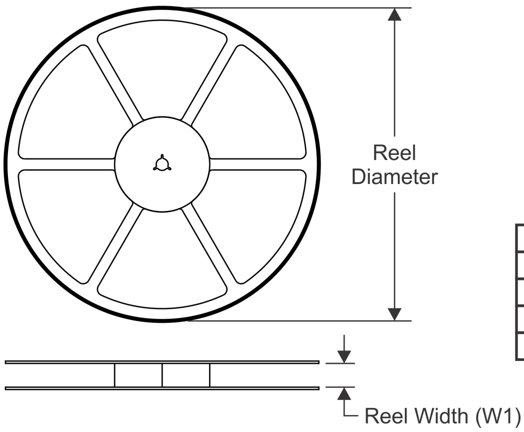
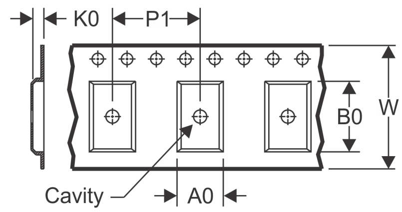
TAPE AND REEL INFORMATION

REEL DIMENSIONS

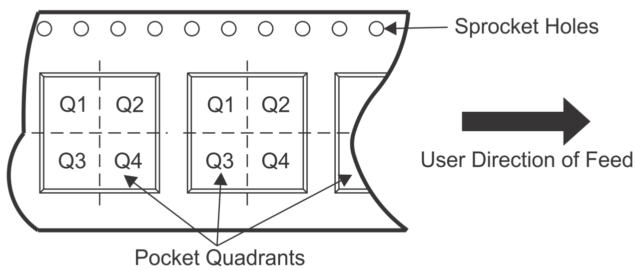


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

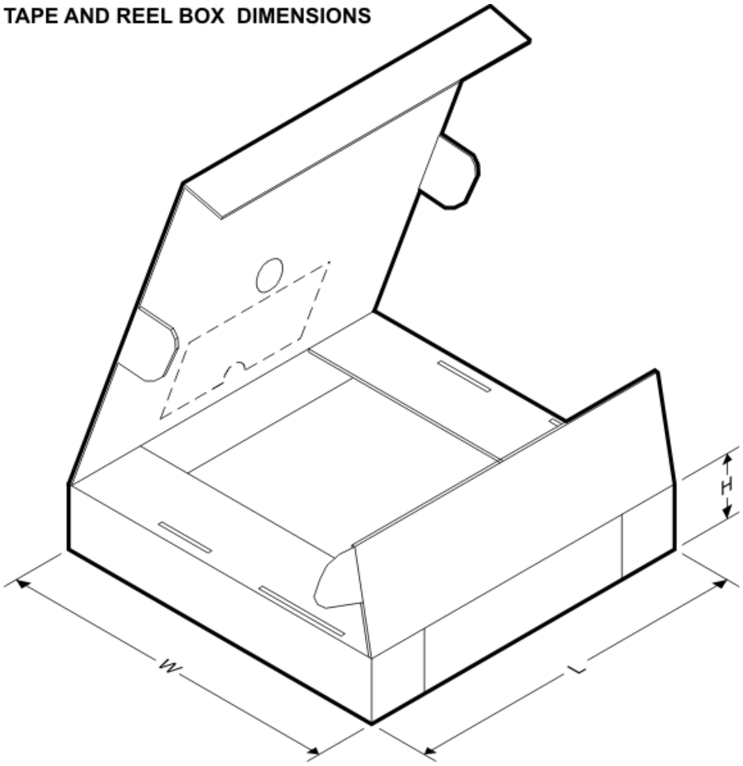
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1H100AQPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1H100BQPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

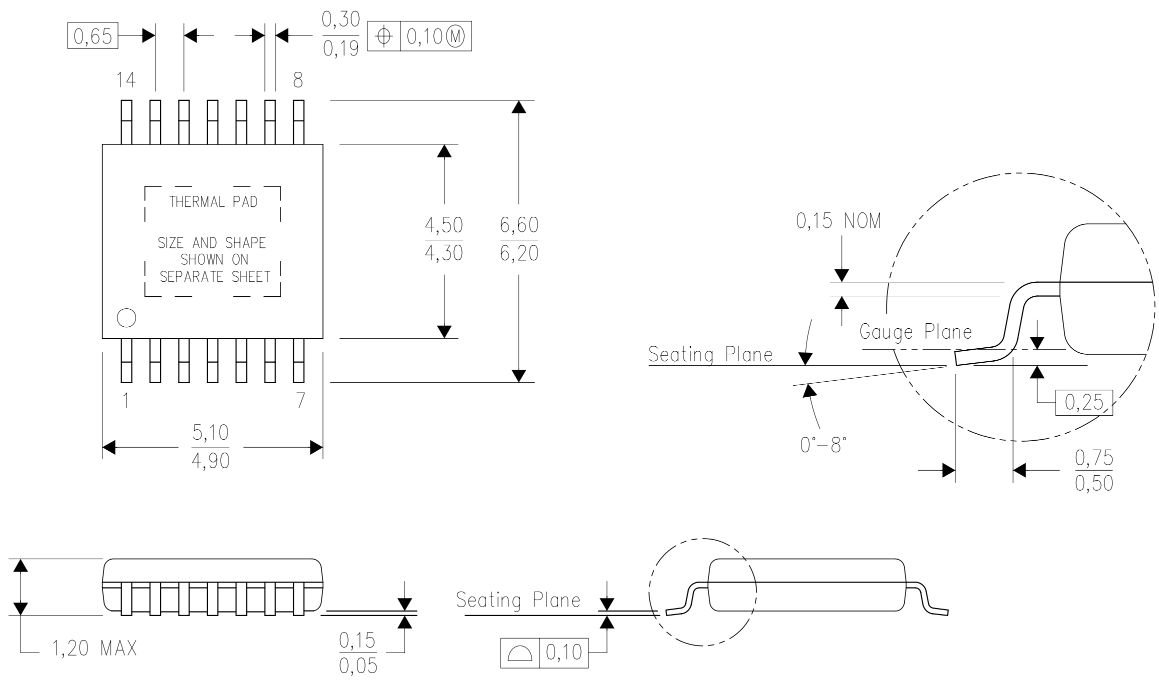
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1H100AQPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	38.0
TPS1H100BQPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	38.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



4073225–2/I 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

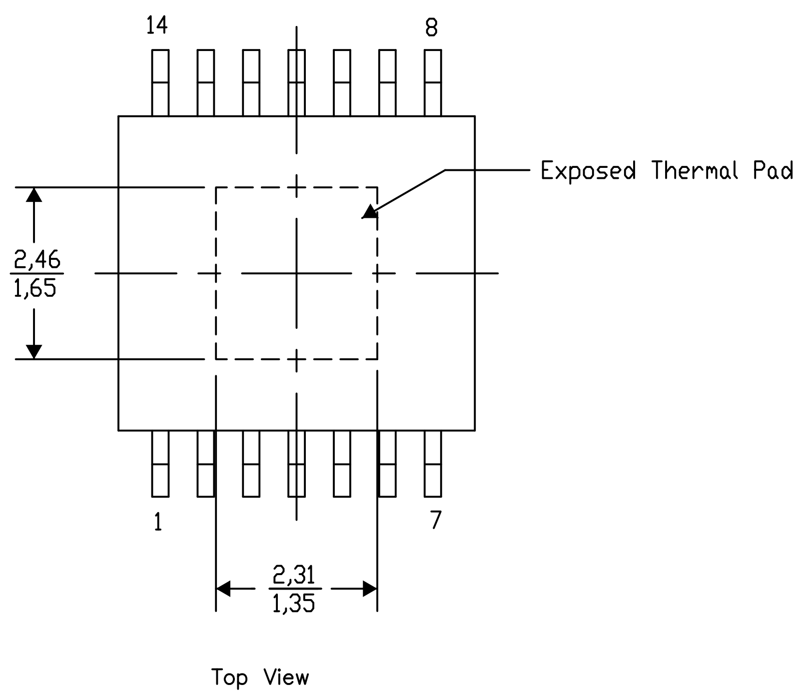
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



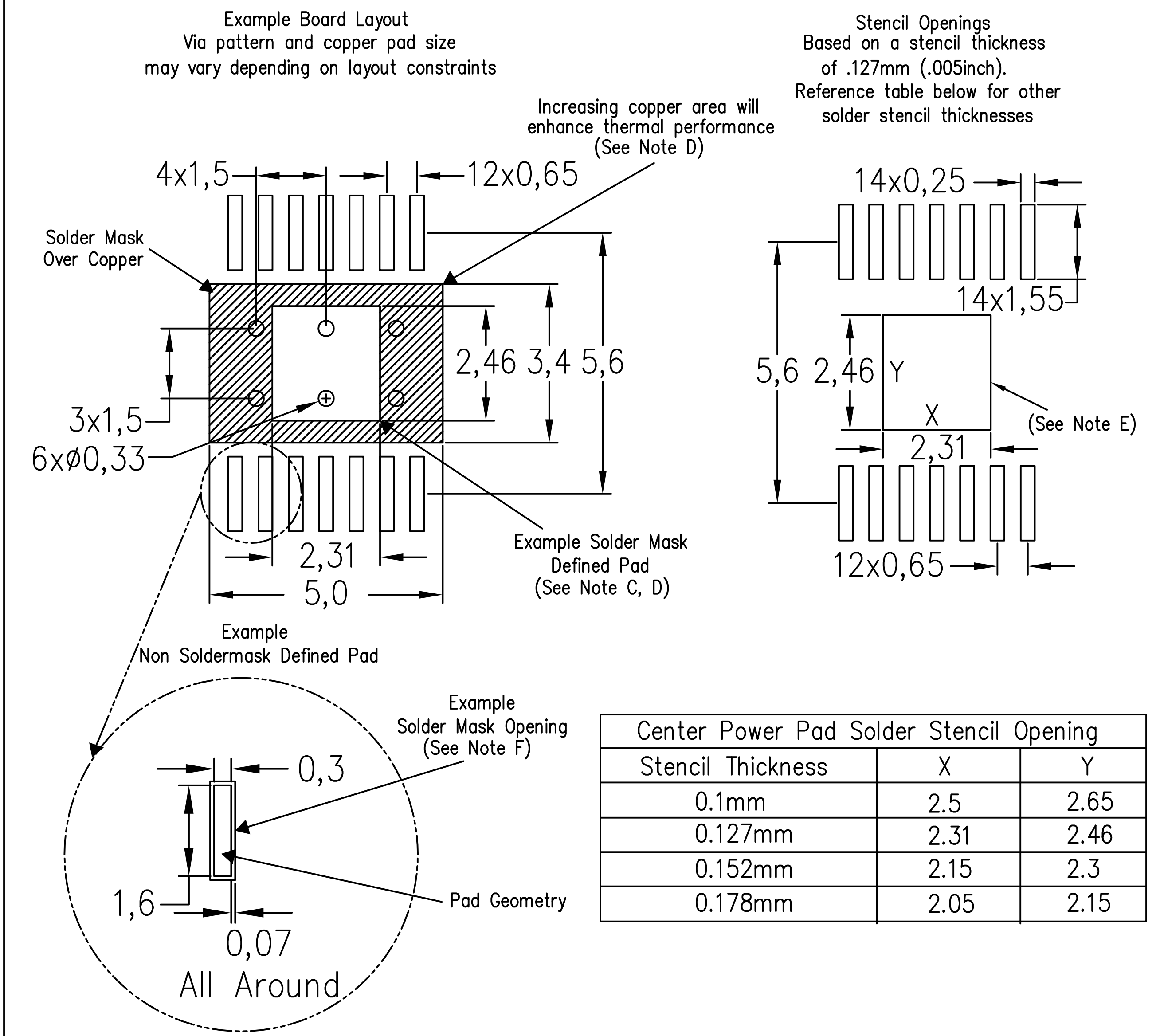
Exposed Thermal Pad Dimensions

4206332-2/A0 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609-2/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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