TPS53317A 用于 DDR 存储器终端的 6A 输出、D-CAP+ 模式、同步降压集成 FET 转换器

1 特性

- 采用 TI 专有的集成金属氧化物半导体场效应晶体管 (MOSFET) 和封装技术
- 支持 DDR 内存终止，具有高达 6A 的持续输出源电流或者吸收电流
- 外部跟踪
- 最少的外部组件数
- 0.9V 至 6V 转换电压
- D-CAP+™ 模式架构
- 支持所有多层片式陶瓷输出电容器和 SP/POSCAP
- 可选跳跃 (SKIP) 模式或者强制 CCM
- 轻量级负载与重负载下的优化效率
- 可选 600kHz 或者1MHz 开关频率
- 可选过流限制 (OCL)
- 过压、过热和断续欠压保护
- 可调输出电压范围为 0.45V 至 2V
- 3.5mm × 4mm 20 引脚超薄四方扁平无引线 (VQFN) 封装

2 应用

- 用于 DDR、DDR2、DDR3 和 DDR4 的存储器终端稳压器
- VTT 终止
- 用于 0.9V 至 6V 输入电源轨的低电压应用

3 说明

TPS53317A 器件是一款设计为主要用于 DDR 终端的集成场效应晶体管 (FET) 同步降压稳压器。 它能够提供一个值为 ½ V_{DDQ}的经稳压输出，此输出具有吸收电流和源电流功能。 TPS53317A 器件采用 D-CAP+ 运行模式，简单易用，所需外部组件数较少并可提供快速瞬态响应。 该器件还可用于其他电流要求高达 6A 的负载点 (POL) 稳压应用。此外，该器件支持具有严格电压调节功能的 6A 完整灌电流输出。

该器件具有两种开关频率设定值（600kHz 和 1MHz），可提供集成压降支持、外部跟踪功能、预偏置启动、输出软放电、集成自举开关、电源正常功能、V5IN 引脚欠压锁定 (UVLO) 保护功能，支持采用陶瓷和 SP/POSCAP 电容。 该器件支持的输入电压最高可达 6V，而输出电压在 0.45V 至 2.0V 范围内可调。

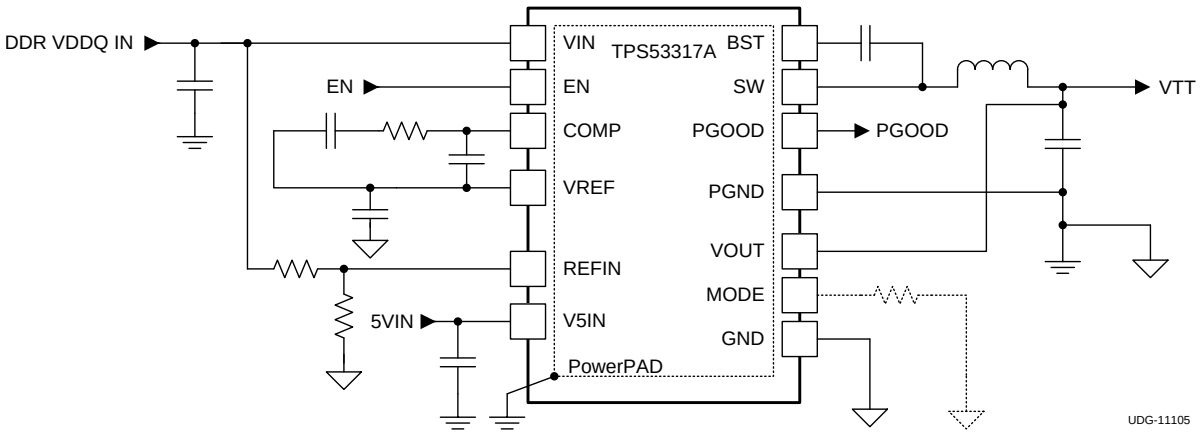
TPS53317A 器件采用 3.5mm × 4mm 20 引脚超薄四方扁平无引线 (VQFN) 封装（绿色环保，符合 RoHS 标准并且无铅），其中应用了 TI 专有的集成 MOSFET 和封装技术，其额定运行温度范围为 –40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS53317A	VQFN (20)	3.50mm × 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用



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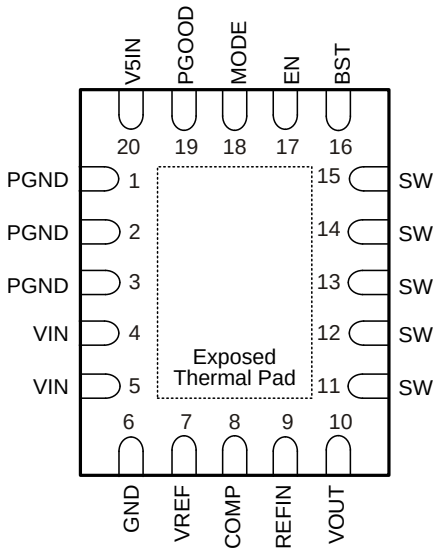
4 修订历史记录

Changes from Original (November 2015) to Revision A	**Page**
• 文档状态已由*产品预览*更改为*量产数据*。	1

5 Pin Configuration and Functions

RGB Package
20-Pin VFQN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BST	16	I	Power supply for internal high-side gate driver. Connect a 0.1-µF bootstrap capacitor between this pin and the SW pin. Include a series boot resistor when the voltage spike on switching node is above 7 V.
COMP	8	O	Connect an R-C-C network between this pin and VREF for loop compensation.
EN	17	I	Enable pin (3.3-V logic compatible).
GND	6	–	Analog ground.
MODE	18	I	Allows selection of different operation modes. (See 表 1)
PGND	1	G	Power ground.
	2		
	3		
PGOOD	19	O	Open drain power good output. Connect pullup resistor.
REFIN	9	I	External tracking reference input. Apply voltage between 0.45 V to 2.0 V. For non-tracking mode, connect REFIN to VREF via resistor divider.
SW	11	I/O	Switching node output.
	12		
	13		
	14		
	15		
V5IN	20	I	5-V power supply for analog circuits and gate drive.
VIN	4	I	Power supply input pin.
	5		
VOUT	10	I	Output voltage monitor input pin.
VREF	7	O	2.0-V reference output. Connect a ceramic capacitor with a value of 0.22-µF or greater between this pin and GND.

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	BST (with respect to SW), V5IN, VIN	–0.3	7	V
	BST	–0.3	14	
	EN	–0.3	7	
	MODE, REFIN	–0.3	3.6	
	VOUT	–1	3.6	
Output voltage range	SW	–2	7	V
	SW (transient 20 ns and E = 5 μJ)	–3		
	COMP, VREF	–0.3	3.6	
	PGOOD	–0.3	7	
	PGND	–0.3	0.3	
Operating junction temperature, T_J		–40	150	˚C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	˚C
Storage temperature, T_{stg}		–55	150	˚C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	BST (with respect to SW), EN, VIN	–0.1		6.5	V
	V5IN	4.5		6.5	
	BST	–0.1		13.5	
	SW	–1.0		6.5	
	VOUT, MODE, REFIN	–0.1		3.5	
Output voltage range	COMP	–0.1		3.5	V
	VREF		2		
	PGOOD	–0.1		6.5	
	PGND	–0.1		0.1	
Operating temperature range, T_A		-40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS53317A RGB (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{V5IN} = 5.0 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS AND 5-V UVLO						
I_{VINSD}	VIN shutdown current	EN = 'LO'		0.02	5	µA
V_{V5IN}	V5IN supply voltage	V5IN voltage range	4.5	5.0	6.5	V
I_{V5IN}	V5IN supply current	EN ='HI', V5IN supply current, f_{SW} = 600 kHz		1.1	2	mA
I_{V5INSD}	V5IN shutdown current	EN = 'LO', V5IN shutdown current		0.2	7.0	µA
V_{V5UVLO}	V5IN UVLO	Ramp up; EN = 'HI'	4.20	4.37	4.50	V
$V_{V5UVHYS}$	V5IN UVLO hysteresis	Falling hysteresis		440		mV
$V_{VREFUVLO}$	REF UVLO(1)	Rising edge of VREF, EN = 'HI'		1.8		V
$V_{VREFUVHYS}$	REF UVLO hysteresis(1)			100		mV
$V_{POR5VFILT}$	Reset	OVP latch is reset by V5IN falling below the reset threshold	1.5	2.3	3.1	V
VOLTAGE FEEDBACK LOOP: VREF, VOUT, AND VOLTAGE GM AMPLIFIER						
V_{OUTTOL}	Output voltage accuracy	V_{REFIN} = 1 V, No droop	–1%	0%	1%	
		V_{REFIN} = 0.6 V, No droop	–1%	0%	1%	
V_{VREF}	VREF	I_{VREF} = 0 µA	1.98	2.00	2.02	V
		I_{VREF} = 50 µA	1.975	2.000	2.025	
I_{REFSNK}	VREF sink current	V_{VREF} = 2.05 V		2.5		mA
g_M	Transconductance			1.00		mS
V_{CM}	Common mode input voltage range(1)		0		2	V
V_{DM}	Differential mode input voltage		0		80	mV
$I_{COMPSNK}$	COMP pin maximum sinking current	V_{COMP} = 2 V, (V_{REFIN} – V_{OUT}) = 80 mV		80		µA
$I_{COMPSRC}$	COMP pin maximum sourcing current	V_{COMP} = 2 V		-80		µA
V_{OFFSET}	Input offset voltage	T_A = 25°C		0		mV
R_{DSCH}	Output voltage discharge resistance			42		Ω
f_{-3dbVL}	–3dB Frequency(1)		4.5	6.0	7.5	MHz
CURRENT SENSE: CURRENT SENSE AMPLIFIER, OVERCURRENT AND ZERO CROSSING						
A_{CSINT}	Internal current sense gain	Gain from the current of the low-side FET to PWM comparator when PWM = "OFF"	43	53	57	mV/A
I_{OCL}	Positive overcurrent limit (valley)			7.6		A
$I_{OCL(neg)}$	Negative overcurrent limit (valley)			–9.3		A
V_{ZXOFF}	Zero crossing comp internal offset			0		mV

(1) Ensured by design, not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{V5IN} = 5.0 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: OVP, UVP, PGOOD, and THERMAL SHUTDOWN						
V_{PGDLL}	PGOOD deassert to lower (PGOOD → Low)	Measured at the VOUT pin wrt/ V_{REFIN}		84%		
$V_{PGHYSHL}$	PGOOD high hysteresis			8%		
V_{PGDLH}	PGOOD de-assert to higher (PGOOD → Low)	Measured at the VOUT pin wrt/ V_{REFIN}		116%		
$V_{PGHYSHH}$	PGOOD high hysteresis			-8%		
$V_{INMINPG}$	Minimum VIN voltage for valid PGOOD	Measured at the VIN pin with a 2-mA sink current on PGOOD pin. V5IN is grounded here.(2)	0.9	1.3	1.5	V
V_{OVP}	OVP threshold	Measured at the VOUT pin wrt/ V_{REFIN}, V_{REFIN} = 1 V	117%	120%	123%	
V_{UVP}	UVP threshold	Measured at the VOUT pin wrt/ V_{REFIN}, device latches OFF, begins soft-stop, V_{REFIN} = 1 V	65%	68%	71%	
TH_{SD}	Thermal shutdown(1)	Latch off controller, attempt soft-stop.		145		°C
$TH_{SD(hys)}$	Thermal Shutdown hysteresis(1)	Controller re-starts after temperature has dropped		10		°C
DRIVERS: BOOT STRAP SWITCH						
$R_{DSONBST}$	Internal BST switch on-resistance	I_{BST} = 10 mA, T_A = 25°C			10	Ω
I_{BSTLK}	Internal BST switch leakage current	V_{BST} = 14 V, V_{SW} = 7 V			1	µA
TIMERS: ON-TIME, MINIMUM OFF-TIME, SS, AND I/O TIMINGS						
$t_{ONESHOTC}$	PWM one-shot(1)	V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 1 MHz		210		ns
		V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 600 kHz		310		
$t_{MIN(off)}$	Minimum OFF time	V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 1 MHz, DRVL on, SW = PGND, V_{VOUT} < V_{REFIN}		270		ns
$t_{INT(SS)}$	Soft-start time	From V_{OUT} ramp starting to V_{OUT} =95%, default setting		1.6		ms
$t_{INT(SSDLY)}$	Internal soft-start delay time	From V_{VREF} = 2 V to V_{OUT} is ready to ramp up		260		µs
t_{PGDDLY}	PGOOD startup delay time	At external tracking, the time from VOUT is ready to ramp up		8		ms
$t_{PGDPDLYH}$	PGOOD high propagation delay time	50 mV over drive, rising edge	0.8	1	1.2	ms
$t_{PGDPDLYL}$	PGOOD low propagation delay time	50 mV over drive, falling edge		10		µs
t_{OVPDLY}	OVP delay time	Time from the VOUT pin out of +20% of REFIN to OVP fault		10		µs
$t_{UVDLYEN}$	Undervoltage fault enable delay	Time from EN_INT going high to undervoltage fault is ready		2		ms
		External tracking from VOUT ramp starts		8		
t_{UVPDLY}	UVP delay time	Time from the VOUT pin out of –32% of REFIN to UVP fault		256		µs
LOGIC PINS: I/O VOLTAGE AND CURRENT						
	PGOOD pull-down voltage	PGOOD low impedance, I_{SINK} = 4 mA, V_{V5IN} = 4.5 V			0.3	V
	PGOOD leakage current	PGOOD high impedance, forced to 5.5 V	–1	0	1	µA
	EN logic high	EN, VCCP logic	2			V
	EN logic low	EN, VCCP logic			0.5	V
	EN input current				1	µA

(2) If V5IN is higher than 1.5 V, PGOOD is valid regardless of the voltage applied at VIN. This is based on bench testing.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{V5IN} = 5.0 V, PGND = GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE threshold voltage(3)	Threshold 1	80	130	180	mV
	Threshold 2	200	250	300	
	Threshold 3	370	420	470	
	Threshold 4	550	600	650	
	Threshold 5	830	880	930	
	Threshold 6	1200	1250	1300	
	Threshold 7	1765	1800	1850	
MODE current			15		µA

(3) See 表 1 for descriptions of MODE parameters.

6.6 Typical Characteristics

Characterization data tested using the TPS53317AEVM-726 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUUBD2 for detailed configuration.

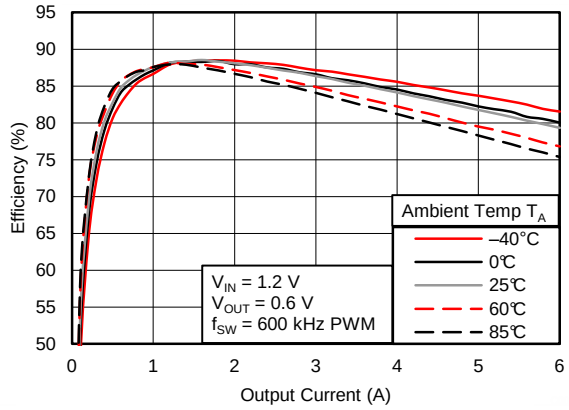


图 1. Efficiency vs. Output Current

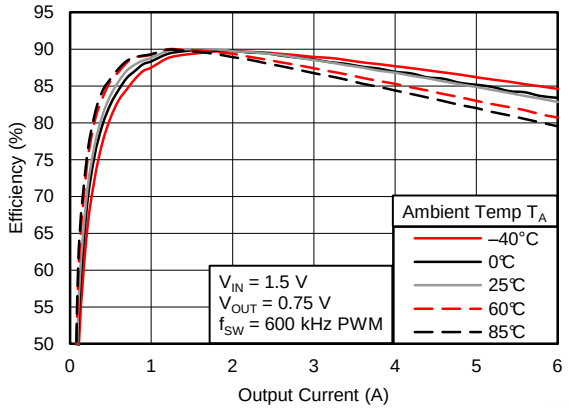


图 2. Efficiency vs. Output Current

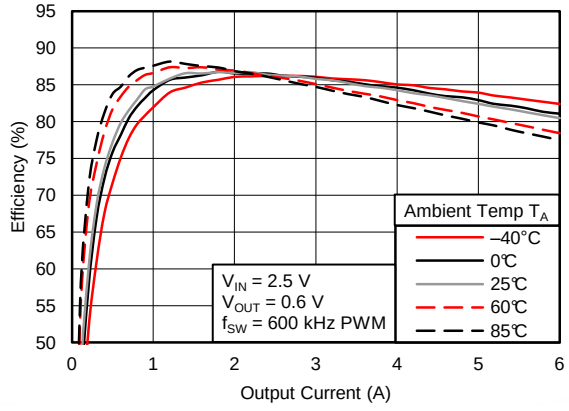


图 3. Efficiency vs. Output Current

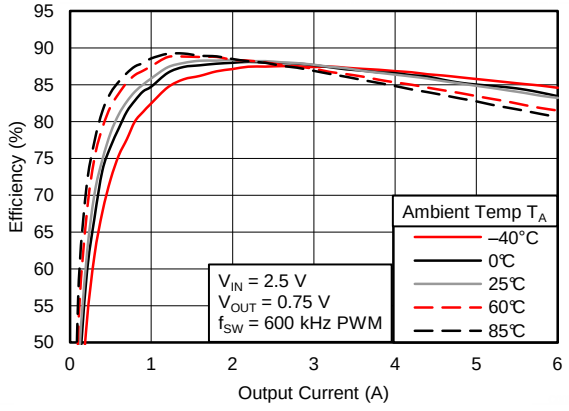


图 4. Efficiency vs. Output Current

Typical Characteristics (接下页)

Characterization data tested using the TPS53317AEVM-726 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUUBD2 for detailed configuration.

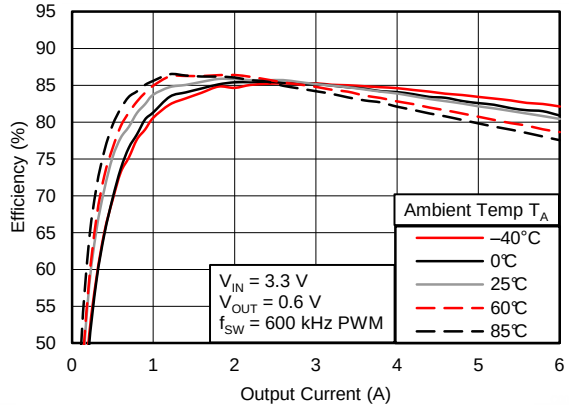


图 5. Efficiency vs. Output Current

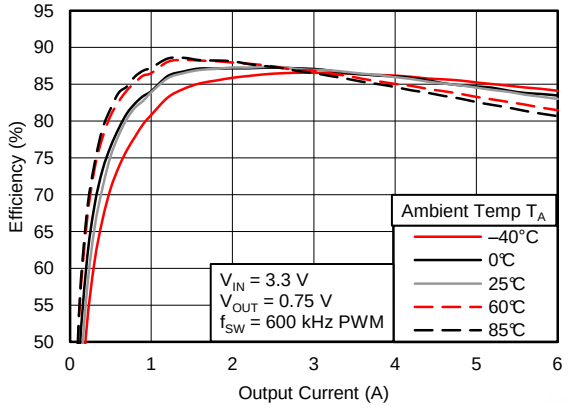


图 6. Efficiency vs. Output Current

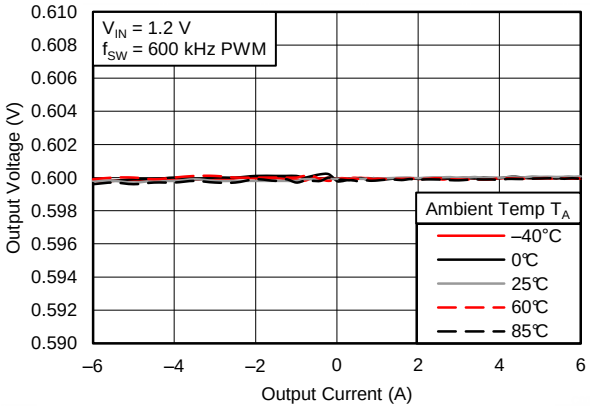


图 7. Load Regulation

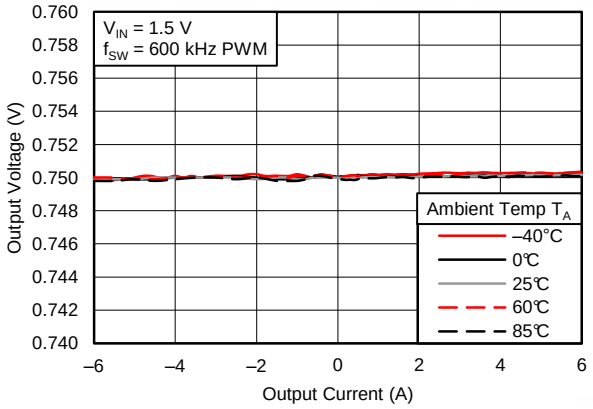


图 8. Load Regulation

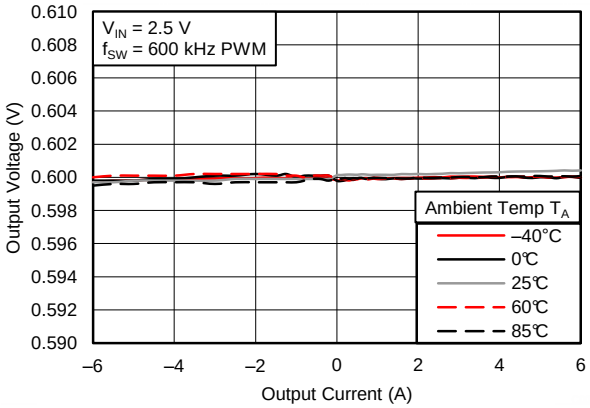


图 9. Load Regulation

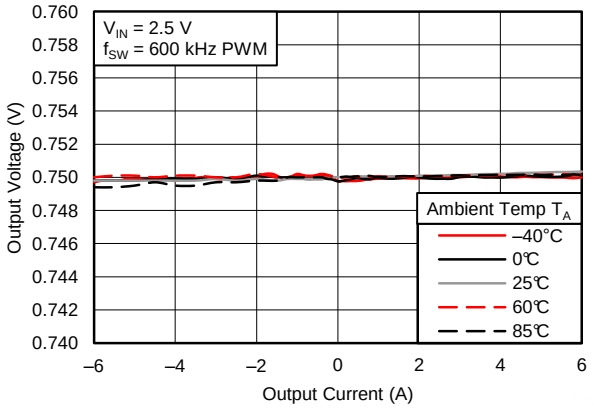


图 10. Load Regulation

Typical Characteristics (接下页)

Characterization data tested using the TPS53317AEVM-726 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUUBD2 for detailed configuration.

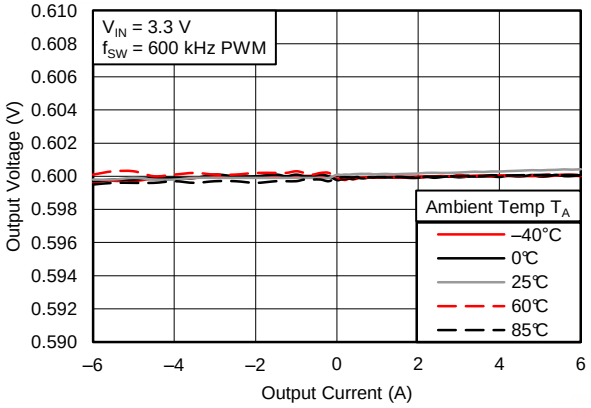


图 11. Load Regulation

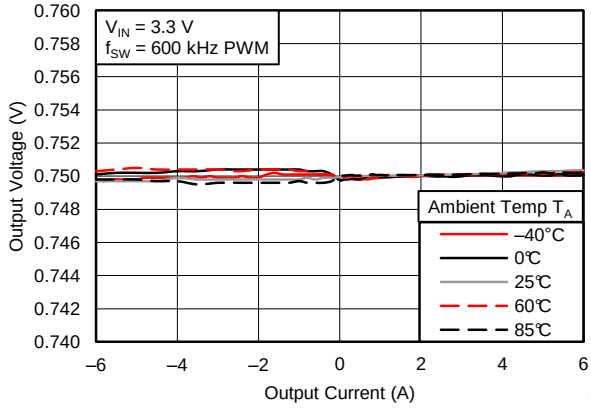


图 12. Load Regulation

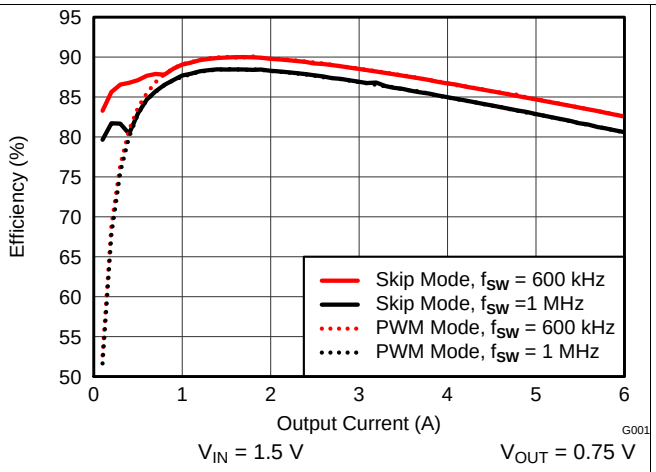


图 13. Efficiency vs Output Current

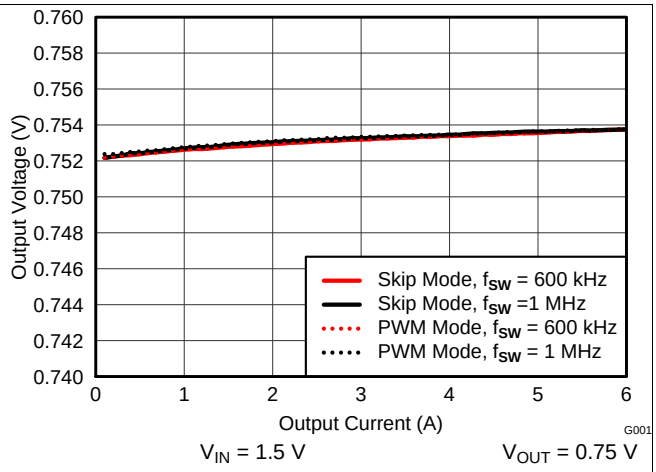


图 14. Load Regulation

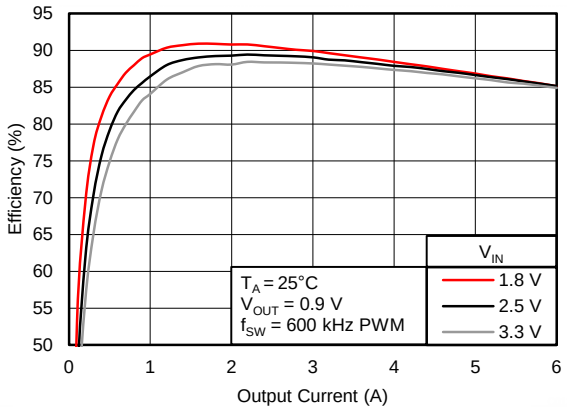


图 15. Efficiency vs. Output Current

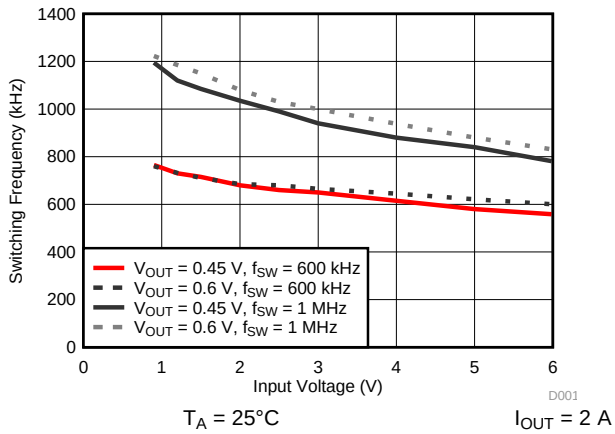


图 16. Switching Frequency vs. Input Voltage

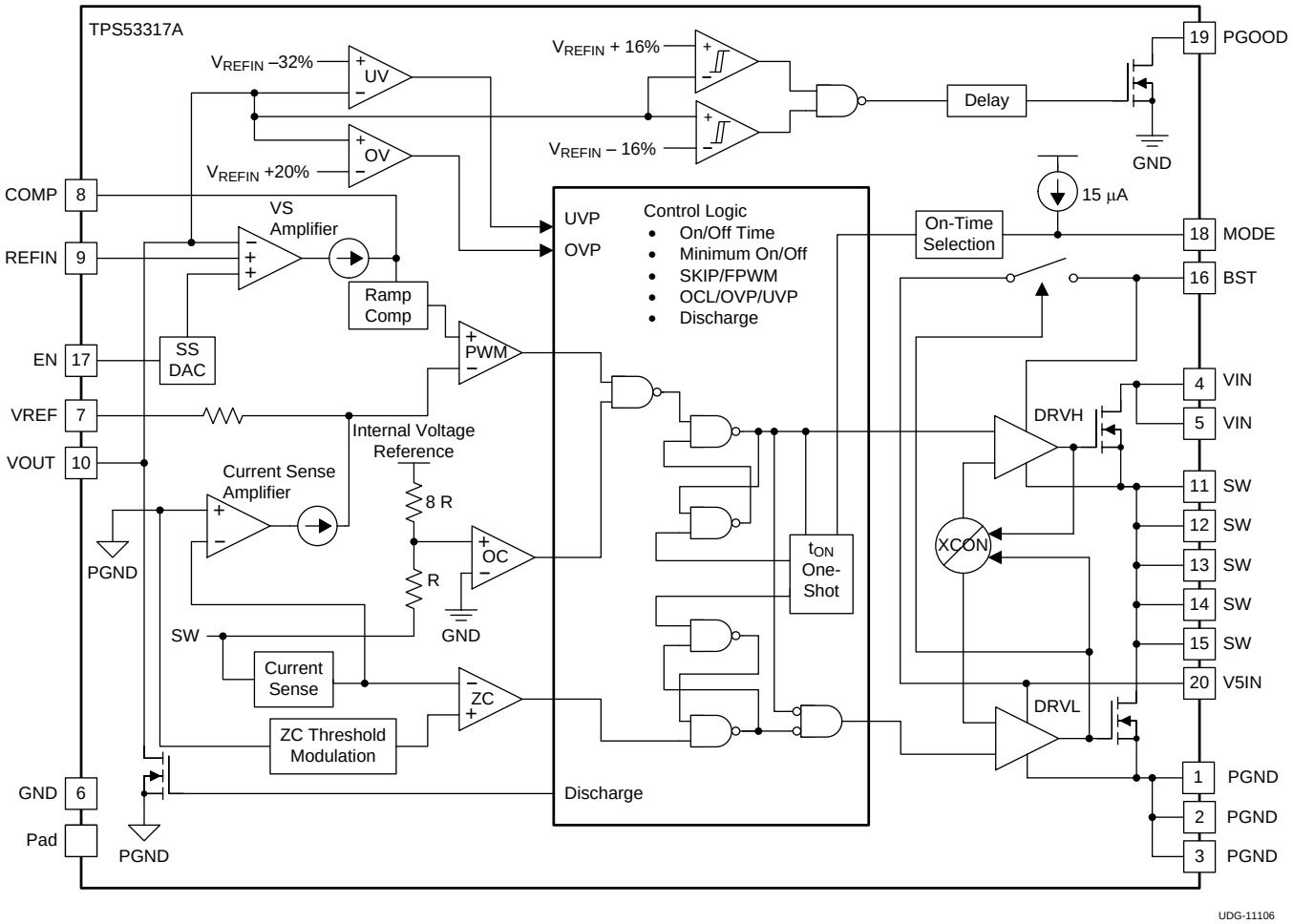
7 Detailed Description

7.1 Overview

The TPS53317A device is a D-CAP+™ mode adaptive on-time converter. Integrated high-side and low-side FETs support a maximum of 6-A DC output current. The converter automatically operates in discontinuous conduction mode (DCM) to optimize light-load efficiency. Multiple switching frequencies are provided to enable optimization of the power train for the cost, size and efficiency requirements of the design (see 表 1).

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53317A device, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the reference voltage and the feedback voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

Referring to 图 17, in steady state, continuous conduction mode, the converter operates in the following way.

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback (V_{CS}) is higher than the error amplifier output (V_{COMP}). V_{CS} falls until it hits V_{COMP}, which contains a component of the output ripple voltage. V_{CS} is not directly accessible by measuring signals on pins of TPS53317A device. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

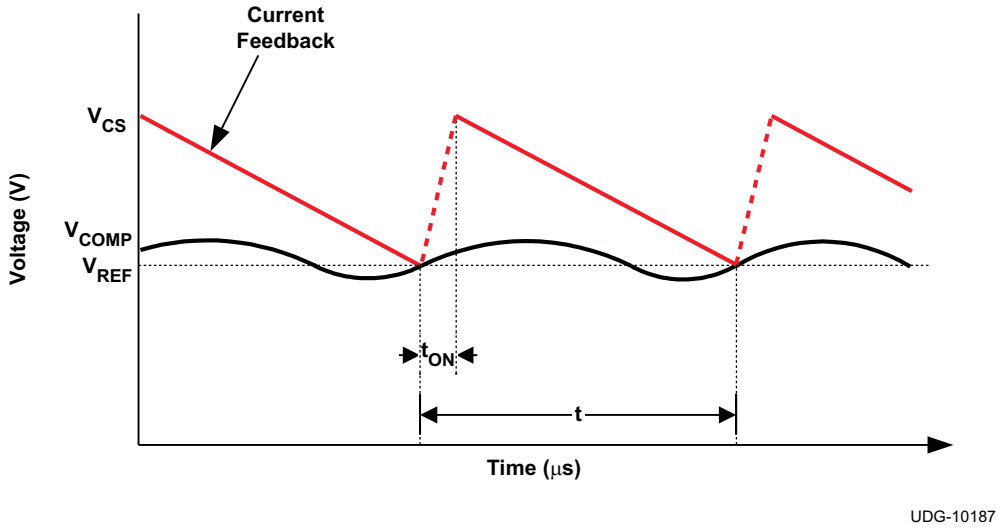


图 17. D-CAP+™ Mode Basic Waveforms

The current feedback is an amplified and filtered version of the voltage between PGND and SW during low-side FET on-time. The device also provides a single-ended voltage (V_{OUT}) feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

7.3.2 PWM Frequency and Adaptive On-Time Control

In general, the on-time (at the SW node) can be estimated by 公式 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

where

- f_{SW} is the frequency selected by the connection of the MODE pin

The on-time pulse is sent to the top FET. The inductor current and the current feedback rises to peak value. Each ON pulse is latched to prevent double pulsing. Switching frequency settings are shown in 表 1.

7.3.3 Light-Load Power Saving Features

The TPS53317A device has an automatic pulse-skipping mode to provide excellent efficiency over a wide load range. The converter senses inductor current and prevents negative flow by shutting off the low-side gate driver. This saves power by eliminating re-circulation of the inductor current. Further, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

The device also provides a special light-load power saving feature, called ripple reduction. Essentially, it reduces the on-time in SKIP mode to effectively reduce the output voltage ripple associated with using an all MLCC capacitor output power stage design.

Feature Description (接下页)

7.3.4 Power Sequences

7.3.4.1 Non-Tracking Startup

The TPS53317A device can be configured for non-tracking application. When non-tracking is configured, output voltage is regulated to the REFIN voltage which taps off the voltage dividers from the 2-V reference voltage. Either the EN pin or the V5IN pin can be used to start up the device. The device uses internal voltage servo DAC to provide a 1.6-ms soft-start time during soft-start initialization. (See 图 19.)

In a non-tracking application, the output voltage is determined by the resistive divider between the VREF pin and the REFIN pin.

$$V_{OUT} = V_{REF} \times \frac{R2}{R1 + R2} \quad (2)$$

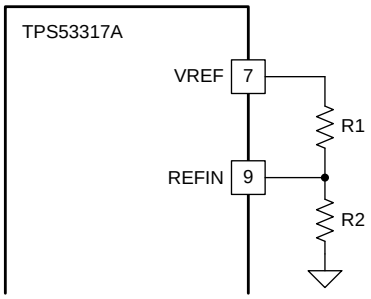


图 18. Non-Tracking Configuration

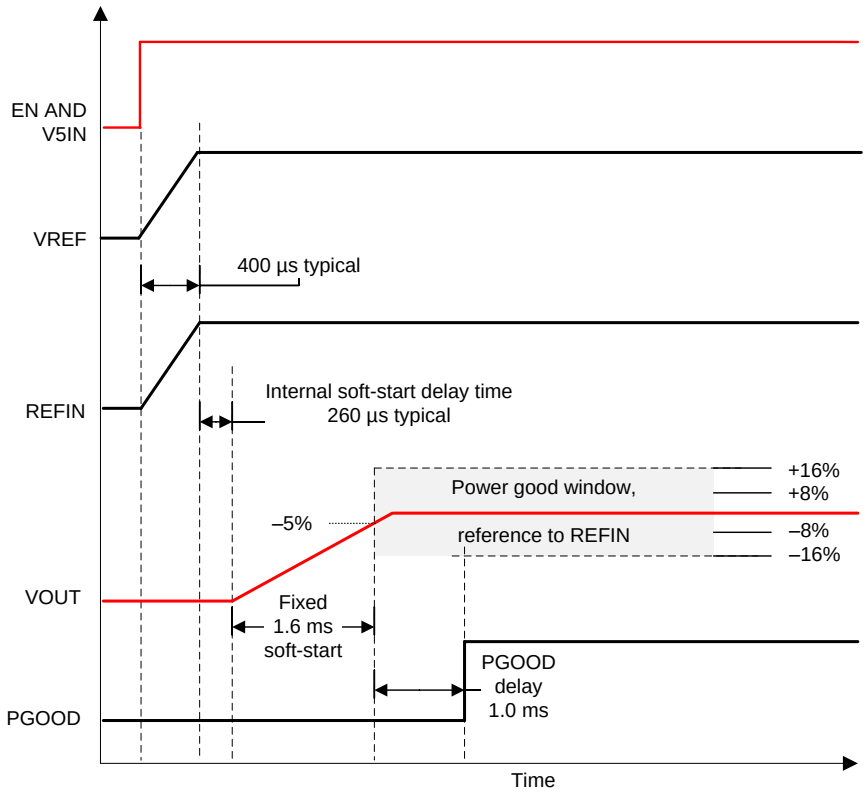


图 19. Non-Tracking Startup Timing

Feature Description (接下页)

7.3.4.2 Tracking Startup

The TPS53317A device can also be configured for tracking application. When tracking configuration is desired, output voltage is also regulated to the REFIN voltage which comes from an external power source. In order for the device to differentiate between a non-tracking configuration or a tracking configuration, there is a minimum delay time of 260 µs required between the time when VREF reaches 2 V to the time when the REFIN pin voltage can be applied, in order for the device to track properly (see 图 22). The valid REFIN voltage range is between 0.45 V and 2 V.

In a tracking application, the output voltage should be one half of the VDDQ voltage. VDDQ can be VIN or it can be an additional voltage rail. Thus, R1= R2 both in 图 20 and 图 21.

$$V_{OUT} = \frac{1}{2} \times V_{VDDQ} \quad (3)$$

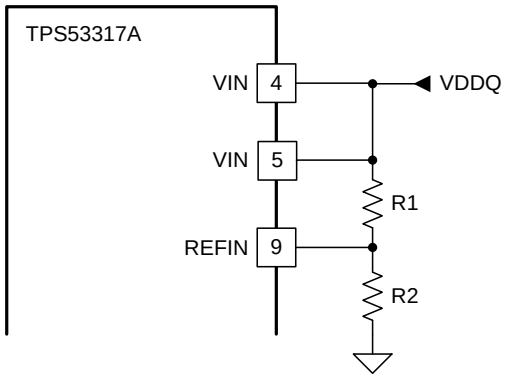


图 20. Tracking Configuration 1

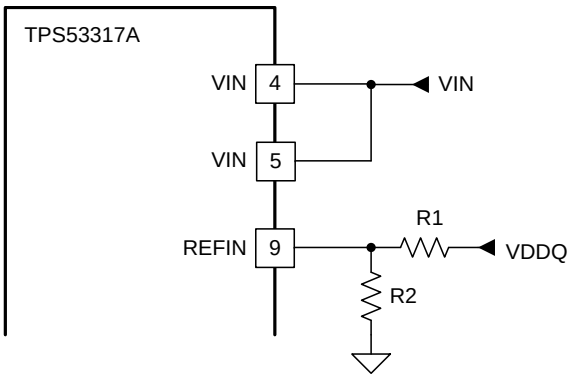


图 21. Tracking Configuration 2

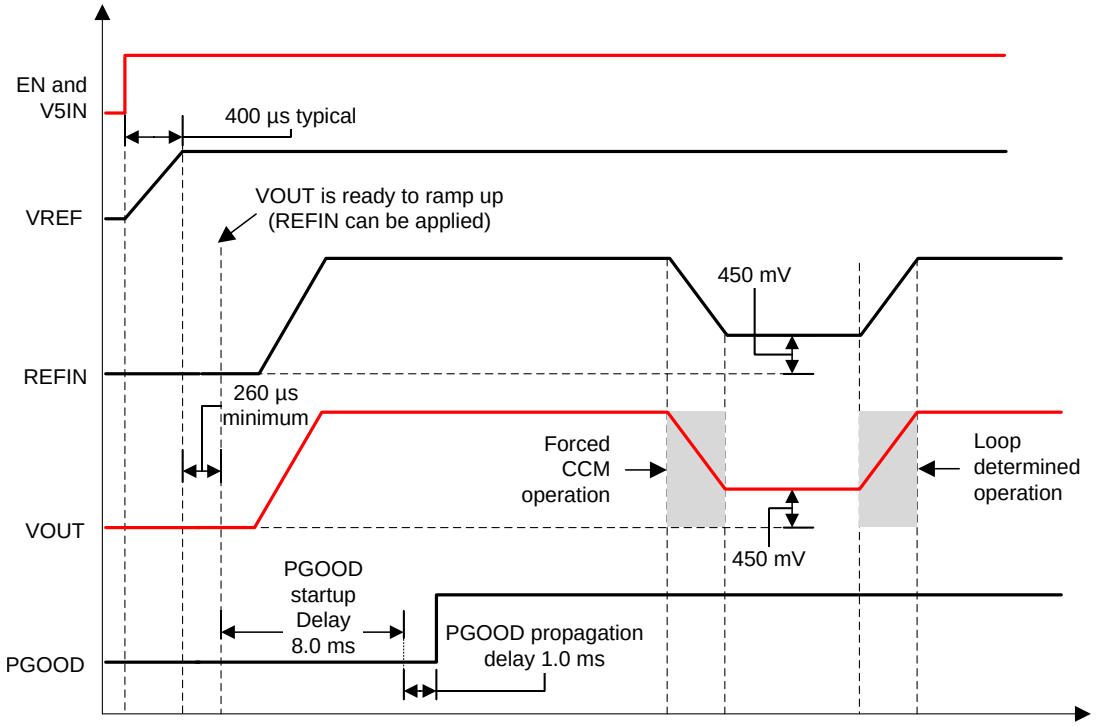


图 22. Tracking Startup Timing

Select PWM mode for an application that requires external tracking, because the output voltage can not be decreased during a no-load condition when the device operates in SKIP mode.

Feature Description (接下页)

7.3.5 Protection Features

The TPS53317A device offers many features to protect the converter power train as well as the system electronics.

7.3.5.1 5-V Undervoltage Protection (UVLO)

The TPS53317A device continuously monitors the voltage on the V5IN pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3 V and has a nominal 440 mV of hysteresis. If the 5-V UVLO limit is reached, the converter transitions the phase node into an off function, and the converter remains in the off state until the device is reset by cycling the 5-V supply until the 5-V POR is reached (2.3-V nominal). The power input does not have a UVLO function.

7.3.5.2 Power Good Signals

The TPS53317A device has one open-drain *power good* (PGOOD) pin. During startup, there is a 1-ms power good high propagation delay. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an undervoltage condition on V5IN or any other fault is detected.

7.3.5.3 Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS53317A device has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately 120% × V_{REFIN}. In this case, the converter de-asserts the PGOOD signals and performs the overvoltage protection function. During OVP, the low-side FET is always on before triggering a negative overcurrent. When a negative OC is also tripped, the low-side FET is no longer continuously on, and pulsed signals are generated to limit the negative inductor current. When the VOUT pin voltage drops below 250 mV, the low-side FET turns off and the converter latches off. The converter remains in the off state until the device is reset by cycling the 5-V supply until the 5-V POR is reached (2.3-V nominal) or when the EN pin is toggled off and on.

7.3.5.4 Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the *Overcurrent Protection* and *Overcurrent Limit* sections. If the output voltage drops below 68% of V_{REFIN}, after approximately a 250-µs delay, the device stops switching and enters hiccup mode. After a hiccup waiting time, a restart is attempted. If the fault condition is not cleared, hiccup mode operation may continue indefinitely.

7.3.5.5 Overcurrent Protection

Both positive and negative overcurrent protection are provided in the TPS53317A device.

- Overcurrent Limit (OCL)
- Negative OCL

7.3.5.5.1 Overcurrent Limit

If the sensed current value is above the OCL setting, the converter delays the next ON pulse until the current drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. The device uses a valley current limiting scheme where the DC OCL trip point is the OCL limit plus half of the inductor ripple current. The typical valley OCL threshold is 7.6 A or 5.4 A (depending on mode selection). The average output current limit calculation is shown in 公式 4.

During the overcurrent protection event, the output voltage droops if the duty cycle cannot satisfy output voltage requirements and continues to droop until the UVP limit is reached. Then, the converter de-asserts the PGOOD pin, and then enters hiccup mode after a 250-µs delay. The converter remains in hiccup mode until the fault is cleared.

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} \quad (4)$$

Feature Description (接下页)

7.3.5.5.2 Negative OCL

The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a *valley* mode, the typical value of the negative OCL set point is –9.3 A or –6.5 A (depending on mode selection).

7.3.6 Thermal Protection

The TPS53317A device has an internal temperature sensor. When the temperature reaches a nominal 145°C, the device shuts down until the temperature decreases by approximately 10°C, when the converter restarts.

7.4 Device Functional Modes

7.4.1 Non-Droop Configuration

The TPS53317A device can be configured as a non-droop solution. The benefit of a non-droop approach is that load regulation is flat, therefore, in a system where tight DC tolerance is desired, the non-droop approach is recommended. For the Intel system agent application, non-droop is recommended as the standard configuration.

The non-droop approach can be implemented by connecting a resistor and a capacitor between the COMP and the VREF pins. The purpose of the type II compensation is to obtain high DC feedback gain while minimizing the phase delay at unity gain cross over frequency of the converter.

The value of the resistor (R_C) can be calculated using the desired unity gain bandwidth of the converter, and the value of the capacitor (C_C) can be calculated by knowing where the zero location is desired. The capacitor C_P is optional, but recommended. Its appropriate capacitance value can be calculated using the desired pole location.

图 23 shows the basic implementation of the non-droop mode using the device

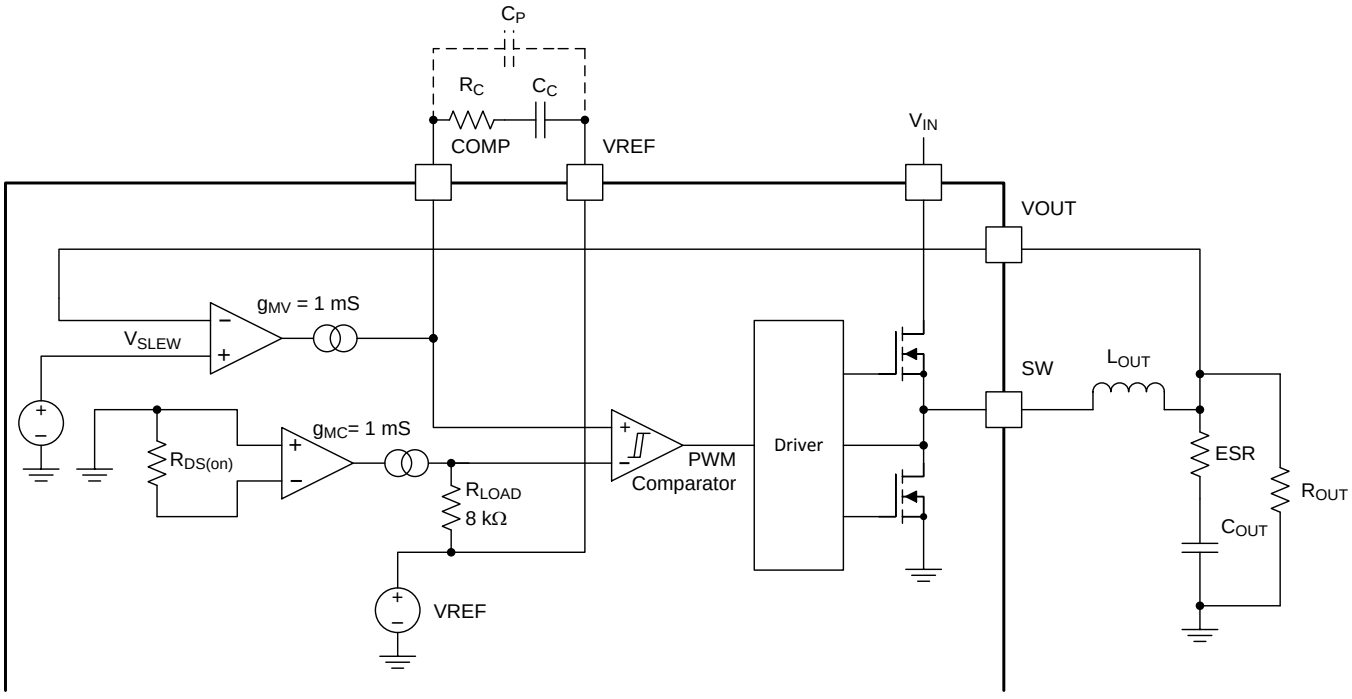


图 23. Non-Droop Mode Basic Implementation

Device Functional Modes (接下页)

图 24 shows shows the load regulation using non-droop configuration.

图 25 shows the transient response of the device using non-droop configuration, where C_{OUT} = 3 x 47 µF. The applied step load is from 0 A to 2 A.

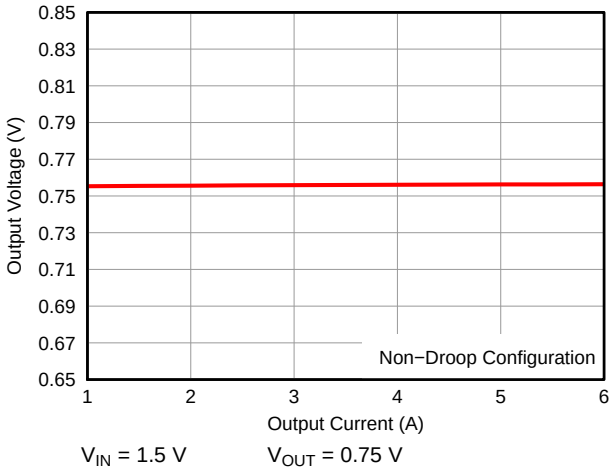


图 24. Load Regulation (Non-Droop Configuration)

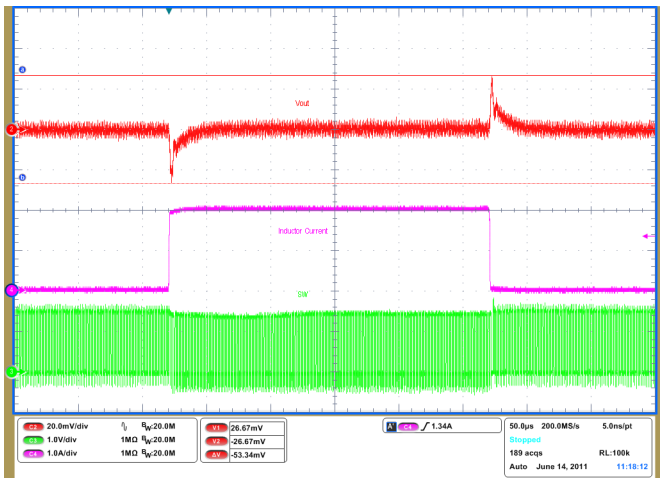


图 25. Non-Droop Configuration Transient Response

7.4.2 Droop Configuration

The terminology for droop is the same as *load line* or *voltage positioning* as defined in the Intel CPU V_{CORE} specification. Based on the actual tolerance requirement of the application, load-line set points can be defined to maximize either cost savings (by reducing output capacitors) or power reduction benefits.

Accurate droop voltage response is provided by the finite gain of the droop amplifier. The equation for droop voltage is shown in 公式 5.

$$V_{DROOP} = \frac{A_{CSINT} \times I_{OUT}}{R_{DROOP} \times g_M} \quad (5)$$

where

- low-side on-resistance is used as the current sensing element
- A_{CSINT} is a constant, which nominally is 53 mV/A.
- I_{OUT} is the DC current of the inductor, or the load current
- R_{DROOP} is the value of resistor from the COMP pin to the VREF pin
- g_M is the transconductance of the droop amplifier with nominal value of 1 mS

公式 6 can be used to easily derive R_{DROOP} for any load line slope/droop design target.

$$R_{LOAD\_LINE} = \frac{V_{DROOP}}{I_{OUT}} = \frac{A_{CSINT}}{R_{DROOP} \times g_M} \quad \therefore R_{DROOP} = \frac{A_{CSINT}}{R_{LOAD\_LINE} \times g_M} \quad (6)$$

Choose a value for the R_{DROOP} resistor that is below 20 kΩ. More than 20 kΩ of droop resistance may cause the loop to become unstable.

Device Functional Modes (接下页)

图 26 shows the basic implementation of the droop mode using the TPS53317A device.

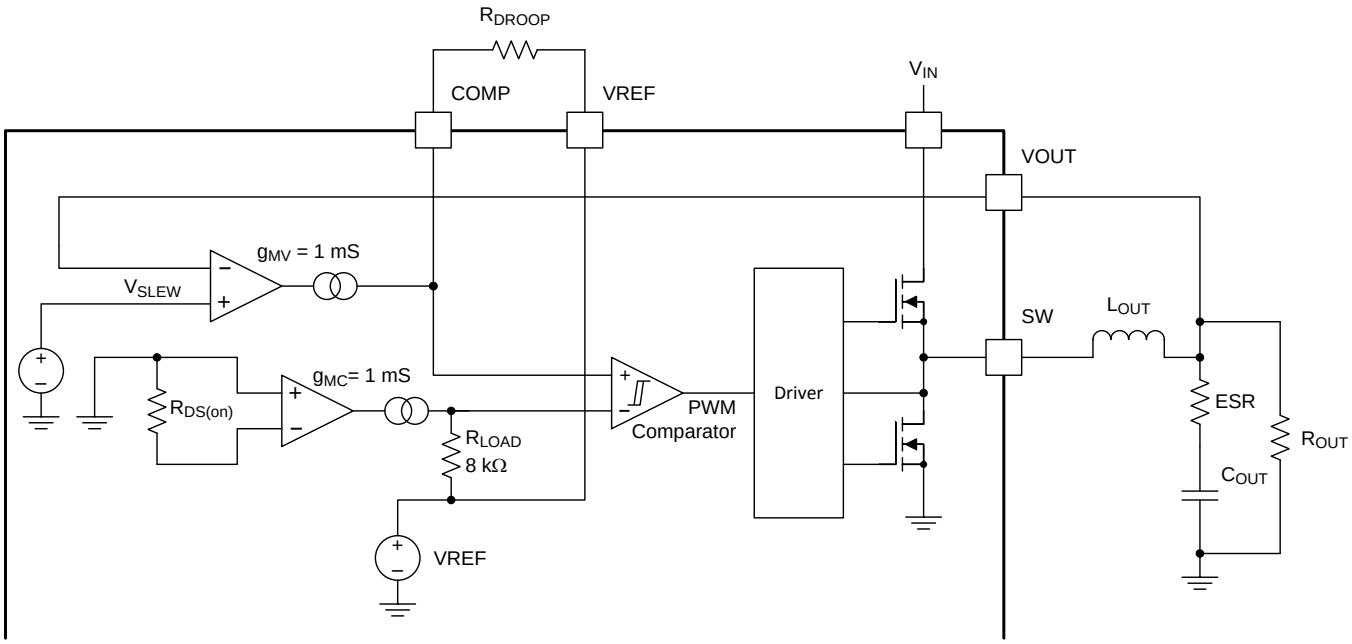


图 26. DROOP Mode Basic Implementation

The droop (voltage positioning) method was originally recommended to reduce the number of external output capacitors required. The effective transient voltage range is increased because of the active voltage positioning (see 图 27).

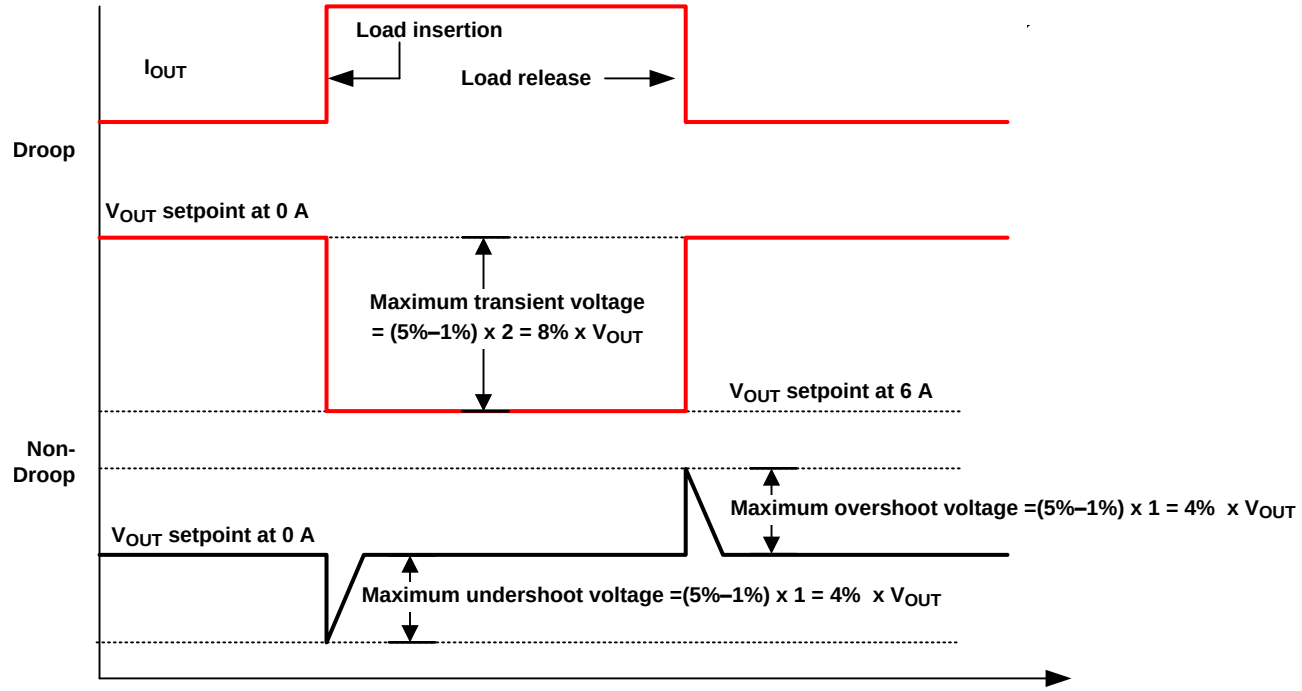


图 27. DROOP vs Non-DROOP in Transient Voltage Window

Device Functional Modes (接下页)

In applications where the DC and the AC tolerances are not separated, (meaning that there is no strict DC tolerance requirement) the droop method can be used.

表 1. Mode Definitions

MODE	MODE RESISTANCE (kΩ)	LIGHT-LOAD POWER SAVING MODE	SWITCHING FREQUENCY (f_{SW})	OVERCURRENT LIMIT (OCL) VALLEY (A)
1	0	SKIP	600 kHz	7.6
2	12		600 kHz	5.4
3	22		1 MHz	5.4
4	33		1 MHz	7.6
5	47	PWM	600 kHz	7.6
6	68		600 kHz	5.4
7	100		1 MHz	5.4
8	OPEN		1 MHz	7.6

图 28 shows the load regulation of the 1.5-V rail using an R_{DROOP} value of 6.8 kΩ.

图 29 shows the transient response of the TPS53317A device using droop configuration and C_{OUT} = 3 × 47 µF. The applied step load is from 0 A to 2 A.

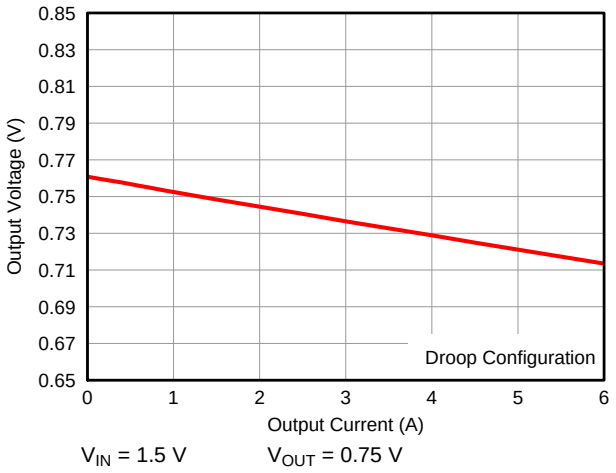


图 28. Load Regulation (Droop Configuration)

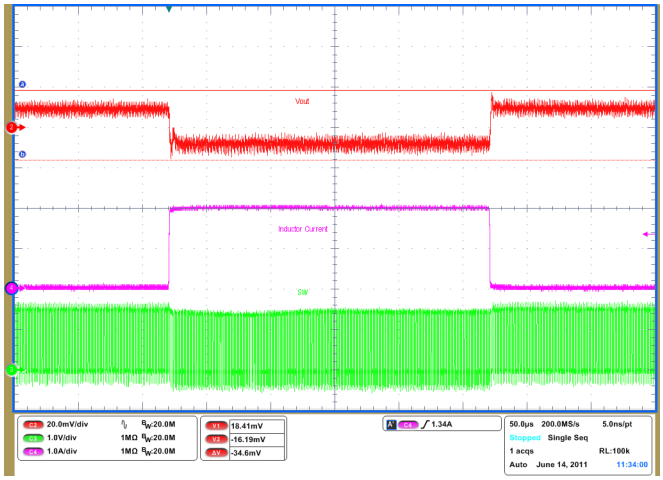


图 29. Droop Configuration Transient Response

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53317A device is a FET-integrated synchronous buck regulator designed mainly for DDR termination. It can provide a regulated output at ½ VDDQ with both sink and source capability. The device employs D-CAP+ mode operation that provides ease-of-use, low external component count and fast transient response.

8.2 Typical Applications

8.2.1 DDR4 SDRAM Application

This DDR4 application requires a tight load tolerance, fast transient response, and sinking current capability, the design uses a non-droop PWM configuration.

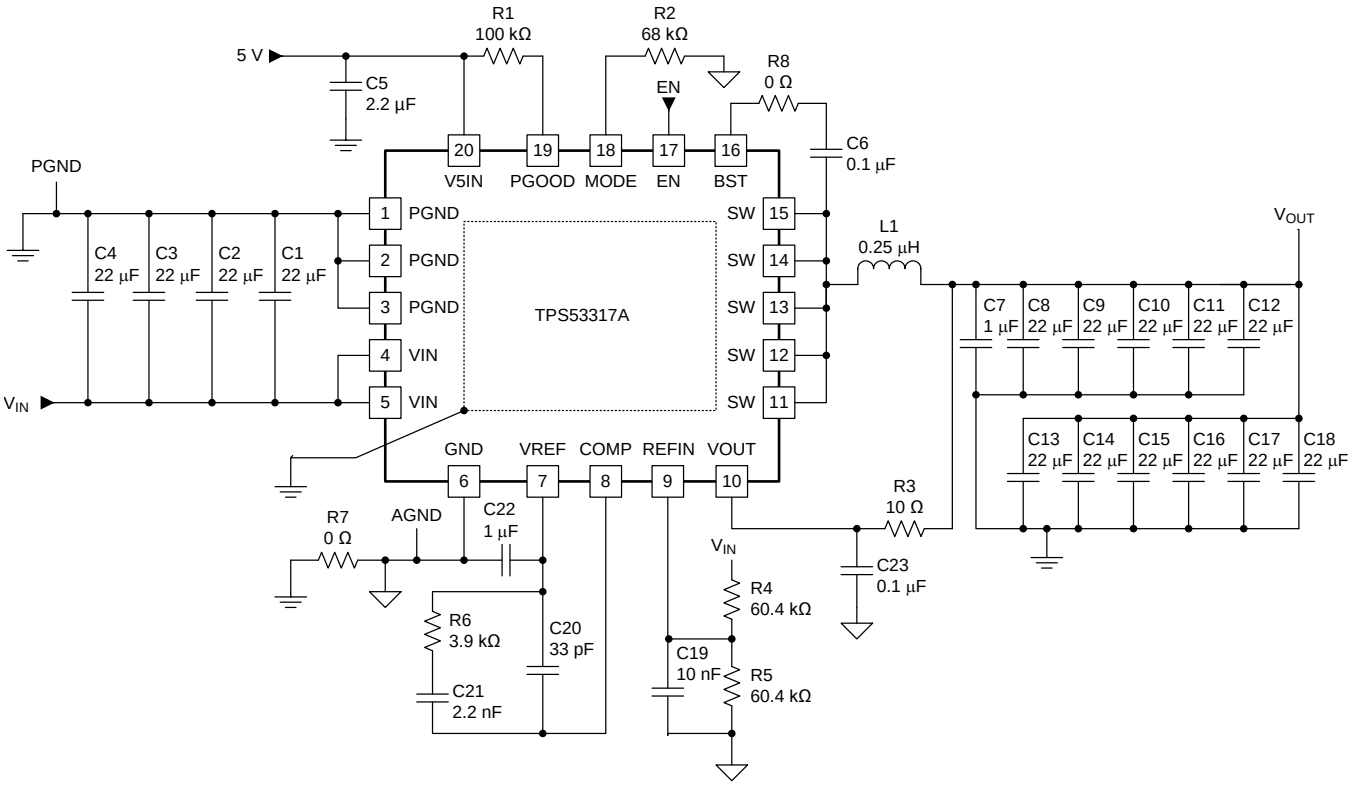


图 30. DDR4 SDRAM Application

8.2.1.1 Design Requirements

- Input voltage : V_{IN} = 1.2 V
- Output voltage: V_{OUT} = 0.6 V
- Maximum load step size of 3 A @ slew rate 7 A/µs (–1.5 A to 1.5 A)
- DC +AC + Ripple voltage regulation limit at sense point: ±42 mV (0.642 V overshoot, 0.558 V undershoot)
- Maximum load: I_{MAX} = 2.5 A

Typical Applications (接下页)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Step 1. Determine Configuration

Because this DDR4 application requires a tight load tolerance, fast transient response, and sinking current capability, the design uses a non-droop PWM configuration. Choose 600-kHz switching frequency due to the duty cycle and minimim off-time of the device, and set an overcurrent (OC) valley limit of 5.4 A due to the maximum load requirement of 2.5 A. Referring to 表 1 select an R_{MODE} value of 68 kΩ.

8.2.1.2.2 Step 2. Select Inductor

Smaller inductor values have better transient performance but higher ripple and lower efficiency. High values have the opposite characteristics. It is common practice to limit the ripple current to 30% to 50% of the maximum current. Choose 50% to allow use of a smaller inductor for faster transient performance.

$$\Delta I_{P-P} = 2.5\ A \times 0.5 = 1.25\ A \tag{7}$$

$$L = \frac{1}{f_{SW} \times \Delta I_{P-P}} \times V_{OUT} \times (1 - D)$$

where

- D = duty cycle (8)

Because this device operates in DCAP+ mode, the frequency and duty cycle vary based on the input voltage, the output voltage and load. With a 2.5-A load, a 1.2-V input voltage and 0.60 V output voltage, f_{SW} is experimentally measured at approximately 800 kHz and duty cycle of 0.55. Therefore L is calculated as shown in 公式 10.

$$L = \frac{1}{(800\ kHz \times 1.25\ A)} \times 0.6V \times 0.45 = 0.270\ \mu H \tag{9}$$

Choose the closest standard value, 0.25 µH.

8.2.1.2.3 Step 3. Determine Output Capacitance

Use 公式 10 to calculate the output capacitance for a desired maximum overshoot.

$$C_{OUT(min),OS} = \frac{\Delta I_{OUT}^2 \times L}{2 \times V_{OUT} \times V_{OS}}$$

where

- $C_{OUT(min),OS}$ is the minimum output capacitance for a desired overshoot
- ΔI_{OUT} is the maximum output current change in the application
- V_{OUT} = desired output voltage
- V_{OS} is the desired output voltage change due to overshoot (10)

Choose a value of 30 mV to account for normal output voltage ripple.

$$C_{OUT(min),OS} = \frac{(3\ \text{A})^2 \times 0.25\ \mu H}{2 \times 0.6\ V \times 0.03\ V} = 62.5\ \mu F \tag{11}$$

Use 公式 12 to calculate the necessary output capacitance for a desired maximum undershoot.

$$C_{OUT(min),US} = \frac{\Delta I_{OUT}^2 \times L \times \left(\frac{V_{OUT}}{V_{IN}} \times t_{SW} + t_{MIN(off)}\right)}{2 \times V_{OUT} \times V_{US} \times \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \times t_{SW} - t_{MIN(off)}\right)}$$

where

- $C_{OUT(min),US}$ is the minimum output capacitance for a desired undershoot
- V_{US} is the desired output voltage change due to overshoot
- t_{SW} is the period of switch node
- $t_{MIN(off)}$ is the minimum off-time (270 ns) (12)

Typical Applications (接下页)

Again, choose 30 mV to account for normal output voltage ripple.

$$C_{OUT(min),US} = \frac{(3\text{ A})^2 \times 0.25\ \mu H \times \left(\frac{0.6\ V}{1.2\ V} \times \frac{1}{800\ kHz} + 270\ ns\right)}{2 \times 0.6\ V \times 0.03\ V \times \left(\frac{1.2\ V - 0.6\ V}{1.2\ V} \times \frac{1}{800\ kHz} - 270\ ns\right)} = 157.6\ \mu F \quad (13)$$

The undershoot requirements determine, so there must be a minimum of 157.6 µF. Because this is a DDR application where size is also a consideration, this design uses only ceramic capacitors. To account for voltage de-rating of capacitors and provide additional margin, this design includes eleven 22-µF output capacitors.

8.2.1.2.4 Step 4. Input Capacitance

This design requires sufficient input capacitance to filter the input current from the host source. Use 公式 14 to calculate the necessary input capacitance.

$$C_{IN(min)} = I_{out} \times \frac{D \times (1 - D)}{\Delta V_{IN(P-P)} \times f_{SW}}$$

where

- $\Delta V_{IN(P-P)}$ is the desired input voltage ripple (typically 1% of the input voltage) (14)

$$C_{IN(min)} = 2.5\ A \times \frac{0.55 \times (1 - 0.55)}{12\text{ mV} \times 800\ kHz} = 64.45\ \mu F \quad (15)$$

As with the output capacitance selection, this design accounts for voltage de-rating of capacitors and provides additional margin, using four 22-µF input capacitors.

8.2.1.2.5 Step 5. Compensation Network

In order to achieve stable operation, the crossover frequency should be less than 1/5 of the switching frequency.

$$f_{CO} = \frac{1}{2\pi} \times \frac{g_M}{C_{OUT}} \times \frac{R_C}{R_S} = 80\ kHz$$

where

- R_S = 53 mΩ (16)

Account for capacitor de-rating here and set the value of C_{OUT} to 160 µF, so that 公式 17 is true.

$$R_C = \frac{f_{CO} \times R_S \times 2\pi \times C_{OUT}}{g_M} = \frac{80\ kHz \times 53\ m\Omega \times 2\pi \times 160\ \mu F}{1\ mS} = 4.26\ k\Omega \quad (17)$$

Choose an R_C value of 3.9 kΩ. Determine C_C by choosing the value of the zero created by R_C and C_C. Using the relationship described in 公式 18.

$$f_z = \frac{f_{CO}}{5} = \frac{1}{2\pi \times R_C \times C_C} \quad (18)$$

公式 18 yields a C_C value of 2.55 nF. Choose the closest common capacitor value of 2.2 nF. To determine a value for C_P, first consider the relationship described in 公式 19.

$$f_p = \frac{1}{2\pi \times R_C \times \frac{C_C \times C_P}{C_C + C_P}} \approx \frac{1}{2\pi \times R_C \times C_P}$$

- $C_C >> C_P$ (19)

Because $C_C >> C_P$, set the pole to be two times the switching frequency as described in 公式 20.

$$C_P \cong \frac{1}{2\pi \times R_C \times 2f_{SW}} = \frac{1}{2\pi \times 3.9\ k\Omega \times 2 \times 800\ kHz} = 25.5\ pF \quad (20)$$

To boost the gain margin, set C_P to 33 pF.

Typical Applications (接下页)

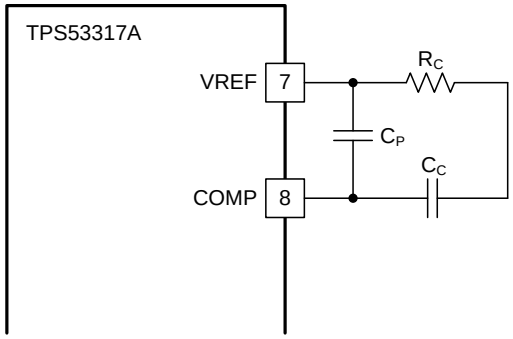


图 31. Compensation Network Circuit

8.2.1.2.6 Peripheral Component Selection

As described in 表 1, connect a 0.22-µF capacitor from the VREF pin to GND and connect a 0.1-µF bootstrap capacitor from the SW pin to the BST pin. Because the PGOOD pin is open drain, connect a pullup resistor between it and the 5-V rail.

8.2.1.3 Application Curves

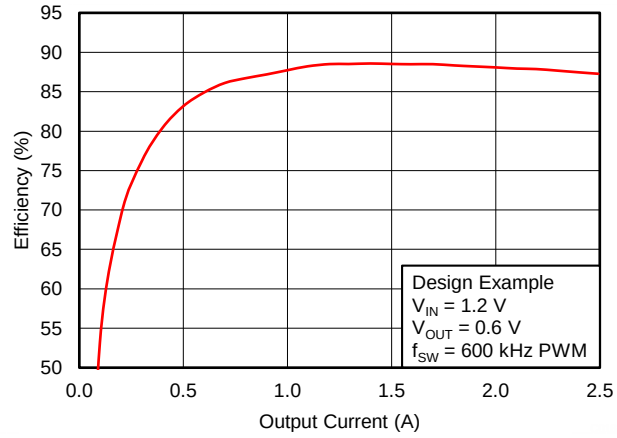


图 32. Efficiency

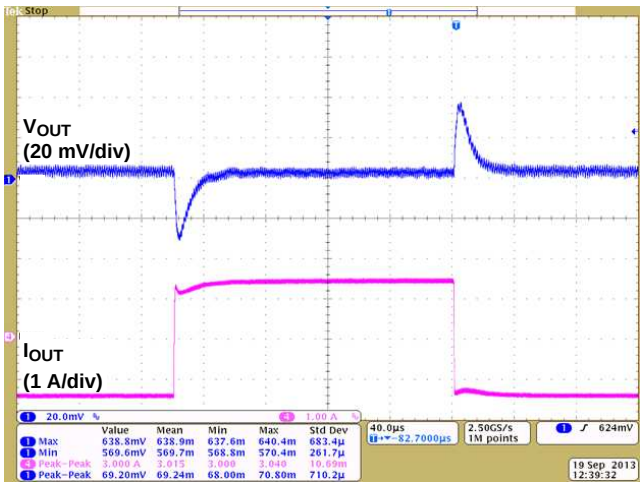


图 33. Load Transient

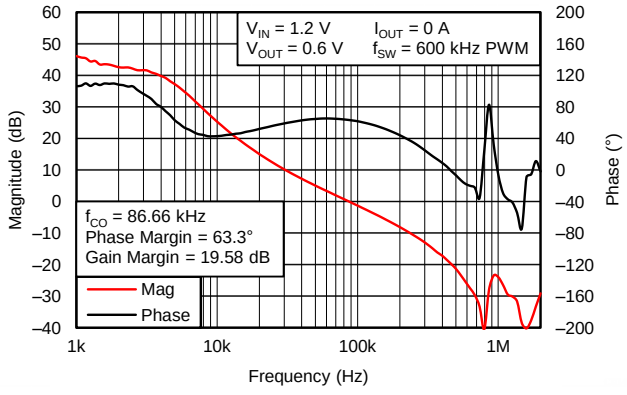


图 34. Bode Plot, No Load

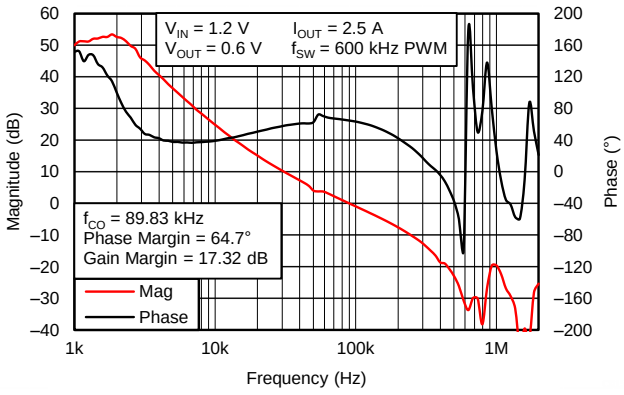


图 35. Bode Plot, Full Load

Typical Applications (接下页)

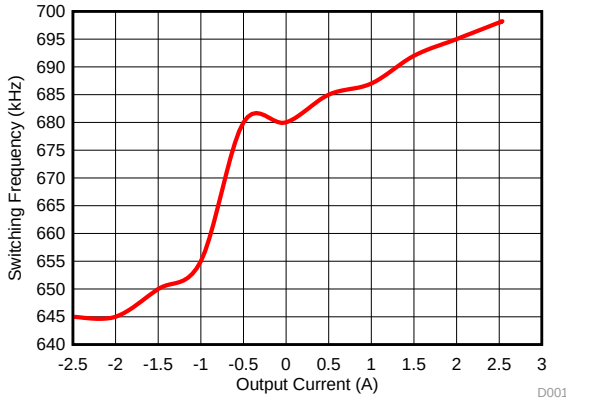


图 36. Switching Frequency vs. Load

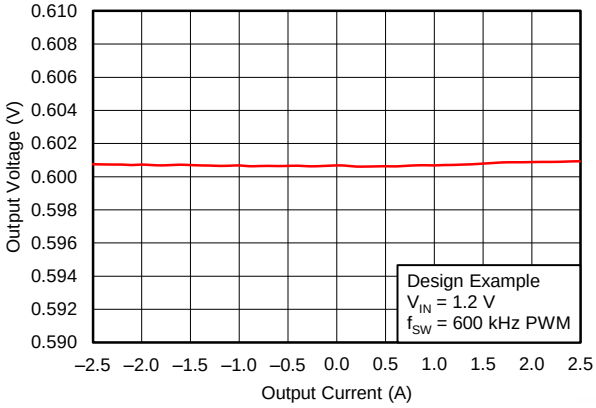


图 37. Load Regulation

8.2.2 DDR3 SDRAM Application

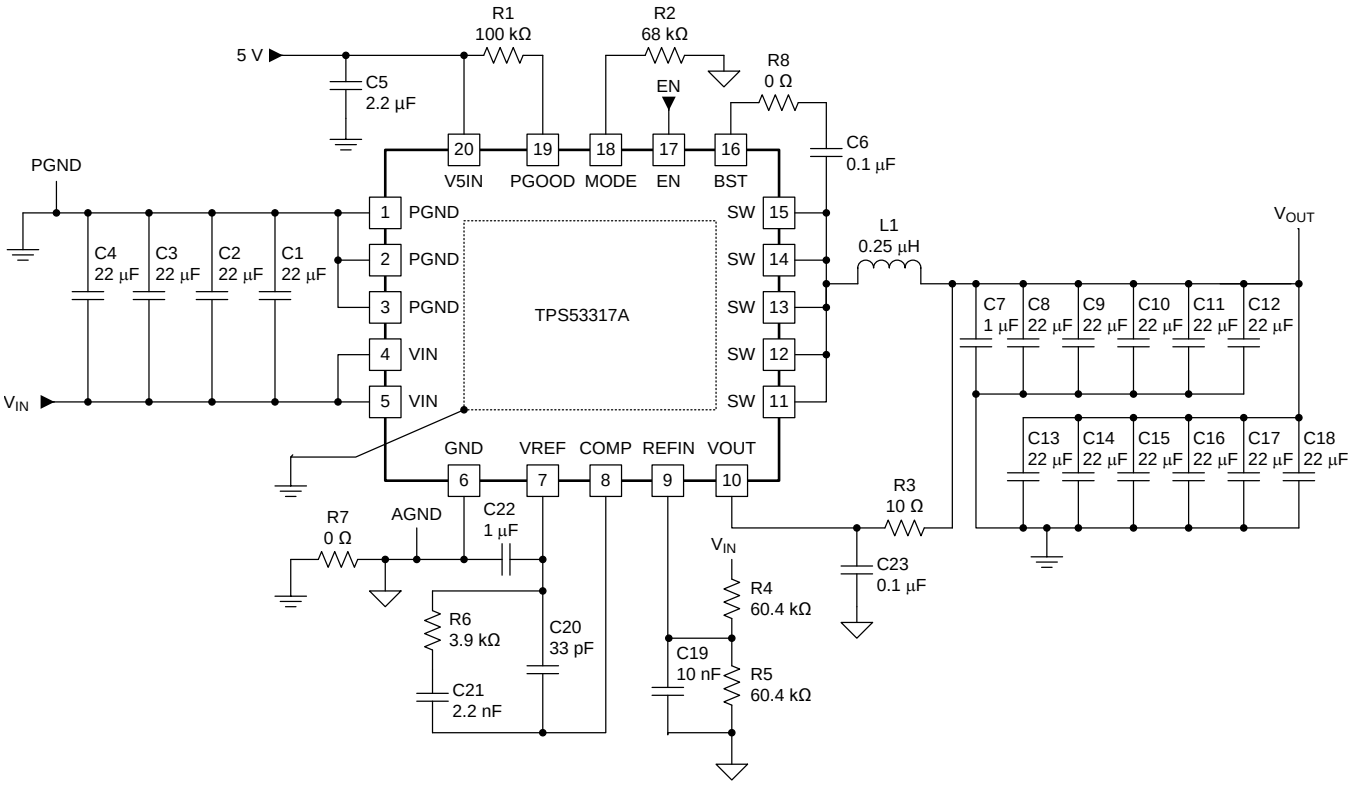


图 38. Typical Application Schematic, DDR3

8.2.2.1 Design Requirements

- V_{IN} = 1.5 V
- V_{OUT} = 0.75 V

Typical Applications (接下页)

8.2.3 Non-Tracking Point-of-Load (POL) Application

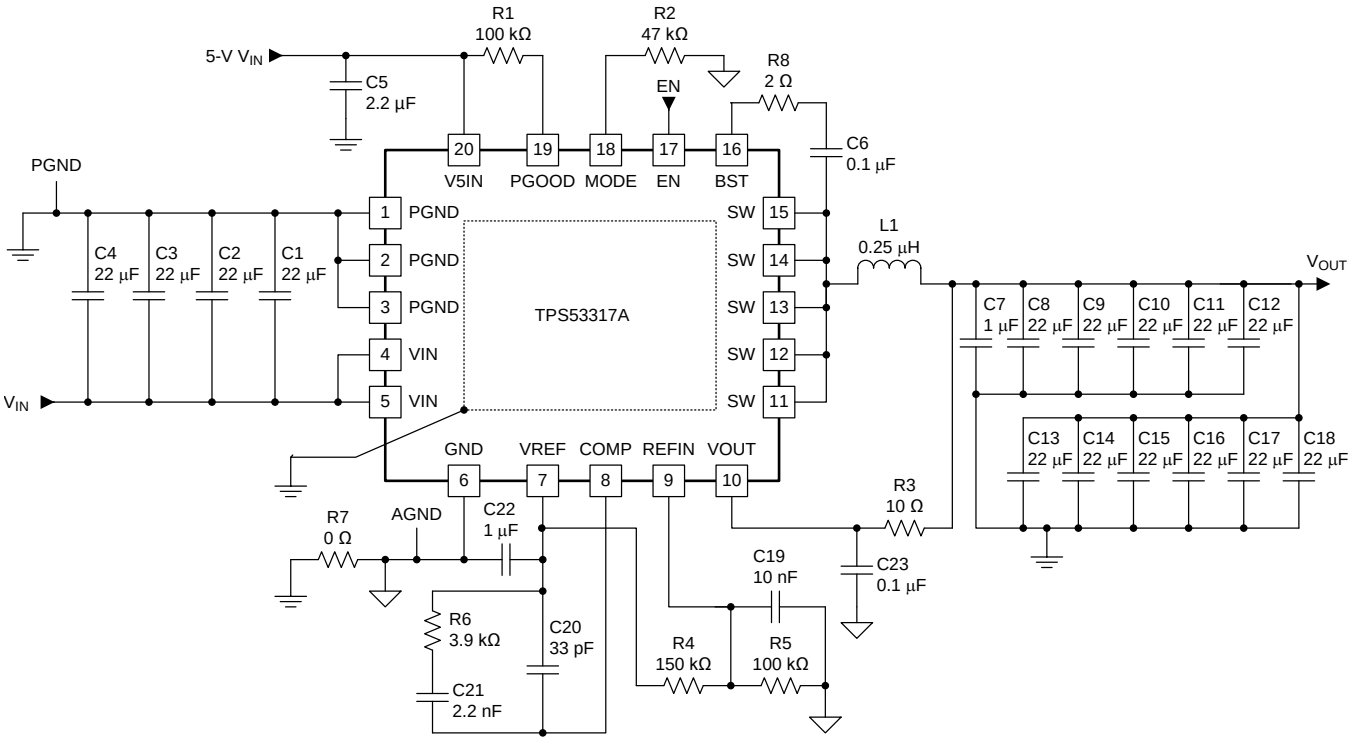


图 39. Typical Application Schematic, Non-Tracking Point-of-Load (POL)

8.2.3.1 Design Requirements

- V_{IN} = 3.3 V
- V_{OUT} = 1.2 V

8.2.3.2 Application Curves

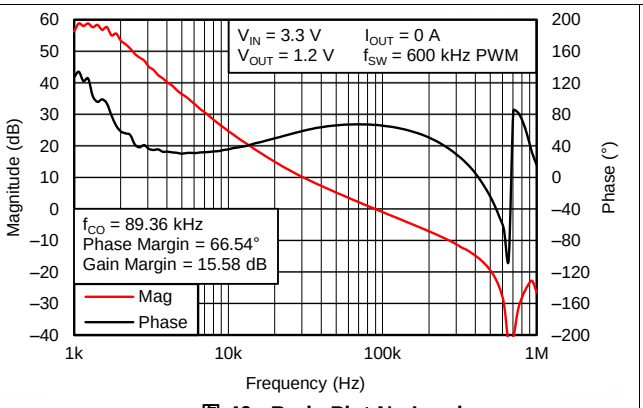


图 40. Bode Plot No Load

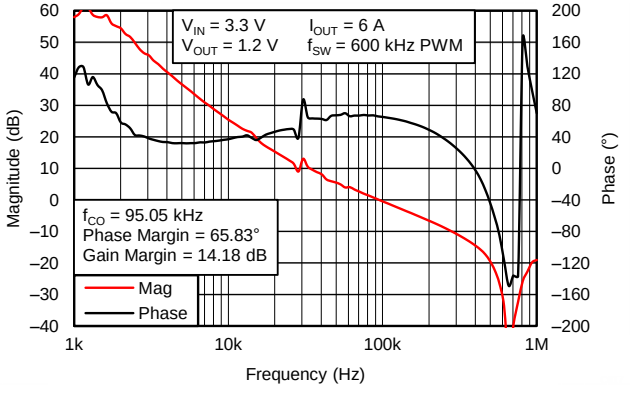


图 41. Bode Plot Full Load

9 Power Supply Recommendations

This device operates from an input voltage supply between 0.9 V and 6 V. This device requires a separate 5-V power supply for analog circuits and gate drive. Use the proper bypass capacitors for both the input supply and the 5-V supply in order to filter noise and to ensure proper device operation.

10 Layout

10.1 Layout Guidelines

Stable power supply operation depends on proper layout. Follow these guidelines for an optimized PCB layout.

- Connect PGND pins to the thermal pad underneath the device. Use four vias to connect the thermal pad to internal ground planes.
- Place VIN, V5IN and VREF decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, PGND and SW pins. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Place COMP and VOUT analog signal traces away from noisy signals (SW, BST).
- The GND pin should connect to the PGND in only one place, through a via or a 0-Ω resistor.

10.2 Layout Example

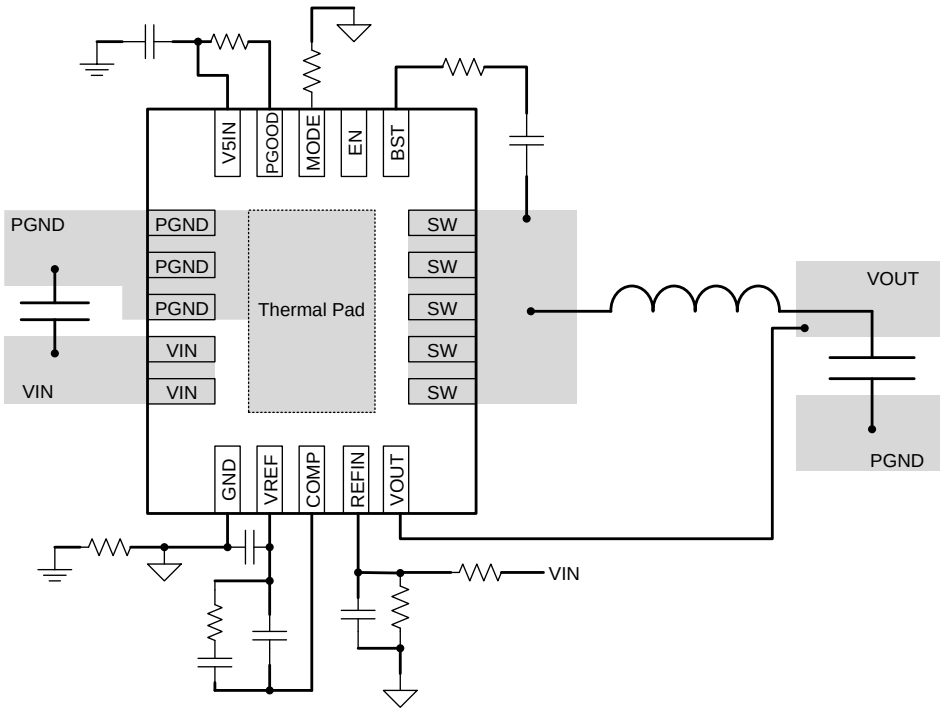


图 42. TPS53317A Board Layout

11 器件和文档支持

11.1 社区资源

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53317ARGBR	ACTIVE	VQFN	RGB	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53317A	Samples
TPS53317ARGBT	ACTIVE	VQFN	RGB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53317A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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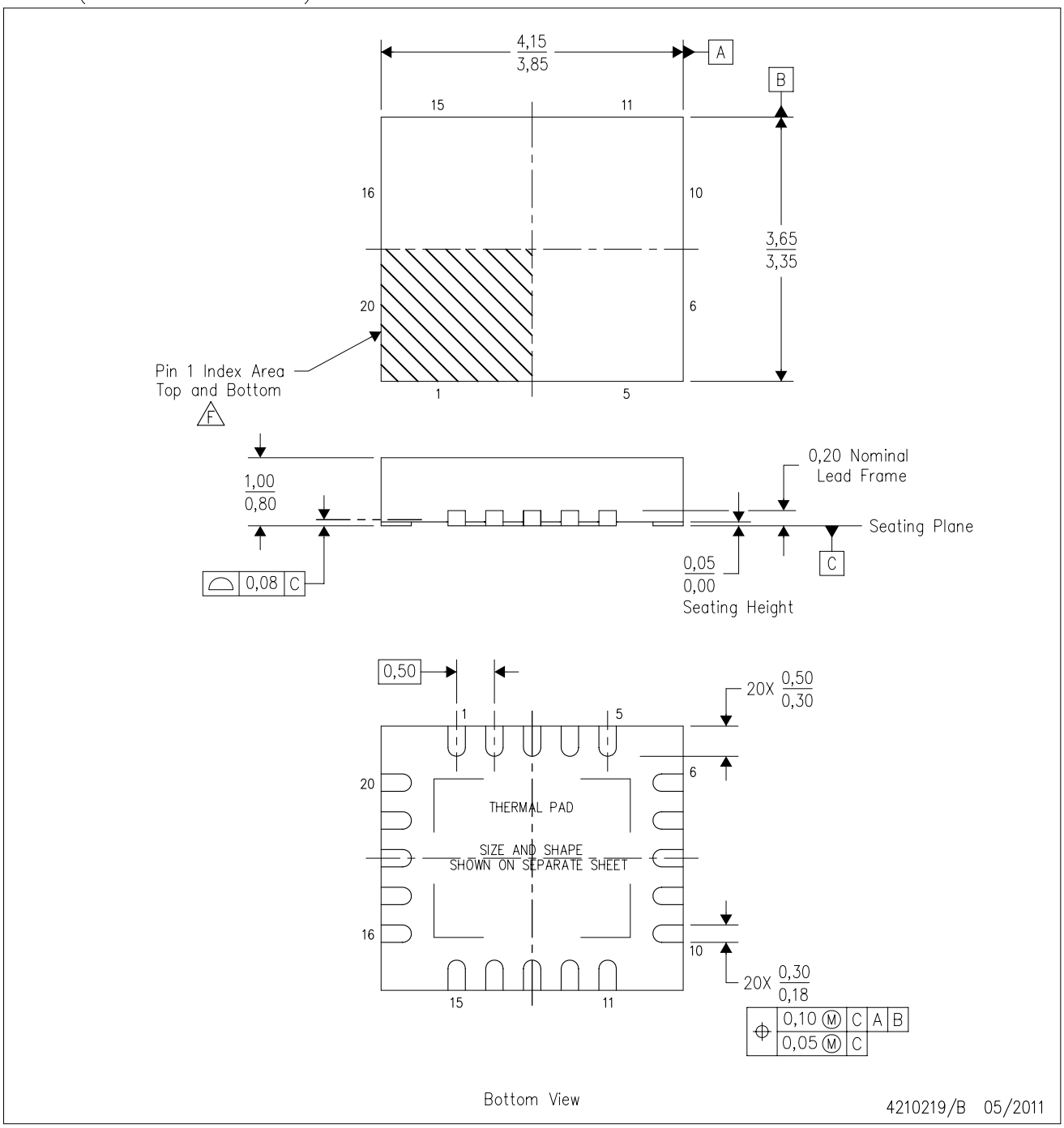


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

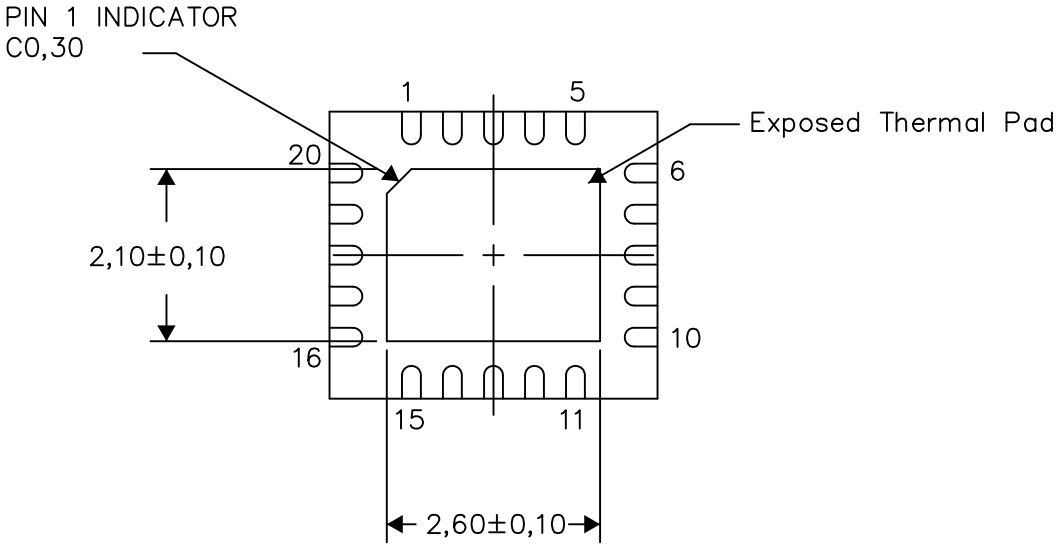
RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



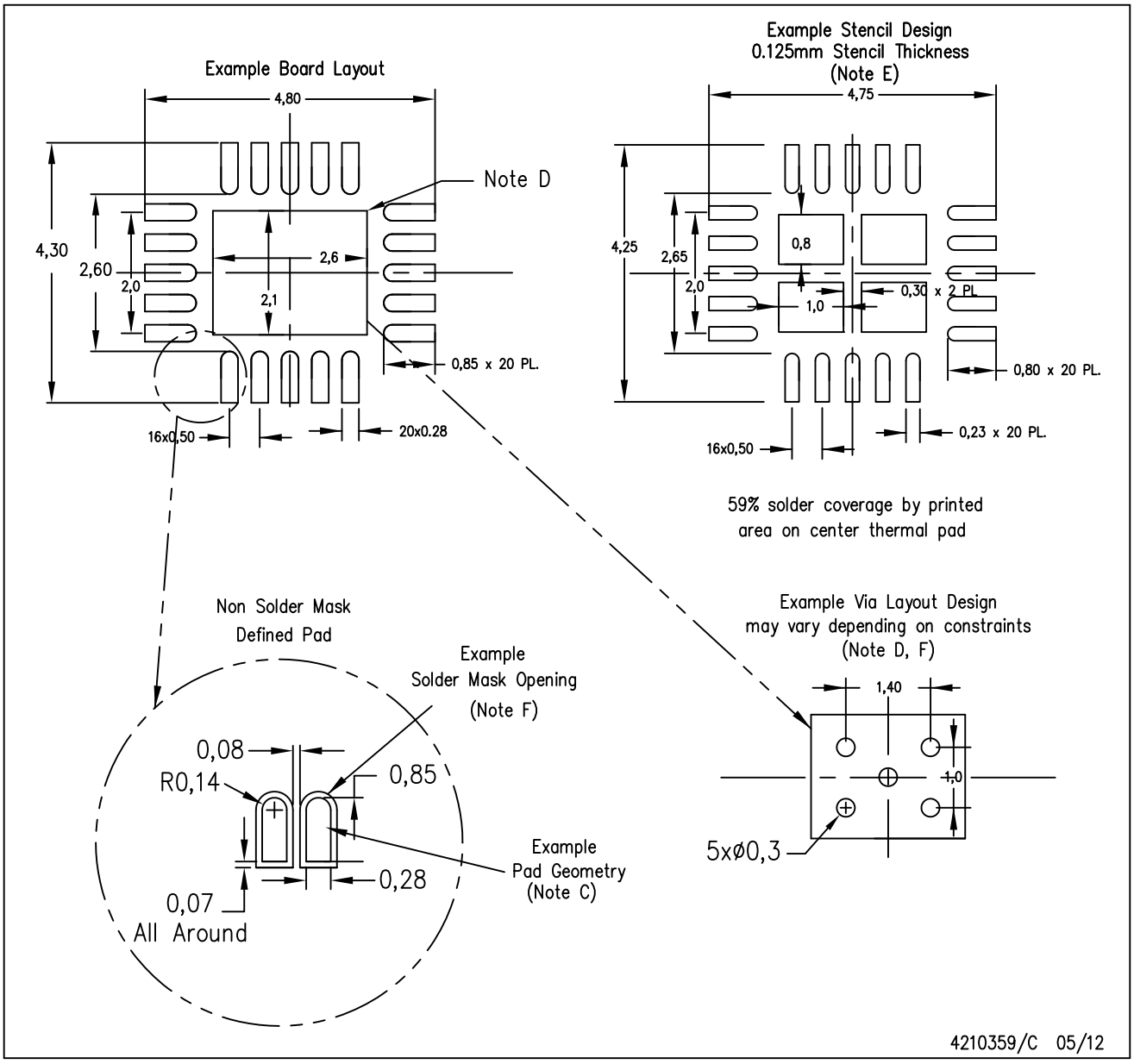
Bottom View

Exposed Thermal Pad Dimensions

4210242/C 05/12

NOTE: All linear dimensions are in millimeters

RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



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C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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