EMC 性能优异的 ISO772x 高速双通道增强型数字隔离器

1 特性

- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 和 5V 电平转换
- 默认输出*高电平*和*低电平*选项
- 宽温度范围：-55°C 至 +125°C
- 低功耗，1Mbps 时每通道的电流典型值为 1.7mA
- 低传播延迟：典型值为 11ns（由 5V 电源供电）
- 高共模瞬态抗扰度 (CMTI)：±100kV/μs（典型值）
- 优异的电磁兼容性 (EMC)
  - 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
  - 低辐射
- 隔离栅寿命：> 40 年
- 宽体小外形尺寸集成电路 (SOIC) (DW-16) 和窄体小外形尺寸集成电路 (SOIC) (D-8) 封装选项
- 安全相关认证：
  - VDE 增强型隔离，符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准
  - 符合 UL 1577 的 $5000V_{RMS}$ (DW) 和 $3000V_{RMS}$ (D) 隔离额定值
  - CSA 组件验收通知 5A、IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证
  - 符合 EN 60950-1 和 EN 61010-1 标准的 TUV 认证
  - 完成 DW 封装的 VDE、UL、CSA 和 TUV 认证；已规划其他所有认证

2 应用

- 工业自动化
- 混合动力电动汽车
- 电机控制
- 电源
- 太阳能逆变器
- 医疗设备

3 说明

ISO772x 器件是高性能双通道数字隔离器，可提供符合 UL 1577 的 $5000V_{RMS}$（DW 封装）和 $3000V_{RMS}$（D 封装）隔离额定值。这些器件还通过了 VDE、TUV、CSA 和 CQC 认证。

在隔离互补金属氧化物半导体 (CMOS) 或者低电压互补金属氧化物半导体 (LVCMOS) 数字 I/O 的同时，ISO772x 器件还可提供高电磁抗扰度和低辐射，同时具备低功耗特性。每个隔离通道都有一个由二氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器。ISO7720 器件具有两条同向通道，而 ISO7721 器件具有两条反向通道。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出*高电平*，带后缀 F 的器件默认输出*低电平*。更多详细信息，请参见 *器件功能模式* 部分。

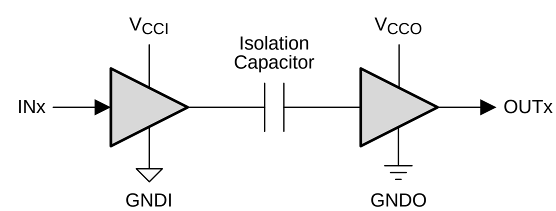
与隔离式电源一起使用时，这些器件有助于防止数据总线或者其他电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。凭借创新型芯片设计和布线技术，ISO772x 器件的电磁兼容性得到了显著增强，可缓解系统级 ESD、EFT 和浪涌问题并符合辐射标准。ISO772x 系列器件可提供 16 引脚 SOIC 宽体 (DW) 和 8 引脚 SOIC 窄体 (D) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7720，ISO7721，ISO7721F，ISO7721F	SOIC (D)	4.90mm x 3.91mm
	SOIC (DW)	10.30mm x 7.50mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

LP38690 的



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2016) to Revision B — **Page**

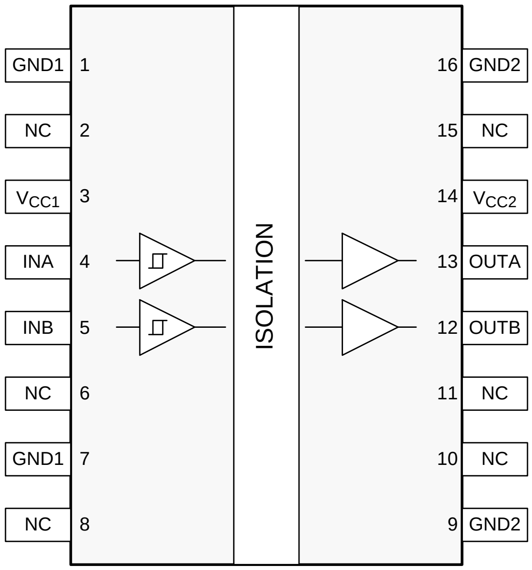
- Added D-8 values for TUV in the *Safety-Related Certifications* table ... 7
- Changed the minimum CMTI value from 40 kV/μs to 85 kV/μs in all *Electrical Characteristics* tables ... 8
- 已添加 *接收文档更新通知* 部分 ... 22
- 已更改 *静电放电注意事项* 声明 ... 22

Changes from Original (November 2016) to Revision A — **Page**

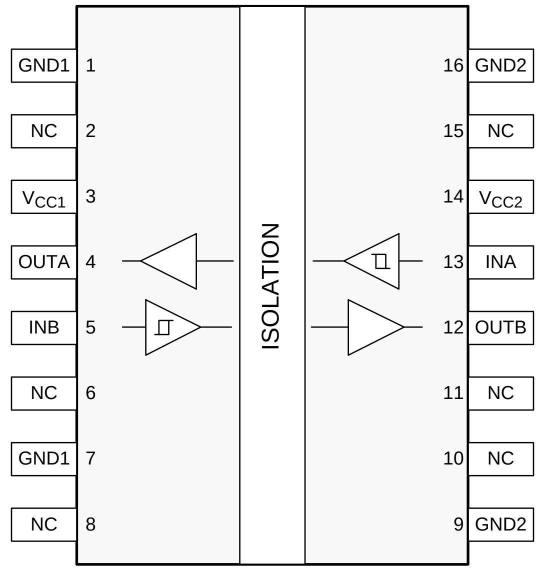
- 已将*特性*从"IEC 60950-1、IEC 60601-1 和 IEC 61010-1 终端设备标准"更改为"IEC 60950-1 和 IEC 60601-1 终端设备标准" ... 1
- Added Climatic category to the *Insulation Specifications* ... 6
- Changed the CSA column of *Regulatory Information* ... 7
- Changed DW package) To: (DW-16) in the TUV column of *Regulatory Information* ... 7
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—5-V Supply* ... 11
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—3.3-V Supply* ... 11
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—2.5-V Supply* ... 11

5 Pin Configuration and Functions

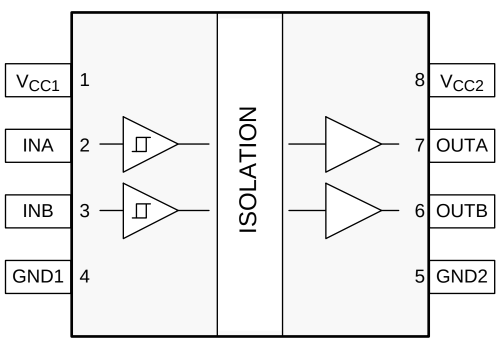
ISO7720 DW Package
16-Pin SOIC
Top View



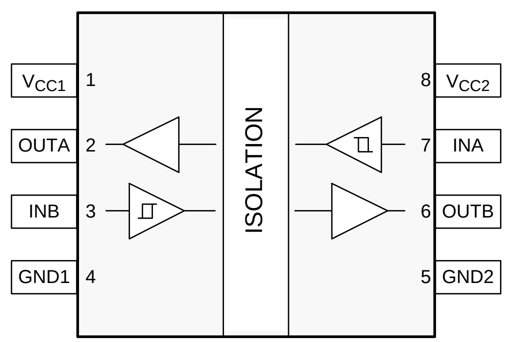
ISO7721 DW Package
16-Pin SOIC
Top View



ISO7720 D Package
8-Pin SOIC
Top View



ISO7721 D Package
8-Pin SOIC
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	DW PACKAGE		D PACKAGE			
	ISO7720	ISO7721	ISO7720	ISO7721		
GND1	1, 7	1, 7	4	4	—	Ground connection for V_{CC1}
GND2	9	9	5	5	—	Ground connection for V_{CC2}
	16	16				
INA	4	13	2	7	I	Input, channel A
INB	5	5	3	3	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	—	—	Not connected
OUTA	13	4	7	2	O	Output, channel A
OUTB	12	12	6	6	O	Output, channel B
V_{CC1}	3	3	1	1	—	Power supply, V_{CC1}
V_{CC2}	14	14	8	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See [1].

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage[2]	–0.5	6	V
V	Voltage at INx, OUTx	–0.5	V_{CC} + 0.5[3]	V
I_O	Output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO}[1] = 5 V	–4			mA
		V_{CCO} = 3.3 V	–2			
		V_{CCO} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}[1]		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR	Signaling rate		0		100	Mbps
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.4 Thermal Information

THERMAL METRIC[(1)]		ISO772x		UNIT
		DW (SOIC)	D (SOIC)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.6	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	71.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.3	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.2	70.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7720						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			20	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			80	mW
ISO7721						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			50	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			50	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	D-8	
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I–III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	n/a	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 (2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test	1000	450	V_{RMS}
		DC voltage	1414	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); t = 1 s (100% production)	8000	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	5000	V_{PK}
q_{pd}	Apparent charge (4)	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output (5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance (5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	5/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s(qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

DW package devices certified according to VDE, CSA, UL, and TUV; All other certifications are planned.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Maximum transient isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 1414 V_{PK} (DW-16, Reinforced) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 5000 V_{PK} (D-8)	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (DW-16) max working voltage	**DW-16:** Single protection, 5000 V_{RMS}; **D-8:** Single protection, 3000 V_{RMS}	**DW-16:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; **D-8:** Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (D-8) 5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certification planned	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 86.5 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			263	mA
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			401	
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			525	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 86.5 °C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1445	mW
T_S	Maximum safety temperature				150	°C
D-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 137.7 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			165	mA
		$R_{\theta JA}$ = 137.7 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			252	
		$R_{\theta JA}$ = 137.7 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 3			330	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 137.7 °C/W, T_J = 150°C, T_A = 25°C, see Figure 4			908	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 13	V_{CCO}[1] – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 13		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$[1] at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 15	85	100		kV/μs
C_I	Input Capacitance[2]	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), V_I = 0 V (ISO7720 with F suffix)		I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
	V_I = 0 V (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.3	1.9	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		2.2	3	
		100 Mbps	I_{CC1}		2.5	3.2	
			I_{CC2}		11.6	14	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), V_I = 0 V (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		1	1.6	mA
	V_I = 0 V (ISO7721), $V_I = V_{CCI}$ (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.7	2.4	
		10 Mbps	I_{CC1}, I_{CC2}		2.2	3	
		100 Mbps	I_{CC1}, I_{CC2}		7.3	9	

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 13	V_{CCO} (1) – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 13		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, VCM = 1200 V; see Figure 15	85	100		kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal	V_I = V_{CCI} (ISO7720), V_I = 0 V (ISO7720 with F suffix)		I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
	V_I = 0 V (ISO7720), V_I = V_{CCI} (ISO7720 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.2	1.9	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		1.9	2.6	
		100 Mbps	I_{CC1}		2.2	3.1	
			I_{CC2}		8.6	11	
ISO7721							
Supply current - DC signal	V_I = V_{CCI} (ISO7721), V_I = 0 V (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		1	1.6	mA
	V_I = 0 V (ISO7721), V_I = V_{CCI} (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.4	
		10 Mbps	I_{CC1}, I_{CC2}		2	2.8	
		100 Mbps	I_{CC1}, I_{CC2}		5.6	7	

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 13	V_{CCO} (1) – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 13		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, VCM = 1200 V; see Figure 15	85	100		kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal	V_I = V_{CCI} (ISO7720), V_I = 0 V (ISO7720 with F suffix)		I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
	V_I = 0 V (ISO7720), V_I = V_{CCI} (ISO7720 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.3	1.9	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		1.7	2.4	
		100 Mbps	I_{CC1}		2.2	3	
			I_{CC2}		6.8	9	
ISO7721							
Supply current - DC signal	V_I = V_{CCI} (ISO7721), V_I = 0 V (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		1	1.6	mA
	V_I = 0 V (ISO7721), V_I = V_{CCI} (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.4	
		10 Mbps	I_{CC1}, I_{CC2}		1.9	2.7	
		100 Mbps	I_{CC1}, I_{CC2}		4.6	6	

6.15 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion(1) $\|t_{PHL} – t_{PLH}\|$	See Figure 13		0.5	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 13		1.8	3.9	ns
t_f	Output signal fall time	See Figure 13		1.9	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion(1) $\|t_{PHL} – t_{PLH}\|$	See Figure 13		0.5	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 13		0.7	3	ns
t_f	Output signal fall time	See Figure 13		0.7	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	7.5	12	18.5	ns
PWD	Pulse width distortion(1) $\|t_{PHL} – t_{PLH}\|$	See Figure 13		0.5	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See Figure 13		1	3.5	ns
t_f	Output signal fall time	See Figure 13		1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

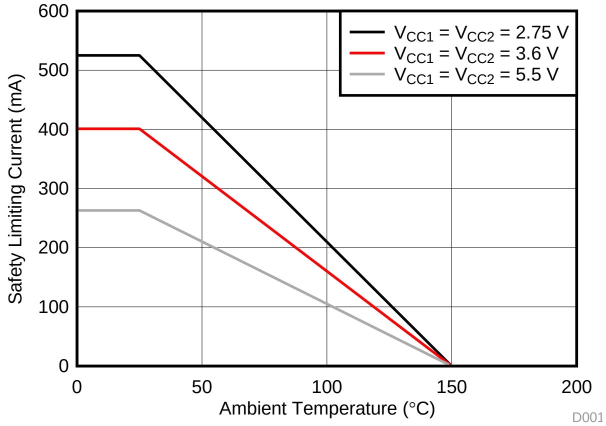


Figure 1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

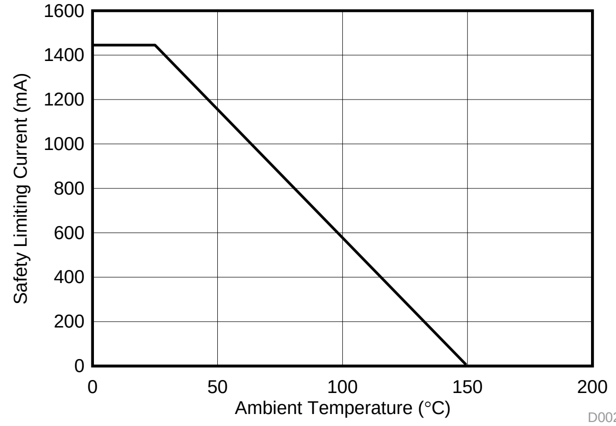


Figure 2. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

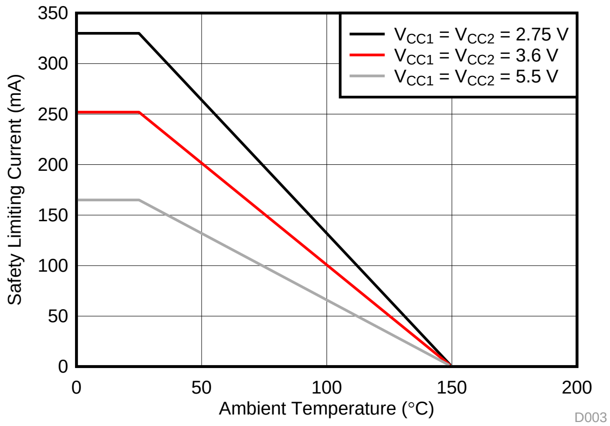


Figure 3. Thermal Derating Curve for Limiting Current per VDE for D-8 Package

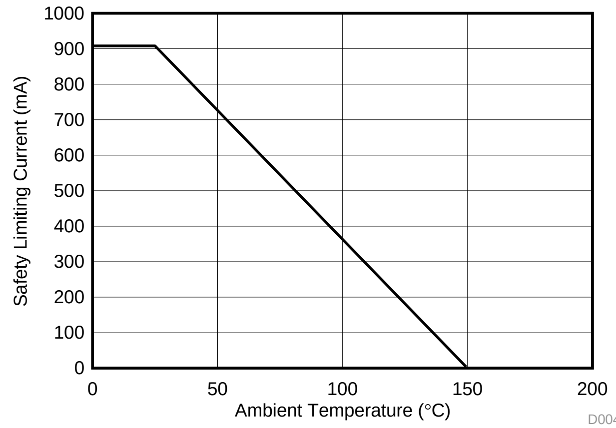
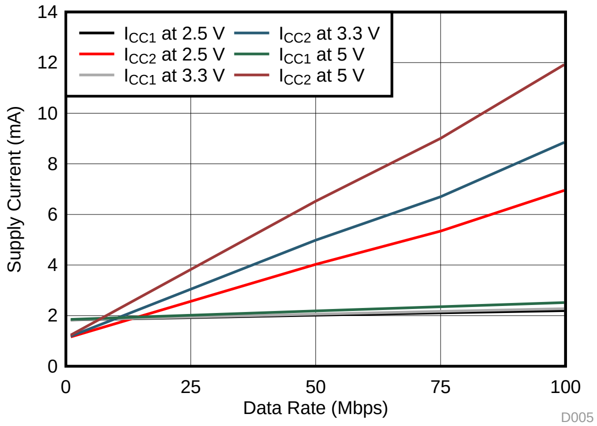


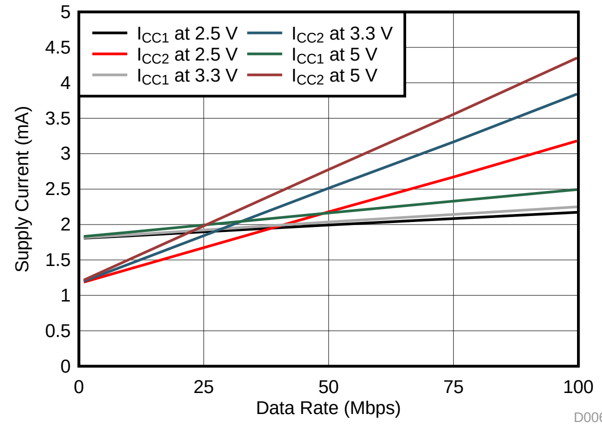
Figure 4. Thermal Derating Curve for Limiting Power per VDE for D-8 Package

6.19 Typical Characteristics



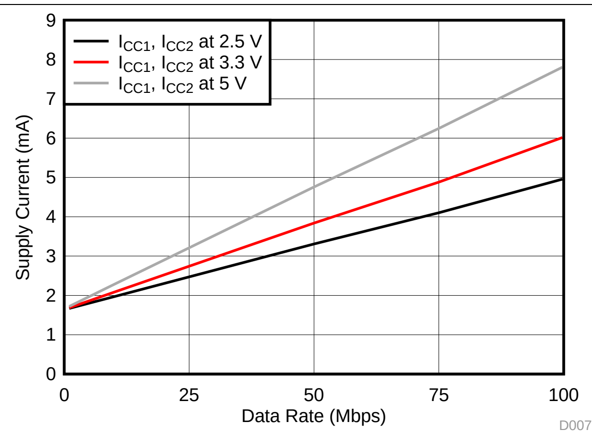
T_A = 25°C C_L = 15 pF

Figure 5. ISO7720 Supply Current vs Data Rate (With 15-pF Load)



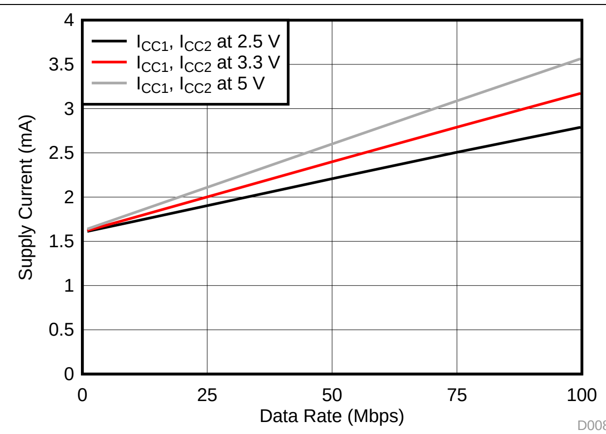
T_A = 25°C C_L = No Load

Figure 6. ISO7720 Supply Current vs Data Rate (With No Load)



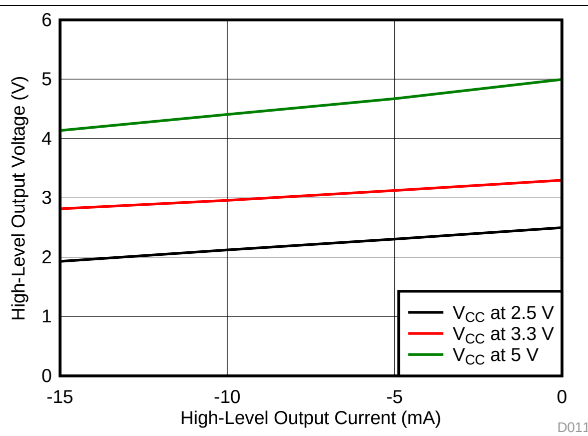
T_A = 25°C C_L = 15 pF

Figure 7. ISO7721 Supply Current vs Data Rate (With 15-pF Load)



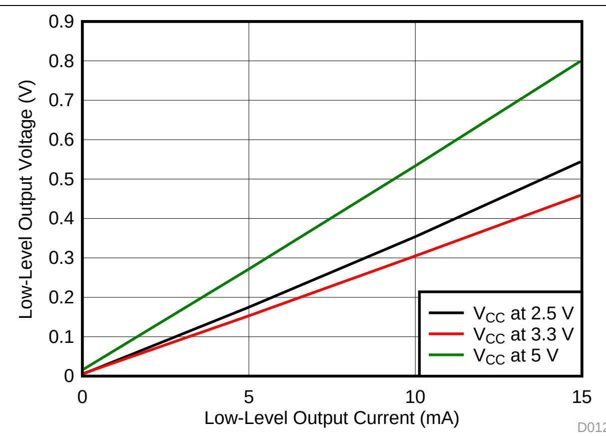
T_A = 25°C C_L = No Load

Figure 8. ISO7721 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 9. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 10. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

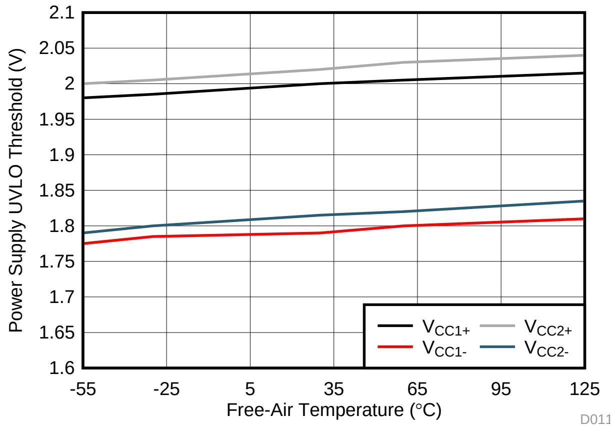


Figure 11. Power Supply Undervoltage Threshold vs Free-Air Temperature

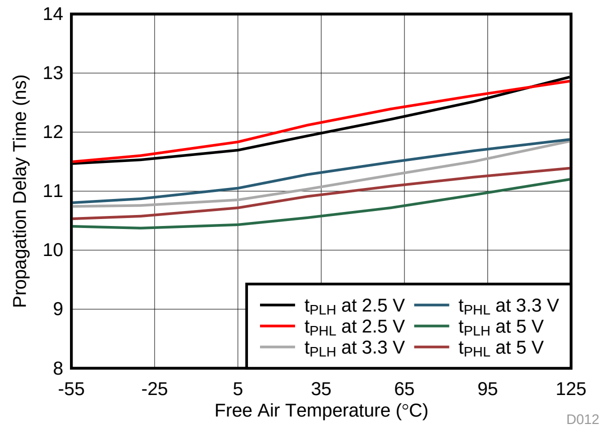
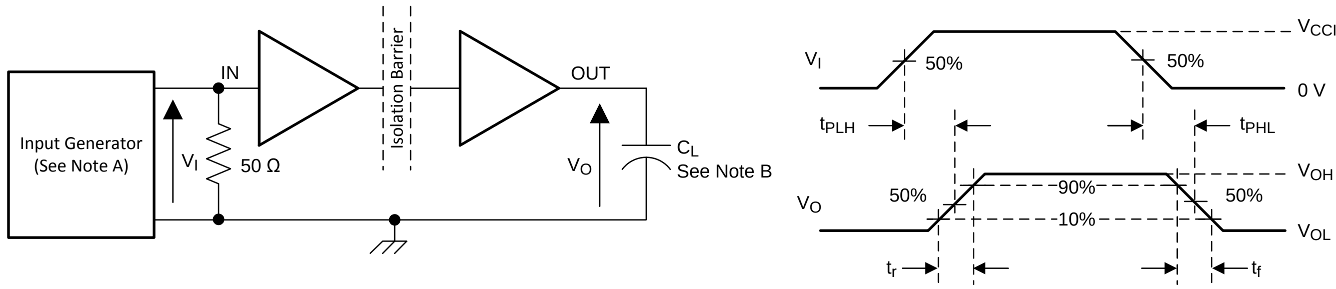


Figure 12. Propagation Delay Time vs Free-Air Temperature

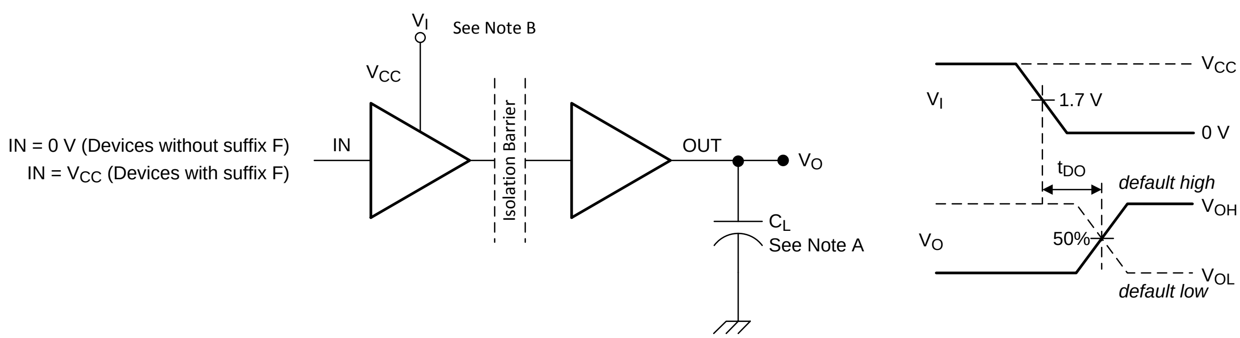
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

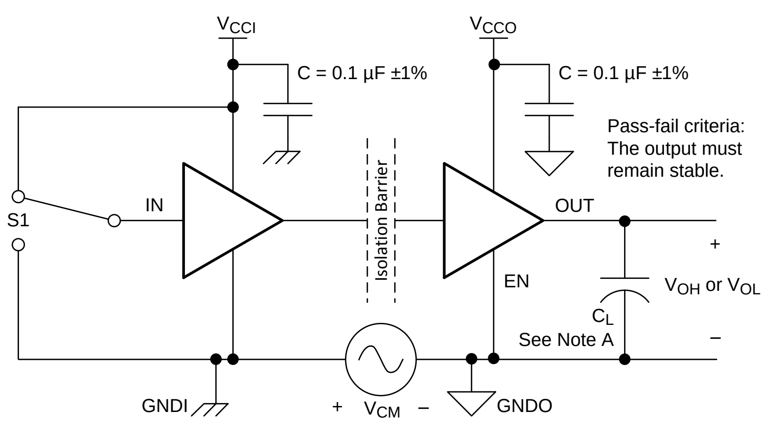
Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 14. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO772x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 16, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

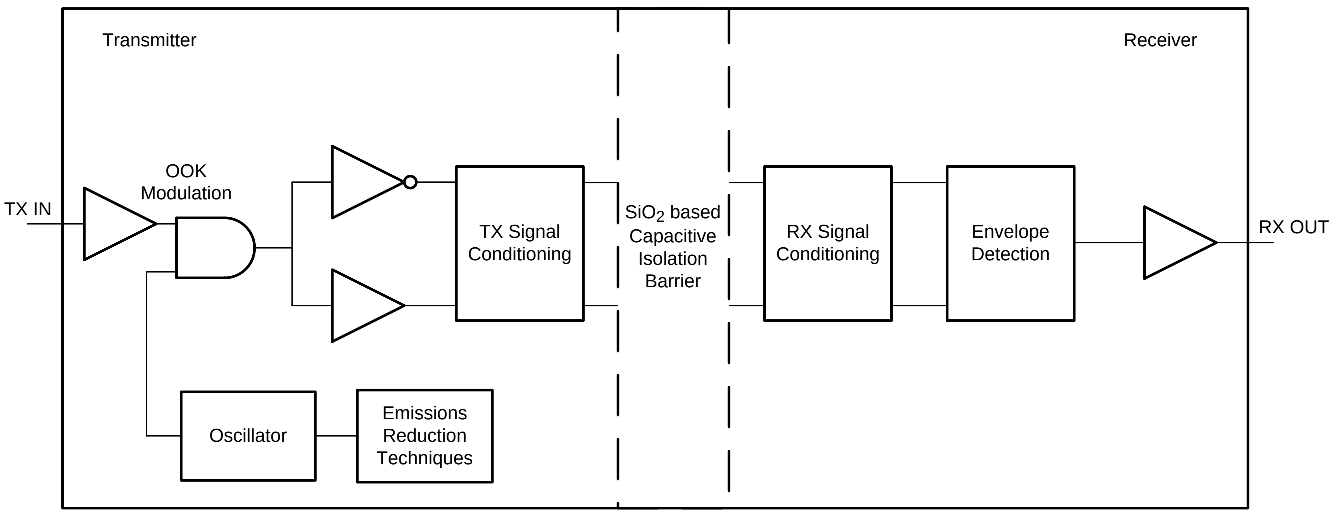


Figure 16. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 17 shows a conceptual detail of how the OOK scheme works.

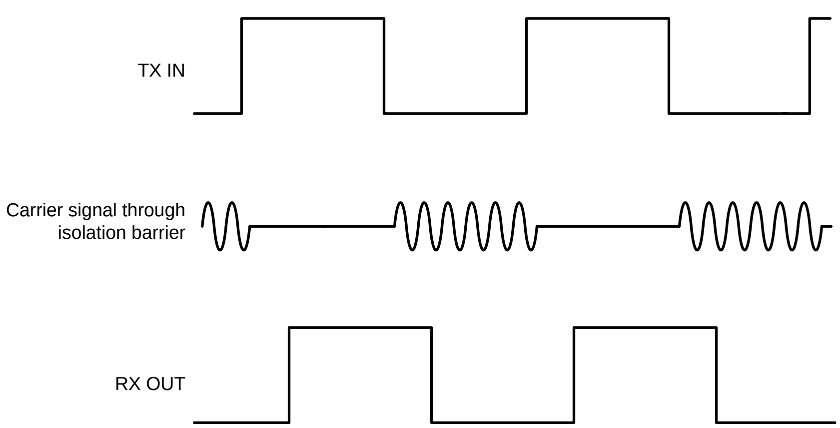


Figure 17. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO772x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 1 lists the device features of the ISO772x devices.

Table 1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION(1)
ISO7720	100 Mbps	2 Forward, 0 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7720F	100 Mbps	2 Forward, 0 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721	100 Mbps	1 Forward, 1 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721F	100 Mbps	1 Forward, 1 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO772x devices.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default high logic state. The default is *High* for ISO772x and *Low* for ISO772x with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is *High* for ISO772x and *Low* for ISO772x with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.7$ V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

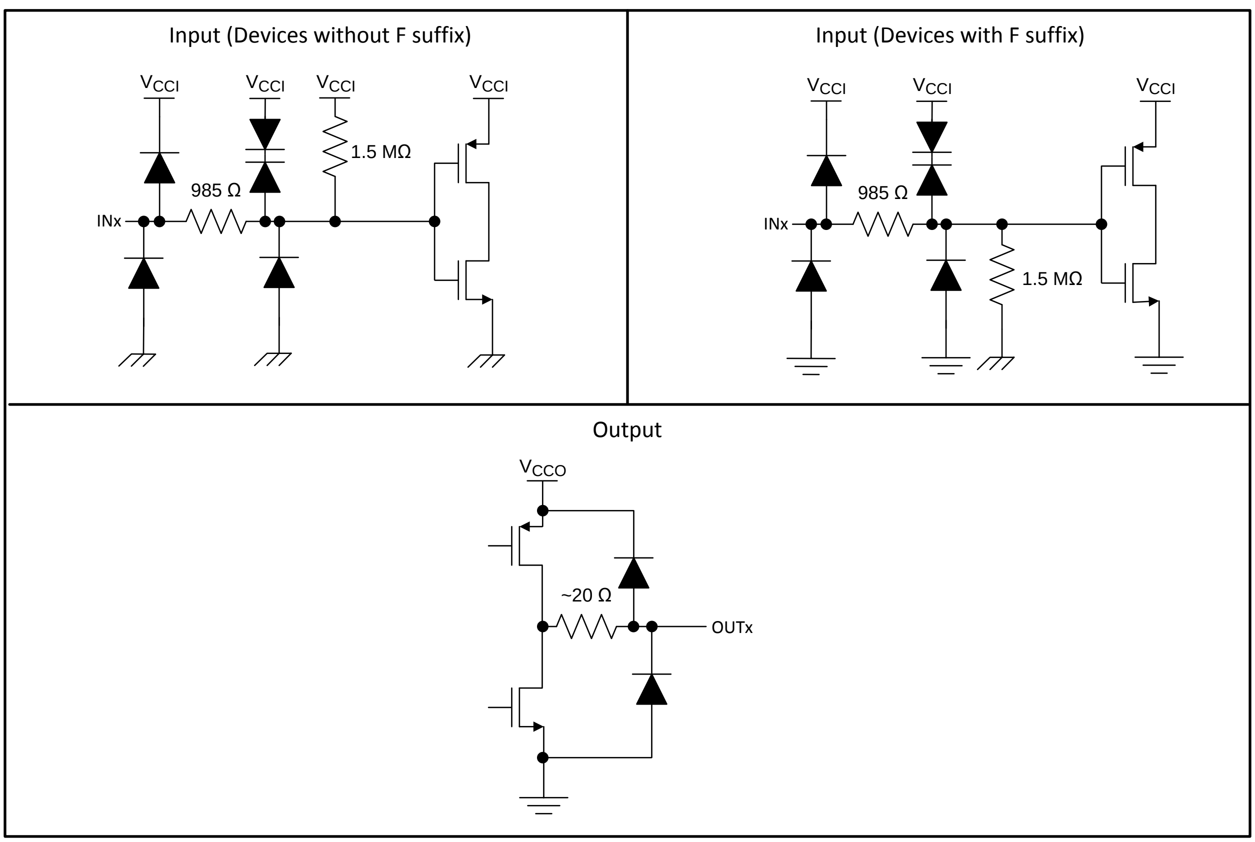


Figure 18. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO772x devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7721 device can be used with Texas Instruments' mixed signal microcontroller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-mA to 20-mA current loop.

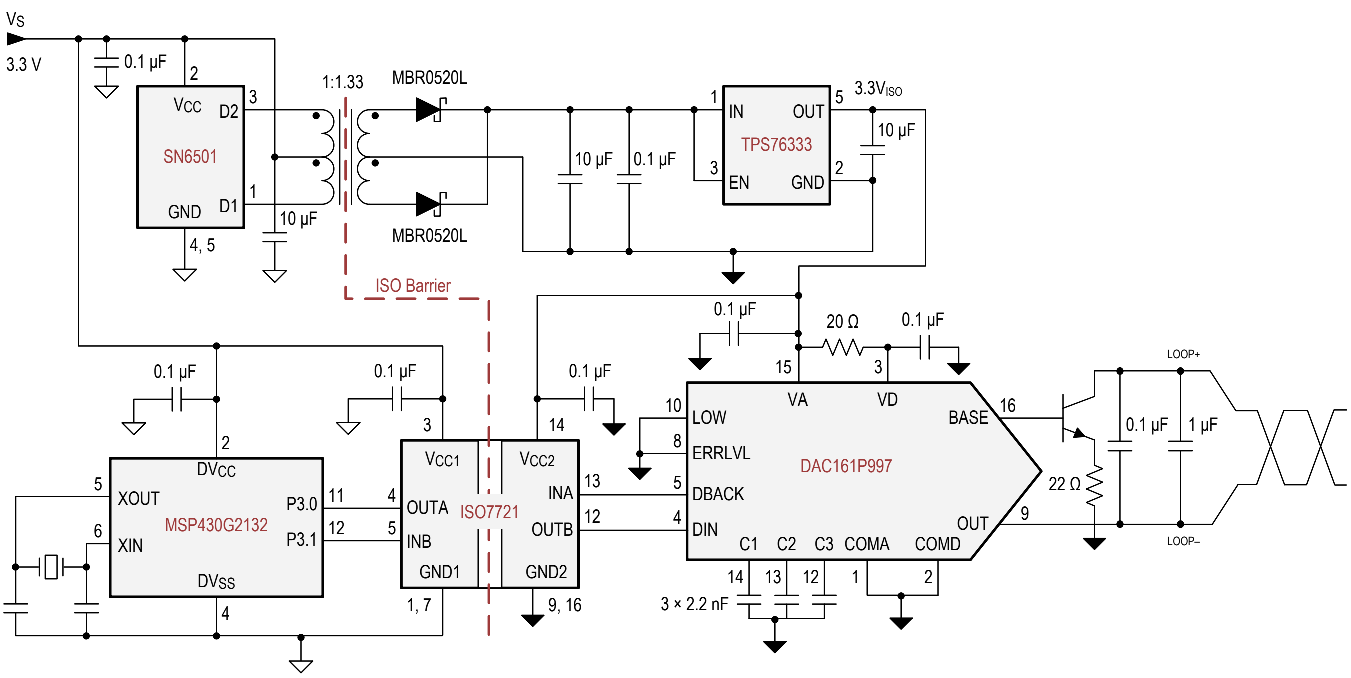


Figure 19. Isolated 4-mA to 20-mA Current Loop

Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x devices only require two external bypass capacitors to operate.

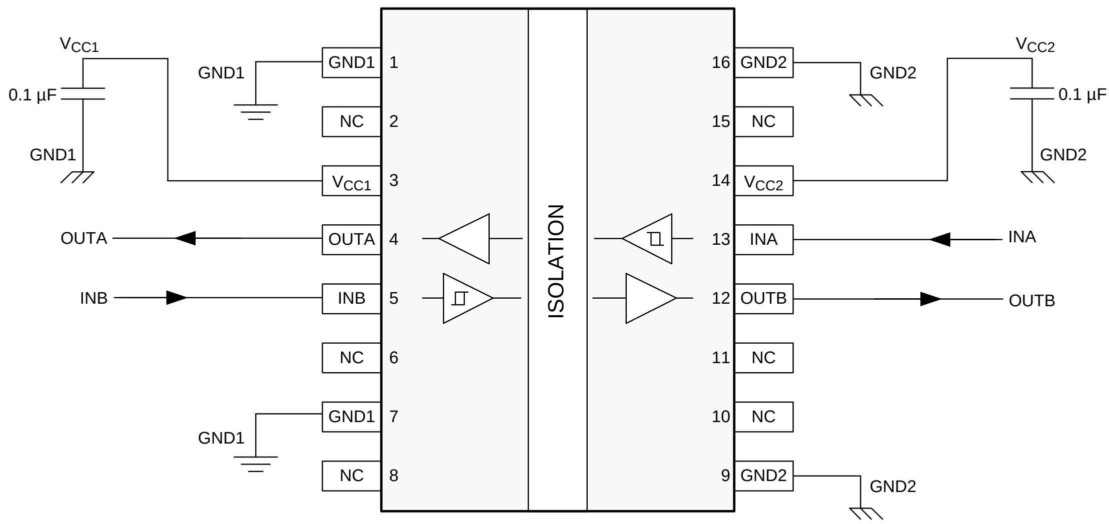


Figure 20. Typical ISO7721 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

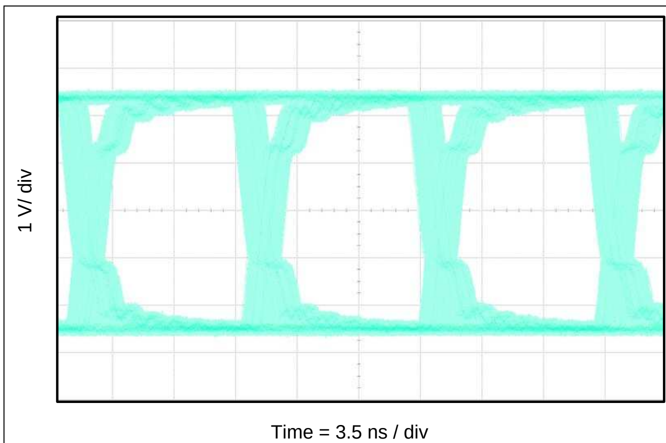


Figure 21. ISO7720 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

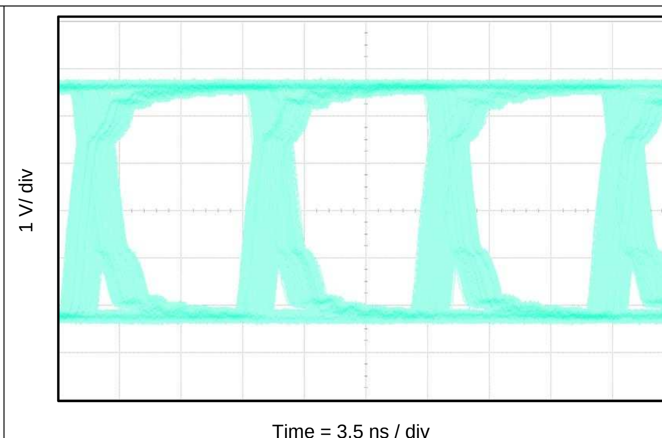


Figure 22. ISO7721 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

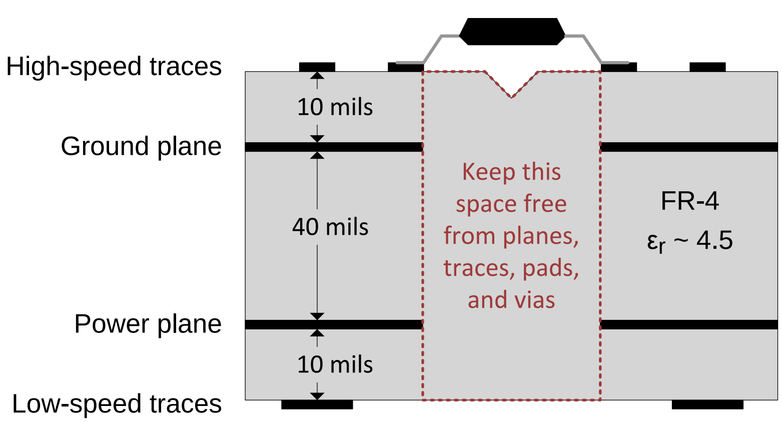


Figure 23. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《适用于 4mA 至 20mA 回路的 DAC161P997 单线 16 位 DAC》*
- *数字隔离器设计指南*
- *隔离相关术语*
- *《MSP430G2132 混合信号微控制器》*
- *《SN6501 用于隔离电源的变压器驱动器》*
- *《TPS76333 低功耗 150mA 低压降线性稳压器》*

12.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
ISO7720	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7721	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

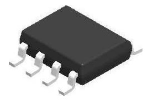
ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

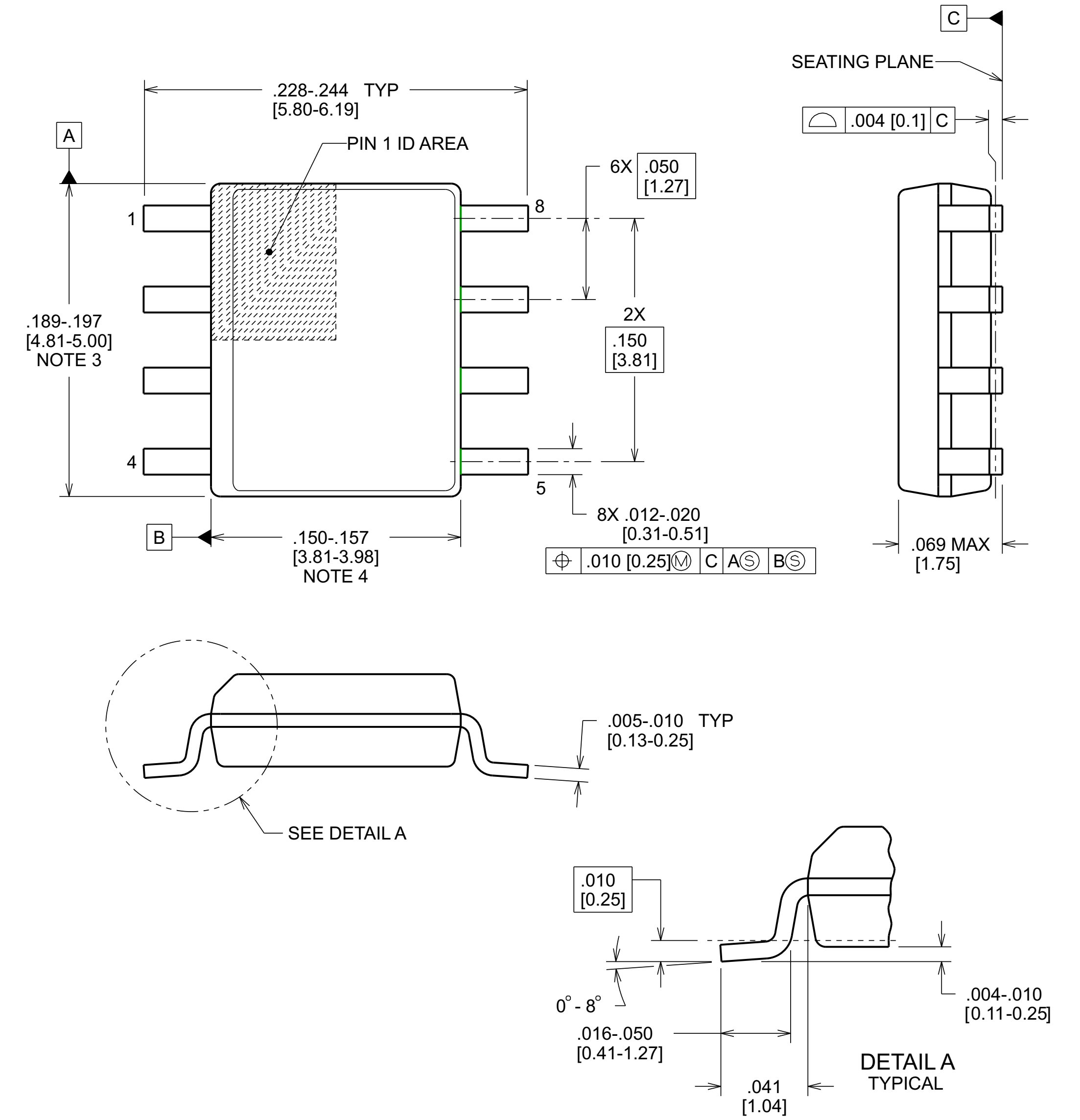


PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

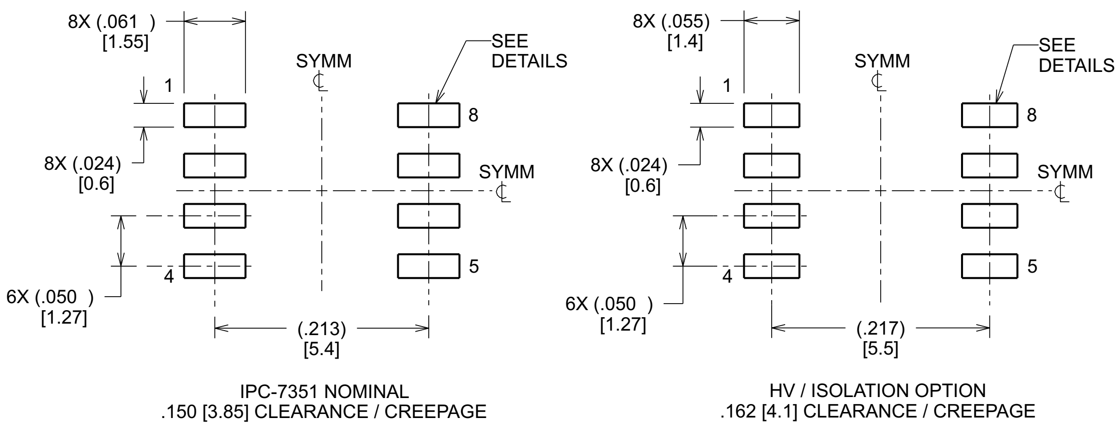
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

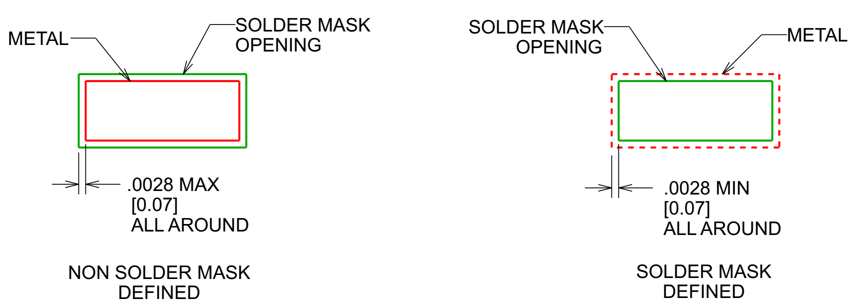
D0008B

SOIC - 1.75 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4221445/B 04/2014

NOTES: (continued)

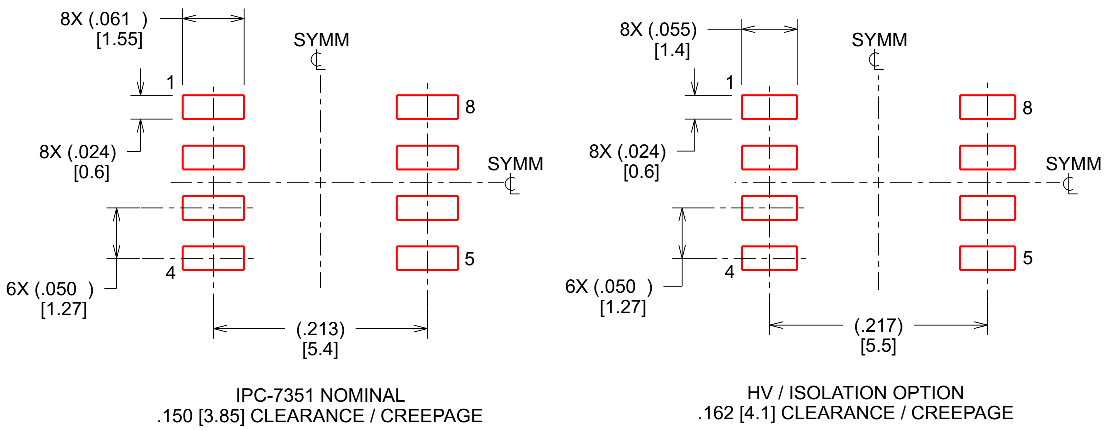
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/B 04/2014

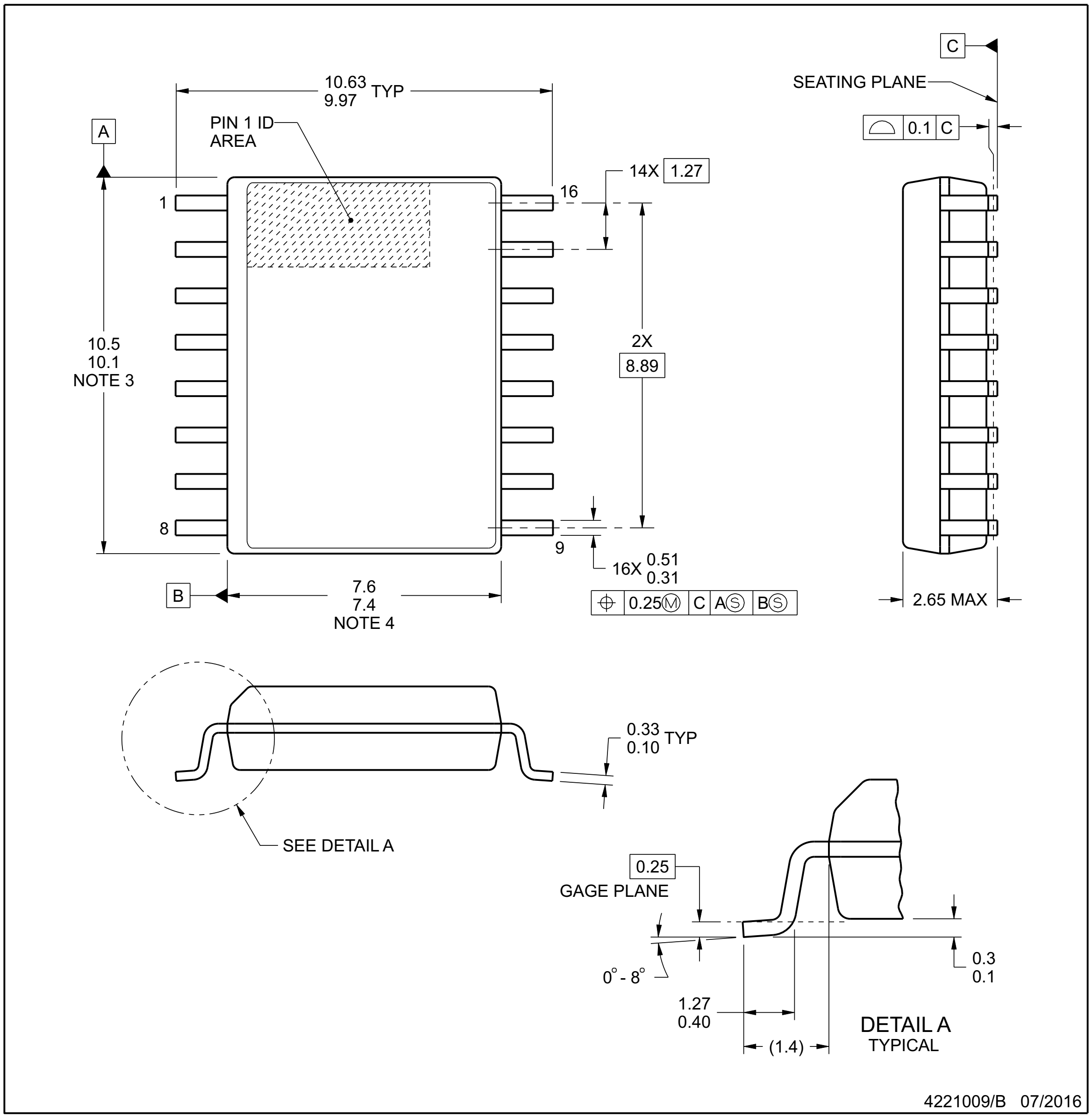
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DW0016B SOIC - 2.65 mm max height

SOIC



NOTES:

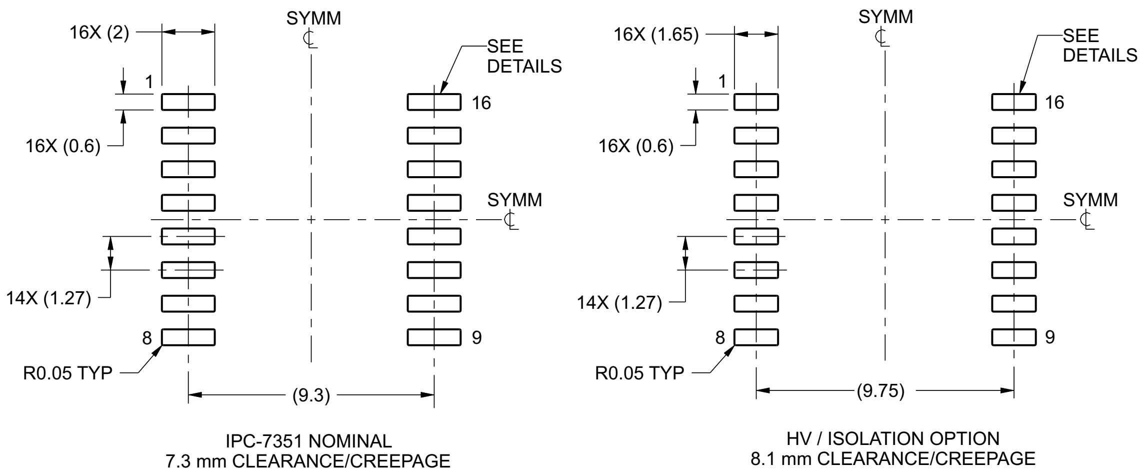
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

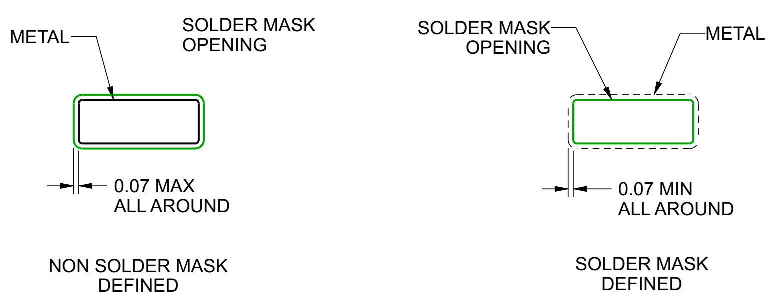
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

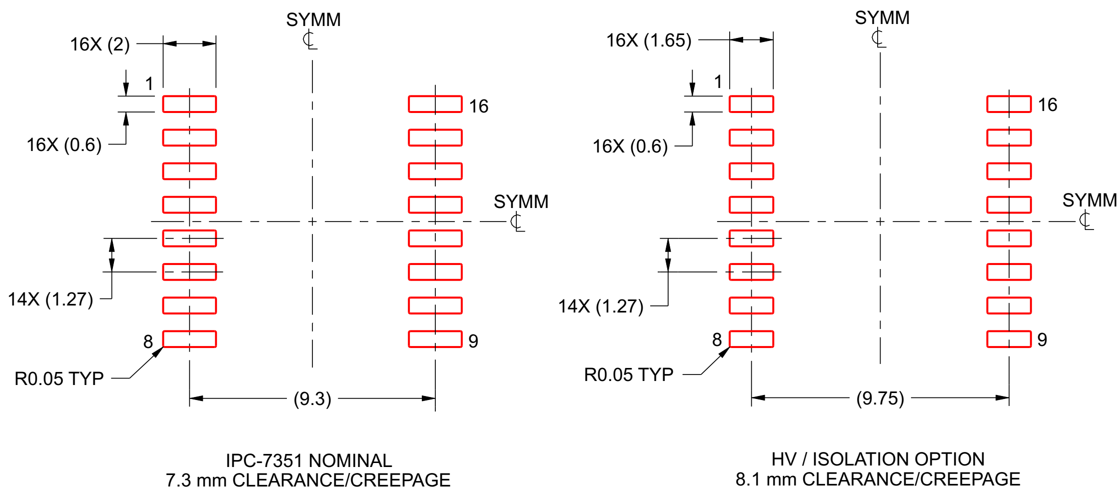
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7720D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7720FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7721D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples
ISO7721FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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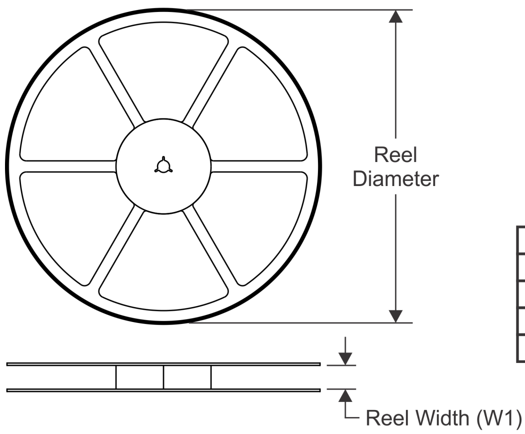
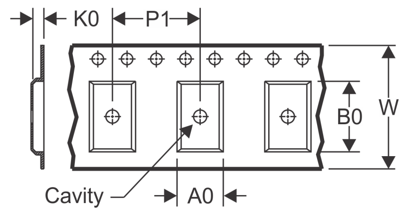
TAPE AND REEL INFORMATION

REEL DIMENSIONS

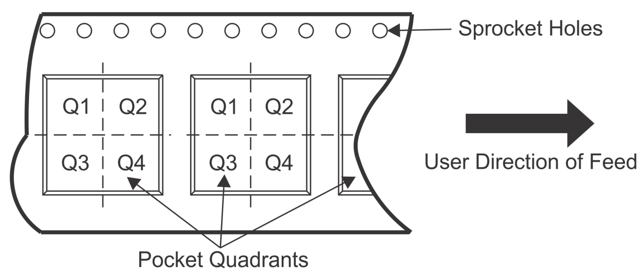


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

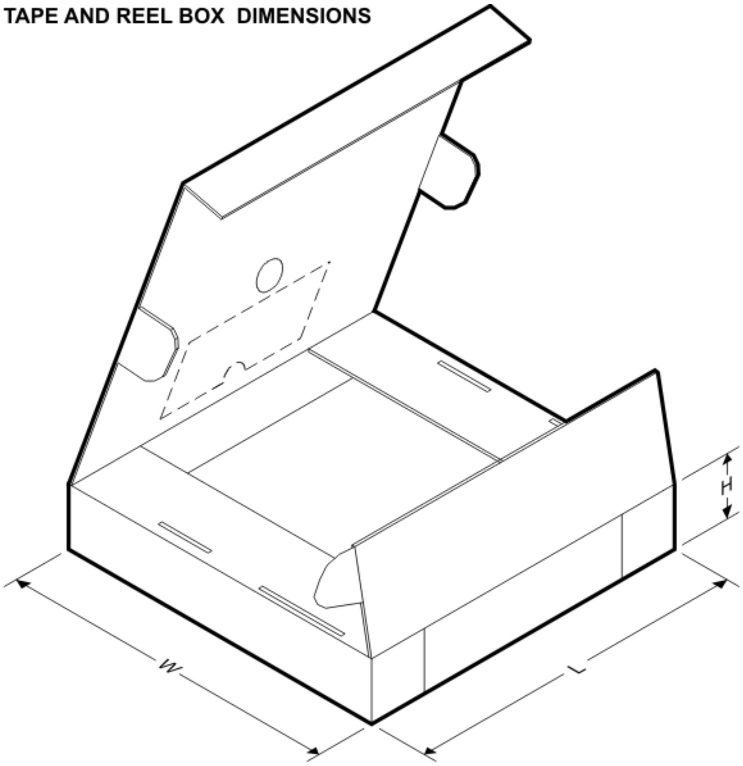
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7720DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7720DR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7720DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7720FDR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7720FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7721DR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7721DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7721FDR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7721FDWR	SOIC	DW	16	2000	367.0	367.0	38.0

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122