# TPS2H160-Q1 40V、160mΩ 双通道智能高侧开关

## 1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 1：环境运行温度范围为 -40°C 至 125°C
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H3A
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 具有丰富诊断功能的双通道 160mΩ 智能高侧开关
  - 版本 A：开漏状态输出
  - 版本 B：电流感测模拟输出
- 宽工作电压范围：3.4V 至 40V
- 超低待机电流：< 500nA
- 高精度电流感测：
  - > 25mA 负载下为 ±17%
- 可使用外部电阻调节电流限值，> 500mA 的负载条件下为 ±15%
- 保护：
  - 通过（内部或外部）电流限制实现接地短路保护
  - 具有锁闭选项的热关断以及热调节
  - 感性负载负电压钳位，已优化转换率
  - 失地保护和失电保护
- 诊断：
  - 过流和接地短路检测
  - 负载开路和电池短路检测
  - 用于实现快速中断的全局故障
- 16 引脚耐热增强型 PWP 封装

## 2 应用

- 双通道 LED 驱动器，灯泡驱动器
- 适用于子模块的双通道高侧开关
- 双通道高侧继电器，螺线管驱动器

## 3 说明

TPS2H160-Q1 系列是一款集成 160mΩ N 沟道金属氧化物半导体 (NMOS) 功率场效应晶体管 (FET) 的双通道智能高侧开关，配备全方位保护功能。

该器件具有丰富的诊断功能和高精度电流感测 功能，可对负载进行智能控制。

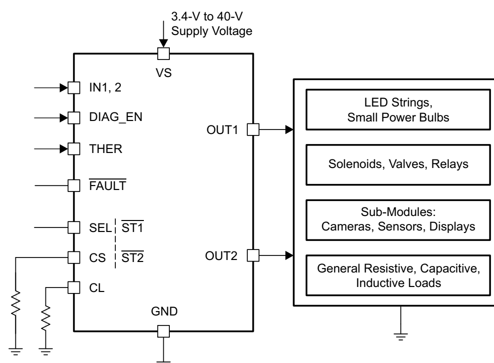
该器件可从外部调节电流限值以限制浪涌或过载电流，从而提升整个系统的可靠性。

器件信息(1)

| 器件型号 | 封装 | 通道 |
|---|---|---|
| TPS2H160-Q1 版本A | HTSSOP (16) | 2 |
| TPS2H160-Q1 版本B | | |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| **Changes from Original (December 2015) to Revision A** | **Page** |
| --- | --- |
| • 已将数据表状态由“产品预览”改为“量产数据” | 1 |


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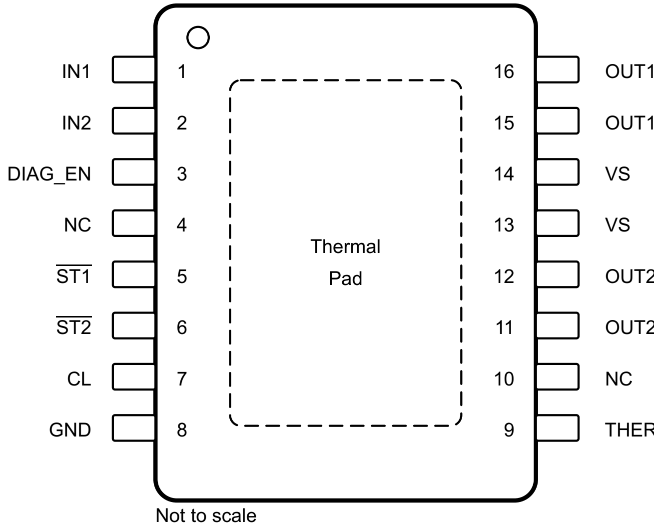
# 5 Device Comparison Table

| PART NUMBER | FAULT REPORTING MODE |
|---|---|
| TPS2H160-Q1 Version A | Open-drain digital output |
| TPS2H160-Q1 Version B | Current-sense analog output |

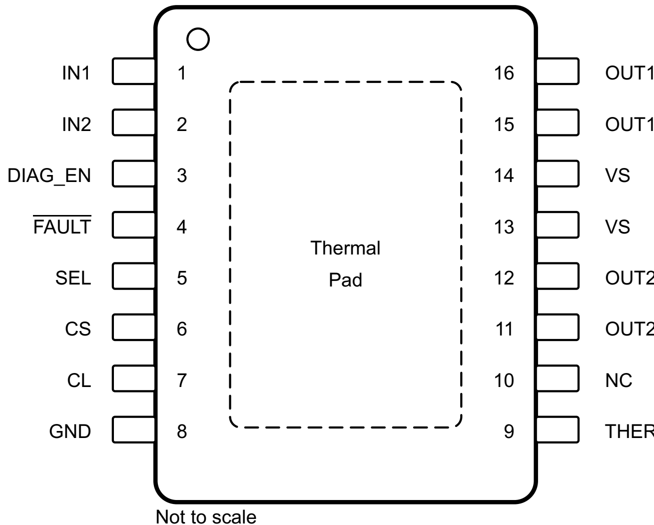
# 6 Pin Configuration and Functions

**PWP PowerPAD™ Package**
**16-Pin HTSSOP With Exposed Thermal Pad**
**TPS2H160-Q1 Version A Top View**




NC – No internal connection

**PWP PowerPAD Package**
**16-Pin HTSSOP With Exposed Thermal Pad**
**TPS2H160-Q1 Version B Top View**




NC – No internal connection

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### Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | VERSION A | VERSION B | | |
| CL | 7 | 7 | O | Adjustable current limit. Connect to device GND if external current limit is not used. |
| CS | — | 6 | O | Current-sense output |
| DIAG_EN | 3 | 3 | I | Enable-disable pin for diagnostics; internal pulldown |
| $\overline{\text{FAULT}}$ | — | 4 | O | Global fault report with open-drain structure, ORed logic for dual-channel fault conditions |
| GND | 8 | 8 | — | Ground pin |
| IN1 | 1 | 1 | I | Input control for channel 1 activation; internal pulldown |
| IN2 | 2 | 2 | I | Input control for channel 2 activation; internal pulldown |
| NC | 4, 10 | 10 | — | No internal connection |
| $\overline{\text{ST1}}$ | 5 | — | O | Open-drain diagnostic status output for channel 1 |
| $\overline{\text{ST2}}$ | 6 | — | O | Open-drain diagnostic status output for channel 2 |
| SEL | — | 5 | I | CS channel-selection bit; internal pulldown |
| THER | 9 | 9 | I | Thermal shutdown behavior control, latch off or auto-retry; internal pulldown |
| OUT1 | 15, 16 | 15, 16 | O | Output of the channel 1 high side-switch, connected to the load |
| OUT2 | 11, 12 | 11, 12 | O | Output of the channel 2 high side-switch, connected to the load |
| VS | 13, 14 | 13, 14 | I | Power supply |
| Thermal pad | — | — | — | Connect to device GND or leave floating |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | t < 400 ms | | 48 | V |
| Reverse polarity voltage(3) | | –36 | | V |
| Current on GND pin | t < 2 minutes | –100 | 250 | mA |
| Voltage on INx, DIAG_EN, SEL, and THER pins | | –0.3 | 7 | V |
| Current on INx, DIAG_EN, SEL, and THER pins | | –10 | — | mA |
| Voltage on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins | | –0.3 | 7 | V |
| Current on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins | | –30 | 10 | mA |
| Voltage on CS pin | | –2.7 | 7 | V |
| Current on CS pin | | — | 30 | mA |
| Voltage on CL pin | | –0.3 | 7 | V |
| Current on CL pin | | — | 6 | mA |
| Inductive load switch-off energy dissipation, single pulse, single channel(4) | | — | 40 | mJ |
| Operating junction temperature | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground plane.
(3) Reverse polarity condition: t < 60 s, reverse current < $I_{R(2)}$, $V_{INx}$ = 0 V, all channels reverse, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: $V_{VS}$ = 13.5 V, L = 8 mH, R = 0 Ω, $T_J$ = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 x 35-µm Cu. 600 $mm^2$ thermal pad copper area.


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## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1] | All pins except VS, OUTx, GND | ±4000 | V |
| | | | Pins VS, OUTx, GND | ±5000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±750 | |
| | | | Corner pins (1, 8, 9, and 16) | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{VS}$ | Supply operating voltage | 4 | 40 | V |
| | Voltage on INx, DIAG EN, SEL, and THER pins | 0 | 5 | V |
| | Voltage on $\overline{STx}$ and $\overline{FAULT}$ pins | 0 | 5 | V |
| | Nominal dc load current | 0 | 2.5 | A |
| $T_A$ | Operating ambient temperature | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | TPS2H160-Q1 | UNIT |
|---|---|---|---|
| | | PWP (HTSSOP) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 40.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 26.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 20.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

5 V < $V_{VS}$ < 40 V; −40°C < $T_J$ < 150°C, unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING VOLTAGE** | | | | | | |
| $V_{VS(nom)}$ | Nominal operating voltage | | 4 | | 40 | V |
| $V_{VS(uvr)}$ | Undervoltage turnon | $V_{VS}$ rises up | 3.5 | 3.7 | 4 | V |
| $V_{VS(uvf)}$ | Undervoltage shutdown | $V_{VS}$ falls down | 3 | 3.2 | 3.4 | V |
| $V_{(uv,hys)}$ | Undervoltage shutdown, hysteresis | | | 0.5 | | V |

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## Electrical Characteristics (continued)

5 V < $V_{VS}$ < 40 V; −40°C < $T_J$ < 150°C, unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING CURRENT** | | | | | | |
| $I_{(op)}$ | Nominal operating current(1) | $V_{VS}$ = 13.5 V, $V_{INx}$ = 5 V, $V_{DIAG_EN}$ = 0 V, $I_{OUTx}$ = 0.5 A, current limit = 2 A, all channels on | | | 7 | mA |
| $I_{(off)}$ | Standby current | $V_{VS}$ = 13.5 V, $V_{INx}$ = $V_{DIAG_EN}$ = $V_{CS}$ = $V_{CL}$ = $V_{OUTx}$ = THER = 0 V, $T_J$ = 25°C | | | 0.5 | μA |
| | | $V_{VS}$ = 13.5 V, $V_{INx}$ = $V_{DIAG_EN}$ = $V_{CS}$ = $V_{CL}$ = $V_{OUTx}$ = THER = 0 V, $T_J$ = 125°C | | | 5 | |
| $I_{(off,diag)}$ | Standby current with diagnostic enabled | $V_{VS}$ = 13.5 V, $V_{INx}$ = 0 V, $V_{DIAG_EN}$ = 5 V, $V_{VS}$ – $V_{OUTx}$ > $V_{(ol,off)}$, not in open-load mode | | | 6 | mA |
| $t_{(off,diag)}$ | Standby mode deglitch time(1) | IN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode. | 10 | 12.5 | 15 | ms |
| $I_{lkg(out)}$ | Output leakage current in off-state | $V_{VS}$ = 13.5 V, $V_{INx}$ = $V_{DIAG_EN}$ = $V_{OUTx}$ = 0 | | | 0.5 | μA |
| **POWER STAGE** | | | | | | |
| $r_{DS(on)}$ | On-state resistance(1) | $V_{VS}$ ≥ 3.5 V, $T_J$ = 25°C | | 155 | | mΩ |
| | | $V_{VS}$ ≥ 3.5 V, $T_J$ = 150°C | | | 280 | |
| $I_{CL(int)}$ | Internal current limit | Internal current limit value, CL pin connected to GND | 9 | | 15 | A |
| $I_{CL(TSD)}$ | Current limit during thermal shutdown(1) | Internal current limit value under thermal shutdown | | 6.8 | | A |
| | | External current limit value under thermal shutdown. The percentage of the external current limit setting value | | 60% | | |
| $V_{DS(clamp)}$ | Drain-to-source internal clamp voltage | | 45 | | 65 | V |
| **OUTPUT DIODE CHARACTERISTICS** | | | | | | |
| $V_F$ | Drain−source diode voltage | IN = 0, $I_{OUTx}$ = −0.15 A. | 0.3 | 0.7 | 0.9 | V |
| $I_{R(1)}$, $I_{R(2)}$ | Continuous reverse current from source to drain(1) | t < 60 s, $V_{INx}$ = 0 V, $T_J$ = 25°C, single channel reversed, short-to-battery condition | | 2.5 | | A |
| | | t < 60 s, $V_{INx}$ = 0 V, GND pin 1-kΩ resistor in parallel with diode. $T_J$ = 25°C. Reverse-polarity condition, all channels reversed | | 2 | | |
| **LOGIC INPUT (INx, DIAG_EN, SEL, THER)** | | | | | | |
| $V_{IH}$ | Logic high-level voltage | | 2 | | | V |
| $V_{IL}$ | Logic low-level voltage | | | | 0.8 | V |
| $R_{(logic,pd)}$ | Logic-pin pulldown resistor | INx, SEL, THER, $V_{INx}$ = $V_{SEL}$ = $V_{THER}$ = 5 V | 100 | 175 | 230 | kΩ |
| | | DIAG_EN. $V_{VS}$ = $V_{DIAG_EN}$ = 5 V | 150 | 275 | 350 | |
| **DIAGNOSTICS** | | | | | | |
| $I_{lkg(GND_loss)}$ | Output leakage current under GND loss condition | | | | 100 | μA |
| $V_{(ol,off)}$ | Open-load detection threshold | IN = 0 V, when $V_{VS}$ – $V_{OUTx}$ < $V_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state | 1.6 | | 2.6 | V |
| $t_{d(ol,off)}$ | Open-load detection threshold deglitch time (see Figure 3) | IN = 0 V, when $V_{VS}$ – $V_{OUTx}$ < $V_{(ol,off)}$ , duration longer than $t_{(ol,off)}$, then open load is detected, off state | 400 | 600 | 800 | μs |
| $I_{(ol,off)}$ | Off-state output sink current | $V_{INx}$ = 0 V, $V_{DIAG_EN}$ = 5 V, $V_{VS}$ = $V_{OUTx}$ = 13.5 V, $T_J$ = 125°C, open load | –75 | | | μA |
| $V_{OL(STx)}$ | Status low-output voltage | $I_{STx}$ = 2 mA, version A only | | | 0.2 | V |
| $V_{OL(FAULT)}$ | Fault low-output voltage | $I_{FAULT}$ = 2 mA, version B only | | | 0.2 | V |
| $t_{CL(deg)}$ | Deglitch time when current limit occurs(1) | $V_{INx}$ = $V_{DIAG_EN}$ = 5 V, the deglitch time from current limit toggling to $\overline{FAULT}$, $\overline{STx}$, CS report. | 80 | | 180 | μs |
| $T_{(SD)}$ | Thermal shutdown threshold(1) | | 160 | 175 | | °C |
| $T_{(SD,rst)}$ | Thermal shutdown status reset threshold(1) | | | 155 | | °C |
| $T_{(SW)}$ | Thermal swing shutdown threshold(1) | | | 60 | | °C |
| $T_{(hys)}$ | Hysteresis for resetting the thermal shutdown or thermal swing(1) | | | 10 | | °C |

(1) Value specified by design, not subject to production test


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## Electrical Characteristics (continued)

5 V < $V_{VS}$ < 40 V; −40°C < $T_J$ < 150°C, unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT SENSE (Version B) AND CURRENT LIMIT** | | | | | | |
| $K_{(CS)}$ | Current-sense ratio | | | 290 | | |
| $K_{(CL)}$ | Current-limit ratio | | | 2500 | | |
| $V_{CL(th)}$ | Current limit internal threshold(1) | | | 0.8 | | V |
| $dK_{(CS)}$ / $K_{(CS)}$ | Current-sense accuracy, ($I_{CS}$ × $K_{(CS)}$ – $I_{OUTx}$) /$I_{OUTx}$ × 100 | $V_{VS}$ = 13.5 V, $I_{OUTx}$ ≥ 5 mA | –85% | | 85% | |
| | | $V_{VS}$ = 13.5 V, $I_{OUTx}$ ≥ 25 mA | –17% | | 17% | |
| | | $V_{VS}$ = 13.5 V, $I_{OUTx}$ ≥ 50 mA | –8% | | 8% | |
| | | $V_{VS}$ = 13.5 V, $I_{OUTx}$ ≥ 100 mA | –4% | | 4% | |
| | | $V_{VS}$ = 13.5 V, $I_{OUTx}$ ≥ 0.5 A | –3% | | 3% | |
| $dK_{(CL)}$ / $K_{(CL)}$ | External current limit accuracy, ($I_{OUTx}$ – $I_{CL}$ × $K_{(CL)}$) × 100 / ($I_{CL}$ × $K_{(CL)}$) | $V_{VS}$ = 13.5 V, $I_{(limit)}$ ≥ 0.25 A | –20% | | 20% | |
| | | $V_{VS}$ = 13.5 V, 0.5 A ≤ $I_{(limit)}$ ≤ 7 A | –15% | | 15% | |
| $V_{CS(lin)}$ | Current-sense voltage linear range(1) | $V_{VS}$ ≥ 6.5 V | 0 | | 4 | V |
| | | 5 V ≤ $V_{VS}$ < 6.5 V | 0 | | $V_{VS}$ – 2.5 | |
| $I_{OUTx(lin)}$ | Output-current linear range(1) | $V_{VS}$ ≥ 6.5 V, $V_{CS(lin)}$ ≤ 4 V | 0 | | 2.5 | A |
| | | 5 V ≤ $V_{VS}$ < 6.5 V, $V_{CS(lin)}$ ≤ $V_{VS}$ – 2.5 V | 0 | | 2.5 | |
| $V_{CS(H)}$ | Current sense pin output voltage(1) | $V_{VS}$ ≥ 7 V, fault mode | 4.5 | | 6.5 | V |
| | | 5 V ≤ $V_{VS}$ < 7 V, fault mode | Min($V_{VS}$ – 2, 4.5) | | 6.5 | V |
| $I_{CS(H)}$ | Current-sense pin output current | $V_{CS}$ = 4.5 V, $V_{VS}$ = 13.5 V | 15 | | | mA |
| $I_{lkg(CS)}$ | Current-sense leakage current in disabled mode | $V_{DIAG_EN}$ = 0 V, $T_J$ =125ºC | | | 0.5 | µA |

## 7.6 Switching Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Delay time, $V_{OUTx}$ 10% after $V_{INx}$↑ (See Figure 1.) | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A, IN rising edge to 10% of $V_{OUTx}$ | 20 | 50 | 90 | µs |
| $t_{d(off)}$ | Delay time, $V_{OUTx}$ 90% after $V_{INx}$↓ (See Figure 1.) | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A, IN falling edge to 90% of $V_{OUTx}$ | 20 | 50 | 90 | µs |
| dV/dt(on) | Turnon slew rate | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A, $V_{OUTx}$ from 10% to 90% | 0.1 | 0.3 | 0.55 | V/µs |
| dV/dt(off) | Turnoff slew rate | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A, $V_{OUTx}$ from 90% to 10% | 0.1 | 0.35 | 0.55 | V/µs |
| $t_{d(match)}$ | $t_{d(rise)}$ – $t_{d(fall)}$ (See Figure 1.) | $V_{VS}$ = 13.5 V, $I_L$ = 0.5A. $t_{d,\ rise}$ is the IN rising edge to $V_{OUTx}$ = 90%.<br>$t_{d(fall)}$ is the IN falling edge to $V_{OUTx}$ = 10%. | –50 | | 50 | µs |
| **CURRENT-SENSE CHARACTERISTICS (See Figure 2.)** | | | | | | |
| $t_{CS(off1)}$ | CS settling time from DIAG_EN disabled(1) | $V_{VS}$ = 13.5 V, $V_{INx}$ = 5 V, $I_{OUTx}$ = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of $V_{CS}$. | | | 20 | µs |
| $t_{CS(on1)}$ | CS settling time from DIAG_EN enabled(1) | $V_{VS}$ = 13.5 V, $V_{INx}$ = 5 V, $I_{OUTx}$ = 0.5 A. current limit is 2 A. DIAG_EN rising edge to 90% of $V_{CS}$. | | | 20 | µs |
| $t_{CS(off2)}$ | CS settling time from IN falling edge | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A. current limit = 2 A. IN falling edge to 10% of $V_{CS}$ | 20 | | 100 | µs |
| $t_{CS(on2)}$ | CS settling time from IN rising edge | $V_{VS}$ = 13.5 V, $V_{DIAG_EN}$ = 5 V, $I_{OUTx}$ = 0.5 A. current limit = 2 A. IN rising edge to 90% of $V_{CS}$ | 50 | | 150 | µs |
| $t_{SEL}$ | Multi-sense transition delay from channel to channel | $V_{DIAG_EN}$ = 5 V, current sense output delay when multi-sense pin SEL transitions from channel to channel | | | 50 | µs |

(1) Value specified by design, not subject to production test

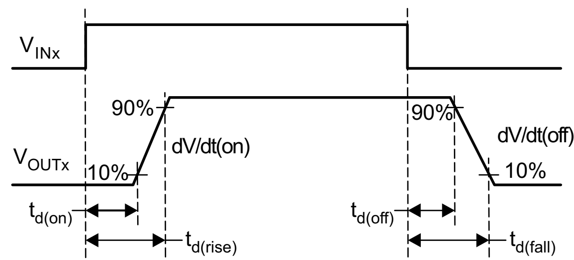


**Figure 1. Output Delay Characteristics**

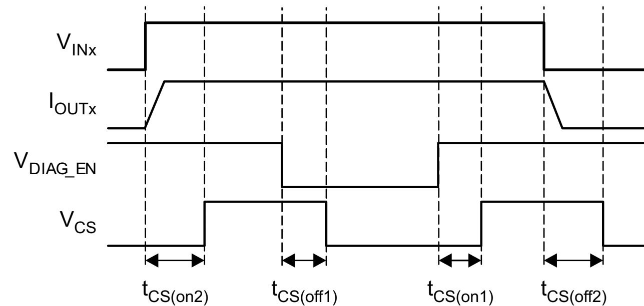


**Figure 2. CS Delay Characteristics**

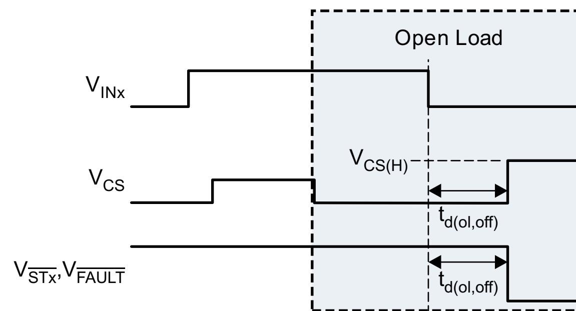


**Figure 3. Open-Load Blanking-Time Characteristics**

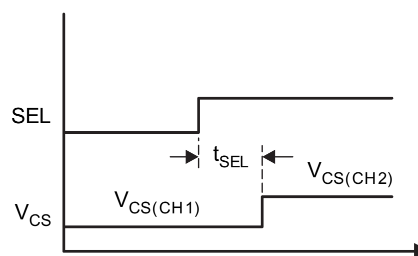


**Figure 4. Multi-Sense Transition Delay**


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## 7.7 Typical Characteristics

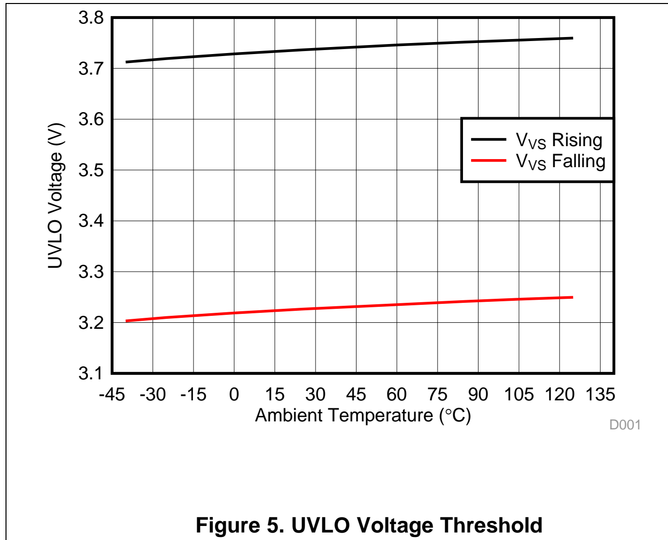


Figure 5. UVLO Voltage Threshold

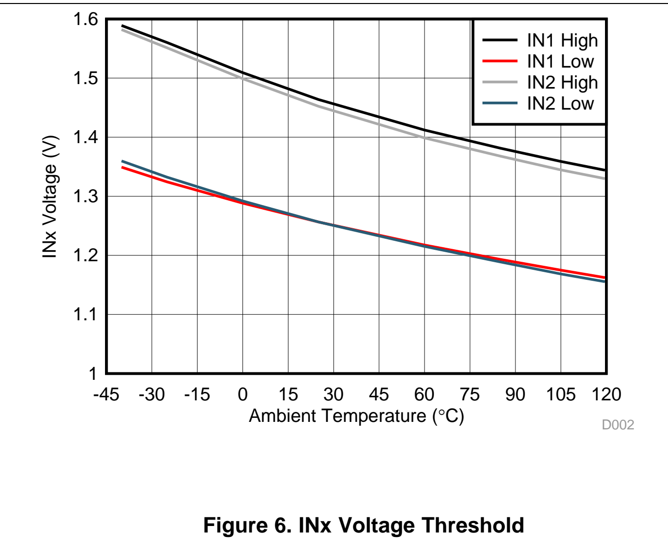


Figure 6. INx Voltage Threshold

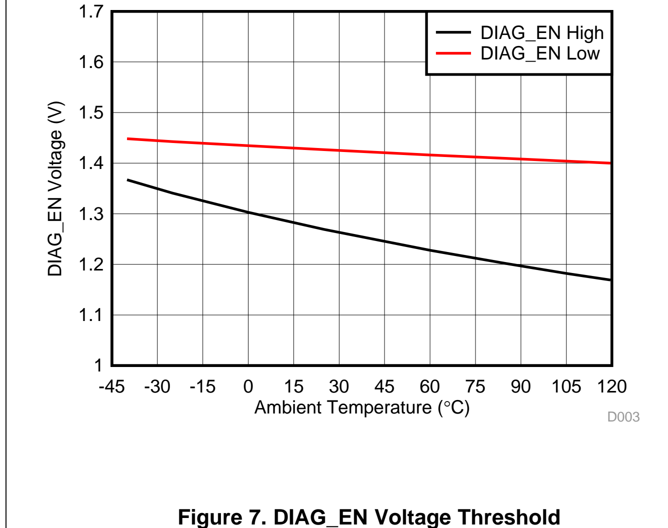


Figure 7. DIAG_EN Voltage Threshold

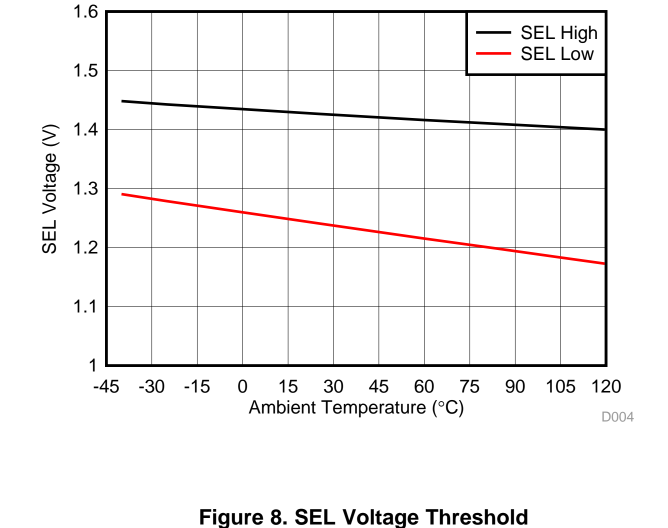


Figure 8. SEL Voltage Threshold

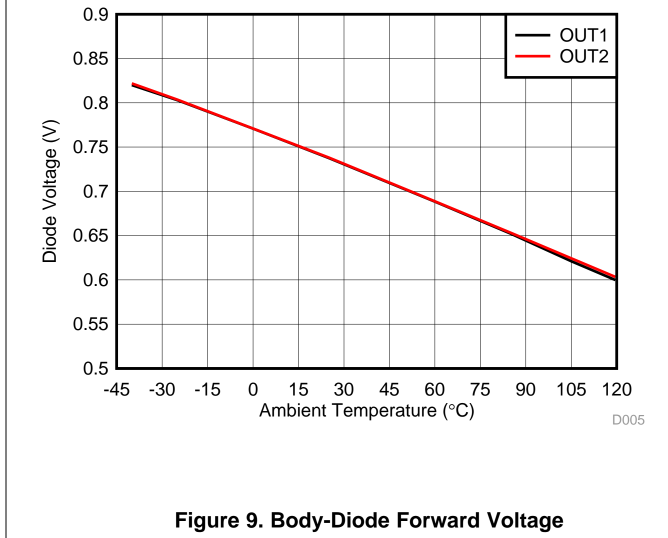


Figure 9. Body-Diode Forward Voltage

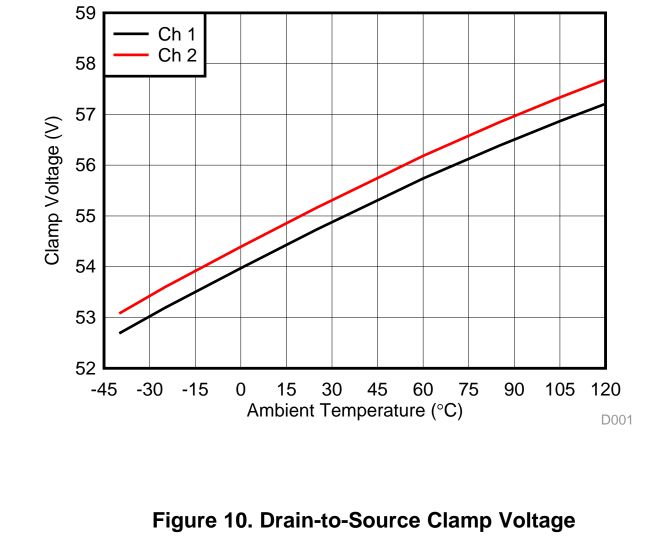


Figure 10. Drain-to-Source Clamp Voltage

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## Typical Characteristics (continued)

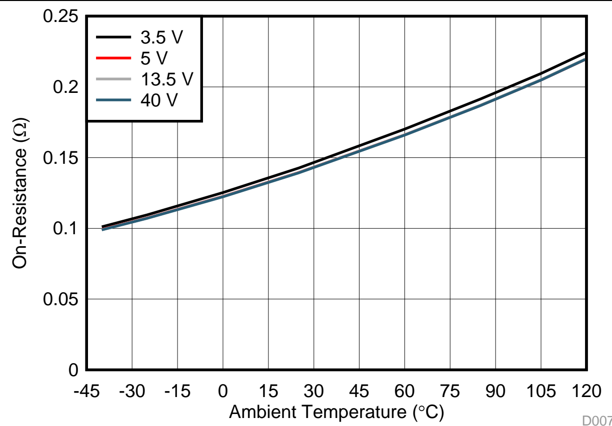


**Figure 11. Channel-1 FET On-Resistance**

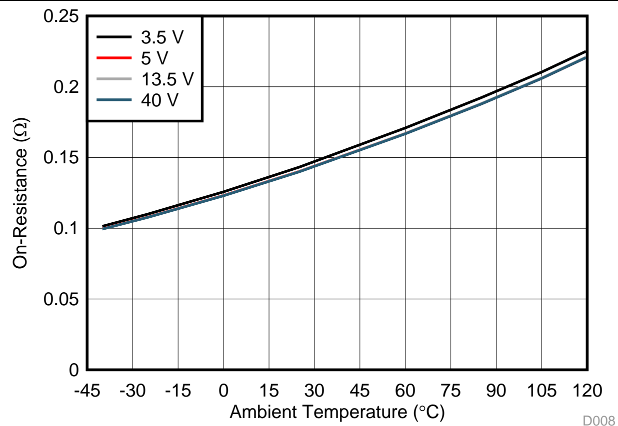


**Figure 12. Channel-2 FET On-Resistance**

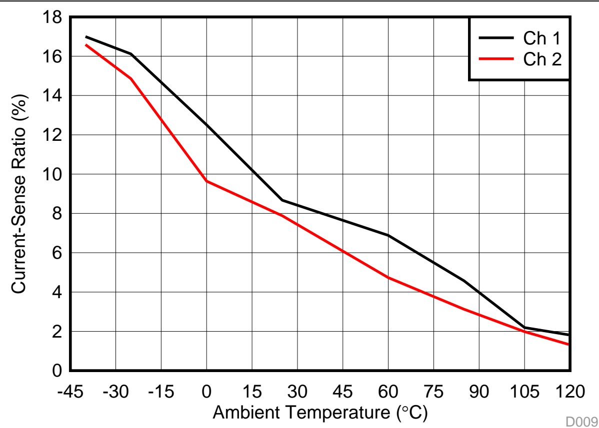


**Figure 13. Current-Sense Ratio at 5 mA**

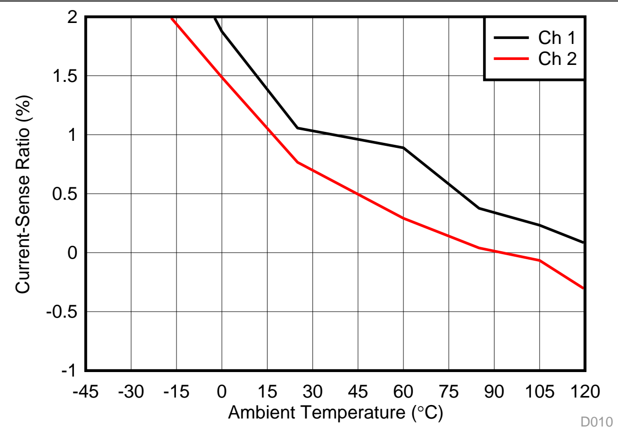


**Figure 14. Current-Sense Ratio at 25 mA**

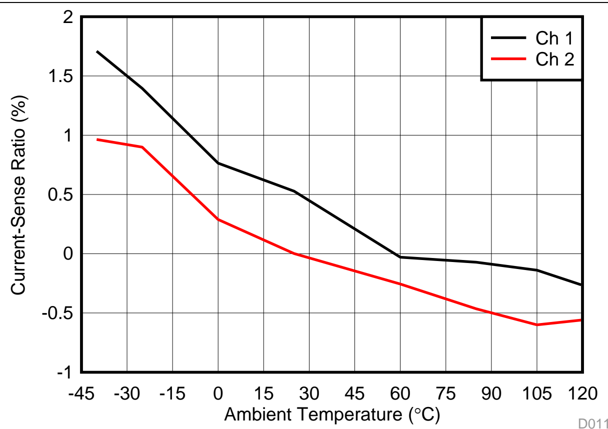


**Figure 15. Current-Sense Ratio at 50 mA**

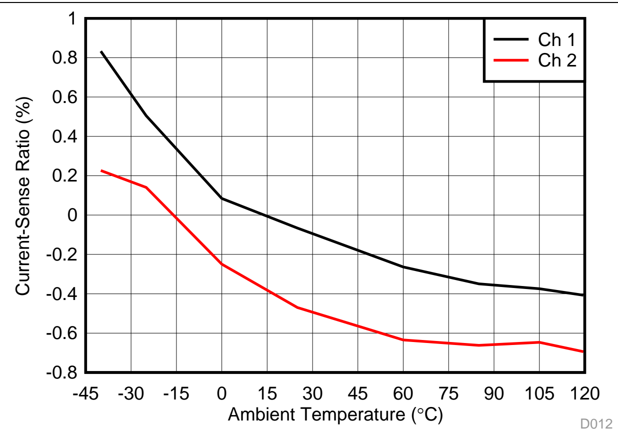


**Figure 16. Current-Sense Ratio at 100 mA**


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## Typical Characteristics (continued)

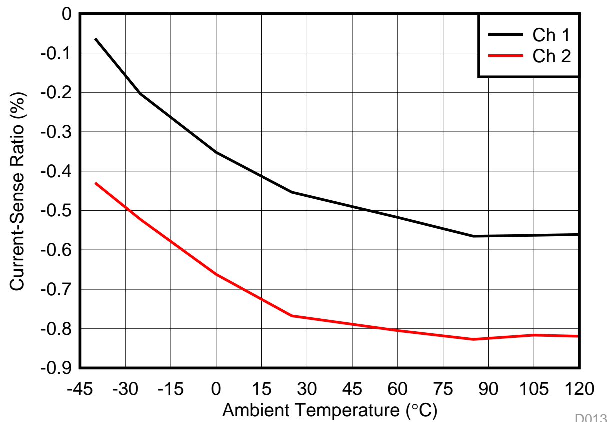


Figure 17. Current-Sense Ratio at 500 mA

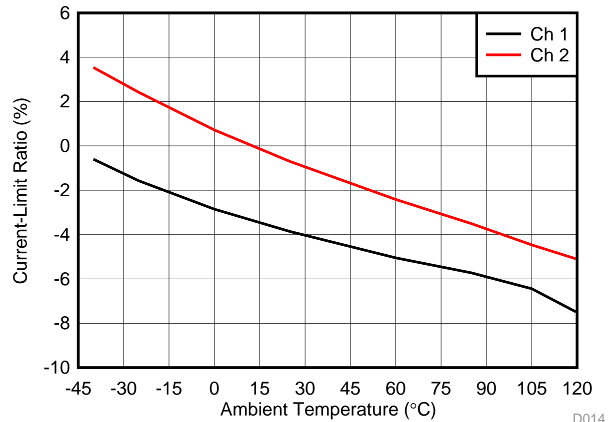


Figure 18. Current-Limit Ratio at 0.25 A

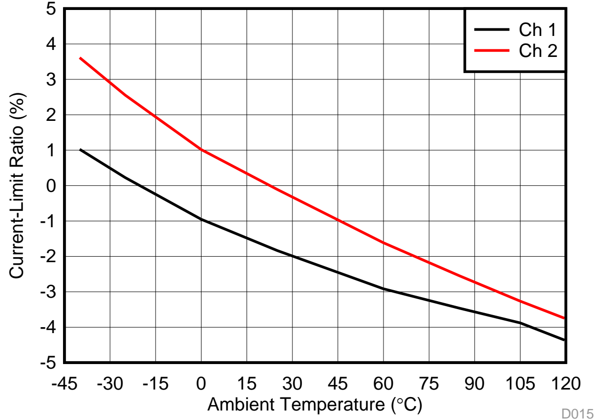


Figure 19. Current-Limit Ratio at 0.5 A

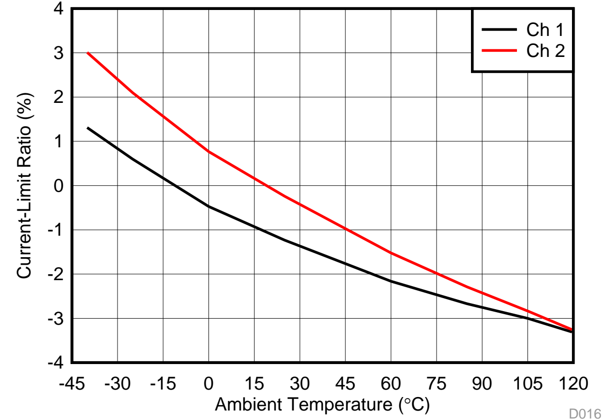


Figure 20. Current-Limit Ratio at 1 A

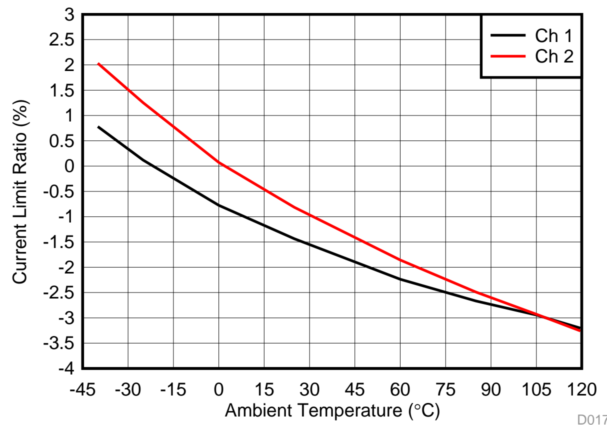


Figure 21. Current-Limit Ratio at 2 A

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# 8 Detailed Description

## 8.1 Overview

The TPS2H160-Q1 device is a smart high-side switch, with internal charge pump and dual-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the $\overline{STx}$ pins together.

For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / $K_{(CS)}$ of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. $K_{(CS)}$ is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS(H)}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS2H160-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.


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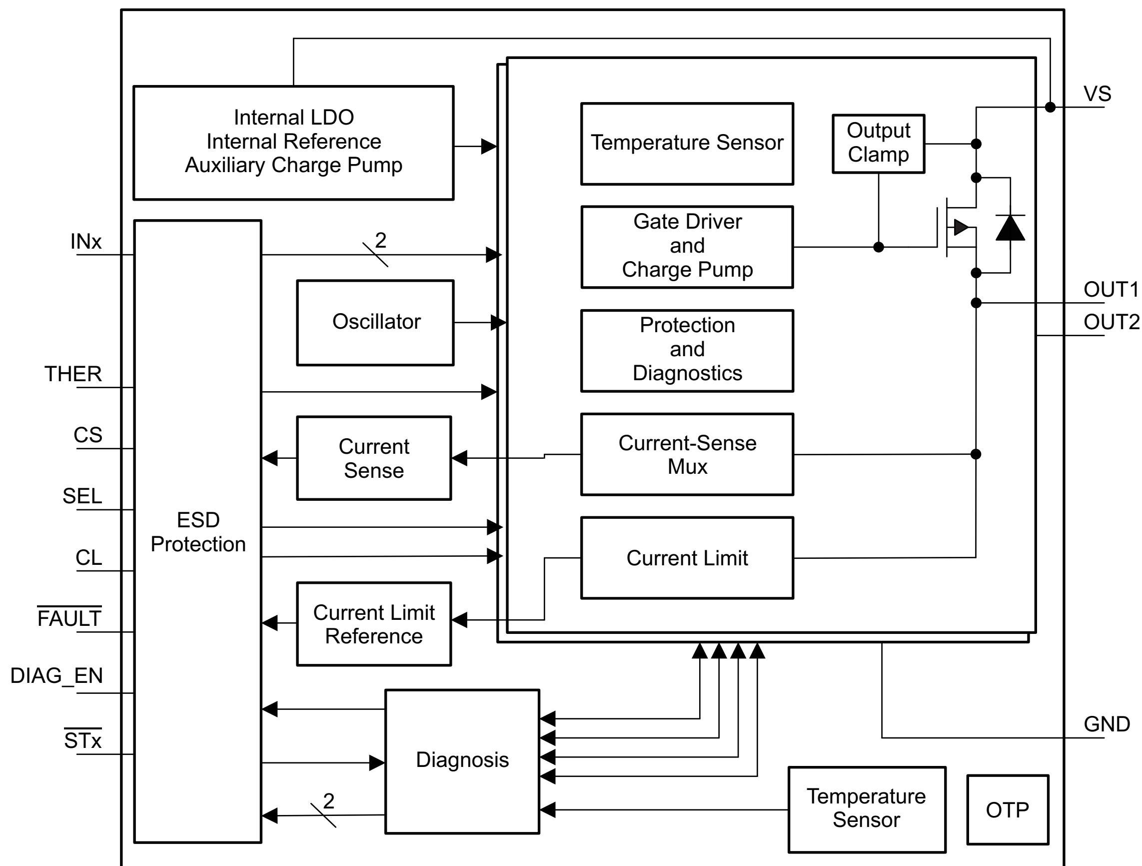
## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 22. All voltages are measured relative to the ground plane.

## Feature Description (continued)

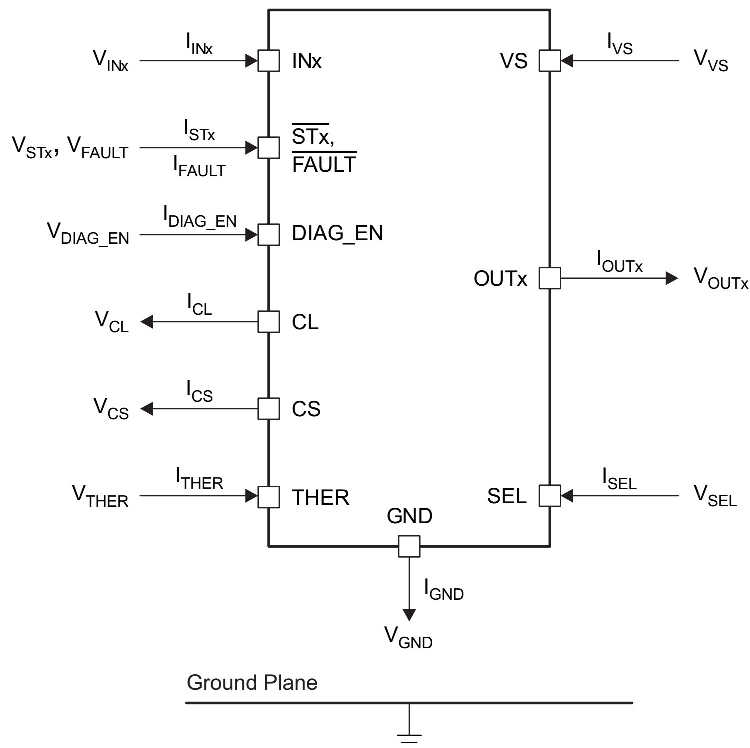



**Figure 22. Voltage and Current Conventions**

### 8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the version-B device. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

One integrated current mirror can source 1 / $K_{(CS)}$ of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the four channels. $K_{(CS)}$ is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See Figure 23 for more details.

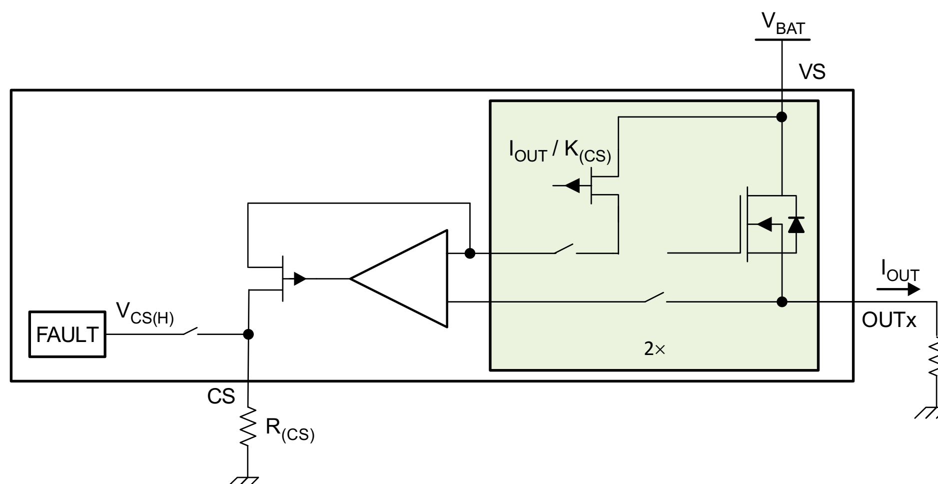



**Figure 23. Current-Sense Block Diagram**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## Feature Description (continued)

When a fault occurs, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. See Figure 24 for more details.

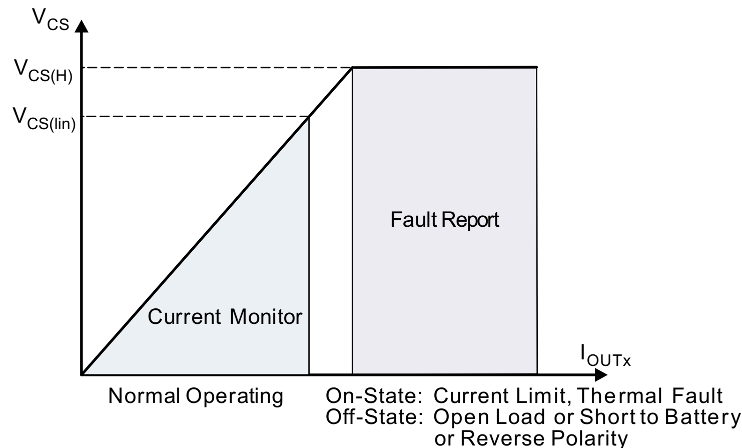


**Figure 24. Current-Sense Output-Voltage Curve**

Use Equation 1 to calculate $R_{(CS)}$.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \tag{1}$$

Take the following points into consideration when calculating $R_{(CS)}$.

- Ensure $V_{CS}$ is within the current-sense linear region ($V_{CS}$, $I_{OUTx(lin)}$) across the full range of the load current. Check $R_{(CS)}$ with Equation 2.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS(lin)}}{I_{CS}} \tag{2}$$

- In fault mode, ensure $I_{CS}$ is within the source capacity of the CS pin ($I_{CS(H)}$). Check $R_{(CS)}$ with Equation 3.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \tag{3}$$

### 8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$ to reduce the power dissipation on the power FET. See Figure 25 for more details.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threashold. Use the Equation 4 to calculate the $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

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## Feature Description (continued)

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (4)$$

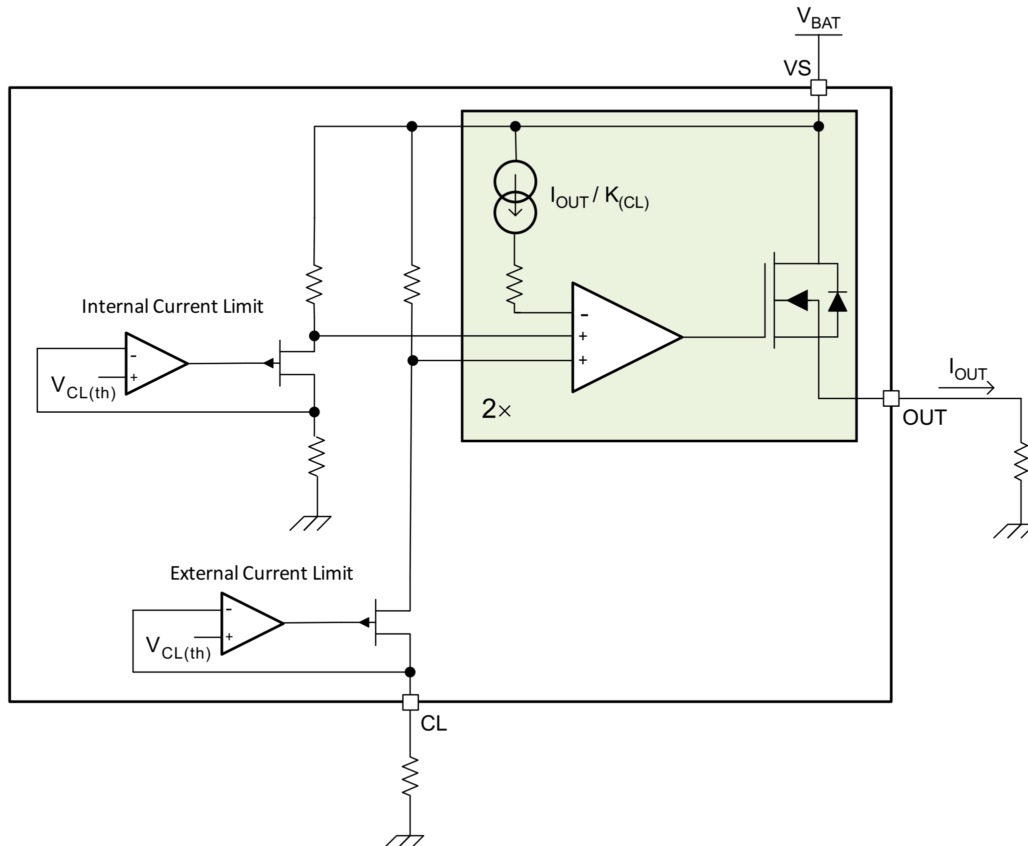


**Figure 25. Current-Limit Block Diargam**

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the INx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 µs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

### 8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (5)$$

During the period of demagnetization ($t_{decay}$), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.


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## Feature Description (continued)

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (6)$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

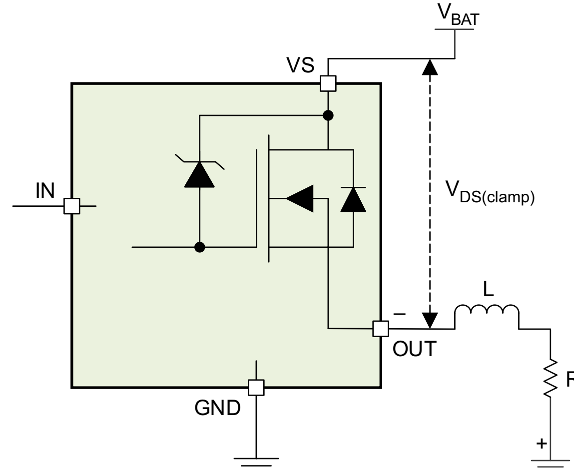


**Figure 26. Drain-to-Source Clamping Structure**

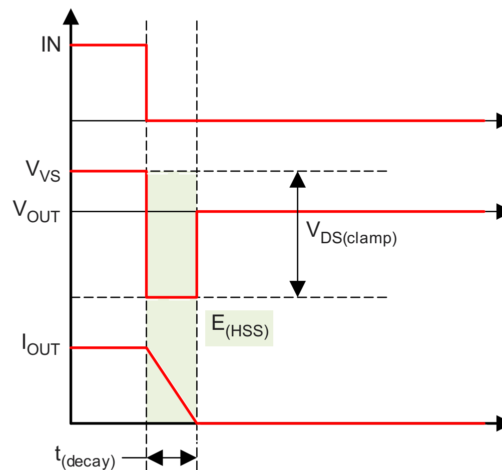


**Figure 27. Inductive Load Switching-Off Diagram**

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (7)$$

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## Feature Description (continued)

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I^2_{OUT(max)} \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \tag{8}$$

Figure 28 is a waveform of the device driving an inductive load, and Figure 29 is waveform with an expanded time scale. Channel 1 is the IN signal, channel 2 is the supply voltage $V_{VS}$, channel 3 is the output voltage $V_{OUT}$, channel 4 is the output current $I_{OUT}$, and channel M is the measured power dissipation $E_{(HSS)}$.

On the waveform, the duration of $V_{OUT}$ from $V_{VS}$ to ($V_{VS}$ – $V_{DS(clamp)}$) is around 120 µs. The device also optimizes the switching-off slew rate when the clamp is active. This optimization can help the system design by keeping the effects of transient power and EMI to a minimum. As shown in Figure 28 and Figure 29, the controlled slew rate is around 0.5 V/µs.

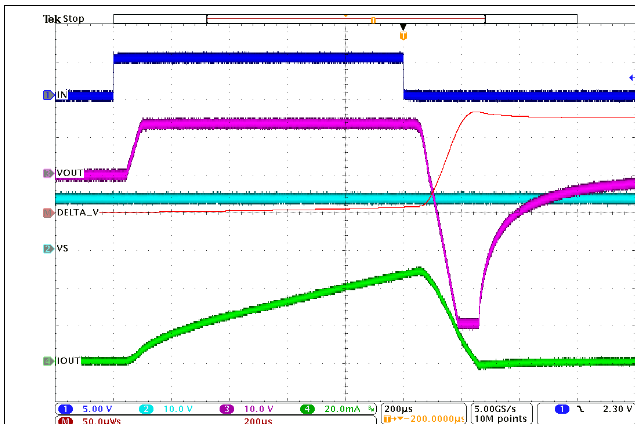


Figure 28. Inductive Load Switching-Off Waveform

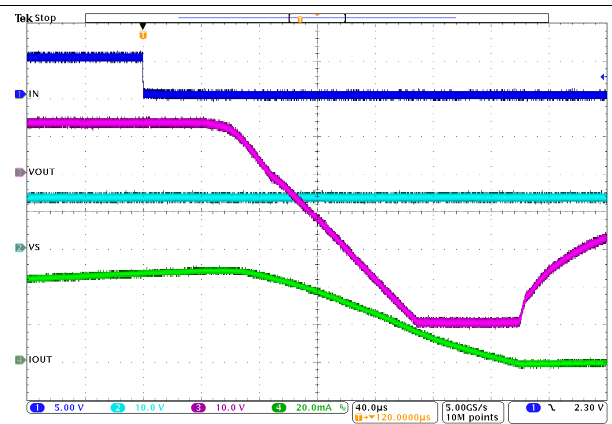


Figure 29. Inductive Load Switching-Off Expanded Waveform

Note that for PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry shown in Figure 30 to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 30 for more details.

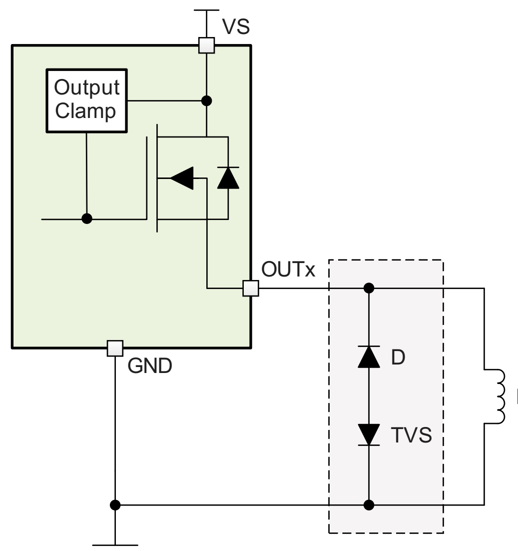


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Figure 30. Protection With External Circuitry


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## Feature Description (continued)

### 8.3.5 Fault Detection and Reporting

#### *8.3.5.1 Diagnostic Enable Function*

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and INx low.

#### *8.3.5.2 Multiplexing of Current Sense*

For version B, SEL is used to multiplex the shared current-sense function between the two channels. See Table 1 for more details.

**Table 1. Diagnosis Configuration Table**

| DIAG_EN | INx | SEL | CS ACTIVATED CHANNEL | CS, $\overline{\text{FAULT}}$, $\overline{\text{STx}}$ | PROTECTIONS AND DIAGNOSTICS |
|---|---|---|---|---|---|
| L | H | — | — | High impedance | Diagnostics disabled, full protection |
| | L | | | | Diagnostics disabled, no protection |
| H | — | 0 | Channel 1 | See Table 2 | See Table 2 |
| | | 1 | Channel 2 | | |

#### *8.3.5.3 Fault Table*

Table 2 applies when the DIAG_EN pin is enabled.

**Table 2. Fault Table**

| CONDITIONS | INx | OUTx | THER | CRITERION | $\overline{\text{STx}}$ (VER. A) | CS (VER. B) | $\overline{\text{FAULT}}$ (VER. B) | FAULT RECOVERY |
|---|---|---|---|---|---|---|---|---|
| Normal | L | L | — | — | H | 0 | H | — |
| | H | H | — | — | H | In linear region | H | — |
| Overlaod, short to ground | H | L | — | Current limit triggered | L | $V_{CS(H)}$ | L | Auto |
| Open load(1), short to battery, reverse polarity | L | H | — | $V_{VS} – V_{OUTx} < V_{(ol,off)}$ | L | $V_{CS(H)}$ | L | Auto |
| Thermal shutdown | H | — | L | $T_{SD}$ triggered | L | $V_{CS(H)}$ | L | Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when INx toggles. |
| | | | H | | | | | Output latch off. Fault recovers when INx toggles. |
| Thermal swing | H | — | — | $T_{SW}$ triggered | L | $V_{CS(H)}$ | L | Auto |

(1) An external pullup is required for open-load detection.

#### *8.3.5.4 $\overline{\text{STx}}$ and $\overline{\text{FAULT}}$ Reporting*

For version A, two individual $\overline{\text{STx}}$ pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls $\overline{\text{STx}}$ down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the $\overline{\text{STx}}$ pins together.

For version B, a global $\overline{\text{FAULT}}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{\text{FAULT}}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the $\overline{\text{FAULT}}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, $V_{CS(H)}$.

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### 8.3.6 Full Diagnostics

#### *8.3.6.1 Short-to-GND and Overload Detection*

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{CL(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

#### *8.3.6.2 Open-Load Detection*

##### 8.3.6.2.1 Channel On

When a channel on, benefiting from the high-accuracy current sense in a small current range, if an open-load event occurs, it can be detected as an ultralow $V_{CS}$ and handled by the microcontroller. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must set the SEL pin to detect the channel-on open-load fault proactively.

##### 8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} – V_{OUTx} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.

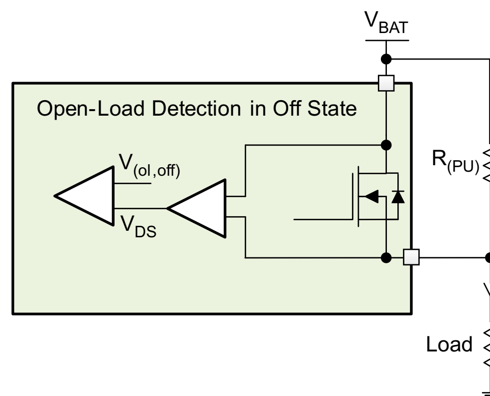


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**Figure 31. Open-Load Detection in Off-State**

#### *8.3.6.3 Short-to-Battery Detection*

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 2 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.

- If $V_{OUTx} – V_{VS} < V_{(F)}$ (body diode forward voltage), no reverse current occurs.
- If $V_{OUTx} – V_{VS} > V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$. Setting an INx pin high can minimize the power stress on its channel. Also, for external reverse protection, see Reverse-Current Protection for more details.

#### *8.3.6.4 Reverse Polarity Detection*

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See Table 2 for more details.


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In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$. Set the related INx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see Reverse-Current Protection for more details.

#### *8.3.6.5 Thermal Fault Detection*

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

##### 8.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thefrmal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.

- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{(SD)} – T_{(hys)}$, but the current is limited to $I_{CL(TSD)}$ to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when $T_J < T_{(SD,rst)}$ or after toggling the related INx pin.
- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} – T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} – T_{(Logic)} < T_{(sw)} – T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 32, multiple thermal swings are triggered before thermal shutdown occurs.

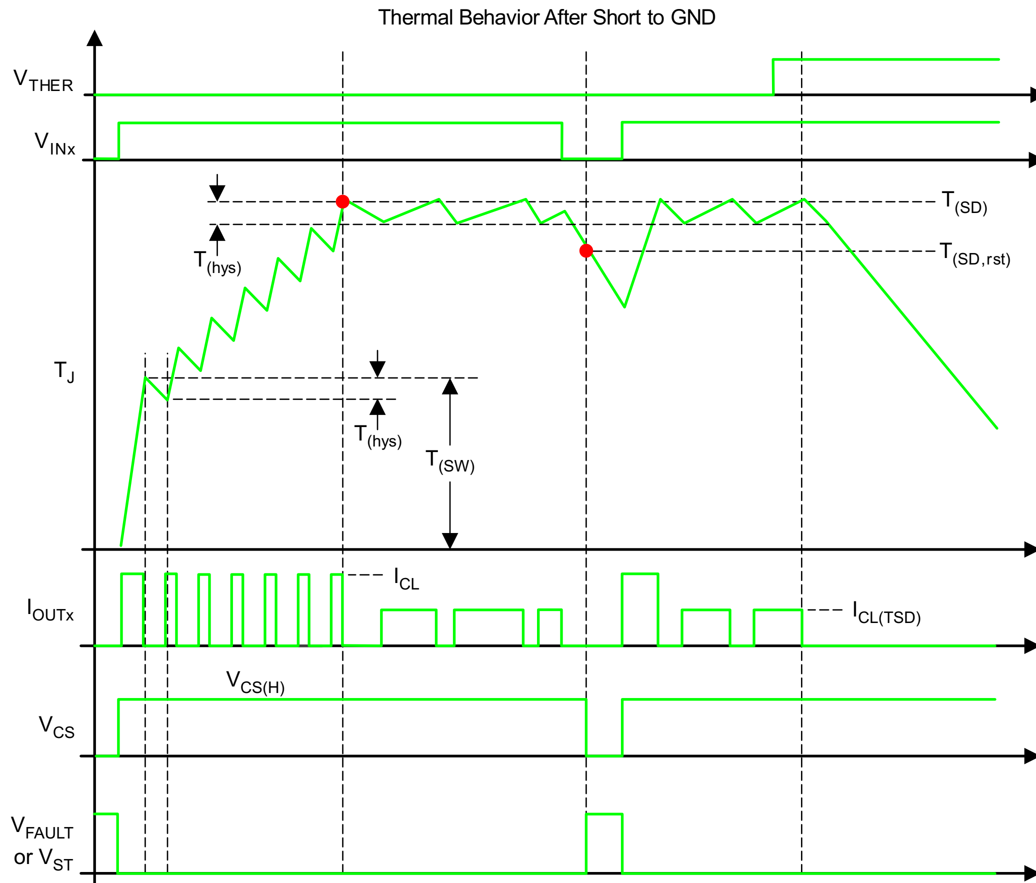


**Figure 32. Thermal Behavior Diagram**

### 8.3.7 Full Protections

#### *8.3.7.1 UVLO Protection*

The device monitors the supply voltage $V_{VS}$, to prevent unpredicted behaviors when $V_{VS}$ is too low. When $V_{VS}$ falls down to $V_{VS(uvf)}$, the device shuts down. When $V_{VS}$ rises up to $V_{VS(uvr)}$, the device turns on.

#### *8.3.7.2 Loss-of-GND Protection*

When loss of GND occurs, output is shut down regardless of whether the INx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

#### *8.3.7.3 Protection for Loss of Power Supply*

When loss of supply occurs, the output is shut down regardless of whether the INx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends the external free-wheeling diode as shown in Figure 33.


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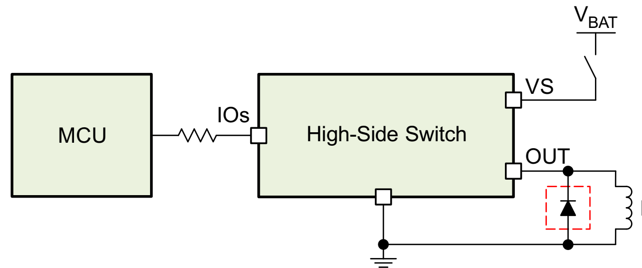


**Figure 33. Protection for Loss of Power Supply**

#### *8.3.7.4 Reverse-Current Protection*

Reverse current occurs in two conditions: short to battery and reverse polarity.

- When a short to the battery occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current. The GND pin maximum current is specified in the Absolute Maximum Ratings.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

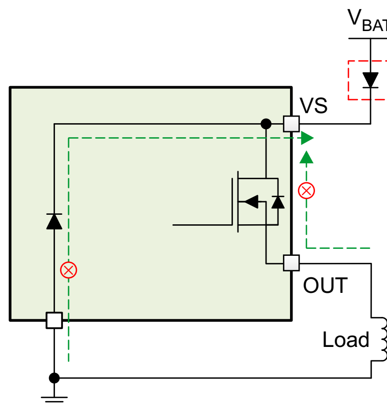


**Figure 34. Reverse-Current External Protection, Method 1**

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

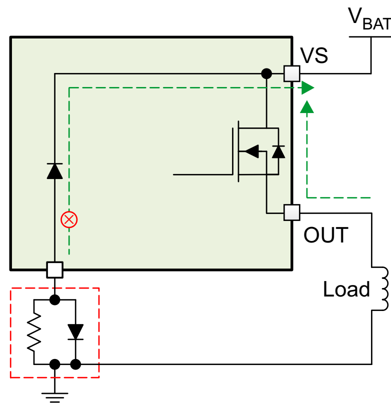


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**Figure 35. Reverse-Current External Protection, Method 2**

#### *8.3.7.5 MCU I/O Protection*

In some severe conditions, such as the ISO7637-2 test or the loss of battery with inductive loads, a negative pulse occurs on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

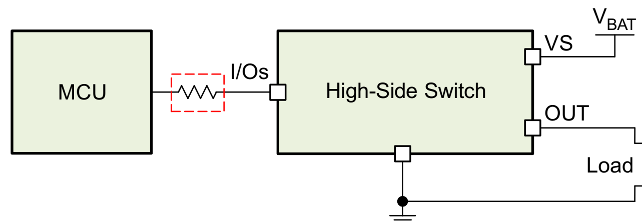


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**Figure 36. MCU I/O External Protection**

## 8.4 Device Functional Modes

### 8.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for $t > t_{(off,deg)}$ to enter the standby mode, where $t_{(off,deg)}$ is the standby mode deglitch time used to avoid false triggering. Figure 37 shows a working-mode diagram.


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## Device Functional Modes (continued)

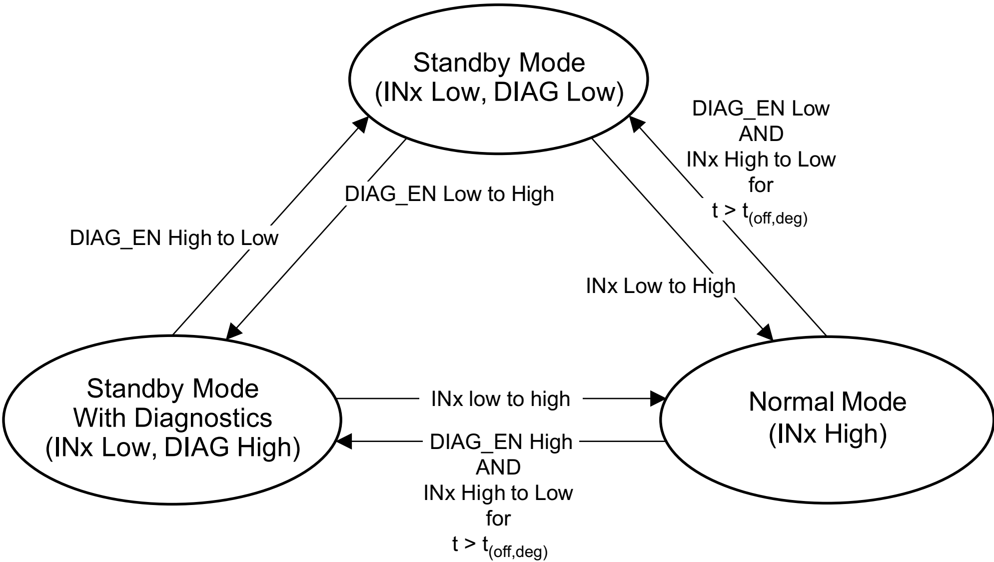


**Figure 37. Working Modes**

# 9 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TPS2H160-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

## 9.2 Typical Application

The following figure shows an example of the external circuitry connections based on the version-B device.

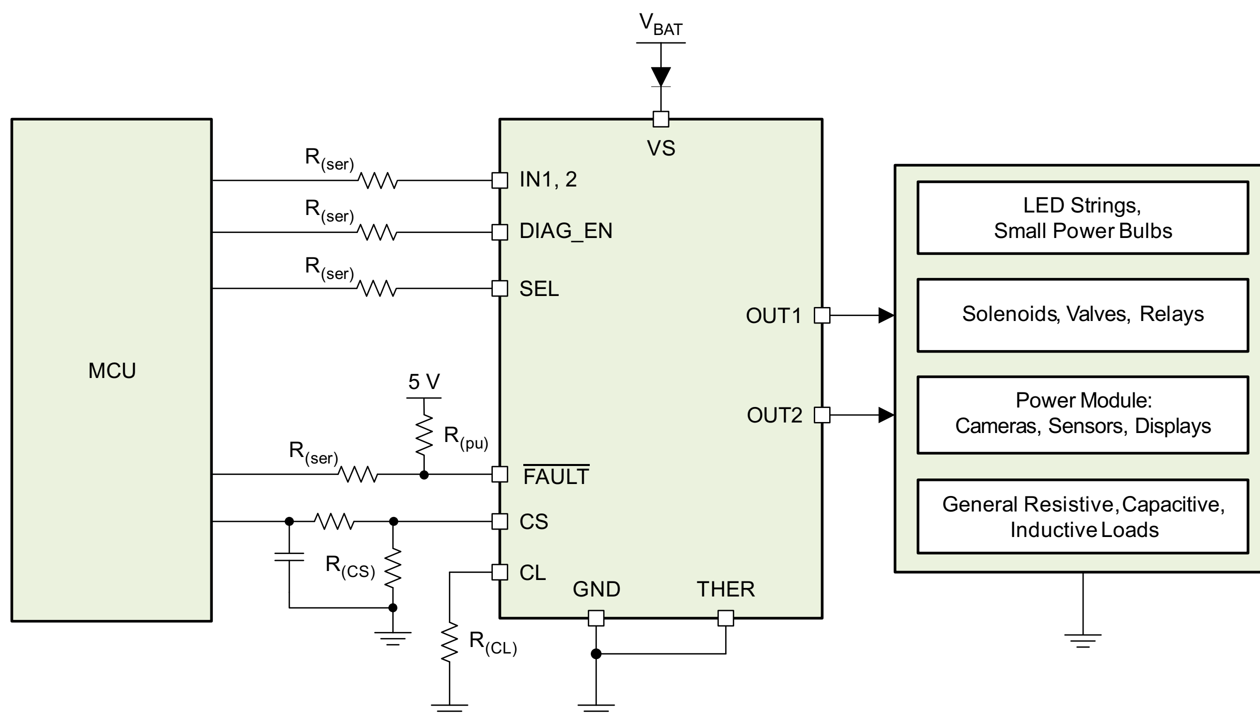


**Figure 38. Typical Application Diagram**

### 9.2.1 Design Requirements

- $V_{VS}$ range from 9 V to 16 V
- Load range is from 0.1 A to 1 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 2.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU
- Reverse-voltage protection with a blocking diode in the power-supply line


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## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

To keep the 1-A nominal current in the 0 to 4-V current-sense range, calculate the $R_{(CS)}$ resistor using Equation 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 290}{1} = 1160\ \Omega \quad (9)$$

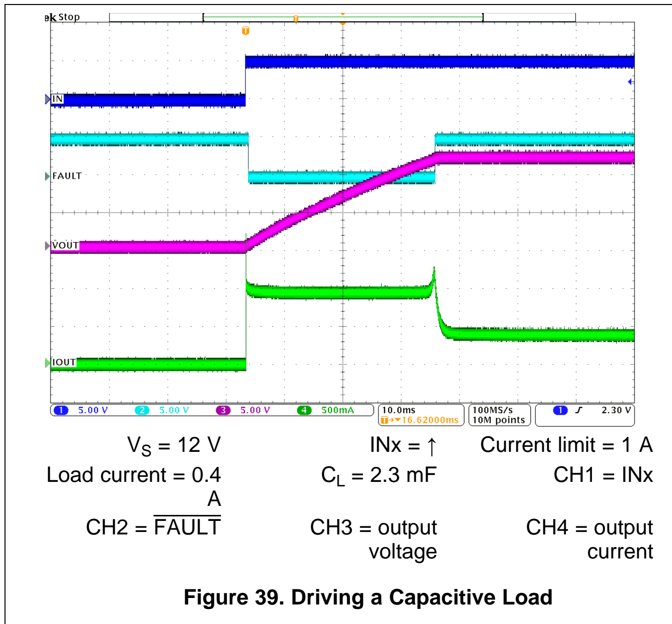
To set the adjustable current limit value at 2.5-A, calculate $R_{(CL)}$ using Equation 10.

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 2500}{2.5} = 800\ \Omega \quad (10)$$

TI recommends $R_{(ser)}$ = 10 kΩ for 5-V MCU, and $R_{(pu)}$ = 10 kΩ as the pullup resistor.

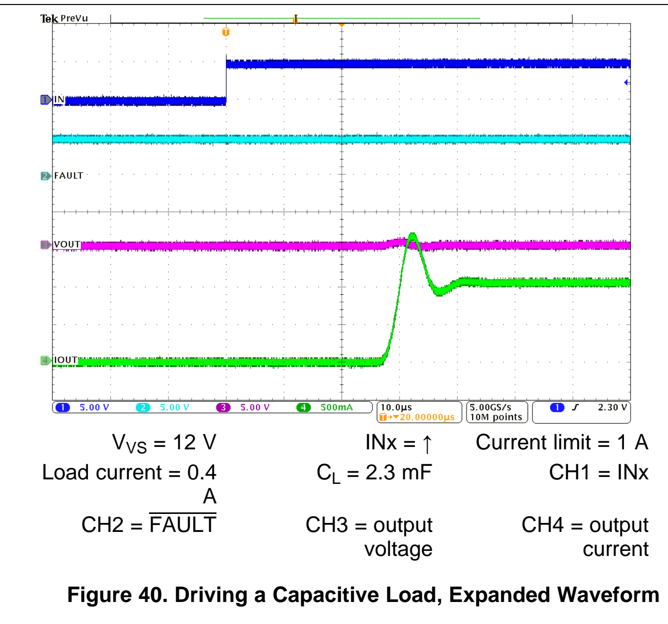
### 9.2.3 Application Curves

Figure 39 shows a test example of soft-start when driving a big capacitive load. Figure 40 shows an expanded waveform of the output current.




| $V_S$ = 12 V | INx = ↑ | Current limit = 1 A |
|---|---|---|
| Load current = 0.4 A | $C_L$ = 2.3 mF | CH1 = INx |
| CH2 = $\overline{FAULT}$ | CH3 = output voltage | CH4 = output current |

**Figure 39. Driving a Capacitive Load**

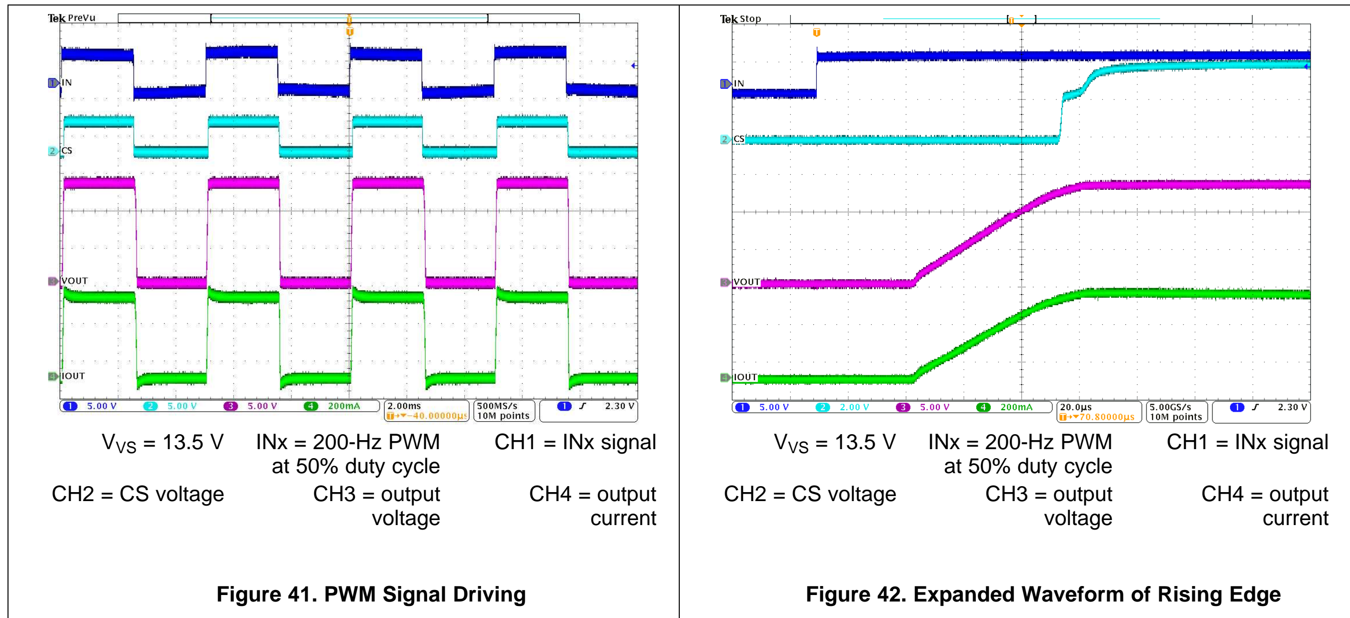



| $V_{VS}$ = 12 V | INx = ↑ | Current limit = 1 A |
|---|---|---|
| Load current = 0.4 A | $C_L$ = 2.3 mF | CH1 = INx |
| CH2 = $\overline{FAULT}$ | CH3 = output voltage | CH4 = output current |

**Figure 40. Driving a Capacitive Load, Expanded Waveform**

## Typical Application (continued)

Figure 41 shows a test example of PWM-mode driving. Figure 42 shows the expanded waveform of the rising edge. Figure 43 shows the expanded waveform of the falling edge.

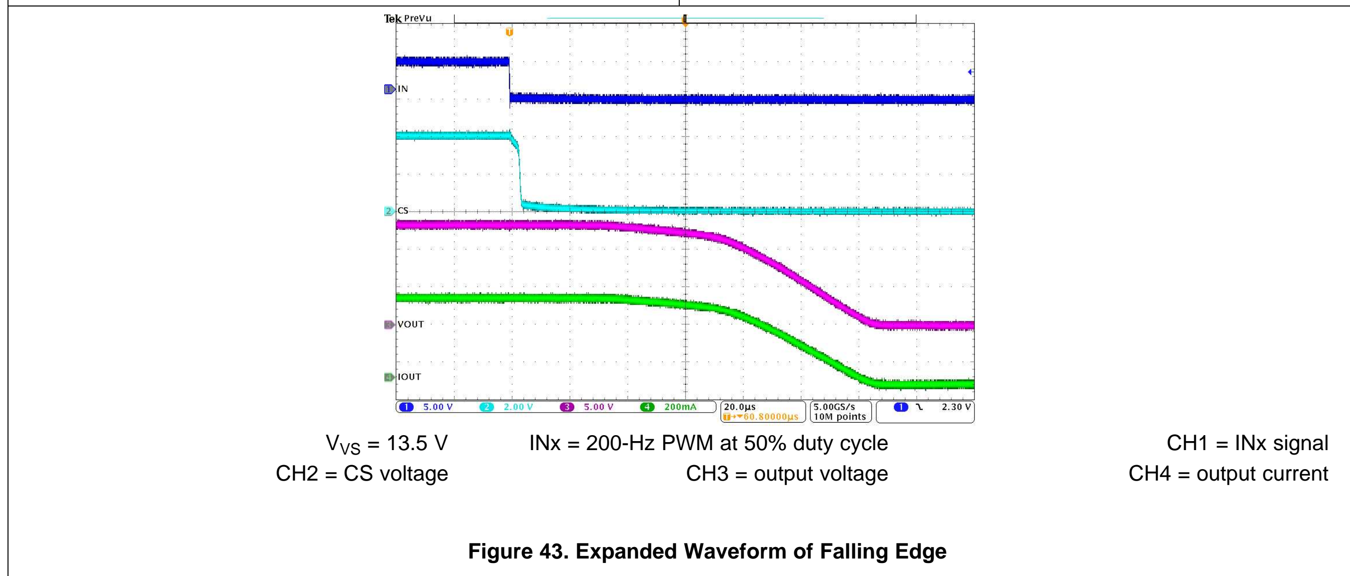



$V_{VS}$ = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

**Figure 41. PWM Signal Driving**

$V_{VS}$ = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

**Figure 42. Expanded Waveform of Rising Edge**




$V_{VS}$ = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

**Figure 43. Expanded Waveform of Falling Edge**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# 10 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. Detailed supply voltage should be within the range specified in the *Recommended Operating Conditions*.

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# 11 Layout

## 11.1 Layout Guidelines

To prevent thermal shutdown, $T_J$ must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

## 11.2 Layout Examples

### 11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

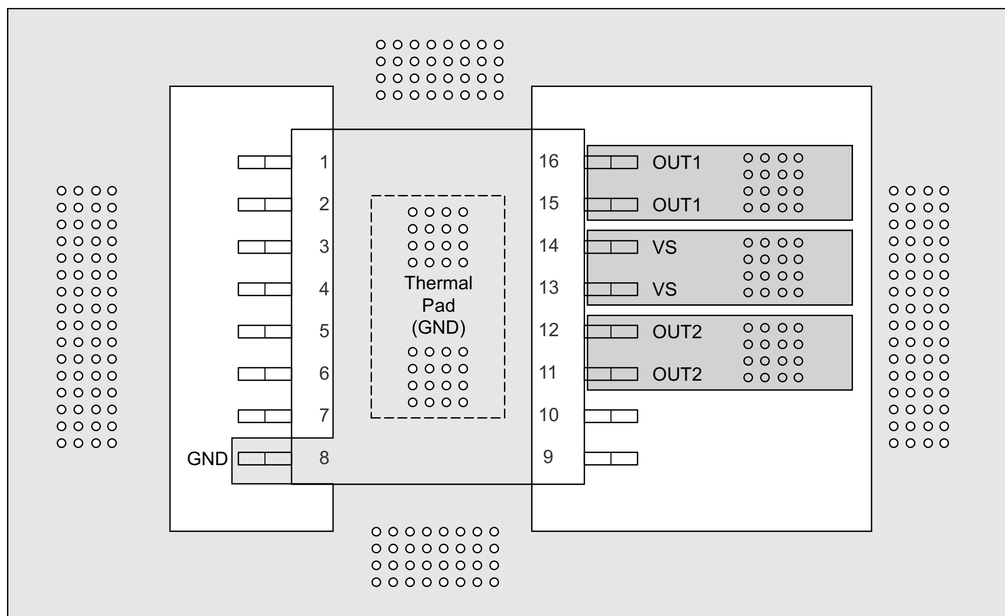


**Figure 44. Layout Example Without a GND Network**


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## Layout Examples (continued)

### 11.2.2 With a GND Network

With a GND network, tie the thermal pad as one trace to the board GND copper.

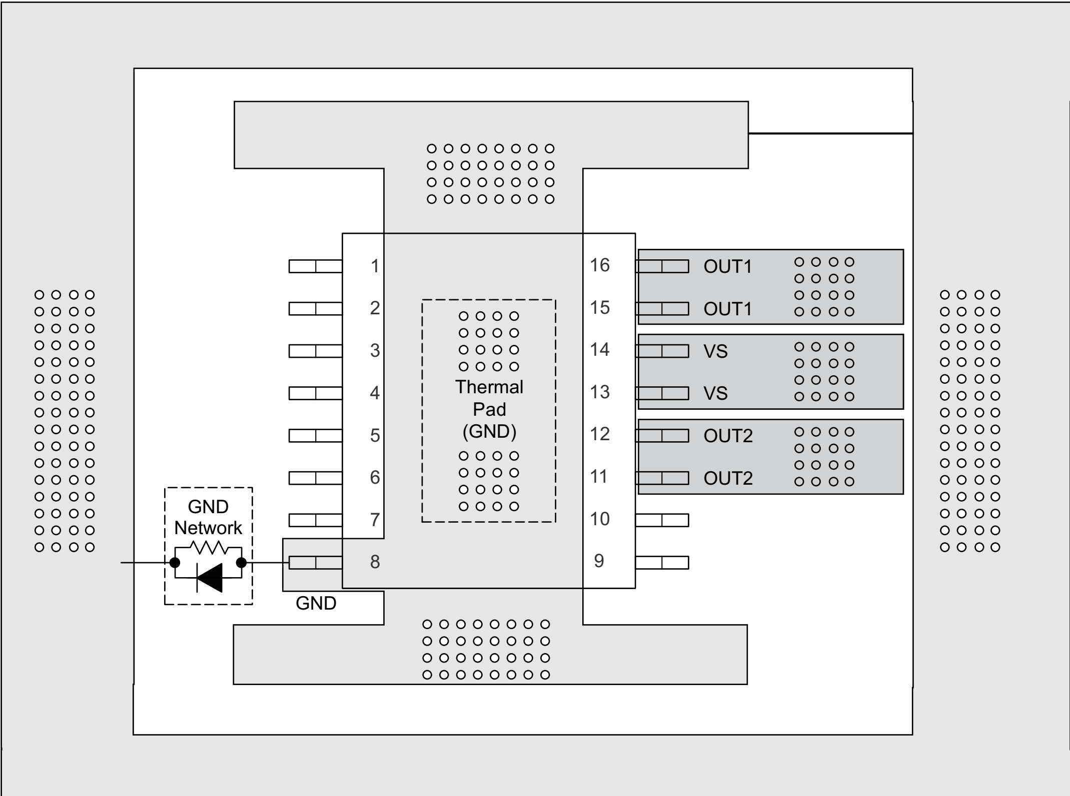


Figure 45. Layout Example With a GND Network

# 12 器件和文档支持

## 12.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏


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| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2H160AQPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | 2H160AQ | Samples |
| TPS2H160BQPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | 2H160BQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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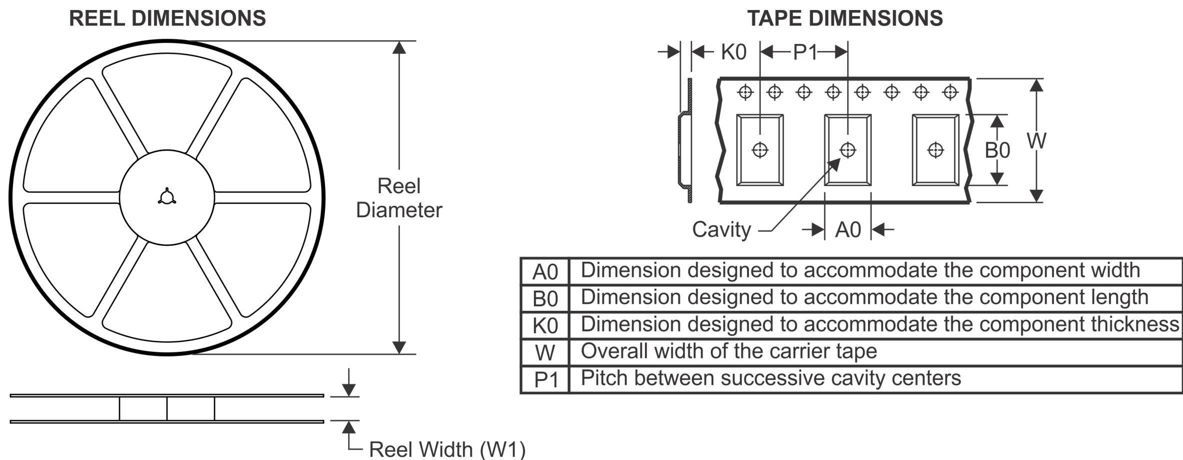
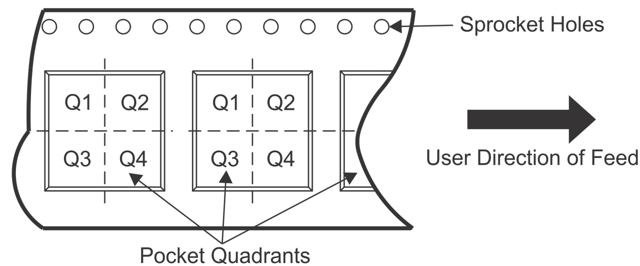



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

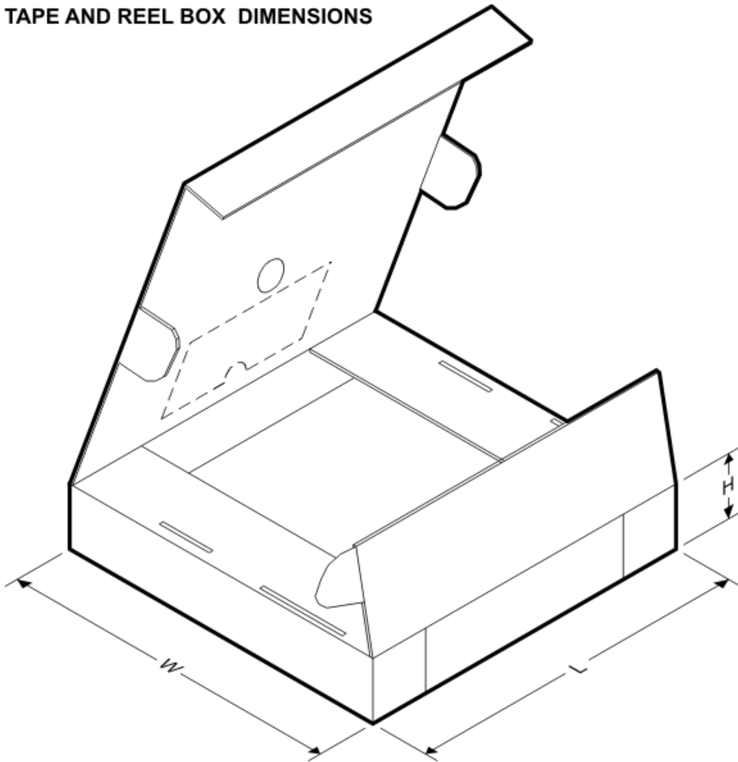
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2H160AQPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS2H160BQPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

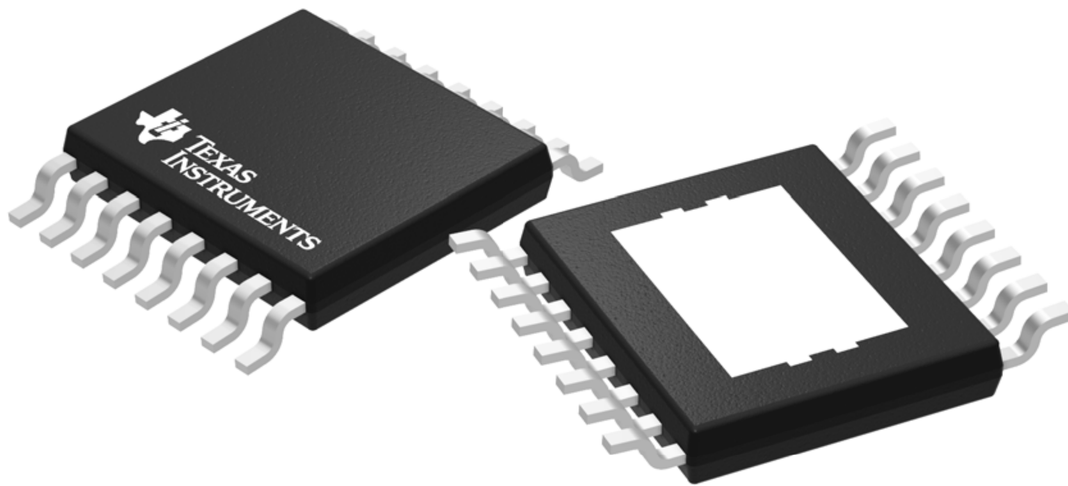



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2H160AQPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS2H160BQPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 38.0 |

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

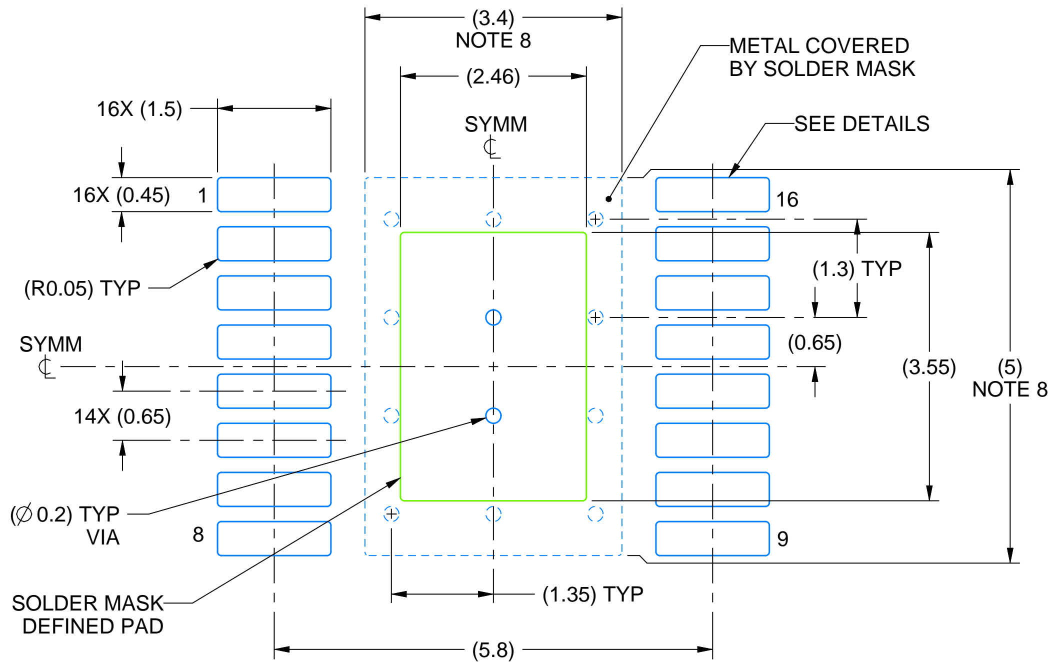



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

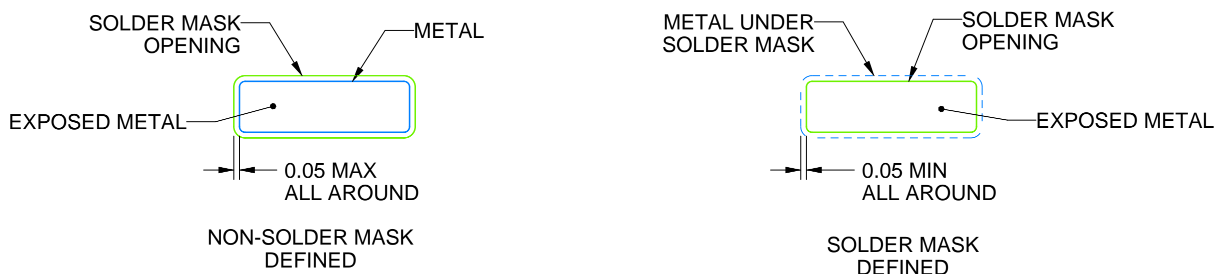
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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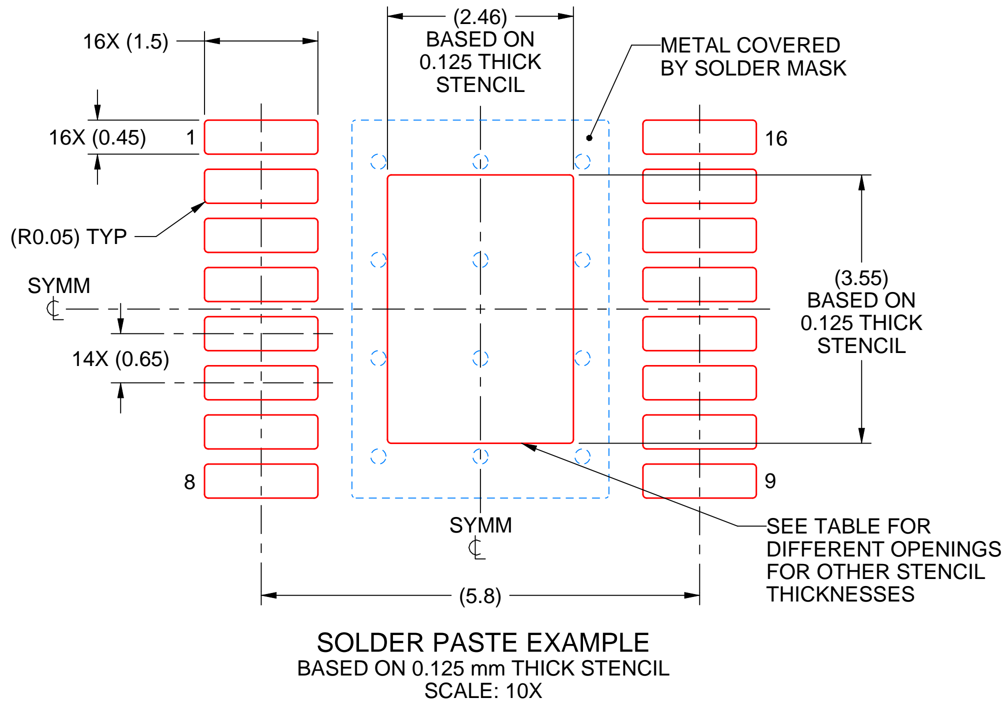
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.75 X 3.97 |
| 0.125 | 2.46 X 3.55 (SHOWN) |
| 0.15 | 2.25 X 3.24 |
| 0.175 | 2.08 X 3.00 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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