REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraphs 1.5, 4.4.4.1, and 4.4.4.2 for radiation hardened requirements. Make change to Input voltage Enable (EN) maximum limit as specified under paragraph 1.3 by deleting “6.5 V” and replacing with “3.6 V”. Delete Peak output current and Power good (PGOOD) pin sink current parameters as specified under paragraph 1.3. Delete footnote under paragraph 1.6. Make change to the Shutdown parameter unit symbol as specified under Table I by deleting “µA” and replacing with “mA”. Add note to AGND terminal description as specified under Figure 1. Add static burn-in to Table IIA. Add subgroup 1 to Group E endpoint parameters under Table IIA. - ro	16-06-21	C. SAFFLE

REV																				
SHEET																				
REV	A	A																		
SHEET	15	16																		

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
16-04-15

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, SINK/SOURCE DDR TERMINATION VOLTAGE REGULATOR, MONOLITHIC SILICON

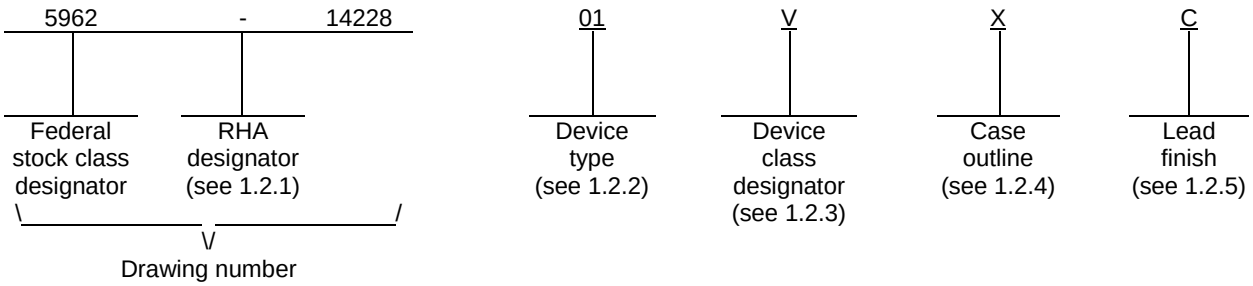
SIZE	CAGE CODE	
A	**67268**	**5962-14228**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H3301-SP	Sink/source double data rate (DDR) termination voltage regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Input voltage: 2/
- Input voltage (V_{IN}) / supply voltage (V_{DD}), supply voltage for low dropout regulator (VLDOIN), remote sensing (VTTSNS), sense input (VDDQSNS) ..... -0.36 V to 3.6 V
- Enable (EN) ..... -0.3 V to 3.6 V
- Signal ground (PGND) to ground (GND) ..... -0.3 V to 0.3 V

Output voltage: 2/
- Output voltage (VO/VTT), reference output (VTTREF) ..... -0.3 V to 3.6 V
- Power good (PGOOD) ..... -0.3 V to 3.6 V

Maximum operating junction temperature (T_J) ..... -55°C to +150°C
Storage temperature range ..... -55°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Electrostatic discharge (ESD) ratings:
- Human body model (HBM) ..... -4,000 V to +4, 000 V 3/
- Charged device model (CDM) ..... -750 V to +750 V 4/

1.4 Recommended operating conditions.

Supply voltages (V_{IN} / V_{DD}) ..... 2.375 V to 3.5 V
Voltage range:
- VLDOIN ..... 0.9 V to 3.5 V
- EN VTTSNS ..... -0.1 V to 3.5 V
- VDDQSNS ..... 1.0 V to 3.5 V
- VO/VTT, PGOOD ..... -0.1 V to 3.5 V
- VTTREF ..... -0.1 V to 1.8 V
- PGND ..... -0.1 V to 0.1 V

Operating junction temperature (T_J) ..... -55°C to +125°C
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total ionizing dose available (dose rate = 50 – 300 rads(Si)/s) ..... 100 krads(Si) 5/
Maximum total ionizing dose available (dose rate = 10 mrads(Si)/s) ..... 100 krads(Si) 5/

The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltage values are with respect to the network ground pin.

3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si).

1.6 Thermal characteristics. 6/ 7/

Thermal metric	Symbol	Limit	Unit
Thermal resistance, junction to case (bottom)	$\theta_{JC(BOT)}$	0.6	°C/W

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC Solid State Technology Association

JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

6/ Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.

7/ Maximum power dissipation may be limited by overcurrent protection.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current.							
Supply current	IIN/IVDD	V_{EN} = 3.3 V, no load	1,2,3	01		30	mA
Shutdown current	IVDD(SDN)	V_{EN} = 0 V, VDDQSNS = 0 V, no load	1,2,3	01		5	mA
		V_{EN} = 0 V, VVVQSNS > 0.78 V, no load				8	
Supply current of VLDOIN	ILDOIN	V_{EN} = 3.3 V, no load	1,2,3	01		1200	µA
Shutdown current of VLDOIN	ILDOIN(SDN)	V_{EN} = 0 V, no load	1,2,3	01		100	µA
Input current.							
Input current, VDDQSNS	IVDDQSNS	VEN = 3.3 V	1,2,3	01		6	µA
VO / VTT output.							
Output dc voltage, VO	VVOSNS/ VTTSNS	V_{LDOIN} = 2.5 V, VVTTREF = 1.25 V (DDR1), I_O = 0 A	1,2,3	01	-6	6	mV
		V_{LDOIN} = 1.8 V, VVTTREF = 0.9 V (DDR2), I_O = 0 A			-6	6	
		V_{LDOIN} = 1.5 V, VVTTREF = 0.75 V (DDR3), I_O = 0 A			-6	6	
		V_{LDOIN} = 1.35 V, VVTTREF = 0.675 V (DDR3L), I_O = 0 A			-6	6	
		V_{LDOIN} = 1.20 V, VVTTREF = 0.60 V (DDR4), I_O = 0 A			-6	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
V_{LODIN} - V_{TT}	V_{LODIN} > VTT	V_{IN}/V_{DD} = 2.95 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 2.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR1)	1,2,3	01		230	mV
		V_{IN}/V_{DD} = 2.95 V, I_O = 1 A, $V_{VDDQSNS}$ = 2.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR1)				300	
		V_{IN}/V_{DD} = 2.95 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 2.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR1)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, 4/ $V_{VDDQSNS}$ = 1.80 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR2)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, 4/ $V_{VDDQSNS}$ = 1.80 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR2)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.80 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR2)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.50 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3)				400	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
$V_{LODIN} > V_{TT}$	V_{LODIN} - VTT	V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)	1,2,3	01		230	mV
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				400	
Output voltage tolerance to VDDQSNS	VVOTOL/ VTTTOL	I_{VO} = -3 A, 4/ across V_{IN} voltage range	1,2,3	01	12	34	mV
		I_{VO} = 3 A, 4/ across V_{IN} voltage range			-12	-34	
VO/VTT source current limit	I_{VOSRCL}	With reference to V_{VTTREF}, V_{VTTSNS} = 90% x V_{VTTREF}	1,2,3	01	3.25	8	A
VO/VTT sink current limit	I_{VOSNCL}	With reference to V_{VTTREF}, V_{VTTSNS} = 110% x V_{VTTREF}	1,2,3	01	3.5	5.5	A
Discharge impedance	RDSCHRG	V_{DDQSNS} = 0 V, V_{VO}= 0.3 V, V_{EN} = 0 V, T_A = +25C	1	01		25	Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Powergood comparator.							
VO/VTT PGOOD threshold	VTH(PG)	PGOOD window lower threshold with respect to V_{VTTREF}	1,2,3	01	-23.5	-17.5	%
		PGOOD window upper threshold with respect to V_{VTTREF}			17.5	23.5	
Output low voltage	$V_{PGOODLOW}$	I_{SINK} = 4 mA	1,2,3	01		0.4	V
Leakage current	IPGOODLK	VOSNS = VREFIN (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V	1,2,3	01		1	µA
V_{DDQSNS} and V_{VTTREF} output.							
V_{DDQSNS} voltage range	V_{DDQSNS_UVLO}		1,2,3	01	1.0	2.8	V
VTTREF voltage tolerance to $V_{VDDQSNS}$	V_{VTTREF}	-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 2.5 V	1,2,3	01	-15	15	mV
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.8 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.5 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.35 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.2 V			-15	15	
VVTTREF source current limit	$I_{VTTREFSRCL}$	V_{REFOUT} = 0 V	1,2,3	01	10		mA
VVTTREF sink current limit	$I_{VTTREFSRCCL}$	V_{REFOUT} = 0 V	1,2,3	01	6		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
UVLO/EN logic threshold.							
UVLO threshold	$V_{VINUVVIN}$	Wake up, T_A = +25°C	1	01		2.25	V
High level input voltage	V_{ENIH}	Enable	1,2,3	01	1.7		V
Low level input voltage	V_{ENIL}	Enable	1,2,3	01		0.3	V
Logic input leakage current	I_{ENLEAK}	Enable, T_A = +25°C	1	01	-1	1	µA

1/ Unless otherwise specified, V_{IN}/V_{DD} = 3.3 V and 2.375 V, V_{VLDOIN} = 1.8 V, $V_{VDDQSNS}$ = 1.8 V, $V_{VOSNS/VTTSNS}$ = 0.9 V, and $V_{EN} = V_{VIN/VDD}$.

2/ Devices supplied to this drawing have been characterized through all levels D, P, L and R of irradiation. However, this device is only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

3/ The manufacturer supplying RHA device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si).

4/ The parameter is guaranteed to the limits specified by characterization but, not production tested.

Case outline X

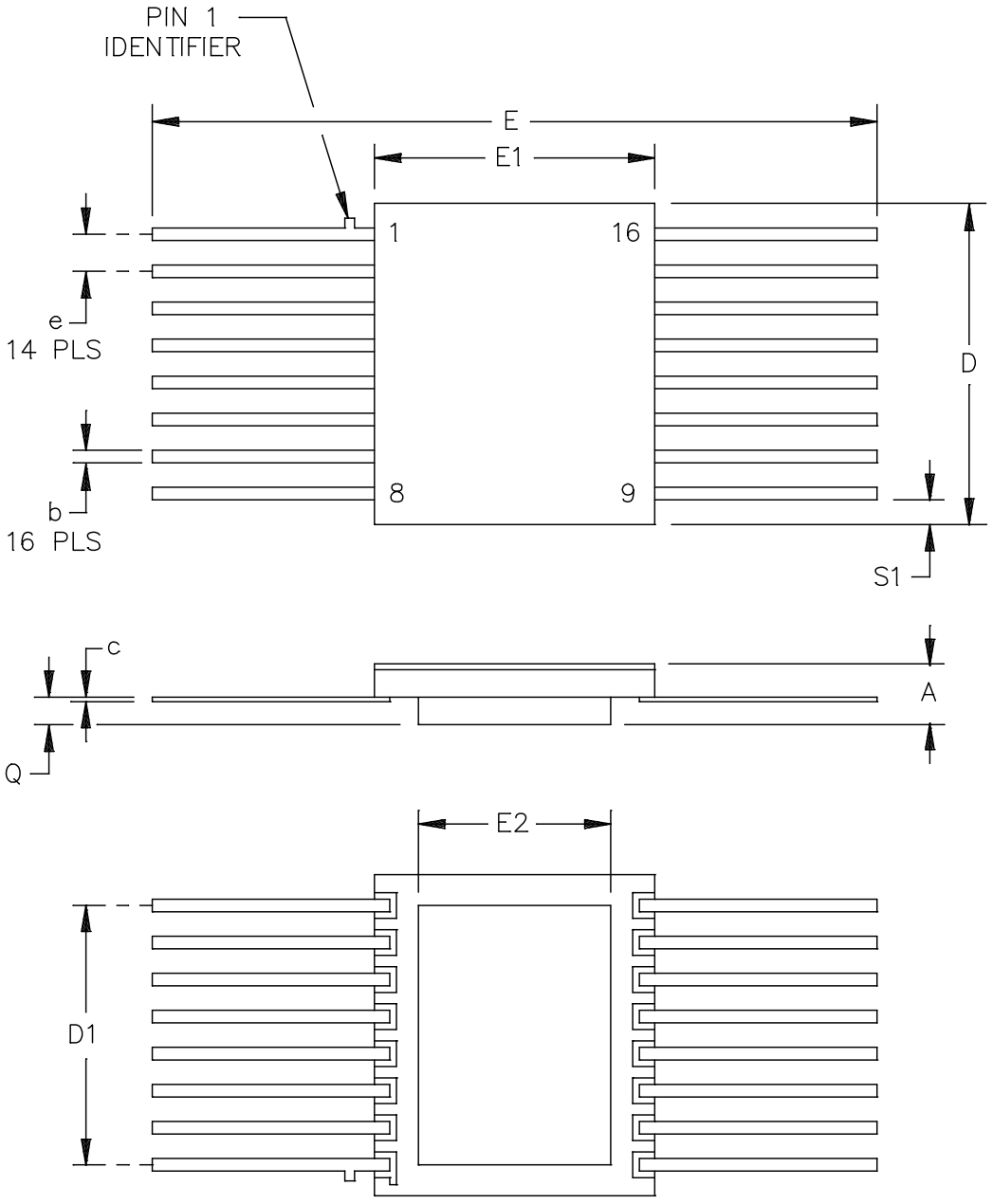


FIGURE 1. Case outline.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.833	2.333	0.072	0.092
b	0.382	0.482	0.015	0.019
c	0.097	0.177	0.004	0.007
D	10.760	11.260	0.424	0.443
D1	8.550	9.050	0.337	0.356
E	24.642	25.142	0.970	0.990
E1	9.380	9.880	0.369	0.389
E2	6.340	6.840	0.250	0.269
e	1.190	1.350	0.047	0.053
Q	0.690	1.190	0.027	0.047
S1	0.844 REF		0.033 REF	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid. Lid and heat sink are connected to pin 8 (GND).
3. The leads are gold plated.
4. Bottom side has a thermal pad.

FIGURE 1. Case outline - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Input / Output	Description
1	VTTREF	O	Reference output. Connect to GND through 0.1 μF ceramic capacitor.
2	VDDQSNS	I	VDDQ sense input. Reference input for VTTREF.
3	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
4	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
5	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
6	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
7	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
8	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
9	EN	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
10	VDD / V_{IN}	I	2.5 V or 3.3 V power supply. A ceramic decoupling capacitor with a value between 1 μF and 10 μF is required.
11	PGOOD	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
12	VTT / VO	O	Power output for VTT low drop out voltage regulator.
13	VTT / VO	O	Power output for VTT low drop out voltage regulator.
14	VTT / VO	O	Power output for VTT low drop out voltage regulator.
15	AGND	---	Signal ground. Connect to negative pin of output capacitors. See note.
16	VTTSNS	I	VDDQ sense input, reference input for VTTREF. Voltage sense for VTT/VO. Connect to positive pin of the output capacitor or the load.

NOTE: Thermal pad and package lid are internally connected to ground.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Static burn-in (see 4.2.1)	1/	1/
Final electrical parameters (see 4.2)	1,2,3 2/	1,2,3 3/
Group A test requirements (see 4.4)	1,2,3	1,2,3
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3 3/
Group D end-point electrical parameters (see 4.4)	1	1
Group E end-point electrical parameters (see 4.4)	---	1

1/ For device classes Q and V, static burn-in I test shall be performed per TM 1015 at test condition A or C.
2/ PDA applies to subgroup 1.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous endpoint electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Conditions	Limit	Unit
Supply current	I_{IN}/I_{VDD}	V_{EN} = 3.3 V, no load	±1	mA
Shutdown current	$I_{VDD(SDN)}$	V_{EN} = 0 V, no load, VDDQSNS > 0.78 V	±0.24	mA
Supply current of VLDOIN	I_{LDOIN}	V_{EN} = 3.3 V, no load	±60	µA
Shutdown current of VLDOIN	$I_{LDOIN(SDN)}$	V_{EN} = 0 V, no load, VDDQSNS > 0.78 V	±8.5	µA
Output DC voltage, VO	V_{VOSNS}/V_{TTSNS}	V_{LDOIN} = 1.8 V, I_O = 0 A, V_{VTTREF} = 0.9 V (DDR2)	±27	mV

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total irradiation dose testing. Total irradiation dose testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and condition D as specified herein.

4.4.4.2 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-06-21

Approved sources of supply for SMD 5962-14228 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1422801VXC	01295	TPS7H3301-SP
5962R1422801VXC	01295	TPS7H3301-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243