TPS25741, TPS25741A USB Type-C™ and USB Power Delivery Host Port Controllers

1 Features

- USB Power Delivery 2.0 Certified Provider, USB Type-C™ Revision 1.2 Compliant Source
- Pin-Selectable Voltage Advertisement
  - 5 V, 12 V, 20 V (TPS25741)
  - 5 V, 9 V, 15 V (TPS25741A)
- Pin-Selectable Peak Power Settings
  - 12 Options 15 W to 100 W (TPS25741)
  - 11 Options 15 W to 81 W (TPS25741A)
- High Voltage and Safety Integration
  - Overvoltage, Overcurrent, Overtemperature Protection and V_{BUS} Discharge
  - IEC 61000-4-2 Protection on CC1 and CC2
  - Input Pin for Fast Shutdown Under Fault
  - Control of External N-ch MOSFETs and P-ch MOSFETs for Single Power Path or Power Mux Architecture
  - 2-Pin External Power Supply Control
  - Wide VIN Supply (4.65 V – 25 V)
- 5.4-µA Quiescent Current When Unattached
- Port Power Management, Plug Polarity, Plug Status, Audio and Debug Accessory Indicators
- Built-in 1.8 V at 35-mA Supply Output

2 Applications

- Desktop and All-in-One Computers
- Automotive Infotainment
- Hub Downstream Ports
- USB-Power Delivery Adaptor (USB data capable)

3 Description

The TPS25741, TPS25741A implements a source compliant to USB Power Delivery 2.0 and USB Type-C revision 1.2. It can be used in either a power mux or DC-DC implementation shown in the figure below.

The device monitors the CC pin to detect a USB Type-C sink attachment, then enables the GDNG and G5V gate drivers to apply 5 V to V_{BUS} (refer to figure below). It then offers up to three voltages using USB Power Delivery. In order to source the second voltage the G5V gate driver is disabled and the GDPG gate driver is enabled. In power mux implementations all gate drivers are used and the CTL pins are not necessary. In DC-DC implementations only the GDNG gate driver is necessary and the CTL pins program the power supply for the required voltage. The device automatically discharges V_{BUS} per USB Power Delivery requirements. The PSEL, HIPWR, PCTRL, and EN9V/EN12V pins are used to configure the voltages and currents advertised.

The device typically draws 5.4 µA (8 µA if VDD = 0 V) when no device is attached. The Port Attachment indicator ($\overline{UFP}$ or DVDD) outputs may be used to disable the power source until a sink is attached for more system power savings.

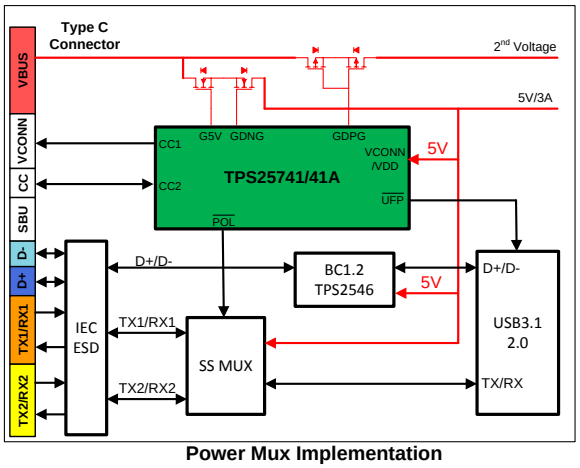
Protection features include over-voltage, over-current, over-temperature, IEC for CC pins, and system override of gate drivers ($\overline{GD}$).

Device Information[1]

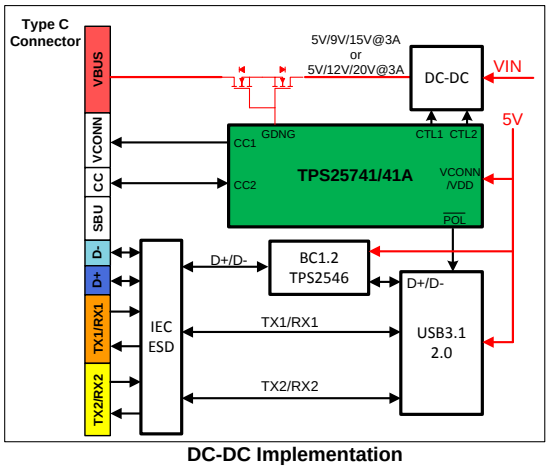
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25741	VQFN (32)	4.00 mm x 4.00 mm
TPS25741A	VQFN (32)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Implementations in DFP Host Ports



Power Mux Implementation



DC-DC Implementation

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4 Revision History

Changes from Revision B (January 2017) to Revision C **Page**

- Changed Shunt capacitance, VCONN value From: MAX = 10 µF To: MIN = 10 µF MAX = 220 µF in the *Recommended Operating Conditions* table ... 7
- Deleted the row for TPS25741A Input resistance, and changed the MAX value From: 5 MΩ To: 6 MΩ in the *Electrical Characteristics* table ... 10
- Changed the Unloaded output voltage on CC pin MIN value From: 2.8 V to 2.7 V and the MAX value From: 5.5 V to 4.35 V in the *Electrical Characteristics* table ... 11
- Deleted t_{WD} Watchdog Timer from the *Timing Requirements* table ... 12
- Deleted t_{ST} row for TPS25741A in the *Switching Characteristics* table ... 13
- Deleted the last sentence from the *Sleep Mode* section: "The TPS25741 will wake up every t_{WD} and check for a connection before returning to sleep mode" ... 38
- Added test: "The TPS25740/TPS25740A Design Calculator Tool.." to the *Application Information* section ... 39
- Added sentence "All slew rate control methods" to the *Voltage Transition Requirements* section ... 44
- Deleted the *Enabling Power Muxing Architecture* section ... 47
- Added text: "The following example is based on TPS25741..." to the A/C Multiplexing Power Source section ... 47
- Deleted Q4 and Note from Figure 50 ... 47
- Changed From: A 400 pF, 50 V, ±5% COG/NPO ceramic To: A 470 pF, 50 V, ±5% COG/NPO ceramic in the *Configurable Components* section ... 48
- Changed From: R_F/C_F: Not used To: R_F/C_F: Provide filtering of both ripple... in the *Configurable Components* section ... 48
- Changed From: A 400 pF, 50 V, ±5% COG/NPO ceramic To: A 470 pF, 50 V, ±5% COG/NPO ceramic in the *Configurable Components* section ... 53
- Added document links to the *Documentation Support* section ... 60

Changes from Revision A (September 2016) to Revision B **Page**

- Added row to Input resistance for TPS25741A in the *Electrical Characteristics* table ... 10
- Changed the Test Conditions t_{WD} Watchdog Timer From: CC pins floating To: CC pins floating (TPS25741) in the *Timing Requirements* table ... 12
- Added TPS25741 to the test conditions for t_{ST} in the *Switching Characteristics* table. Added row to t_{ST} for TPS25741A in the test conditions and TYP value of 30 ms in the *Switching Characteristics* table ... 13
- Changed the last sentence of the *Sleep Mode* section: From: "The TPS25741/TPS25741A will also wake up every t_{WD} and check for a connection before returning to sleep mode." To: "The TPS25741 will wake up every t_{WD} and check for a connection before returning to sleep mode ... 38
- Changed section title From: VOUT Ripple Filtering using RF and CF To: Tuning OCP Using RF and CF. Updated section text ... 46
- Added Note to Q4 of Figure 50 ... 47
- Changed section title From: Dual-Port A/C Power Source (Wall Adaptor) To: Dual-Port Power Managed A/C Power Source (Wall Adaptor) ... 56

Changes from Original (August 2016) to Revision A **Page**

- Changed from Product Preview to Production Data for the TPS25741 ... 1

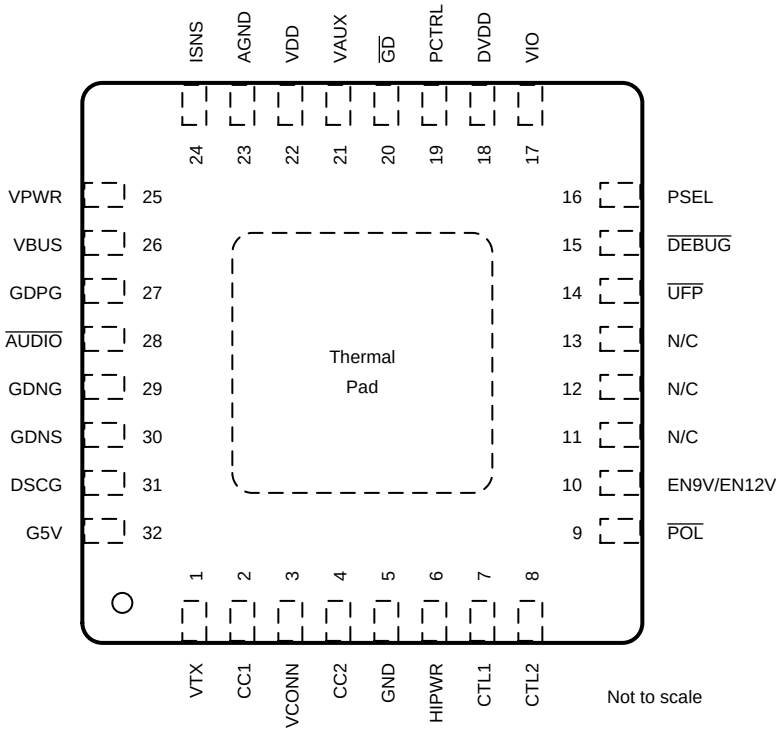
5 Device Comparison Table

DEVICE NUMBER	VOLTAGE OPTION
TPS25741	Offers 5 V, 12 V, and 20 V
TPS25741A(1)	Offers 5 V, 9 V, and 15 V

(1) Product Preview. Contact TI factory for more information.

6 Pin Configuration and Functions

RSM Package
32-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AGND	23	—	Analog ground is associated with monitoring and power conditioning circuits. Connect to GND and PAD.
AUDIO	28	O	Low when an audio accessory is present, high-z otherwise.
CC1	2	I/O	Multifunction configuration channel interface pin to USB Type-C. Functions include connector polarity, end-device connection detect, current capabilities, and Power Delivery communication.
CC2	4	I/O	Multifunction configuration channel interface pin to USB Type-C. Functions include connector polarity, end-device connection detect, current capabilities, and Power Delivery communication.
CTL1	7	O	Digital output pin used to control an external voltage regulator.
CTL2	8	O	Digital output pin used to control an external voltage regulator.
DEBUG	15	O	Low when a debug accessory is present, high-z otherwise.
DSCG	31	O	Discharge is an open-drain output that discharges the system V_{BUS} line through an external resistor.
DVDD	18	O	Internally regulated 1.85 V rail for external use up to 35 mA. Connect this pin to GND via the recommended bypass capacitor.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
EN9V/EN12V	10	I	For TPS25741: If it is pulled high, then the 12 V PDO may be transmitted. If it is pulled low, the 12-V PDO will not be advertised. For TPS25741A: If it is pulled high, then the 9 V PDO may be transmitted. If it is pulled low, the 9-V PDO will not be advertised.
GDPG	27	O	High-voltage open drain gate driver which may be used to drive PMOS power switches.
G5V	32	O	Analog gate drive output for an external NMOS power switch.
$\overline{GD}$	20	I	Master enable for the GDNG/GDNS gate driver. The system can drive this low to force the power path switch off.
GDNG	29	O	High-voltage open drain gate driver which may be used to drive NMOS power switches. Connect to the gate terminal.
GDNS	30	O	High-voltage open drain gate driver which may be used to drive NMOS power switches. Connect to the source terminal.
GND	5	—	Power ground is associated with power management and gate driver circuits. Connect to AGND and PAD.
HIPWR	6	I	Four-state input pin used to configure the voltages and currents that will be advertised. It may be connected directly to GND or DVDD, or it may be connected to GND or DVDD via a resistance R_{SEL}.
ISNS	24	I	The ISNS input is used to monitor a VBUS-referenced sense resistor for over-current events.
PCTRL	19	I	Input pin used to control the power that will be advertised. It may be pulled high or low dynamically.
$\overline{POL}$	9	O	Low when a UFP is connected on CC2, high-z otherwise.
PSEL	16	I	A four-state input used for selecting the maximum power that can be provided. It may be connected directly to GND or DVDD, or it may be connected to GND or DVDD via a resistance R_{SEL}
$\overline{UFP}$	14	O	Digital output pin used to indicate that either CC1 or CC2 (but not both) is pulled down by a USB Type-C Sink.
VAUX	21	O	Internally regulated rail for use by the power management circuits. Connect this pin to GND via the recommended bypass capacitor.
VBUS	26	I	The voltage monitor for the V_{BUS} line. The USB connector V_{BUS} line is the high-side power conductor.
VCONN	3	I	The voltage applied to this pin will be internally current limited and routed through the TPS25741 to the CCx pin that is not connected to the CC wire in the USB cable once the $\overline{UFP}$ pin is pulled low. Connect this pin to GND via the recommended bypass capacitor.
VDD	22	I	Optional input supply.
VIO	17	I	Connect VIO to the DVDD pin.
VPWR	25	I	Connect to an external voltage as a source of bias power. If VDD is supplied, this supply is optional while is $\overline{UFP}$ high.
VTX	1	O	Bypass pin for transmit driver supply. Use a 0.1-µF ceramic capacitor.
N/C	11		Connect to GND.
N/C	12		Connect to GND.
N/C	13		Connect to GND.
THERMAL PAD			Connect PAD to GND / AGND plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage (sustained)	$\overline{\text{AUDIO}}$, VDD , EN12V, EN9V, CTL1, CTL2, $\overline{\text{UFP}}$, PCTRL, CC1, CC2, $\overline{\text{DEBUG}}$, $\overline{\text{POL}}$, VIO	–0.3	6	V
	VTX(2)	–0.3	2.1	V
	VAUX(2)	–0.3	4.5	V
	$\overline{\text{GD}}$ (3)	–0.3	7	V
	HIPWR, PSEL, DVDD(2)	–0.3	2.1	V
	GDPG	–0.3	30	V
	G5V	–0.3	20	V
	GDNG(2)	–0.5	40	V
	VCONN	–0.3	7	V
	VBUS,VPWR, ISNS, DSCG, GDNS	–0.5	30	V
Pin voltage (transient for 1 ms)	VBUS,VPWR, ISNS, DSCG, GDNS	–1.5	30	V
Pin-to-pin voltage	$V_{(GDNG)} – V_{(GDNS)}$	–0.3	20	V
	AGND to GND	–0.3	0.3	V
	ISNS to VBUS	–0.3	0.3	V
Sinking current (average)	$\overline{\text{AUDIO}}$, GDPG		3.5	mA
	CTL1, CTL2, $\overline{\text{UFP}}$, $\overline{\text{DEBUG}}$, $\overline{\text{POL}}$		8	mA
	$\overline{\text{GD}}$		100	µA
	DSCG		10	mA
Sinking current (transient, 50 ms pulse 0.25% duty cycle)	DSCG		375	mA
Current sourcing	VTX, VCONN, CC1, CC2	Internally limited		mA
	VAUX	0	25	µA
Operating junction temperature range, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply voltage to these pins.
(3) Voltage allowed to rise above Absolute Maximum provided current is limited.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC (3) 61000-4-2 contact discharge, CC1, CC2	±8000	
		IEC (4) 61000-4-2 air-gap discharge, CC1, CC2	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
(4) These results were passing limits that were obtained on an application-level test board. Individual results may vary based on implementation. Surges per IEC61000-4-2, 1999 applied between CC1/CC2 and output ground of TPS25741EVM-802 and TPS25741AEVM-802

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply Voltage	VCONN	4.65		5.5	V
		VDD	0		5.5	V
		VPWR	4.65		25	V
V_I	Applied Voltage	$\overline{AUDIO}$, EN9V, EN12V, PCTRL, CC1, CC2, CTL1, CTL2, $\overline{DEBUG}$, $\overline{POL}$	0		5.5	V
		$\overline{GD}$	0		6.5	V
		DSCG, GDNS, VBUS	0		25	V
		GDPG	0		25	V
		G5V	0		16	V
		HIPWR, PSEL	0		1.96	V
		EN9V, EN12V	1.36			V
V_{IH}	High-Level Input Voltage	PCTRL	1.65			V
		$\overline{GD}$	1.64			V
V_{IL}	Low-Level Input Voltage	EN9V, EN12V			0.53	V
		PCTRL			1.85	V
		$\overline{GD}$			1.81	V
I_S	Sinking Current	$\overline{AUDIO}$, GDPG			1	mA
		CTL1, CTL2, $\overline{UFP}$, $\overline{DEBUG}$, $\overline{POL}$			5	mA
		$\overline{GD}$			80	µA
		DSCG, transient sinking current 50ms pulse, 0.25% duty cycle			350	mA
		DSCG, average			5	mA
	Sourcing Current	VCONN		200	600	mA
C_S	Shunt capacitance	CC1, CC2 (C_{RX})	200	560	600	pF
		VBUS (C_{PDIN})			10	µF
		DVDD	0.198	0.22	0.242	µF
		VAUX	0.09	0.1	0.11	µF
		VTX	0.09	0.1	0.11	µF
		VCONN	10		220	µF
		VDD	0.09			µF
R_{PUD}	Pull up/down resistance	HIPWR, PSEL (direct to GND or direct to DVDD)	0		1	kΩ
		HIPWR, PSEL (R_{SEL})	80	100	120	kΩ
R_{DSCG}	Series resistance	Maximum V_{BUS} voltage of 25 V	80			Ω
		Maximum V_{BUS} voltage of 15 V	43			Ω
		Maximum V_{BUS} voltage of 6 V	20			Ω
T_J	Operating junction temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS25741 TPS25741A RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND;EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Comparator (VBUS)						
V_{BUS_RTH}	VBUS Threshold (Rising voltage)		4.25	4.45	4.65	V
V_{BUS_FTH}	VBUS Threshold (Falling voltage)		3.5	3.7	3.9	V
	VBUS Threshold (Hysteresis)			0.75		V
Power Supply (VDD, VPWR)						
V_{DD_TH}	VDD UVLO threshold	Rising voltage	2.8	2.91	2.97	V
		Falling voltage	2.8	2.86	2.91	
		Hysteresis, comes into effect once the rising threshold is crossed.		0.05		
V_{PWR_TH}	VPWR UVLO threshold	Rising voltage	4.2	4.45	4.65	V
		Falling voltage	3.5	3.7	3.9	
		Hysteresis, comes into effect once the rising threshold is crossed.		0.75		
	Supply current drawn from VDD in sleep mode	VPWR = 0 V, VDD = 5 V, CC1 and CC2 pins are open. T_J = 25°C		8.5		µA
		VPWR = 0 V, VDD = 3.3 V, CC1 and CC2 pins are open. T_J = 25°C		5.4		µA
		VPWR = 0 V, VDD = 5 V,CC1 pin open, CC2 pin tied to GND. T_J = 25°C		93		µA
	Supply current drawn from VPWR in sleep mode	VPWR = 5 V, VDD = 0 V, CC1 and CC2 pins are open. T_J = 25°C		8		µA
		VPWR = 5 V, VDD = 0 V, CC1 pin open, CC2 pin tied to GND. T_J = 25°C		89		µA
I_{SUPP}	Typical operating current (from VPWR and VDD)	Power Delivery Sourcing active, VBUS = 5 V, VPWR = 5 V, VDD = 3.3 V	1	1.8	3	mA
Over/Under Voltage Protection (VBUS)						
V_{FOVP}	Fast OVP threshold, always enabled	5 V Power Delivery contract	5.8	6.05	6.3	V
		12 V Power Delivery contract (TPS25741)	13.2	13.75	14.3	V
		20 V Power Delivery contract (TPS25741)	22.1	23.05	24.0	V
		9 V Power Delivery contract (TPS25741A)	10.1	10.55	11.0	V
		15 V Power Delivery contract (TPS25741A)	16.2	16.95	17.7	V

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND;EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SOVP}	Slow OVP threshold, disabled during voltage transitions. (see Figure 1)	5 V Power Delivery contract	5.5	5.65	5.8	V
		12 V Power Delivery contract (TPS25741)	13.1	13.4	13.7	V
		20 V Power Delivery contract (TPS25741)	21.5	22.0	22.5	V
		9 V Power Delivery contract (TPS25741A)	10	10.2	10.4	V
		15 V Power Delivery contract (TPS25741A)	16.3	16.5	17	V
V_{SUVP}	UVP threshold, disabled during voltage transitions (see Figure 1)	5 V Power Delivery contract	3.5	3.65	3.8	V
		12 V Power Delivery contract (TPS25741)	9.2	9.45	9.7	V
		20 V Power Delivery contract (TPS25741)	15.7	16.1	16.5	V
		9 V Power Delivery contract (TPS25741A)	6.8	6.95	7.1	V
		15 V Power Delivery contract (TPS25741A)	11.7	11.95	12.2	V
VAUX						
V_{VAUX}	Output voltage	0 ≤ I_{VAUX} ≤ $I_{VAUXEXT}$	2.875	3.2	4.1	V
	VAUX Current limit		1		5	mA
$I_{VAUXEXT}$	External load that may be applied to VAUX.				25	µA
DVDD						
V_{DVDD}	Output voltage	0 mA ≤ I_{DVDD} ≤ 35 mA, CC1 or CC2 pulled to ground via 5.1 kΩ, or both CC1 and CC2 pulled to ground via 1 kΩ	1.75	1.85	1.95	V
	Load Regulation	Overshoot from V_{DVDD}, 10-mA minimum, 0.198-µF bypass capacitor	1.7		2	V
		Undershoot from V_{DVDD}, 10-mA minimum, 0.198-µF bypass capacitor	1.7		2	V
	Current limit	DVDD tied to GND	40		150	mA
VTX						
	Output voltage	Not transmitting or receiving, 0 to 2 mA external load	1.050	1.125	1.200	V
	Current Limit	VTX tied to GND	2.5		10	mA
Gate Driver Disable ($\overline{GD}$)						
V_{GD_TH}	Input enable threshold voltage	Rising voltage	1.64	1.725	1.81	V
		Hysteresis		0.15		V
V_{GDC}	Internal clamp voltage	$I_{\overline{GD}}$ = 80 µA	6.5	7.5	8.5	V
R_{GD}	Internal pulldown resistance	From 0 V to 6 V	3	6	9.5	MΩ
Discharge (DSCG) (1)(2)						
V_{DSCGT}	ON state (linear)	I_{DSCG} = 100 mA	0.15	0.42	1	V
I_{DSCGT}	ON state (saturation)	V_{DSCG} = 4 V, pulsed testing	220	553	1300	mA
R_{DSCGB}	Discharge bleeder	While CC1 is pulled down by 5.1 kΩ and CC2 is open, V_{DSCG} = 25 V, compute V_{DSCG}/I_{DSCG}	6.6	8.2	10	kΩ
	Leakage current	0 V ≤ V_{DSCG} ≤ 25 V			2	µA
P-ch MOSFET Gate Driver (GDPG)						
I_{GDPG}	Sinking current (ON)	2 V ≤ V_{GDPG} ≤ 25 V	34	41	48	µA
I_{LGDPG}	Leakage current	0 V ≤ V_{GDPG} ≤ 25 V			2	µA
N-ch MOSFET Gate Driver (G5V)						
I_{G5VON}	Sourcing current	0 V ≤ V_{G5V} ≤ 9 V	6.6	10		µA
V_{G5VON}	Sourcing voltage (ON)	I_{G5V} ≤ 2 µA	10		16	V

(1) If T_{J1} is perceived to have been exceeded an OTSD occurs and the discharge FET is disabled.
(2) The discharge pull-down is not active in the sleep mode.

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND;EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{G5VOFF}	Sinking strength (OFF)	V_{G5V} = 1 V			200	Ω
	Sinking strength UVLO (safety)	V_{DD} = 1.3 V, V_{PWR} = 0 V, V_{G5V} = 1 V		288		µA
		V_{PWR} = 1.3 V, V_{DD} = 0 V, V_{G5V} = 1 V		343		µA
	Off-state leakage	V_{G5V} = 15V			2	µA
N-ch MOSFET Gate Driver (GDNG,GDNS)						
I_{GDNGON}	Sourcing current	0 V ≤ V_{GDNS} ≤ 25 V, 0 V ≤ V_{GDNG} – V_{GDNS} ≤ 6 V	13.2	20	30	µA
V_{GDNGON}	Sourcing voltage while enabled (V_{GDNG} – V_{GDNS})	0 V ≤ V_{GDNS} ≤ 25 V, I_{GDNGON} ≤ 4 µA, VPWR = 0 V	7		12	V
		0 V ≤ V_{GDNS} ≤ 25 V, I_{GDNGON} ≤ 4 µA, VDD = 0 V	8.5		12	V
$R_{GDNGOFF}$	Sinking strength while disabled	V_{GDNG} – V_{GDNS}= 0.5 V, 0 ≤ V_{GDNS} ≤ 25 V		150	300	Ω
	Sinking strength UVLO (safety)	VDD = 1.4 V, V_{GDNG} = 1 V, V_{GDNS} = 0 V, VPWR = 0 V		145		µA
		VDD = 1.4 V, V_{GDNG} = 1 V, V_{GDNS} = 0 V, VDD = 0 V		145		µA
	Off-state leakage	V_{GDNS} = 25 V, V_{GDNG} open			7	µA
Power Control Input (PCTRL)						
V_{PCTRL_TH}	Active threshold voltage(3)	Voltage rising	1.65	1.75	1.85	V
		Hysteresis		100		mV
	Input resistance	0 V ≤ V_{PCTRL} ≤ V_{VAUX}	1.5	2.9	6	MΩ
Voltage Select (HIPWR), Power Select (PSEL)(4)						
	Leakage current	0 V ≤ V_{HIPWR} ≤ V_{DVDD}, 0 V ≤ V_{PSEL} ≤ V_{DVDD}	–1		1	µA
Port Status and Voltage Control (CTL1, CTL2, $\overline{UFP}$, $\overline{POL}$, $\overline{DEBUG}$)(5)						
V_{OL}	Output low voltage	I_{OL} = 4 mA sinking			0.4	V
	Leakage Current (6)	In Hi-Z state, 0 ≤ V_{CTLx} ≤ 5.5 V or 0 ≤ $V_{\overline{UFP}}$ ≤ 5.5V	–0.5		0.5	µA
Presence of Audio Accessory ($\overline{AUDIO}$)(7)						
I_{AUD}	Current pull down	V_{AUDIO} = 1 V	34	40	46	kΩ
	Leakage current	0 V ≤ V_{AUDIO} ≤ 5.5 V			2	µA
Enable 9 V, 12 V Capability (EN9V, EN12V)(8)						
V_{ILGIO}	Input low threshold voltage				0.585	V
V_{IHGIO}	Input high threshold voltage		1.225			V
	Input hysteresis			0.25		V
Transmitter Specifications (CC1, CC2)						
R_{TX}	Output resistance (zDriver, refer to USB Power Delivery in *Documentation Support*)	During transmission	33	48	75	Ω
V_{TXHI}	Transmit high voltage	External Loading per Figure 28	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage	External Loading per Figure 28	–75		75	mV
Receiver Specifications (CC1, CC2)						
V_{RXHI}	Receive threshold (rising)		800	840	885	mV
V_{RXLO}	Receive threshold (falling)		485	525	570	mV
	Receive threshold (hysteresis)			315		mV

(3) When voltage on the PCTRL pin is less than $V_{(PCTRL\_TH)}$, the amount of power advertised is reduced by half.
(4) Leaving HIPWR or PSEL open is an undetermined state and leads to unpredictable behavior.
(5) These pins are high-z during a UVLO, reset, or in Sleep condition.
(6) The pins were designed for less leakage, but testing only verifies that the leakage does not exceed 1 µA.
(7) $\overline{AUDIO}$ is high-z during a UVLO, reset, or Device Sleep condition.
(8) Protection is provided against a voltage greater than V_{DVDD} being applied externally.

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND;EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Amplitude of interference that can be tolerated.	Interference is 600 kHz square wave, rising 0 to 100 mV.			100	mV
		Interference is 1 MHz sine wave			1	V_{PP}
DFP Specifications (CC1, CC2)						
V_{DSTD}	Detach threshold when cable is detached while in standard DFP mode.	In standard DFP mode(9), voltage rising	1.52	1.585	1.65	V
		Hysteresis		0.02		V
V_{D1p5}	Detach threshold when cable is detached.	In 1.5 A DFP mode(10), voltage rising	1.52	1.585	1.65	V
		Hysteresis		0.02		V
V_{D3p0}	Detach threshold when cable is detached	In 3 A DFP mode(11), voltage rising	2.50	2.625	2.75	V
		Hysteresis		0.05		V
V_{OCN}	Unloaded output voltage on CC pin	normal mode	2.7		4.35	V
V_{OCDS}		V_{PWR} = 0 V (in UVLO) or in sleep mode	1.8		5.5	V
I_{RPSTD}	Loaded output current while connected through CCx	In standard DFP mode(9), CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	64	80	96	µA
$I_{RP1.5}$	Loaded output current while connected through CCx	In 1.5 A DFP mode(10), CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	166	180	194	µA
$I_{RP3.0}$	Loaded output current while connected through CCx	In 3 A DFP mode(11), CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	304	330	356	µA
V_{RDSTD}	Ra, Rd detection threshold (falling)	In standard DFP mode(9), 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.15	0.19	0.23	V
		Hysteresis		0.02		V
$V_{RD1.5}$	Ra, Rd detection threshold (falling)	In 1.5 A DFP mode(10), CCy open 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.35	0.39	0.43	V
		Hysteresis		0.02		V
$V_{RD3.0}$	Ra, Rd detection threshold (falling)	In 3 A DFP mode(11), CCy open 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.75	0.79	0.83	V
		Hysteresis		0.02		V
V_{WAKE}	Wake threshold (rising and falling), exit from sleep mode	VPWR = 4.65 V , 0 V ≤ VDD ≤ 3 V	1.6		3.0	V
I_{DSDFP}	Output current on CCx in sleep mode to detect Ra removal.	CCx = 0V, CCy floating	40	73	105	µA
Connector Power Specifications (CC1, CC2, VCONN)(12)						
	UVLO for VCONN (13)	Turn-on, VCONN rising	2.2	2.4	2.6	V
		Hysteresis		0.1		V
R_{DSON}	Resistance from VCONN to CC1 or CC2(14)(15)	4.75 V ≤ V_{CONN} ≤ 5.5 V (Fixed Supply mode), I_{CCx} = 250 mA –40°C ≤ T_J ≤ 125°C		300	500	mΩ
		4.75 V ≤ V_{CONN} ≤ 5.5 V (Fixed Supply mode), I_{CCx} = 250 mA T_J = 25°C		300	350	mΩ
I_{OS}	Current limit measured on CC1 or CC2(16)	4.75 V ≤ V_{CONN} ≤ 5.5 V (Fixed Supply mode)	415	490	562	mA
	Fault threshold		1.1×I_{OS}		1.25×I_{OS}	mA

(9) Standard DFP mode is active after a USB Type-C sink, debug accessory, or audio accessory is attached until the first USB Power Delivery message is transmitted (after GDNG has been enabled).
(10) 1.5 A DFP mode is active after a USB Power Delivery contract has been negotiated.
(11) 3 A DFP mode is active after GDNG has been enabled until a USB Power Delivery message is received.
(12) VCONN is always applied when a UFP is attached, regardless of whether Ra is detected.
(13) The VCONN pin has reverse blocking.
(14) Based on 120 mV drop at 250 mA (to deliver more than 1 W at VCONN = 4.75 V).
(15) There are requirements for the VCONN voltage supplied to CC1 or CC2 in [1]; customers need to take the R_{DSON} into account when designing to meet those requirements.
(16) While providing VCONN power, the CCx output is monitored for faults (overloads). Thermal shutdown is provided with thermal cycling (auto-restart).

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND;EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over-Current Protection (ISNS, VBUS)						
V_{ITRIP}	Current trip shunt voltage	Specified as $V_{ISNS} – V_{BUS}$. The OCP trip point setting assumes the sense resistor is 5 mΩ				
		HIPWR: 5 A not enabled	19.2		22.6	mV
		HIPWR: 5 A enabled	29		34	mV
OTSD						
T_{J1}	Die Temperature (Analog)(17)	T_J ↑	125	135	145	°C
		Hysteresis		10		
T_{J2}	Die Temperature (Analog)(18)	T_J ↑	140	150	163	°C
		Hysteresis		10		

(17) When T_{J1} trips a hard reset is transmitted and discharge is disabled, but the bleeder discharge is not disabled.
(18) T_{J2} trips only when some external heat source drives the temperature up. When it trips the DVDD, and VAUX power outputs are turned off.

7.6 Timing Requirements

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3.0 V ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND, EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted).

			MIN	NOM	MAX	UNIT
t_{FOVPDG}	Deglitch for fast over-voltage protection			9		µs
t_{OCP}	Deglitch Filter for over-current protection				15	µs
	Time power is applied until CC1 and CC2 pull-ups are applied.	$V_{VPWR} > V_{PWR\_TH}$ OR $V_{VDD} > V_{DD\_TH}$		2.5	4	ms
t_{CC}	Falling/Rising voltage deglitch time for detection on CC1 and CC2			120		µs
Transmitter Specifications (CC1, CC2)						
t_{UI}	Bit unit interval		3.05	3.3	3.70	µs
	Rise/fall time, t_{Fall} and t_{Rise} (refer to USB Power Delivery in *Documentation Support*)	External Loading per Figure 28	300		600	ns

7.7 Switching Characteristics

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3.0 V ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND, EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VP}	Delay from enabling external NFET until under-voltage and OCP protection are enabled	VBUS = GND		190		ms
t_{STL}	Source settling time, time from CTL1 and CTL2 being changed until a PS_RDY USB Power Delivery message is transmitted to inform the sink is may draw full current per USB Power Delivery in *Documentation Support*.			260		ms
t_{SR}	Time that VBUS is held low after a hard reset. This is $t_{SrcRecover}$ in USB Power Delivery in *Documentation Support*.	$T_J > T_{J1}$		765		ms
t_{HR}	Time after hard reset is transmitted until GDNG is disabled. This is $t_{PSHardReset}$ in USB Power Delivery in *Documentation Support*.			30		ms

Switching Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3.0 V ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND, EN9V = GND; EN12V = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CCDeb}	Time until $\overline{UFP}$ or $\overline{AUDIO}$ or $\overline{DEBUG}$ is pulled low after an attachment, this is the USB Type-C required debounce time for attachment detection called $t_{CCDebounce}$ [1].			185		ms
t_{ST}	Delay after sink request is accepted until CTL1 and/or CTL2 is changed. This is called $t_{SnkTransition}$ in USB Power Delivery in *Documentation Support*.			30		ms
t_{FLT}	The time in between hard reset transmissions in the presence of a persistent supply fault.	$\overline{GD}$ = GND or VPWR = GND, sink attached		1395		ms
t_{SH}	The time in between retries (hard reset transmissions) in the presence of a persistent VBUS short.	VBUS = GND, sink attached		985		ms
t_{ON}	The time from $\overline{UFP}$ being pulled low until a hard reset is transmitted. Designed to be greater than $t_{SrcTurnOn}$ in USB Power Delivery in *Documentation Support*.	$\overline{GD}$ = 0 V or VPWR = 0 V		600		ms
	Retry interval if USB Power Delivery sink stops communicating without being removed or if sink does not communicate after a fault condition. Time GDNG remains enabled before a hard reset is transmitted. This is the $t_{NoResponse}$ time in USB Power Delivery in *Documentation Support*.	Sink attached		4.8		s
t_{DVDD}	Delay before DVDD is driven high	After sink attached			5	ms
t_{GDoff}	Turnoff delay, time until V_{GDNG} is below 10% of its initial value after the $\overline{GD}$ pin is low.	$V_{\overline{GD}}$: 5 V → 0 V in < 0.5 µs.			5	µs
t_{FOVP}	Response time when VBUS exceeds the fast-OVP threshold	VBUS ↑ to GDNG OFF (V_{GDNG} below 10% its initial value)			30	µs
	OCP large signal response time	5 A enabled, V_{ISNS} – V_{VBUS}: 0 V → 42 mV measured to GDNG transition start.			30	µs
	Time until discharge is stopped after T_{J1} is exceeded.	0 V ≤ V_{DSCG} ≤ 25 V			10	µs
	Digital output fall time	V_{PULLUP} = 1.8 V, C_{Load} = 10 pF, R_{PULLUP} = 10 kΩ, $V_{(CTLx)}$ or $V_{\overline{UFP}}$: 70% V_{PULLUP} → 30% V_{PULLUP}	20		300	ns
t_{VCON}	VCONN turn-on time	Measured from when $\overline{UFP}$ is pulled low until VCONN FET is enabled.			2	ms
	VBUS turn-on time	Measured from when $\overline{UFP}$ is pulled low until GDNG begins sourcing its full current			2	ms

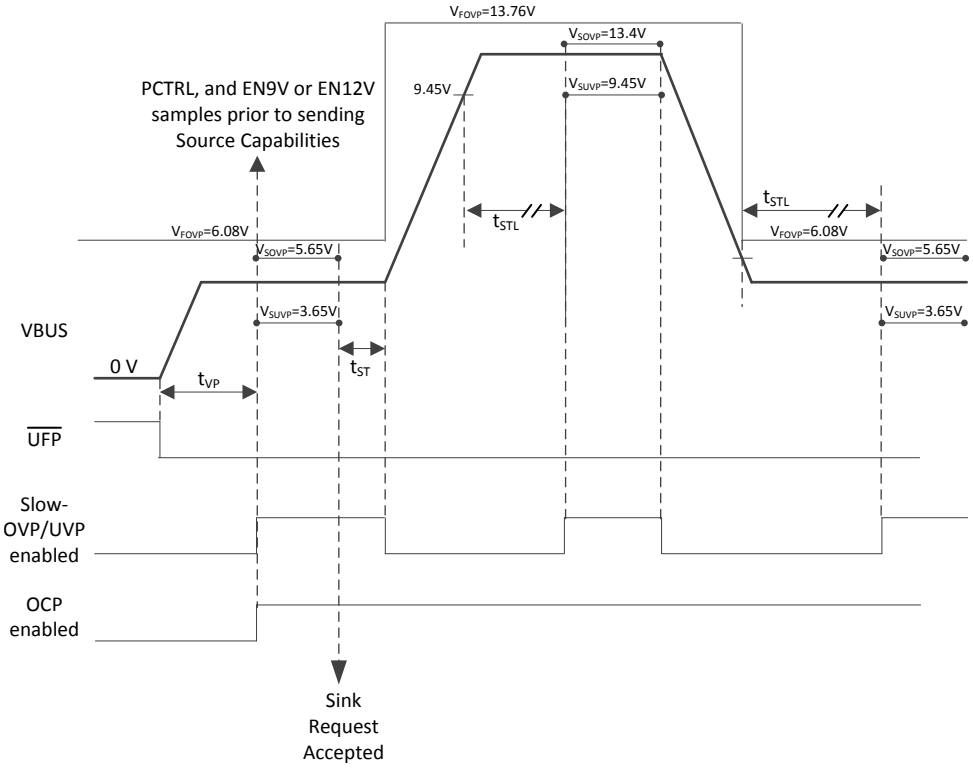


Figure 1. Timing Diagram for t_{VP}, t_{ST}, and t_{STL}, After Sink Attachment. V_{SOVP} and V_{SUVP} are Disabled Around Voltage Transitions

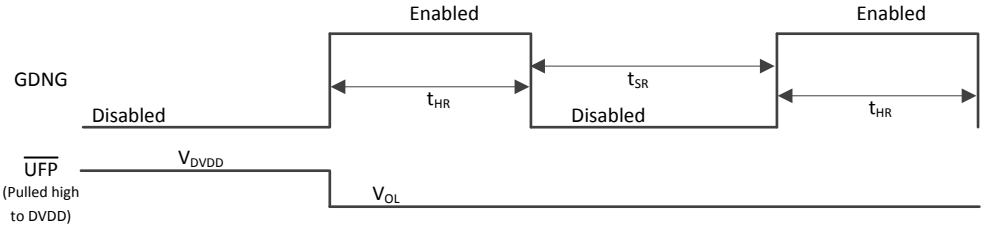


Figure 2. Timing Diagram for t_{HR} and t_{SR}, After Sink Attachment with $T_J > T_{J1}$

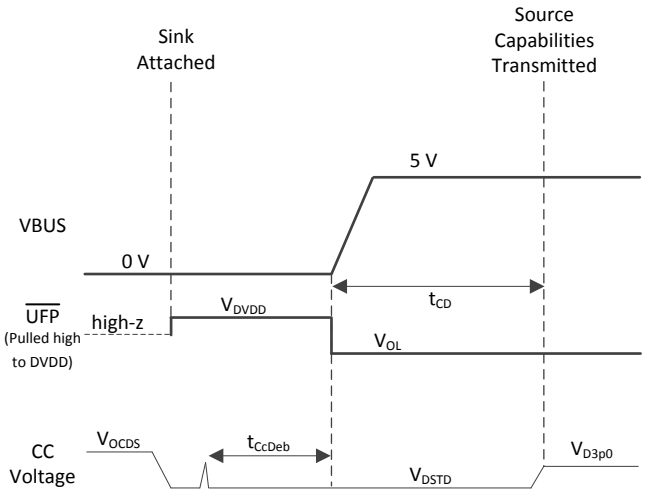


Figure 3. Timing Diagram for t_{CCDeb} and t_{CD}, Under Persistent Fault Condition

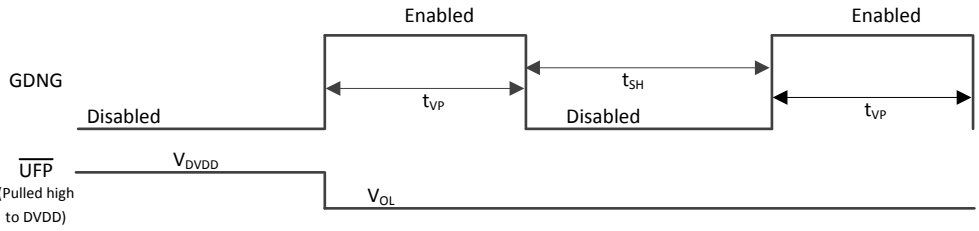


Figure 4. Timing Diagram for t_{SH} and t_{VP}, with VBUS Shorted to Ground

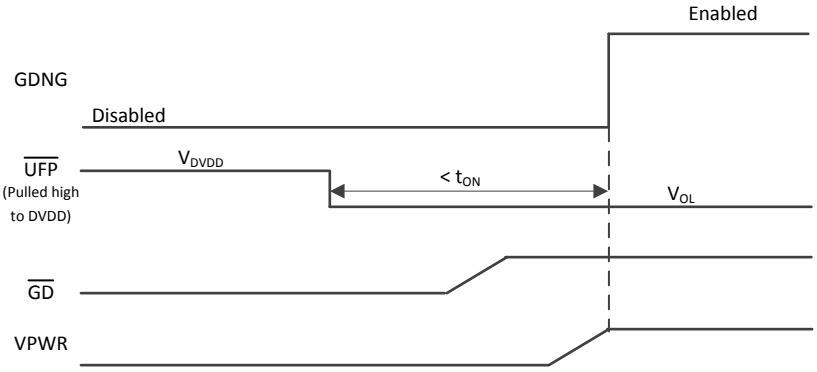


Figure 5. Timing Diagram for t_{ON}

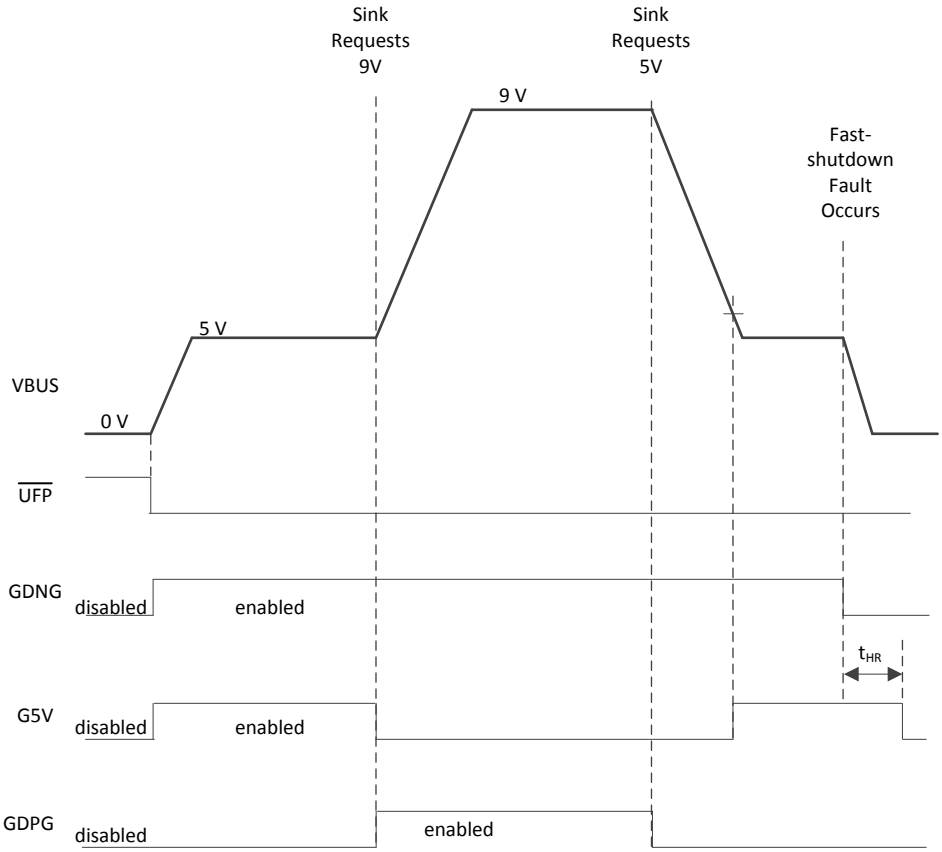
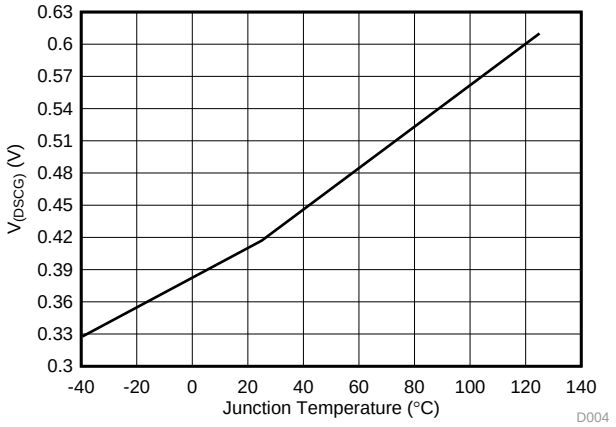


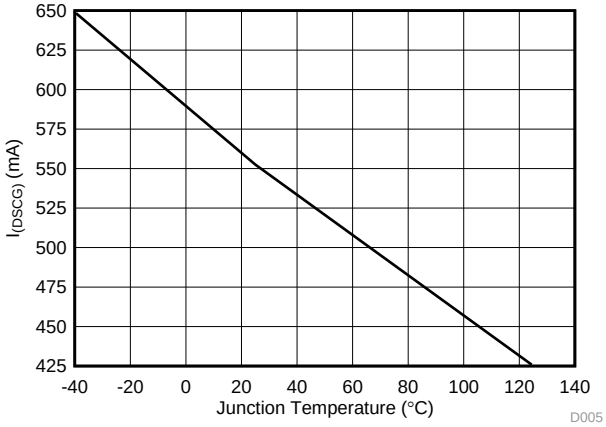
Figure 6. Timing Diagram for GDPG, G5V, and GDNG with Fast-Shutdown Fault

7.8 Typical Characteristics



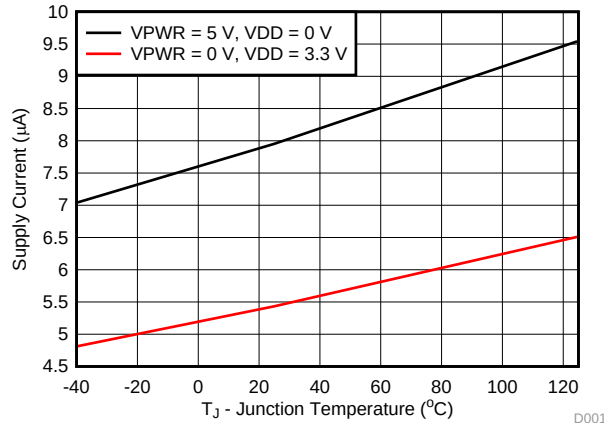
I_{DSCG} = 100 mA

Figure 7. V_{DSCG} when V_{PWR} > 4.65 V



V_{DSCG} = 4 V pulsed testing

Figure 8. I_{DSCG} when V_{PWR} > 4.65 V



CC pins are open

Figure 9. Supply Current when V_{PWR} = 5 V

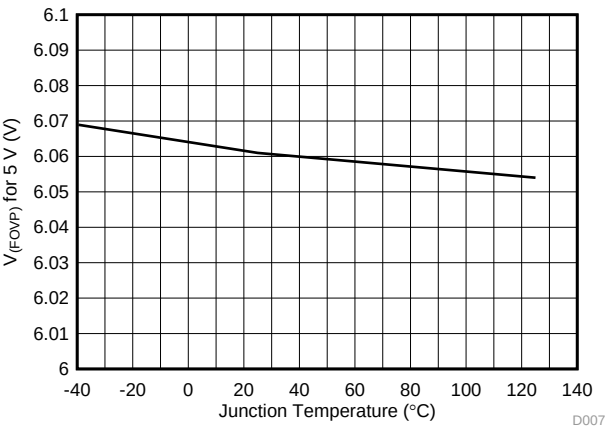


Figure 10. V_{FOVP} While Supplying 5 V

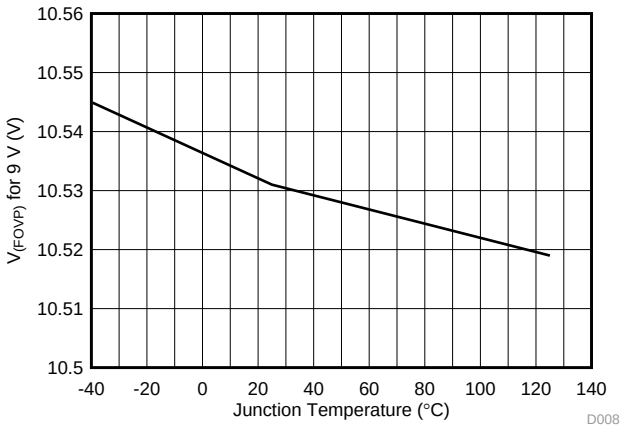


Figure 11. V_{FOVP} While Supplying 9 V, TPS25741A

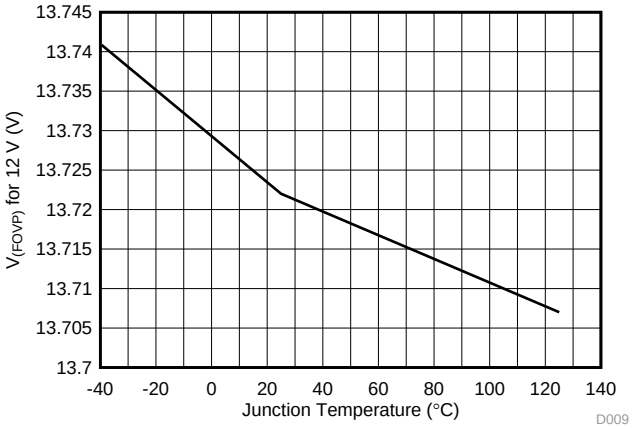


Figure 12. V_{FOVP} While Supplying 12 V, TPS25741

Typical Characteristics (continued)

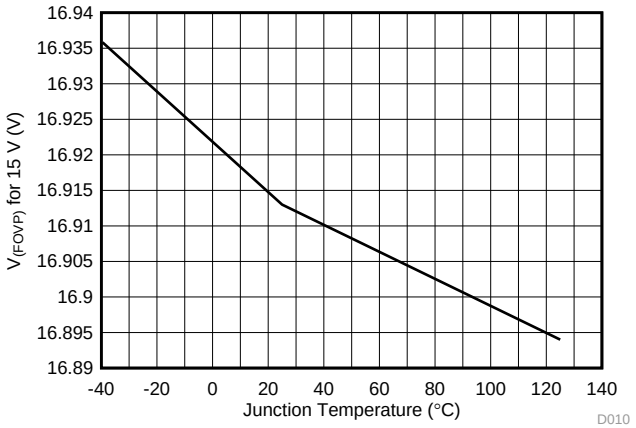


Figure 13. V_{FOVP} While Supplying 15 V, TPS25741A

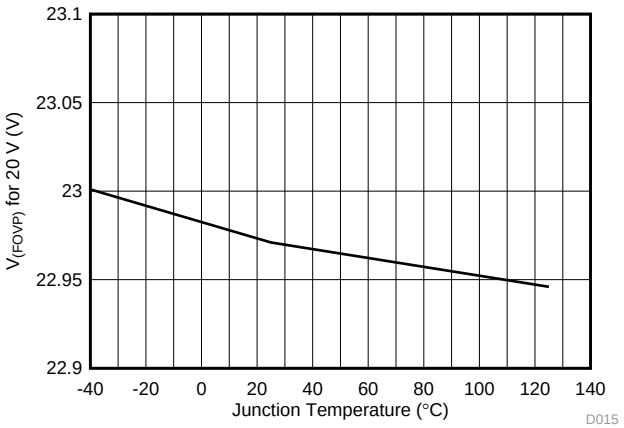
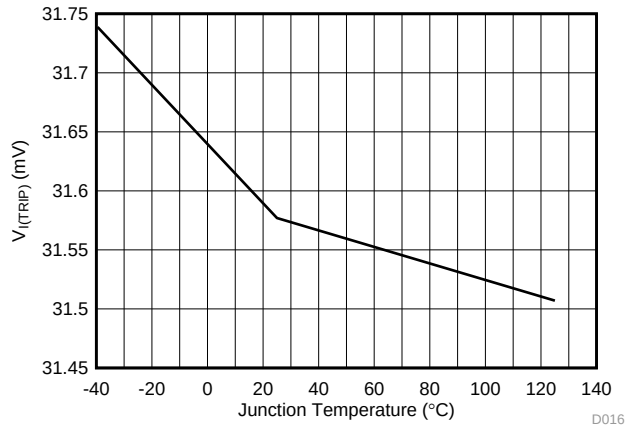
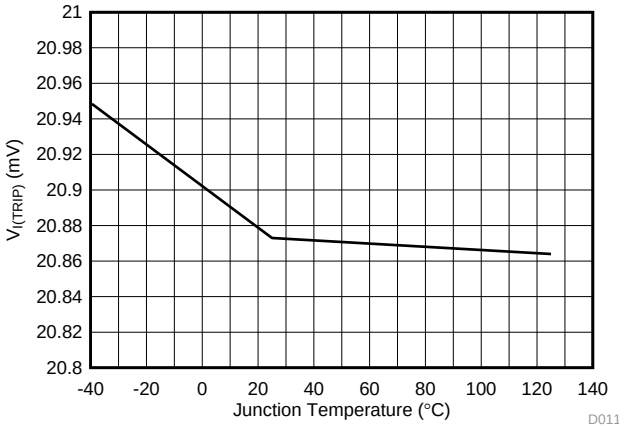


Figure 14. V_{FOVP} While Supplying 20 V, TPS25741



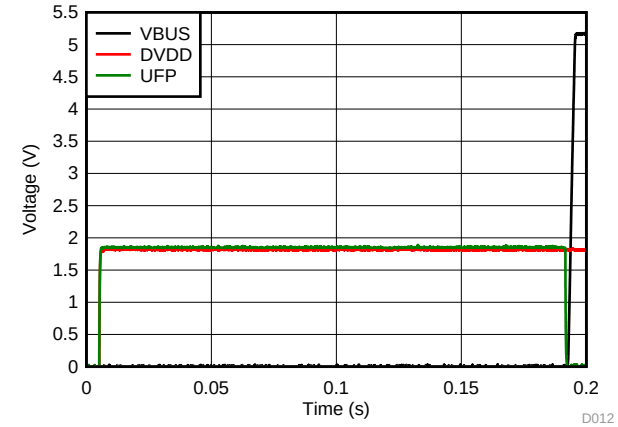
5 A enabled

Figure 15. V_{ITRIP} When V_{PWR} > 4.65 V



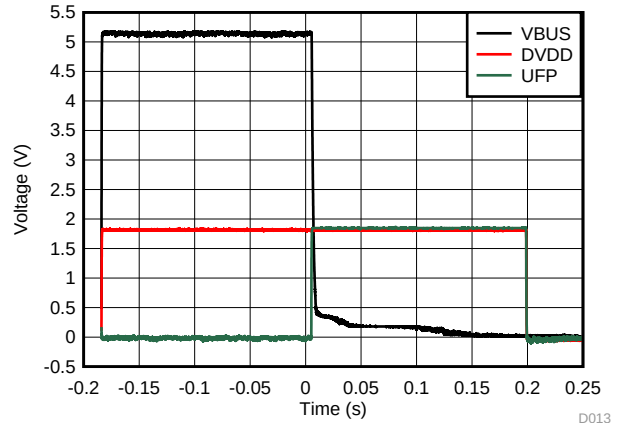
3 A enabled

Figure 16. V_{ITRIP} When V_{PWR} > 4.65 V



Sink attached at time 0
$\overline{UFP}$ pulled up to DVDD

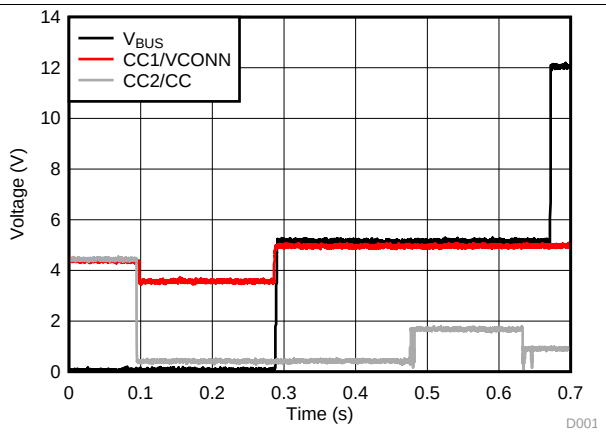
Figure 17. DVDD and $\overline{UFP}$ Upon Sink Attachment



Sink detached at time 0.19s
Sleep mode entered at time 0.39s.
$\overline{UFP}$ pulled up to DVDD

Figure 18. DVDD and $\overline{UFP}$ Upon Sink Attachment

Typical Characteristics (continued)



VDD = 5 V

Figure 19. VBUS, CC1, and CC2 Upon Attachment

8 Detailed Description

8.1 Overview

The TPS25741/TPS25741A and supporting circuits perform the functions required to implement a USB Power Delivery 2.0 Power Delivery as a provider-only and a USB Type-C revision 1.2 source. It uses its CC pins to detect the attachment of a sinking device or upward facing port (UFP) and to determine which of CC1 or CC2 is connected to the CC wire of the cable. It will then communicate over the CC wire in the cable bundle using USB Power Delivery to offer a set of voltages and currents. USB Power Delivery is a technology that utilizes the ubiquitous USB communications and hardware infrastructure to extend the amount of power available to devices from the 7.5 W range for USB BC1.2 to as high as 100 W in a dock. It is a compatible overlay to USB 2.0 and USB 3.0, coexisting with the existing 5 V powered universe of devices by use of adapter cables. Some basic characteristics of this technology relevant to the TPS25741/TPS25741A include:

- Increased power achieved by providing higher current and/or higher voltage.
- New 3 A cable and 5 A connector to support greater than the traditional 1.5 A.
  - Cables have controlled voltage drop
- Voltages greater than 5 V are negotiated between Power Delivery partners.
  - Standard 5 V is always the default source voltage.
  - Voltage and current provisions are negotiated between Power Delivery partners.
- Power Delivery partners negotiate over the CC line to avoid conflict with existing signaling (that is, D+, D-)
- Layered communication protocol defined including PHY, Protocol Layer, Policy Engine, and Device Policy Manager all implemented within the TPS25741/TPS25741A.
- The Type-C connector standard implements pre-powerup signaling to determine:
  - Connector orientation
  - Source 5-V capability
  - Detect through connection of a UFP (upward facing port) to a DFP (downward facing port)
  - Detection of when the connected UFP is disconnected. V_{BUS} is unpowered until a through-connection is present

Figure 20, Figure 21, and Figure 22 show typical configurations for the TPS25741/TPS25741A.

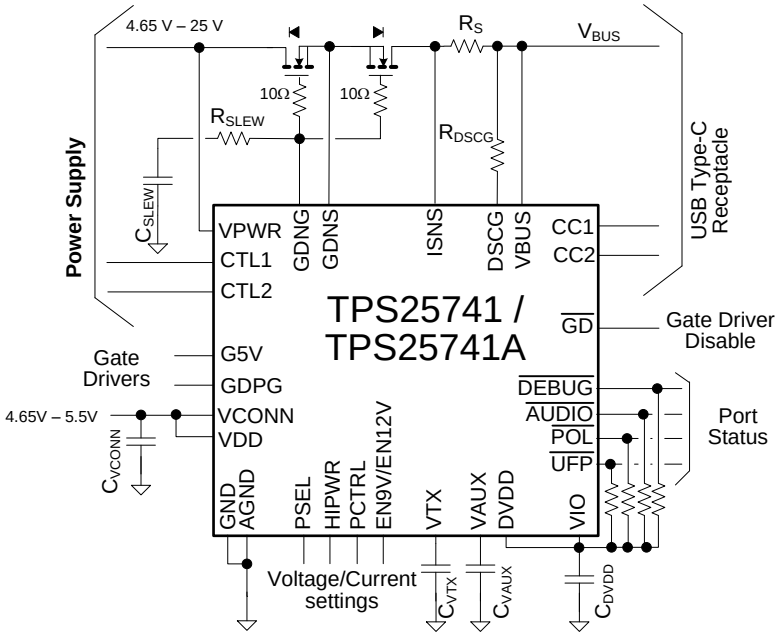


Figure 20. Reference Schematic 1

Overview (continued)

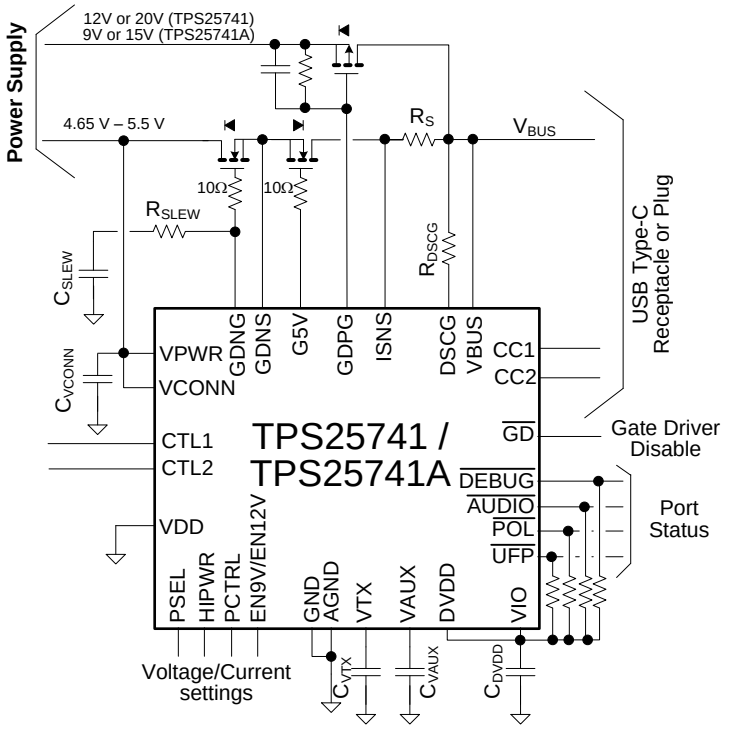


Figure 21. Reference Schematic 2

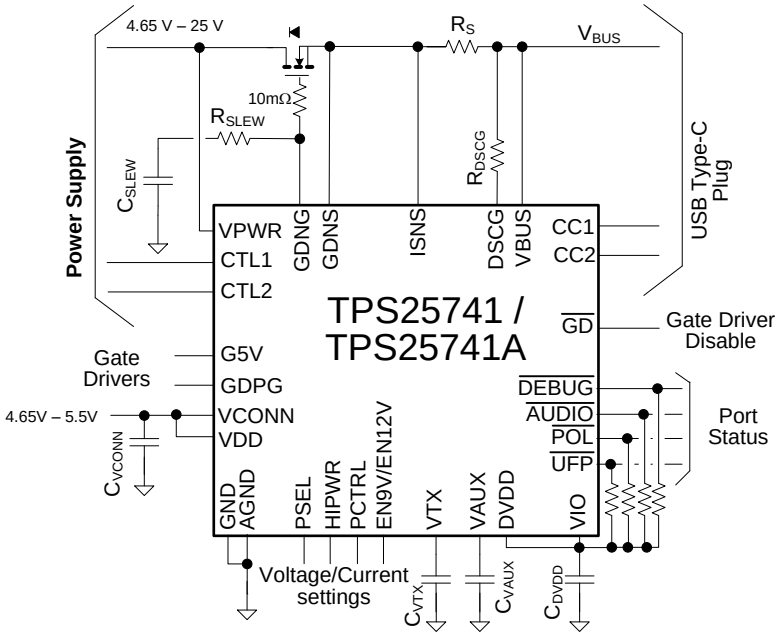


Figure 22. Reference Schematic 3

Overview (continued)

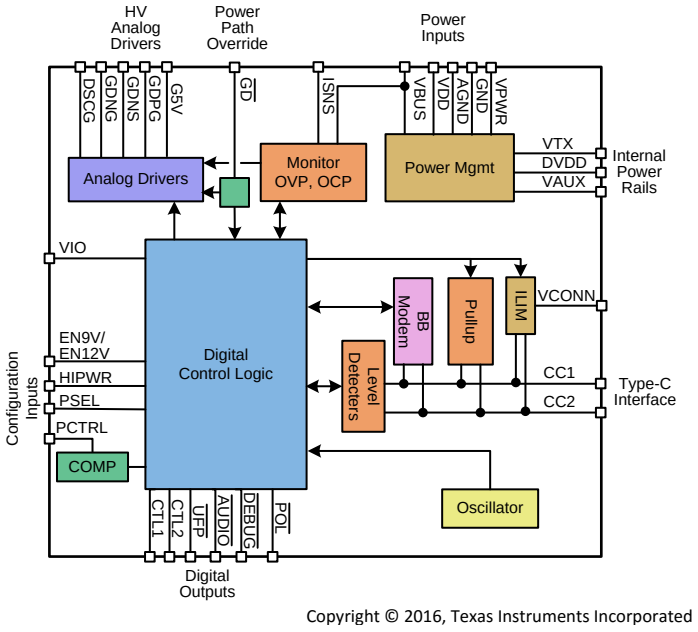
8.1.1 VBUS Capacitance

The USB Type-C specification requires that the capacitance on the V_{BUS} pin of an empty receptacle be below 10 µF. This is to protect legacy USB sources that are not designed to handle the larger inrush capacitance and which may be connected via an A-to-C cable. For applications with USB Type-C receptacles and large bulk capacitance, this means back-to-back blocking FETs are required as shown in Figure 20. However, for applications with a USB Type-C plug this requirement does not apply since an adaptor cable with a USB Type-C receptacle and a Type-A plug is not defined or allowed by the USB I/F.

8.1.2 USB Data Communications

The USB Power Delivery specification requires that sources such as the TPS25741/TPS25741A advertise in the source capabilities messages they transmit whether or not they are in a product that supports USB data communications. The TPS25741/TPS25741A is designed for systems with data communication, so it has this bit hard-coded to 1.

8.2 Functional Block Diagram



8.3 Feature Description

This section describes the features associated with each pin for the TPS25741 and TPS25741A.

8.3.1 USB Type-C CC Logic (CC1, CC2)

The TPS25741/TPS25741A uses a current source to implement the pull up resistance USB Type-C requires for Sources. While waiting for a valid connection, the TPS25741/TPS25741A applies a default pullup of I_{RPSTD}. A sink attachment is detected when the voltage on one (not both) of the CC pins remains between V_{RDSTD} and V_{DSTD} for t_{CcDeb} and the voltage on the VBUS pin is below V_{BUS_FTH}. Then after turning on VBUS and disabling the Rp current source and applying VCONN to the CCx pin not connected through the cable, the TPS25741/TPS25741A applies $I_{RP3.0}$ to advertise 3A to non-Power Delivery sinks. Finally, if it is determined that the attached sink is Power Delivery-capable, the TPS25741/TPS25741A applies $I_{RP1.5}$. During this sequence if the voltage on the monitored CC pin exceeds the detach threshold then the TPS25741/TPS25741A removes VBUS and begins watching for a sink attachment again.

The TPS25741 or TPS25741A digital logic selects the current source switch as illustrated in Figure 23.

Feature Description (continued)

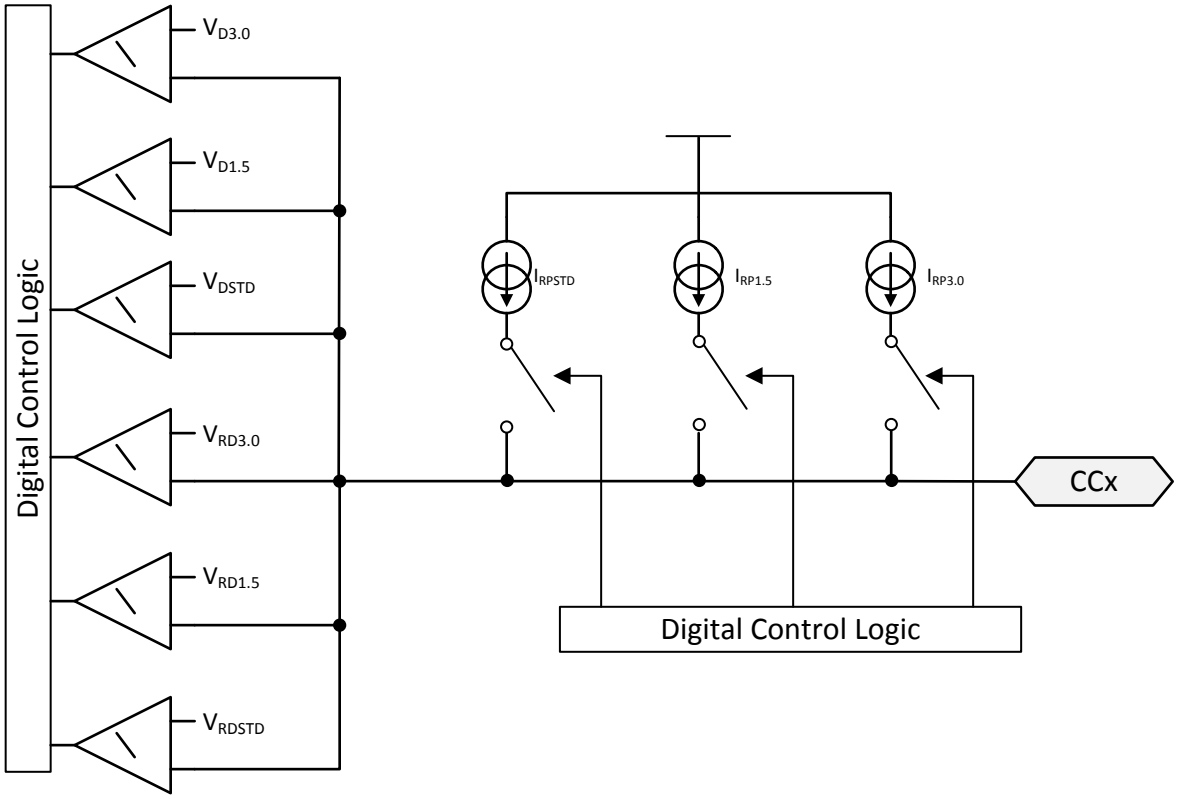


Figure 23. USB Type-C Rp Current Sources and Detection Comparators

If the voltage on both CC pins remains above V_{RDSTD} for t_{CcDeb}, then the TPS25741 or TPS25741A goes to the sleep mode. In the sleep mode a less accurate current source is applied and less accurate comparator watches for attachment (see V_{WAKE}, and I_{DSDFP}).

8.3.2 9.3.2 VCONN Supply (VCONN, CC1, CC2)

Once a sink attachment is detected and the power supply is ready, the TPS25741/TPS25741A applies VCONN to either CC1 or CC2. VCONN is passed through to whichever of CC1 or CC2 is not connected to the sink via the CC wire in the cable.

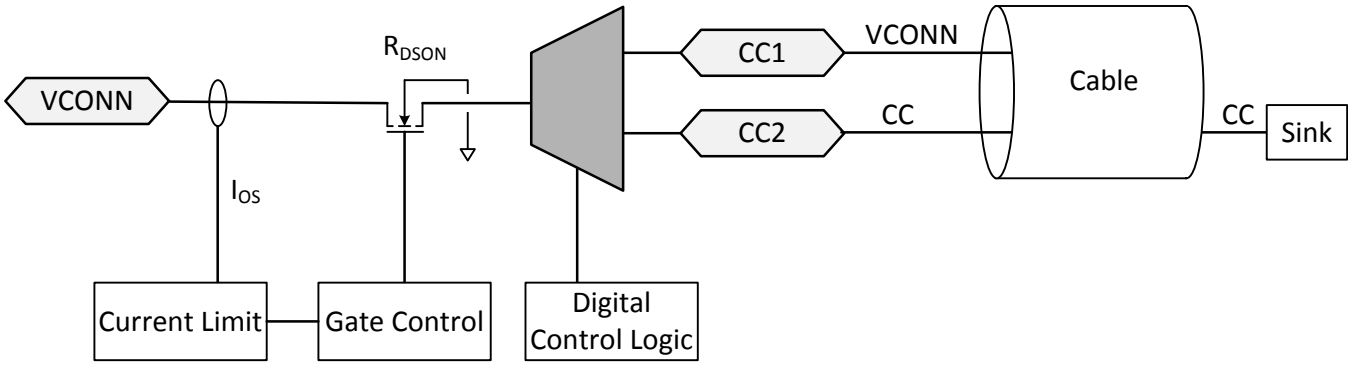


Figure 24. VCONN Current-Limiting Switch

Feature Description (continued)

8.3.3 USB Power Delivery BMC Transmission (CC1, CC2, VTX)

An example of the BMC signal, specifically the end of the preamble and beginning of start-of-packet (SOP) is shown below. There is always an edge at the end of each bit or unit interval, and ones have an edge half way through the unit interval.

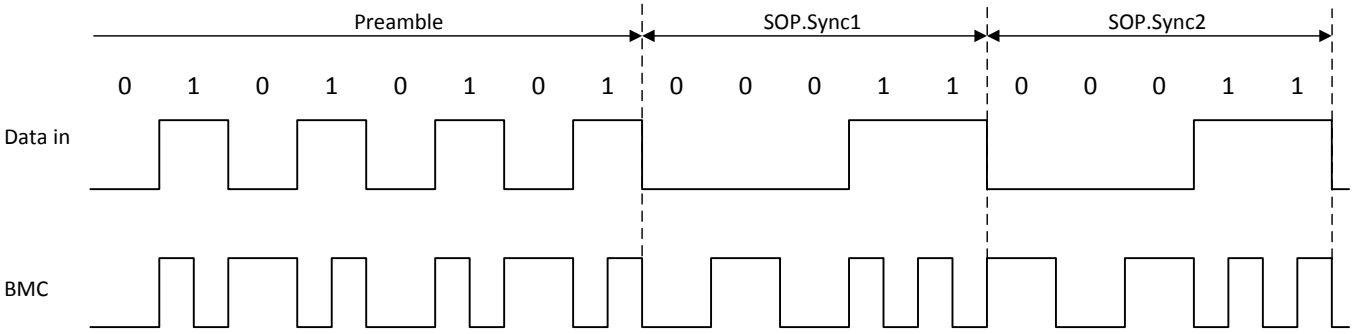


Figure 25. BMC Encoded End of Preamble, Beginning of SOP

While engaging in USB Power Delivery communications, the TPS25741 or TPS25741A is applying $I_{RP1.5}$ or $I_{RP3.0}$, so the CC line has a DC voltage of 0.918 V or 1.68 V, respectively. When the BMC signal is transmitted on the CC line, the transmitter overrides this DC voltage as shown in Figure 26. The transmitter bias rail (VTX) is internally generated and may not be used for any other purpose in the system. The VTX pin is only high while the TPS25741 or TPS25741A is transmitting a USB Power Delivery message.

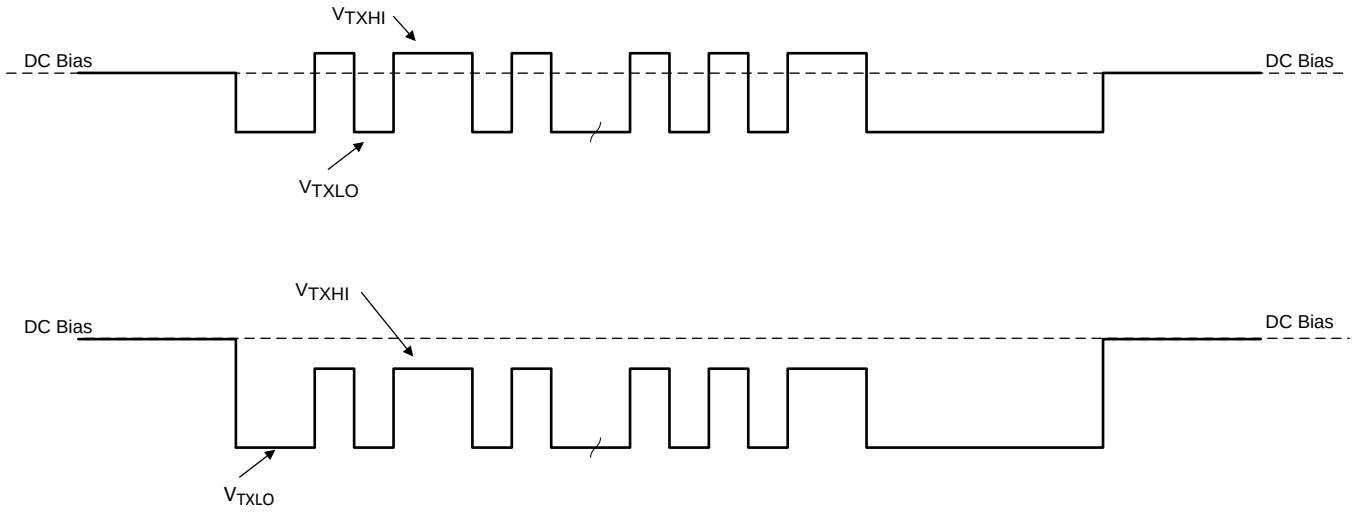


Figure 26. USB Power Delivery BMC Transmission on the CC Line

The device transmissions meet the eye diagram requirements from USB Power Delivery in *Documentation Support*. Figure 27 shows the transmitter schematic.

Feature Description (continued)

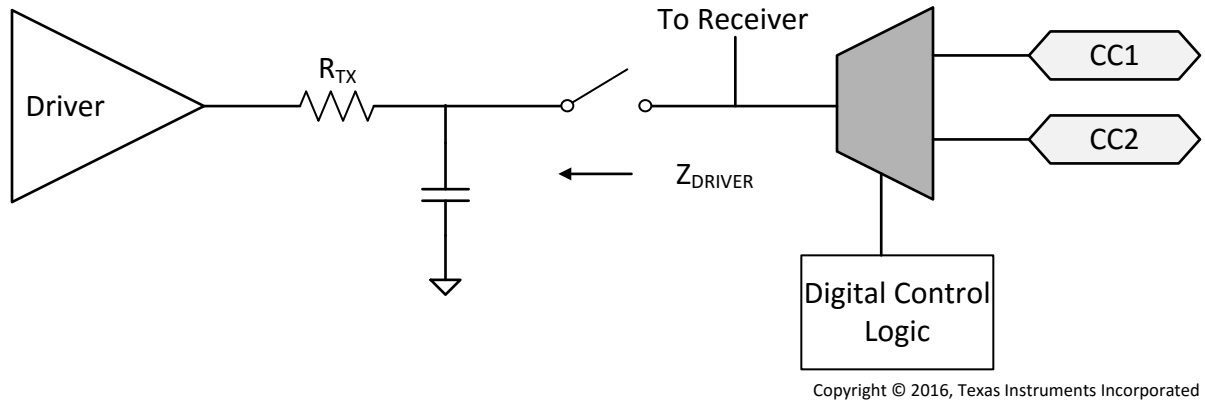


Figure 27. USB Power Delivery BMC Transmitter Schematic

The transmit eye diagram shown in Figure 29 was measured using the test load shown in Figure 28 with a C_{LOAD} within the allowed range. The total capacitance C_{LOAD} is computed as:

$$C_{LOAD} = C_{RX} + C_{CablePlug} \times 2 + Ca + C_{Receiver} \quad (1)$$

Where:

- 200 pF < C_{RX} < 600 pF
- $C_{CablePlug}$ < 25 pF
- Ca < 625 pF
- 200 pF < C*Receiver* < 600 pF

Therefore, 400 pF < C_{LOAD} < 1850 pF.

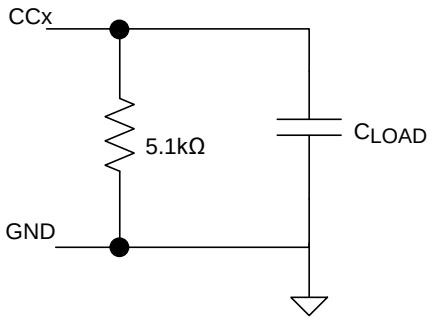


Figure 28. Test Load for BMC Transmitter

Figure 29 shows the transmit eye diagram for the TPS25741 and TPS25741A.

Feature Description (continued)

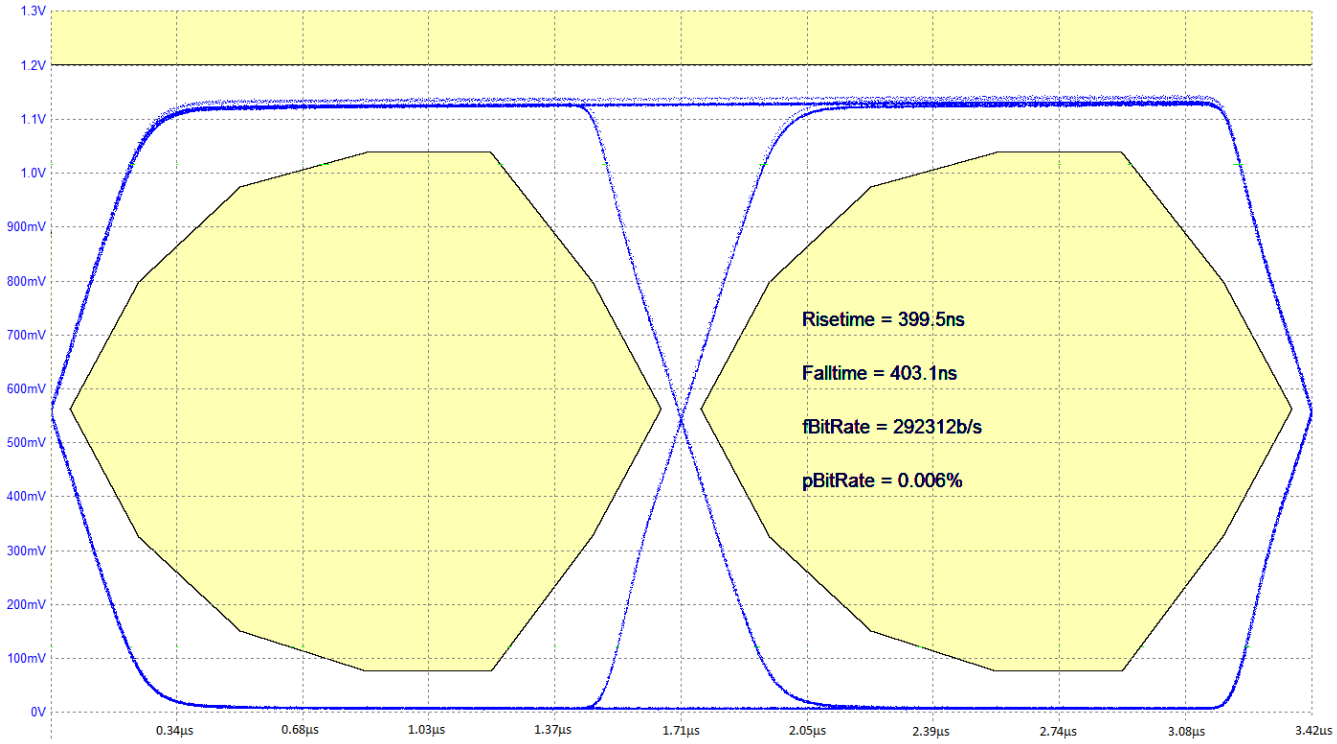


Figure 29. Transmit Eye Diagram (BMC)

The transmitter bias rail (VTX) is internally generated and may not be used for any other purpose in the system. Connect a 0.1-µF capacitor to GND from this pin. The VTX pin is only high while the TPS25741/TPS25741A is transmitting a USB Power Delivery message.

8.3.4 USB Power Delivery BMC Reception (CC1, CC2)

The TPS25741 or TPS25741A BMC receiver follows the requirements in *Application Information* using the schematic shown in Figure 30.

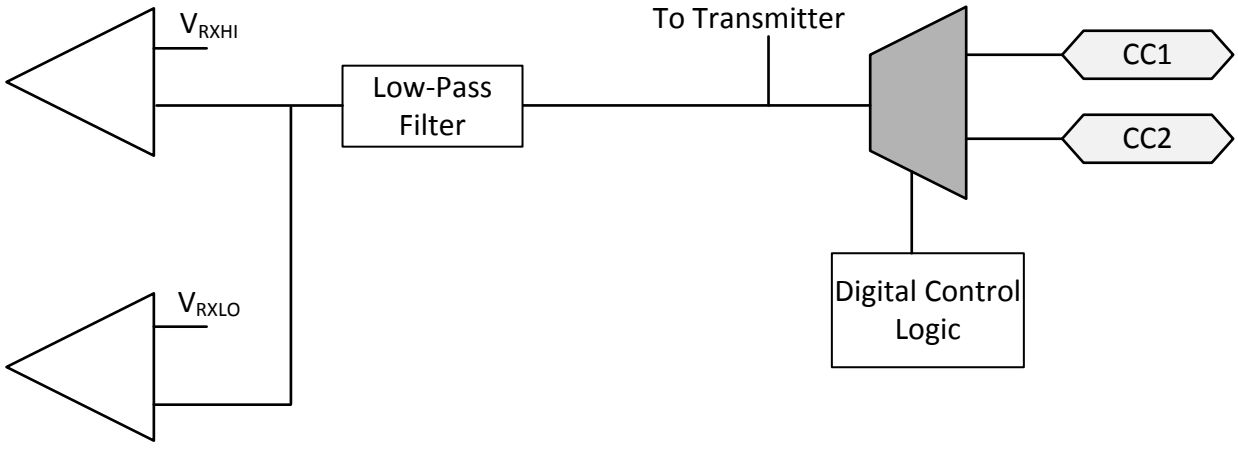


Figure 30. USB Power Delivery BMC Receiver Schematic

The device low-pass filter design and receiver threshold design allows it to reject interference that may couple onto the CC line from a noisy VBUS power supply or any other source.

Feature Description (continued)

8.3.5 Discharging (DSCG, VPWR)

The DSCG pin allows for two different pull-downs that are used to apply different discharging strengths. In addition, a load may be applied to the VPWR pin to discharge the power supply.

If too much power is dissipated by the device (that is, the T_{J1} temperature is exceeded) an OTSD occurs that disables the discharge FET; therefore, an external resistor is recommended in series with the DSCG pin to absorb most of the dissipated power. The external resistor R_{DSCG} should be chosen such that the current sunk by the DSCG pin does not exceed I_{DSCGT}.

The VPWR pin should always be connected to the supply side (as opposed to the connector side) of the power-path switch (Figure 31 shows one example). This pin is monitored before enabling the GDNG gate driver to apply the voltage to the V_{BUS} pin of the connector.

From sink attachment, and while the device has not finalized a USB Power Delivery contract, the device applies R_{DSCGB}.

Also from sink attachment, and while the device has not finalized a USB Power Delivery contract, the device draws I_{SUPP} through the VPWR pin even if VDD is above its UVLO. This helps to discharge the power supply source bulk capacitance.

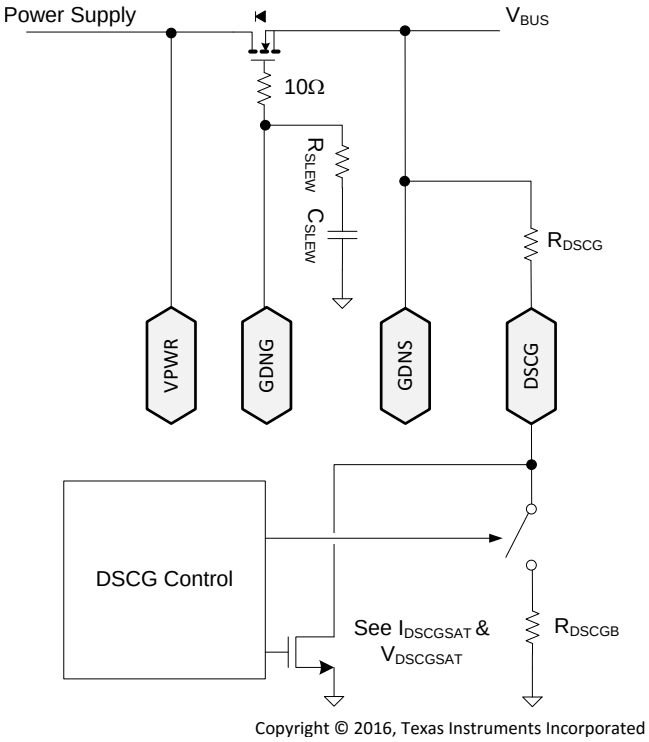


Figure 31. Discharge Schematic

The discharge procedure used in the TPS25741 or TPS25741A is intended to allow the DSCG pin to help pull the power supply down from high voltage, and then also pull V_{BUS} at the connector down to the required level quickly (refer to USB Power Delivery in *Documentation Support*).

8.3.5.1 Discharging after a Fault (VPWR)

There are two types of faults that cause the TPS25741 or TPS25741A to begin a full discharge of VBUS: Slow-shutdown faults and fast-shutdown faults. When a slow-shutdown fault occurs, the device does not disable GDNG until after VBUS is measured below V_{SOVP} (for 5 V contract). When a fast-shutdown fault occurs, the device disables GDNG immediately and then discharges the connector side of the power-path. In both cases, the bleed discharge is applied to the DSCG pin and I_{SUPP} is drawn from the VPWR pin.

Feature Description (continued)

Slow-shutdown faults that do not include transmitting a hard reset:

- Receiving a Hard Reset signal (25 ms < $t_{ShutdownDelay}$ < 35 ms)
- Cable is unplugged ($t_{ShutdownDelay}$ < 20 µs)

Slow-shutdown faults that include transmitting hard reset (25 ms < $t_{ShutdownDelay}$ < 35 ms)

- T_J exceeds T_{J1} (an overtemperature event)
- Low voltage alarm occurring outside of a voltage transition
- High voltage alarm occurring outside of a voltage transition (but not high enough to cause OVP)
- Receiving an unexpected message during a voltage transition
- Failure of power supply to transition voltages within required time of 600 ms (tPSTransition [refer to USB Power Delivery in *Documentation Support*]).
- A Soft Reset USB Power Delivery message is not acknowledged or Accepted (as required per USB Power Delivery in *Documentation Support*).
- A Request USB Power Delivery message is not received in the required time (as required per USB Power Delivery in *Documentation Support*).
- Failure to discharge down to 0.725 V after a fault of any kind.

Fast-shutdown faults (hard reset always sent):

- Fast OVP event occurring at any time.
- OCP event occurring at any time starting from the transmission of the first USB Power Delivery message.
  - VBUS falling below V_{BUS_FTH} is treated as an OVP event.
- $\overline{GD}$ falling edge

The DSCG pin is used to discharge the supply line after a slow-shutdown fault occurs. Figure 32 illustrates the signals involved. Depending on the specific slow-shutdown fault the time $t_{ShutdownDelay}$ in Figure 32 is different as indicated in the list above. If the slow-shutdown fault triggers a hard reset, it is sent at the beginning of the $t_{ShutdownDelay}$ period. However, the device behavior after the time $t_{ShutdownDelay}$ is the same for all slow-shutdown faults. After the $t_{ShutdownDelay}$ period, the device sets CTL1 and CTL2 to select 5 V from the power supply and puts the DSCG pin into its ON state (Full Discharge). This discharging continues until the voltage on the VBUS pin reaches V_{SOPV} (for 5 V contract). The device then disables GDNG and again puts the DSCG pin into its ON state. This discharging state lasts until the voltage on VBUS reaches 0.725 V (nominal). If the discharge does not complete within 650 ms, then the device sends a Hard Reset signal and the process repeats. In Figure 32, the times labeled as $T_{20->5}$ and $T_{5->0}$ can vary, they depend on the size of the capacitance to be discharged and the size of the external resistor between the DSCG pin and V_{BUS}. The time labeled as T_S is a function of how quickly the NFET opens.

Feature Description (continued)

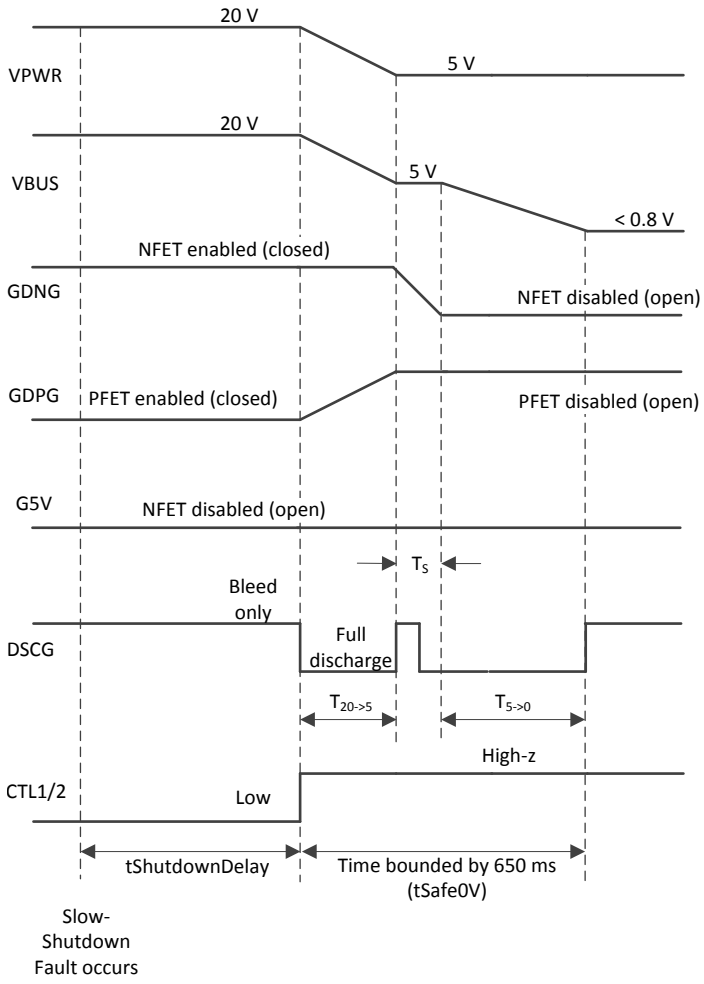


Figure 32. Illustration of Slow-Shutdown VBUS Discharge

Figure 33 illustrates a similar discharge procedure for fast-shutdown faults. The main difference from Figure 32 is that the NFET is opened immediately. It is assumed for the purposes of this illustration that the power supply output capacitance (that is, C_{SOURCE} in the reference schematics shown in Figure 20 and Figure 21) is not discharged by the power supply itself, but the VPWR pin is bleeding current from that capacitance. The VPWR pin then draws I_{SUPP} after GDNG disables the external NFET. So, as shown in the figure, the VPWR voltage discharges slowly, while the VBUS pin is discharged quickly once the full discharge is enabled. If the voltage on the VPWR pin takes longer than $T_{20->5} + T_{5->0} + 0.765s$ to discharge below V_{FOVP}, then it causes an OVP event and the process repeats.

Feature Description (continued)

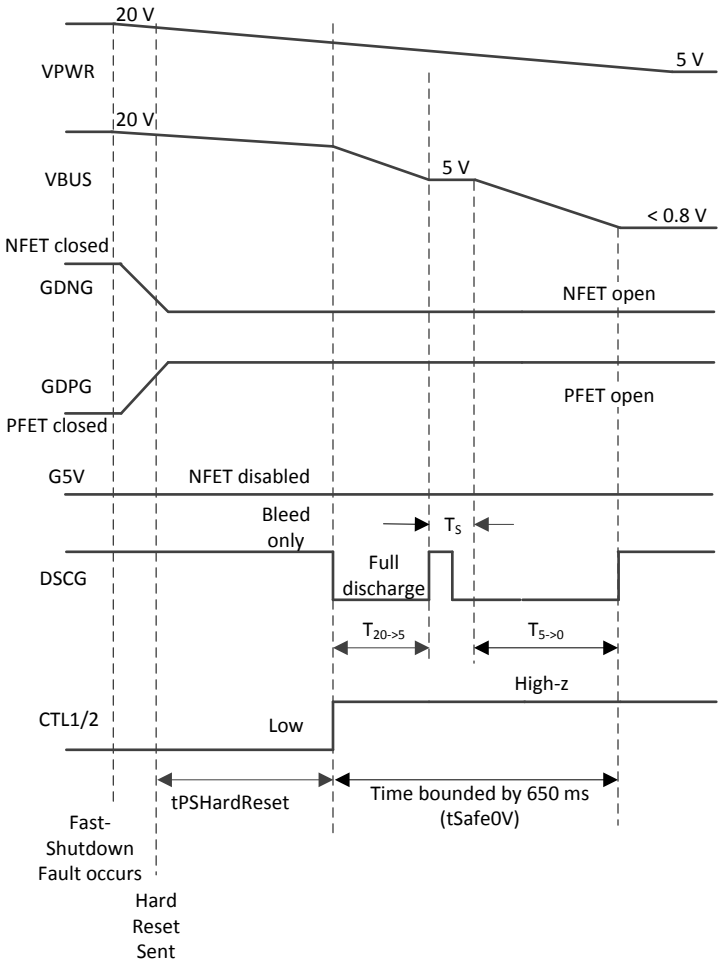


Figure 33. Illustration of Fast-Shutdown Discharge

If the discharge does not complete successfully it is treated as a slow-shutdown fault, and the TPS25741 or TPS25741A repeats the discharge procedure until it does complete successfully. Once the discharge completes successfully as described above (that is, VBUS on connector is below 0.725 V), the device waits for 0.765 s (nominal) before trying to source VBUS again.

8.3.6 Configuring Voltage Capabilities (HIPWR, EN9V, EN12V)

The voltages advertised to USB Power Delivery-capable sinks can be configured to one of four different sets. The EN12V, or EN9V pin is not envisioned to be changed dynamically in the system, so changing its state does not trigger sending source capabilities. However, the TPS25741 or TPS25741A checks the status of the pin each time before it sends a source capabilities message using USB Power Delivery. Note that changing the state of the PCTRL pin forces capabilities to be re-transmitted. The device reads the HIPWR pin after a reset and latches the result.

Table 1. Voltage Programming (TPS25741)

EN12V PIN	HIPWR PIN	VOLTAGES ADVERTISED via USB POWER DELIVERY [V]
High	Connected to DVDD or GND directly	5, 12, 20
High	Connected to DVDD or GND via RSEL	5, 12
Low	Connected to DVDD or GND directly	5, 20

Feature Description (continued)

Table 1. Voltage Programming (TPS25741) (continued)

EN12V PIN	HIPWR PIN	VOLTAGES ADVERTISED via USB POWER DELIVERY [V]
Low	Connected to DVDD or GND via RSEL	5

Table 2. Voltage Programming (TPS25741A)

EN9V PIN	HIPWR PIN	VOLTAGES ADVERTISED via USB POWER DELIVERY [V]
High	Connected to DVDD or GND directly	5, 9, 15
High	Connected to DVDD or GND via RSEL	5, 9
Low	Connected to DVDD or GND directly	5, 15
Low	Connected to DVDD or GND via RSEL	5

8.3.7 Configuring Power Capabilities (PSEL, PCTRL, HIPWR)

The power advertised to non-Power Delivery Type-C Sinks is always 15 W. However, the TPS25741 or TPS25741A only advertises Type-C default current until it debounces the Sink attachment for t_{CcDeb} and the VBUS voltage has been given t_{VP} to stabilize.

The device does not communicate with the cable to determine its capabilities. Therefore, unless the device is in a system with a USB Type-C plug and a cable built to support 5 A, the HIPWR pin should be used to limit the advertised current to 3 A.

PCTRL is an input pin used to control how much of the maximum allowed power the port will advertise. This pin may be changed dynamically in the system and the device automatically updates any existing USB Power Delivery contract. If the PCTRL pin is pulled below $V_{PCTRL\_TH,}$ then the source capabilities offers half of the maximum power specified by the PSEL pin.

The devices read the PSEL and HIPWR pins after a reset and latches the result, but the PCTRL pin is read dynamically by the device and if its state changes new capabilities are calculated and then transmitted.

While USB Power Delivery allows a maximum power of 100 W, the TPS25741 only advertises up to 93 W, which allows margin to ensure the output power remains below 100 W.

The PSEL pin offers four possible maximum power settings, but the devices can actually advertise more power settings depending upon the state of the HIPWR and PCTRL pins. Table 3 summarizes the four maximum power settings that are available via PSEL, again note this is not necessarily the maximum power that is advertised.

Table 3. PSEL Configurations

MAXIMUM POWER (P_{SEL}) [W]	PSEL
P_{SEL} = 36	Direct to GND
P_{SEL} = 45	DVDD via RSEL
P_{SEL} = 65	GND via RSEL
P_{SEL} = 93	Direct to DVDD

The following list provides a quick reference which applies to both TPS25741 and TPS25741A to see how the HIPWR, PSEL, and PCTRL pins affect what current is advertised with each voltage in the source capabilities message:

- If the PCTRL pin is low, then Pmax = P_{SEL}/2
- If the PCTRL pin is high, then Pmax = P_{SEL}.
- If the HIPWR pin is pulled high, then Imax = 3 A.
- If the HIPWR pin is pulled low, then Imax = 5 A.
- For a voltage Vx, the advertised current is Ix
  - Ix = min(Pmax/Vx, Imax)

Table 4 and Table 5 provide a comprehensive list of the currents and voltages that are advertised for each voltage.

Table 4. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25741)

P_{SEL}	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 3 A DVDD through RSEL or Direct to DVDD	3	3
DVDD via RSEL			3	3
GND via RSEL			3	3
Direct to DVDD			3	3
Direct to GND	12		1.5	3
DVDD via RSEL			1.87	3
GND via RSEL			2.7	3
Direct to DVDD			3	3
Direct to GND	20	Max = 3 A Direct to DVDD	0.9	1.8
DVDD via RSEL			1.12	2.24
GND via RSEL			1.62	3
Direct to DVDD			2.32	3
Direct to GND	5	Max = 5 A GND through RSEL or Direct to GND	3.6	5
DVDD via RSEL			4.5	5
GND via RSEL			5	5
Direct to DVDD			5	5
Direct to GND	12		1.5	3
DVDD via RSEL			1.87	3.74
GND via RSEL			2.7	5
Direct to DVDD			4.16	5
Direct to GND	20	Max = 5 A Direct to GND	0.9	1.8
DVDD via RSEL			1.12	2.24
GND via RSEL			1.62	3.24
Direct to DVDD			2.32	4.64

Table 5. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25741A)

P_{SEL}	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 3 A DVDD through RSEL or Direct to DVDD	3	3
DVDD via RSEL			3	3
GND via RSEL			3	3
Direct to DVDD			3	3
Direct to GND	9		2	3
DVDD via RSEL			2.5	3
GND via RSEL			3	3
Direct to DVDD			3	3
Direct to GND	15	Max = 3 A Direct to DVDD	1.2	2.4
DVDD via RSEL			1.5	3
GND via RSEL			2.17	3
Direct to DVDD			3	3

Table 5. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25741A) (continued)

P_{SEL}	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 5 A GND through RSEL or Direct to GND	3.6	5
DVDD via RSEL			4.5	5
GND via RSEL			5	5
Direct to DVDD			5	5
Direct to GND	9		2	4
DVDD via RSEL			2.5	5
GND via RSEL			3.61	5
Direct to DVDD			5	5
Direct to GND	15	Max = 5 A Direct to GND	1.2	2.4
DVDD via RSEL			1.5	3
GND via RSEL			2.17	4.34
Direct to DVDD			3.1	5

8.3.8 Gate Drivers

8.3.8.1 GDNG, GDNS

The GDNG and GDNS pins may control a single NFET or back-to-back NFETs in a common-source configuration. The GDNS is used to sense the voltage so that the voltage differential between the pins is maintained.

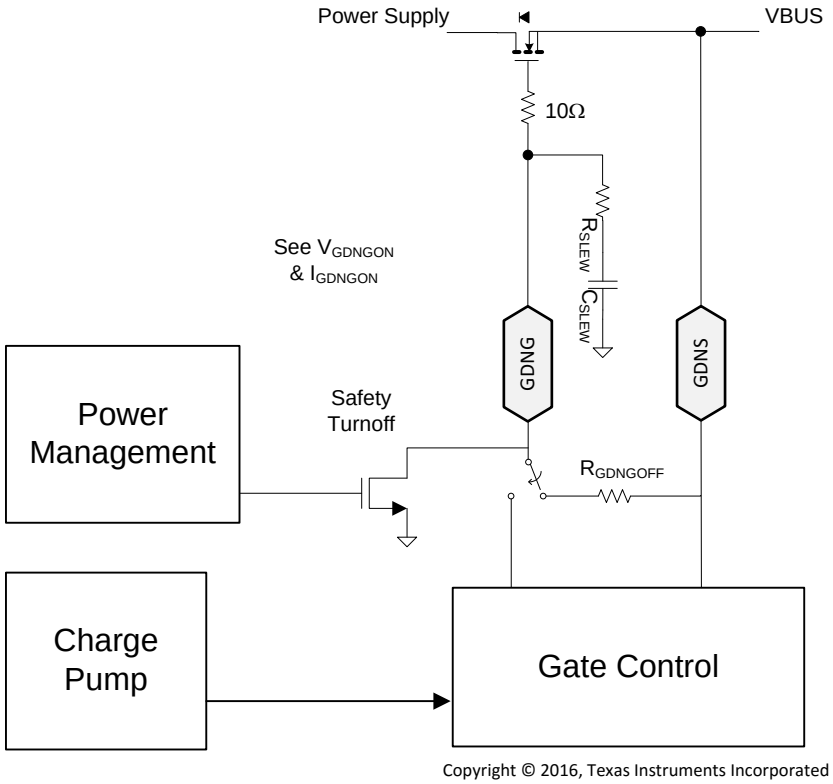


Figure 34. GDNG/GDNS Gate Control

8.3.8.2 G5V

The G5V pin may control an external NFET when the TPS25741/TPS25741A is used in a power multiplexor configuration, where one of two voltage inputs is connected to the VBUS pin. When G5V is not used to control an NFET, then it can be used to indicate if VBUS is being sourced at 5 V or not.

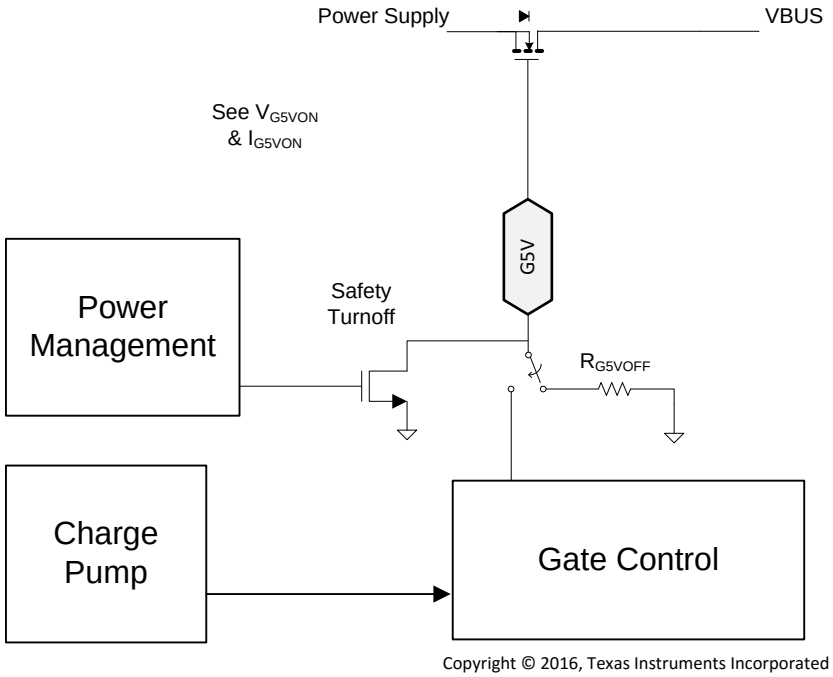


Figure 35. G5V Gate Control

8.3.8.3 GDPG

The GDPG pin may control an external PFET (single or back-to-back) when the TPS25741/TPS25741A is used in a power multiplexor configuration, where one of two voltage inputs is connected to the VBUS pin. When not used to control a PFET, this pin may be used to indicate when VBUS is being sourced at more than 5 V.

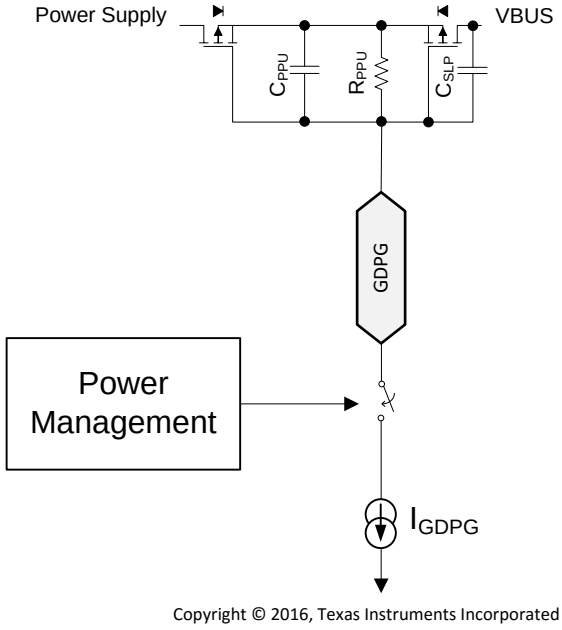


Figure 36. GDPG Gate Control

8.3.9 Fault Monitoring and Protection

8.3.9.1 Over/Under Voltage (VBUS)

The TPS25741 or TPS25741A uses the VBUS pin to monitor for overvoltage or undervoltage conditions and implement the fast-OVP, slow-OVP, and slow-UVP features.

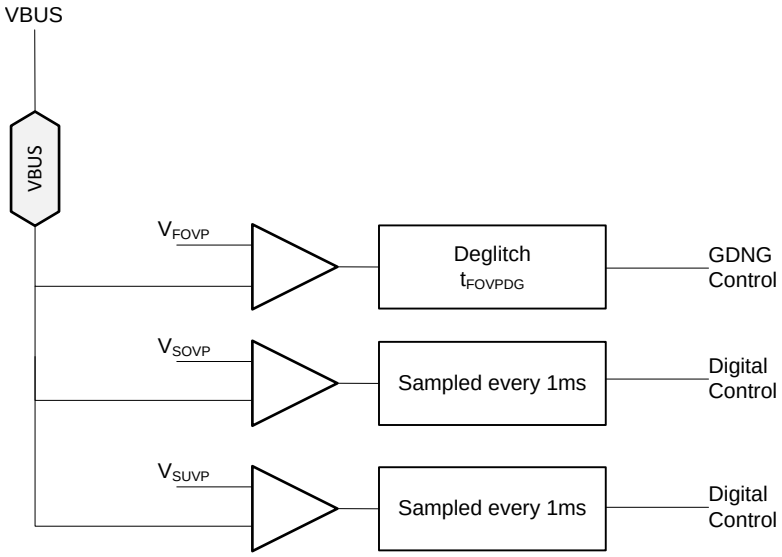


Figure 37. Voltage Monitoring Circuits

If an over-voltage condition is sensed by the Fast OVP mechanism, GDNG is disabled within t_{FOVP} + t_{FOVPDG}, then a Hard Reset is transmitted and the VBUS discharge sequence is started. At power up the voltage trip point is set to V_{VFOVP} (5 V contract). When a contract is negotiated the trip point is set to the corresponding V_{FOVP} value.

The devices employ another slow over-voltage protection mechanism as well that sends the Hard Reset before disabling the external NFET. It catches many OV events before the Fast OVP mechanism. During intentional positive voltage transitions, this mechanism is disabled (see Figure 1). However, t_{VP} after the external NFET has been enabled if the voltage on the VBUS pin exceeds V_{SOVP}, a Hard Reset is transmitted to the Sink then the VBUS discharge sequence is started. Once a Power Delivery contract has been negotiated, if the voltage on the VBUS pin exceeds the selected voltage threshold (V_{SOVP}) a Hard Reset is transmitted to the Sink then the VBUS discharge sequence is started.

The devices employ a slow under-voltage protection mechanism as well that sends the Hard Reset before disabling GDNG. During intentional negative voltage transitions, this mechanism is disabled (see Figure 1). However, t_{VP} after the external NFET has been enabled if the voltage on the VBUS pin falls below V_{SUVP}, a Hard Reset is transmitted to the Sink then the VBUS discharge sequence is started..

8.3.9.2 Over-Current Protection (ISNS, VBUS)

OCP protection is enabled t_{VP} after the voltage on the VBUS pin has exceeded V_{BUS_RTH}, see Figure 38. Prior to OCP being enabled, the $\overline{GD}$ pin can be used to protect against a short.

The OCP protection circuit monitors the differential voltage across an external sense resistor to detect when the current outflow exceeds V_{ITRIP} which in turn activates an over-current circuit breaker and disables the GDNG / GDNS gate driver. Once the OCP is enabled, if the voltage on the VBUS pin falls below V_{BUS_FTH} then that is also treated like an OCP event.

Following the recommended implementation of a 5 mΩ sense resistor, when the device is configured to deliver 3 A (via HIPWR pin), the OCP threshold lies between 3.8 A and 4.5 A. When configured to deliver 5 A (via HIPWR pin), the OCP threshold lies between 5.8 A and 6.8 A. The sense resistor may be increased to tighten the OCP threshold.

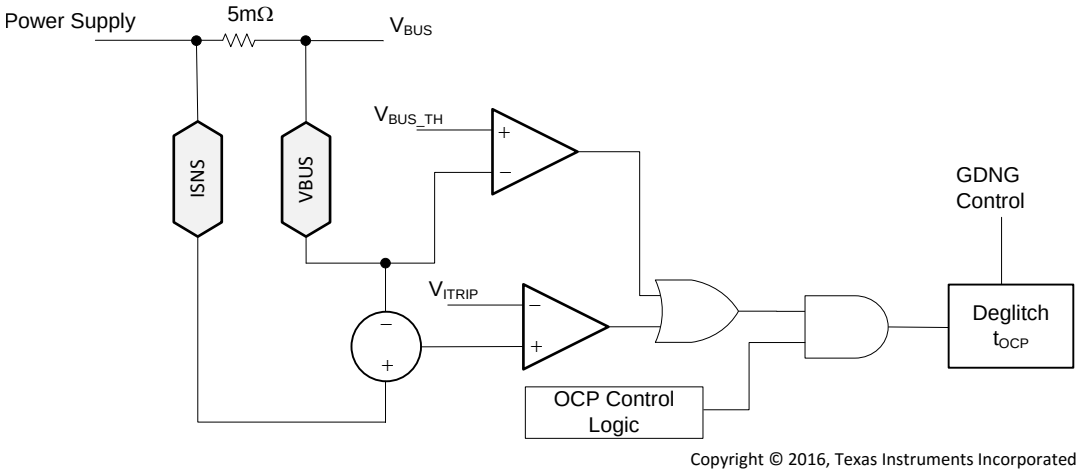


Figure 38. Overcurrent Protection Circuit

8.3.9.3 System Fault Input ($\overline{GD}$, VPWR)

The gate-driver disable pin provides a method of overriding the internal control of GDNG and GDNS. A falling edge on $\overline{GD}$ disables the gate driver within t_{GDoff}. If $\overline{GD}$ is held low after a sink is attached for 600 ms then a hard reset will be generated and the device sends a hard reset and goes through its startup process again.

The $\overline{GD}$ input can be controlled by a voltage or current source. An internal voltage clamp is provided to limit the input voltage in current source applications. The clamp can safely conduct up to 80 µA and will remain high impedance up to V_{GDC} before clamping.

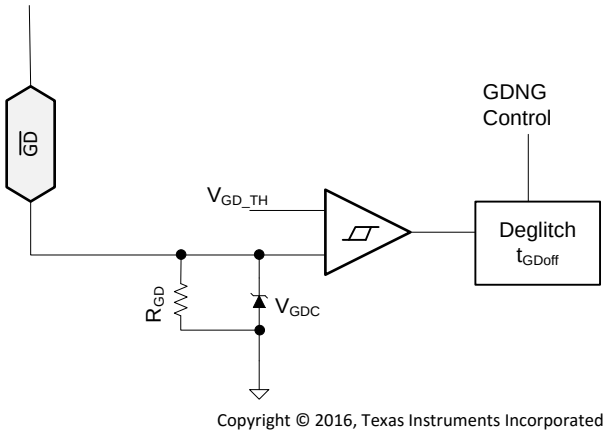


Figure 39. Overcurrent Protection Circuit

If the VPWR pin remains below its falling UVLO threshold (V_{PWR_TH}) for more than 600 ms after a sink is attached then the devices consider it a fault and will not enable GDNG. If the VPWR pin is between the rising and falling UVLO threshold, the TPS25741/TPS25741A may enable GDNG and proceed with normal operations. However, after GDNG is enabled, if the VBUS pin does not rise above its UVLO within 190 ms the devices consider it a fast-shutdown fault and disables GDNG. Therefore, in order to ensure USB Type-C compliance and normal operation, the VPWR pin must be above its rising UVLO threshold (V_{PWR_TH}) within 275 ms of when $\overline{UFP}$ is pulled low and the VBUS pin must be above V_{BUS_RTH} within 190 ms of GDNG being enabled.

8.3.10 Voltage Control (CTL1, CTL2)

CTL1 and CTL2 are open-drain output pins used to control an external power supply as summarized in Table 6. Depending upon the voltage requested by the sink, the device sets the CTL pins accordingly. No current flows into the pin in its high-z state.

Table 6. States of CTL1 and CTL2 as a Function of Target Voltage on V_{BUS} for TPS25741 and TPS25741A

VOLTAGE CONTAINED in PDO REQUESTED by UFP	CTL2 STATE	CTL1 STATE
5 V	High-z	High-z
9 V (TPS25741A)	Low	High-z
12 V (TPS25741)	Low	High-z
15 V (TPS25741A)	Low	Low
20 V (TPS25741)	Low	Low

8.3.11 Sink Attachment Indicator ($\overline{\text{UFP}}$, DVDD)

$\overline{\text{UFP}}$ is an open-drain output pin used to indicate the status of the port. It is high-z unless a sink is attached to the port, in which case it is pulled low. A sink attachment is detected when the voltage on one (not both) of the CC pins remains between V_{RDSTD} and V_{DSTD} for t_{CcDeb} and the voltage on the VBUS pin is below V_{BUS_FTH}. After being pulled low, $\overline{\text{UFP}}$ remains low until the sink has been removed for t_{CcDeb}.

DVDD is a power supply pin that is high-z until a sink is attached, in which case it is pulled high. Therefore, it can be used as a sink attachment indicator that is active high. However, DVDD will also be high when an Audio or Debug accessory is attached. See Figure 18 for typical behavior.

8.3.12 Accessory Attachment Indicator ($\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$)

$\overline{\text{AUDIO}}$ is an open-drain output pin used to indicate the attachment of a USB Type-C audio accessory. After both CC1 and CC2 are pulled below V_{RDSTD} for at least tCcDeb, $\overline{\text{AUDIO}}$ is pulled low until at least one of the CC pins rises above V_{RDSTD} for at least t_{CcDeb}.

$\overline{\text{DEBUG}}$ is an open-drain output pin used to indicate the attachment of a USB Type-C debug accessory. After both CC1 and CC2 are between V_{DSTD} and V_{RDSTD} for at least t_{CcDeb}, $\overline{\text{DEBUG}}$ is pulled low until at least one of the CC pins rises above V_{DSTD} or below V_{RDSTD}. This complies with the USB Type-C version 1.1 debug accessory detection.

8.3.13 Plug Polarity Indication ($\overline{\text{POL}}$)

The $\overline{\text{POL}}$ pin is pulled low when the CC wire in the attached USB Type-C cable is connected to the CC2 pin. This pin is open-drain if the attached cable has the opposite polarity or if nothing is attached.

8.3.14 Power Supplies (VAUX, VDD, VPWR, DVDD)

The VAUX pin is the output of a linear regulator and the input supply for internal power management circuitry. The VAUX regulator draws power from VDD after establishing a USB Power Delivery contract unless it is not available in which case it draws from VPWR. Changes in supply voltages will result in seamless switching between supplies.

If there is a load on the DVDD pin, that current will be drawn from the VPWR pin unless the TPS25741/TPS25741A has stabilized into a USB Power Delivery contract or VPWR is below its UVLO.

The TPS25741/TPS25741A cannot function properly until VPWR is above its UVLO. However, for improved system efficiency when $\overline{\text{UFP}}$ is high-z, VPWR can be low (the high voltage power supply can be disabled) if VDD is above its UVLO.

Connect a 0.1-µF ceramic capacitor from VAUX to GND. Do not connect any external load that draws more than $I_{VAUXEXT}$. Locate the bypass capacitor close to the pin and provide a low impedance ground connection from the capacitor to the ground plane.

VDD should either be grounded or be fed by a low impedance path and have input bypass capacitance. Locate the bypass capacitors close to the VDD and VPWR pins and provide a low impedance ground connection from the capacitor to the ground plane.

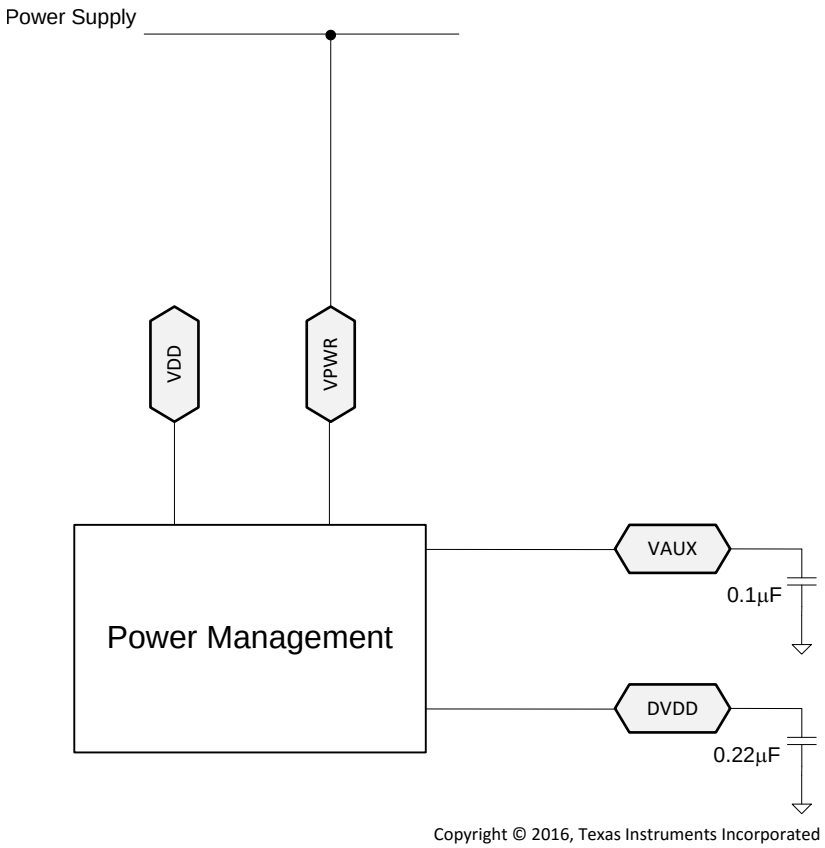


Figure 40. Power Management

8.3.15 Grounds (AGND, GND)

GND is the substrate ground of the die. Most circuits return to GND, but certain analog circuitry returns to AGND to reduce noise and offsets. The power pad (on those devices that possess one) is electrically connected to GND. Connect AGND, GND and the power pad (if present) to the ground plane through the shortest and most direct connections possible.

8.3.16 Output Power Supply (DVDD)

The DVDD pin is the output of an internal 1.85 V linear regulator, and the input supply for internal digital circuitry. This regulator normally draws power from VPWR until a USB Power Delivery contract has stabilized, but will seamlessly swap to drawing power from VDD in the event that VPWR drops below its UVLO threshold. External circuitry can draw up to 35 mA from DVDD. Note that as more power is drawn from the DVDD pin more heat will be dissipated in the TPS25741/TPS25741A, and if excessive the OTSD could be tripped which will reset the TPS25741/TPS25741A.

Connect a 0.22-µF or 0.33-µF ceramic capacitor from DVDD to GND (do not exceed this recommended bypass capacitance value).

Locate the bypass capacitor close to the pin and provide a low impedance ground connection from the capacitor to the ground plane.

8.4 Device Functional Modes

8.4.1 Sleep Mode

Many adaptors that include USB Power Delivery must consume very low quiescent power to meet regulatory requirements (for example “Green”, Energy Star, or the like). The TPS25741/TPS25741A supports the sleep mode to minimize power consumption when the receptacle or plug is unattached. The TPS25741/TPS25741A will enter sleep mode when there is no valid plug termination attached; a valid plug termination is defined as one of: sink, Audio accessory, or Debug accessory. If an active cable is attached but its far-end is left unconnected or “dangling”, then the TPS25741/TPS25741A will also enter sleep mode. It will exit the sleep mode whenever the plug status changes. This could be a dangling cable being removed or a sink being connected.

8.4.2 Checking VBUS at Start Up

When first powered up, the TPS25741/TPS25741A will not enable GDNG if the voltage on VBUS is already above its UVLO. This is a protective measure taken to avoid the possibility of turning on while connected to another active power supply in some non-compliant configuration.

This means that the VBUS pin must be connected between the power-path NFET and the USB connector. This also allows for a controlled discharge of VBUS all the way down to the required voltage on the connector (refer to USB Power Delivery in *Documentation Support*).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS25741/TPS25741A implements a fully compliant USB Power Delivery 2.0 provider and Type-C source (also known as downward facing port (DFP)). The TPS25741/TPS25741A basic schematic diagram is shown in Figure 41. Subsequent sections describe detailed design procedures for several applications with differing requirements. The TPS25741/TPS25741A Design Calculator Tool (refer to the *Documentation Support*) is available for download and use in calculating the equations in the following sections.

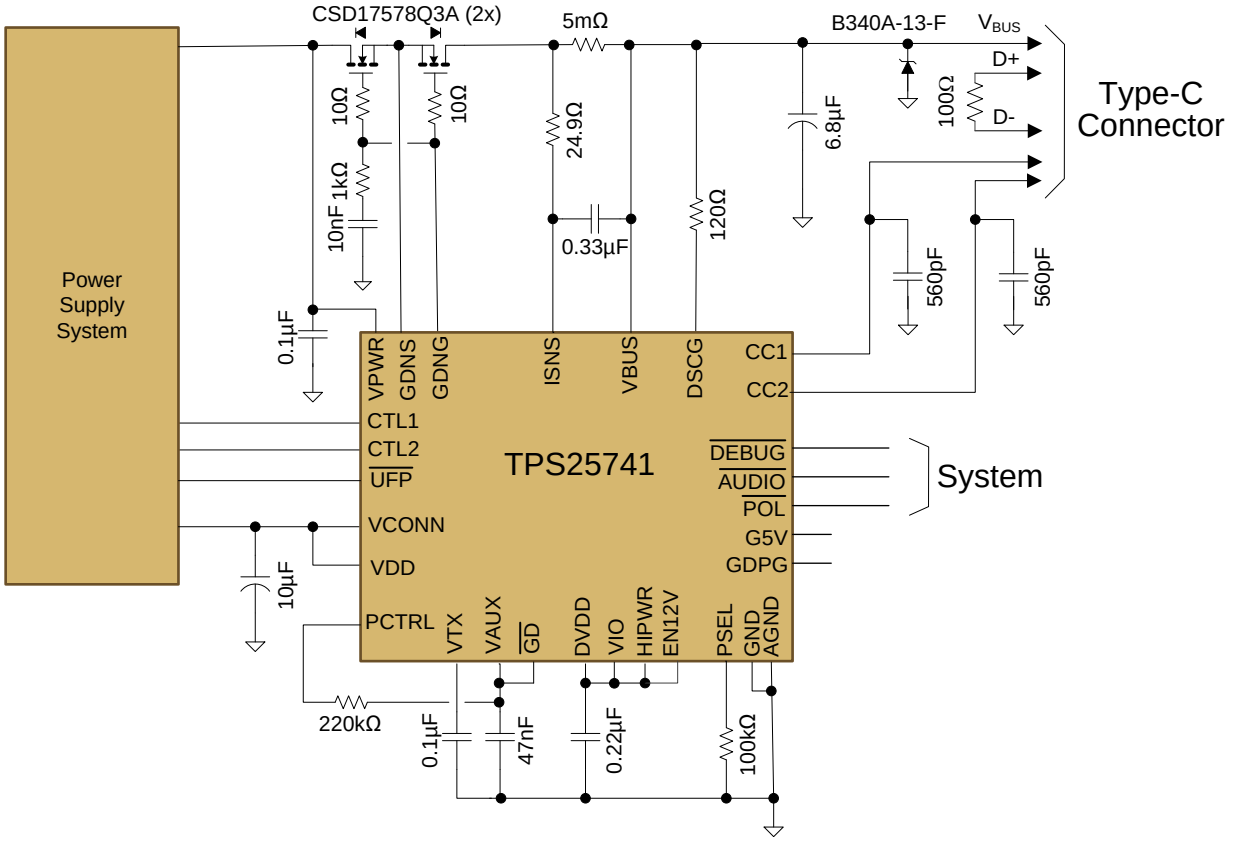


Figure 41. Basic Schematic Diagram (P_{SEL} = 65 W at 5 V, 12 V, 20 V)

9.1.1 System-Level ESD Protection

System-level ESD (per EN61000-4-2) may occur as the result of a cable being plugged in, or a user touching the USB connector or cable. Figure 42 shows an example ESD protection for the VBUS path that helps protect the VBUS pin, ISNS and DSCG pins of the TPS25741/TPS25741A from system-level ESD. The TPS25741/TPS25741A has ESD protection built into the CC1 and CC2 pins so that no external protection is necessary. Refer to the layout guidelines section for external component placement and routing recommendations.

The Schottky diode is to protect against VBUS being drawn below ground by an inductive load, the cable inductance may be as high as 900 nH.

Application Information (continued)

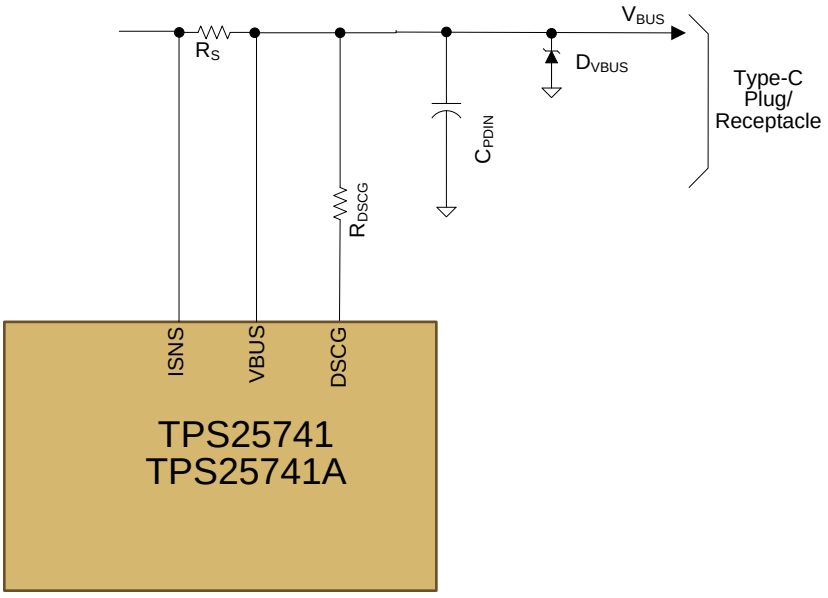


Figure 42. V_{BUS} ESD Protection

9.1.2 Use of $\overline{GD}$ Internal Clamp

As described in the *Configuring Power Capabilities (PSEL, PCTRL, HIPWR)* section, the $\overline{GD}$ pin has an internal clamp. Figure 43 shows an example of how it may be used. V_{OUT} is the voltage from a power supply that is to be provided onto the VBUS wire of the USB Type-C cable through an NFET. If V_{OUT} drops, the NFET should be automatically disabled by the device. This can be accomplished by tying the $\overline{GD}$ pin to V_{OUT} via a resistor.

The internal resistance of the $\overline{GD}$ pin is specified to exceed R_{GD}, and the input threshold is V_{GD_TH}. The $\overline{GD}$ pin would therefore draw no more than V_{GD_TH}(max) / R_{GD}(min) < 603 nA. As an example, assume the minimum value of V_{OUT} for which $\overline{GD}$ should be high is 4.5 V, then the resistor between $\overline{GD}$ and V_{OUT} may not exceed (4.5 – V_{GD_TH}(max) / 603e-9 = 4.5 MΩ. To make it robust against board leakage a smaller resistor such as 1 MΩ can be chosen, but the smaller the resistance the more leakage current into the $\overline{GD}$ pin. In this example, when V_{OUT} is 25 V, the current into the $\overline{GD}$ pin is (25-V_{GDC}) / 1e6 < 18.5 µA.

Application Information (continued)

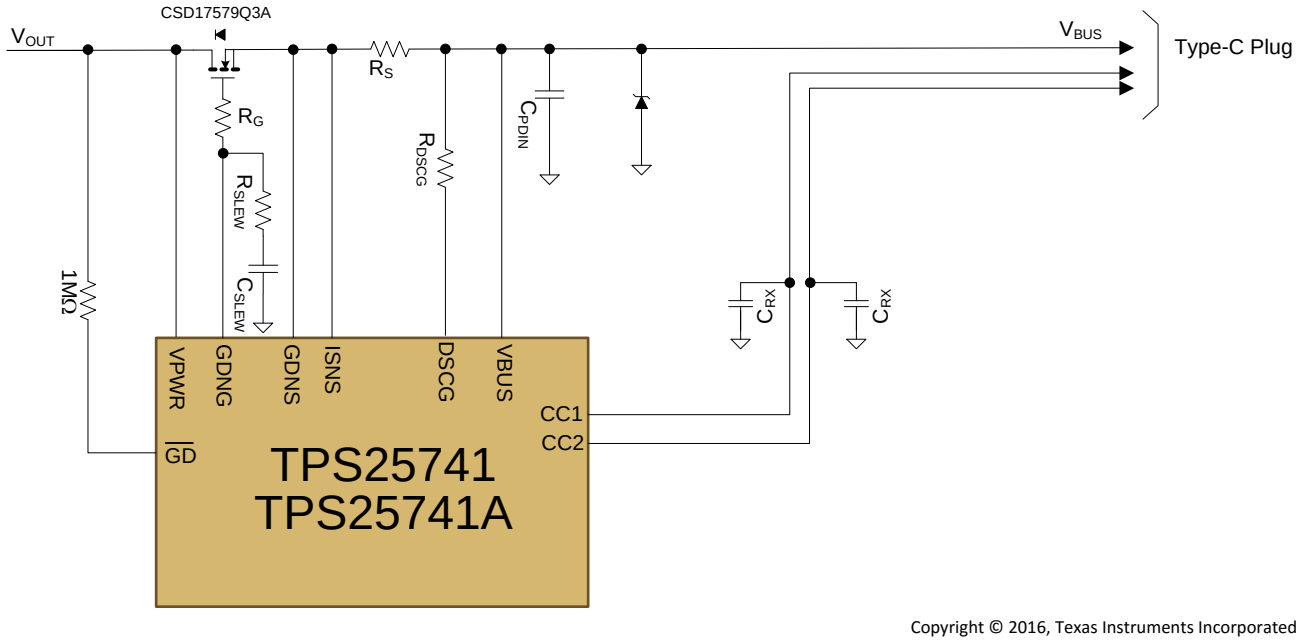


Figure 43. Use of $\overline{GD}$ Internal Clamp

9.1.3 Resistor Divider on $\overline{GD}$ for Programmable Start Up

Figure 44 shows an alternative usage of the $\overline{GD}$ pin can help protect against shorts on the V_{BUS} pin in the receptacle. A resistor divider is used to minimize the time it takes the $\overline{GD}$ pin to be pulled low. Consider the situation where the VBUS pin is shorted at startup. At some point, the device closes the NFET switch to supply 5 V to V_{BUS}. At that point, the short pulls down on the voltage seen at the VPWR pin. With the resistor values shown in Figure 44, once the voltage at the VPWR pin reaches 3.95 V the voltage at the $\overline{GD}$ pin is specified to be below V_{GD_TH}(min). Without the 700-kΩ resistor, the voltage at the VPWR pin would have to reach V_{GD_TH}(min) which takes longer. This comes at the expense of increased leakage current.

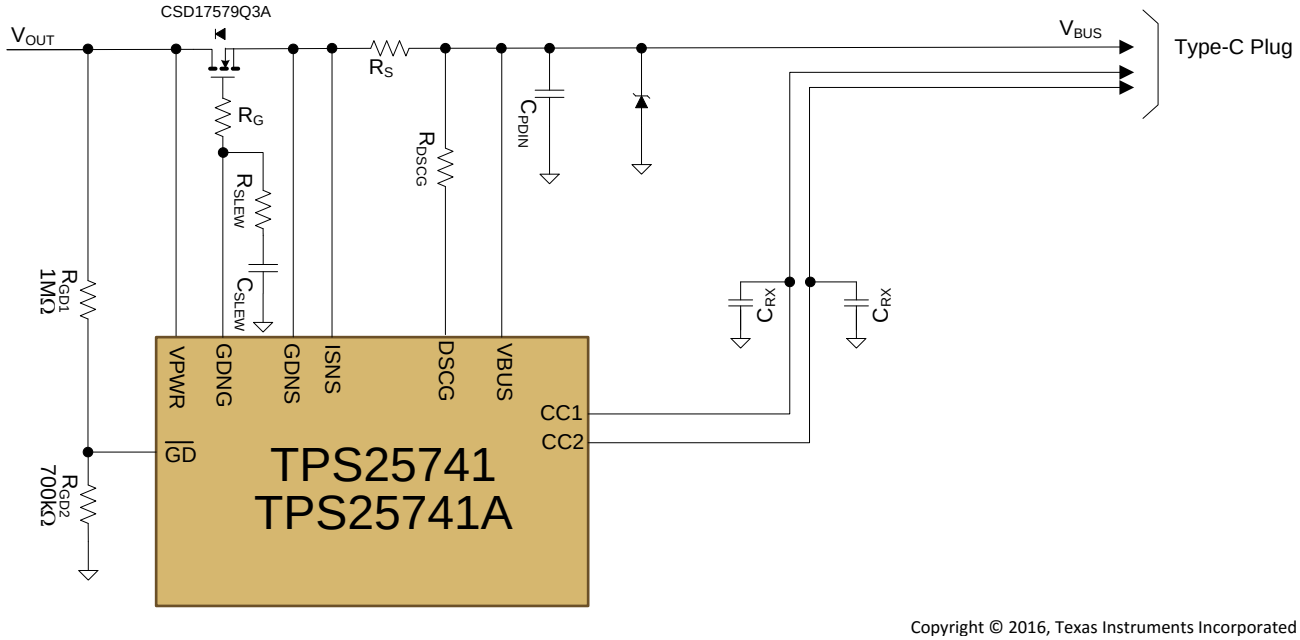


Figure 44. Programmable $\overline{GD}$ Turn On

Application Information (continued)

The $\overline{GD}$ resistor values can be calculated using the following process. First, calculate the smallest R_{GD1} that should be used to prevent the internal clamp current from exceeding I_{GD} of 80 µA. For a 20 V advertised voltage, the OVP trip point could be as high as 24 V. Using V_{GDC}(min) = 6.5 V and V_{OUT} = V_{FOVP20}(max) = 24 V, provides Equation 2:

$$R_{GD1} > \frac{V_{FOVP20} - V_{GDC}}{I_{GD}} = \frac{24\ V - 6.5\ V}{80\ \mu A} = 219\ k\Omega \quad (2)$$

The actual clamping current is less than 80 µA as some current flows into R_{GD2}. Next, R_{GD2} can be calculated as follows:

$$R_{GD2} < R_{GD1} \times \frac{V_{GD\_TH}}{V_{VPWR} - V_{GD\_TH}} \quad (3)$$

where $V_{(VPWR)}$ = $V_{(PWR\_TH)}$ falling (max) and $V_{(GD\_TH)}$ = $V_{(GD\_TH)}$ falling (min).

For this case, V_{VPWR} = V_{PWR_TH} falling (max) and V_{GD_TH} = V_{GD_TH} falling (min).

9.1.4 Selection of the CTL1 and CTL2 Resistors (R_{FBL1} and R_{FBL2})

R_{FBL1} and R_{FBL2} provide a means to change the power supply output voltage when switched in by the CTL1 and CTL2 open drain outputs, respectively. When 12 V is requested by the UFP then CTL2 will go low and place R_{FBL2} in parallel with R_{FBL}. When 20 V is requested by the UFP then CTL2 remains low and CTL1 goes low placing R_{FBL1} in parallel with R_{FBL2} and R_{FBL}.

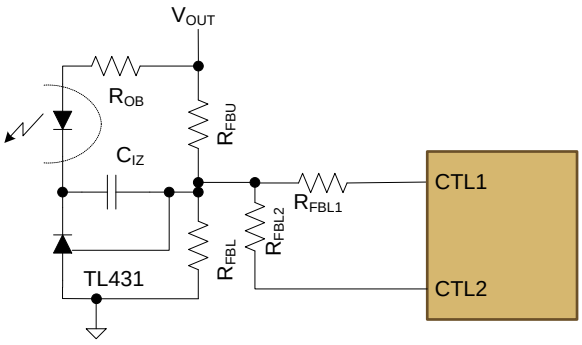


Figure 45. Circuit to Change V_{OUT} Upon Sink/UFP Request

R_{FBL2} is calculated using Equation 4. In this example, V_{OUT12} is 12 V and V_{OUT20} is 20 V. V_{OUT} is the default output voltage (5 V) for the regulator and is set by R_{FBU}, R_{FBL}, and error amplifier V_{REF}.

$$R_{FBL2} = \frac{R_{FBL} \times R_{FBU} \times V_{REF}}{R_{FBL} \times (V_{OUT12} - V_{REF}) - R_{FBU} \times V_{REF}} \quad (4)$$

R_{FBL1} is calculated using the equation below after a standard 1% value for R_{FBL2} is chosen.

$$R_{FBL1} = \frac{\frac{R_{FBL2} \times R_{FBL}}{R_{FBL2} + R_{FBL}} \times R_{FBU} \times V_{REF}}{\frac{R_{FBL2} \times R_{FBL}}{R_{FBL2} + R_{FBL}} \times (V_{OUT20} - V_{REF}) - R_{FBU} \times V_{REF}} \quad (5)$$

R_{FBL1} and R_{FBL2} should be large enough so that the CTL1/CTL2 sinking current is minimized (< 1 mA). The sinking current for CTL1 and CTL2 is V_{REF} / R_{FBL1} and V_{REF}/R_{FBL2} respectively.

Application Information (continued)

9.1.5 Voltage Transition Requirements

During VBUS voltage transitions, the slew rate ($v_{SrcSlewPos}$ in USB in *Documentation Support*) must be kept below 30 mV/µs in all portions of the waveform, settle ($t_{SrcSettle}$) in less than 275 ms, and be ready ($t_{SrcReady}$ in USB in *Documentation Support*) in less than 285 ms. For most power supplies, these requirements are met naturally without any special circuitry but in some cases, the voltage transition ramp rate must be slowed in order to meet the slew rate requirement.

The requirements for linear voltage transitions are shown in Table 7. In all cases, the minimum slew time is below 1 ms.

Table 7. Minimum Slew-Rate Requirements

VOLTAGE TRANSITION	5 V ↔ 12 V	5 V ↔ 20 V	12 V ↔ 20 V	5 V ↔ 9 V	5 V ↔ 15 V	9 V ↔ 15 V
Minimum Slew Time	233 µs	500 µs	267 µs	133 µs	333 µs	200 µs

When transition slew control is required, the interaction of the slew mechanism and dc/dc converter loop response must be considered. A simple R-C filter between the device CTL pins and converter feedback node may lead to instability under some conditions. Figure 46 shows a method which manages the slew control without adding capacitance to the converter feedback node.

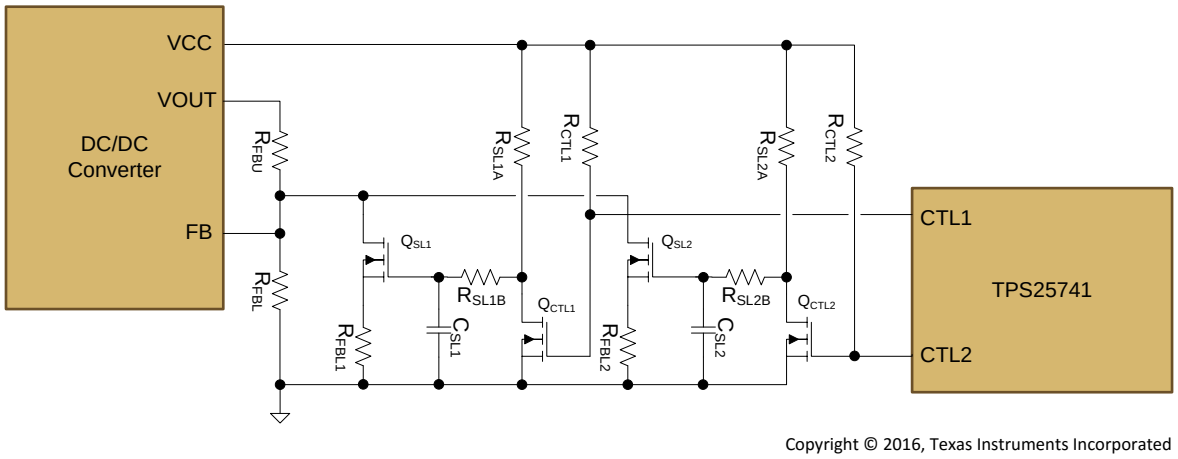


Figure 46. Slew-Rate Control Example Number 1

When V_{OUT} = 5 V, both CTL1 and CTL2 are in a high impedance state. When a 5 V to 12 V transition is requested, CTL2 goes low and turns off Q_{CTL2}. Q_{SL2} gate starts to rise towards VCC at a rate determined by R_{SL2A} + R_{SL2B} and C_{SL2}. Q_{SL2} gate continues to rise, until Q_{SL2} is fully enhanced placing R_{FBL2} in parallel with R_{FBL}. In similar fashion when CTL1 goes low, Q_{CTL1} turns off allowing R_{FBL1} to slew in parallel with R_{FBL2} and R_{FBL}.

The slewing resistors and capacitor can be chosen using the following equations. V_T is the V_{GS} threshold voltage of Q_{SL1} and Q_{SL2}. V_{REF} is the feedback regulator reference voltage. Choose the slewing resistance in the 100 kΩ range to reduce the loading on the bias voltage source (VCC) and then calculate C_{SL}. The falling transitions are shorter than the rising transitions in this topology.

Falling transitions:

- 20 V to 12 V

$$R_{SL1B} \times C_{SL1} = \frac{\Delta T_{20V-12V}}{\ln\left(\frac{V_T + V_{REF}}{V_{VCC}}\right) - \ln\left(\frac{V_T}{V_{VCC}}\right)} \quad (6)$$

- 12 V to 5 V

$$R_{SL2B} \times C_{SL2} = \frac{\Delta T_{12V-5V}}{\ln\left(\frac{V_T + V_{REF}}{V_{VCC}}\right) - \ln\left(\frac{V_T}{V_{VCC}}\right)} \quad (7)$$

Rising transitions:

- 5 V to 12 V

$$(R_{SL2A} + R_{SL2B}) \times C_{SL2} = \frac{\Delta T_{5V-12V}}{\ln\left(1 - \frac{V_T}{V_{VCC}}\right) - \ln\left(1 - \frac{V_T + V_{REF}}{V_{VCC}}\right)} \quad (8)$$

- 12 V to 20 V

$$(R_{SL1A} + R_{SL1B}) \times C_{SL1} = \frac{\Delta T_{12V-20V}}{\ln\left(1 - \frac{V_T}{V_{VCC}}\right) - \ln\left(1 - \frac{V_T + V_{REF}}{V_{VCC}}\right)} \quad (9)$$

Some converter regulators can tolerate a balance of capacitance on the feedback node without affecting loop stability. The LM5175 has been tested using Figure 47 to combine V_{OUT} slewing with a minimal amount of extra circuitry.

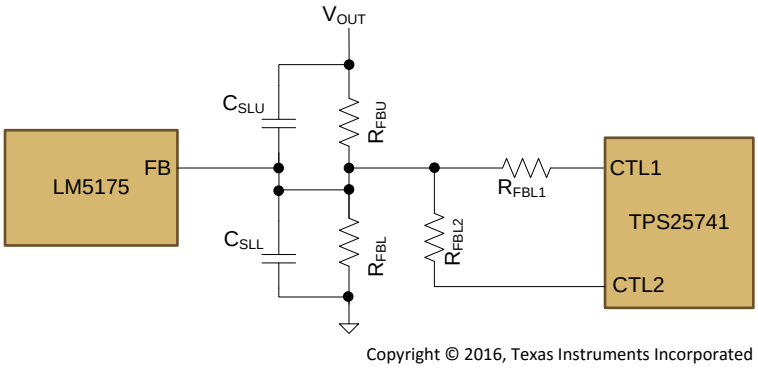


Figure 47. Slew-Rate Control Example Number 2

When a higher voltage is requested from TPS25741, CTL1 or CTL2 goes low changing the sensed voltage at the FB pin. The LM5175 compensates by increasing V_{OUT}. As V_{OUT} increases, C_{SLU} is charged at a rate proportional to R_{FBU}. Three time constants yield a voltage change of approximately 95% and can be used to calculate the desired slew time. C_{SLU} can be calculated using Equation 10 and Equation 11.

$$\Delta T_{SLEW} = 3 \times R_{FBU} \times C_{SLU} \quad (10)$$

$$C_{SLU} = \frac{\Delta T_{SLEW}}{3 \times R_{FBU}} \quad (11)$$

In order to minimize loop stability effects, a capacitor C_{SLL} in parallel with R_{FBL} is required. The ratio of C_{SLU}/C_{SLL} should be chosen to match the ratio of R_{FBL}/R_{FBU}. Choose C_{SLL} according to Equation 12.

$$C_{SLL} = C_{SLU} \times \frac{R_{FBU}}{R_{FBL}} \quad (12)$$

All slew rate control methods should be verified on the bench to ensure that the slew rate requirements are being met when the external VBUS capacitance is between 1 μF and 100 μF.

9.1.6 V_{BUS} Slew Control using GDNG C_{SLEW}

Care should be taken to control the slew rate of Q1 using C_{SLEW}; particularly in applications where C_{OUT} >> C_{SLEW}. The slew rate observed on V_{BUS} when charging a purely capacitive load is the same as the slew rate of V_{GDNG} and is dominated by the ratio I_{GDNGON} /C_{SLEW}. R_{SLEW} helps block C_{SLEW} from the GDNG pin enabling a faster transient response to OCP.

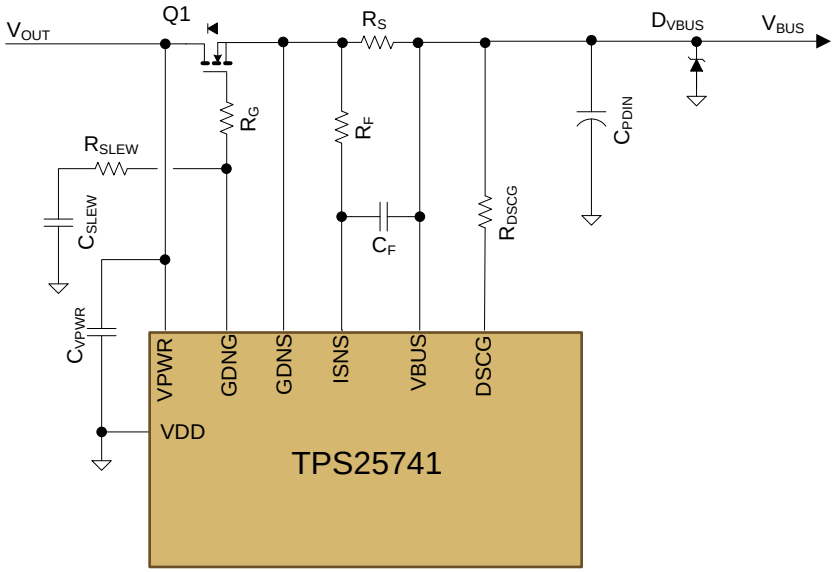


Figure 48. Slew-Rate Control Using GDNG

There may be fault conditions where the voltage on V_{BUS} triggers an OVP condition and then remains at a high voltage even after the TPS25741 configures the voltage source to output 5 V via CTL1 and CTL2. When this OVP occurs, the TPS25741 opens Q1 within t_{FOVP} + t_{FOVPDG}. The TPS25741 then issues a hard reset, discharges the power-path via the R_{DSCG}, and waits for 795 ms before enabling Q1 again. Due to the fault condition the voltage again triggers an OVP event when the voltage on V_{BUS} exceeds V_{FOVP}. This retry process would continue as long as the fault condition persists, periodically pulsing up to V_{FOVP} + $V_{SrcSlewPos}$ x (t_{FOVP} + t_{FOVPDG}) onto the V_{BUS} of the Type-C receptacle. It is recommended to use a slew rate less than the maximum of $V_{SrcSlewPos}$ (30 mV/µs), refer to *Documentation Support* section, the slew rate should instead be set in order to meet the requirement to have the voltage reach the target voltage within $t_{SrcSettle}$ (275 ms) (refer to USB Power Delivery in *Documentation Support*). This also limits the out-rush current from the C_{OUT} capacitor into the C_{PDIN} capacitor and helps protect Q1 and R_S.

9.1.7 Tuning OCP Using R_F and C_F

In applications where there are load transients or moderate ripple on C_{OUT}, the OCP performance of TPS25741 or TPS25741A may be impacted. Adding the R_F/C_F filter network as shown in Figure 49 helps mitigate the impact of the ripple and load transients on OCP performance.

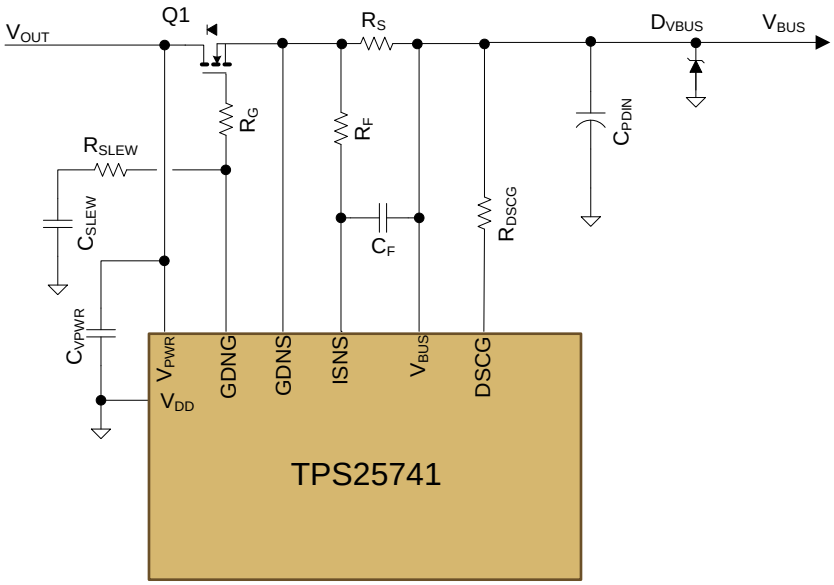


Figure 49. ISNS Filtering Example

R_F/C_F can be tailored to the amount of ripple on C_{OUT} as shown in Table 8.

Table 8. Ripple on C_{OUT}

FREQUENCY x RIPPLE (kHz x V)	SUGGESTED FILTER TIME CONSTANT (µs)
< 5 (Ex: 50 mV ripple at 100 kHz)	None
5 to 15	2.2 µs (R_F = 10 Ω, C_F = 220 nF)
15 to 35	4.7 µs (R_F = 10 Ω, C_F = 470 nF)
35 to 105	10 µs (R_F = 10 Ω, C_F = 1 µF)

9.2 Typical Applications

9.2.1 A/C Multiplexing Power Source

In this design example, two system power supply voltages are available with a limited power budget. The TPS25741 can act as a power multiplexer and switch between the two sources when requested. GDNG and G5V manage the 5-V path and GDPG manages the 12-V path. CTL2 and $\overline{\text{UFP}}$ can be used as optional power supply ON/OFF for applications where additional power saving is required and the LDO can be used to keep the TPS25741 powered when the 5-V power supply is off. The following example is based on TPS25741 Power Multiplexing Introduction and Design Considerations and TPS25741EVM-802 (refer to *Documentation Support*).

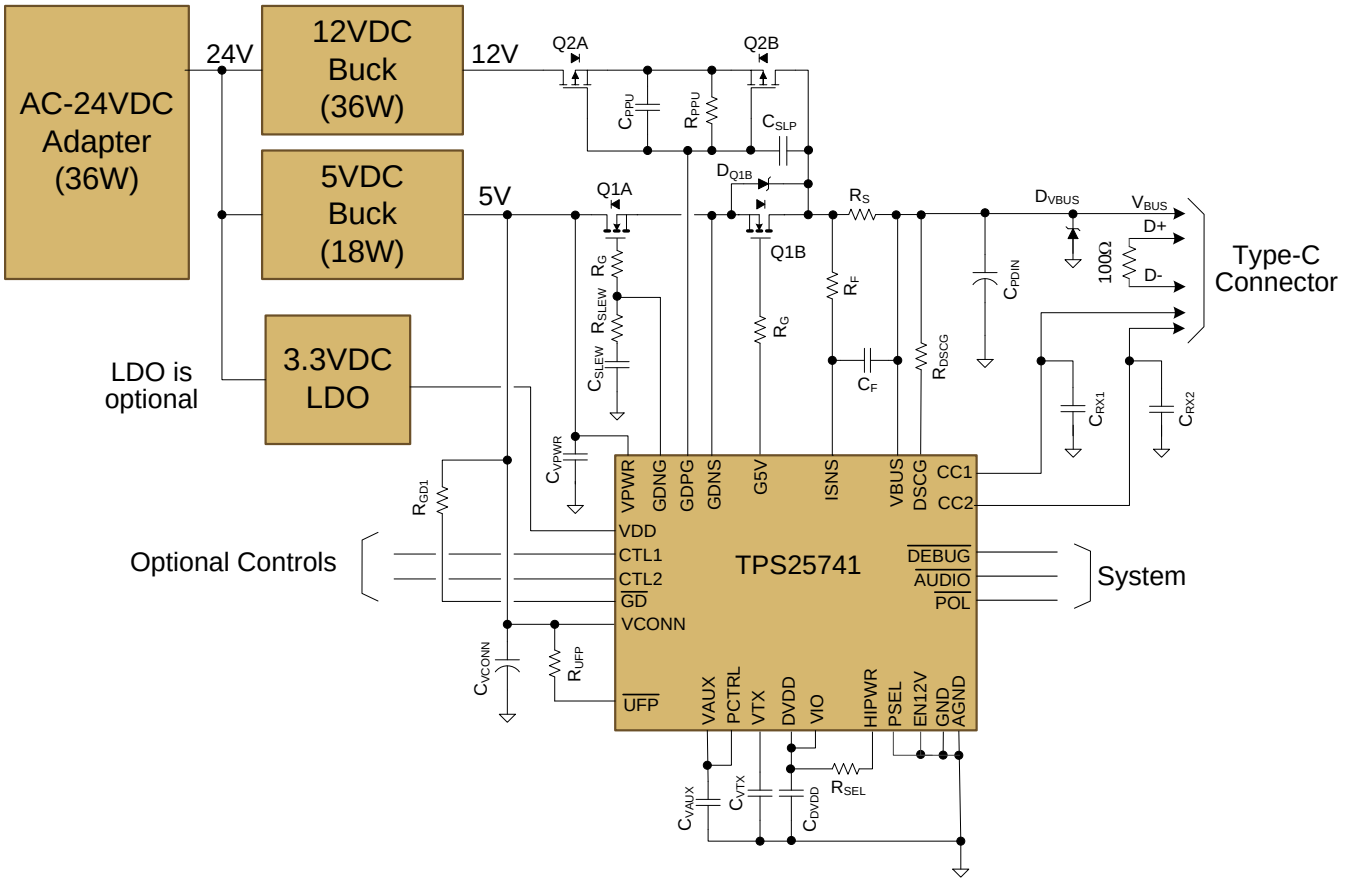


Figure 50. 12-V, 5-V Power Multiplexer Schematic

9.2.1.1 Design Requirements

Table 9. Design Parameters

DESIGN PARAMETER	VALUE
Advertised Power Limit	18 W, 36 W
Advertised Voltages	5 V, 12 V
Advertised Current Limit	3 A
Over Current Protection Set point	4.2 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Power Pin Bypass Capacitors

- C_{VPWR}: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 25 (VPWR). If VPWR is tied to a lower voltage source, then the voltage rating of the capacitor can be reduced.
- C_{VDD}: 0.1 µF, 10 V, X7R ceramic at pin 22 (VDD). If VDD is not used in the application, then tie VDD to GND. VDD and VCONN may be connected to the same 5-V supply.
- C_{VCONN}: 10 µF, 10 V, X7R ceramic at pin 3 (VCONN). If VCONN is not used in the application, then tie VCONN to GND. VCONN and VDD may be connected to the same 5-V supply.
- C_{DVDD}: 0.22 µF, 10 V, ±10%, X5R ceramic at pin 18 (DVDD)
- C_{VIO}: Connect pin 17 (VIO) to DVDD (pin 18)
- C_{VAUX}: 0.1 µF, 10 V, ±10%, X7R ceramic at pin 21 (VAUX)
- C_{VTX}: 0.1 µF, 10 V, ±10%, X7R ceramic at pin 1 (VTX)

9.2.1.2.2 Non-Configurable Components

- R_{SEL}: When the application requires advertisement using R_{SEL}, use a 100 kΩ, ±1% resistor.
- R_{PCTRL}: If PCTRL will be pulled low with an external device then it can be connected to VAUX using a 220 kΩ, ±5% resistor. If PCTRL is always high, then it can be directly connected to VAUX.
- R_{SLEW}: Use a 1 kΩ, ±1% resistor
- R_G: Use a 10 Ω, ±1% resistor
- R_{UFP}: Use a 220 kΩ, ±5% resistor
- R_{GD1}: Use a 1 MΩ, ±1% resistor

9.2.1.2.3 Configurable Components

- C_{RX}: Choose C_{RX} between 200 pF and 600 pF. A 470 pF, 50 V, ±5% COG/NPO ceramic is recommended for both CC1 and CC2 pins.
- Q_{1A}/Q_{1B}: For a 3-A application, an N-Channel MOSFET with $R_{DS(on)}$ in the 10 mΩ range is sufficient. BV_{DSS} should be rated for 30 V for applications delivering 20 V, and 25 V for 12 V applications. For this application, the TI CSD17579Q3A (SLPS527) NexFET™ is suitable.
- D_{Q1B}: During the dead time between Q1B open and Q2 closed, 5V current is sourced onto VBUS through the body diode of Q1B with a small voltage drop. To reduce the voltage drop, an external Schottky can be added in parallel with Q1B.
- Q_{2A}/Q_{2B}: For a 3-A application, an P-Channel MOSFET with $R_{DS(on)}$ in the 10 mΩ range is sufficient. BV_{DSS} should be rated for 30 V for applications delivering 20 V and 20 V for 12 V applications. For this application, the TI CSD25404Q3 (SLPS570) NexFET™ is suitable.
- R_S: TPS25741 or TPS25741A OCP set point thresholds are targeted towards a 5 mΩ, ±1% sense resistor. Power dissipation for R_S at 3 A load is approximately 45 mW.
- R_{DSCG}: The minimum value of R_{DSCG} is chosen based on the application V_{BUS}(max) and I_{DSCGT}. For V_{BUS}(max) = 12 V and I_{DSCGT} = 350 mA, R_{DSCG}(min) = 34.3 Ω. The size of the external resistor can then be chosen based on the capacitive load that needs to be discharged and the maximum allowed discharge time of 265 ms. Typically, a 120 Ω, 0.5 W resistor provides suitable performance.
- R_F/C_F: Provide filtering of both ripple and transients. For this example, RF is a 24 Ω, 5% resistor and CF is a 0.33 µF, ceramic capacitor.
- C_{PDIN}: The requirement for C_{PDIN} is 10 µF maximum. A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor is suitable for most applications.
- D_{VBUS}: D_{VBUS} provides reverse transient protection during large transient conditions when inductive loads are present. A Schottky diode with a V_{RRM} rating of 30 V in a SMA package such as the B340A-13-F provides suitable reverse voltage clamping performance.
- C_{SLEW}: To achieve a slew rate from zero to 5 V of less than 30 mV/µs using the typical GDNG current of 20 µA then C_{SLEW} (nF) > 20 µA/30 mV/µs = 0.67 nF be used. Choosing C_{SLEW} = 10 nF yields a ramp rate of 2 mV/µs.
- R_{FBL1}/R_{FBL2}: Not used
- C_{SLU}/C_{SLL}: Not used
- R_{PPU}: R_{PPU} is the Q2 gate drive pullup resistor. The TPS25741 applies a sink current of 40 µA typical to turn

on Q2 and R_{PPU} should be large enough to fully enhance Q2 but not too large as it also discharges C_{SLP} during turn off. The CSD25404Q3 lists an acceptable $R_{DS(on)}$ with V_{GS} = -4.5V and I_D = -10A. Using $I_{GMV(min)}$ = 34 µA and V_{GS} = -4.5V yields R_{PPU} = 132kΩ. Use a standard 1% resistor = 133kΩ resistor for R_{PPU}.

- C_{SLP}: C_{SLP} provides slew rate and inrush current limiting from the 12 V supply during VBUS transition from 5 V to 12 V. While the sink is attached, there could be as much as 110 µF on VBUS. The slew time must be > 233 µs and the inrush current must be < 3.85 A (V_{ITRIP}(min)/RS). For this design, target an inrush current of 2 A during 5 V to 12 V slew. The charge rate across C_{SLP} will be the same as for the 110 µF load capacitor such that $I_{LOAD}/C_{LOAD} = I_{CSLP}/C_{SLP}$. Using the CSD25404Q3 Gate Charge curve, a plateau threshold voltage of V_{PTH} ~ 1.8 V can be used to calculate C_{SLP} with the equations below.

$$C_{SLP} = C_{LOAD} \times \frac{I_{CSLP}}{I_{LOAD}} = C_{LOAD} \times \frac{I_{GDPG} - \frac{V_{PTH}}{R_{PPU}}}{I_{LOAD}} \quad (13)$$

C_{LOAD} = 110 µF, I_{GDPG} = 40 µA, V_{PTH} = 1.8V, R_{PPU} = 133 kΩ, I_{LOAD} = 2 A (14)

$$C_{SLP} = 110\mu F \times \frac{40\mu A - \frac{1.8V}{133k\Omega}}{2A} = 1.46nF \quad (15)$$

Choose C_{SLP} = 1.5 nF

$$\text{Slew time} = C_{SLP} \times \frac{12V - 5V}{I_{GDPG} - \frac{V_{PTH}}{R_{PPU}}} = 1.5nF \times \frac{7V}{40\mu A - \frac{1.8V}{133k\Omega}} = 397\mu s \quad (16)$$

- C_{PPU}: C_{PPU} contributes a small Q2 turn on delay just prior to the 5 V to 12 V transition, but the primary function is to inhibit Q2 output turn on during ramp up of the 12 V power supply. When the 12 V power supply is OFF C_{SLP} will be discharged. As the 12 V power supply ramps up, the common sources of Q2 will rise and C_{SLP} will be charged through R_{PPU}. C_{PPU} is required to prevent Q2 V_{GS} from exceeding the turn on threshold and prematurely charging VBUS for the case where the 12V bus ramps up quickly. C_{PPU} and C_{SLP} form a capacitive divider network with $V_{GS(th)} \approx 12\ V \times C_{SLP} / (C_{SLP} + C_{PPU})$. Choose $C_{PPU} \approx (12\ V/V_{GS(th)} - 1) \times C_{SLP}$. For this example, $V_{GS(th)}$ = 0.9 V and C_{PPU} = 18 nF. If the 12 V power supply is enabled while the 5 V supply is on then C_{PPU} can be smaller set by the voltage difference between the 12 V and 5 V supply. Always validate the final design on the test bench.
- For faster fault turn off, Q3 can be connected as shown in Figure 51 and triggered using the GDNG pin. Q3 must have a ±20V V_{GS}(max) rating for 20 V muxing applications.

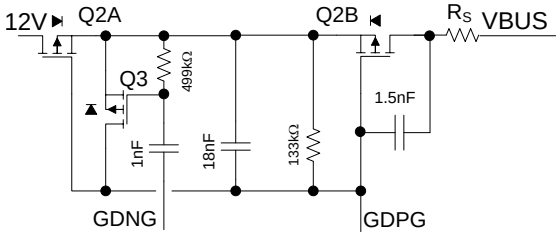
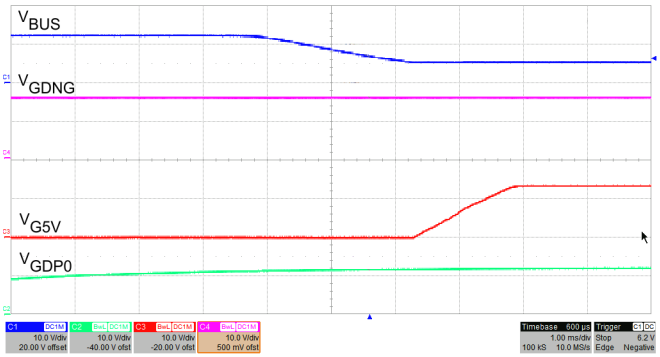


Figure 51. Fast Turnoff Circuit

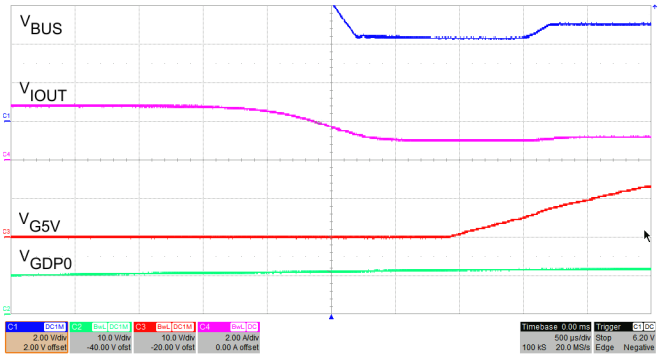
- Power Supply ON/OFF Considerations: For applications that can disable one or both of the power supplies, additional considerations apply. Refer to the TPS25741EVM-802 User Guide (refer to *Documentation Support*). for more information.

9.2.1.3 Application Curves



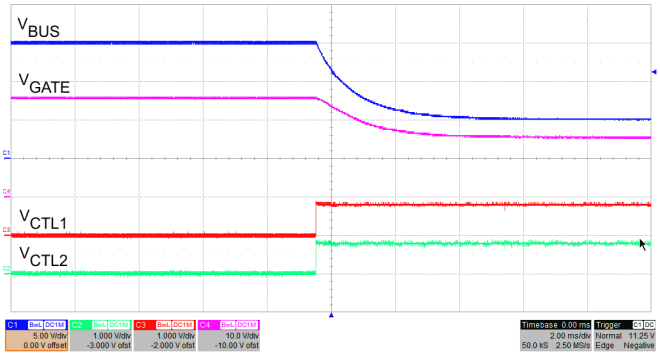
No Load

Figure 52. VBUS 12 V – 5 V Transition, TPS25741



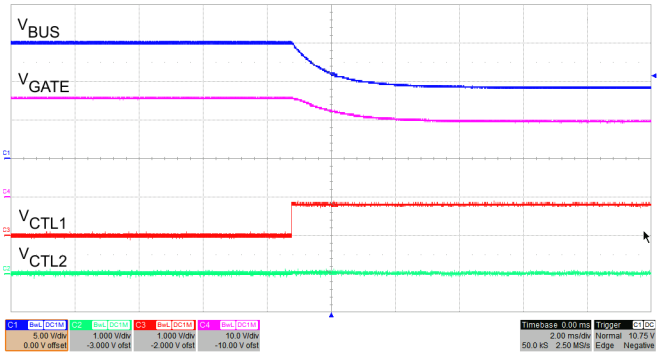
Zoomed 4Ω, 100µF

Figure 53. VBUS 12 V – 5 V Transition, TPS25741



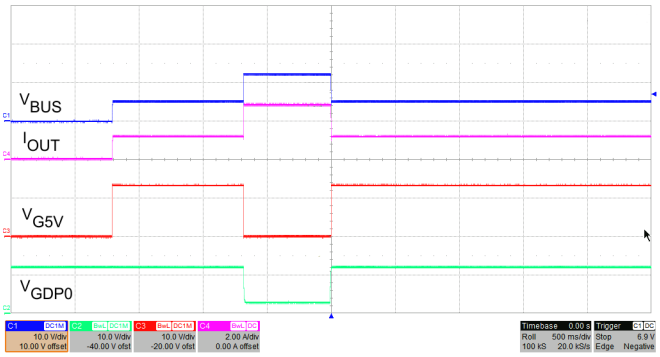
No Load

Figure 54. VBUS 15 V – 5 V Transition, TPS25741A



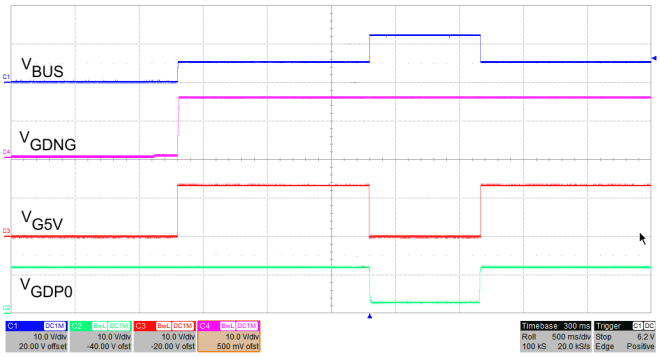
No Load

Figure 55. VBUS 15 V – 9 V Transition, TPS25741A



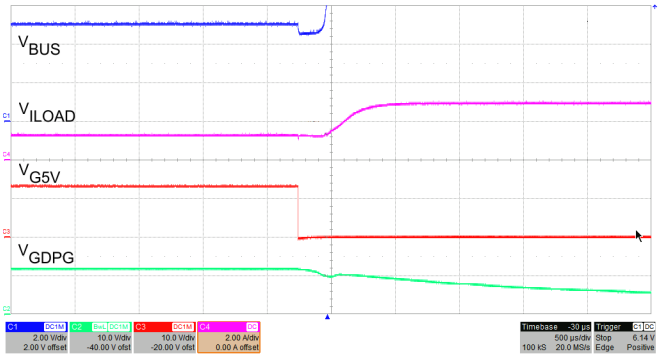
4Ω, 100µF

Figure 56. VBUS 5 V – 12 V – 5 V Transition, TPS25741



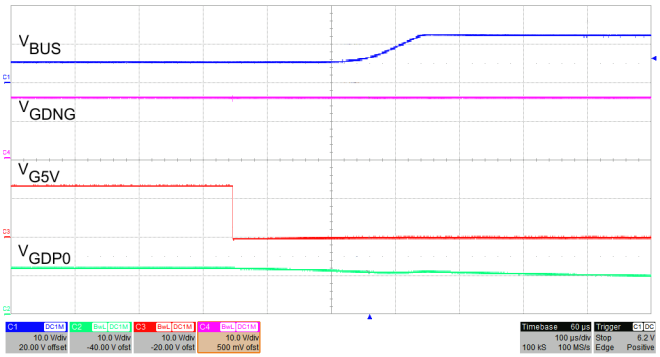
No Load

Figure 57. VBUS 5 V – 12 V – 5 V Transition, TPS25741



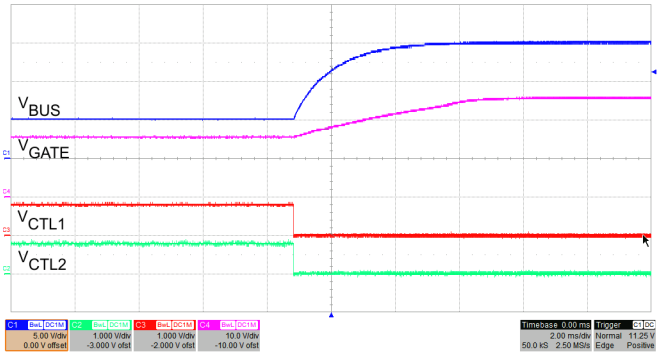
Zoomed 4Ω, 100µF

Figure 58. VBUS 5 V – 12 V Transition, TPS25741



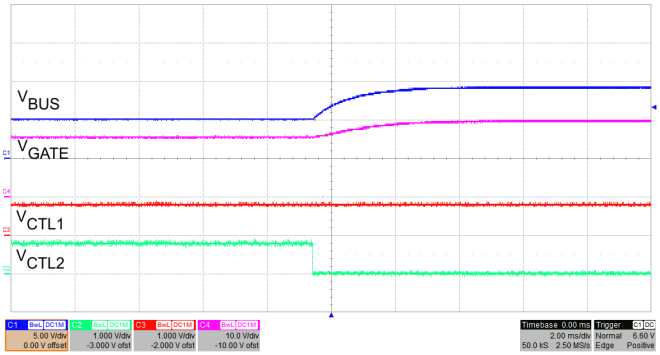
No Load Zoomed

Figure 59. VBUS 5 V – 12 V Transition, TPS25741



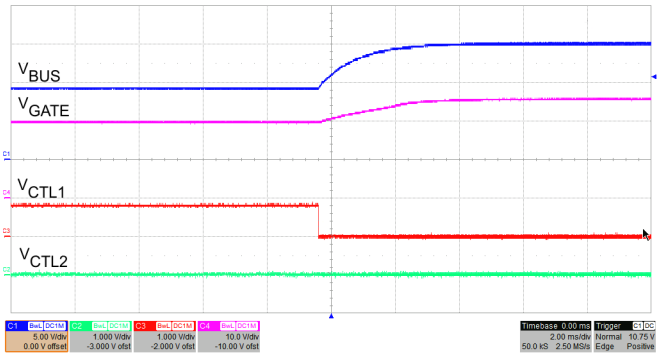
No Load

Figure 60. VBUS 5 V – 15 V Transition, TPS25741A



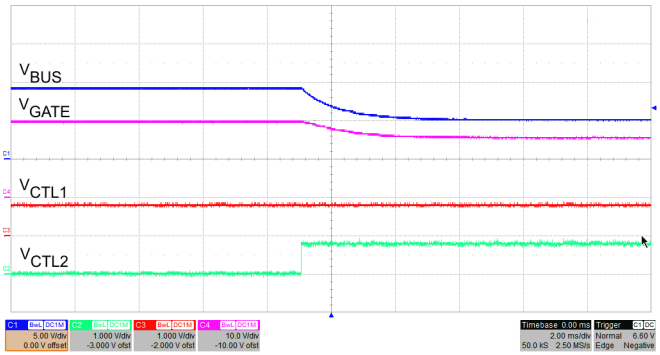
No Load

Figure 61. VBUS 5 V – 9 V Transition, TPS25741A



No Load

Figure 62. VBUS 9 V – 15 V Transition, TPS25741A



No Load

Figure 63. VBUS 9 V – 5 V Transition, TPS25741A

9.2.2 D/C Power Source

In this design example the P_{SEL} is configured such that P_{SEL} = 65 W (see Table 10). Voltages offered are 5 V, 9 V, and 15 V at a maximum of 3 A. The overcurrent protection (OCP) trip point is set just above 3 A and VDD on the TPS25741A is grounded.

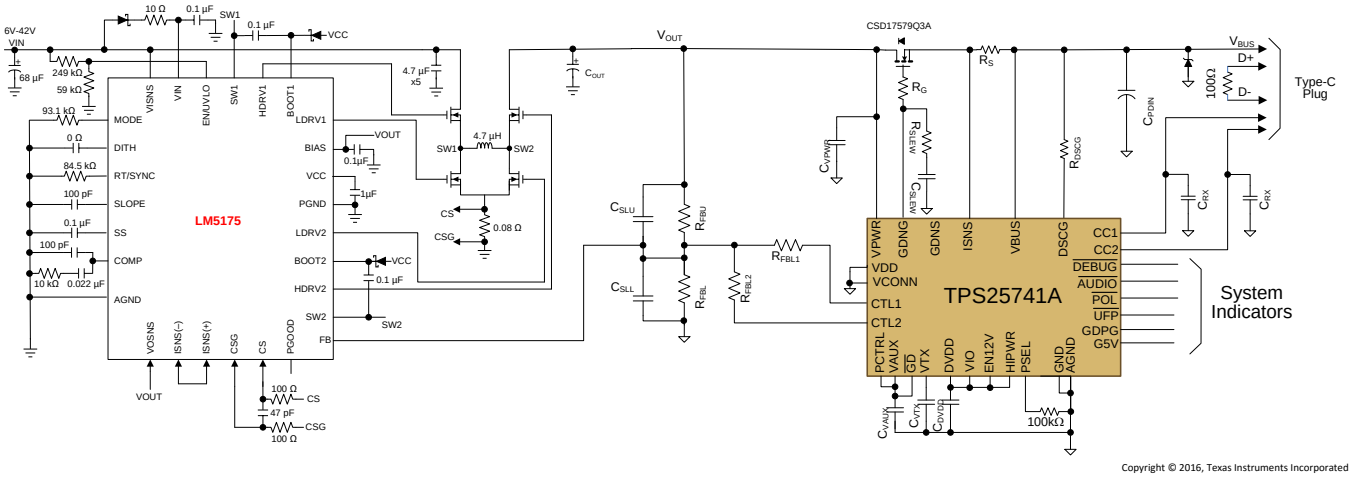


Figure 64. DC Power Source

9.2.2.1 Design Requirements

Table 10. Design Parameters

DESIGN PARAMETER	VALUE
Advertised Power Limit	65 W
Advertised Voltages	5 V, 9 V, 15 V
Advertised Current Limit	3 A
Over Current Protection Set point	4.2 A

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Power Pin Bypass Capacitors

- C_{VPWR}: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 25 (VPWR)
- C_{VDD}: 0.1 µF, 50 V, X7R ceramic at pin 22 (VDD). If VDD is not used in the application, then tie VDD to GND. VDD and VCONN may be connected to the same 5-V supply.
- C_{VCONN}: 10 µF, 10 V, X7R ceramic at pin 3 (VCONN). If VCONN is not used in the application, then tie VCONN to GND. VCONN and VDD may be connected to the same 5-V supply.
- C_{DVDD}: 0.22 µF, 10 V, ±10%, X5R ceramic at pin 18 (DVDD)
- C_{VIO}: Connect pin 17 (VIO) to DVDD (pin 18)
- C_{VAUX}: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 21 (VAUX)
- C_{VTX}: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 1 (VTX)

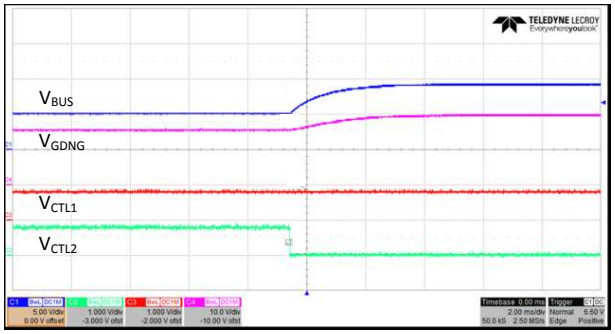
9.2.2.2.2 Non-Configurable Components

- R_{SEL}: When the application requires advertisement using R_{SEL}, use a 100 kΩ, ±1% resistor.
- R_{PCTRL}: If PCTRL will be pulled low with an external device then it can be connected to VAUX using a 220 kΩ, ±5% resistor. If PCTRL will always be high then it can be directly connected to VAUX.
- R_{SLEW}: Use a 1 kΩ, ±1% resistor
- R_G: Use a 10 Ω, ±1% resistor

9.2.2.2.3 Configurable Components

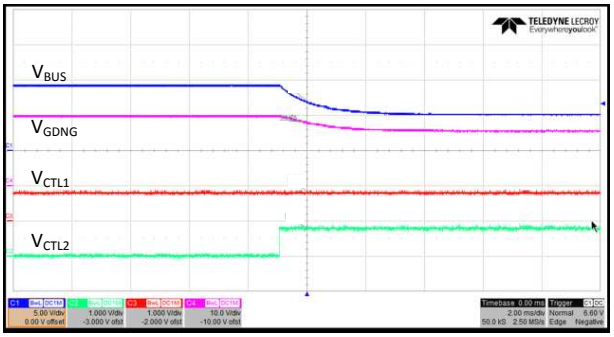
- C_{RX}: Choose C_{RX} between 200 pF and 600 pF. A 470 pF, 50 V, ±5% COG/NPO ceramic is recommended for both CC1 and CC2 pins.
- Q_1: For a 3 A application, an N-Channel MOSFET with $R_{DS(on)}$ in the 10 mΩ range is sufficient. BV_{DSS} should be rated for 30 V for applications delivering 20 V, and 25 V for 12 V applications. For this application, the TI CSD17579Q3A (SLPS527) NexFET™ is suitable.
- R_S: TPS25741 or TPS25741A OCP set point thresholds are targeted towards a 5 mΩ, ±1% sense resistor. Power dissipation for R_S at 3 A load is approximately 45 mW.
- R_{DSCG}: The minimum value of R_{DSCG} is chosen based on the application V_{BUS}(max) and I_{DSCGT}. For V_{BUS}(max) = 12 V and $I_{(DSCGT)}$ = 350 mA, R_{DSCG}(min) = 34.3 Ω. The size of the external resistor can then be chosen based on the capacitive load that needs to be discharged and the maximum allowed discharge time of 90 ms. Typically, a 120 Ω, 0.5 W resistor provides suitable performance.
- R_F/C_F: Not used
- C_{PDIN}: The requirement for C_{PDIN} is 10 µF maximum. A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor is suitable for most applications.
- D_{VBUS}: D_{VBUS} provides reverse transient protection during large transient conditions when inductive loads are present. A Schottky diode with a V_{RRM} rating of 30 V in a SMA package such as the B340A-13-F provides suitable reverse voltage clamping performance.
- C_{SLEW}: To achieve a slew rate from zero to 5 V of less than 30 mV/µs using the typical GDNG current of 20 µA then C_{SLEW} (nF) > 20 µA/30 mV/µs = 0.67 nF be used. Choosing C_{SLEW} = 10 nF yields a ramp rate of 2 mV/µs.
- R_{FBL1}/R_{FBL2}: In this design example, R_{FBU} = 49.9 kΩ and R_{FBL} = 9.53 kΩ. The feedback error amplifier V_{REF} = 0.8 V. Using the equations for R_{FBL2} (Equation 4 and Equation 5) provide a calculated value of 9.9 kΩ and a selected value of 9.76 kΩ. In similar fashion for R_{FBL1}, a calculated value of 6.74 kΩ and a selected value of 6.65 kΩ is provided.
- C_{SLU}/C_{SLL}: The value of C_{SLU} is calculated based on the desired 95% slew rate of 3 ms. C_{SLU} = 3 ms/(3 x 49.9 kΩ) = 20 nF. Choose a 22-nF capacitor for C_{SLU}. Next, C_{SLL} is calculated as C_{SLU} x (R_{FBU}/R_{FBL}) = 22 nF x (49.9 kΩ/9.53 kΩ) = 115 nF. Choose a 100-nF capacitor for C_{SLL}.

9.2.2.3 Application Curves



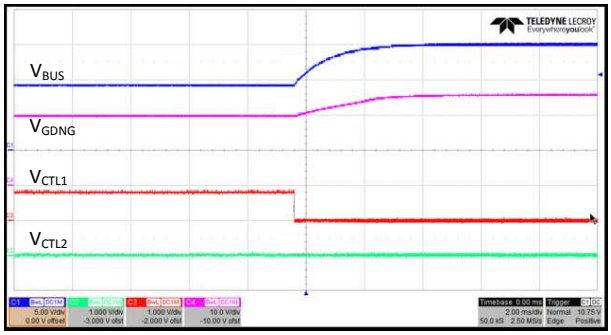
No Load

Figure 65. VBUS 5 V – 9 V Transition



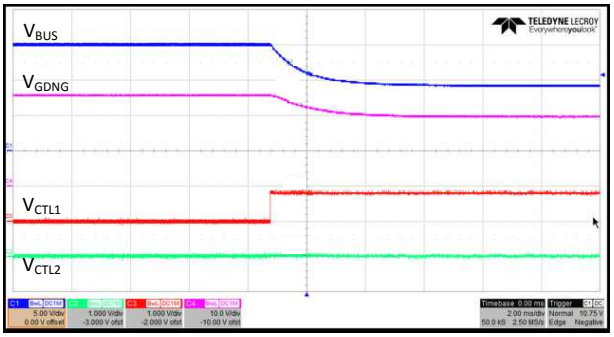
No Load

Figure 66. VBUS 9 V – 5 V Transition



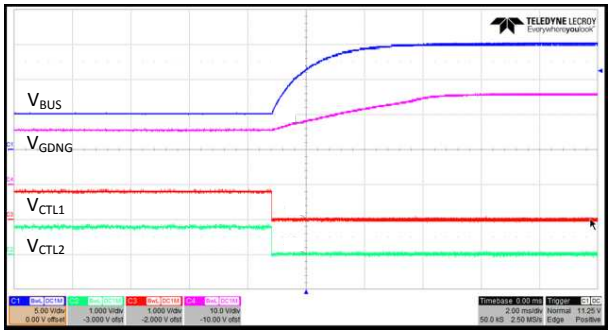
No Load

Figure 67. VBUS 9 V – 15 V Transition



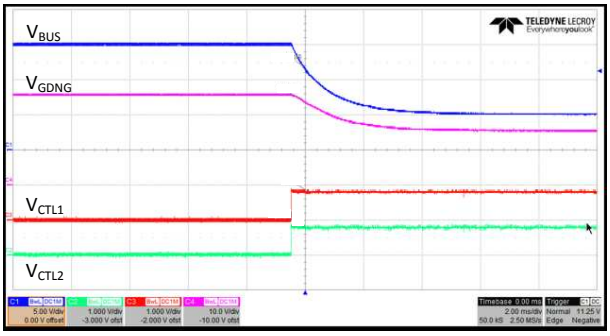
No Load

Figure 68. VBUS 15 V – 9 V Transition



No Load

Figure 69. VBUS 5 V – 15 V Transition



No Load

Figure 70. VBUS 15 V – 5 V Transition

9.3 System Examples

9.3.1 A/C Power Source (Wall Adapter)

In this system design example, the PSEL is configured such that P_{SEL} = 36 W, and only 5 V and 12 V are offered at a maximum of 3 A. The over-current protection (OCP) trip point is set just above 3 A. VDD on the TPS25741 is grounded, if there is a suitable power supply available in the system the TPS25741 operates more efficiently if it is connected to VDD since $V_{VPWR} > V_{VDD}$.

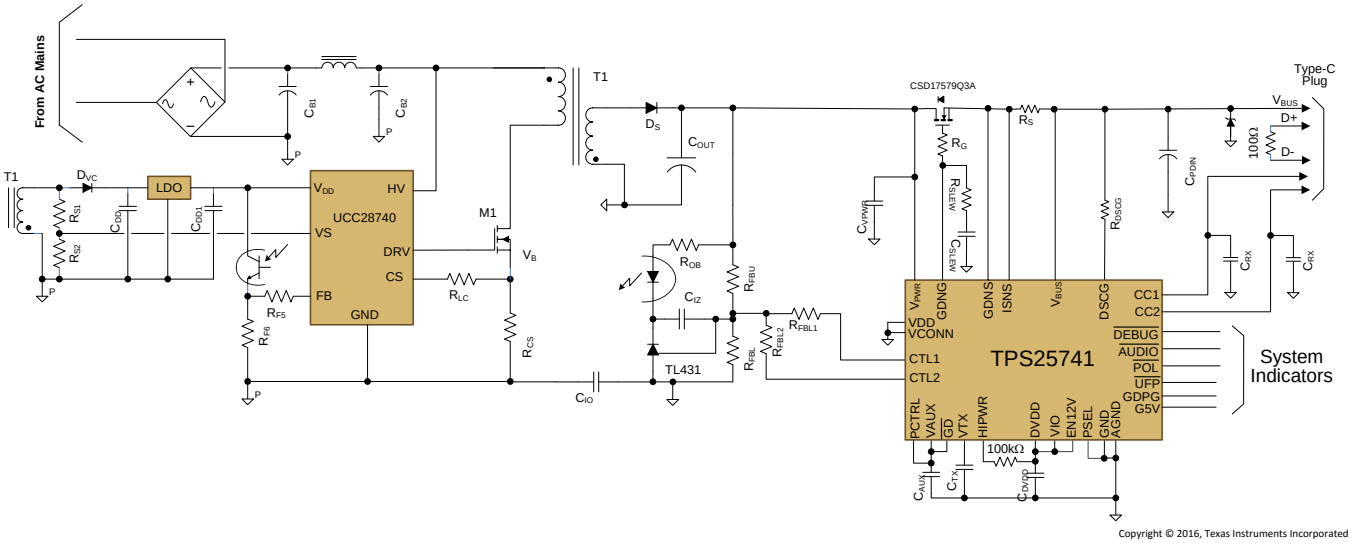


Figure 71. Adapter Provider Concept

System Examples (continued)

9.3.2 Dual-Port Power Managed A/C Power Source (Wall Adapter)

In this system design example, the PSEL is configured such that P_{SEL} = 36 W, and only 5 V and 12 V are offered at a maximum of 3 A. The over-current protection (OCP) trip point is set just above 3 A.

The $\overline{UFP}$ pin from one TPS25741 is attached to the PCTRL pin on the other TPS25741. When one port is not active (no UFP attached through the receptacle) its $\overline{UFP}$ pin is left high-z so the PCTRL pin on the other port is pulled high. This allows the adaptor to provide up to the full 36 W on a single port if a single UFP is attached. If two UFP's are attached (one to each port) then each port only offers current that would reach a maximum of 18 W. So each port is allocated half of the overall power when each port has a UFP attached.

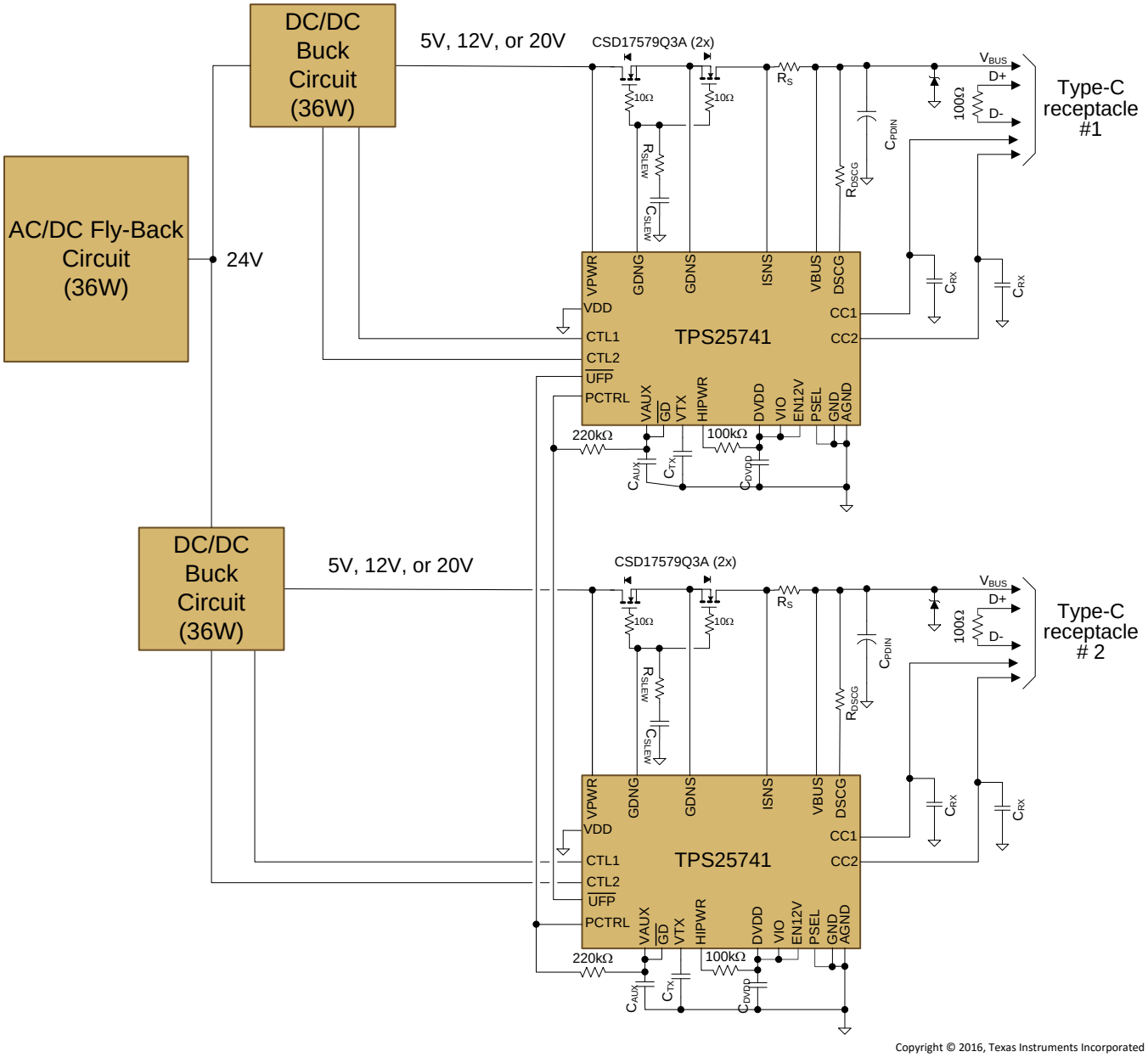


Figure 72. Dual-Port Adapter Provider Concept

10 Power Supply Recommendations

10.1 VDD

The recommended VDD supply voltage range is 3 V to 5.5 V. The device requires approximately 2 mA (I_{SUPP}) typical in normal operating mode and below 10 µA in sleep mode. If the VDD supply is not used, then it may be connected to AGND/GND.

10.2 VCONN

The recommended VCONN supply voltage range is 4.65 V to 5.5 V. If the VCONN supply is not used, then it may be connected to AGND/GND.

10.3 VPWR

The recommended VPWR supply voltage range is 0 V to 25 V. The device requires approximately 2 mA (I_{SUPP}) typical in normal operating mode and below 10 µA in sleep mode.

11 Layout

11.1 Layout Guidelines

11.1.1 Port Current Kelvin Sensing

Figure 73 provides a routing example for accurate current sensing for the overcurrent protection feature. The sense amplifier measurement occurs between the ISNS and VBUS pins of the device. Improper connection of these pins can result in poor OCP performance.

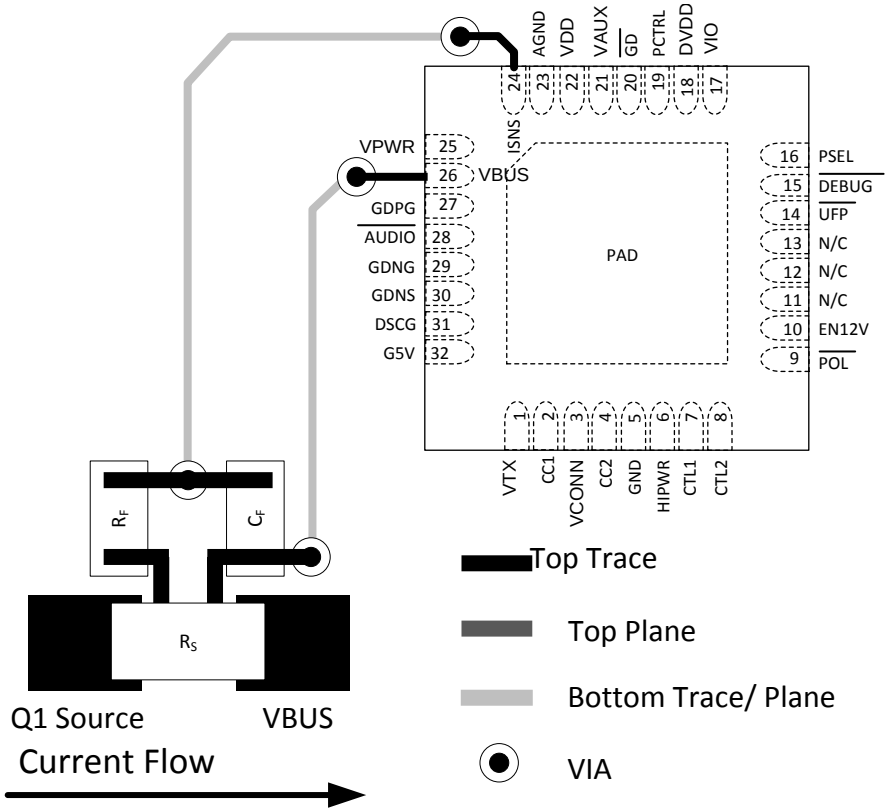


Figure 73. Kelvin Sense Layout Example

11.1.2 Power Pin Bypass Capacitors

- C_{VPWR}: Place close to pin 25 (VPWR) and connect with low inductance traces and vias according to Figure 74.
- C_{VDD}: Place close to pin 22 (VDD) and connect with low inductance traces and vias according to Figure 74.
- C_{VCONN}: Place close to pin 3 (VDD) and connect with low inductance traces and vias according to Figure 74.
- C_{DVDD}: Place close to pin 18 (DVDD) and connect with low inductance traces and vias according to Figure 74.
- C_{VIO}: Place close to pin 17 (VDD) and connect with low inductance traces and vias according to Figure 74.
- C_{VAUX}: Place close to pin 21 (VAUX) and connect with low inductance traces and vias according to Figure 74.
- C_{VTX}: Place close to pin 1 (VTX) and connect with low inductance traces and vias according to Figure 74.

11.1.3 Supporting Components

- C_{RX}: Place C_{RX1} and C_{RX2} in line with the CC1 and CC2 traces as shown in Figure 26. These should be placed within one inch from the Type C connector. Minimize stubs and tees from on the trace routes.
- Q_1: Place Q_1 in a manner such that power flows uninterrupted from Q_1 drain to the Type C connector VBUS connections. Provide adequate copper plane from Q_1 drain and source to the interconnecting circuits.
- R_S: Place R_S as shown in Figure 74 to facilitate uninterrupted power flow to the Type C connector. Orient R_S for optimal Kelvin sense connection/routing back to the TPS25741 or TPS25741A. In high current applications

Layout Guidelines (continued)

where the power dissipation is over 250 mW, provide an adequate copper feed to the pads of R_S.

- R_G: Place R_G near Q_1 as shown in Figure 74. Minimize stray leakage paths as the GDNG sourcing current could be affected.
- R_{SLEW}/C_{SLEW}: Place R_{SLEW} and C_{SLEW} near RG as shown in Figure 74.
- R_{DSCG}: Place on top of the VBUS copper route and connect to the DSCG pin with a 15 mil trace.
- R_F/C_F: When required, place R_F and C_F as shown in Figure 74 to facilitate the Kelvin sense connection back to the device.
- C_{VBUS}/D_{VBUS}: Place C_{VBUS} and D_{VBUS} within one inch of the Type C connector and connect them to VBUS and GND using adequate copper shapes.
- R_{SEL}/R_{PCTRL}: Place R_{SEL} and R_{PCTRL} near the device.

11.2 Layout Example

The basic component placement and layout is provided in Figure 74. This layout represents the circuit shown in Figure 41. The layout for other power configurations will vary slightly from that shown below.

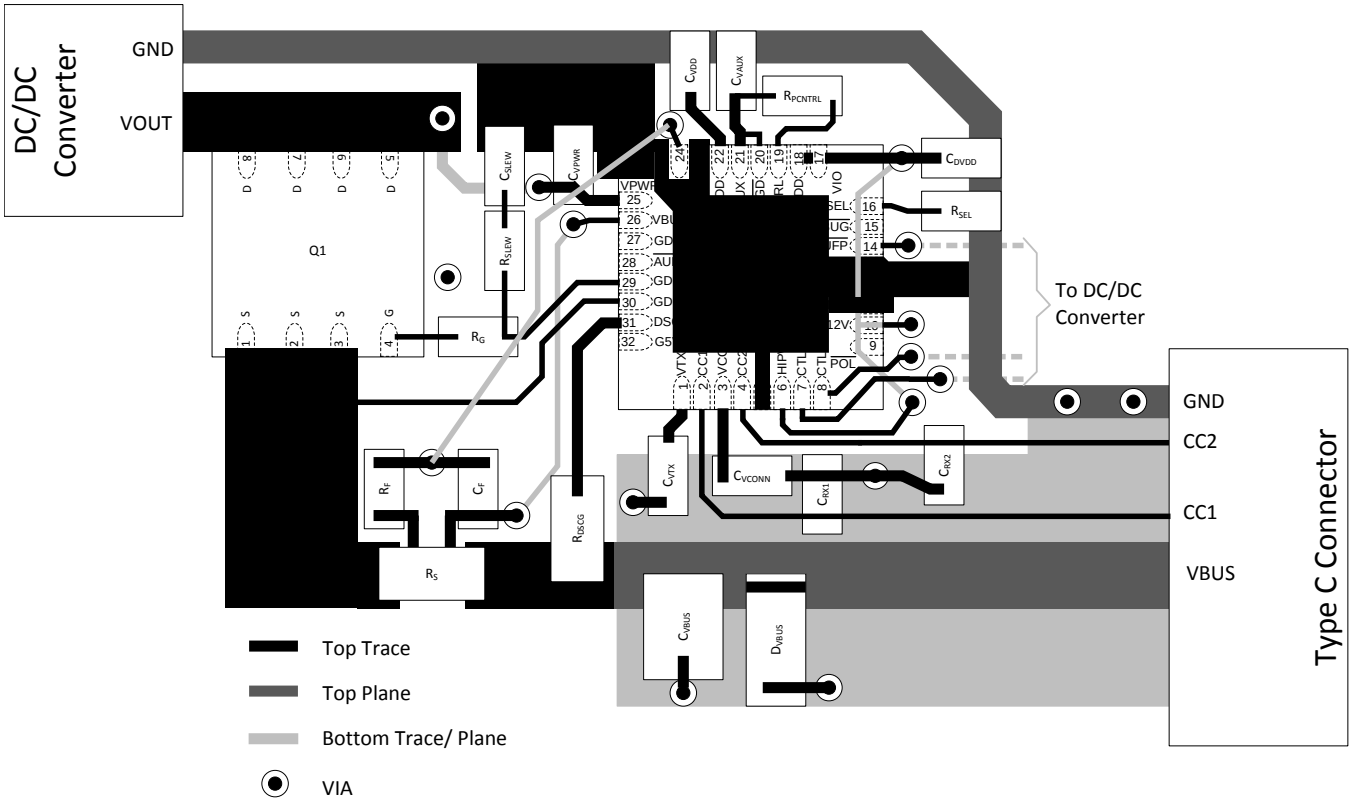


Figure 74. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

USB Power Delivery and USB Type-C specifications available at: http://www.usb.org/home

TPS25741EVM-802 and TPS25741AEVM-802 EVM User's Guide for Desktops

TPS25741/TPS25741A Design Calculator Tool

TPS25741 Power Multiplexing Introduction and Design Considerations

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS25741	Click here	Click here	Click here	Click here	Click here
TPS25741A	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25741ARSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25741A	Samples
TPS25741ARSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25741A	Samples
TPS25741RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTPS BX 25741	Samples
TPS25741RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTPS BX 25741	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

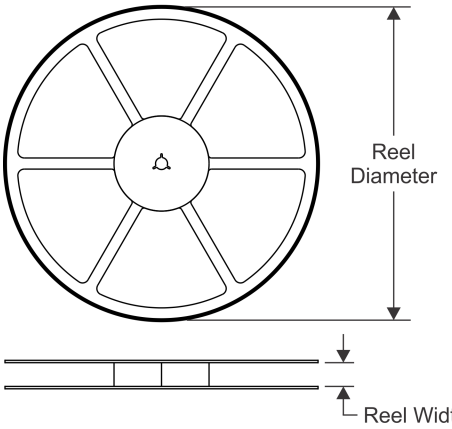
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

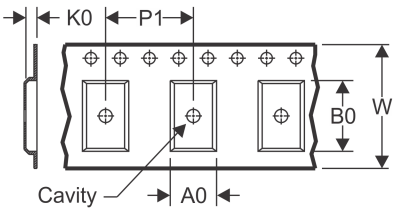
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

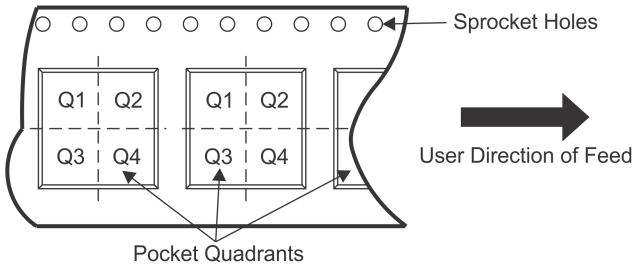


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

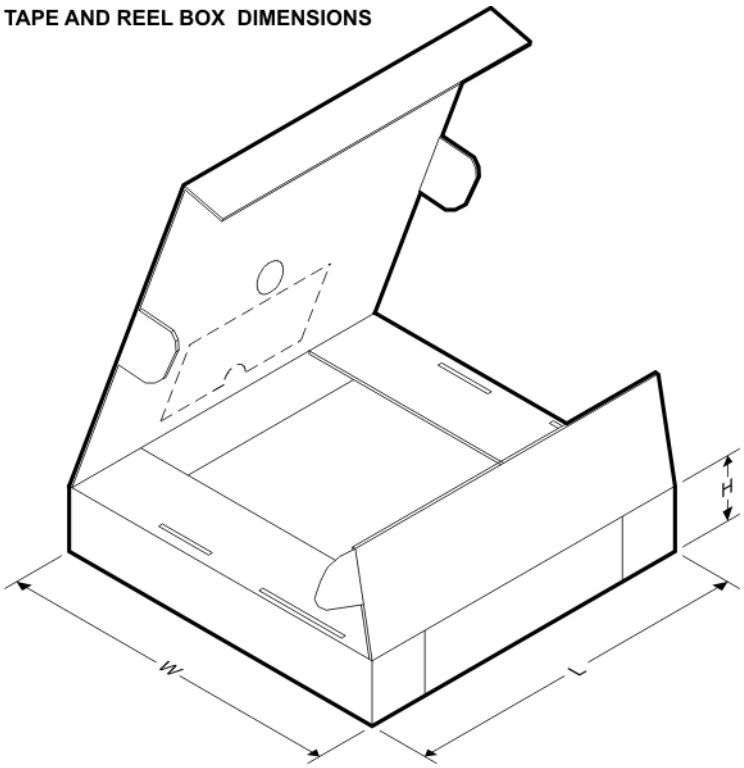
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25741ARSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25741ARSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25741RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25741RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

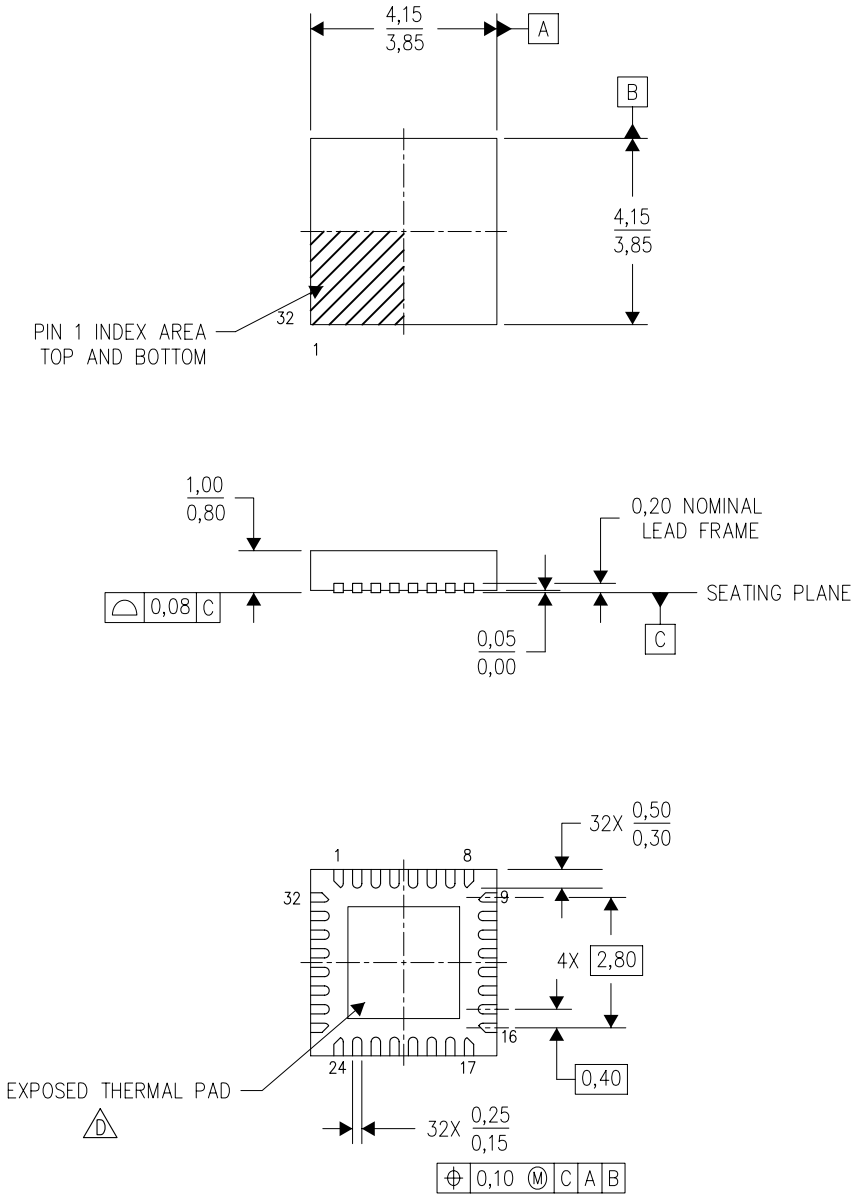
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25741ARSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS25741ARSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TPS25741RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS25741RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

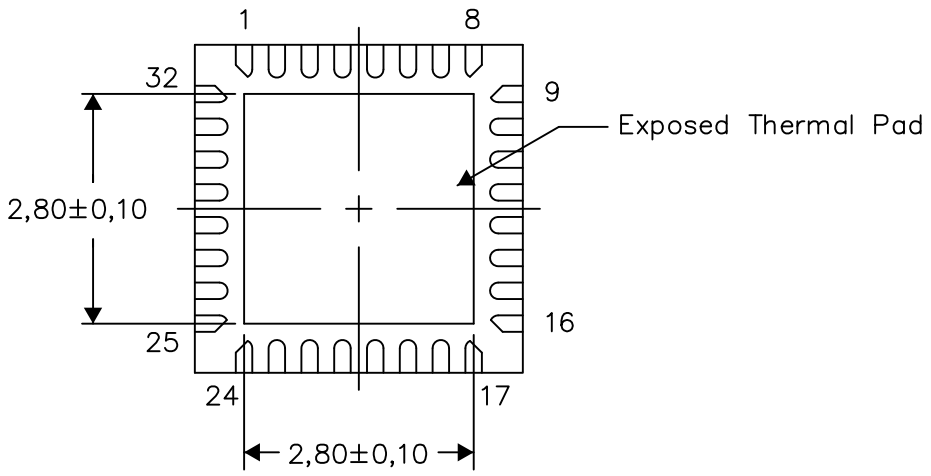
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



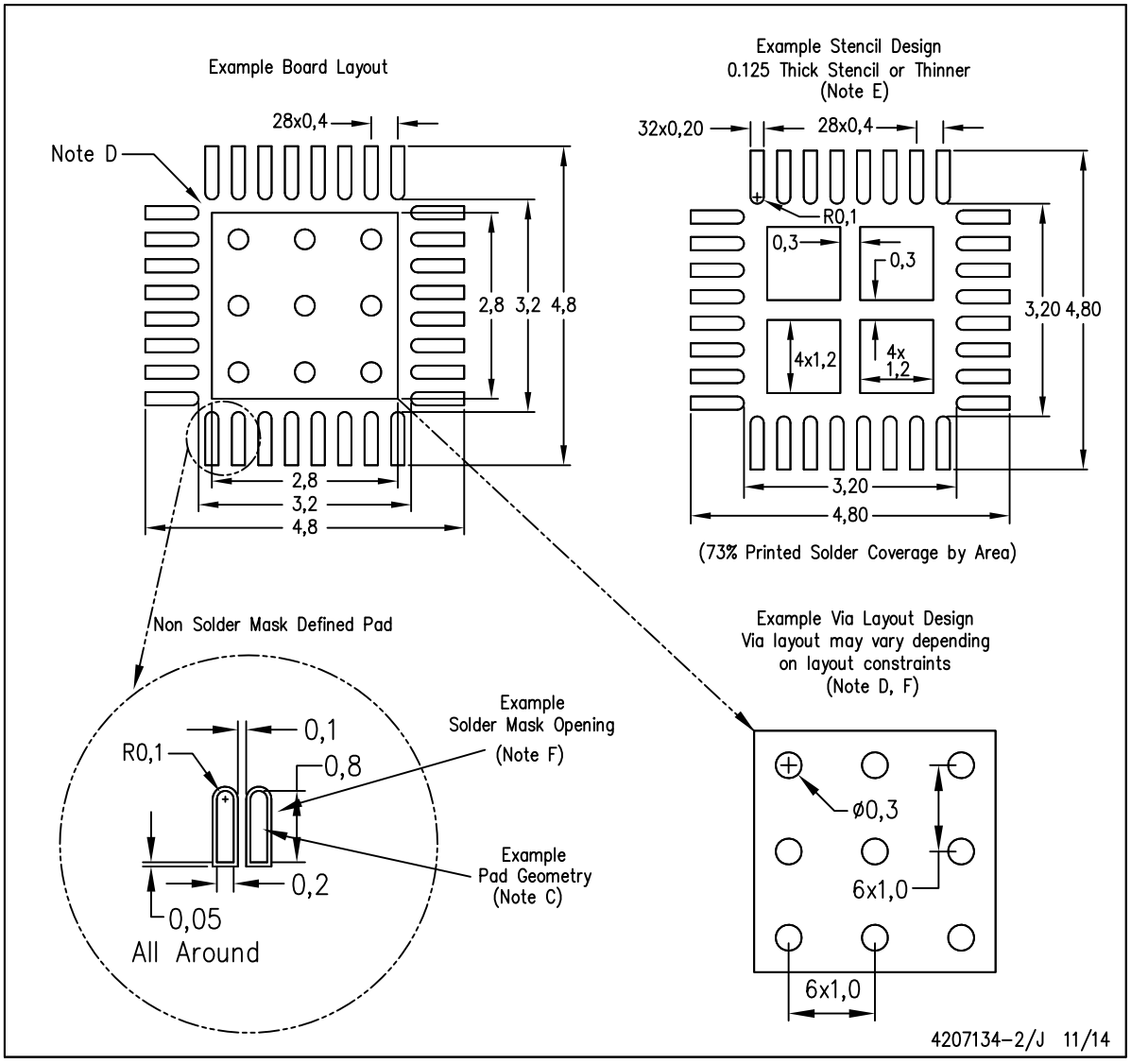
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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