TPS544x20 4.5V 至 18V，20A 和 30A SWIFT ™ 同步降压控制器，此控制器具有 PMBus™

1 特性

- 启用 PMBus 的转换器：20A，30A
- 4.5V 至 18V 输入，0.6V 至 5.5V 输出
- 5mm x 7mm 薄型四方扁平无引线 (LQFN) 封装，焊球间距为 0.5mm
- 单个散热焊盘
- 集成 4.5mΩ 和 2.0mΩ 堆叠 NexFET™ 功率级
- 600mV，0.5% 基准
- 无损耗、低侧金属氧化物半导体场效应晶体管 (MOSFET) 电流感测
- 可选 D-CAP™ 和 D-CAP2™ 模式控制
- 差分远程感应
- 单启动至预偏置输出
- 输出电压裕度和修整
- 输出电压和输出电流报告
- 使用 2N3904 时的外部温度监视
- 可经由 PMBus 编程
  - 过流保护
  - 欠压闭锁 (UVLO)，软启动
  - 电源正常 (PGOOD)，过压 (OV)，欠压 (UV)，过热 (OT) 电平
  - 故障响应
  - 接通和关闭延迟
- 热关断
- 引脚兼容 20A，30A 转换器

2 应用范围

- 测试和测量仪器
- 以太网交换机、光交换机、路由器、基站
- 服务器
- 企业级存储固态硬盘 (SSD)
- 高密度电源解决方案

3 说明

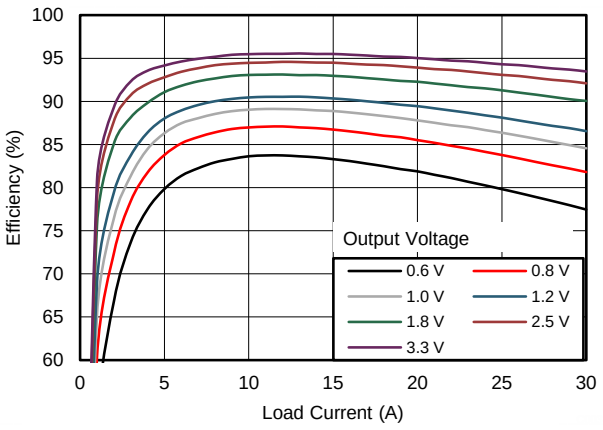
TPS544B20 和 TPS544C20 器件是 PMBus 兼容、非隔离式直流-直流集成场效应晶体管 (FET) 转换器，此转换器能够以 5mm x 7mm 封装支持高频运行并传送 20A 或 30A 电流输出，从而用尽可能小的印刷电路板 (PCB) 面积实现高功率密度和快速瞬态性能。 PMBus 接口用于转换器配置，并监视关键参数，其中包括输出电压、电流和一个可选外部温度。 由集成 NexFET 功率级和经优化驱动器提供的高频、低损耗开关可实现极高密度电源解决方案以及减小的电感器和滤波电容器尺寸。 根据系统要求，对故障情况的响应可被设定为重新启动或锁断。

器件信息(1)

部件名称	封装	封装尺寸（标称值）
TPS544B20	LQFN (40)	5.00mm x 7.00mm
TPS544C20		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

效率与输出电流间的关系



V_{IN} = 12 V　L = 410 nH　Snubber = Open
f_{SW} = 500 kHz　R_{DCR} = 0.3 mΩ　R_{BOOT} = 0 Ω

目录

4 修订历史记录

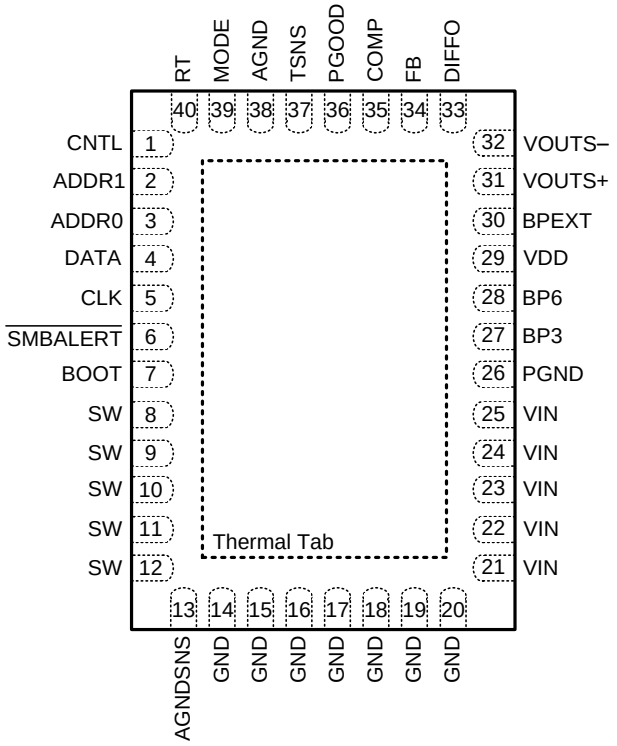
日期	修订版本	注释
2014 年 5 月	*	最初发布。

5 Device Comparison Table

ORDER NUMBER	QTY	REEL SIZE (mm)	CURRENT OPTION (A)
TPS544B20RVFR	3000	330	20
TPS544B20RVFT	250	180	
TPS544C20RVFR	3000	330	30
TPS544C20RVFT	250	180	

6 Pin Configuration and Functions

RVF (LQFN) PACKAGE
40 PINS
(TOP VIEW)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ADDR0	3	O	Sets low order 3-bits of the PMBus address. Connect a resistor from this pin to AGND.
ADDR1	2	O	Sets high order 3-bits of the PMBus address. Connect a resistor from this pin to AGND.
AGNDSNS	13	G	Analog ground sense. Provides Kelvin connection point to analog ground for precise current measurement. AGNDSNS is internally connected to the thermal tab. Do not connect to the thermal tab externally. Kelvin connect back to AGND pin with a low impedance, low noise path. This kelvin connection serves as the only connection between AGND and GND.
AGND	38	G	Analog ground return for control circuitry. AGND should not be connected to the exposed thermal pad, GND or PGND, but should be kelvin connected to the AGNDSNS pin.
BP3	27	S	Output of the 3.3-V on-board regulator. This regulator powers the controller and should be bypassed with a minimum of 100-nF capacitor to AGND.
BP6	28	S	Output of the 6-V on-board regulator. This regulator powers the driver stage of the controller and should be bypassed with a 4.7-µF ceramic capacitor PGND.

(1) I = Input, O = Output, P = Supply, G = Ground

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BOOT	7	S	Bootstrap pin for the internal flying high-side driver. Connect a typical 100-nF capacitor from this pin to the SW pins.
BPEXT	30	I	External BP voltage for BP crossover function. Bypass with a 4.7-µF ceramic capacitor to PGND if used.. Connect to GND if not used.
CLK	5	I	PMBus CLK pin. See PMBus specification.
CNTL	1	I	PMBus CNTL pin. See PMBus specification.
COMP	35	O	Output of the error amplifier. This regulates the D-CAP and D-CAP2 valley voltage reference for output regulation and should be bypassed with a 10-nF capacitor to AGND.
DATA	4	I/O	PMBus DATA pin. See PMBus specification.
DIFFO	33	O	Output of the differential sense amplifier.
FB	34	I	Feedback pin for the control loop. Regulates to a nominal 600 mV if there is no trim applied to the device using VREF_TRIM.
GND	14	G	Power stage ground return.
	15		
	16		
	17		
	18		
	19		
	20		
PGND	26	G	Power ground return for controller device. Connect to GND at the thermal tab with a minimum 8 mil wide PCB trace
PGOOD	36	O	Power good output. Open drain output that floats up when the device is operating and in regulation. Any fault condition causes this pin to pull low.
RT	40	O	Frequency-setting resistor. Connect a resistor from this pin to AGND to program the switching frequency.
$\overline{\text{SMBALERT}}$	6	O	SMBus alert pin. See SMBus specification.
SW	8	O	Switched power output of the device. Connect the output averaging filter and bootstrap capacitor to this group of pins.
	9		
	10		
	11		
	12		
MODE	39	I	D-CAP and D-CAP2 control mode selection pin. Connect to BP3 for D-CAP2 mode control. Connect to AGND for D-CAP mode control.
TSNS	37	O	External temperature sense signal input. TSNS can be connected to AGND to disable external temperature measurement.
VDD	29	I	Input Voltage for analog control circuitry. Bypass with a minimum 1.0-µF capacitor to AGND. The VDD voltage is also used for input feed-forward, ON-time generation and High Side Over Current (HSOC). VIN and VDD must be at the same voltage for accurate short circuit protection.
VIN	21	I	Input power to the power stage. Bypass High-Frequency bypassing with multiple ceramic capacitors to GND is critical. See Layout Recommendations
	22		
	23		
	24		
	25		
VOUTS+	31	I	Output voltage sensing, positive side. This sensing provides remote sensing for PMBus reporting and the voltage control loop. Connect to V_{OUT} at desried regulation point through > 100-Ω resistor. Route with GND to VOUT- using coupled differential pair PCB routing.
VOUTS–	32	I	Output voltage sensing, negative or common side. This sensing provides remote sensing for PMBus reporting and the voltage control loop. Connect to Ground at desried regulation point through > 100-Ω resistor. Route with V_{OUT} to VOUT+ using coupled differential pair PCB routing.
Thermal tab			Package thermal tab. Connect to GND. The thermal tab must have adequate solder coverage for proper operation.

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN, VDD	–0.3	20	V
	BOOT	–0.3	37	
	BOOT – SW (BOOT to SW differential)	–0.3	7	
	CLK, DATA	–0.3	3.6	
	FB, SYNC, CNTL, VOUTS–, VOUTS+, BPEXT	–0.3	7	
Output voltage range	BP6	–0.3	7	V
	SW	–1	30	
	SW (> 50 ns, > 10 µJ)	-5	30	
	COMP, DIFFO, $\overline{\text{SMBALERT}}$, PGOOD	–0.3	7	
	ADDR0, ADDR1, BP3, RT, TSNS	–0.3	3.6	
T_J operating junction temperature range		–40	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) If Military or Aerospace specified devices are required, contact the Texas Instruments Sales/Office/Distributors for availability and specifications.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Controller input voltage	4.5		18	V
V_{IN}	Power stage input voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS544B20 TPS544C20	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	27.5	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance(3)	13.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.0	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.3	
ψ_{JB}	Junction-to-board characterization parameter(5)	3.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance(6)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = V_{VDD}= 12 V, R_{RT} = 38.3 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		18	V
V_{VIN}	Power stage voltage range		4.5		18	V
I_{VDD}	Input Operating Current	Not switching			10	mA
UVLO						
$V_{IN(on)}$	Input turn on voltage	Default settings	4.05	4.25	4.45	V
$V_{IN(off)}$	Input turn off voltage	Default settings	3.8	4	4.2	V
$V_{INON(rng)}$	Programmable range for turn-on voltage		4.25		16	V
$V_{INOFF(rng)}$	Programmable range for turn-off voltage		4		15.75	V
ERROR AMPLIFIER AND FEEDBACK VOLTAGE						
V_{FB}	Feedback Voltage	0°C ≤ T_J ≤ 70°C	597	600	603	mV
		–40°C ≤ T_J ≤ 125°C	594	600	606	
g_M	Transconductance			130		µS
I_{FB}	FB pin bias current (out of pin)	V_{FB} = 0.6 V			50	nA
V_{LOOP_COMP}	Loop comparator offset voltage	V_{FB} = 0.6 V, T_J = 25°C	-7.5		7.5	mV
BP6 REGULATOR						
V_{BP6}	Output voltage	I_{BP6} = 10 mA	6.2	6.5	6.8	V
$V_{BP6(do)}$	Dropout voltage	V_{VIN} – V_{BP6}, V_{VDD} = 4.5 V, I_{BP6} = 25 mA			100	mV
I_{BP6}	Output current(1)	V_{VDD} = 12 V	120			mA
V_{BP6UV}	Regulator UVLO voltage(1)		3.3	3.55	3.8	V
$V_{BP6UV(hyst)}$	Regulator UVLO voltage hysteresis(1)		230	255	270	mV
BPEXT						
$V_{BPEXT(swover)}$	BPEXT switch-over voltage	VDD > $V_{IN(on)}$	4.5	4.65		V
$V_{hys(swover)}$	BPEXT switch-over hysteresis		100		200	mV
$V_{BPEXT(do)}$	BPEXT dropout voltage	V_{BPEXT} -V_{BP6}, V_{BPEXT} = 4.8 V, I_{BP6} = 25 mA			100	mV
BOOTSTRAP						
$V_{BOOT(drop)}$	Bootstrap voltage drop	I_{BOOT} = 5 mA			150	mV
BP3 REGULATOR						
V_{BP3}	Output voltage	V_{VDD} = 4.5 V, I_{BP3} ≤ 5 mA	3.1	3.3	3.5	V
SOFT START						
t_{SS}	Soft-start time(2)	Factory default settings		2.7		ms
	Programmable range(1)		0.6		9	ms
	Accuracy over range(1)			±10%		
$t_{ON(DELAY)}$	Turn-on delay	Factory default settings		0		ms
$t_{OFF(DELAY)}$	Turn-off delay	Factory default settings		0		ms

(1) Specified by design. Not production tested.
(2) Soft-start time is defined by the rise time of the internal reference, V_{REF}

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = V_{VDD}= 12 V, R_{RT} = 38.3 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REMOTE SENSE AMPLIFIER							
$V_{DIFFO(ERROR)}$	Error voltage from DIFFO to V_{SNS}	(V_{OUTS+} – $V_{OUTS–}$) = 0.6 V		-5		5	mV
		(V_{OUTS+} – $V_{OUTS–}$) = 1.2 V		-8		8	
		(V_{OUTS+} – $V_{OUTS–}$) = 3.0 V		-17		17	
BW	Closed-loop bandwidth(3)			2			MHz
R_{VOUTx}	Output voltage sense input impedance	V_{OUT+} = 1.2V		55	80	105	kΩ
$V_{DIFFO(max)}$	Maximum DIFFO output voltage			V_{BP6}-0.2			V
I_{DIFFO}	DIFFO sourcing current			1			mA
	DIFFO sinking current			1			
POWER STAGE							
R_{HS}	High-side on-resistance	V_{VDD} = 4.5 V, T_J = 25°C			4.9		mΩ
		V_{VDD} ≥ 12 V, T_J = 25°C			4.5		
$I_{HS(leak)}$	High-side leakage current	V_{VDD} = 18 V, T_J = 25°C			0.4	0.7	µA
		V_{VDD} = 18 V, T_J = 125°C(3)			1.5		
R_{LS}	Low-side on-resistance	V_{VDD} = 4.5 V, T_J = 25°C			2.2		mΩ
		V_{VDD} ≥ 12 V, T_J = 25°C			2.0		
CURRENT LIMIT							
$t_{OFF(OC)}$	Off time between restart attempts	Hiccup mode			7 × t_{SS}		ms
$I_{OC(flt)}$	Output current overcurrent fault threshold	Factory default settings	TPS544B20		26		A
		Programmable range		5		30	
		Factory default settings	TPS544C20		39		
		Programmable range		5		45	
$I_{OC(warn)}$	Output current overcurrent warning threshold	Factory default settings	TPS544B20		20		A
		Programmable range		4		29.5	
		Factory default settings	TPS544C20		30		
		Programmable range		4		44.5	
$I_{OC(acc)}$	Output current overcurrent fault and warning accuracy	I_{OCF} = 20 A(3)			±3		A
$t_{LSOC(min)}$	Minimum LDRV pulse width for valid current sensing(3)				400	500	ns
HIGH-SIDE SHORT CIRCUIT PROTECTION							
I_{HSOC}	High-side short-circuit protection fault threshold	T_J = 25°C	TPS544B20	30		58	A
			TPS544C20	45		75	
POWER GOOD (PGOOD)							
V_{FBPGH}	FB PGOOD high threshold	Factory default settings			675		mV
V_{FBPGL}	FB PGOOD low threshold	Factory default settings			525		mV
$V_{PG(acc)}$	PGOOD accuracy over range	Factory default settings		–5%		5%	
$V_{pg(hyst)}$	FB PGOOD hysteresis voltage			10		50	mV
R_{PGOOD}	PGOOD pull-down resistance	V_{FB} = 0, I_{PGOOD} = 5 mA			30	70	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	Factory default settings, V_{PGOOD} = 5 V				20	µA
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION							
V_{FBOV}	FB pin over voltage threshold	Factory default settings			700		mV
V_{FBUV}	FB pin under voltage threshold	Factory default settings			499		mV
$V_{UVOV(acc)}$	FB UV, OV accuracy over range	Factory default settings		–4.5%		4.5%	

(3) Specified by design. Not production tested.

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = V_{VDD}= 12 V, R_{RT} = 38.3 kΩ; zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE TRIMMING AND MARGINING						
$V_{FBTM(step)}$	Resolution of FB steps with trim and margin			2		mV
$t_{FBTM(step)}$	Transition time per trim or margin step	After soft-start time		30		µs
$V_{FBTM(max)}$	Maximum FB voltage with trim or margin only			660		mV
$V_{FBTM(min)}$	Minimum FB voltage with trim or margin only			480		mV
$V_{FBTM(rng)}$	FB voltage range with trim and margin combined		420		660	mV
V_{FBMH}	Margin high FB pin voltage	Factory default settings		660		mV
V_{FBML}	Margin low FB pin voltage	Factory default settings		540		mV
TEMPERATURE SENSE AND THERMAL SHUTDOWN						
T_{SD}	Junction shutdown temperature(4)		135	145	155	°C
T_{HYST}	Thermal shutdown hysteresis(4)		20	25	30	°C
$I_{TSNS(ratio)}$	Ratio of bias current flowing out of TSNS pin, state 2 to state 1		9.7	10.0	10.3	µA/µA
I_{TSNS}	State 1 current out of TSNS pin			10		µA
I_{TSNS}	State 2 current out of TSNS pin			100		µA
V_{TSNS}	Voltage range on TSNS pin(4)		0		1.00	V
$T_{OT(flt)}$	Overtemperature fault limit(4)	Factory default settings		150		°C
	OT fault limit range(4)		120		165	
$T_{OT(warn)}$	Overtemperature warning limit(4)	Factory default settings		125		°C
	OT warning limit range(4)		100		140	
$T_{OT(step)}$	OT fault, warning step(4)			5		°C
$T_{OT(hys)}$	OT fault, warning hysteresis(4)		15	20	25	°C
MEASUREMENT SYSTEM						
$M_{VOUT(rng)}$	Output voltage measurement range		0.5		5.8	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy		–2.0%		2.0%	
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution			1.95		mV
$M_{IOUT(acc)}$	Output current measurement accuracy(5)	I_{OUT} ≥ 20 A, -40 ≤ T_A ≤ 85°C	-15%		+15%	
		3 A ≤ I_{OUT} < 20 A, –40 ≤ T_A ≤ 85°C	-3		+3	A
$M_{IOUT(lsb)}$	Output current measurement bit resolution(4)			62.5		mA
$M_{TSNS(rng)}$	External temperature sense range(4)		-40		165	°C
$M_{TSNS(acc)}$	External temperature sense accuracy(4)	-40°C ≤ $T_{J(sensor)}$ ≤ 165°C	-8		8	°C
$M_{TSNS(lsb)}$	External temperature sense bit resolution(4)			1.238		°C
PMBus INTERFACE ADDRESSING						
I_{ADD}	Address pin bias current		8.23	9.75	11.21	µA
$V_{ADD(rng)}$	Address pin legal address voltage range		0.08		2.35	V

(4) Specified by design. Not production tested.
(5) Current sense amplifier gain and offset are production tested. Output current monitoring guaranteed by correlation.

7.6 Switching Characteristics

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 38.3 kΩ (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TON GENERATOR AND SW TIMING						
f_{SW}	Switching frequency(1)	Adjustment range	250		1000	kHz
		R_{RT} = 10.0 kΩ	210	250	290	
		R_{RT} = 17.8 kΩ	250	300	350	
		R_{RT} = 27.4 kΩ	340	400	460	
		R_{RT} = 38.3 kΩ	425	500	575	
		R_{RT} = 56.2 kΩ	550	650	750	
		R_{RT} = 86.6 kΩ	640	750	860	
		R_{RT} = 133 kΩ	720	850	980	
		R_{RT} = 205 kΩ	850	1000	1150	
I_{RT}	RT output current			9.75		µA
$t_{OFF(min)}$	Minimum off-time(2) (3)			175		ns
$t_{ON(min)}$	Minimum controllable pulse width(2)				80	ns
V_{DCAP2}	D-CAP2 mode threshold				2.10	V
V_{DCAP}	D-CAP mode threshold		0.8			V
I_{MODE}	MODE output current		7		13	µA
t_{DEAD}	Power stage driver dead-time(2)	SW rising		15		ns
		SW falling		15		
$t_{SLEW(SW)}$	SW slew rate(2)	SW rising (10% to 90%), I_{OUT} = 30 A, R_{BOOT}= 0 Ω		9.2		V/ns
		SW falling (90% to 10%), I_{OUT} = 30 A, R_{BOOT}= 0 Ω		6.2		

(1) On-times are production tested, but steady-state switching frequency is not.
(2) Specified by design. Not production tested.
(3) Minimum off time for valid current sensing is 400-ns typical, 500-ns maximum.

7.7 Typical Characteristics

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 38.3 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.

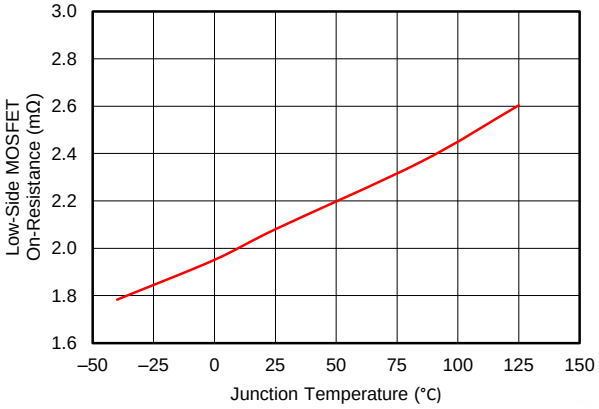


Figure 1. Low-Side MOSFET On-Resistance ($R_{DS(on)}$) vs. Junction Temperature

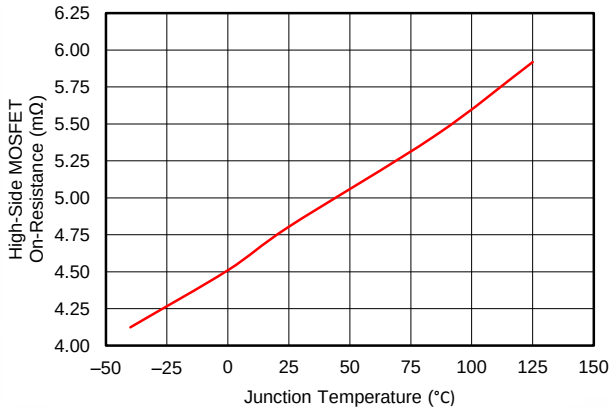


Figure 2. High-Side MOSFET On-Resistance ($R_{DS(on)}$) vs. Junction Temperature

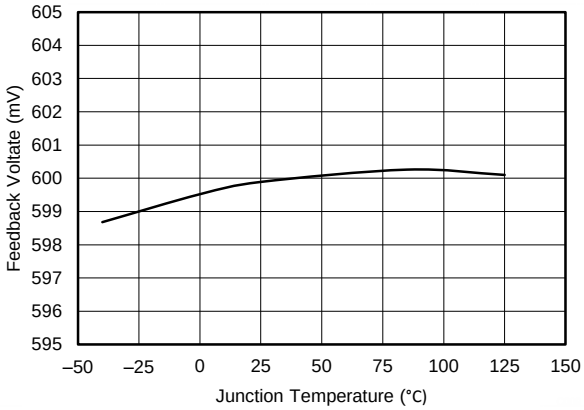


Figure 3. Feedback Voltage vs. Junction Temperature

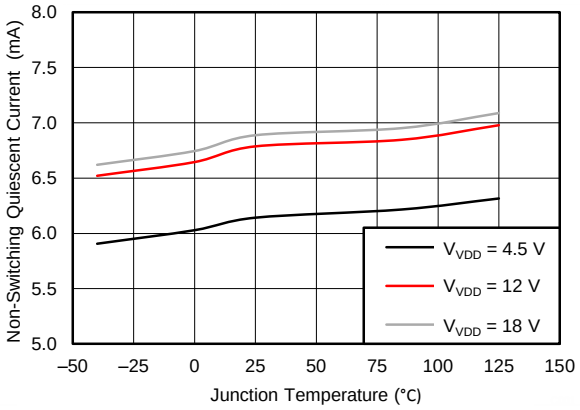
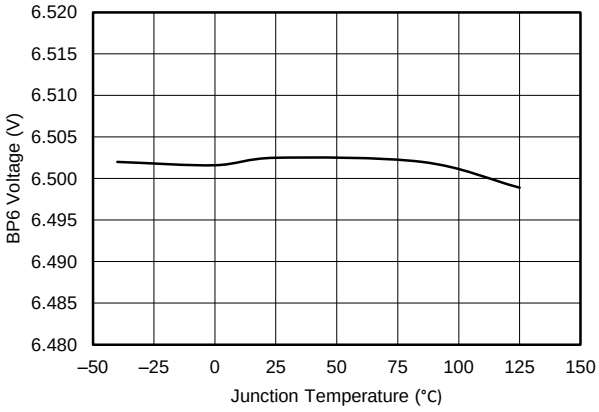
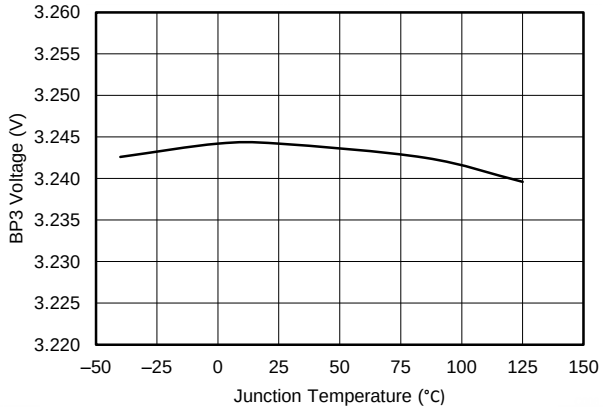


Figure 4. Non-Switching Input Current (I_{VDD}) vs. Junction Temperature



I_{BP6} = 25 mA

Figure 5. BP6 Voltage vs. Junction Temperature



I_{BP3} = 5 mA

Figure 6. BP3 Voltage vs. Junction Temperature

Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 38.3 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.

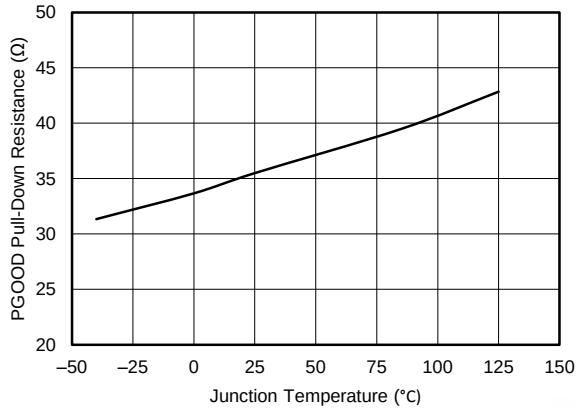
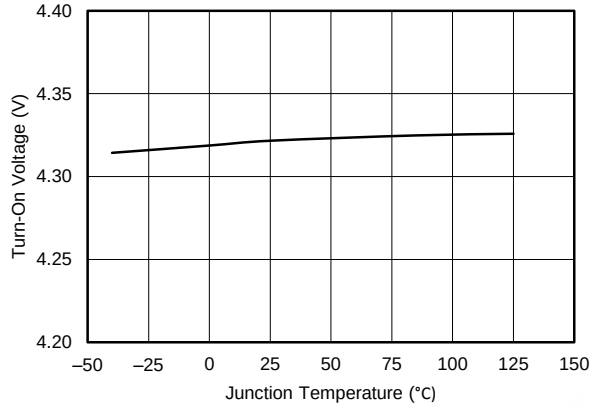
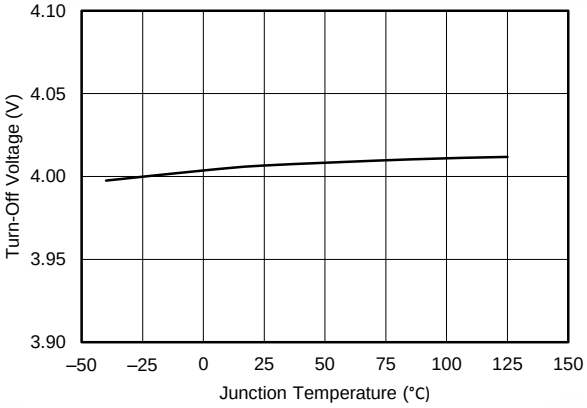


Figure 7. PGOOD Pull-Down Resistance vs. Junction Temperature



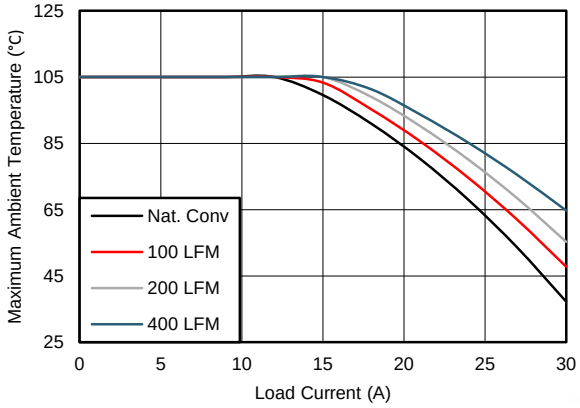
VIN_ON = 4.25 V

Figure 8. Turn-On Voltage vs. Junction Temperature



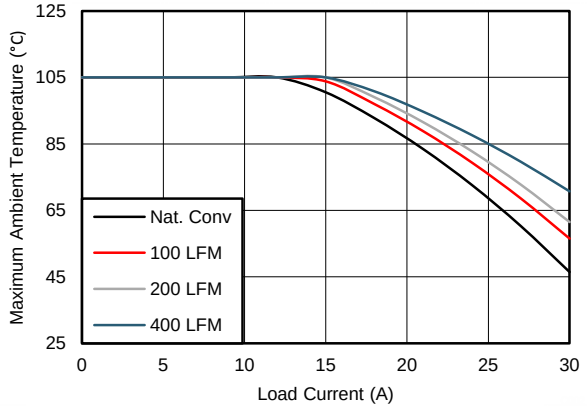
VIN_OFF = 4.00 V

Figure 9. Turn-Off Voltage vs. Junction Temperature



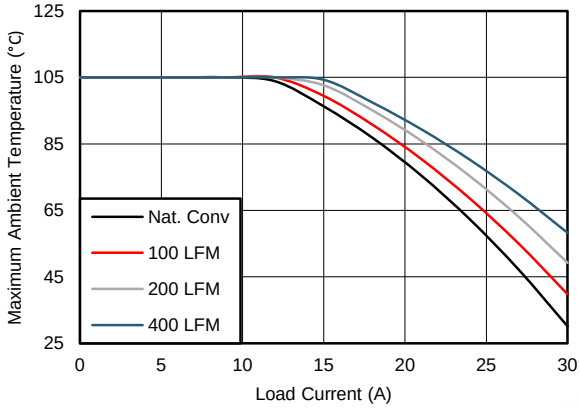
V_{IN} = 12 V V_{OUT} = 0.9 V f_{SW} = 650 kHz

Figure 10. Safe Operating Area



V_{IN} = 12 V V_{OUT} = 0.9 V f_{SW} = 300 kHz

Figure 11. Safe Operating Area

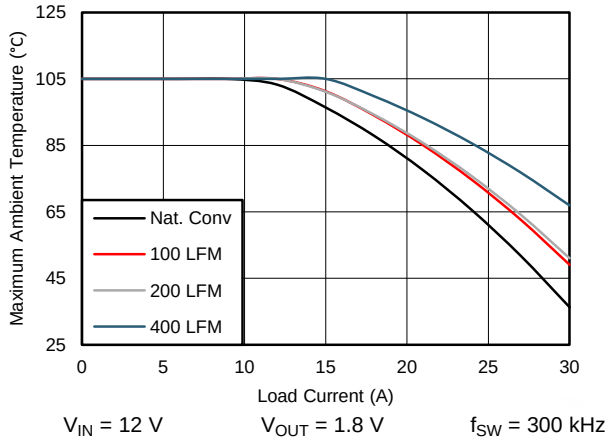


V_{IN} = 12 V V_{OUT} =1.8 V f_{SW} = 650 kHz

Figure 12. Safe Operating Area

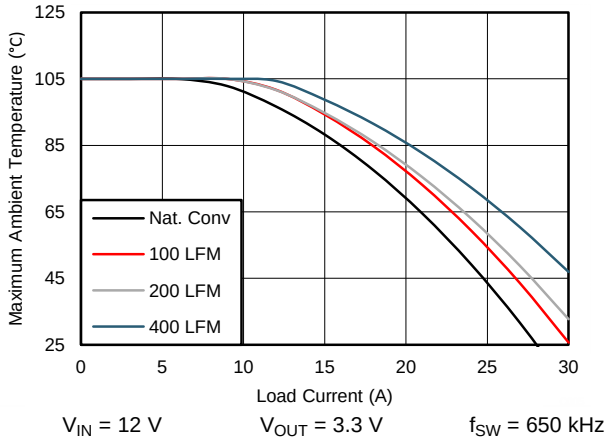
Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 38.3 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.



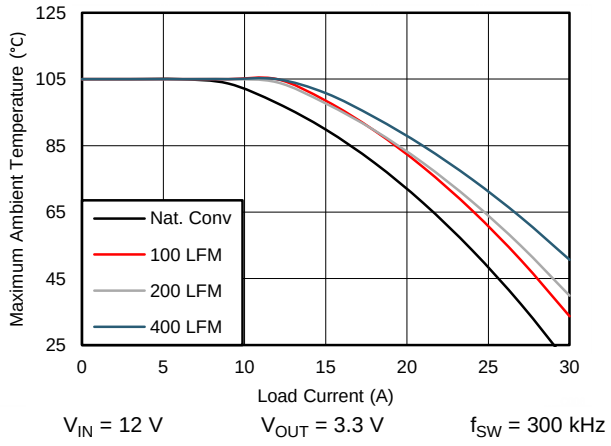
V_{IN} = 12 V V_{OUT} = 1.8 V f_{SW} = 300 kHz

Figure 13. Safe Operating Area



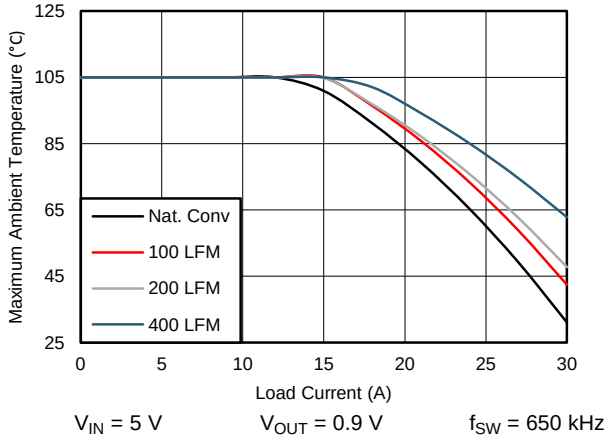
V_{IN} = 12 V V_{OUT} = 3.3 V f_{SW} = 650 kHz

Figure 14. Safe Operating Area



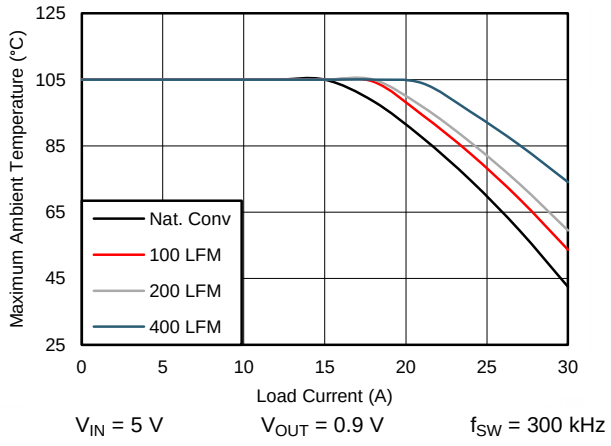
V_{IN} = 12 V V_{OUT} = 3.3 V f_{SW} = 300 kHz

Figure 15. Safe Operating Area



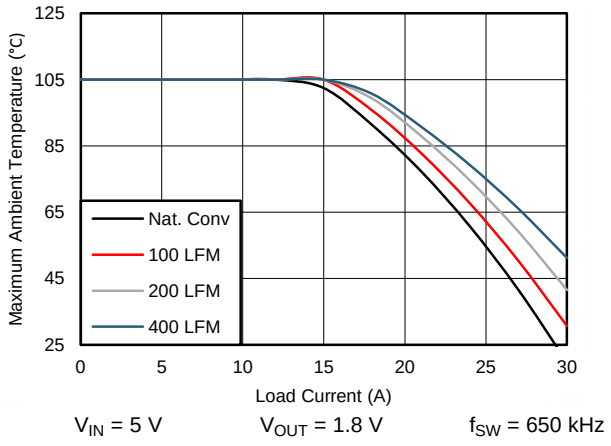
V_{IN} = 5 V V_{OUT} = 0.9 V f_{SW} = 650 kHz

Figure 16. Safe Operating Area



V_{IN} = 5 V V_{OUT} = 0.9 V f_{SW} = 300 kHz

Figure 17. Safe Operating Area



V_{IN} = 5 V V_{OUT} = 1.8 V f_{SW} = 650 kHz

Figure 18. Safe Operating Area

Typical Characteristics (continued)

V_{IN} = V_{DD} = 12 V, T_A = 25 ºC, R_{RT} = 38.3 kΩ (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments Evaluation Module.

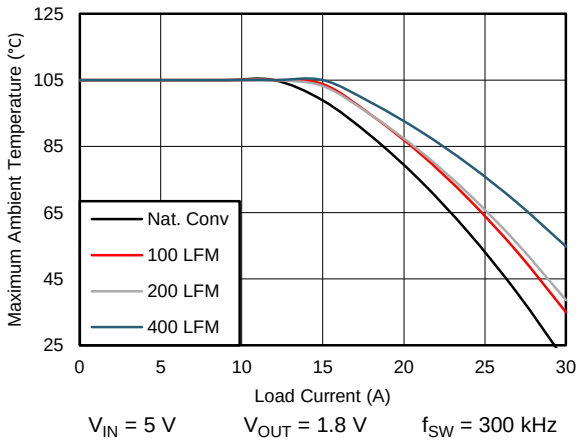


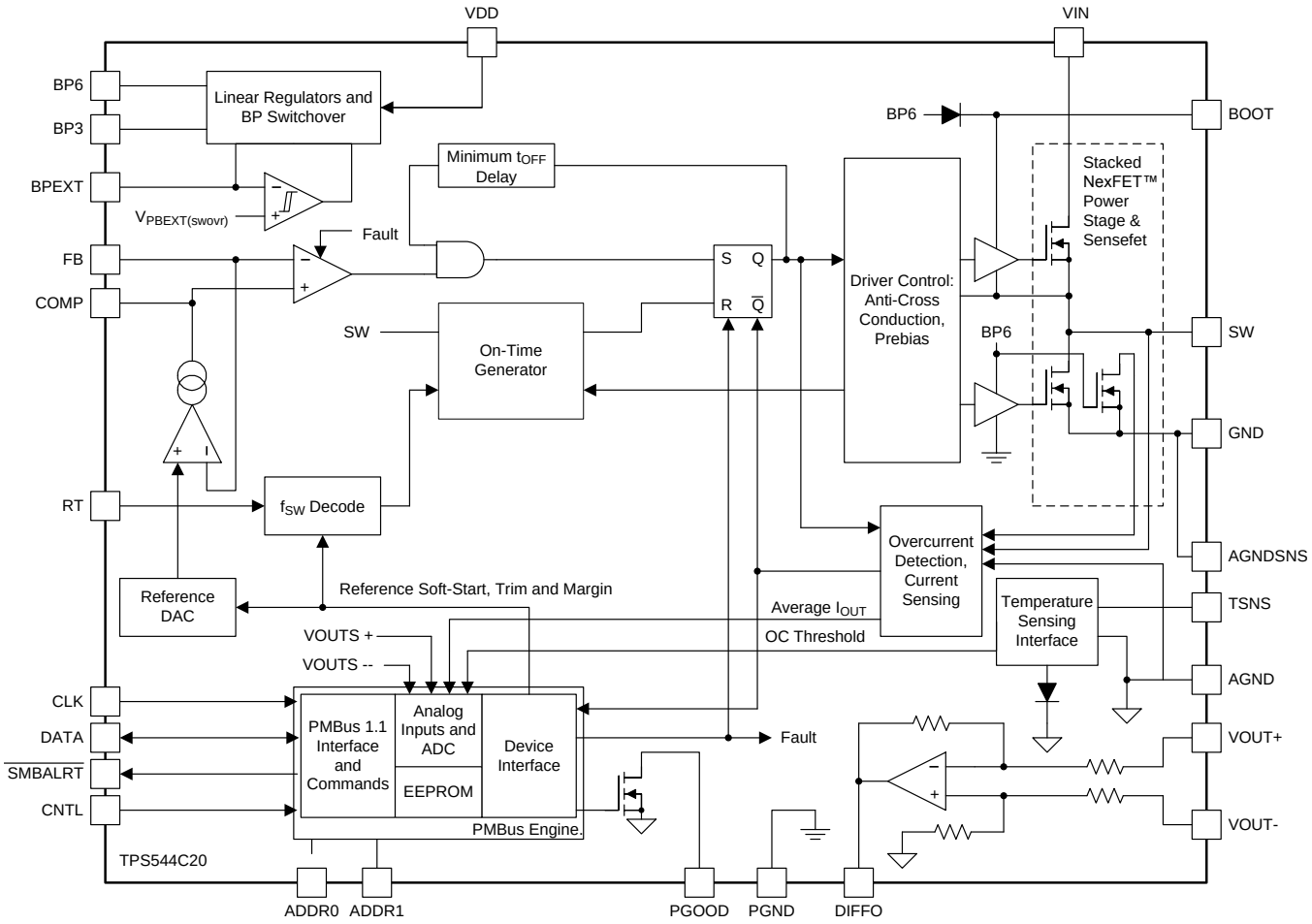
Figure 19. Safe Operating Area

8 Detailed Description

8.1 Overview

The TPS544B20 and TPS544C20 devices are 20-A, and 30-A, high-performance, synchronous buck converters with two integrated N-channel NexFET™ power MOSFETs. These devices implement TI's proprietary D-CAP and D-CAP2 mode control providing natural input voltage feed-forward and fast transient response with a precision error amplifier and low-offset differential remote sense amplifier for precise ouptut voltage regulation with minimal external compensation. Monotonic pre-bias capability eliminates concerns about damaging sensitive loads. Integrated PMBus capability provides current, voltage and on-board temperature monitoring, as well as many user-programmable configuration options as well as Adaptive Voltage Scaling (AVS) and output voltage margin testing.

8.2 Functional Block Diagram



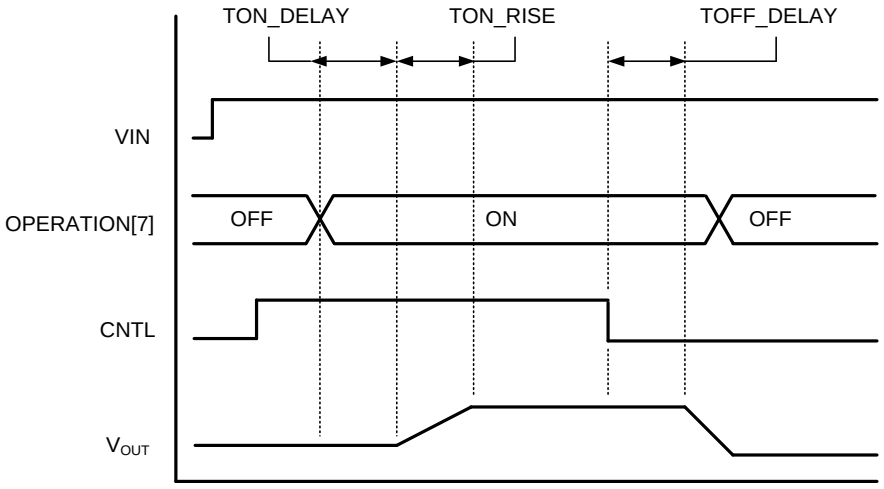
8.3 Feature Description

8.3.1 Turn-On and Turn-Off Delay and Sequencing

The TPS544C20 and TPS544B20 devices provide many sequencing options. Using the ON_OFF_CONFIG command, the device can be configured to start up when the input voltage is above the undervoltage lockout (UVLO) threshold, or to additionally require a signal on the CNTL pin and/or receive an update to the OPERATION command according to the PMBus protocol. When the gating signal as specified by ON_OFF_CONFIG command is asserted, a programmable turn-on delay can be set with the TON_DELAY command to delay the start of regulation. Similarly, a programmable turn-off delay can be set with the TOFF_DELAY command to delay the stop of regulation once the gating signal is de-asserted. Delay times are specified as an integer multiple of the soft-start time.

When the output voltage remains within the PGOOD window after the start-up period, PGOOD is released, and rises to an externally supplied logic level. The PGOOD signal can be connected to the CNTL pin of another device to provide additional controlled turn-on and turn-off sequencing.

Figure 20 shows control of the start-up and shutdown operations of the device, when the device is configured to respond to a logical AND of both CNTL and the OPERATION command. The device can also be configured to respond to only the CNTL signal, only the OPERATION command, or to convert power whenever VDD is greater than the VIN_ON command value setting.



(1) Bit 7 of OPERATION is used to control power conversion. Other bits in this register control output voltage margining.

Figure 20. Turn-On Controlled By Both Operation and Control

8.3.2 Pre-Biased Output Start-Up

The TPS544C20 and TPS544B20 devices prevent current from discharging from the output during start-up, when a pre-biased output condition exists. No SW pulses occur until the internal soft-start voltage rises above the error amplifier input voltage (FB pin), if the output is pre-biased. When the soft-start voltage exceeds the error amplifier input, and SW pulses start, the device limits synchronous rectification time after each SW pulse with a narrow on-time. The low-side MOSFET on-time slowly increases each switching cycle until it generates 128 pulses. After 128 pulses, the synchronous rectifier runs fully complementary to the high-side MOSFET. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to-regulation sequences are smooth and monotonic. These devices respond to a pre-biased output over-voltage condition immediately upon power-up, even during soft-start, while disabled or below the PMBus programmable undervoltage lockout on-time ($UVLO_{ON}$).

The combination of D-CAP and D-CAP2 mode control and the limited on-time of the low-side MOSFET during the pre-bias sequence allows these devices to operate at low switching frequencies for the first 128 switching cycles, after which the device operates using pseudo-constant frequency.

Feature Description (continued)

8.3.3 Voltage Reference

A 600-mV bandgap cell connects internally to the non-inverting input of the error amplifier. The 0.5% tolerance on the reference voltage allows for a power supply design that yields very high DC accuracy

8.3.4 Differential Remote Sense and Output Voltage Setting

The TPS544C20 and TPS544B20 devices implement a differential remote sense amplifier to provide excellent load regulation by cancelling IR-drop in high current applications. The VOUTS+ and VOUTS– pins should be kelvin-connected to the output capacitor bank directly at the load, and routed back to the device as a tightly coupled differential pair. Ensure that these traces are isolated from fast switching signals and high current paths on the final PCB layout to mitigate differential-mode noise. Optionally, use a small coupling capacitor (330-pF typical) between the VOUTS+ and VOUTS– pins to improve noise immunity. The output of the differential remote sense amplifier (DIFFO) sets the output voltage.

A voltage divider from the DIFFO pin to the FB pin sets the nominal output voltage. The output voltage must be divided down to the nominal reference voltage of 600 mV. The feedback voltage can be adjusted within –30% and +10% from the nominal 600 mV using PMBus commands, allowing the output voltage to vary by the same percentage. During the power-up sequence, the feedback reference is 600 mV plus any offset generated by the MARGIN command or VREF_TRIM command values which were previously stored in EEPROM. The initial output voltage equals the feedback voltage scaled by the divider ratio. See the *PMBus Output Voltage Adjustment* section for further details.

The device enables telemetry by digitizing the voltage at the DIFFO pin, averaging it to reduce measurement noise, and storing it in the READ_VOUT (8Bh) register.

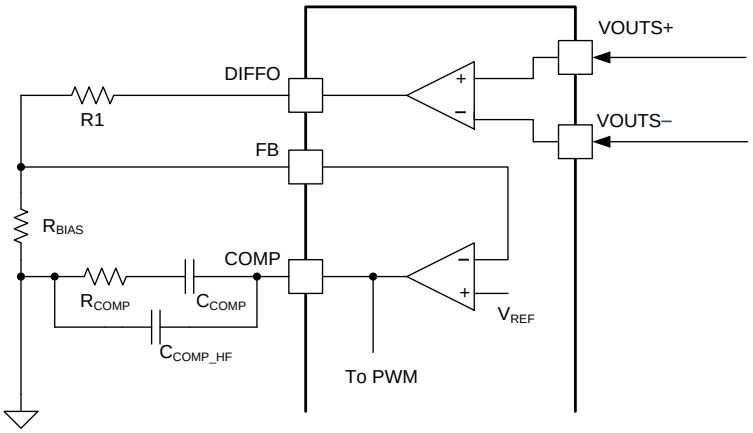


Figure 21. Output Voltage Setting

Equation 1 calculates the nominal output voltage. R1 can be arbitrarily selected to be 10-kΩ, with R_{BIAS} being scaled appropriately.

$$V_{OUT} = \left(1 + \frac{R1}{R_{Bias}}\right) \times V_{FB} \quad (1)$$

8.3.5 PMBus Output Voltage Adjustment

The nominal output voltage of the converter can be adjusted by changing the feedback voltage, V_{FB}, using the VREF_TRIM command. The adjustment range is between –20% and +10% from the nominal output voltage. This command adjusts the final output voltage of the converter to a high degree of accuracy, without relying on high-precision feedback resistors. The resolution of the adjustment is 7 bits, with a resulting minimum step size of approximately 2 mV, or 0.4%. The total output voltage adjustable range, including MARGIN and VREF_TRIM is –30% to + 10%.

Feature Description (continued)

The TPS544C20 and TPS544B20 devices allow simple output voltage margin testing, by applying a either a positive or negative offset to the feedback voltage. The STEP_VREF_MARGIN_HIGH and STEP_VREF_MARGIN_LOW commands control the size of the applied high or low offset respectively. The OPERATION command toggles the converter between three states:

- Margin none (no output margining). See Equation 2
- Margin high. See Equation 3
- Margin low. See Equation 4

$$V_{FB} = VREF\_TRIM + 0.6\ V \quad (2)$$

$$V_{FB} = VREF\_TRIM + STEP\_VREF\_MARGIN\_HIGH + 0.6\ V \quad (3)$$

$$V_{FB} = VREF\_TRIM + STEP\_VREF\_MARGIN\_LOW + 0.6\ V \quad (4)$$

Figure 22 shows an example of the VREF_TRIM and margin timing.

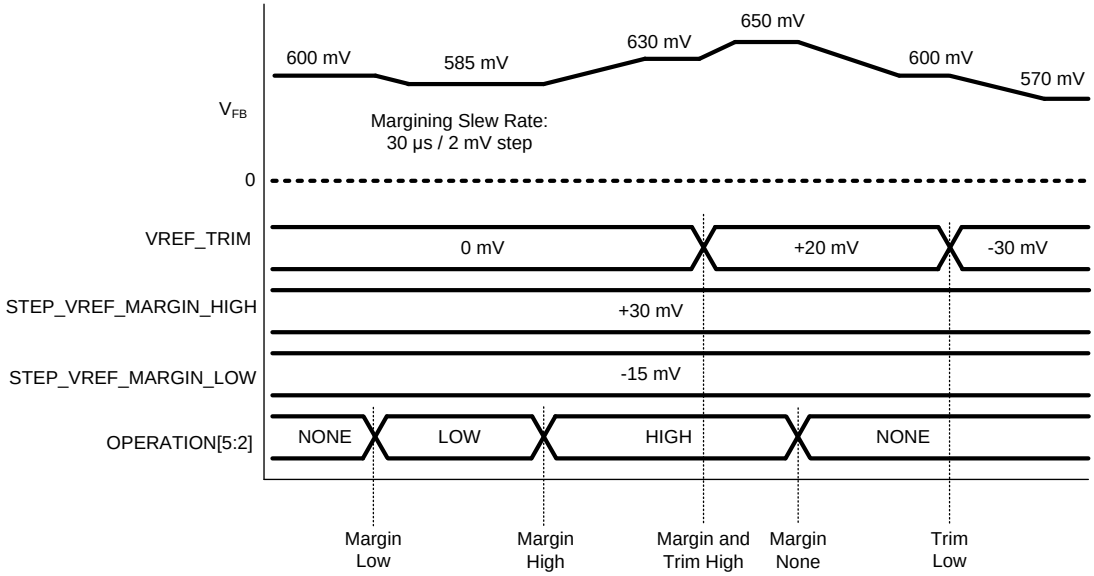


Figure 22. VREF_TRIM and Margin Example

The nominal 600-mV FB pin references the OV fault, UV fault, and PGOOD limits, as defined by PCT_VOUT_FAULT_PG_LIMIT command, regardless of VREF_TRIM or output margining. These limits remain fixed percentages of the nominal 600 mV reference, regardless of output margining.

8.3.6 Switching Frequency

A resistor from the RT pin to AGND establishes the switching frequency during the power-up sequence. To ensure proper detection, select a resistor with 1% tolerance from Table 1.

Table 1. Required RT Resistors

NOMINAL FREQUENCY (kHz)	1% RESISTOR VALUE (kΩ)
250	10.0
300	17.8
400	27.4
500	38.3
650	56.2
750	86.6

Table 1. Required RT Resistors (continued)

NOMINAL FREQUENCY (kHz)	1% RESISTOR VALUE (kΩ)
850	133
1000	205

The TPS544B20 and TPS544C20 devices detect values that are out-of-range on the RT pin. If the device detects that RT pin has an out-of-range resistance connected to it, the device selects a frequency setting of either 250 kHz (if the resistance is less than 5 kΩ) or 1 MHz (if the resistance is greater than 300 kΩ) . When the device has completed the Power-on-reset sequence, it latches the frequency in memory and deactivates the RT pin until the BP6 voltage falls below the BP6 undervoltage threshold setting. Once VDD is applied, the frequency latches in memory and RT pin deactives until BP6 falls below V_{BP6UV}

8.3.7 Soft-Start

To control the inrush current needed to charge the output capacitors during the start-up sequence, the TPS544C20 and TPS544B20 devices implement a soft-start time. When the device is enabled, the feedback reference voltage, V_{REF}, rises from 0 V to its final value (including output margining or VREF_TRIM value) at a slew rate defined by the TON_RISE command. The slew rate needed to increase the reference voltage from 0 V to 600 mV at each given rise time defines the specified rise times. During the soft-start period, the error amplifier operates as a unity-gain buffer to force the COMP pin voltage to track the internal reference and minimize the offset between the internal reference and the output voltage. Because D-CAP mode or D-CAP2 mode control regulates the valley voltage, the average output voltage can exceed the final regulation voltage several millivolts at the end of the soft-start period See Figure 23.

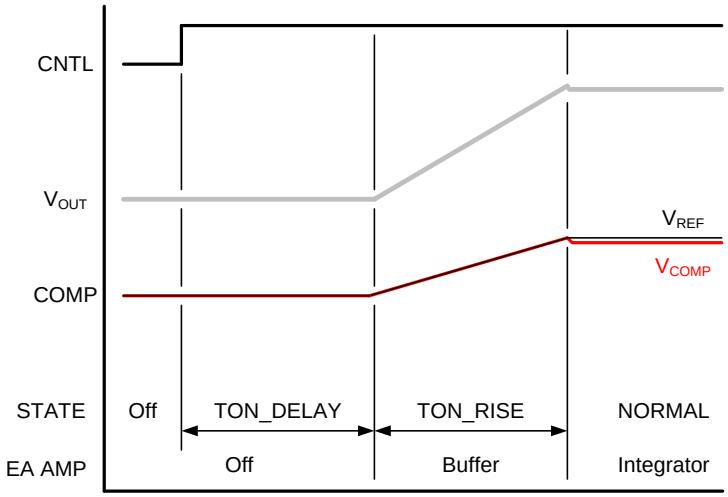


Figure 23. Soft-Start

8.3.8 Linear Regulators BP3 and BP6

Two on-board linear regulators provide suitable power for the internal circuitry of the devices. Externally bypass pins BP3 and BP6 for the converter to function properly. BP3 requires a minimum of 100 nF of capacitance connected to AGND. BP6 should be bypassed to PGND with a 4.7-µF capacitor.

These devices allow the use of an internal regulator to power other circuits. Ensure that external loads placed on the regulators do not adversely affect operation of the controller. Avoid loads with heavy transient currents that can affect the regulator outputs. Transient voltages on these outputs can result in noisy or erratic operation. Observe the current limits. Shorting the BP3 pin to GND can damage the BP3 regulator. The BP3 regulator input comes from the BP6 regulator output. The BP6 regulator can supply 120 mA of current and the total current drawn from both regulators must be less than 120 mA. This total current includes the device operating current (I_{VDD}) plus the gate-drive current required to drive the power MOSFETs.

8.3.9 External Bypass (BPEXT)

The BPEXT pin provides an external bypass of the internal BP6 regulator when the application includes an external bias supply between 4.5 V and 6.5 V. Using an external supply reduces the power dissipation in these devices and can slightly improve system efficiency. If the input voltage is less than the UVLO threshold, or if the voltage on the BPEXT pin is lower than the switch-over voltage, $V_{BPEXT(swover)}$, these devices use the internal BP6 regulator. If the voltage on the BPEXT pin exceeds this switch-over voltage, then these devices disable the internal BP6 regulator and BPEXT outputs to BP6, replacing the internal linear regulator, until the voltage on the BPEXT pin falls by the BPEXT switch-over hysteresis amount, $V_{HYS(swover)}$. If the application does not require the BPEXT function, connect the BPEXT pin to PGND.

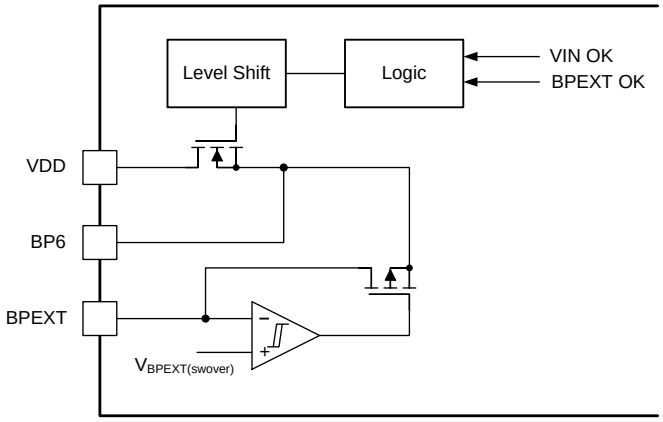


Figure 24. BP External

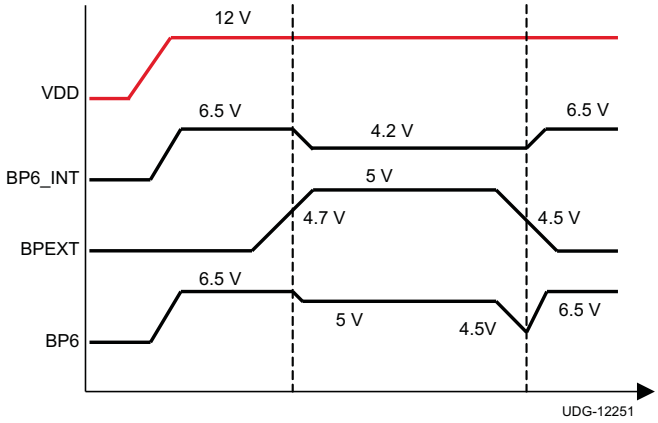


Figure 25. BP Crossover Diagram

NOTE

It is not recommended to transition BPEXT across the switch-over voltage, $V_{BPEXT(swover)}$, during regulation. The transition causes an overshoot or undershoot response on the output voltage. Instead, the BPEXT voltage should be either fully established to its final level, or pulled low to PGND prior to entering regulation.

8.3.10 Current Monitoring and Low-Side MOSFET Overcurrent Protection

The TPS544C20 and TPS544B20 devices sense average output current using an internal sensefet. A sensefet conducts a scaled-down version of the power-stage current. Sampling this current in the middle of the low-side drive signal determines the average output current. This architecture achieves excellent current monitoring and better overcurrent threshold accuracy than inductor DCR current sensing with minimal temperature variation and no dependence on power loss in a higher DCR inductor. This enables the use of lower DCR inductors to improve efficiency. Use the IOUT_CAL_OFFSET command to improve current sensing and overcurrent accuracy by removing board layout-related systematic errors post assembly. The devices continually digitize the sensed output current, and average it to reduce measurement noise. The devices then store the current value in the read-only READ_IOUT register, enabling output current telemetry.

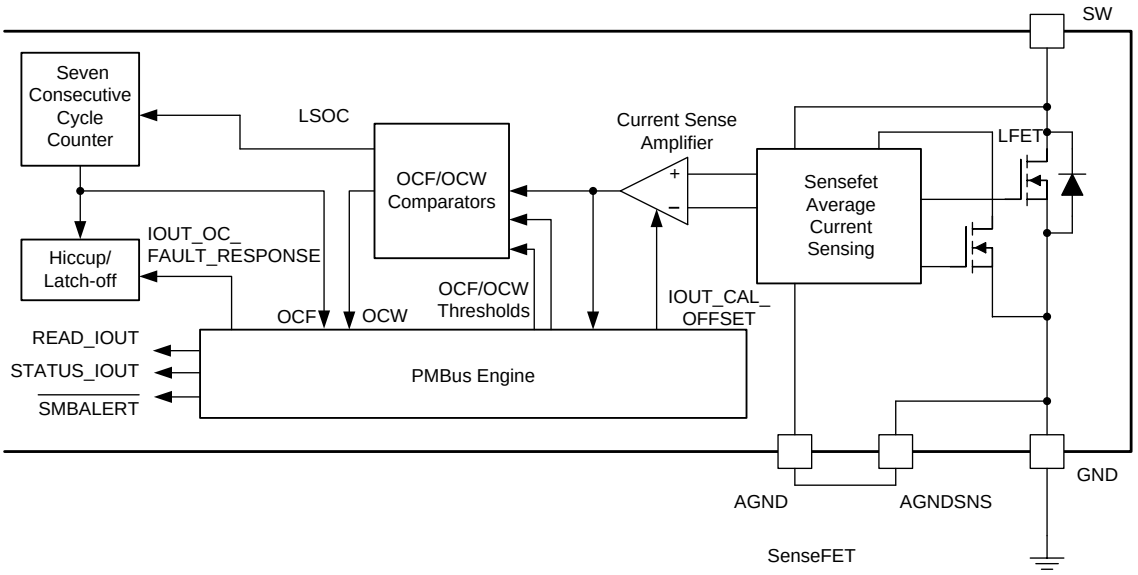


Figure 26. Sensefet Average Current Sensing and Low-Side Overcurrent Protection

The TPS544C20 and TPS544B20 devices also implement low-side MOSFET overcurrent protection with programmable fault and warning thresholds. The IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands set the low-side overcurrent thresholds.

As shown in Figure 26, if an overcurrent event is detected in a given switching cycle, the device increments an overcurrent counter. When the device detects seven consecutive low-side overcurrent events, the converter responds, flagging the appropriate status registers, triggering $\overline{\text{SMBALERT}}$ if it is not masked, and entering either continuous restart hiccup, or latch-off according to the IOUT_OC_FAULT_RESPONSE command. In continuous restart hiccup mode, the devices implement a time-out function that occurs after seven soft-start cycles; followed by a normal soft-start attempt. When the overcurrent fault clears, normal operation resumes, otherwise, the device detects overcurrent and the process repeats.

8.3.11 High-Side MOSFET Short-Circuit Protection

The TPS544B20 and devices also implement a fixed high-side MOSFET overcurrent (HSOC) protection to limit peak current, and prevent inductor saturation in the event of a short circuit. The devices detect an overcurrent event by sensing the voltage drop across the high-side MOSFET when it is on. If the peak current reaches the HSOC level on any given cycle, the cycle terminates to prevent the current from increasing any further. For accurate high-side MOSFET overcurrent protection, the VIN and VDD pins must be at the same voltage; split rail operation is not supported.

8.3.12 Over-Temperature Protection

An internal temperature sensor protects the devices from thermal runaway. The internal thermal shutdown threshold, T_{SD}, is fixed at 145°C typical. When the devices sense a temperature above T_{SD}, an over-temperature fault internal (OTFI) is flagged, and power conversion stops until the sensed junction temperature falls by the thermal shutdown hysteresis amount, T_{HYST}, (25°C typical). Additionally, the OTFI bit in STATUS_MFR_SPECIFIC setting indicates when the devices detect an internal over-temperature event.

The TPS544C20 and TPS544B20 devices also provide programmable external over-temperature fault and warning thresholds using measurements from an external temperature sensor connected on the TSNS pin. The temperature sensor circuit applies two bias currents to an external NPN transistor, and measures ΔV_{BE} to infer the junction temperature of the sensor. The TPS544C20 and TPS544B20 devices are designed to use a standard 2N3904 NPN transistor as a temperature sensor. Other sensors may be used, but the devices assume an ideality factor, *n*, of 1.008 for use with the 2N3904. The devices then digitize the result and compare it to the user-configured over-temperature fault and warning thresholds. When an external over-temperature fault (OTF) is

detected, power conversion stops until the sensed temperature falls by 20°C. The READ_TEMPERATURE_2 (8Eh) register is continually updated with the digitized temperature measurement, enabling temperature telemetry. The OT_FAULT_LIMIT (4Fh) and OT_WARN_LIMIT (51h) commands set the PMBus over-temperature fault and warning thresholds. When an overtemperature event is detected, the device sets the appropriate flags in STATUS_TEMPERATURE (7Dh) and triggers SMBALERT if it is not masked.

TI recommends routing a differential pair of AGND and TSNS from the TPS544B20 and TPS544C20 to the collector-base and emitter terminals of the 2N3904. Include a 330-pF capacitor between the TSNS and AGND pair traces to reduce temperature measurement noise and associated error. Implement the option to disable external temperature sensing by terminating TSNS to AGNS with a 0-Ω resistor. This termination forces the external temperature measurement to –40°C, and prevents external over-temperature faults tripping. The internal temperature sensor, and internal over-temperature fault remain enabled regardless of the TSNS pin termination.

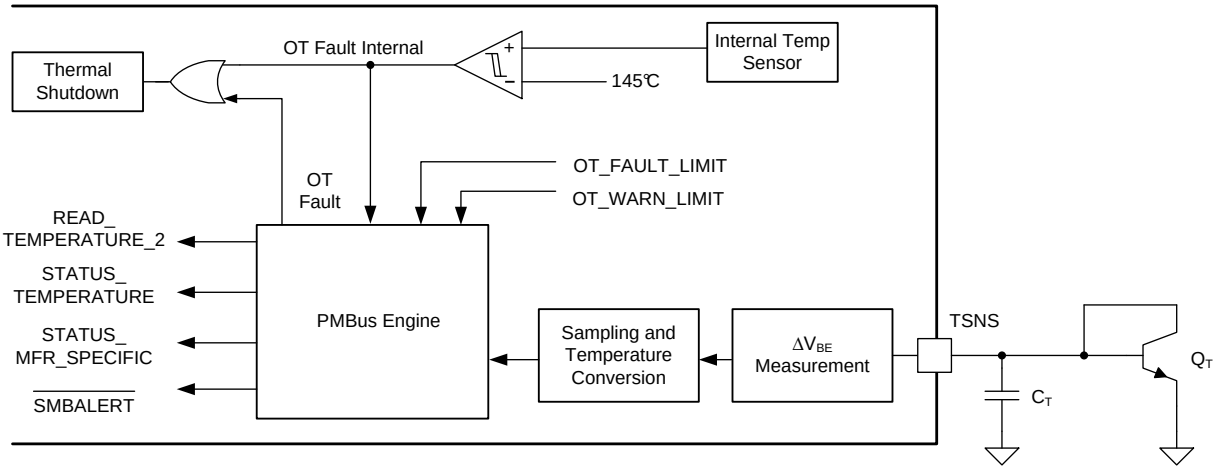


Figure 27. Over-Temperature Protection

8.3.13 Input Undervoltage Lockout (UVLO)

The TPS544C20 and TPS544B20 devices provide flexible user adjustment of the undervoltage lockout threshold and hysteresis. Two PMBus commands, VIN_ON (35h) and VIN_OFF (36h) allow the user to set these input voltage turn-on and turn-off thresholds independently, with a minimum of 4-V turn-off to a maximum 16-V turn-on. See the command descriptions for more details.

8.3.14 Output Overvoltage and Undervoltage Protection

The TPS544C20 and TPS544B20 devices include both output overvoltage protection (OVP) and output undervoltage (UVP) protection. The devices compare the FB pin voltage to internal selectable pre-set voltages, as defined by the PCT_VOUT_FAULT_PG_LIMIT (MFR_SPECIFIC_07) (D7h) command. As the output voltage rises or falls from the nominal voltage, the FB voltage tracks a direct divider ratio of the output voltage. If the FB voltage rises above the OVP threshold, the device terminates normal switching, declares an OV fault and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. If the FB voltage falls below the OVP threshold, the low-side FET turns off and normal switching resumes.

If the FB voltage falls below the undervoltage protection level after soft-start sequence has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, and awaits an external reset or begins a hiccup time-out delay prior to restart, depending on the value of the IOUT_OC_FAULT_RESPONSE (47h) command. The output undervoltage response is shared with the over-current fault response.

8.3.15 Fault Protection Responses

Table 2 summarizes the various fault protections and associated responses.

Table 2. Fault Protection Summary

FAULT	VDD UV	UV	OV	HSOC	LSOC	OT	TSD (OTFI)
FAULT CAUSES	1) Input undervoltage 2) Loss of input	1) Output overcurrent 2) Low-side short 3) FB short high	1) Pre-biased output 2) High-side short 3) FB short to GND	1) High-side short 2) Output short to GND	1) Low-side short 2) Output overcurrent	High board temperature	High device temperature due to ambient or power dissipation
MONITORING SIGNAL	Voltage on VDD pin	Voltage on FB pin	Voltage on FB pin	Voltage drop across high-side MOSFET	Sensed current in low-side MOSFET	Voltage on TSNS pin	Temperature on internal sensor
HIGH-SIDE MOSFET	Latch off	Latch off	Latch off	Turns off on cycle-by-cycle basis, incrementing OC counter; latch off when counter overflows	Tripping increments OC counter; latch off when counter overflows	Latch off	Latch off
LOW-SIDE MOSFET	Latch off	Latch off	Latch on until VOUT returns to within PG window	Latch off when counter overflows	Latch off when counter overflows	Latch off	Latch off
HICCUP	No	Yes(1)	No(2)	Yes(1)	Yes(1)	Hiccup after temperature below reset threshold	Hiccup after temperature below reset threshold
DURING SOFT-START	Enabled	Disabled	Enabled	Enabled	Enabled during or after SS once LDRV pulse width first exceeds CSA sampling period	Enabled	Enabled
AFTER SOFT-START	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

(1) If the device is configured to restart continuously, triggering the fault causes a hiccup.
(2) Hiccup is not triggered if the device can bring the output voltage back to regulation. Hiccup remains enabled if the output reaches the UV limit following an OV event

8.3.16 PMBus General Description

Timing and electrical characteristics of the PMBus specification can be found in the *PMB Power Management Protocol Specification, Part 1, revision 1.1* available at http://pmbus.org. The TPS544B20 and TPS544C20devices support both the 100-kHz and 400-kHz bus timing requirements. The TPS544B20 and TPS544C20 devices do not implement clock stretching when communicating with the master device.

Communication over the PMBus interface can support Packet Error Checking (PEC) if desired. If the PMbus host supplies clock (CLK pin) pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

These devices support a subset of the commands in the PMBus 1.1 Power Management Protocol Specification. See the *Supported PMBus Commands* section for more information.

The devices also support the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave device (such as the TPS544C20 device or the TPS544B20 device) can alert the master device that it is available for communication. The master device processes this event and simultaneously accesses all slave devices on the bus (that support the protocol) through the alert response address (ARA). Only the slave device that caused the alert acknowledges this request. The host device performs a modified receive byte operation to ascertain the slave devices address. At this point, the master device can use the PMBus status commands to query the slave device that caused the alert. By default, these devices implement the *auto alert response*, a manufacturer specific improvement to the SMBALERT response protocol, intended to mitigate the issue of *bus hogging*. See the *Auto ARA (Alert Response Address) Response* section for more information. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The devices contain non-volatile memory that stores configuration settings and scale factors. However, the devices do not save the settings programmed into this non-volatile memory. The STORE_USER_ALL (15h) command must be used to commit the current settings to non-volatile memory as device defaults. Settings available for storage in NVM are noted in their detailed descriptions.

8.3.17 PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The TPS544B20 and TPS544C20 devices each have 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high order digit and ADDR0 is the low-order digit. These address selection resistors must be 1% tolerance or better. Using resistors other than the recommended values can result in devices responding to adjacent addresses.

The E96 series resistors recommended for each digit value are shown in Table 3.

Table 3. Required Address Resistors

DIGIT	1% RESISTOR VALUE (kΩ)
0	10.0
1	17.8
2	27.4
3	38.3
4	56.2
5	86.6
6	133
7	205

The devices detect values that are out-of-range on the ADDR0 and ADDR1 pins. If the device detects that either pin has an out-of-range resistance connected to it, the device continues to respond to PMBus commands, but does so at address 127, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other devices are present on the bus or if another device could possibly occupy the 127 address.

The device reserves certain addresses in the I^2C address space for special functions. The PMBus protocol allows the address of the device to respond to these addresses. The user is responsible for knowing which of these reserved addresses are in use in a system and for setting the address of the device accordingly so as not to interfere with other system operations.

NOTE

These devices can be set to respond to the reserved GLOBAL CALL address or Address 0. Do not set a device to this address unless the design allows no other devices to respond to this address and that the overall bus is not affected by the presence of such an address.

8.3.18 PMBus Connections

The TPS544B20 and TPS544C20 devices support both the 100-kHz and 400-kHz bus speeds. Connection for the PMBus interface should follow the specification given in section *3.1.3 High-Power DC* in the SMBus specification V2.0 for the 400-kHz bus speed or the *3.1.2 Low Power DC* section. The complete SMBus specification is available from the SMBus web site, smbus.org.

8.3.19 Auto ARA (Alert Response Address) Response

By default, the TPS544B20 and TPS544C20 devices implement the *auto alert response*, a manufacturer specific improvement to the standard SMBALERT response protocol defined in the SMBus specification. The auto alert response is designed to prevent SMBALERT monopolizing in the case of a persistent fault condition on the bus. The user can choose to disable the auto ARA response, and use the standard SMBALERT response as defined in the SMBus specification, by using bit 8 of the MASK_SMBALERT (MFR_SPECIFIC_23) (E7h) command.

In the case of a fault condition, the slave device experiencing the fault pulls down the shared SMBALERT line, to alert the host that a fault condition has occurred. To establish which slave device has experienced the fault, the host issues a modified receive byte operation to the alert response address (ARA), to which only the slave device pulling down on SMBALERT should respond. The SMBus protocol provides a method for address arbitration in the case that multiple slave devices on the same bus are experiencing fault conditions. Once the host has established the address of the offending device, it must take any necessary action to release the SMBALERT line. For more information on the standard SMBus alert response protocol, see the System Management Bus (SMBus) specification.

In the case of a non-persistent fault (for example, a single-time event, such as an invalid command or data byte), the host can ascertain the address of the slave device experiencing a fault using the standard ARA response, and simply issue CLEAR_FAULTS (03h) to release the SMBALERT line, and resume normal operation. However, in the case of a persistent fault (i.e. one which remains active for some time, such as a short-circuit, or thermal shutdown), once the device issues a CLEAR_FAULTS (03h) command, the fault immediately re-triggers, and SMBALERT continues to be pulled low. In this case, the device holds low the SMBALERT line until the host masks the SMBALERT line using MASK_SMBALERT (MFR_SPECIFIC_23) (E7h) and then issues the CLEAR_FAULTS (03h) command. Because the SMBALERT line remains low, the host cannot be alerted to other fault conditions on the bus until it clears SMBALERT. This situation is known as *bus hogging*. Figure 28 and Figure 29 illustrate an example of this response.

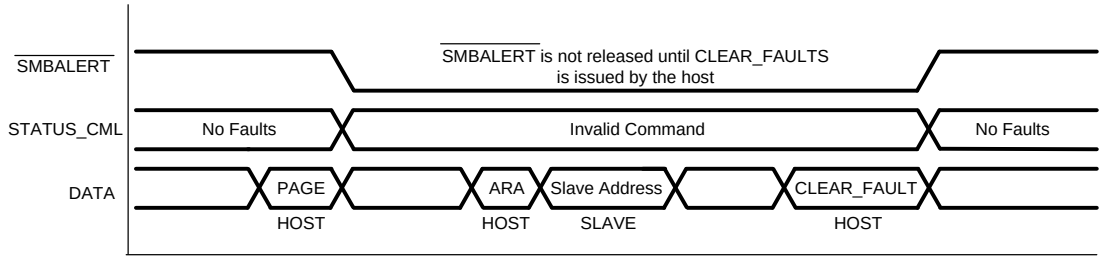


Figure 28. Example Standard ARA Response to Non-Persistent Fault

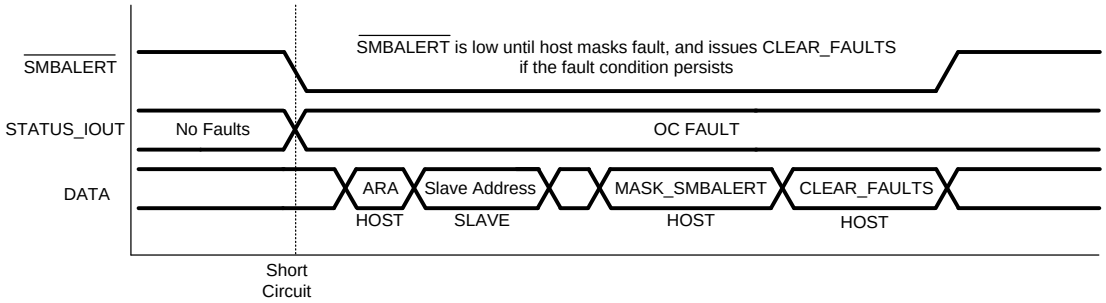


Figure 29. Example Standard ARA Response to a Persistent Fault

In order to mitigate the problem of *bus hogging*, these devices implement the Auto ARA response. When Auto ARA is enabled, the devices release SMBALERT automatically after successfully responding to access from the host at the alert response address. In this case, even when a device is experiencing a persistent fault, it does not hold the SMBALERT line low following successful notification of the host, and the host can be alerted to other faults on the bus in the normal manner. Examples of the auto ARA response are illustrated in Figure 30 and Figure 31.

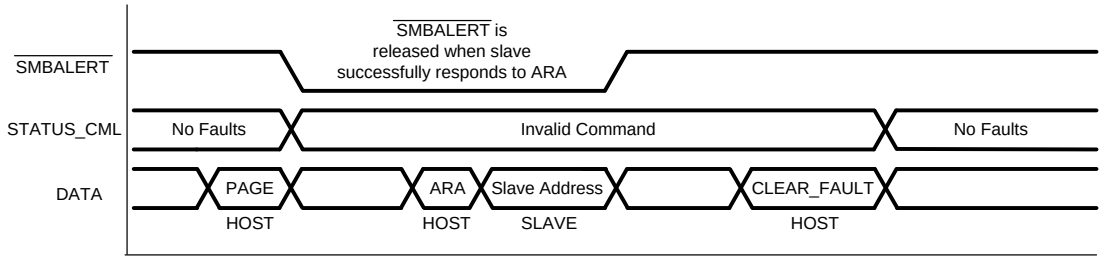


Figure 30. Example Auto ARA Response to Non-Persistent Fault

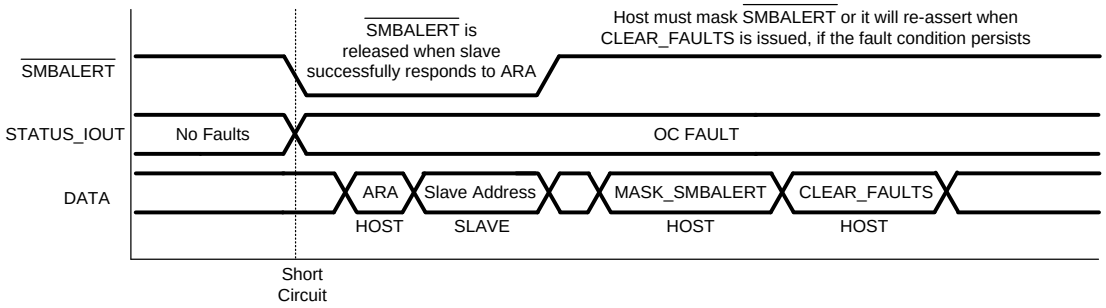


Figure 31. Example Auto ARA Response to Persistent Fault

8.4 Device Functional Modes

8.4.1 Continuous Conduction Mode

The TPS544B20 and TPS544C20 devices operate in continuous conduction mode (CCM) at a fixed frequency, regardless of the output current. For the first 128 switching cycles, the low-side MOSFET on-time is slowly increased to prevent excessive current sinking when the device starts up with a pre-biased output. Following the first clock 128 cycles, the low-side MOSFET and the high-side MOSFET on-times are fully complementary.

8.4.2 Operation with Internal BP6 Regulator

The TPS544B20 and TPS544C20 devices include an internal linear regulator to supply bias for internal logic and the power MOSFET drivers. The BP6 regulator steps down the VDD voltage to approximately 6.5 V when V_{VDD} is above 6.5 V, or operates with a maximum of 100-mV dropout when V_{VDD} is less than 6.5 V. In this case, the BPEXT pin should be connected to PGND.

8.4.3 Operation with BP External

The TPS544B20 and TPS544C20 devices can operate with an externally supplied voltage applied on the BPEXT pin to bypass the BP6 regulator, which powers the MOSFET drivers. Using BP External reduces the power dissipation inside the device, and leads to a small gain in overall efficiency. In this case, the BP6 regulator should be bypassed as normal, but the BPEXT pin should also have a minimum of 2.2-µF bypass capacitance relative to PGND. See External Bypass (BPEXT) for more information.

8.4.4 Operation with CNTL Signal Control

According to the value in the ON_OFF_CONFIG register, The TPS544B20 and TPS544C20 devices can be commanded to use the CNTL pin to enable or disable regulation, regardless of the state of the OPERATION command. The minimum input high threshold for the CNTL signal is 2.1 V, and the maximum input low threshold for the CNTL signal is 0.8 V. The CNTL pin can be configured as either active high or active low (inverted) logic.

8.4.5 Operation with OPERATION Control

According to the value in the ON_OFF_CONFIG register, these devices can be commanded to use the OPERATION command to enable or disable regulation, regardless of the state of the CNTL signal.

Device Functional Modes (continued)

8.4.6 Operation with CNTL and OPERATION Control

According to the value in the ON_OFF_CONFIG register, these devices can be commanded to require both a signal on the CNTL pin, and the OPERATION command to enable or disable regulation.

8.4.7 Operation with Output Margining

The OPERATION command can be used to toggle the device between three states:

- Margin none
- Margin low
- Margin high

In the margin none state, the feedback reference, V_{REF}, is equal to the nominal 600-mV reference, plus any offset defined by the VREF_TRIM command. In the margin low state, a negative offset defined by the STEP_VREF_MARGIN_LOW command is applied to the feedback reference, moving the converter output voltage down by an equivalent percentage. In the margin high state, a positive offset defined by the STEP_VREF_MARGIN_HIGH command is applied to the feedback reference, moving the converter output voltage up by an equivalent percentage. See the *PMBus Output Voltage Adjustment* section for more information.

8.5 Programming

8.5.1 Supported PMBus Commands

The commands listed in the Table 4 section are implemented as described to conform to the PMBus 1.1 specification. It also shows default behavior and register values.

Table 4. Supported PMBus Commands and Default Values

CMD CODE	PMBus 1.1 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
01h	OPERATION	Can be configured via ON_OFF_CONFIG to be used to turn the output on and off with or without input from the CTRL pin. Also used to turn on and off margin high and low.	Margin None. OPERATION is not used to enable regulation	00h
02h	ON_OFF_CONFIG	Configures the combination of CNTL pin input and OPERATION command for turning output on and off.	CNTL only. Active High	16h
03h	CLEAR_FAULTS	Clears all fault status registers to 0x00 and releases $\overline{\text{SMBALERT}}$.	Write-only	n/a
10h	WRITE_PROTECT	Used to control writing to the device.	Allow writes to all registers	00h
15h	STORE_USER_ALL	Stores all current storable register settings into EEPROM as new defaults.	Write-only	n/a
16h	RESTORE_USER_ALL	Restores all storable register settings from EEPROM.	Write-only	n/a
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.	Read only. PMBus v1.1, 400 kHz, PEC enabled	B0h
20h	VOUT_MODE	Read-only output mode indicator.	Linear, exponent = –9	17h
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.	4.25 V	F011h
36h	VIN_OFF	Sets value of input voltage at which the device should stop power conversion.	4.0V	F010h
39h	IOUT_CAL_OFFSET	Can be set to null out offsets in the current sensing circuit.	0.0000 A	E000h

Programming (continued)

Table 4. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.1 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
46h	IOUT_OC_FAULT_LIMIT	Sets the value of the output current that causes an overcurrent fault condition.	39 A (TPS544C20) 26 A (TPS544B20)	F84Eh (TPS544C20) F834h (TPS544B20)
47h	IOUT_OC_FAULT_RESPONSE	Sets response to output overcurrent and undervoltage faults to latch-off or hiccup mode.	Hiccup	3Fh
4Ah	IOUT_OC_WARN_LIMIT	Sets the value of the output current that causes an overcurrent warning condition.	30 A (TPS544C20) 20 A (TPS544B20)	F8C3h (TPS544C20) F828h (TPS544B20) F814h ()
4Fh	OT_FAULT_LIMIT	Sets the value of the sensed temperature that causes an overtemperature fault condition.	150 °C	0096h
51h	OT_WARN_LIMIT	Sets the value of the sensed temperature that causes an overtemperature warning condition.	125 °C	007Dh
61h	TON_RISE	Sets the time from when the output starts to rise until the voltage has entered the regulation band.	2.7 ms	E02Bh
78h	STATUS_BYTE	Returns one byte summarizing the most critical faults.	Read only	Current status
79h	STATUS_WORD	Returns two bytes summarizing fault and warning conditions.	Read only	Current status
7Ah	STATUS_VOUT	Returns one byte detailing if an output fault or warning has occurred	Read only	Current status
7Bh	STATUS_IOUT	Retyrns one byte detailing if an overcurrent fault or warning has occurred	Read only	Current status
7Dh	STATUS_TEMPERATURE	Returns one byte detailing if a sensed temperature fault or warning has occurred.	Read only	Current status
7Eh	STATUS_CML	Returns one byte containing PMBus serial communication faults.	Read only	Current status
80h	STATUS_MFR_SPECIFIC	Returns one byte detailing if internal overtemperature or address detection fault has occurred.	Read only	Current status
8Bh	READ_VOUT	Returns the output voltage in volts.	Read only	Current status
8Ch	READ_IOUT	Returns the channel current in amps.	Read only	Current status
8Eh	READ_TEMPERATURE_2	Returns the sensed temperature in degrees Celsius.	Read only	Current status
98h	PMBUS_REVISION	Returns PMBus revision to which the device is compliant.	Read only	11h
D0h	MFR_SPECIFIC_00	Two bytes dedicated as a user scratch pad.	00h	00h
D4h	VREF_TRIM (MFR_SPECIFIC_04)	Used to apply a fixed offset voltage to the reference voltage.	0.000 V	0000h
D5h	STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05)	Sets the increase to the value of the reference voltage for shifting the reference higher.	60 mV	001Eh
D6h	STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06)	Sets the decrease to the value of the reference voltage for shifting the reference lower.	–60 mV	FFE2h

Programming (continued)

Table 4. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.1 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE
D7h	PCT_VOUT_FAULT_PG_LIMIT (MFR_SPECIFIC_07)	Sets the PGOOD and output undervoltage and overvoltage limits as a percent of nominal.	UV Fault: –16.8% PGOOD (falling): –12.5% PGOOD (rising): 12.5% OV Fault: 16.8 %	00h
D8h	SEQUENCE_TON_TOFF_DELAY (MFR_SPECIFIC_08)	Sets the delays for turning the output on and off as a ratio of TON_RISE.	TON_DELAY: 0ms TOFF_DELAY: 0ms	00h
E5h	OPTIONS (MFR_SPECIFIC_21)	Sets miscellaneous user selectable options.	ADC is enabled. Telemetry is enabled.	0004h
E7h	MASK_SMBALERT (MFR_SPECIFIC_23)	Used to mask which faults or warnings assert SMBALERT, and enable Auto ARA.	Auto ARA is enabled. No SMBALERT sources are masked	0100h
FCh	DEVICE_CODE (MFR_SPECIFIC_44)	Returns a 12-bit unique identifier code for the device and a 4-bit revision code.	0153h (TPS544C20) 0143h (TPS544B20)	0153h (TPS544C20) 0143h (TPS544B20)

8.6 Register Maps

This family of devices supports the following commands from the PMBus 1.1 specification.

8.6.1 OPERATION (01h)

The OPERATION command turns the device output on or off in conjunction with input from the CNTL signal. It also sets the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CNTL pin instructs the device to change to another mode.

COMMAND	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r	r/w	r/w	r/w	r/w	r	r
Function	ON	X	Margin				X	X
Default Value	0	0	0	0	0	0	X	X

8.6.1.1 On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled if the input voltage is above undervoltage lockout, OPERATION is configured as a gating signal in ON_OFF_CONFIG, and no fault conditions exist.

8.6.1.2 Margin

If Margin Low is enabled, the feedback voltage is offset with the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, the feedback voltage is offset with the value from the STEP_VREF_MARGIN_HIGH command. (See *PMBus specification* for more information)

- 00XX: Margin Off
- 0101: Margin Low (Ignore on Fault)
- 0110: Margin Low (Act on Fault)
- 1001: Margin High (Ignore on Fault)
- 1010: Margin High (Act on Fault)

NOTE

Because the PGOOD, OV and UV thresholds remain referenced to the nominal 600-mV feedback reference, it is possible to use the Margin High, Margin Low or VREF_TRIM options to set the reference voltage into a PGOOD or Undervoltage Fault based on the ranges provided. When using the Ignore Fault option of the OPERATION command, these faults are masked when entering Margin High or Margin Low, but they PGOOD or Under Voltage Fault can be triggered when returning to Margin Off.

8.6.2 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CNTL pin input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

COMMAND	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	0

8.6.2.1 pu

The pu bit sets the default to either operate any time power is present or for power conversion to be controlled by CNTL pin and PMBus OPERATION command. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up.

BIT VALUE	ACTION
0	Device powers up any time power is present regardless of state of the CNTL pin.
1	Device does not power up until commanded by the CNTL pin and OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

8.6.2.2 cmd

The cmd bit controls how the device responds to the OPERATION command.

BIT VALUE	ACTION
0	Device ignores the “on” bit in the OPERATION command.
1	Device responds to the “on” bit in the OPERATION command.

8.6.2.3 cpr

The cpr bit sets the CNTL pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

BIT VALUE	ACTION
0	Device ignores the CNTL pin. Power conversion is controlled only by the OPERATION command.
1	Device requires the CNTL pin to be asserted to start the unit.

8.6.2.4 pol

The pol bit controls the polarity of the CNTL pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using the STORE_USER_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTL pin.

BIT VALUE	ACTION
0	CNTL pin is active low.
1	CNTL pin is active high.

8.6.2.5 cpa

The cpa bit sets the CNTL pin action when turning the controller off. This bit is read internally and cannot be modified by the user.

BIT VALUE	ACTION
0	Turn off the output using the programmed delay.

8.6.3 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT output if the device is asserting SMBALERT. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

8.6.4 WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. Write protection also prevents protected registers from being updated in the event of a RESTORE_USER_ALL. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

COMMAND	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

8.6.4.1 bit5

BIT VALUE	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG. (bit6 and bit7 must be 0 to be valid data)

8.6.4.2 bit6

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT, and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

8.6.4.3 bit7

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set. An invalid setting of the WRITE_PROTECT command results in no write protection.

8.6.5 STORE_USER_ALL (15h)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'oth' bit in the STATUS_CML registers.

The following registers can be stored to EEPROM memory using STORE_USER_ALL:

- ON_OFF_CONFIG
- WRITE_PROTECT
- VIN_ON
- VIN_OFF
- IOUT_CAL_OFFSET
- IOUT_OC_FAULT_LIMIT
- IOUT_OC_WARN_LIMIT
- IOUT_OC_FAULT_RESPONSE
- OT_FAULT_LIMIT
- OT_WARN_LIMIT
- TON_RISE
- MFR_SPECIFIC_00
- VREF_TRIM
- STEP_VREF_MARGIN_HIGH
- STEP_VREF_MARGIN_LOW
- PCT_VOUT_FAULT_PG_LIMIT
- SEQUENCE_TON_TOFF_DELAY
- OPTIONS
- MASK_SMBALERT

8.6.6 RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory.

Do not use this command while the device is actively switching, this causes the device to stop switching and the output voltage to fall during the restore event. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

NOTE

A VIN_UV fault may be triggered when RESTORE_USER_ALL command is set. The firmware workaround is accomplished by verifying that, upon completion of a RESTORE_USER_ALL command, the sole source asserting SMBALERT is the VIN_UV bit in STATUS_BYTE. If so, issue a CLEAR_FAULTS command. Any other source asserting SMBALERT under these circumstances (i.e. completion of RESTORE_USER_ALL) would indicate an actual fault condition.

8.6.7 CAPABILITY (19h)

The CAPABILITY command provides a way for a host system to determine some key capabilities of this PMBus device.

COMMAND	CAPABILITY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	SPD		ALRT	Reserved			
Default Value	1	0	1	1	0	0	0	0

The default values indicate that the device supports Packet Error Checking (PEC), a maximum bus speed of 400 kHz (SPD) and the SMBus Alert Response Protocol using SMBALERT.

8.6.8 VOUT_MODE (20h)

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are fixed and do not permit the user to change the values.

COMMAND	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	0	1	1	1

8.6.8.1 Mode:

Value fixed at 000, linear mode.

8.6.8.2 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9.

8.6.9 VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_ON values are shown in Table 5:

Table 5. Supported VIN_ON Values

VIN_ON Values (V)				
4.25 (default)	4.5	4.75	5	5.25
5.5	5.75	6	6.25	6.5
6.75	7	7.25	7.5	8
8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5
12	12.5	13	14	15
16				

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

COMMAND	VIN_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1

8.6.9.1 Exponent

–2 (dec), fixed.

8.6.9.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 17 (dec), corresponding to a default of 4.25 V.

8.6.10 VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_OFF values are shown in Table 6:

Table 6. Supported VIN_OFF Values

VIN_OFF Values (V)				
4 (default)	4.25	4.5	4.75	5
5.25	5.5	5.75	6	6.25
6.5	6.75	7	7.25	7.5
8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25
11.75	12	13.75	14.75	15.75

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the cml bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

COMMAND	VIN_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0

8.6.10.1 Exponent

–2 (dec), fixed.

8.6.10.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 16 (dec). This corresponds to a default value of 4.0 V.

8.6.11 IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5 mA and the range is +3937.5 mA to -4000 mA. Values written outside of this range alias into the supported range. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

COMMAND	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.11.1 Exponent

–4 (dec), fixed.

8.6.11.2 Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec).

8.6.12 IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. The IOUT_OC_FAULT_LIMIT should be set equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert SMBALERT. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	See Below															

8.6.12.1 Exponent

–1 (dec), fixed.

8.6.12.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable.

The actual output current for a given mantissa and exponent is shown in Equation 5.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (5)$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_FAULT_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPS544C20	5	39	45	A
TPS544B20	5	26	30	A

8.6.13 IOUT_OC_FAULT_RESPONSE (47h)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT undervoltage (UV) fault. The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT or POUT bit in the STATUS_WORD
- Sets the IOUT OC Fault bit in the STATUS_IOUT register
- Notifies the PMBus host by asserting $\overline{\text{SMBALERT}}$

The contents of this register can be stored to non-volatile memory using the STORE_USER command.

COMMAND	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r	r	r
Function	X	X	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	1	1	1	1	1	1

8.6.13.1 RS[2:0]

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert $\overline{\text{SMBALERT}}$ along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

8.6.14 IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the IOUT or POUT bit in the STATUS_WORD
- Sets the IOUT overcurrent Warning (OCW) bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert $\overline{\text{SMBALERT}}$. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	See Below															

8.6.14.1 Exponent

–1 (dec), fixed.

8.6.14.2 Mantissa

The upper four bits are fixed at 0.
Lower seven bits are programmable.

The actual output warning current level for a given mantissa and exponent is:

$$I_{OUT\,(OCW)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (6)$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_WARN_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPS544C20	4	30	45	A
TPS544B20	4	20	30	A

8.6.15 OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature fault condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the device takes the following actions:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Fault bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature fault is tripped, the output is latched off until the external sensed temperature falls 20°C from the OT_FAULT_LIMIT, at which point the output goes through a normal startup (soft-start).

The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as asserts $\overline{\text{SMBALERT}}$. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The OT_FAULT_LIMIT takes a two byte data word formatted as shown below.

COMMAND	OT_FAULT_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

8.6.15.1 Exponent

0 (dec), fixed.

8.6.15.2 Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 150 (dec).

The default over-temperature fault setting is 150°C. Values can range from 120°C to 165°C in 1°C increments.

8.6.16 OT_WARN_LIMIT (51h)

The OT_ WARN _LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature warning condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature warning, the device takes the following actions:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature warning is tripped, the warning flag is latched until the external sensed temperature falls 20°C from the OT_WARN_LIMIT.

The OT_WARN_LIMIT must always be less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than or equal to OT_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert $\overline{\text{SMBALERT}}$. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The OT_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	OT_WARN_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

8.6.16.1 Exponent

0 (dec), fixed.

8.6.16.2 Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 125 (dec).

The default over-temperature fault setting is 125°C. Values can range from 100°C to 140°C in 1°C increments.

8.6.17 TON_RISE (61h)

The TON_RISE command sets the time in ms, from when the reference starts to rise until the voltage has entered the regulation band. It also determines the rate of the transition of the reference voltage (either due to VREF_TRIM or STEP_VREF_MARGIN_x commands) when this transition is executed during the soft-start period. There are several discrete settings that this command supports. Commanding a value other than one of these values results in the nearest supported value being selected.

The supported TON_RISE times over PMBus are shown in Table 7:

Table 7. Supported TON_RISE Values

TON_RISE VALUES (ms)				
0.6	0.9	1.2	1.7	2.7 (default)
4.2	6.0	9.0		

A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The TON_RISE command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	1

8.6.17.1 Exponent

–4 (dec), fixed.

8.6.17.2 Mantissa

The upper two bits are fixed at 0.
The lower eight bits are programmable with a default value of 43 (dec).

8.6.18 STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults.

COMMAND	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In this family of devices, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred. Check STATUS_TEMPERATURE.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred. Check STATUS_CML.

NONE OF THE ABOVE:

A fault or warning not listed in bit1 through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition. Check other status registers.

8.6.19 STATUS_WORD (79h)

The STATUS_WORD command returns two bytes of information with a summary of the device fault and warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

COMMAND	STATUS_WORD (low byte) = STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	x	0	0	0	0	0	0

A "1" in any of the low byte (STATUS_BYTE) bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In this family of devices this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred. Check STATUS_TEMPERATURE.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred. Check STATUS_CML.

NONE OF THE ABOVE:

A fault or warning not listed in bits 1-7 has occurred. See other status registers.

COMMAND	STATUS_WORD (high byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT	IOUT or POUT	X	MFR	$\overline{\text{POWER\_GOOD}}$	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of the high byte bit positions indicates that:

VOUT:

An output voltage fault or warning has occurred. Check STATUS_VOUT.

IOUT/POUT:

An output current warning or fault has occurred. The PMBus specification states that this warning also applies to output power. This family of devices does not support output power warnings or faults. Check STATUS_IOUT.

MFR:

An internal thermal shutdown (TSD) fault has occurred in the device. Check STATUS_MFR_SPECIFIC.

$\overline{\text{POWER\_GOOD}}$:

The power good signal has not transitioned from high-to-low.

8.6.20 STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte of information relating to the status of the output voltage related faults. The only bits of this register supported are:

- VOUT_OV Fault
- VOUT_UV Fault

COMMAND	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT OV Fault	X	X	VOUT UV Fault	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

VOUT OV Fault:

The device has seen the output voltage rise above the output overvoltage threshold.

VOUT UV Fault:

The device has seen the output voltage fall below the output undervoltage threshold.

8.6.21 STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte of information relating to the status of the output current related faults. The only bits of this register supported are:

- IOUT_OC Fault
- IOUT_OC Warning

COMMAND	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OC Fault	X	IOUT_OC Warning	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

IOUT_OC Fault:

The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT.

IOUT_OC Warn:

The device has seen the output current rise relating to the level set by IOUT_OC_WARN_LIMIT.

8.6.22 STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults. The only bits of this register supported are:

- OT Fault
- OT Warning

COMMAND	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OT Fault	OT Warning	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OT Fault:

The measured external temperature has exceeded the level set by OT_FAULT_LIMIT.

OT Warning:

The measured external temperature has exceeded the level set by OT_WARN_LIMIT.

8.6.23 STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults. The bits of this register supported by the this family of devices are:

- Invalid or Unsuppported Command
- Invalid or Unsupported Data
- Packet Error Check Failed
- Memory Fault Detected
- Other Communication Fault.

COMMAND	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid or Unsupported Command	Invalid or Unsupported Data	Packet Error Check Failed	Memory Fault Detected	X	X	Other Communication Fault	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

Invalid or Unsupported Command:

An invalid or unsupported command has been received.

Invalid or Unsupported Data

Invalid or unsupported data has been received

Packet Error Check Failed

A packet has failed the CRC checksum error check.

Memory Fault Detected

A fault has been detected with the internal memory.

Other Communication Fault

Some other communication fault or error has occurred

8.6.24 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer-specific faults or warnings.

COMMAND	STATUS_MFR_SPECIFIC							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OTFI	X	X	IVADDR	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OTFI:

The internal temperature is above the thermal shutdown (TSD) fault threshold

IVADDR:

The PMBus address detection circuit is not resolving to a valid address. In this event, the device responds to the address 127 (dec).

8.6.25 READ_VOUT (8Bh)

The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the controller. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The data format is as shown below:

COMMAND	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command as well. In this family of devices, VOUT_MODE is set to linear mode with an exponent of –9 and cannot be altered. The output voltage calculation is shown in Equation 7.

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (7)$$

8.6.26 READ_IOUT (8Ch)

The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the controller. The average output current is sensed according to the method described in *Low-Side MOSFET Current Sensing and Overcurrent Protection*. The data format is as shown below:

COMMAND	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The device scales the output current before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA. The maximum value that can be reported is 64 A. The user must set the IOUT_CAL_OFFSET parameter correctly in order to obtain accurate results. Calculate the output current using Equation 8.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (8)$$

8.6.26.1 Exponent

Fixed at -4.

8.6.26.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the average output current, as indicated by the output of the internal current sense amplifier. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A.

8.6.27 READ_TEMPERATURE_2 (8Eh)

The READ_TEMPERATURE_2 command returns the external temperature in degrees Celsius of the current channel.

COMMAND	READ_TEMPERATURE_2															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

8.6.27.1 Exponent

0 (dec), fixed.

8.6.27.2 Mantissa

The lower 11 bits are the result of the ADC conversion of the external temperature. The default reading is 25 (dec) corresponding to a temperature of 25°C.

8.6.28 PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that these devices are compatible with the 1.1 revision of the PMBus specification.

COMMAND	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	0	1	0	0	0	1

8.6.29 MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 register is dedicated as a user scratch pad.

COMMAND	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	User scratch pad															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

8.6.30 VREF_TRIM (MFR_SPECIFIC_04) (D4h)

The VREF_TRIM command applies a fixed offset voltage to the reference voltage. It is most typically used to trim the output voltage at the time the PMBus device is assembled into the final application design. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

the settings of the VOUT_MODE command determine the effect of VREF_TRIM command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal).

$$V_{REF(offset)} = VREF\_TRIM \times 2^{-9} \quad (9)$$

The maximum trim ranges between –20% to +10% of the nominal reference voltage (600 mV) in 2 mV steps. Permissible values range from –120 mV to +60 mV. If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is –180 mV to +60 mV (-30% to +10%). If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during the soft-start period. Any transition in the reference voltage after soft-start is complete occurs at the slew rate defined by the slowest soft-start time, or 0.067 mV/µs. For example, a trim which moves the reference by 10%, occurs in approximately 900 µs.

COMMAND	VREF_TRIM															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.6.31 STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h)

The STEP_VREF_MARGIN_HIGH command sets the target voltage which the reference voltage changes to when the OPERATION command is set to "Margin High". The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). The actual reference voltage commanded by a margin high command can be found by:

$$V_{REF(MH)} = (STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM) \times 2^{-9} \quad (10)$$

The margin high range is between 0% and 10% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from 0 mV to 60 mV. If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is –180 mV to 60 mV (-30% to 10%). If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the slew rate defined by the slowest soft-start time, or 0.067 mV/µs. For example, a trim which moves the reference by 10%, occurs in approximately 900 µs.

COMMAND	STEP_VREF_MARGIN_HIGH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

The default value of STEP_VREF_MARGIN_HIGH is 30 (dec), corresponding to a default margin high voltage of 60 mV (+10%) .

8.6.32 STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h)

The STEP_VREF_MARGIN_LOW command sets the target voltage which the reference voltage changes to when the OPERATION command is set to *Margin Low*. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). Equation 11 shows the actual output voltage commanded by a margin high command.

$$V_{REF(ML)} = (STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM) \times 2^{-9} \quad (11)$$

The margin low ranges between –20% and 0% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from –120 mV to 0 mV. If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is –180 mV to 60 mV (–30% to +10%). If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during the soft-start period. Any transition in the reference voltage after soft-start is complete occurs at the slew rate defined by the slowest soft-start time, or 0.067 mV/µs. For example, a trim which moves the reference by 10%, occurs in approximately 900 µs.

COMMAND	STEP_VREF_MARGIN_LOW															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0

The default value of STEP_VREF_MARGIN_LOW is –30 (dec), corresponding to a default margin low voltage of –60 mV (–10%).

8.6.33 PCT_VOUT_FAULT_PG_LIMIT (MFR_SPECIFIC_07) (D7h)

The PCT_VOUT_FAULT_PG_LIMIT command is used to set the PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) limits as a percentage of nominal.

The PCT_VOUT_FAULT_PG_LIMIT takes a one byte data word formatted as shown below:

COMMAND	PCT_VOUT_FAULT_PG_LIMIT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PCT_MSB	PCT_LSB
Default Value	0	0	0	0	0	0	0	0

The PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) settings are shown in Table 8, as a percentage of nominal reference voltage on the FB pin.

Table 8. Protection Settings (typical)

PCT_MSB	PCT_LSB	UV	PGL LOW	PGH HIGH	OV
0	0	-16.8%	-12.5%	12.5%	16.8%
0	1	-12.0%	-7.0%	7.0%	12.0%
1	0	-28.0%	-22.0%	7.0%	12.0%
1	1	-42.0%	-36.0%	7.0%	12.0%

The PGOOD pin may trip if the output voltage is too high (using PGH high) or too low (using PGL low). Additionally, the PGOOD pin has hysteresis.

Additionally, when output overvoltage (OV) is tripped, the output must lower below the PGH high threshold minus the hysteresis, before PGOOD and OV are reset. Likewise, when output undervoltage (UV) is tripped, the output must rise above the PGOOD high threshold plus the hysteresis, before PGOOD and UV are reset.

8.6.34 SEQUENCE_TON_TOFF_DELAY (MFR_SPECIFIC_08) (D8h)

The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and turning off the device as a ratio of TON_RISE.

The SEQUENCE_TON_TOFF_DELAY takes a one byte data word formatted as shown below:

COMMAND	SEQUENCE_TON_TOFF_DELAY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r	r/w	r/w	r/w	r
Function	TON_DELAY			X	TOFF_DELAY			X
Default Value	0	0	0	0	0	0	0	0

TON_DELAY:

This parameter selects the delay from when the output is enabled until soft-start beings, as an integer multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1. When TON_DELAY = 0, the device imposes a minimum delay of 50 µs.

TOFF_DELAY:

This parameter selects the delay from when the output is disabled until the output stops switching, as an integer multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1.

8.6.35 OPTIONS (MFR_SPECIFIC_21) (E5h)

The OPTIONS register can be used for setting user selectable options, as shown below.

COMMAND	OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r	r
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	EN_ADC_CNTL	X	X
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

A “1” in any of these bit positions indicates that:

EN_ADC_CNTL:

Enables ADC operation used for voltage, current and temperature monitoring.

NOTE

The EN_ADC_CNTL bit must be set in order to enable output voltage, current and temperature telemetry. When the EN_ADC_CNTL bit is zero, the READ_VOUT, READ_IOUT and READ_TEMPERATURE_2 registers do not update continuously, and retain their previous values from the last time EN_ADC_CNTL was set.

8.6.36 MASK_SMBALERT (MFR_SPECIFIC_23) (E7h)

The MASK SMBALERT command may be used to prevent a warning or fault condition from asserting $\overline{\text{SMBALERT}}$.

COMMAND	MASK_SMBALERT (High Byte)							
Format	Unsigned Binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	mOTFI	mPRTCL	mSMBTO	mIVC	mIVD	mPEC	mMEM	Auto_ARA
Default Value	0	0	0	0	0	0	0	1

COMMAND	MASK_SMBALERT (Low Byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	mOTF	mOTW	mOCF	mOCW	mOVF	mUVF	mPGOOD	mVIN_UV
Default Value	0	0	0	0	0	0	0	0

8.6.36.1 mOTFI

This bit controls whether an internal overtemperature fault (OTFI) asserts $\overline{\text{SMBALERT}}$.

- 0: OTFI (STATUS_MFR_SPECIFIC[7]) asserts $\overline{\text{SMBALERT}}$.
- 1: OTFI does not assert $\overline{\text{SMBALERT}}$.

8.6.36.2 mPRTCL

This bit controls whether an SMBus Protocol Error causes $\overline{\text{SMBALERT}}$ to assert.

- 0: SMBus Protocol Errors assert $\overline{\text{SMBALERT}}$.
- 1: SMBus Protocol Errors do not assert $\overline{\text{SMBALERT}}$.

8.6.36.3 mSMBTO

This bit controls whether an SMBus Timeout causes SMBALERT to assert.

- 0: SMBus Timeout asserts SMBALERT.
- 1: SMBus Timeout does not assert SMBALERT.

8.6.36.4 mIVC

This bit controls whether an invalid command (IVC) causes SMBALERT to assert.

- 0: Issuing an invalid command asserts SMBALERT.
- 1: Issuing an invalid command does not assert SMBALERT.

8.6.36.5 mIVD

This bit controls whether an invalid or unsupported data (IVD) causes SMBALERT to assert.

- 0: Issuing invalid or unsupported data asserts SMBALERT.
- 1: Issuing invalid or unsupported data does not assert SMBALERT.

8.6.36.6 mPEC

This bit controls whether an invalid packet error check (PEC) byte causes SMBALERT to assert.

- 0: Invalid PEC byte asserts SMBALERT.
- 1: Invalid PEC byte does not assert SMBALERT.

8.6.36.7 mMEM

This bit controls whether a memory error (MEM) causes SMBALERT to assert.

- 0: Memory error (MEM) asserts SMBALERT.
- 1: Memory error (MEM) does not assert SMBALERT.

8.6.36.8 Auto_ARA

This bit controls whether the *Auto ARA Response* is enabled.

- 0: Auto ARA is disabled. Host must take all action necessary to clear SMBALERT
- 1: Auto ARA is enabled. The device releases SMBALERT after successfully responding to an ARA from the host.

8.6.36.9 mOTF

This bit controls whether an overtemperature fault (OTF) causes SMBALERT to assert.

- 0: Overtemperature fault (OTF) asserts SMBALERT.
- 1: Overtemperature fault does not assert SMBALERT.

8.6.36.10 mOTW

This bit controls whether an overtemperature warning (OTW) causes SMBALERT to assert.

- 0: Overtemperature warning (OTW) asserts SMBALERT.
- 1: Overtemperature warning (OTW) does not assert SMBALERT.

8.6.36.11 mOCF

This bit controls whether an overcurrent fault (OCF) causes SMBALERT to assert.

- 0: Overcurrent fault (OCF) asserts SMBALERT to assert.
- 1: Overcurrent fault (OCF) does not assert SMBALERT.

8.6.36.12 mOCW

This bit controls whether an overcurrent warning (OCW) causes SMBALERT to assert.

- 0: Overcurrent warning (OCW) asserts SMBALERT.
- 1: Overcurrent warning (OCW) does not assert SMBALERT.

8.6.36.13 mOVF

This bit controls whether an output overvoltage (OVF) causes $\overline{\text{SMBALERT}}$ to assert.

- 0: Output overvoltage fault (OVF) causes $\overline{\text{SMBALERT}}$ to assert.
- 1: Mask $\overline{\text{SMBALERT}}$ assertion due to STATUS_VOUT[7].

8.6.36.14 mUVF

This bit controls whether an output undervoltage (UVF) causes $\overline{\text{SMBALERT}}$ to assert.

- 0: Output undervoltage fault (UVF) asserts $\overline{\text{SMBALERT}}$.
- 1: Output undervoltage fault does not assert $\overline{\text{SMBALERT}}$.

8.6.36.15 mPGOOD

This bit controls whether a PGOOD transition from high-to-low causes $\overline{\text{SMBALERT}}$ to assert.

- 0: PGOOD transition from high-to-low asserts $\overline{\text{SMBALERT}}$.
- 1: PGOOD transition from high to low does not assert $\overline{\text{SMBALERT}}$.

8.6.36.16 mVIN_UV

This bit controls whether an input undervoltage fault (VIN_UV) causes $\overline{\text{SMBALERT}}$ to assert.

- 0: Input undervoltage fault (VIN_UV) asserts $\overline{\text{SMBALERT}}$.
- 1: Input undervoltage fault (VIN_UV) does not assert $\overline{\text{SMBALERT}}$.

8.6.37 DEVICE_CODE (MFR_SPECIFIC_44) (FCh)

The DEVICE_CODE command returns a two byte unsigned binary 12-bit device identifier code and 4-bit revision code in the following format.

COMMAND	MFR_SPECIFIC_44															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Identifier Code												Revision Code			
Default Value	See Below.															

This command provides similar information to the DEVICE_ID command but for devices that do not support block read and write functions.

The fixed, read-only values for each device are summarized below:

DEVICE	IDENTIFIER CODE	REVISION CODE	REGISTER VALUE
TPS544C20	015h	3h	0153h
TPS544B20	014h	3h	0143h

9 Applications and Implementation

9.1 Application Information

The TPS544B20 and TPS544C20 devices are highly-integrated synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 20 A and 30 A respectively.

9.2 Typical Application

Use the following design procedure to select key component values for this family of devices, and set the appropriate behavioral options according to the PMBus protocol.

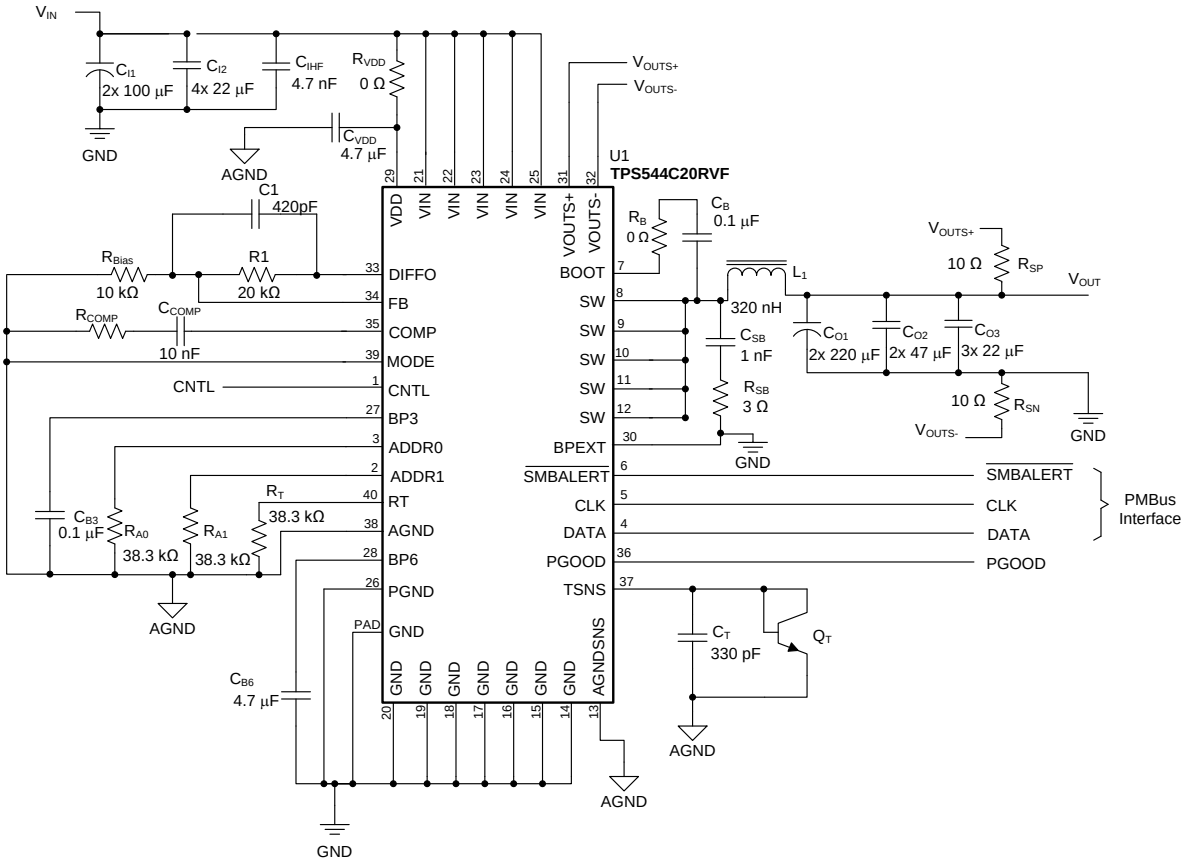


Figure 32. TPS544C20 4.5-V to 18-V Input, 1.8-V Output, 30-A Converter

9.2.1 Design Requirements

For this design example, use the following input parameters.

Table 9. Design Example Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_I	Input voltage		4.5	12.0	18.0	V
$V_{I(ripple)}$	Input ripple voltage	I_{OUT} = 30 A			0.4	V
V_O	Output voltage			1.8		V
	Line regulation	4.5 V ≤ V_I ≤ 18 V			0.5%	
	Load regulation	0 V ≤ I_O ≤ 30 A			0.5%	
$V_{(PP)}$	Output ripple voltage	I_O = 30 A			18	mV
$V_{(OVER)}$	Transient response overshoot	$I_{(STEP)}$ = 10 A			36	mV

Typical Application (continued)

Table 9. Design Example Specifications (continued)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{(UNDER)}$	Transient response undershoot	$I_{(STEP)}$ = 10 A	-36			mV
I_O	Output current	5 V ≤ V_I ≤ 18 V	0	20	30	A
t_{SS}	Soft-start time	V_I = 12 V		2.7		ms
I_{OC}	Overcurrent trip point			40		A
η	Efficiency	I_O = 20 A, V_I = 12 V		90%		
f_{SW}	Switching frequency			500		kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Switching Frequency Selection

There is a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency produce higher switch losses, which decrease efficiency and impact thermal performance. In this design, a moderate switching frequency of 500 kHz achieves both a balance between a small solution size and high-efficiency operation. With the frequency selected, use Table 1 to select the timing resistor. For a frequency of 500 kHz R_{RT} is 38.2 kΩ.

9.2.2.2 Inductor Selection

To calculate the value of the output inductor, use Equation 12. The coefficient K_{IND} represents the amount of peak-to-peak inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current; therefore, choosing a high inductor ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. To achieve balanced performance, maintain a K_{IND} coefficient between 0.3 and 0.4. Using this target ripple current, the required inductor size can be calculated as shown in Equation 12.

$$L1 = \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \times \frac{V_{IN} - V_{OUT}}{I_{OUT(max)} \times K_{IND}} = \frac{1.8\,V \times (18\,V - 1.8\,V)}{18\,V \times 500\,kHz \times 0.3} = 360\,nH \quad (12)$$

Selecting K_{IND} = 0.3, the target inductance L_1 = 360 nH. Using the next standard value, the 320 nH Pulse (brand) PG077.321NL is chosen in this application for its high current rating, low DCR, and small size. The inductor ripple current, RMS current, and peak current can be calculated using Equation 13, Equation 14 and Equation 15. These values should be used to select an inductor with approximately the target inductance value, and current ratings that allow normal operation with some margin.

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \times \frac{V_{IN(max)} - V_{OUT}}{L1} = \frac{1.8\,V \times (18\,V - 1.8\,V)}{18\,V \times 500\,kHz \times 320\,nH} = 10.1\,A \quad (13)$$

$$I_{L(rms)} = \sqrt{I_{OUT(max)}^2 + \frac{1}{12} I_{RIPPLE}^2} = \sqrt{(30\,A)^2 + \frac{1}{12}(10.1\,A)^2} = 30.14\,A \quad (14)$$

$$I_{L\ peak} = I_{OUT} + \frac{1}{2} I_{RIPPLE} = 30\,A + \frac{1}{2} \times 10.1A = 35.1\,A \quad (15)$$

The Pulse PG077.321NL is rated for 45 A RMS current, and 48-A saturation. Using this inductor, the ripple current I_{RIPPLE}= 10.1 A, the RMS inductor current $I_{L(rms)}$= 30.14 A, and peak inductor current $I_{L(peak)}$= 35 A.

9.2.2.3 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- how the regulator responds to a load transition
- the output voltage ripple
- the minimum output capacitance needed to maintain stable D-CAP2 mode control

The output capacitance needs to be selected based on the most stringent of these three criteria.

9.2.2.3.1 Response to a Load Transition

The desired response to a load transition is the first criterion. The output capacitor must supply the load with the required current when not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation during the transient.

These devices use Adaptive Constant On-Time (COT) control. During a transient, the ON-time remains unchanged from normal operation, but the off-time shortens to allow a rapid increase in the inductor current in order to meet the demands of the load transition. To estimate the time required to respond to a load increase, calculate the number of switching cycles required to change the inductor current using Equation 16.

$$\#_{cycles} \approx \frac{I_{TRAN}}{I_{RIPPLE}} = \frac{10\ A}{10.1\ A} = 1 \tag{16}$$

And estimate the time needed to produce that number of cycles during a transient as Equation 17:

$$T_{TRANS} \approx \frac{\#_{cycle}}{2 \times f_{SW}} \left(1 + \frac{V_{OUT}}{V_{IN\,(min)}}\right) = \frac{1}{2 \times 500\ kHz} \left(1 + \frac{1.8\ V}{4.5\ V}\right) = 1.4\ \mu s \tag{17}$$

The output capacitor must support the full change in output current for half of the time, so the minimum output capacitance can be estimated by Equation 18:

$$C_{undershoot} = \frac{I_{TRAN} \times T_{TRANS}}{2 \times V_{Under}} = \frac{10\ A \times 1.4\ \mu s}{2 \times 36\ mV} = 193\ \mu F \tag{18}$$

The output capacitor must also absorb the full change in output current for half of the time needed to remove the excess current from the inductor during a rapid load decrease. This minimum output capacitance can be estimated using Equation 19:

$$C_{overshoot} = \frac{(I_{TRAN})^2 \times L1}{V_{OUT} \times V_{OVER}} = \frac{(10\ A)^2 \times 320\ nH}{1.8\ V \times 36\ mV} = 494\ \mu F \tag{19}$$

In order to meet the transient response requirements, the output capacitance must be greater than the larger of $C_{undershoot}$ and $C_{overshoot}$.

In this case, the highest minimum output capacitance ($C_{OUT(min)}$) to meet the response to a load transition is the overshoot requirement, which dictates the minimum output capacitance. Therefore, using Equation 19, the minimum output capacitance required to meet the transient requirement is 494 µF.

9.2.2.3.2 Output Voltage Ripple

The output voltage ripple is the second criterion. Equation 20 calculates the minimum output capacitance required to meet the output voltage ripple specification. This criterion is the requirement when the impedance of the output capacitance is dominated by ESR.

$$C_{ripple} = \frac{1}{8 \times f_{SW}} \times \frac{I_{RIPPLE}}{V_{OUT\,(ripple)}} = \frac{10.1\ A}{8 \times 500\ kHz \times 18\ mV} = 140\ \mu F \tag{20}$$

In this case, the maximum output voltage ripple is 18 mV. Under this requirement, the minimum output capacitance for ripple (as calculated in Equation 20) yields 140 µF. Because this capacitance value is smaller than the output capacitance required to meet the transient response, select the output capacitance value based on the transient requirement. For this application, two 220-µF, low-ESR polymer bulk capacitors, three 47-µF capacitors and three 22-µF ceramic capacitors are selected to meet the transient specification with at least 80% margin. Therefore C_{OUT} equals 647 µF.

With the target output capacitance value chosen, Equation 21 calculates the maximum ESR the output capacitor bank can have to meet the output voltage ripple specification. Equation 21 indicates the ESR should be less than 1.4 mΩ. The six ceramic capacitors each contribute approximately 2 mΩ, making the effective ESR of the output capacitor bank approximately 0.33 mΩ, meeting the specification with sufficient margin.

$$ESR_{MAX} = \frac{V_{OUT\ ripple} - \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}}{I_{RIPPLE}} = \frac{18\ mV - \frac{10.1\ A}{8 \times 500\ kHz \times 647\ \mu F}}{10.1\ A} = 1.4\ m\Omega \quad (21)$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in, which increases the minimum required capacitance value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Equation 22 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 22 yields 2.28 A.

$$I_{CO(rms)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\sqrt{12} \times V_{IN(max)} \times L1 \times f_{SW}} = \frac{1.8\ V \times (18\ V - 1.8\ V)}{\sqrt{12} \times 18\ V \times 320\ nH \times 500\ kHz} = 2.92\ A \quad (22)$$

9.2.2.4 D-CAP Mode and D-CAP2 Mode Stability

D-CAP mode control requires that the ESR ripple at the FB pin be at least 15 mV (or 2.5%) of the output voltage and the ESR-zero frequency of the output capacitor is less than 1/4 the switching frequency. Because this design requires output voltage ripple less than 2.5% of the output voltage and uses low-ESR, specialty polymer, and ceramic output capacitors, this design uses D-CAP2 mode control. Because D-CAP2 mode control uses an internally generated ramp to emulate the ESR of the output capacitor, D-CAP2 mode requires sufficient output capacitance to maintain an effective ESR-zero frequency less than 1/4 of the nominal switching frequency with this emulated ESR. The minimum capacitance for stability can be calculated in Equation 23 using τ_{Iem} from Table 10:

$$C_{stability} = \frac{2 \times V_{ref} \times \tau_{Iem}}{\pi \times V_{OUT} \times L1 \times f_{SW}} = \frac{2 \times 600\ mV \times 76\ \mu s}{3.14 \times 1.8\ V \times 320\ nH \times 500\ kHz} = 100\ \mu F \quad (23)$$

Table 10. D-CAP2 Mode Current Emulation Time Constants

NOMINAL FREQUENCY (kHz)	τ_{Iem}(µs)
250	104
300	98
400	87
500	76
650	60
750	52
850	44
1000	33

9.2.2.5 Input Capacitor Selection

The TPS544B20 and TPS544C20 devices require a capacitor with these features:

- high-quality
- ceramic
- type X5R or X7R
- input decoupling feature
- a value of at least 4.7 µF of effective capacitance on the VDD pin, relative to AGND

The power stage input decoupling capacitance (effective capacitance at the VIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using Equation 24.

$$I_{CIN\,(rms)} = I_{OUT\,(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN\,(min)}} \times \frac{\left(V_{IN\,(min)} - V_{OUT}\right)}{V_{IN\,(min)}}} = 30\ A \times \sqrt{\frac{1.8\ V}{4.5\ V} \times \frac{(4.5\ V - 1.8\ V)}{4.5\ V}} = 14.7\ Arms \tag{24}$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in Equation 25 and Equation 26. The input ripple is composed of a capacitive portion, $V_{RIPPLE(cap)}$, and a resistive portion, $V_{RIPPLE(esr)}$.

$$C_{IN\,(min)} = \frac{I_{OUT\,(max)} \times V_{OUT}}{V_{ripple\ (cap)} \times V_{IN\,(max)} \times f_{SW}} = \frac{30\ A \times 1.8\ V}{100\ mV \times 18\ V \times 500\ kHz} = 60\ \mu F \tag{25}$$

$$ESR_{CIN\ \ max} = \frac{V_{RIPPLE\ \ ESR}}{I_{OUT\ \ max} + \frac{1}{2} I_{RIPPLE}} = \frac{0.1\ V}{30\ A + \frac{1}{2} \times\ 10.1\ A} = 2.8\ m\Omega \tag{26}$$

The value of a ceramic capacitor varies significantly with temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectric capacitors are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable during temperature changes. The input capacitor must also be selected with the DC bias taken into account. To support the maximum input voltage, this design requires a ceramic capacitor with a rating of at least 25 V. Allow 0.1-V input ripple for $V_{RIPPLE(cap)}$, and 0.3-V input ripple for $V_{RIPPLE(esr)}$. Using Equation 25 and Equation 26, the minimum input capacitance for this design is 60 µF, and the maximum ESR is 2.8 mΩ. Four 22-µF, 25-V ceramic capacitors and two additional 100-µF, 25-V low-ESR polymer capacitors in parallel were selected for the power stage. For the VDD pin, one 4.7-µF, 25-V ceramic capacitor was selected. The input voltage (VIN) and power input voltage (PVIN) pins must be tied together. The input capacitance value determines the input ripple voltage of the regulator. Using the design example values, $I_{OUT(max)}$ = 30 A, C_{IN} = 288 µF, f_{SW} = 500 kHz, yields a maximum RMS input ripple current of 14.7 Arms.

9.2.2.6 Bootstrap Capacitor and Resistor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have voltage rating of 25 V or higher. To reduce the dV/dt of the rising edge of the SW node, reduce ringing and EMI, a resistor R_{BOOT} up to 5 Ω can be placed in series with the bootstrap capacitor.

9.2.2.7 BP6, BP3 and BPEXT

This design does not include an auxiliary 5-V supply, so BPEXT is terminated to PGND. According to the recommendations in , BP3 is bypassed to AGND with 100 nF of capacitance, and BP6 is bypassed to PGND with 4.7-µF of capacitance. In order for the regulator to function properly, it is important that these capacitors be located close to the TPS544C20, with low-impedance return paths to AGND or GND as appropriate. See Figure 45 for more information.

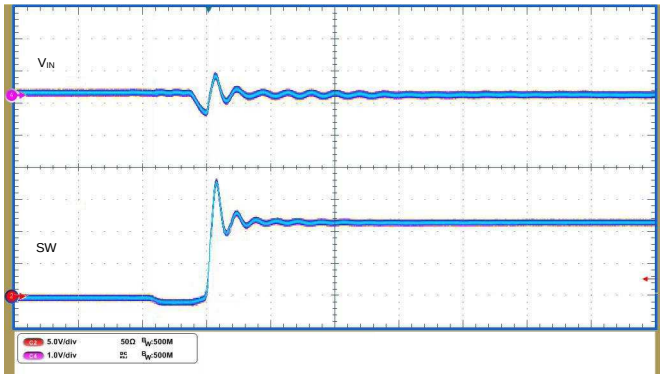
9.2.2.8 R-C Snubber and VIN Pin High-Frequency Bypass

Although it is possible to operate the TPS544C20 within absolute maximum ratings without including any ringing reduction techniques, some designs may require external components to further reduce ringing levels. This example uses two approaches:

- a high frequency power stage bypass capacitor on the VIN pins
- an R-C snubber between the SW and GND

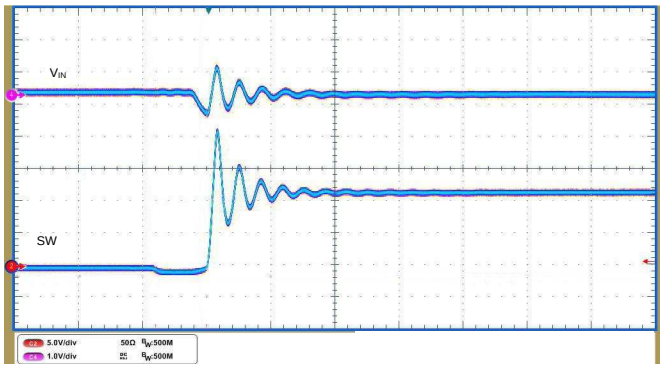
Including a high-frequency bypass capacitor is a lossless ringing reduction technique which helps minimizes the outboard parasitic inductances in the power stage. These capacitors store energy during the low-side MOSFET on-time, and discharge once the high-side MOSFET is turned on. For this example a 4.7-nF, 25-V, 0402 sized high-frequency capacitor is selected. The placement of this capacitor (shown in Figure 46) is critical to its effectiveness.

Additionally, an R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 1-nF capacitor and a 3-Ω resistor are chosen. In this example an 0805 resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. Figure 33 and Figure 34 show the effect of the R-C snubber on the rising edge of the SW pin. See SLUP100 for more information about snubber circuits.



V_{IN} = 12 V I_{OUT} = 20 A Snubber = 1nF + 3Ω

Figure 33. SW Rising Edge



V_{IN} = 12 V I_{OUT} = 20 A Snubber = Open

Figure 34. SW Rising Edge

9.2.2.9 Temperature Sensor

This application design uses a surface-mount MMBT3904SL for the temperature sensor, Q_T. In this example, the sensor monitors the PCB temperature where it is generally the highest, next to the power inductor. Placement of the temperature sensor and routing back to the TSNS pin are critical design features to reduce noise its temperature measurements. In this example, the temperature sensor is placed on the V_{OUT} side of the power inductor to avoid switching noise from the SW plane, and routed back to the TSNS and AGND pin. Additionally, a 330-pF capacitor, C_T, is placed from TSNS to AGND near the TSNS pin.

Disable external temperature sensing by terminating TSNS to AGND with a 0-Ω resistor. This termination forces the temperature readings to –40 °C, and prevents external over-temperature fault trips.

9.2.2.10 Key PMBus Parameter Selection

Several of the key design parameters for the TPS544B20 and TPS544C20 device can be configured according to the PMBus protocol, and stored to its non-volatile memory (NVM) for future use.

9.2.2.10.1 Enable, UVLO and Sequencing

Use the ON_OFF_CONFIG (02h) command to select the turn-on behavior of the converter. For this example, the CNTL pin was used to enable or disable the converter, regardless of the state of OPERATION (01h), as long as input voltage is present, and above the UVLO threshold.

The minimum input voltage, $V_{IN(min)}$, for this example is 4.5 V. The VIN_ON command was set to 4.25 V, and the VIN_OFF command was set to 4.0 V, giving 250 mV of hysteresis. If VIN falls below VIN_OFF, power conversion stops, until it is raised above VIN_ON.

This example lacks specific turn-on or turn-off delay requirements, so SEQUENCE_TON_TOFF_DELAY was used to set both the turn-on and turn-off delays to 0 × the soft-start time, the delay between enabling power conversion, and the rise of the output voltage is approximately 400 µs. See the *Soft-Start* section for more information.

9.2.2.10.2 Soft-Start Time

The TON_RISE command sets the soft-start time. When selecting the soft-start time, consider the charging current for the output capacitors. In some applications (for example those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To avoid nuisance tripping, the output capacitor charging current should be included when choosing a soft-start time, and overcurrent threshold. The capacitor charging current can be calculated using Equation 27.

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.8\ V \times 647\ \mu F}{2.7\ ms} = 432\ mA \quad (27)$$

After calculating the charging current, the overcurrent threshold can then be calibrated to the sum of the maximum load current and the output capacitor charging current plus some margin.

In this example, the soft-start time is arbitrarily selected to be the default value, 2.7 ms. In this case, the charging current, I_{CAP} = 337 mA.

9.2.2.10.3 Overcurrent Threshold and Response

The IOUT_OC_FAULT_LIMIT command sets the overcurrent threshold. The current limit should be set to the maximum load current, plus the output capacitor charging current during start-up, plus some margin for load transitions and component variation. The amount of margin required depends on the individual application, but a suggested starting point is 30%. More or less may be required. For this application, the maximum load current is 30 A, the output capacitor charging current is 337 mA. This design uses the factory default overcurrent threshold of 39 A.

The IOUT_OC_FAULT_RESPONSE command sets the desired response to an overcurrent event. In this example, the converter is configured to latch-off in the event of an overcurrent. TPS544C20 device can also be configured to *hiccup*, (continuously restart waiting for a 7 x soft-start time-out between re-trials.)

9.2.2.10.4 Power Good, Output Overvoltage and Undervoltage Protection

The PCT_VOUT_FAULT_PG_LIMIT command configures the PGOOD, and regulation windows. This example includes a moderate threshold setting. The resulting power good window is ±12.5%, and the resulting overvoltage and undervoltage window is ±16.8%. More or less aggressive protection levels can be selected according to the PMBus protocol.

9.2.2.11 Output Voltage Setting and Frequency Compensation Selection

A feedback divider from DIFFO to AGND sets the output voltage. This design arbitrarily selects an R1 value of 20 kΩ. Using R1 and the desired output voltage, and calculate R_{BIAS} using Equation 28 to be 10 kΩ.

$$R_{Bias} = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R1 = \frac{0.6\ V}{1.8\ V - 0.6\ V} \times 20\ k\Omega = 10\ k\Omega \quad (28)$$

The TPS544B20 and TPS544C20 devices use D-CAP2 mode control with a transconductance error amplifier to eliminate the output voltage error introduced by valley voltage regulation. To stabilize the error amplifer, TI recommends a 10-nF capacitor from COMP to AGND. To improve transient response and increase phase margin, a series resistor, R_{COMP}, can be added. When using R_{COMP}, add a 1.0-nF capacitor from COMP to AGND to limit the error amplifier gain at high frequency. Use Equation 29 to calculate the value of R_{COMP}.

$$R_{COMP} = 3 \times \frac{V_{OUT} \times L1}{V_{ref} \times \tau_{lem}} \times \frac{C_{OUT}}{C_{COMP}} = 3 \times \frac{1.8\ V \times 320\ nH}{0.600\ V \times 76\ \mu s} \times \frac{647\ \mu F}{10\ nF} = 2.45\ k\Omega \quad (29)$$

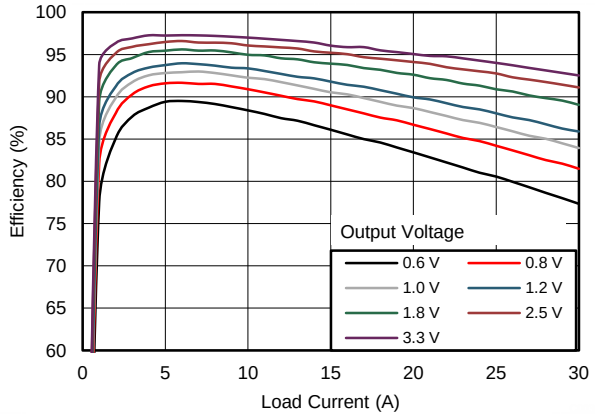
Alternatively, for output voltages 1.2 V and higher, a feedforward capacitor, C1, can be added in parallel with R1 from DIFFO to FB to provide similar improvement to transient response and phase margin. Use Equation 30 to calculate the value of C1.

$$C_1 = \frac{V_{OUT} \times L1}{V_{ref} \times \tau_{lem}} \times \frac{C_{OUT}}{R1} = \frac{1.8\ V \times 320\ nH}{0.600\ V \times 76\ \mu s} \times \frac{647\ \mu F}{20\ k\Omega} = 409\ pF \quad (30)$$

The resulting design example frequency compensation values are:

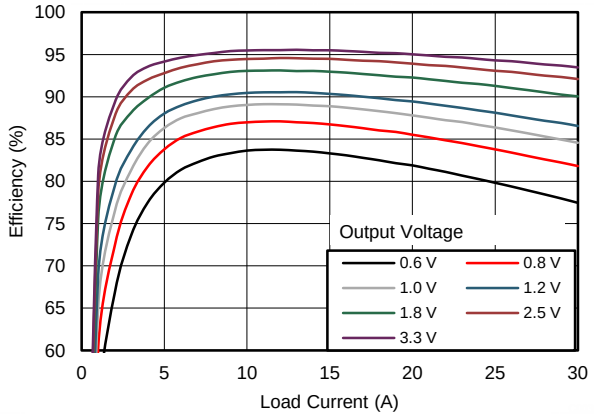
- R1 = 20 kΩ
- R_{BIAS} = 10 kΩ
- C1 = 420 pF

9.2.3 Application Curves



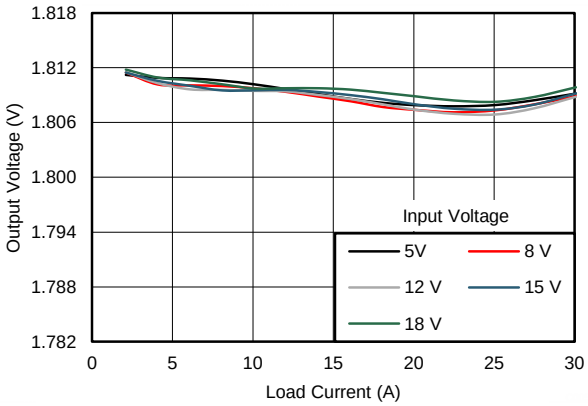
V_{IN} = 5 V f_{SW} = 500 kHz T_A = 25 °C
L = 410 nH Snubber = Open R_{BOOT} = 0 Ω
R_{DCR} = 0.3 mΩ

Figure 35. Power Efficiency vs. Load Current



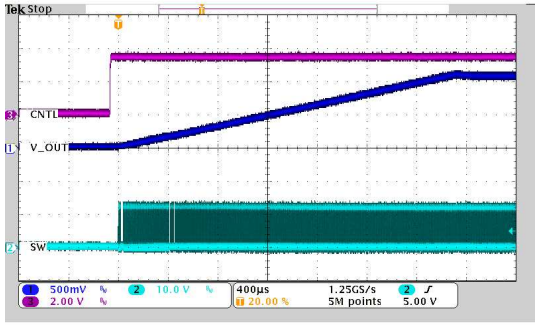
V_{IN} = 12 V f_{SW} = 500 kHz T_A = 25 °C
L = 410 nH Snubber = Open R_{BOOT} = 0 Ω
R_{DCR} = 0.3 mΩ

Figure 36. Power Efficiency, V_{IN} = 12 V



V_{IN} = 12 V

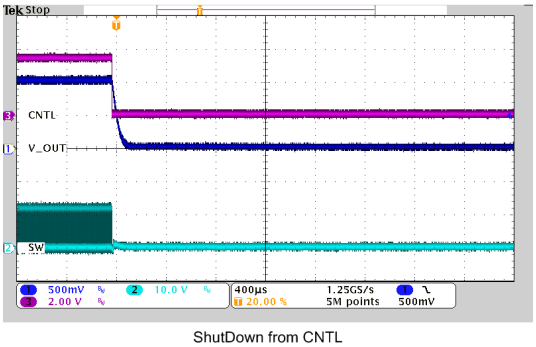
Figure 37. Load Regulation



StartUp from CNTL into 20A

V_{IN} = 12 V I_{OUT} = 20 A

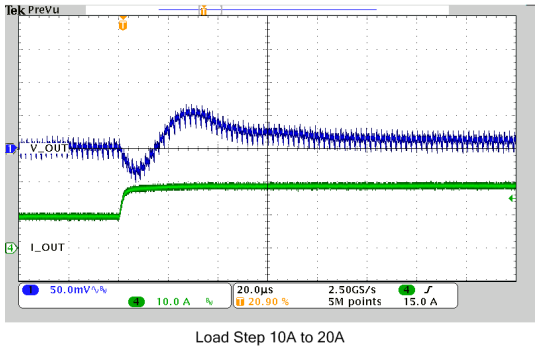
Figure 38. Startup from CNTL



ShutDown from CNTL

V_{IN} = 12 V I_{OUT} = 20 A

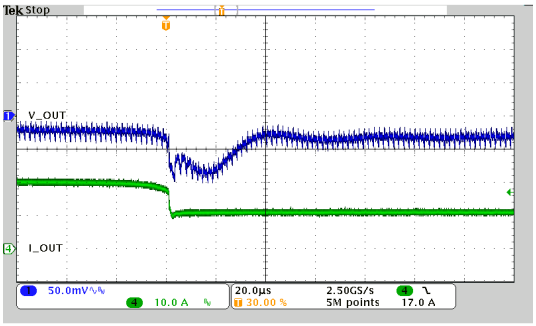
Figure 39. Shutdown from CNTL



Load Step 10A to 20A

V_{IN} = 12 V I_{OUT} = 20 A t_{RISE} = 2.0 µs

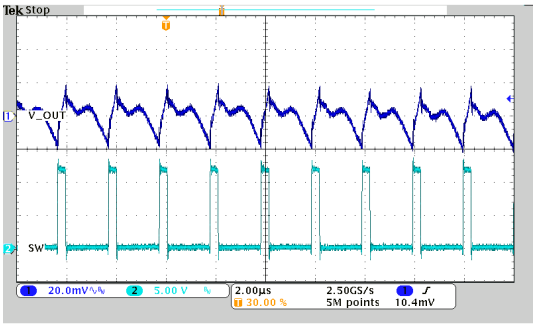
Figure 40. Load Transition 10-A to 20-A



Load Release 20At o 10A

V_{IN} = 12 V I_{OUT} = 20 A t_{FALL} = 2.0 µs

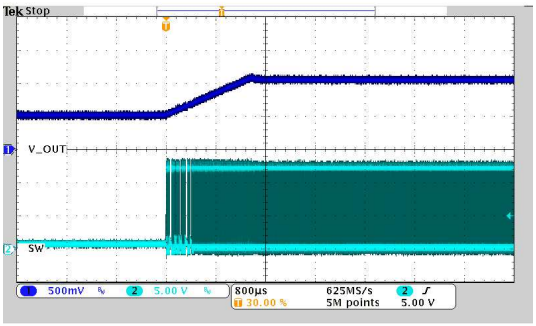
Figure 41. Load Transition 20-A to 10-A



DC Ripple

V_{IN} = 12 V I_{OUT} = 20 A

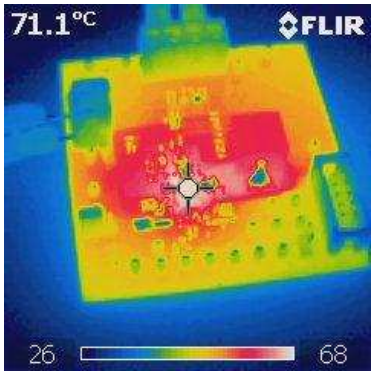
Figure 42. DC Ripple



50% PreBias Start No Load

V_{IN} = 12 V I_{OUT} = 0 A $V_{PRE-BIAS}$= 900 mV

Figure 43. 50% Pre-Biased Start-Up



Natural Convection

V_{IN} = 12 V I_{OUT} = 20 A f_{SW} = 500 kHz

Figure 44. Thermal Image

10 Power Supply Recommendations

These devices operate from an input voltage supply between 4.5 V and 18 V. These devices are not designed for split-rail operation. The VIN and VDD pins must be the same voltage for accurate high-side short circuit protection. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following layout recommendations will help guide you through a good layout of the TPS544B20 and TPS544C20 Devices. Figure 45 shows the recommended PCB layout configuration for additional reference.

- As with any switching regulator, there are several signal paths that conduct fast switching voltages or currents. Minimize the loop area formed by these paths and their bypass connections.
- Bypass the VIN pins to GND with a low-impedance path. Power-stage input bypass capacitors should be as close as physically possible to the VIN and GND pins. Additionally, a high-frequency bypass capacitor on the VIN pins can help to reduce switching spikes. See Figure 46 for placement recommendation.
- The AGNDSNS pin must be kelvin connected to the AGND pin, with a low-noise, low-impedance path to ensure accurate current monitoring. This connection must be made on an internal or bottom layer. It should not segment the thermal tab copper area. This connection serves as the only connection between AGND and GND for this device.
- Signal components should be terminated or bypassed to a separate analog ground (AGND) copper area, which is isolated from fast switching voltage and current paths. This copper area should not be connected to the thermal tab, or to an internal ground plane, and should be reserved for this regulator only.
- Minimize the SW copper area for best noise performance. Route sensitive traces away from SW and BOOT, as these nets contain fast switching voltages, and lend easily to capacitive coupling.
- Snubber component placement is critical to its effectiveness of ringing reduction. These components should be on the same layer as the devices, and be kept as close as possible to the SW and GND copper areas.
- Keep signal components and regulator bypass capacitors local to the device, and place them as close as possible to the pins to which they are connected. These components include the feedback resistors, frequency compensation, the R_{RT} resistor, ADDR0 and ADDR1 resistors, as well as bypass capacitors for BP3, BP6, VDD, and optionally BPEXT.
- The VIN and VDD pins must be the same voltage for accurate short circuit protection, but high frequency switching noise on the VDD pin can degrade performance. VDD should be connected to VIN through a trace from the input copper area. Optionally form a small low-pass R-C between VIN and VDD, with the VDD bypass capacitor (4.7 µF) and a 0-2 Ω resistor between VIN and VDD. See Figure 45.
- The VDD bypass capacitor can conduct high frequency switching currents into AGND. It is important to avoid sharing a path to AGND between the VDD capacitor and the FB to AGND (R_{bias}) resistor and COMP to AGND (C_{comp}) capacitor to avoid injecting noise into the regulation path.
- The TPS544B20 and TPS544C20 devices have several pins which require good local bypassing. Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground. Poor bypassing on VDD, BP3 and BP6 can degrade the performance of the regulator.
- Route the VOUTS+ and VOUTS– lines from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair. It is critical that these traces be kept away from switching or noisy areas which can add differential-mode noise.
- Routing of the temperature sensor traces is critical to the noise performance of temperature monitoring. Keep these traces away from switching areas or high current paths on the layout. It is also recommended to use a small 1-nF capacitor from TSNS to AGND to improve the noise performance of temperature readings.

11.2 Layout Example

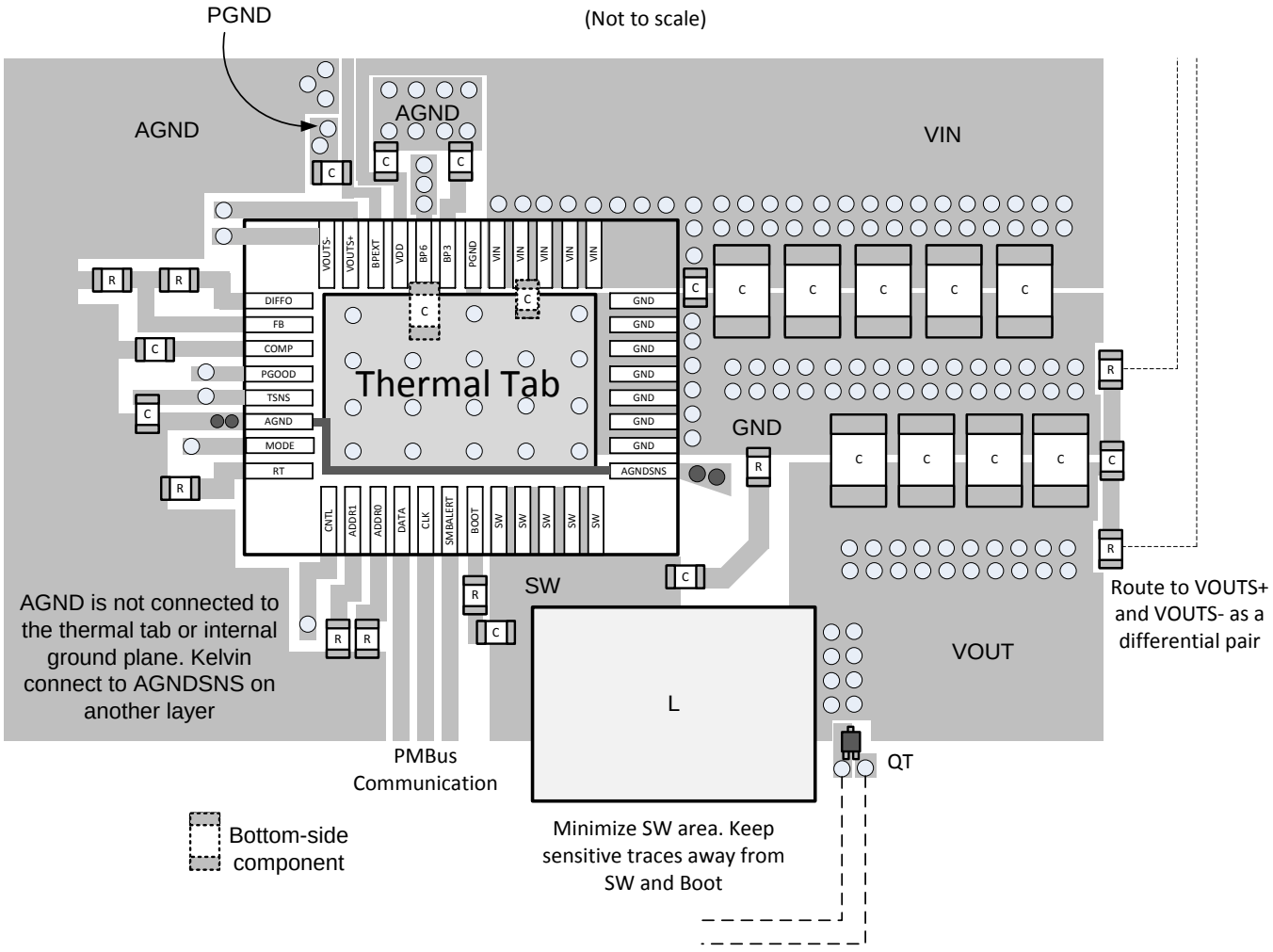


Figure 45. PCB Layout Recommendation

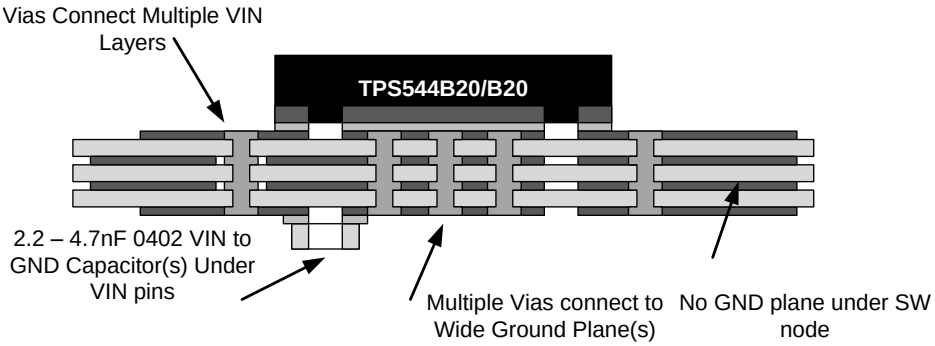


Figure 46. High-Frequency Bypass Capacitor Placement

Layout Example (continued)

11.2.1 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal tab with solder. Excessive heat during the reflow process can affect electrical performance. Figure 47 shows the recommended reflow oven thermal profile. Proper post-assembly cleaning is also critical to device performance. See SLUA271 for more information.

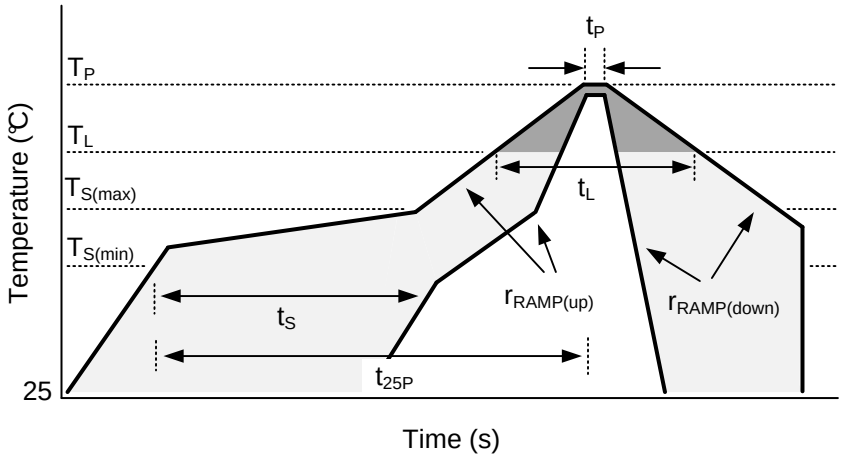


Figure 47. Recommended Reflow Oven Thermal Profile

Table 11. Recommended Thermal Profile Parameters

PARAMETER		MIN	TYP	MAX	UNIT
RAMP UP AND RAMP DOWN					
$r_{RAMP(up)}$	Average ramp-up rate, $T_{S(max)}$ to T_P			3	°C/s
$r_{RAMP(down)}$	Average ramp-down rate, T_P to $T_{S(max)}$			6	°C/s
PRE-HEAT					
T_S	Pre-Heat temperature	150		200	°C
t_S	Pre-heat time, $T_{S(min)}$ to $T_{S(max)}$	60		180	s
REFLOW					
T_L	Liquidus temperature		217		°C
T_P	Peak temperature			260	°C
t_L	Time maintained above liquidus temperature, T_L	60		150	s
t_P	Time maintained within 5 °C of peak temperature, T_P	20		40	s
t_{25P}	Total time from 25 °C to peak temperature, T_P			480	s

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 德州仪器 (TI) Fusion Digital Power™ 设计人员

TPS544B20 和 TPS544C20 器件由德州仪器 (TI) 数字电源设计工具 (Digital Power Designer) 完全支持。 Fusion Digital Power Designer 是一款图形用户界面 (GUI)，此界面可根据 PMBus 接口协议，经由德州仪器 (TI) USB 到通用输入输出接口 (GPIO) 适配器来配置和监视 TPS544B20 和 TPS544C20 器件。

单击此链接下载德州仪器 (TI) Fusion Digital Power Designer 软件包。

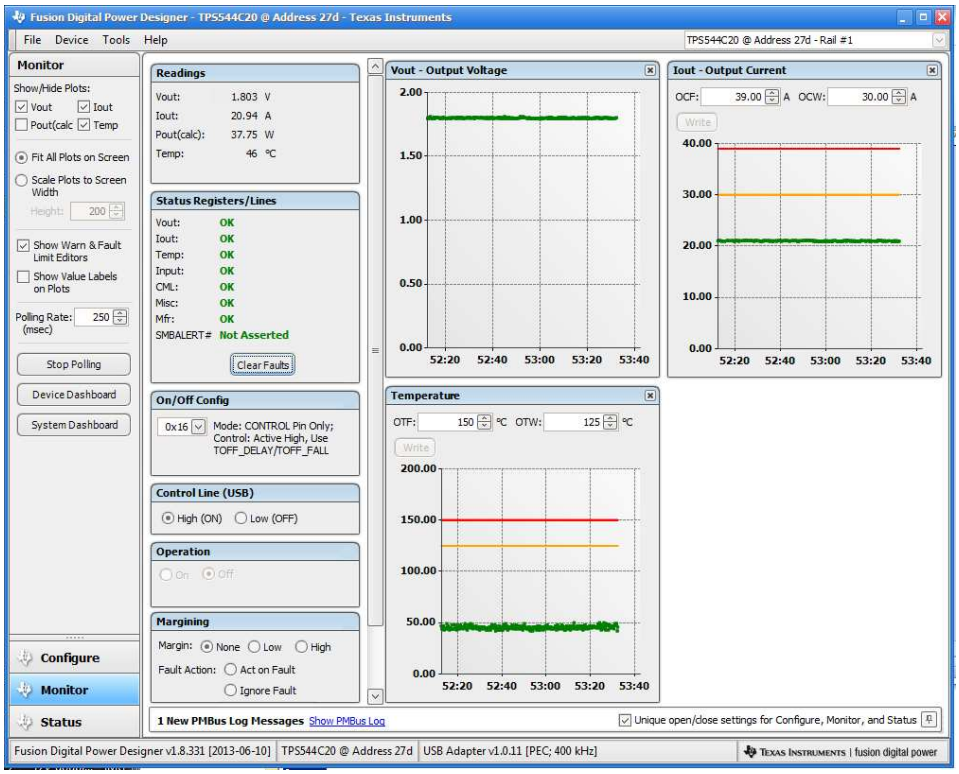


Figure 48. 使用 **Fusion Digital Power Designer** 进行器件监控

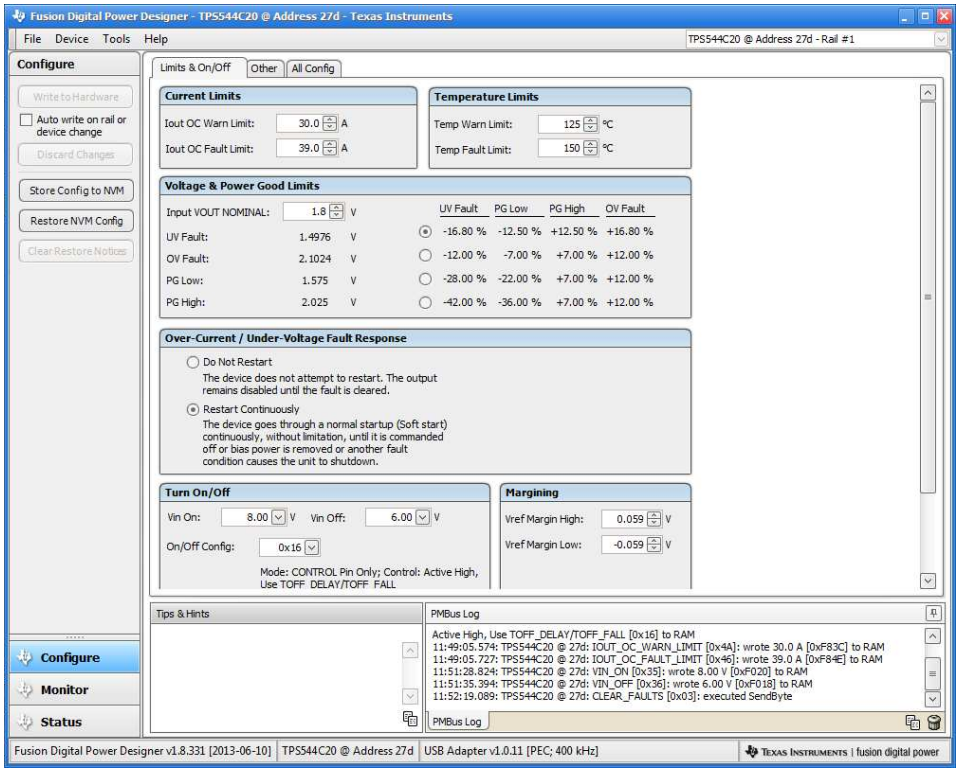


Figure 49. 使用 **Fusion Digital Power Designer** 进行器件配置

12.1.2 器件命名规则

总线占用 在共用通信总线上的长时间器件运行防止此共用总线上其他器件的正常通信时出现。

12.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

Table 12. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS544B20	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS544C20	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 Trademarks

SWIFT, NexFET, D-CAP, D-CAP2, Fusion Digital Power are trademarks of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS544B20RVFR	ACTIVE	LQFN-CLIP	RVF	40	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS544B20	Samples
TPS544B20RVFT	ACTIVE	LQFN-CLIP	RVF	40	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS544B20	Samples
TPS544C20RVFR	ACTIVE	LQFN-CLIP	RVF	40	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS544C20	Samples
TPS544C20RVFT	ACTIVE	LQFN-CLIP	RVF	40	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS544C20	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

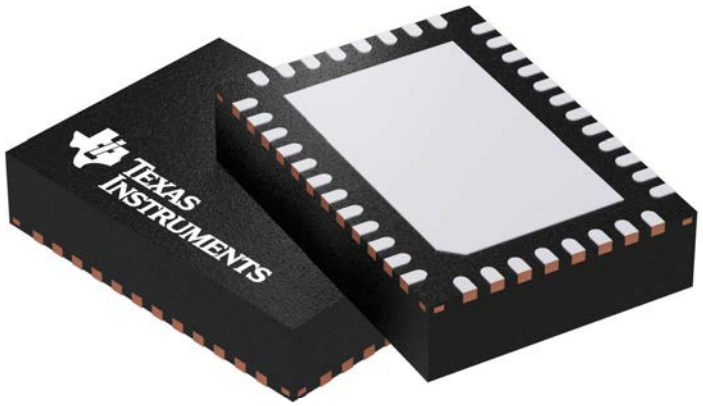
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RVF 40 LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



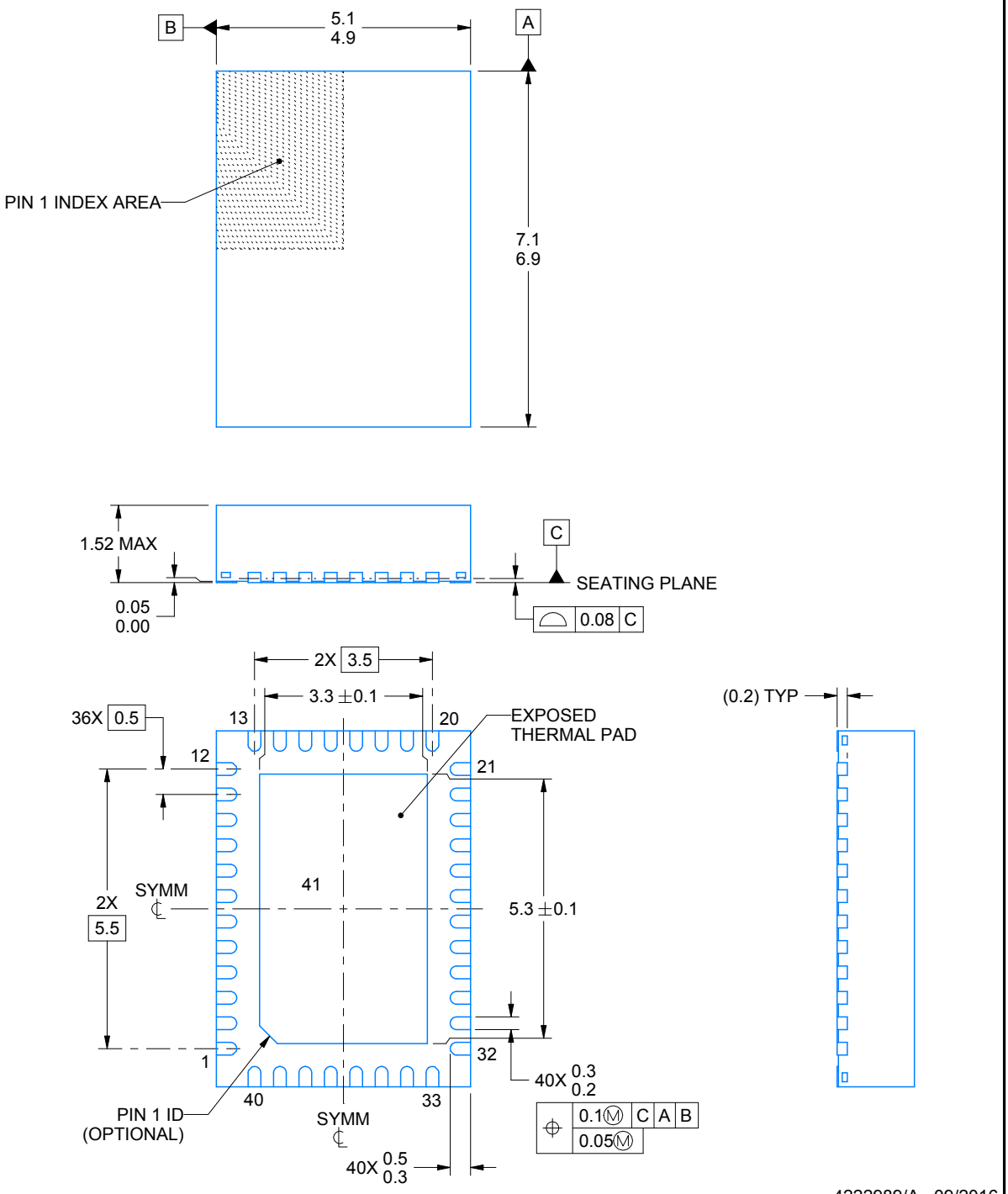
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RVF0040A

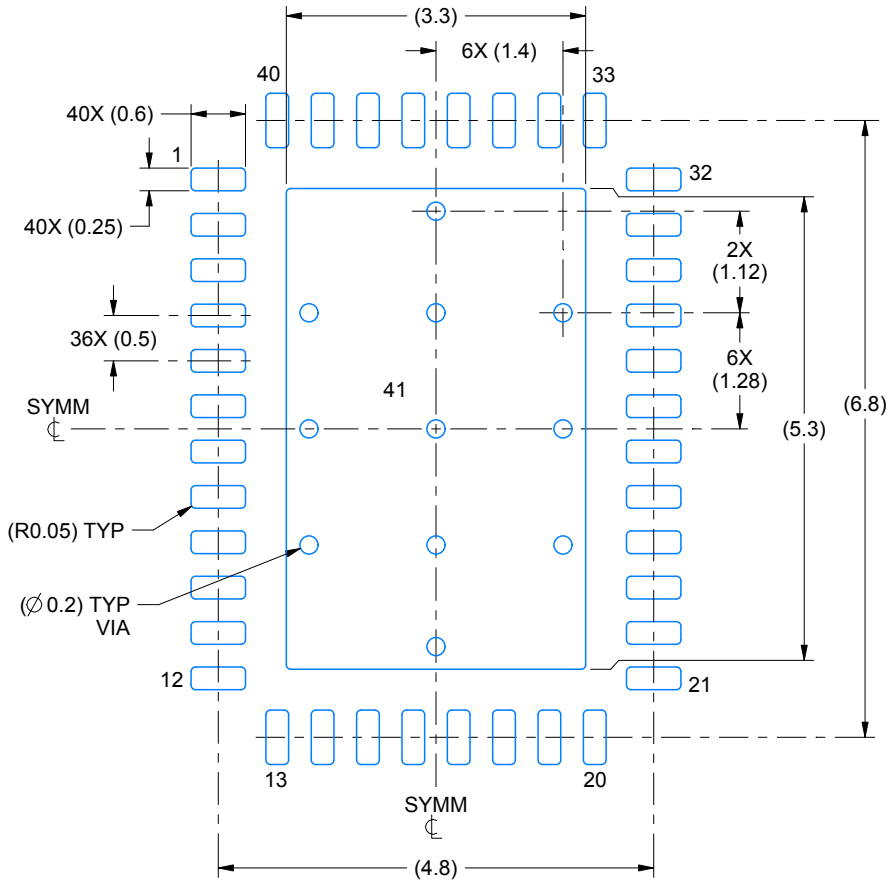
LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

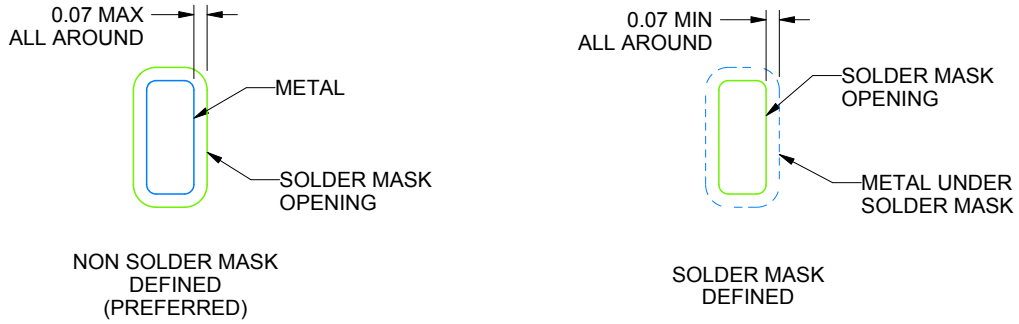


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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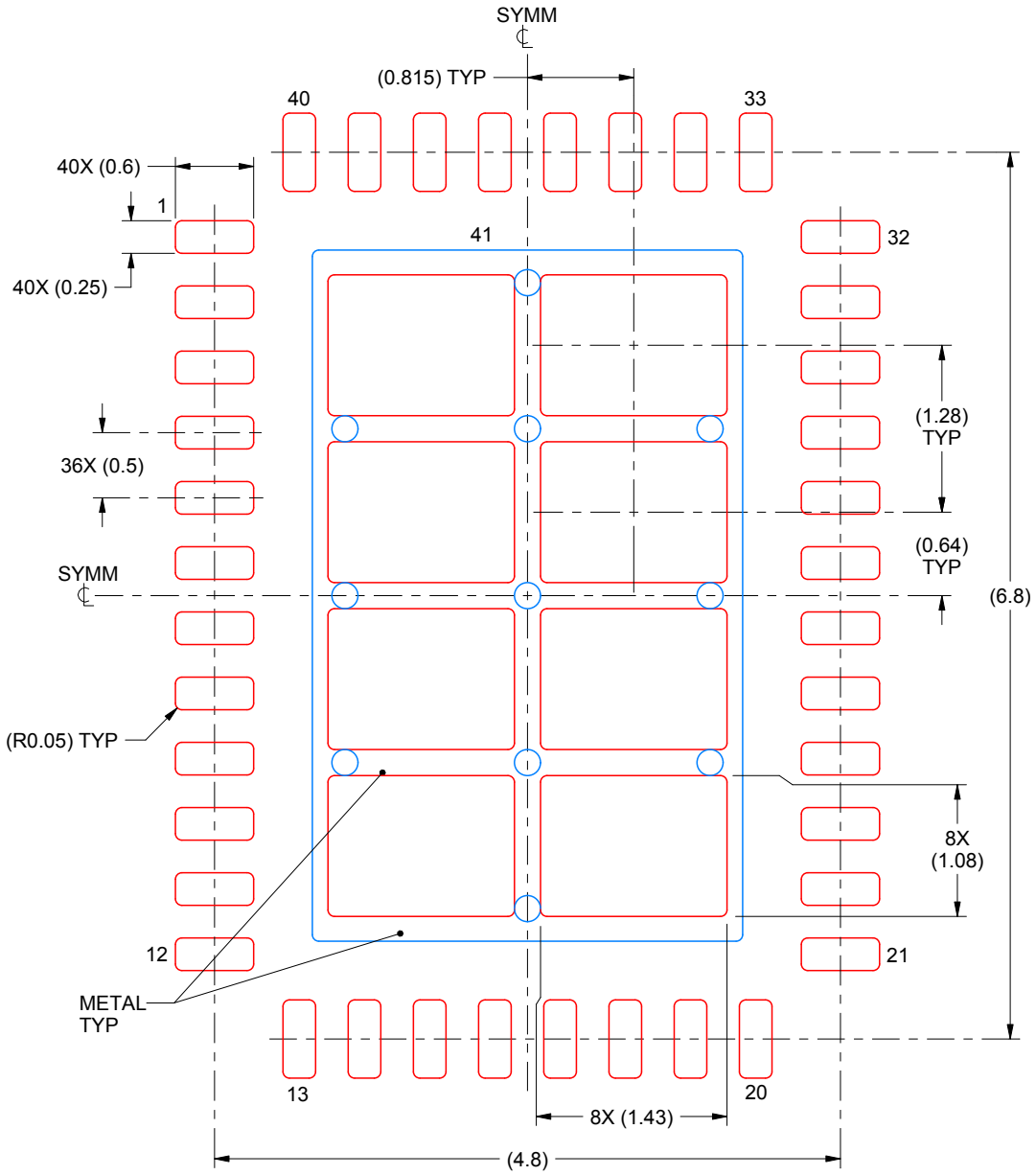
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

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设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

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