

# CC256x *Bluetooth*<sup>®</sup> Smart Ready 控制器

## Data Manual



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Products conform to specifications per the terms of the Texas  
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## Bluetooth® Smart Ready 控制器

### 1 特性

- 单片蓝牙 **Smart Ready** 解决方案集成了蓝牙基本速率 (**BR**) / 增强型数据速率 (**EDR**) / 低功耗 (**LE**) 并且与蓝牙 4.0 技术规范 (直到 **HCI** 层) 兼容
- **BR/EDR** 特性包括:
  - 多达七个激活器件
  - 分散网: 同时具有 **3** 个微微网, **1** 个作为主控网和 **2** 个作为受控网
  - 在同一个或者不同微微网上具有多达 **2** 个 同步面向 (**SCO**) 连接
  - 支持所有语音编码-连续可变斜率增量调制 (**CVSD**), **A** 规则,  $\mu$  规则和透明传输 (未编码)
- **LE** 特性包括:
  - 支持多达 **6** 个同步连接
  - 紧密耦合在一起的多重呼吸示例以实现最小功耗
  - 针对 **LE** 的独立缓冲可实现大量多重连接而又不会影响 **BR/EDR** 性能。
  - 包括针对 **BR/EDR** 和 **LE** 的内置共存和优先级处理
- 针对简便堆栈集成和不同的微处理器内验证的灵活性, 诸如 **Stellaris®** 和 **MSP430™**
- 针对低成本设计进行了高度优化
  - 单端 **50Ω RF** 接口
  - 封装尺寸: **76** 引脚, **0.6mm** 焊球间距, **8.10mm x 7.83mm** 多行四方扁平无引线 (**mrQFN**) 封装
- 业界最佳的蓝牙 (**RF**) 性能 (**TX** 电源, **RX** 灵敏度, 阻断)
  - 类 **1.5" TX** 功率高达 **+12dBm**
  - 内部温度检测和补偿以确保温度范围内 **RF** 性能的最小变化, 而无需外部校准
  - 已改进的 **AFH** 算法, 最大程度地缩短了采用时间
  - 提供更长的范围, 包括 **2** 倍于其它只支持 **BLE** 解决方案的范围
- 高级电源管理, 可延长电池寿命, 并易于设计:
  - 片载电源管理, 包括到电池的直接连接
  - 针对激活、待机和扫描蓝牙模式的低功耗
  - 针对页面和查询扫描的私有低功耗扫描使用其它解决方案
  - 的关断和睡眠模式以大大减少功耗
- 物理接口:
  - **H4 UART** 上的标准 **HCI**, 最大速率 **4Mbps**
  - 完全可编程数字 **PCM-I2S™** 编解码器接口
- **HCI** 蓝牙工具: **Windows PC** 应用程序以评估器件的 **RF** 性能



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## 1.1 说明

TICC256x 器件是一款完整的蓝牙 BR/EDR/LE/HCI 解决方案，此解决方案减轻了设计工作并可实现快速上市。基于 TI 的第七代蓝牙内核，器件实现了已经证明的解决方案，此解决方案支持蓝牙 4.0 双模式 (BR/EDR/LE) 协议。

TI 的电源管理硬件和软件算法大大节省了所有广泛使用的蓝牙 BR/EDR/LE 模式运行的能耗。

当与一个 MCU 器件耦合时，这个 HCI 器件为以下应用提供业界最佳的 RF 性能：

- 手机附件
- 体育和健身应用
- 无线音频解决方案
- 遥控
- 玩具

借助于传输功率和接收敏感度，相对于其它只支持 BLE 的解决方案，这个解决方案提供大约 2 倍的业界最佳范围。TI 提供的一款无版权软件蓝牙堆栈被与 TI MSP430 和 Stellaris MCU 预先集成在一起。TI 的合作伙伴 Stonestreet One 也通过 MFi 解决方案和其它 MCU 提供此堆栈 ([www.stonestreetone.com](http://www.stonestreetone.com))。目前支持的一些配置包括：

- 串行端口配置 (SPP)
- 高级音频分配配置 (A2DP)
- 几个 BLE 配置（根据支持的 MCU，这些配置会发生变化）

除了软件，这个解决方案包含一个使用低 BOM 成本的参考设计。与用于蓝牙的 TI 无线平台解决方案有关的更多信息，请参阅 TI 无线连接维基 (Wiki) 网站 ([www.ti.com/connectivitywiki](http://www.ti.com/connectivitywiki))。

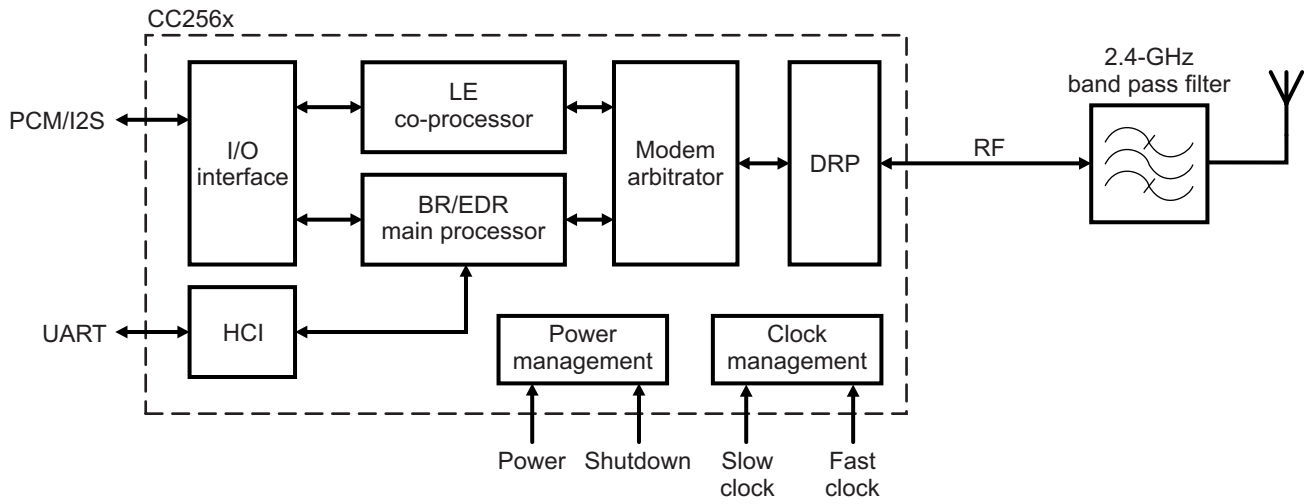
表 1-1 显示了 CC256x 系列产品成员。

表 1-1. CC256x 系列产品成员

器件	支持的技术			
	说明	BR/EDR	LE	ANT
CC2560A	蓝牙 4.0 (支持 EDR)	√		
CC2564	蓝牙 4.0+BLE <sup>(1)</sup>	√	√	√
	蓝牙 4.0+ANT <sup>(1)</sup>	√		√

(1) CC2569 器件不支持 LE 和 ANT 的同时运行。

图 1-1 显示了器件方框图。



Note: The CC2560A device does not contain the LE co-processor.

SWRS121-001

图 1-1. 功能方框图



## 2 BLUETOOTH

### 2.1 BR/EDR Features

### 2.2 Changes from *Bluetooth* v2.1 + EDR to v3.0 and v4.0

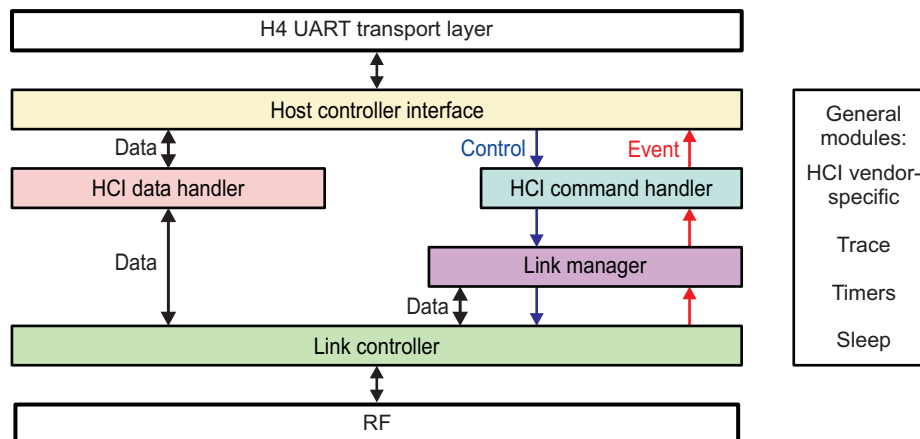
Several new features are introduced in the *Bluetooth* core specification v3.0 and v4.0. The major areas of improvement for the CC256x family (*Bluetooth* HCI controller) are:

- *Bluetooth* v3.0 introduces these features in BR/EDR:
  - Enhanced power control (EPC)
  - HCI Read Encryption Key Size command
- *Bluetooth* v4.0 introduces LE, including:
  - LE physical layer and link layer
  - Enhancements to HCI for LE
  - LE direct test mode
  - Advanced encryption standard (AES) encryption

Features are not deprecated in v3.0 and v4.0. For more information, see the *Bluetooth* SIG website at [www.bluetooth.org](http://www.bluetooth.org).

### 2.3 Transport Layers

Figure 2-1 shows the *Bluetooth* transport layers.



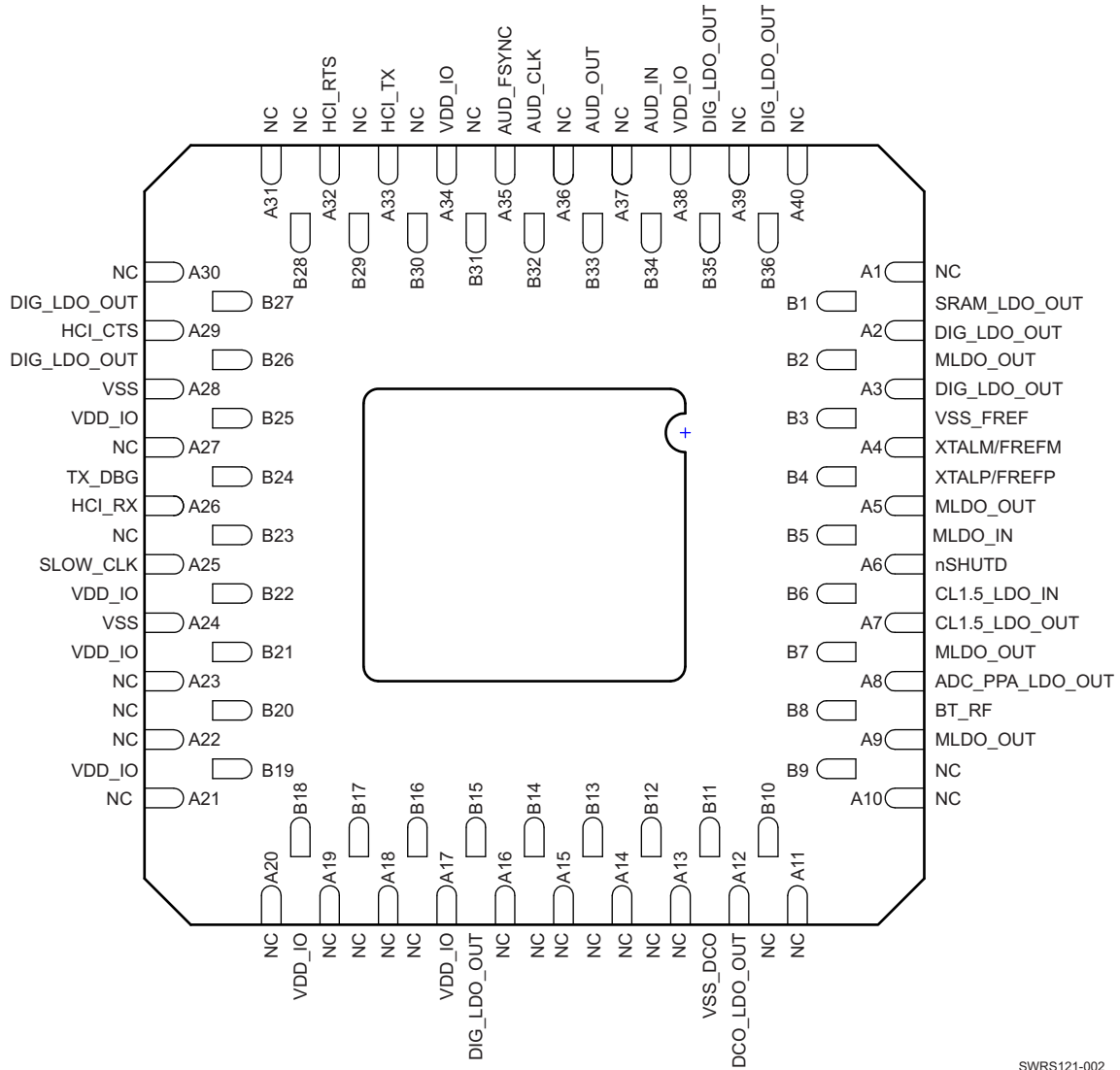
SWRS092-002

Figure 2-1. *Bluetooth* Transport Layers

### 3 DETAILED DESCRIPTION

#### 3.1 Pin Designation

Figure 3-1 shows the bottom view of the pin designations.



NOTE: NC = Not connected

SWRS121-002

Figure 3-1. Pin Designation (Bottom View)

### 3.2 Terminal Functions

Table 3-1 describes the terminal functions.

**Table 3-1. Device Pad Descriptions**

Name	No.	Pull at Reset	Def. Dir. <sup>(1)</sup>	I/O Type <sup>(2)</sup>	Description	
<b>I/O Signals</b>						
HCI_RX	A26	PU	I	8 mA	HCI universal asynchronous receiver/transmitter (UART) data receive	
HCI_TX	A33	PU	O	8 mA	HCI UART data transmit	
HCI_RTS	A32	PU	O	8 mA	HCI UART request-to-send The host is allowed to send data when HCI_RTS is low.	
HCI_CTS	A29	PU	I	8 mA	HCI UART clear-to-send The CC256x device is allowed to send data when HCI_CTS is low.	
AUD_FSYNC	A35	PD	I/O	4 mA	pulse-code modulation (PCM) frame-sync signal	Fail-safe
AUD_CLK	B32	PD	I/O	HY, 4 mA	PCM clock	Fail-safe
AUD_IN	B34	PD	I	4 mA	PCM data input	Fail-safe
AUD_OUT	B33	PD	O	4 mA	PCM data output	Fail-safe
TX_DBG	B24	PU	O	2 mA	TI internal debug messages. TI recommends leaving an internal test point.	
<b>Clock Signals</b>						
SLOW_CLK	A25		I		32.768-kHz clock in	Fail-safe
XTALP/FREFP	B4		I		Fast clock in analog (sine wave) Output terminal of fast-clock crystal	Fail-safe
XTALM/FREFM	A4		I		Fast clock in digital (square wave) Input terminal of fast-clock crystal	Fail-safe
<b>Analog Signals</b>						
BT_RF	B8		I/O		Bluetooth RF I/O	
nSHUTD	A6	PD	I		Shutdown input (active low)	
<b>Power and Ground Signals</b>						
VDD_IO	A17, A34, A38, B18, B19, B21, B22, B25		I		I/O power supply (1.8-V nominal)	
MLDO_IN	B5		I		Main LDO input Connect directly to battery	
MLDO_OUT	A5, A9, B2, B7		I/O		Main LDO output (1.8-V nominal)	
CL1.5_LDO_IN	B6		I		Power amplifier (PA) LDO input Connect directly to battery	
CL1.5_LDO_OUT	A7		O		PA LDO output	
DIG_LDO_OUT	A2, A3, B15, B26, B27, B35, B36		O		Digital LDO output QFN pin B26 or B27 must be shorted to other DIG_LDO_OUT pins on the PCB.	
SRAM_LDO_OUT	B1		O		SRAM LDO output	
DCO_LDO_OUT	A12		O		DCO LDO output	

(1) I = input; O = output; I/O = bidirectional

(2) I/O Type: Digital I/O cells. HY = input hysteresis, current = typical output current

**Table 3-1. Device Pad Descriptions (continued)**

Name	No.	Pull at Reset	Def. Dir. <sup>(1)</sup>	I/O Type <sup>(2)</sup>	Description
ADC_PPA_LDO_OUT	A8		O		ADC/PPA LDO output
VSS	A24, A28		I		Ground
VSS_DCO	B11		I		DCO ground
VSS_FREF	B3		I		Fast clock ground
<b>No Connect</b>					
NC	A1				Not connected
NC	A10				Not connected
NC	A11				Not connected
NC	A14				Not connected
NC	A18				Not connected
NC	A19				Not connected
NC	A20				Not connected
NC	A21				Not connected
NC	A22				Not connected
NC	A23				Not connected
NC	A27				Not connected
NC	A30				Not connected
NC	A31				Not connected
NC	A40				Not connected
NC	B9				Not connected
NC	B10				Not connected
NC	B16				Not connected
NC	B17				Not connected
NC	B20				Not connected
NC	B23				Not connected
NC	A13		O		TI internal use
NC	A15		O		TI internal use
NC	A16		I/O		TI internal use
NC	A36		I/O		TI internal use
NC	A37		I/O		TI internal use
NC	A39		I/O		TI internal use
NC	B12		I		TI internal use
NC	B13		I		TI internal use
NC	B14		O		TI internal use
NC	B29		O		TI internal use
NC	B30		I/O		TI internal use
NC	B31		I		TI internal use
NC	B28		I		TI internal use

### 3.3 Device Power Supply

The CC256x power-management hardware and software algorithms provide significant power savings, which is a critical parameter in a microcontroller-based system.

The power-management module is optimized for drawing very low currents.

#### 3.3.1 Power Sources

The CC256x device requires two power sources:

- VDD\_IN: Main power supply for the *Bluetooth* core
- VDD\_IO: Power source for the 1.8-V I/O ring

The device includes several on-chip voltage regulators for increased noise immunity and can be connected directly to the battery.

#### 3.3.2 Device Power-Up and Power-Down Sequencing

The device includes these power-up requirements (see also [Figure 3-2](#)):

- nSHUTD must be low. VDD\_IN and VDD\_IO are don't-care when nSHUTD is low. However, signals are not allowed on the I/O pins if I/O power is not supplied, because the I/Os are not fail-safe. Exceptions are CLK\_REQ\_OUT, SLOW\_CLK\_IN, and AUD\_xxx, which are fail-safe and can tolerate external voltages with no VDD\_IO and VDD\_IN.
- VDD\_IO and VDD\_IN must be stable before releasing nSHUTD.
- The fast clock must be stable for a maximum of 20 ms after nSHUTD goes high.
- The slow clock must be stable within 2 ms of nSHUTD going high.

The device indicates that the power-up sequence is complete by asserting RTS low, which occurs up to 100 ms after nSHUTD goes high. If RTS does not go low, the device is not powered-up. In this case, ensure that the sequence and requirements are met.

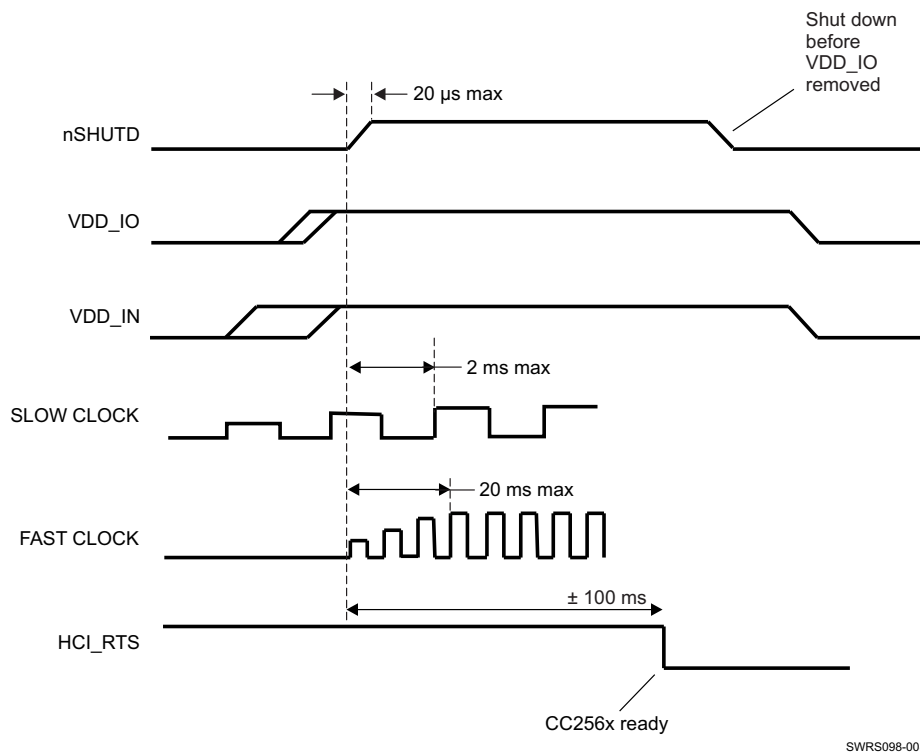


Figure 3-2. Power-Up and Power-Down Sequence

### 3.3.3 Power Supplies and Shutdown—Static States

The nSHUTD signal puts the device in ultra-low power mode and also performs an internal reset to the device. The rise time for nSHUTD must not exceed 20  $\mu$ s, and nSHUTD must be low for a minimum of 5 ms.

To prevent conflicts with external signals, all I/O pins are set to the high-impedance state during shutdown and power up of the device. The internal pull resistors are enabled on each I/O pin, as described in [Table 3-1](#).

[Table 3-2](#) describes the static operation states.

**Table 3-2. Power Modes**

	VDD_IN <sup>(1)</sup>	VDD_IO <sup>(1)</sup>	nSHUTD <sup>(1)</sup>	PM_MODE	Comments
1	None	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on non fail-safe pins.
2	None	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on non fail-safe pins.
3	None	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
4	None	Present	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
5	Present	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
6	Present	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
7	Present	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
8	Present	Present	Deasserted	Active	See <a href="#">Section 3.3.4</a> , <i>I/O States In Various Power Modes</i> .

- (1) The terms *None* or *Asserted* can imply any of the following conditions: directly pulled to ground or driven low, pulled to ground through a pulldown resistor, or left NC or floating (high-impedance output stage).

### 3.3.4 I/O States In Various Power Modes

#### CAUTION

Some device I/Os are not fail-safe (see [Table 3-1](#)). Fail-safe means that the pins do not draw current from an external voltage applied to the pin when I/O power is not supplied to the device. External voltages are not allowed on these I/O pins when the I/O supply voltage is not supplied because of possible damage to the device.

I/O Name	Shut Down <sup>(1)</sup>		Default Active <sup>(1)</sup>		Deep Sleep <sup>(1) (2)</sup>	
	I/O State	Pull	I/O State	Pull	I/O State	Pull
HCI_RX	Z	PU	I	PU	I	<sup>(3)</sup>
HCI_TX	Z	PU	O-H	—	O	—
HCI_RTS	Z	PU	O-H	—	O	—
HCI_CTS	Z	PU	I	PU	I	<sup>(3)</sup>
AUD_CLK	Z	PD	I	PD	I	PD
AUD_FSYNC	Z	PD	I	PD	I	PD
AUD_IN	Z	PD	I	PD	I	PD
AUD_OUT	Z	PD	Z	PD	Z	PD
CLK_REQ_OUT	Z	PD	O-H	PD	O-L	PD
TX_DBG	Z	PU	O	—		

(1) I = input, O = output, Z = Hi-Z, — = no pull, PU = pullup, PD = pulldown, H = high, L = low

(2) Shown only if different from active. Can be changed by vendor-specific (VS) command.

(3) PU or no pull; depends on the setting in the init script.

## 3.4 Clock Inputs

### 3.4.1 Slow Clock

An external source must supply the slow clock and connect to the SLOW\_CLK\_IN pin. The source must be a digital signal in the range of 0 to 1.8 V.

The accuracy of the slow clock frequency must be 32.768 kHz  $\pm$ 250 ppm for *Bluetooth* use (as specified in the *Bluetooth* specification).

The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

### 3.4.2 Fast Clock Using External Clock Source

An external clock source is fed to an internal pulse-shaping cell to provide the fast clock signal for the device. The device incorporates an internal, automatic clock-scheme detection mechanism that automatically detects the fast-clock scheme used and configures the F<sub>REF</sub> cell accordingly. This ensures that the electrical characteristics (loading) of the fast-clock input remain static regardless of the scheme used and eliminates any power-consumption penalty-versus-scheme used.

The following paragraphs describe the requirements for fast clock use.

The frequency variation of the fast-clock source must not exceed  $\pm$ 20 ppm (as defined by the *Bluetooth* specification).

The external clock can be AC- or DC-coupled, sine or square wave.

#### 3.4.2.1 External F<sub>REF</sub> DC-Coupled

Figure 3-3 and Figure 3-4 show the clock configuration when using a square wave, DC-coupled external source for the fast clock input.

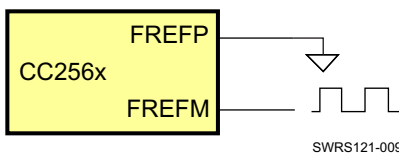


Figure 3-3. Clock Configuration (Square Wave, DC-Coupled)

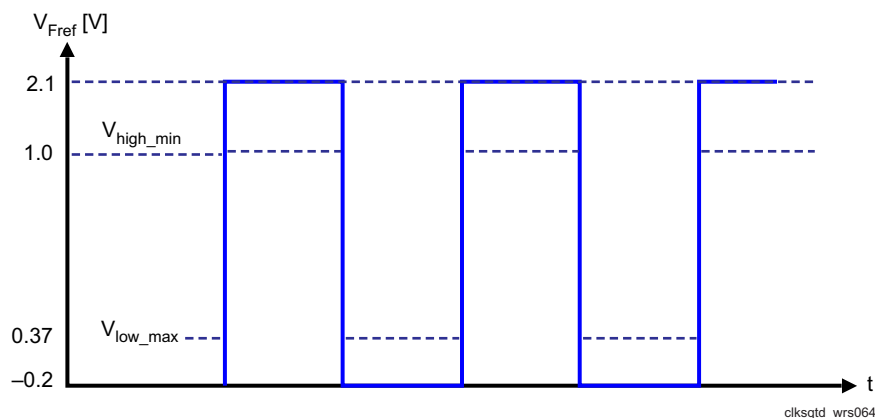


Figure 3-4. External Fast Clock (Square Wave, DC-Coupled)

Figure 3-5 and Figure 3-6 show the clock configuration when using a sine wave, DC-coupled external source for the fast clock input.



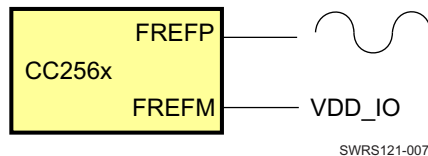


Figure 3-5. Clock Configuration (Sine Wave, DC-Coupled)

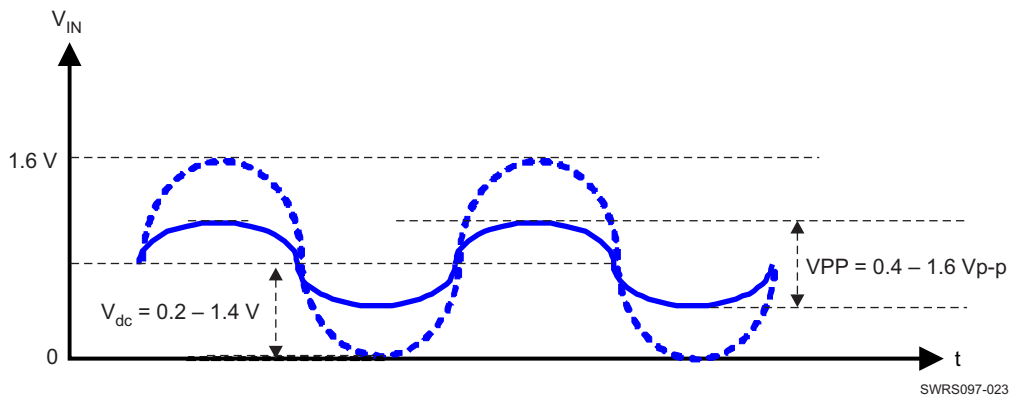


Figure 3-6. External Fast Clock (Sine Wave, DC-Coupled)

### 3.4.2.2 External F<sub>REF</sub> Sine Wave, AC-Coupled

Figure 3-7 shows the configuration when using a sine wave, AC-coupled external source for the fast-clock input.

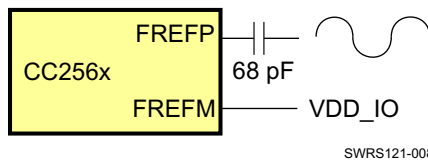
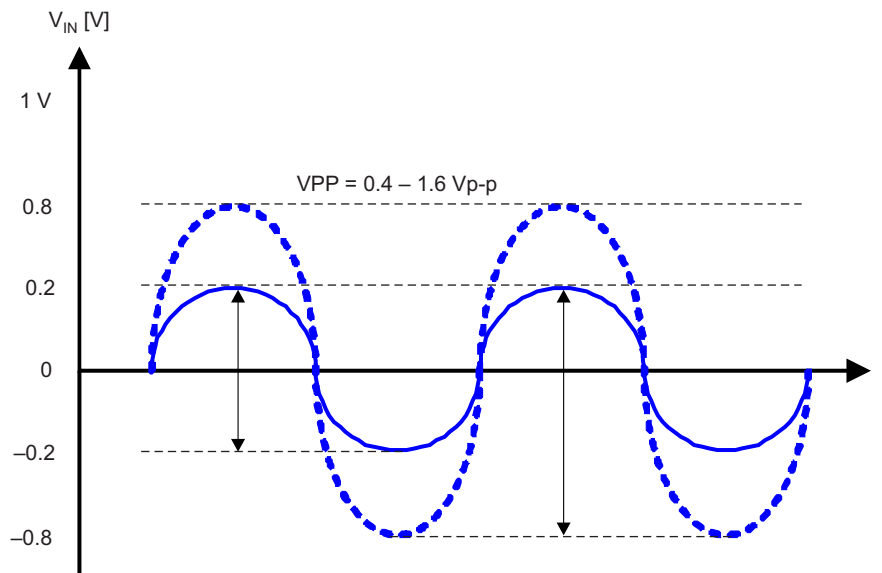


Figure 3-7. Clock Configuration (Sine Wave, AC-Coupled)



SWRS097-022

**Figure 3-8. External Fast Clock (Sine Wave, AC-Coupled)**

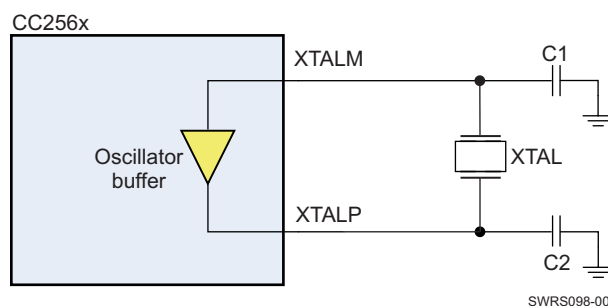
In cases where the input amplitude is greater than 1.6 V<sub>p-p</sub>, the amplitude can be reduced to within limits. Using a small series capacitor forms a voltage divider with the internal input capacitance of approximately 2 pF to provide the required amplitude at the device input.

**3.4.2.3 Fast Clock Using External Crystal**

The CC256x device incorporates an internal crystal oscillator buffer to support a crystal-based fast-clock scheme. The supported crystal frequency is 26 MHz.

The frequency accuracy of the fast clock source must not exceed ±20 ppm (including the accuracy of the capacitors, as specified in the *Bluetooth* specification).

Figure 3-9 shows the recommended fast-clock circuitry.



SWRS098-003

**Figure 3-9. Fast-Clock Crystal Circuit**

Table 3-3 lists component values for the fast-clock crystal circuit.

**Table 3-3. Fast-Clock Crystal Circuit Component Values**

FREQ (MHz)	C1 (pF) <sup>(1)</sup>	C2 (pF) <sup>(1)</sup>
26	15 pF typ	15 pF typ

- (1) To achieve the required accuracy, values for C1 and C2 must be taken from the crystal manufacturer's data sheet and layout considerations.

### 3.5 Functional Blocks

The CC256x architecture comprises a DRP and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMI<sup>®</sup> core. The device includes several on-chip peripherals to enable easy communication with a host system and the *Bluetooth* BR/EDR/LE core.

#### 3.5.1 DRP

The device is the third generation of TI *Bluetooth* single-chip devices using DRP architecture. Modifications and new features added to the DRP further improve radio performance.

Figure 3-10 shows the DRP block diagram.

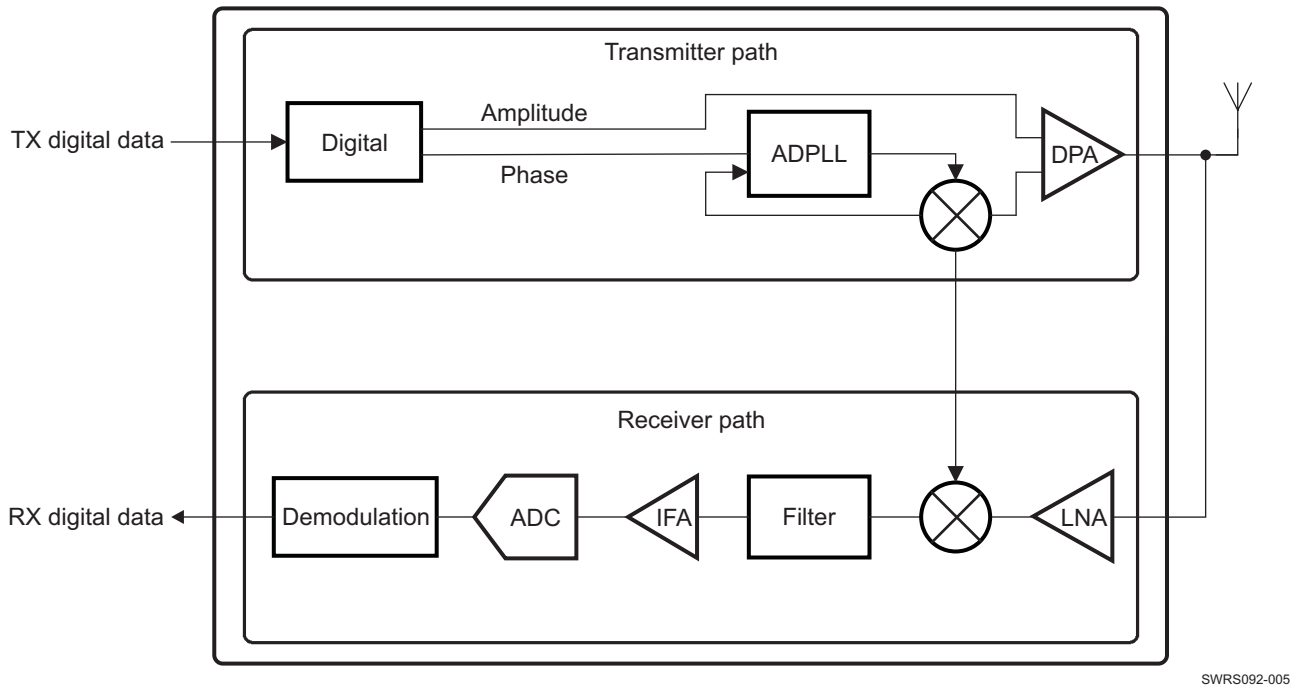


Figure 3-10. DRP Block Diagram

##### 3.5.1.1 Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. The signal received from the external antenna is input to a single-ended LNA (low-noise amplifier) and passed to a mixer that downconverts the signal to IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta analog-to-digital converter (ADC) and further processed to reduce the interference level.

The demodulator digitally downconverts the signal to zero-IF and recovers the data stream using an adaptive-decision mechanism. The demodulator includes EDR processing with:

- State-of-the-art performance
- A maximum-likelihood sequence estimator (MLSE) to improve the performance of basic-rate GFSK sensitivity
- Adaptive equalization to enhance EDR modulation

New features include:

- LNA input range narrowed to increase blocking performance
- Active spur cancellation to increase robustness to spurs

### 3.5.1.2 Transmitter

The transmitter is an all-digital, sigma-delta phase-locked loop (ADPLL) based with a digitally controlled oscillator (DCO) at 2.4 GHz as the RF frequency clock. The transmitter direct modulates the digital PLL. The power amplifier is also digitally controlled. The transmitter uses the polar-modulation technique. While the phase-modulated control word is fed to the ADPLL, the amplitude-modulated controlled word is fed to the class-E amplifier to generate a *Bluetooth* standard-compliant RF signal.

New features include:

- Improved TX output power
- LMS algorithm to improve the differential error vector magnitude (DEVm)

### 3.5.2 Host Controller Interface

The CC256x device incorporates one UART module dedicated to the HCI transport layer. The HCI interface transports commands, events, and asynchronous connection-oriented link (ACL) between the device and the host using HCI data packets.

The UART module supports the H4 (4-wire) protocol with a maximum baud rate of 4 Mbps for all fast-clock frequencies.

After power up, the baud rate is set for 115.2 kbps, regardless of the fast-clock frequency.

The baud rate can thereafter be changed with a VS command. The device responds with a Command Complete event (still at 115.2 kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS and RTS hardware flow control

Table 3-4 lists the UART module default settings.

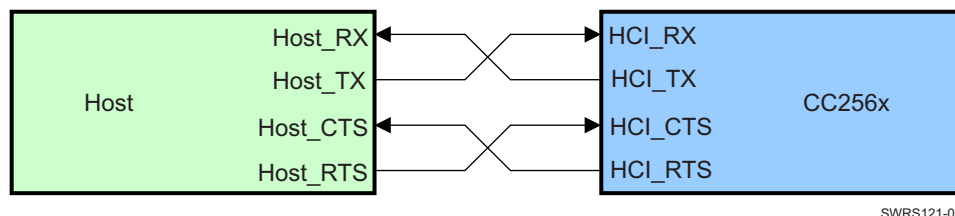
**Table 3-4. UART Default Settings**

Parameter	Value
Bit rate	115.2 kbps
Data length	8 bits
Stop-bit	1
Parity	None

#### 3.5.2.1 UART 4-Wire Interface—H4

The interface includes four signals: TX, RX, CTS, and RTS. Flow control between the host and the CC256x device is byte-wise by hardware.

Figure 3-11 shows how the device obtains flow control.



**Figure 3-11. HCI UART Connection**

When the UART RX buffer of the CC256x device passes the flow control threshold, it sets the UART\_RTS signal high to stop transmission from the host.

When the UART\_CTS signal is set high, the CC256x device stops its transmission on the interface. If HCI\_CTS is set high while transmitting a byte, the CC256x device finishes transmitting the byte and stops the transmission.

### 3.5.2.2 eHCILL—4-Wire Power-Management Protocol

The CC256x device includes a mechanism that handles the transition between operating mode and deep-sleep low-power mode. The protocol occurs through the UART and is known as the enhanced HCI low level (eHCILL) power-management protocol.

### 3.5.3 Digital Codec Interface

The codec interface is a fully programmable port to support seamless interfacing with different PCM and Inter-IC Sound (I2S) codec devices. The interface includes the following features:

- Two voice channels
- Master and slave modes
- All voice coding schemes defined by the *Bluetooth* specification: linear, A-Law, and  $\mu$ -Law
- Long and short frames
- Different data sizes, order, and positions
- High-rate interface for EDR connection
- High flexibility to support a variety of codecs
- Bus sharing: Data\_Out is in Hi-Z mode when the interface is not transmitting voice data.

#### 3.5.3.1 Hardware Interface

The interface includes four signals:

- Clock: configurable direction (input or output)
- Frame\_Sync and Word\_Sync: configurable direction (input or output)
- Data\_In: input
- Data\_Out: output or 3-state

The CC256x device can be master of the interface when generating the clock and the frame-sync signals or the slave when receiving these two signals.

For slave mode, clock input frequencies of up to 15 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the CC256x device can generate any clock frequency between 64 kHz and 4.096 MHz.

#### 3.5.3.2 I2S

When the codec interface is configured to support the I2S protocol, these settings are recommended:

- Bidirectional, full-duplex interface
- Two time slots per frame: time slot-0 for the left channel audio data; and time slot-1 for the right channel audio data
- Each time slot is configurable up to 40 serial clock cycles long, and the frame is configurable up to 80 serial clock cycles long.

#### 3.5.3.3 Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits in 1-bit increments when working with 2 channels, or up to 640 bits when working with 1 channel. The data length can be set independently for each channel.

- The data position within a frame is also configurable within 1 clock (bit) resolution and can be set independently (relative to the edge of the Frame\_Sync signal) for each channel.
- The Data\_In and Data\_Out bit order can be configured independently. For example; Data\_In can start with the most-significant bit (MSB); Data\_Out can start with the least-significant bit (LSB). Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.
- It is not necessary for Data\_In and Data\_Out to be the same length.
- The Data\_Out line is configured to Hi-Z output between data words. Data\_Out can also be set for permanent Hi-Z, regardless of data out. This allows the CC256x device to be a bus slave in a multislave PCM environment. At power up, Data\_Out is configured as Hi-Z.

### 3.5.3.4 Frame Idle Period

The codec interface handles frame idle periods, in which the clock pauses and becomes 0 at the end of the frame, after all data are transferred.

The CC256x device supports frame idle periods both as master and slave of the codec bus.

When the CC256x device is master of the interface, the frame idle period is configurable. There are two configurable parameters:

- Clk\_Idle\_Start: indicates the number of clock cycles from the beginning of the frame to the beginning of the idle period. After Clk\_Idle\_Start clock cycles, the clock becomes 0.
- Clk\_Idle\_End: indicates the time from the beginning of the frame to the end of the idle period. The time is given in multiples of clock periods.

The delta between Clk\_Idle\_Start and Clk\_Idle\_End is the clock idle period.

For example, for clock rate = 1 MHz, frame sync period = 10 kHz, Clk\_Idle\_Start = 60, Clk\_Idle\_End = 90.

Between both frame-sync signals there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts  $90 - 60 = 30$  clock cycles. This means that the idle period ends  $100 - 90 = 10$  clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period.

Figure 3-12 shows the frame idle timing.

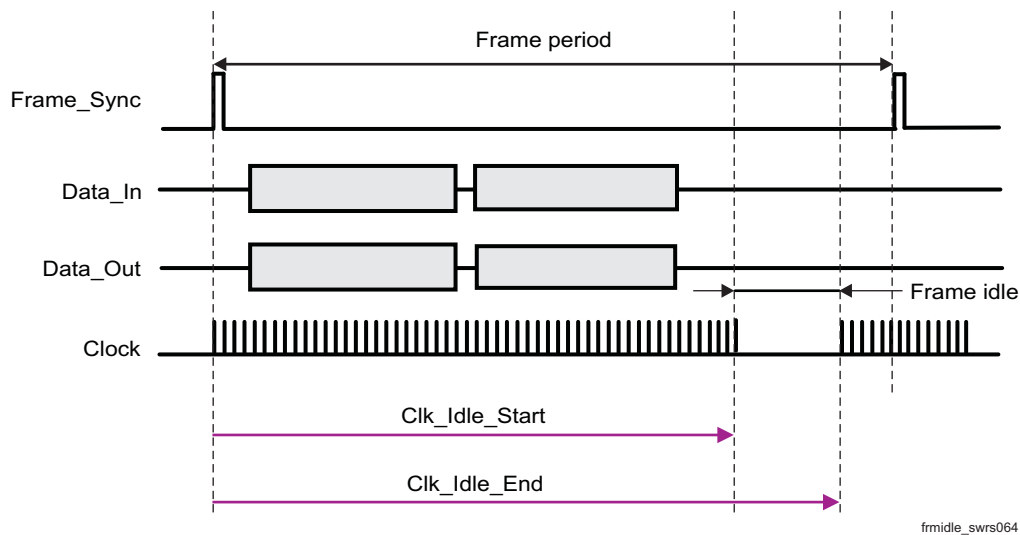


Figure 3-12. Frame Idle Period

3.5.3.5 Clock-Edge Operation

The codec interface of the CC256x device can work on the rising or the falling edge of the clock and can sample the frame-sync signal and the data at inversed polarity.

Figure 3-13 shows the operation of a falling-edge-clock type of codec. The codec is the master of the bus. The frame-sync signal is updated (by the codec) on the falling edge of the clock and is therefore sampled (by the CC256x device) on the next rising clock. The data from the codec is sampled (by the CC256x device) on the falling edge of the clock.

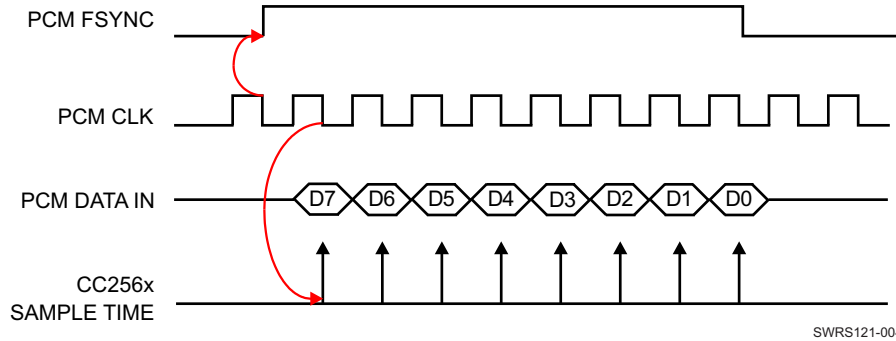


Figure 3-13. Negative Clock Edge Operation

3.5.3.6 Two-Channel Bus Example

Figure 3-14 shows a 2-channel bus in which the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for frame timer.)

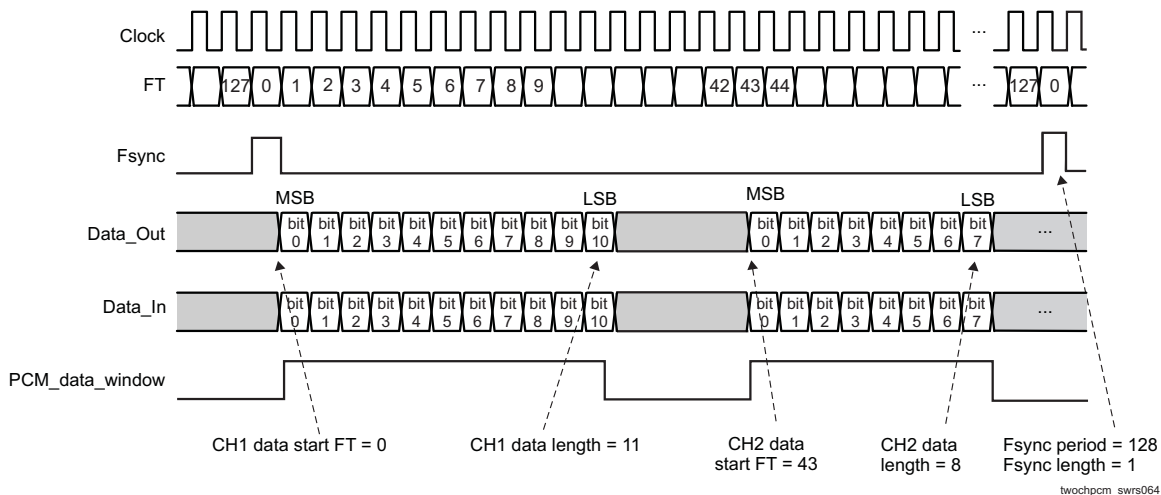


Figure 3-14. Two-Channel Bus Timing

3.5.3.7 Improved Algorithm For Lost Packets

The CC256x device features an improved algorithm to improve voice quality when received voice data packets are lost. There are two options:

- Repeat the last sample: possible only for sample sizes up to 24 bits. For sample sizes larger than 24 bits, the last byte is repeated.
- Repeat a configurable sample of 8 to 24 bits (depending on the real sample size) to simulate silence (or anything else) in the bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.



### 3.5.3.8 *Bluetooth* and Codec Clock Mismatch Handling

In *Bluetooth* RX, the CC256x device receives RF voice packets and writes them to the codec interface. If the CC256x device receives data faster than the codec interface output allows, an overflow occurs. In this case, the *Bluetooth* has two possible behavior modes:

- Allow overflow: if overflow is allowed, the *Bluetooth* continues receiving data and overwrites any data not yet sent to the codec.
- Do not allow overflow: if overflow is not allowed, RF voice packets received when the buffer is full are discarded.

## 4 DEVICE SPECIFICATIONS

Unless otherwise indicated, all measurements are taken at the device pins of the TI test evaluation board (EVB).

All specifications are over process, voltage and temperature, unless otherwise indicated.

### 4.1 General Device Requirements and Operation

#### 4.1.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

#### NOTE

Unless otherwise indicated, all parameters are measured as follows:

$$VDD\_IN = 3.6\text{ V}, VDD\_IO = 1.8\text{ V}$$

See <sup>(1)</sup>		Value	Unit
Ratings over operating free-air temperature range			
VDD_IN	Supply voltage range	-0.5 to 4.8	V <sup>(2)</sup>
VDDIO_1.8V		-0.5 to 2.145	V
	Input voltage to analog pins <sup>(3)</sup>	-0.5 to 2.1	V
	Input voltage to all other pins	-0.5 to (VDD_IO + 0.5)	V
	Operating ambient temperature range <sup>(4)</sup>	-40 to 85	°C
	Storage temperature range	-55 to 125	°C
	Bluetooth RF inputs	10	dBm
ESD stress voltage <sup>(5)</sup>	Human body model (HBM) <sup>(6)</sup>	Device	V
	Charged device model (CDM) <sup>(7)</sup>	Device	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum allowed depends on accumulated time at that voltage: VDD\_IN is defined in [Section 5, Reference Design for Power and Radio Connections](#).
- (3) Analog pins: BT\_RF, XTALP, and XTALM
- (4) The reference design supports a temperature range of -20°C to 70°C because of the operating conditions of the crystal.
- (5) ESD measures device sensitivity and immunity to damage caused by electrostatic discharges into the device.
- (6) The level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible, if necessary precautions are taken. Pins listed as 1000 V can actually have higher performance.
- (7) The level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible, if necessary precautions are taken. Pins listed as 250 V can actually have higher performance.

## 4.1.2 Recommended Operating Conditions

Rating	Condition	Sym	Min	Max	Unit
Power supply voltage		VDD_IN	2.2	4.8	V
I/O power supply voltage		VDD_IO	1.62	1.92	V
High-level input voltage	Default	V <sub>IH</sub>	0.65 x VDD_IO	VDD_IO	V
Low-level input voltage	Default	V <sub>IL</sub>	0	0.35 x VDD_IO	V
I/O input rise and all times, 10% to 90% — asynchronous mode		t <sub>r</sub> and t <sub>f</sub>	1	10	ns
I/O input rise and fall times, 10% to 90% — synchronous mode (PCM)			1	2.5	ns
Voltage dips on VDD_IN (V <sub>BAT</sub> ) duration = 577 μs to 2.31 ms, period = 4.6 ms				400	mV
Maximum ambient operating temperature <sup>(1) (2)</sup>			–40	85	°C

- (1) The device can be reliably operated for 7 years at T<sub>ambient</sub> of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).
- (2) A crystal-based solution is limited by the temperature range required of the crystal to meet 20 ppm.

## 4.1.3 Current Consumption

### 4.1.3.1 Static Current Consumption

Characteristics	Min 25°C	Typ 25°C	Max 25°C	Min –40°C	Typ –40°C	Max –40°C	Min 85°C	Typ 85°C	Max 85°C	Unit
Current consumption in shut-down mode <sup>(1)</sup>		1	3						7	μA
Current consumption in deep-sleep mode <sup>(2)</sup>		40	105							μA
Total I/O current consumption for active mode			1			1			1	mA

- (1) V<sub>BAT</sub> + V<sub>IO</sub>
- (2) V<sub>BAT</sub> + V<sub>IO</sub> + V<sub>SD</sub> (shutdown)

### 4.1.3.2 Dynamic Current Consumption

#### 4.1.3.2.1 Current Consumption for Different Bluetooth BR/EDR Scenarios

Conditions: VDD\_IN = 3.6 V, 25°C, 26-MHz fast clock, nominal unit, 4 dBm output power

Mode Description	Master and Slave	Average Current	Unit
Idle current (ARM off)	Master and slave	2.5	mA
synchronous connection oriented (SCO) link HV3	Master and slave	12	mA
extended SCO (eSCO) link EV3 64 kbps, no retransmission	Master and slave	11.5	mA
eSCO link 2-EV3 64 kbps, no retransmission	Master and slave	8.3	mA
GFSK full throughput: TX = DH1, RX = DH5	Master and slave	38.5	mA
EDR full throughput: TX = 2-DH1, RX = 2-DH5	Master and slave	39.2	mA
EDR full throughput: TX = 3-DH1, RX = 3-DH5	Master and slave	39.2	mA
Sniff, one attempt, 1.28 seconds	Master and slave	76 and 100	μA
Page or inquiry scan 1.28 seconds, 11.25 ms	Master and slave	300	μA
Page (1.28 seconds) and inquiry (2.56 seconds) scans, 11.25 ms	Master and slave	430	μA
Low power scan, 1.28 seconds interval, quiet environment	Master and slave	135	μA

#### 4.1.3.2.2 Current Consumption for Different LE Scenarios

Conditions: VDD\_IN = 3.6 V, 25°C, 26-MHz fast clock, nominal unit, 10 dBm output power

Mode	Description	Average Current	Unit
Advertising, nonconnectable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	104	μA
Advertising, discoverable	Advertising in all three channels 1.28-seconds advertising interval 15 bytes advertise data	121	μA
Scanning	Listening to a single frequency per window 1.28-seconds scan interval 11.25-ms scan window	302	μA
Connected (master role)	500-ms connection interval 0-ms slave connection latency Empty TX and RX LL packets	169	μA

#### 4.1.4 General Electrical Characteristics

Rating		Condition	Min	Max	Unit	
High-level output voltage, V <sub>OH</sub>		At 2, 4, 8 mA	0.8 x VDD_IO	VDD_IO	V	
		At 0.1 mA	VDD_IO – 0.2	VDD_IO	V	
Low-level output voltage, V <sub>OL</sub>		At 2, 4, 8 mA	0	0.2 x VDD_IO	V	
		At 0.1 mA	0	0.2	V	
I/O input impedance		Resistance	1		MΩ	
		Capacitance		5	pF	
Output rise and fall times, 10% to 90% (digital pins)		C <sub>L</sub> = 20 pF		10	ns	
I/O pull currents	PCM-I2S bus, TX_DBG, CLK_REQ_OUT	PU	typ = 6.5	3.5	9.7	μA
		PD	typ = 27	9.5	55	
	All others	PU	typ = 100	50	300	μA
		PD	typ = 100	50	360	

#### 4.1.5 nSHUTD Requirements

Parameter	Sym	Min	Max	Unit
Operation mode level <sup>(1)</sup>	V <sub>IH</sub>	1.42	1.98	V
Shutdown mode level <sup>(1)</sup>	V <sub>IL</sub>	0	0.4	V
Minimum time for nSHUT_DOWN low to reset the device		5		ms
Rise and fall times	t <sub>r</sub> and t <sub>f</sub>		20	μs

(1) Internal pulldown retains shut-down mode when no external signal is applied to this pin.

#### 4.1.6 Slow Clock Requirements

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)	<i>Bluetooth</i>				±250	ppm
	Input transition time t <sub>r</sub> and t <sub>f</sub> (10% to 90%)		t <sub>r</sub> and t <sub>f</sub>		200	
Frequency input duty cycle			15%	50%	85%	
Phase noise	At 1 kHz				–125	dBc/Hz
Jitter	Integrated over 300 to 15000 Hz				1	Hz

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Slow clock input voltage limits	Square wave, DC-coupled	$V_{IH}$	$0.65 \times V_{DD\_IO}$		$V_{DD\_IO}$	V peak
		$V_{IL}$	0		$0.35 \times V_{DD\_IO}$	V peak
Input impedance			1			M $\Omega$
Input capacitance					5	pF

#### 4.1.7 External Fast Clock Crystal Requirements and Operation

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Supported crystal frequencies		$f_{in}$	26			MHz
Frequency accuracy (Initial + temperature + aging)					$\pm 20$	ppm
Crystal oscillator negative resistance	26 MHz, external capacitance = 8 pF $I_{osc} = 0.5$ mA		650	940		$\Omega$
	26 MHz, external capacitance = 20 pF $I_{osc} = 2.2$ mA		490	710		

#### 4.1.8 Fast Clock Source Requirements (–40°C to +85°C)

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Supported frequencies		$F_{REF}$	26			MHz
Reference frequency accuracy	Initial + temp + aging				$\pm 20$	ppm
Fast clock input voltage limits	Square wave, DC-coupled	$V_{IL}$	–0.2		0.37	V
		$V_{IH}$	1.0		2.1	V
	Sine wave, AC-coupled		0.4		1.6	$V_{p-p}$
	Sine wave, DC-coupled		0.4		1.6	$V_{p-p}$
	Sine wave input limits, DC-coupled		0		1.6	V
Fast clock input rise time (as % of clock period)	Square wave, DC-coupled				10%	
Duty cycle			35%	50%	65%	
Jitter	10 Hz to 1 MHz, $F_{REF} = 38.4$ MHz				0.022	° RMS
Phase noise for 26 MHz	@ offset = 1 kHz				–123.4	dBc/Hz
	@ offset = 10 kHz				–133.4	dBc/Hz
	@ offset = 100 kHz				–138.4	dBc/Hz

## 4.2 Bluetooth BR/EDR RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz TCXO under a temperature range from –40°C to 85°C and an RF load of 50 Ω at the BT\_RF port of the IC.

### 4.2.1 Bluetooth Receiver—In-Band Signals

Characteristics	Condition	Min	Typ	Max	Bluetooth Specification	Unit	
Operation frequency range		2402		2480		MHz	
Channel spacing			1			MHz	
Input impedance			50			Ω	
Sensitivity, dirty TX on <sup>(1)</sup>	GFSK, BER = 0.1%		–95		–70	dBm	
	Pi/4-DQPSK, BER = 0.01%		–94.5		–70		
	8DPSK, BER = 0.01%		–87.5		–70		
	Pi/4-DQPSK and 8DPSK, BER error floor at sensitivity + 10 dB, dirty TX off	Pi/4-DQPSK		1E–7		1E–5	
	8DPSK		1E–6		1E–5		
Maximum usable input power	GFSK, BER = 0.1%	–5			–20	dBm	
	Pi/4-DQPSK, BER = 0.1%	–10					
	8DPSK, BER = 0.1%	–10					
Intermodulation characteristics	Level of interferers For n = 3, 4, and 5		–30		–39	dBm	
C/I performance  Note: Numbers show desired-signal to interfering-signal ratio. Smaller numbers indicate better C/I performance. Image = –1 MHz	GFSK, co-channel		8		11	dB	
	EDR, co-channel	Pi/4-DQPSK		9.5			13
		8DPSK		16.5			21
	GFSK, adjacent ±1 MHz			–10			0
	EDR, adjacent ±1 MHz, (image)	Pi/4-DQPSK		–10			0
		8DPSK		–5			5
	GFSK, adjacent +2 MHz			–38			–30
	EDR, adjacent +2 MHz,	Pi/4-DQPSK		–38			–30
		8DPSK		–38			–25
	GFSK, adjacent –2 MHz			–28			–20
	EDR, adjacent –2 MHz	Pi/4-DQPSK		–28			–20
		8DPSK		–22			–13
	GFSK, adjacent ≥  ±3  MHz			–45			–40
	EDR, adjacent ≥  ±3  MHz	Pi/4-DQPSK		–45			–40
8DPSK			–44		–33		
RF return loss				–10		dB	
RX mode LO leakage	Frf = (received RF frequency – 0.6 MHz)		–63			dBm	

(1) Sensitivity degradation up to 3 dB may occur for minimum and typical values where the *Bluetooth* frequency is a harmonic of the fast clock.

### 4.2.2 Bluetooth Receiver—General Blocking

Characteristics	Condition	Min	Typ	Unit
Blocking performance over full range, according to <i>Bluetooth</i> specification <sup>(1)</sup>	30 to 2000 MHz		–6	dBm
	2000 to 2399 MHz		–6	
	2484 to 3000 MHz		–6	
	3 to 12.75 GHz		–6	

(1) Eleven of the 24 exceptions allowed in the *Bluetooth* specification

### 4.2.3 Bluetooth Transmitter—GFSK

Characteristics	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF output power		12			dBm
Power variation over <i>Bluetooth</i> band	-1		1		dB
Gain control range		30			dB
Power control step		5		2 to 8	
Adjacent channel power $ M-N  = 2$		-45		$\leq -20$	dBm
Adjacent channel power $ M-N  > 2$		-50		$\leq -40$	

### 4.2.4 Bluetooth Transmitter—EDR

Characteristics		Min	Typ	Max	Bluetooth Specification	Unit
EDR maximum output power	Pi/4-DQPSK		8			dBm
	8DPSK		8			
EDR rel power <sup>(1)</sup>		-2		1	-4 to +1	dB
Power variation over <i>Bluetooth</i> band		-1		1		
Gain control range <sup>(1)</sup>			30			
Power control step <sup>(1)</sup>			5		2 to 8	
Adjacent channel power $ M-N  = 1$ <sup>(1)</sup>			-36		$\leq -26$	dBc
Adjacent channel power $ M-N  = 2$ <sup>(1) (2)</sup>			-30		$\leq -20$	dBm
Adjacent channel power $ M-N  > 2$ <sup>(1) (2)</sup>			-42		$\leq -40$	dBm

(1) For both Pi/4-DQPSK and 8DPSK

(2) Assumes 3-dB insertion loss in external filter

### 4.2.5 Bluetooth Modulation—GFSK

Characteristics	Condition	Sym	Min	Typ	Max	Bluetooth Specification	Unit
-20 dB BW	GFSK			925	995	$\leq 1000$	kHz
Average deviation Detector bandwidth – 10 MHz	Mod data = 4-1, 4-0 1111000011110000...	F1 avg	150	165	170	140 to 175	kHz
Instantaneous deviation	Mod data = 1010101...	F2 max	115	130		$> 115$	kHz
dF2, dF1			85%	88%		$> 80\%$	
Absolute carrier frequency drift	DH1		-25		25	$< \pm 25$	kHz
	DH3 and DH5		-35		35	$< \pm 40$	kHz
Drift rate	External TCXO				15	$< 20$	kHz/ 50 $\mu$ s
Initial carrier frequency tolerance			-25		25	$< \pm 75$	kHz

#### 4.2.6 Bluetooth Modulation—EDR

Characteristics	Condition	Min	Typ	Max	Bluetooth Specification	Unit
Carrier frequency stability			±3	±5	≤ 10	kHz
Initial carrier frequency tolerance				±25	±75	kHz
Rms DEVM <sup>(1)</sup>	Pi/4-DQPSK		6%	15%	20%	
	8DPSK		6%	13%	13%	
99% DEVM <sup>(1)</sup>	Pi/4-DQPSK			30%	30%	
	8DPSK			20%	20%	
Peak DEVM <sup>(1)</sup>	Pi/4-DQPSK		14%	30%	35%	
	8DPSK		16%	25%	25%	

(1) Max performance refers to maximum TX power.

#### 4.2.7 Bluetooth Transmitter—Out-of-Band and Spurious Emissions

Characteristics	Condition	Typ	Max	Unit
Second harmonic <sup>(1)</sup>	Measured at 10-dBm output power	-14		dBm
Third harmonic <sup>(1)</sup>		-10		dBm
Fourth harmonics <sup>(1)</sup>		-19		dBm

(1) Meets FCC and ETSI requirements with external filter shown in [Figure 5-1](#)



### 4.3 Bluetooth LE RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz TCXO under a temperature range from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and an RF load of  $50\ \Omega$  at the BT\_RF port of the IC.

#### 4.3.1 BLE Receiver—In Band Signals

Characteristic	Condition	Min	Typ	Max	BLE Specific ation	Unit
Operation frequency range		2402		2480		MHz
Channel spacing			2			MHz
Input impedance			50			$\Omega$
Sensitivity dirty TX on <sup>(1)</sup>	PER = 30.8%; dirty TX on		-96		$\leq -70$	dBm
Maximum usable input power	GMSK, PER = 30.8%	-5			$\geq -10$	dBm
Intermodulation characteristics	Level of interferers. For n = 3, 4, 5		-30		$\geq -50$	dBm
C/I performance Note: Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance. Image = -1 MHz	GMSK, co-channel		8		$\leq 21$	dB
	GMSK, adjacent $\pm 1$ MHz		-5		$\leq 15$	
	GMSK, adjacent +2 MHz		-45		$\leq -17$	
	GMSK, adjacent -2 MHz		-22		$\leq -15$	
	GMSK, adjacent $\geq  \pm 3 $ MHz		-47		$\leq -27$	
RX mode LO leakage	Fr <sub>f</sub> = (received freq - 0.6 MHz)		-63			dBm

(1) Sensitivity degradation up to 3 dB may occur where the BLE frequency is a harmonic of the fast clock.

#### 4.3.2 BLE Receiver—General Blocking

Characteristics	Condition	Min	Typ	BLE spec	Unit
Blocking performance over full range, according to BLE specification <sup>(1)</sup>	30–2000 MHz		-15	$\geq -30$	dBm
	2000–2399 MHz		-15	$\geq -35$	
	2484–3000 MHz		-15	$\geq -35$	
	3–12.75 GHz		-15	$\geq -30$	

(1) Seven of the 10 exceptions allowed in the BLE specification

#### 4.3.3 BLE Transmitter

Characteristics	Min	Typ	Max	BLE Specification	Unit
Maximum RF output power		12 <sup>(1)</sup>		$\leq 10$	dBm
Power variation over BLE band			1		dB
Adjacent channel power $ M-N  = 2$		-45		$\leq -20$	dBm
Adjacent channel power $ M-N  > 2$		-50		$\leq -30$	

(1) To achieve the BLE specification of 10-dBm maximum, use normal system losses from, for example, filters or reduce the value using the VS command.

#### 4.3.4 BLE Modulation

Characteristics	Condition	Sym	Min	Typ	Max	BLE Specification	Unit
Average deviation detector bandwidth – 10 MHz	Mod data = 4-1, 4-0 1111000011110000...	$\Delta f1$ avg	240	250	260	225 to 275	kHz
Instantaneous deviation	Mod data = 1010101...	$\Delta f2$ max	185	210		$\geq 185$	kHz
$\Delta f2, \Delta f1$			0.85	0.9		$\geq 0.8$	
Absolute carrier frequency drift			-25		25	$\leq \pm 50$	kHz
Drift rate					15	$\leq 20$	kHz/50 ms
Initial carrier frequency tolerance			-25		25	$\leq \pm 100$	kHz

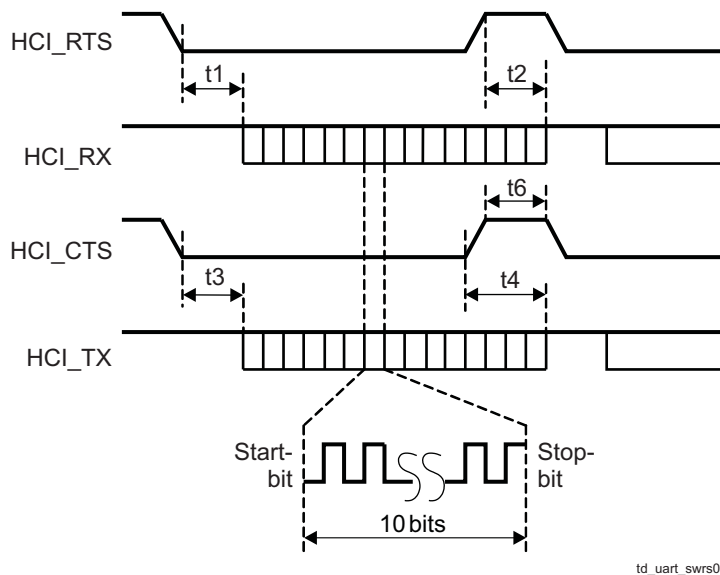
#### 4.3.5 BLE Transceiver, Out-Of-Band and Spurious Emissions

See [Section 4.2.7](#), *Bluetooth Transmitter, Out-of-Band and Spurious Emissions*.

## 4.4 Interface Specifications

### 4.4.1 UART

Figure 4-1 shows the UART timing diagram. Table 4-1 lists the UART timing characteristics.



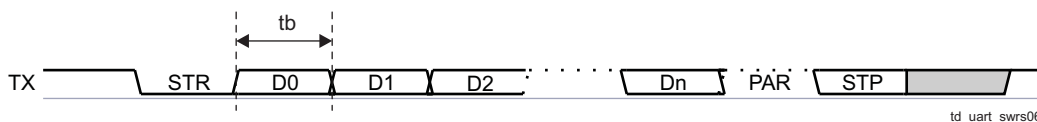
td\_uart\_swrs064

Figure 4-1. UART Timing

Table 4-1. UART Timing Characteristics

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate		37.5		4000	kbps
	Baud rate accuracy per byte	Receive and transmit	-2.5		1.5	%
	Baud rate accuracy per bit	Receive and transmit	-12.5		12.5	%
t3	CTS low to TX_DATA on		0	2		μs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		μs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte

Figure 4-2 shows the UART data frame. Table 4-2 describes the symbols used in Table 4-2.



td\_uart\_swrs064

Figure 4-2. Data Frame

Table 4-2. Data Frame Key

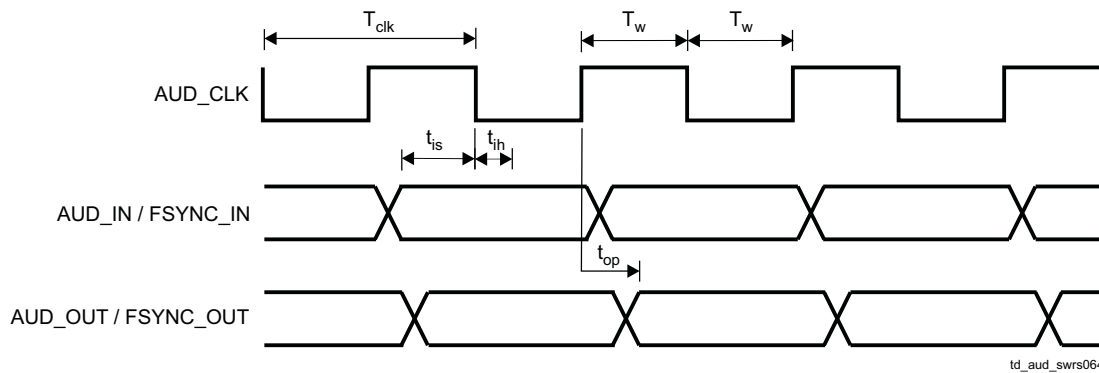
Symbol	Description
STR	Start-bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)

**Table 4-2. Data Frame Key (continued)**

Symbol	Description
STP	Stop-bit

**4.4.2 PCM**

Figure 4-3 shows the interface timing for the PCM. Table 4-3 and Table 4-4 lists the associated master and slave parameters.



**Figure 4-3. PCM Interface Timing**

**Table 4-3. PCM Master**

Symbol	Parameter	Condition	Min	Max	Unit
$T_{clk}$	Cycle time		244.14 (4.096 MHz)	15625 (64 kHz)	ns
$T_w$	High or low pulse width		50% of $T_{clk}$ min		
$t_{is}$	AUD_IN setup time		25		
$t_{ih}$	AUD_IN hold time		0		
$t_{op}$	AUD_OUT propagation time	40-pF load	0	10	
$t_{op}$	FSYNC_OUT propagation time	40-pF load	0	10	

**Table 4-4. PCM Slave**

Symbol	Parameter	Condition	Min	Max	Unit
$T_{clk}$	Cycle time		66.67 (15 MHz)		ns
$T_w$	High or low pulse width		40% of $T_{clk}$		
$T_{is}$	AUD_IN setup time		8		
$T_{ih}$	AUD_IN hold time		0		
$t_{is}$	AUD_FSYNC setup time		8		
$t_{ih}$	AUD_FSYNC hold time		0		
$t_{op}$	AUD_OUT propagation time	40-pF load	0	21	

## 5 REFERENCE DESIGN AND BOM FOR POWER AND RADIO CONNECTIONS

Figure 5-1 shows the reference schematics for the CC256x device. Consult TI for complete schematics and PCB layout guidelines.

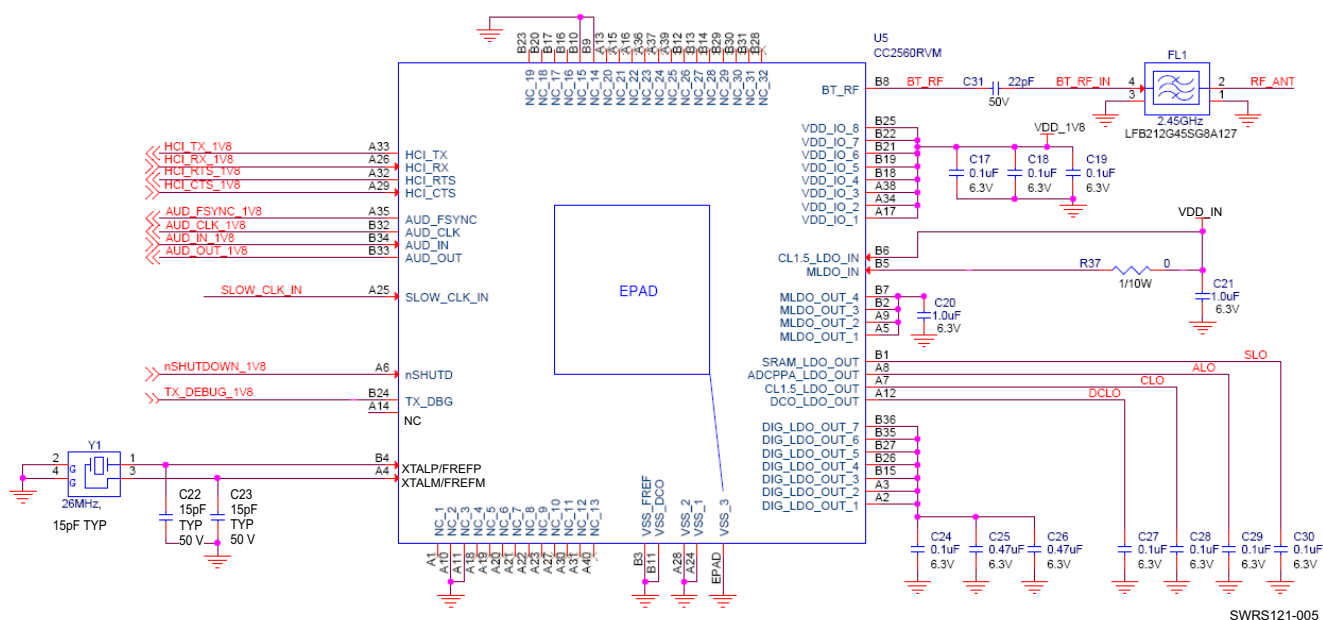


Figure 5-1. Reference Schematics

Table 5-1 lists the BOM for the CC256x device.

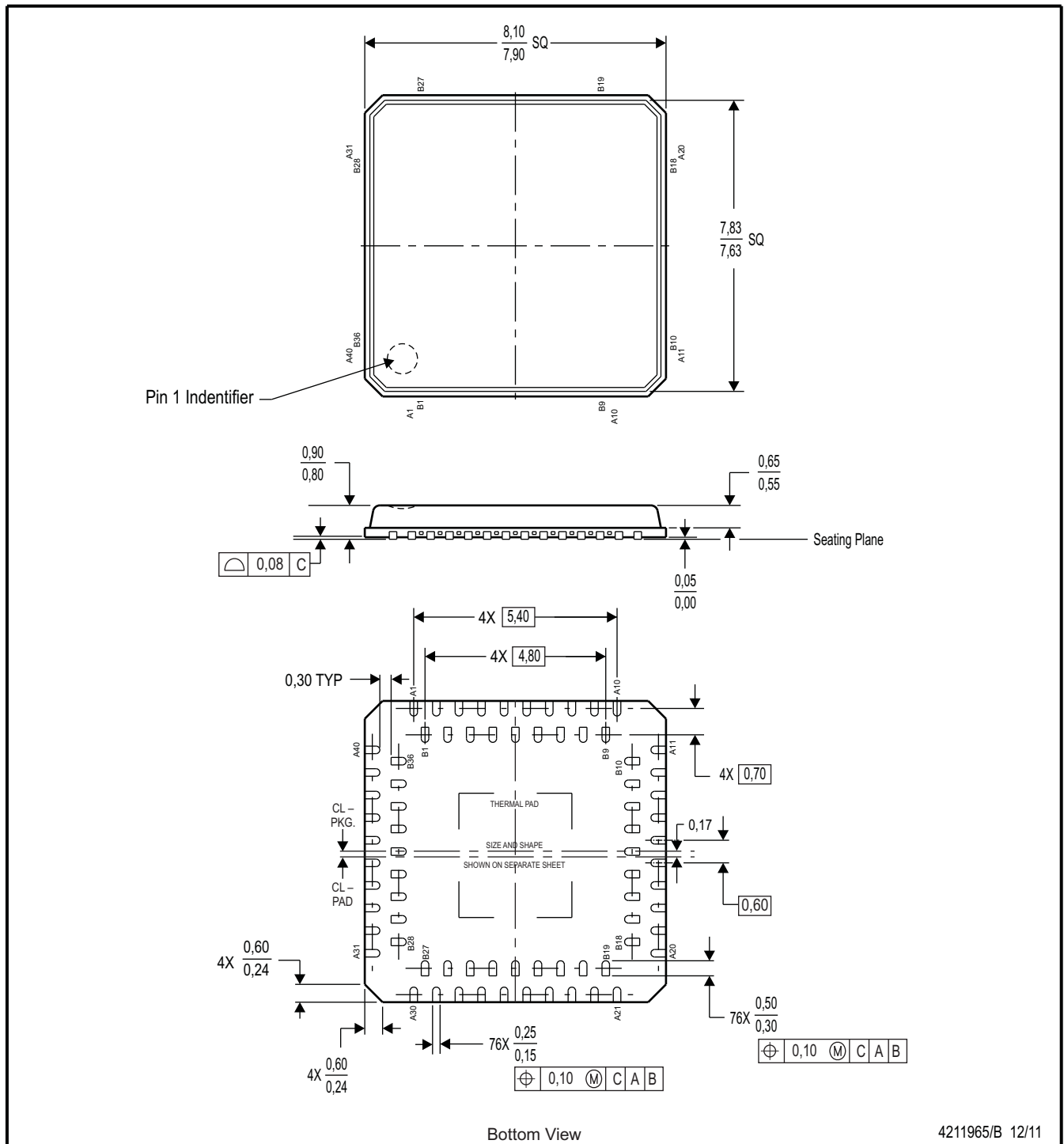
Table 5-1. Bill of Materials

Qty	Reference Des.	Value	Description	Manufacturer	Manufacturer Part Number	Alternate Part	Note
1	ANT1	NA	ANT_IIFA_CC2420_32mil_MIR	NA	IIFA_CC2420	Chip antenna	Copper antenna on PCB
8	Capacitor	0.1 $\mu$ F	CAP CER 1.0UF 6.3 V X5R 10% 0402	Kemet	C0402C104K9RACTU		
2	Capacitor	1.0 $\mu$ F	CAP CER 10-pF 50 V 5% NP0 0402	Taiyo Yuden	JMK105BJ105KV-F		
2	Capacitor	10 pF (TBD)	CAP CER 1.0 $\mu$ F 6.3 V X5R 10% 0402	Murata Electronics	GRM1555C1H100JZ01 D		
2	Capacitor	0.47 $\mu$ F	FILTER CER BAND PASS 2.45 GHZ SMD	Taiyo Yuden	JMK105BJ474KV-F		
1	FL1	2.45 GHz	FILTER CER BAND PASS 2.45 GHZ SMD	Murata Electronics	LFB212G45SG8C341		Place brown marking up
1	OSC1	32,768 kHz 15 pF	OSC 32.768 KHZ 15 pF 1.5 V 3.3 V SMD	Abrakon Corporation	ASH7K-32.768KHZ-T		Optional
1	U1	LP2985-18DBV	IC REG LDO 1.8 V 0.15 A SOT23-5	Texas Instruments	LP2985-18DBV		Optional
3	U2 U3 U4	SN74AVC4T774RSV	IC BUS TRANSCVR 4 BIT WITH 1.2–3.6 V 16-UQFN	Texas Instruments	LP2985-18DBV		Optional
1	U5	CC2560RVM or CC2564RVM	Bluetooth BR/EDR/LE or ANT Single-Chip Solution	Texas Instruments	CC256xRVM		
1	XSHLD1	RF shield cover	Board shield 0.650X0.650" cover	Laird Technologies EMI	BMI-S-202-C		
1	Y1	26 MHz	Crystal, 26 MHz, 8 pF	NDK	NX2016SA	TZ1325D (Tai-Saw TST)	

## 6 mrQFN MECHANICAL DATA

RVM (S-PVQFN-N76)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

SWRS115-001

RVM (S-PVQFN-N76)

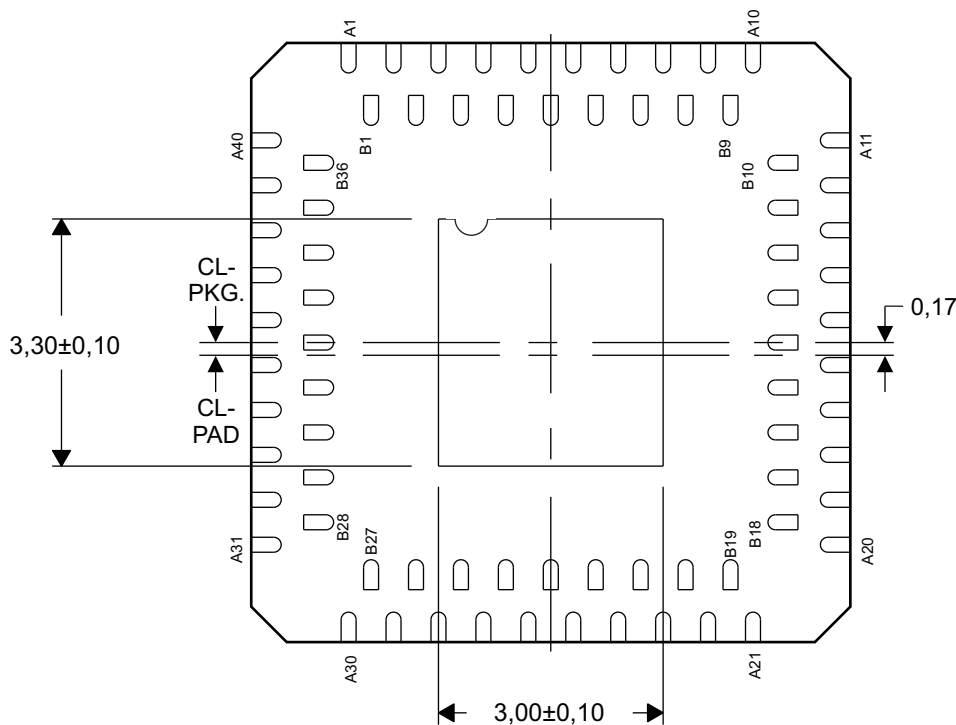
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212066/B 12/11

NOTE: All linear dimensions are in millimeters

SWRS115-018

## 7 CHIP PACKAGING AND ORDERING

### 7.1 Package and Ordering Information

The mrQFN packaging is 76 pins and a 0.6-mm pitch.

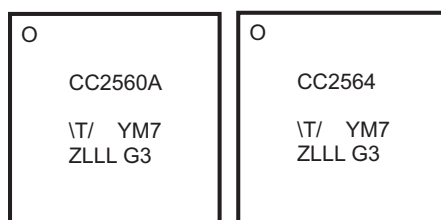
For detailed information, see [Section 6](#), *mrQFN Mechanical Data*.

[Table 7-1](#) lists the package and order information for the device family members.

**Table 7-1. Package and Order Information**

Device	Package Suffix	Pieces/Reel
CC2560ARVMT	RVM	250
CC2560ARVMR	RVM	2500
CC2564RVMT	RVM	250
CC2564RVMR	RVM	2500

[Figure 7-1](#) shows the chip markings for the CC256x family.



- \T/ = TI logo
- YM = Year month date code
- 7 = Primary site code for ANM
- Z = Secondary site code for ANM
- LLL = Assembly lot code
- O = Pin 1 indicator

SWRS121-010

**Figure 7-1. Chip Markings**

#### 7.1.1 Device Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.

- X Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI specifications. Experimental/Prototype devices are shipped against the following disclaimer: "This product is still in development and is intended for internal evaluation purposes." Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
- null Device is qualified and released to production. TI's standard warranty applies to production devices.



## 7.2 Empty Tape Portion

Figure 7-2 shows the empty portion of the carrier tape.

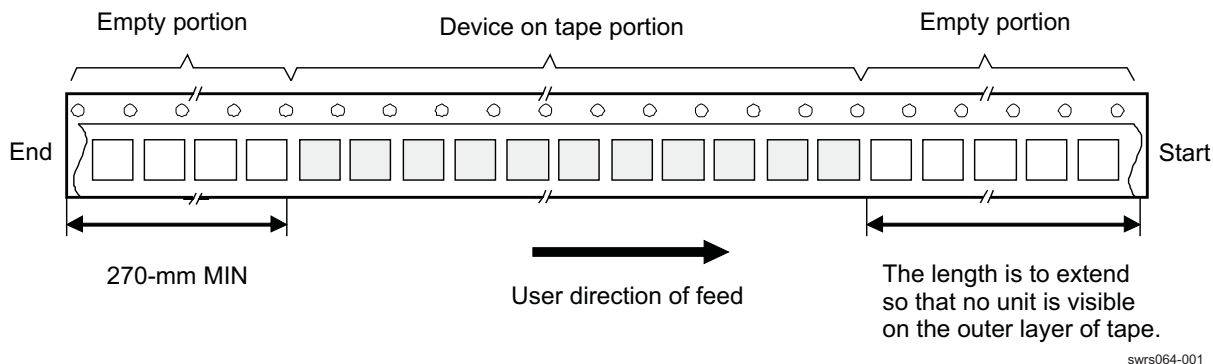


Figure 7-2. Carrier Tape and Pockets

## 7.3 Device Quantity and Direction

When pulling out the tape, the A1 corner is on the left side (see Figure 7-3).

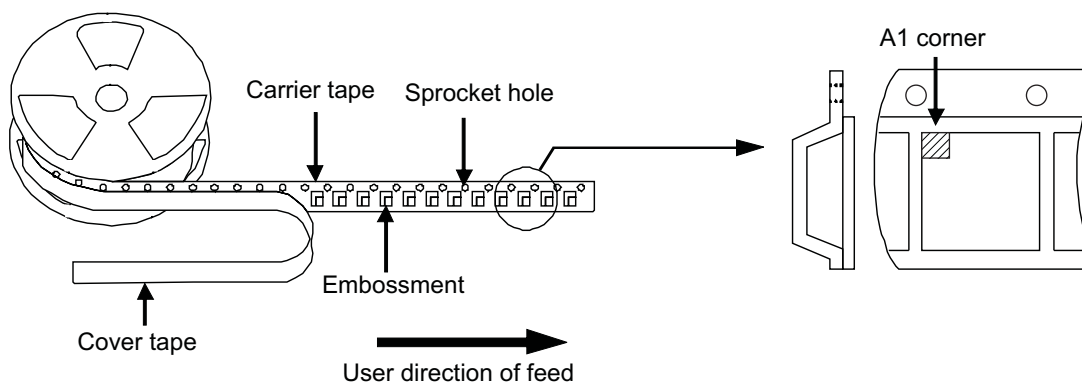


Figure 7-3. Direction of Device

## 7.4 Insertion of Device

Figure 7-4 shows the insertion of the device.

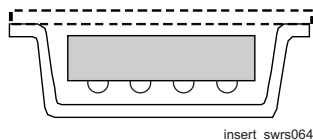


Figure 7-4. Insertion of Device

## 7.5 Tape Specification

The dimensions of the tape are:

- Tape width: 16 mm
- Cover tape: The cover tape does not cover the index hole and does not shift to outside from the carrier tape.
- Tape structure: The carrier tape is made of plastic. The device is put in the embossed area of the carrier tape and covered by the cover tape, which is made of plastic.
- ESD countermeasure: The plastic material used in the carrier tape and the cover tape is static dissipative.

## 7.6 Reel Specification

Figure 7-5 shows the reel specifications:

- 330-mm reel, 16-mm width tape
- Reel material: Polystyrene (static dissipative/antistatic)

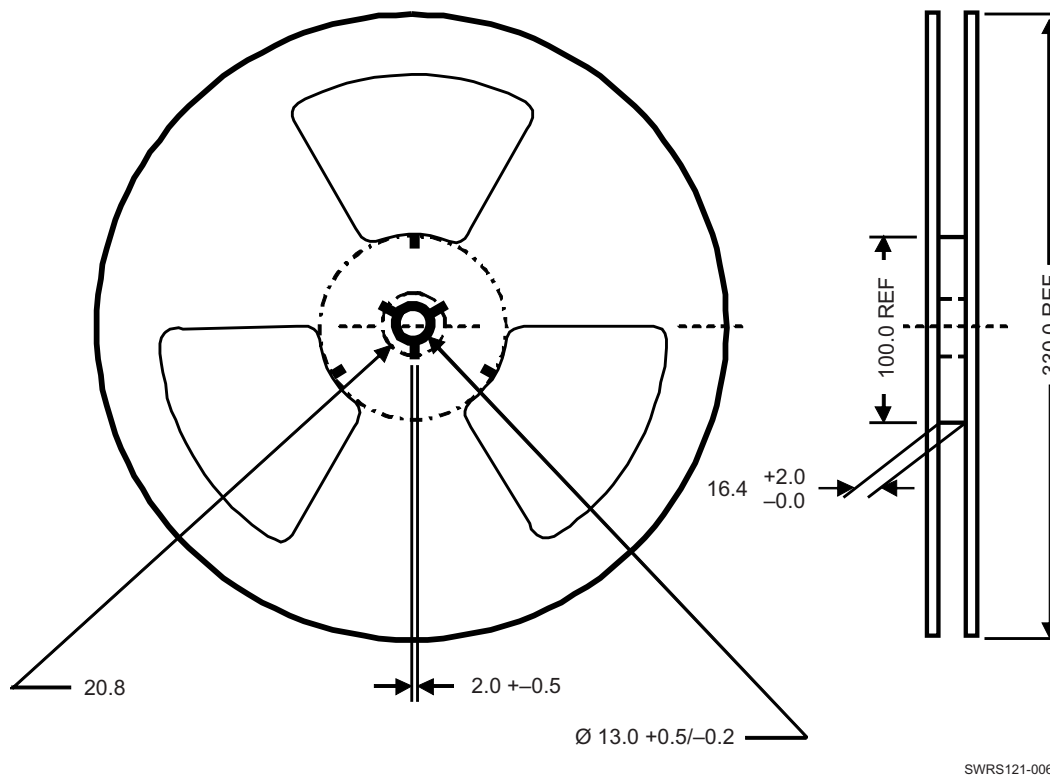
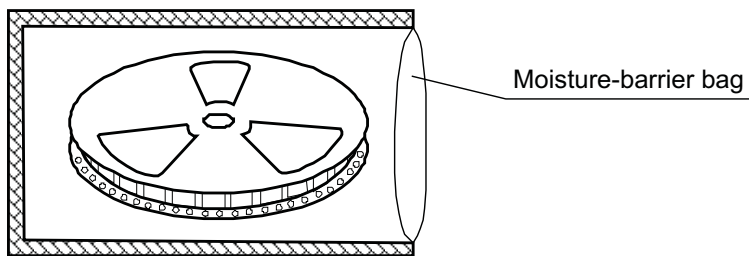


Figure 7-5. Reel Dimensions (mm)

## 7.7 Packing Method

The end of the leader tape is secured by drafting tape. The reel is packed in a moisture barrier bag fastened by heat-sealing (see Figure 7-6).



reelpk\_swrs064

**Figure 7-6. Reel Packing Method**

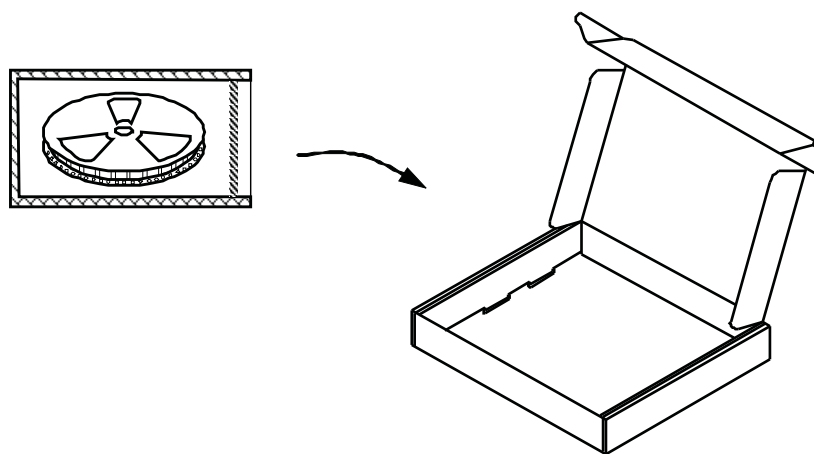
**CAUTION**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause devices not to meet their published specifications.

**7.8 Packing Specification**

**7.8.1 Reel Box**

Each moisture-barrier bag is packed into a reel box, as shown in [Figure 7-7](#).



rlbx\_swrs064

**Figure 7-7. Reel Box (Carton)**

**7.8.2 Reel Box Material**

The reel box is made from corrugated fiberboard.

**7.8.3 Shipping Box**

If the shipping box has excess space, filler (such as cushion) is added.

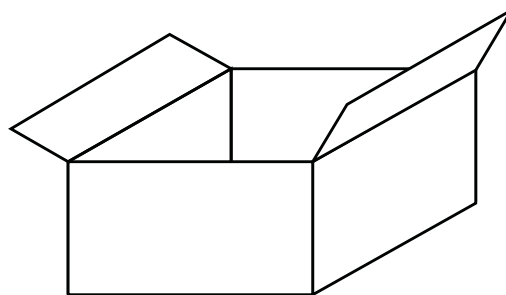
[Figure 7-8](#) shows a typical shipping box.

---

**NOTE**

The size of the shipping box may vary depending on the number of reel boxes packed.

---



box\_swrs064

**Figure 7-8. Shipping Box (Carton)**

#### **7.8.4 Shipping Box Material**

The shipping box is made from corrugated fiberboard.

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

The following table summarizes the Data Manual versions.

Version	Literature Number	Date	Notes
*	SWRS121	July 2012	See <sup>(1)</sup> .
A	SWRS121	October 2012	See <sup>(2)</sup> .

- (1) Initial release.
- (2) *CC256x QFN Device* – SWRS121A: Sections impacted by changes between version \* and version A:
- Title: Revised title from *CC256x Bluetooth BR/EDR/LE Single-Chip Solution*
  - Features section: Revised and added features, including BR/EDR and LE.
  - Section 2: Revised section.
  - Section 3: Moved BR/EDR and LE features to Features section.
  - Section 5.2: Revised section
  - Section 5.3: Revised section
  - Section 6: Added BOM

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2560ARVMR	NRND	VQFNP-MR	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2560A	
CC2560ARVMT	NRND	VQFNP-MR	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2560A	
CC2560BRVMR	ACTIVE	VQFNP-MR	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2560B	<a href="#">Samples</a>
CC2564BRVMR	ACTIVE	VQFNP-MR	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2564B	<a href="#">Samples</a>
CC2564BRVMT	ACTIVE	VQFNP-MR	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2564B	<a href="#">Samples</a>
CC2564NSRVMR	NRND	VQFNP-MR	RVM	76	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CC2564	
CC2564NSRVMT	NRND	VQFNP-MR	RVM	76	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CC2564	
CC2564RVMR	NRND	VQFNP-MR	RVM	76	2500	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2564	
CC2564RVMT	NRND	VQFNP-MR	RVM	76	250	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-3-260C-168 HR	-40 to 85	CC2564	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

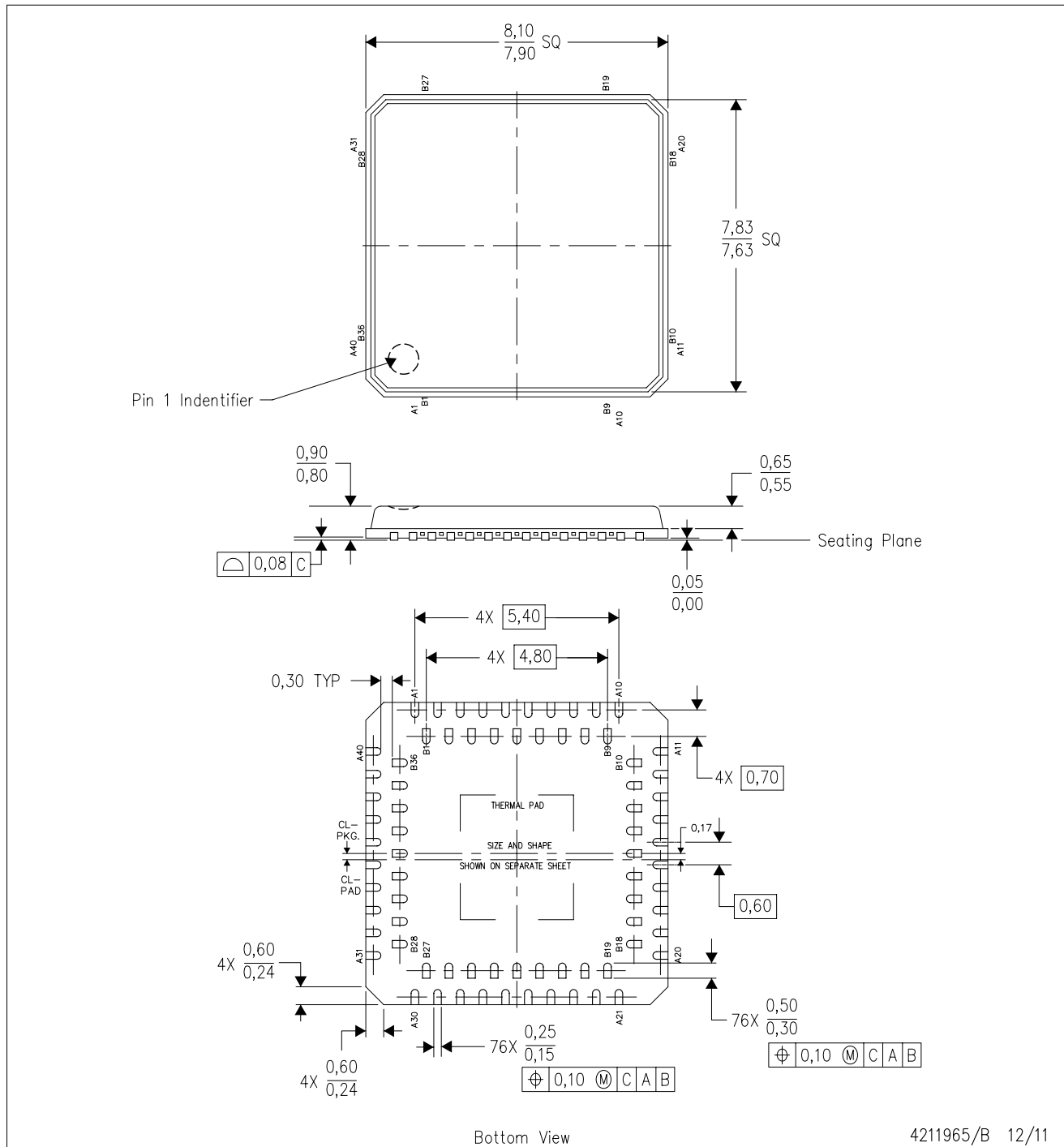
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RVM (S-PVQFN-N76)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



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