LMG3410 600-V 12-A Single Channel GaN Power Stage

1 Features

- Integrated 70-mΩ, 600-V GaN and Driver
- Single Package for Ease of Design and Layout
- Up to 1 MHz Steady-State Operation
- 20-ns Typical Propagation Delay
- Operates From a Single Unregulated 12-V Supply
- Externally-Adjustable Drive Strength for Switching Performance and EMI Control
  - Supports 25 to 100 V/ns
- Integrated DC-DC Converter for Negative Drive Voltage
- Fault Output Ensures Safety
  - UVLO Protection
  - Over-Current Protection
  - Over-Temperature Protection
- High Edge-Rate Tolerance

2 Applications

- Server/Telecom AC-DC Supplies
- Rack-Mount Server DC Power Distribution
- Solar Inverters
- Motor Drives

3 Description

The LMG3410 Single-Channel Gallium-Nitride (GaN) Power Stage contains a 70-mΩ, 600-V GaN power transistor and specialized driver in an 8-mm by 8-mm QFN package. Our Direct Drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off via its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally-generated negative voltage supply.

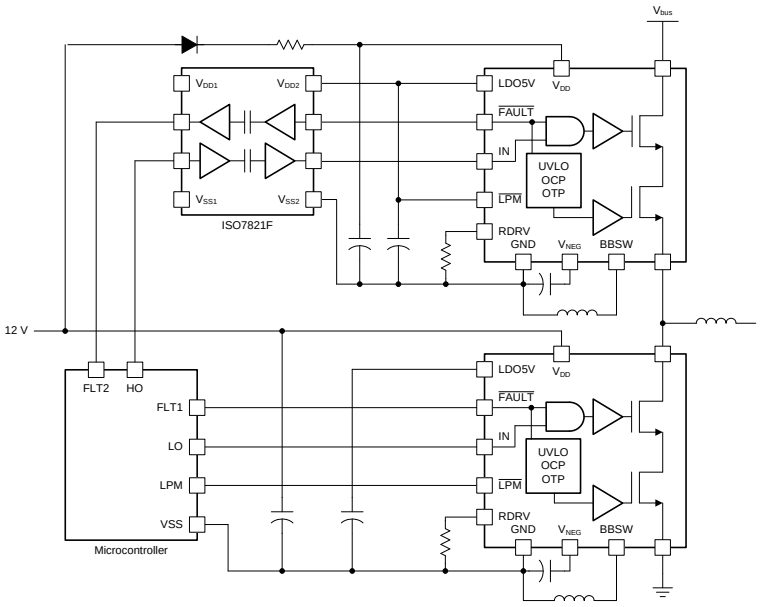
The integrated driver provides additional protection and convenience features. Fast over-current, over-temperature and under-voltage lockout (UVLO) protections help create a fail-safe system; the device's status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG3410	QFN (32)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified System Diagram



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- Changed Gan Technology Preview to Advanced Information ... 1

Changes from Original (April 2016) to Revision A — **Page**

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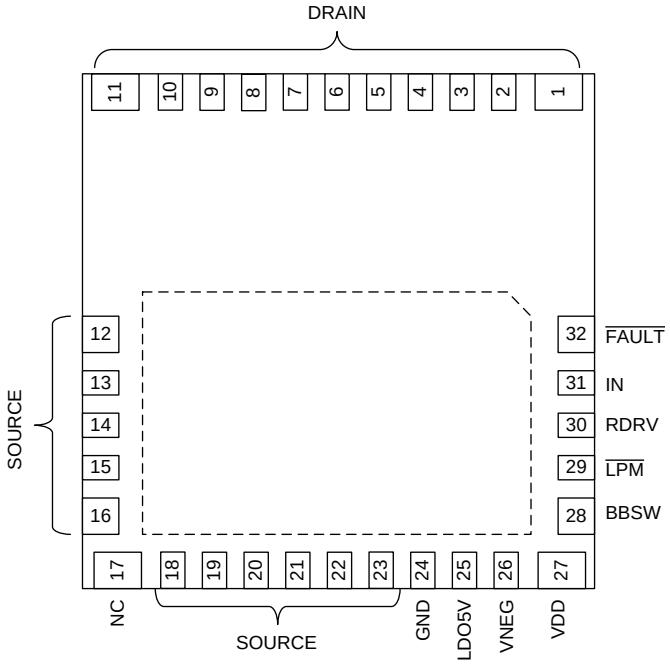
- Clarified first-page description to better describe functionality of device ... 1
- Changed Theta_JA number to JEDEC standard PCB ... 4
- Clarified definition of turn-on and turn-off energy ... 10
- Corrected wording in Do's and Don'ts section ... 17
- Removed non-suitable isolated supply recommendation ... 18
- Added note on MSL 3 manufacturing guidance ... 23

5 Pin Configuration and Functions

RWH (QFN) PACKAGE
32 PINS
(Top View)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BBSW	28	P	Buck-boost converter switch pin. Connect an inductor from this point to GND.
DRAIN	1-11	P	Power transistor drain
$\overline{\text{FAULT}}$	32	O	Fault output, push-pull, active low
GND	24	G	Signal ground reference and kelvin source; **connected to source internally**
IN	31	I	CMOS-compatible non-inverting gate drive input
LDO5V	25	P	5-V LDO output for digital isolator, generated internally with linear regulator.
$\overline{\text{LPM}}$	29	I	Enables low-power-mode by pulling the pin to ground
SOURCE	12 to 16, 18 to 23	P	Power transistor source, die-attach pad, thermal sink
RDRV	30	I	Drive strength selection pin. Connect a resistor from this pin to ground to set the turn-on drive strength to control slew rate
VDD	27	P	12-V power input, relative to GND. Supplies 5-V rail and gate drive supply.
VNEG	26	P	Negative supply output; bypass to GND with 2.2-µF capacitor.
NC	17	—	Not connected, Connect to source or leave floating
PAD	GND	P	Thermal Pad; tie to source with multiple vias

(1) I = Input, O = Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DS}	Drain-Source Voltage		600	V
V_{DD}	Supply Voltage	–0.3	20	V
I_{DS}	Drain-Source Current, Pulsed	–32	32	A
V_{IN}	IN, $\overline{LPM}$ Pin Voltage		5.5	V
T_{STG}	Storage Temperature	–55	150	°C
T_J	Operating Temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DS}	Drain-Source Voltage			480	V
V_{DD}	Supply Voltage	9.5	12	18	V
I_{DS}	DC Drain-Source Current			12	A
I_{+5V}	LDO External Load Current			5	mA
T_J	Operating Temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1) (2)		LMG3410 RWH (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3)	26.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) The Theta_JA specification is based on a JEDEC 2s2p PCB using thermal vias in still air.

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6.5 Electrical Characteristics

over operating free-air temperature range, 9.5 V < V_{DD} < 18 V, $\overline{LPM}$ = 5 V, V_{NEG} = -14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GaN POWER TRANSISTOR						
$R_{DS,ON}$	Total On-state Resistance	T_J = 25°C		70		mΩ
		T_J = 150°C		135		
V_{SD}	Third-quadrant mode source-drain voltage	IN = 0 V, I_{SD} = 0.1 A		5		V
		IN = 0 V, I_{SD} = 10 A		7.8		
I_{DSS}	Drain Leakage Current	V_{DS} = 600 V, T_J = 25°C		1	5	µA
		V_{DS} = 600 V, T_J = 150°C		10		
C_{oss}	GaN output capacitance	IN = 0 V, V_{DS} = 400 V, f_{SW} = 250 kHz		71		pF
$C_{oss,er}$	Effective output capacitance, energy related	IN = 0 V, V_{DS} =0-400 V		95		pF
$C_{oss,tr}$	Effective output capacitance, time related	I_D = 5 A, IN = 0 V, V_{DS} = 0-400 V		145		pF
Q_{rr}	Reverse recovery charge	V_R = 400 V, I_{SD} = 5 A, dI_{SD}/dt = 1 A/ns		0		nC
DRIVER SUPPLY						
$I_{VDD,LPM}$	Quiescent current, ultra-low-power mode	V_{LPM} = 0 V, V_{DD} = 12 V, T_J = 25°C		80	125	µA
		T_J = 150°C		125		
$I_{VDD,Q}$	Quiescent current (average)	Transistor held off		0.7		mA
		Transistor held on		0.7		
$I_{VDD,op}$	Operating current	V_{DD} = 12 V, f_{SW} = 1 MHz, R_{DRV}=40 kΩ, 50% duty cycle		43		mA
V_{+5V}	5V LDO output voltage	V_{DD} = 12 V	4.7		5.3	V
V_{NEG}	Negative Supply	30-mA load current		–13.9		V
BUCK-BOOST CONVERTER						
$f_{SW,DCDC}$	DC-DC switching frequency	I_{OUT} = 20 mA		1		MHz
$I_{DCDC,PK}$	Peak inductor current	I_{OUT} = 20 mA, V_{IN} = 12 V, V_{OUT} = -14 V		250	350	mA
ΔV_{NEG}	DC-DC output ripple voltage, pk-pk	C_{NEG} = 1 µF, I_{OUT} = 20 mA		200		mV
η_{DCDC}	DC-DC converter efficiency	I_{OUT} = 20 mA, V_{IN} = 12 V, V_{NEG} = -14 V		75%		
DRIVER INPUT						
V_{IH}	Input pin, $\overline{LPM}$ pin, logic high threshold				2.5	V
V_{IL}	Input pin, $\overline{LPM}$ pin, low threshold		0.8			V
V_{HYST}	Input pin, $\overline{LPM}$ pin, hysteresis			0.8		V
$R_{IN,L}$	Input pull-down resistance			150		kΩ
R_{LPM}	$\overline{LPM}$ pin pull-down resistance			150		kΩ
UNDERVOLTAGE LOCKOUT						
$V_{DD,UVLO}$	Under-voltage Lockout	Turn-on voltage	8.6		9.4	V
$\Delta V_{DD,UVLO}$	UVLO Hysteresis			500		mV
FAULT						
I_{trip}	Current Fault Trip Point		24	36	50	A
T_{trip}	Temperature Trip Point	Trip point		165		°C
$T_{tripHys}$	Temperature Trip Hysteresis			20		°C

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6.6 Switching Characteristics

over operating free-air temperature range, 9.5 V < V_{DD} < 18 V, V_{NEG} = -14 V, V_{BUS} = 400 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GaN FET						
dv/dt	Turn-on Drain Slew Rate	R_{DRV} = 15 kΩ		100		V/ns
		R_{DRV} = 40 kΩ		50		
		R_{DRV} = 100 kΩ		25		
Δdv/dt	Slew Rate Variation	turn on, I_L = 5 A, R_{DRV} = 40 kΩ		25%		
dv/dt	Edge Rate Immunity	Drain dv/dt, device remains off inductor-fed, max di/dt = 10 A/ns		150		V/ns
STARTUP						
t_{START}	Startup Time, V_{IN} rising above UVLO	Time until gate responds to IN C_{NEG} = 2.2 µF, C_{LDO} = 1 µF		2		ms
DRIVER						
$t_{pd,on}$	Propagation delay, turn on	IN rising to I_{DS} > 10 mA, V_{DS} = 100 V R_{DRV} = 40 kΩ, V_{NEG} = -14 V		20		ns
$t_{delay,on}$	Turn on delay time	I_{DS} > 1 A to V_{DS} < 320 V, R_{DRV} = 40 kΩ		12		ns
t_{rise}	Rise Time	V_{DS} = 320 V to V_{DS} = 80 V, I_D = 5 A		4.2		ns
$t_{pd,off}$	Propagation delay, turn off	IN falling to V_{DS} > 10 V; I_D = 5 A		36		ns
t_{fall}	Fall Time	V_{DS} = 80 V to V_{DS} = 320 V, I_D = 5 A		15		ns
FAULT						
t_{curr}	Current Fault Delay	I_{DS} > I_{TH} to $\overline{FAULT}$ low		50		ns
t_{blank}	Current Fault Blanking Time			20		ns
t_{reset}	Fault reset time	IN held low		350		µs

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6.7 Typical Characteristics

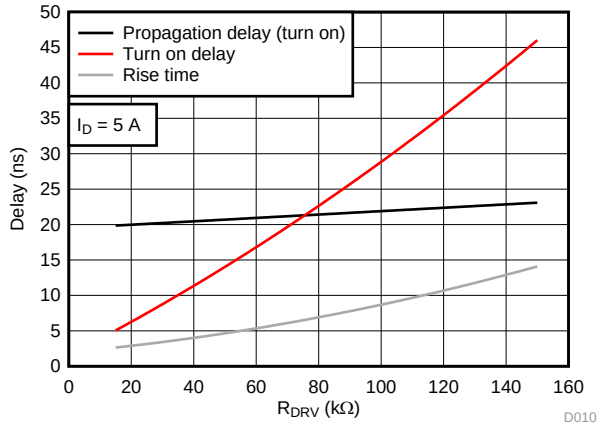

Figure 1. Turn-on Delays vs Drive-Strength Resistor

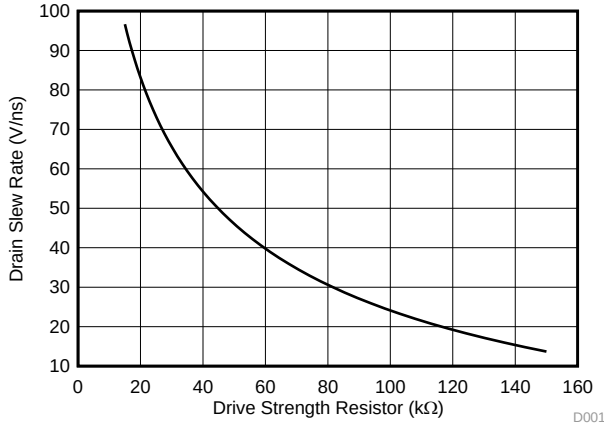

Figure 2. Drain Slew Rate vs Drive-Strength Resistor

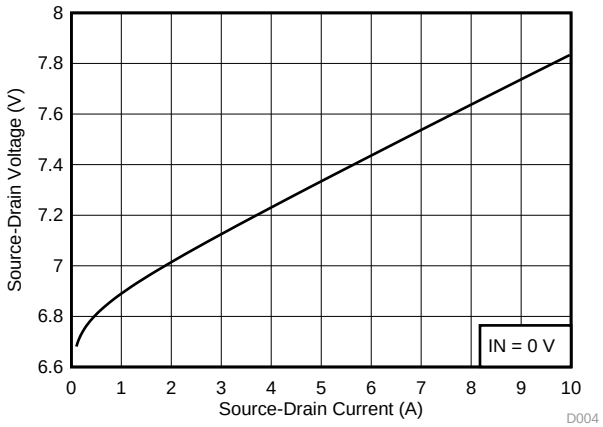

Figure 3. Source-Drain Voltage in 3rd Quadrant Operation

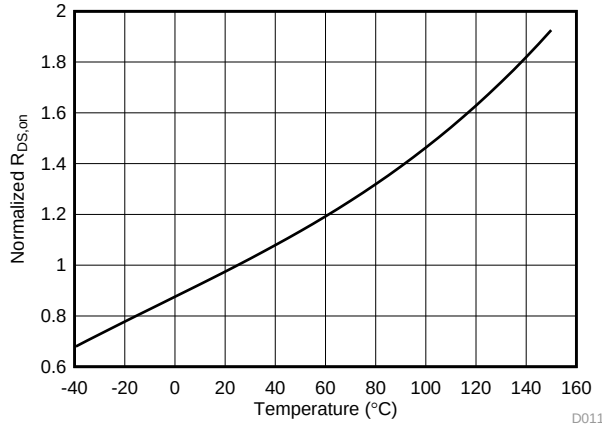

Figure 4. Normalized On Resistance vs Temperature

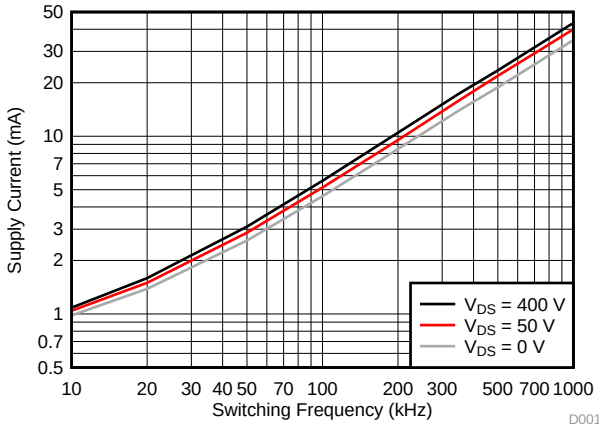

Figure 5. V_{DD} Supply Current vs Switching Frequency

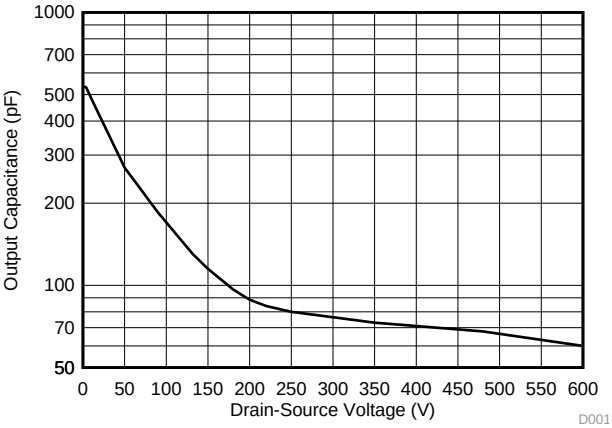

Figure 6. Output Capacitance

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Typical Characteristics (continued)

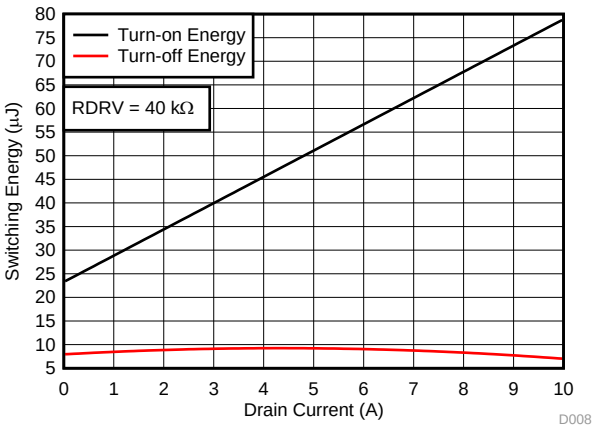

Figure 7. Hard-switched Half-Bridge Turn-on and Turn-off Switching Energy vs Drain Current

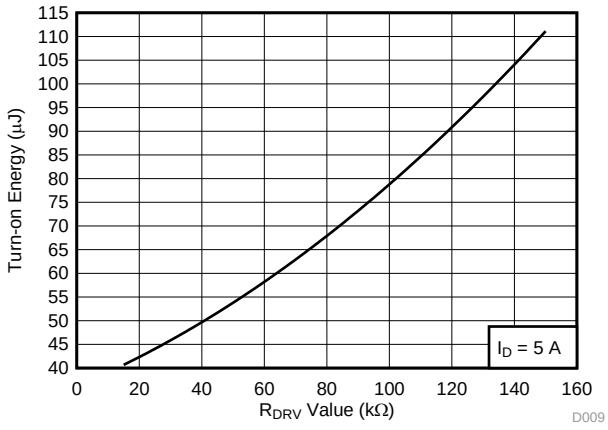

Figure 8. Hard-switched Half-Bridge Turn-On Switching Energy vs Slew Rate Resistor

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7 Parameter Measurement Information

7.1 Switching Parameters

The circuit used to measure most switching parameters is shown in Figure 9. The top LMG3410 in this circuit is used to recirculate the inductor current and functions in third-quadrant mode only. The bottom device is the active device; it is turned on to increase the inductor current to the desired test current. The bottom device is then turned off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage is measured. The specific timing measurement is shown in Figure 10.

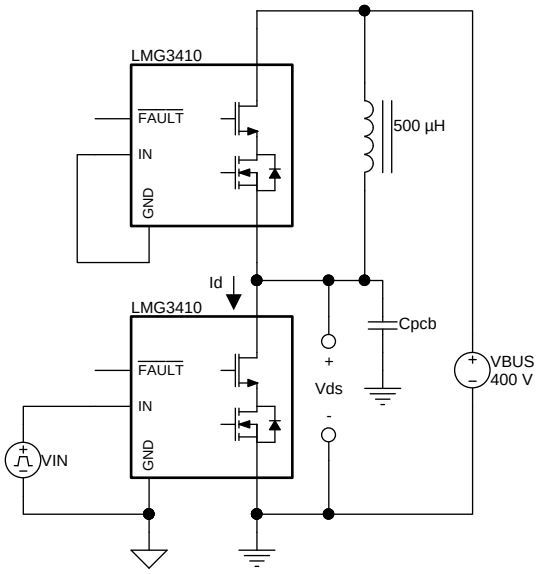


Figure 9. Circuit Used to Determine Switching Parameters

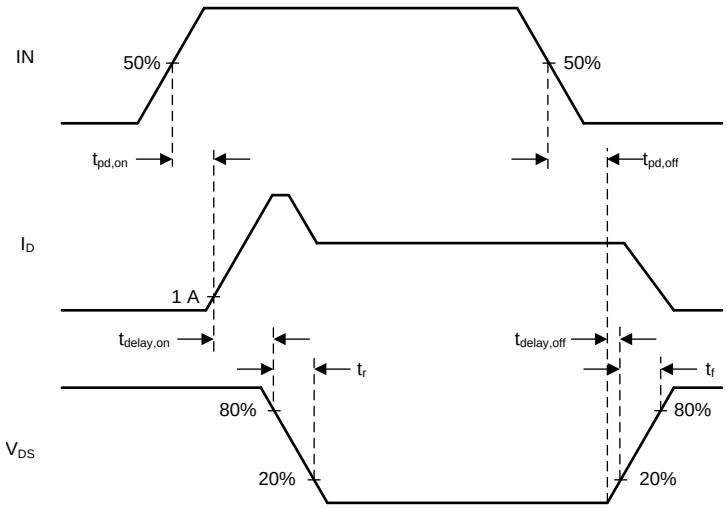


Figure 10. Measurement to Determine Propagation Delays and Slew Rates

Switching Parameters (continued)

7.1.1 Turn-on Delays

The timing of the turn-on transition is broken into three components: propagation delay, turn-on delay and rise time. The first component is the propagation delay of the driver from when the input goes high to when the GaN FET starts turning on. The turn-on delay is the delay from when the FET starts turning on (represented by 1 A drain current) to when the drain voltage swings down by 20 percent. Finally, the rise time is the time it takes the drain voltage to slew between 80 percent and 20 percent of the bus voltage. The drive-strength resistor value has a large effect on turn-on delay and rise time but does not affect the propagation delay significantly.

The propagation delay specification is comparable to MOSFET drivers while the turn-on delay and the rise time are comparable to the respective MOSFET specifications. Note that per industry standards, the fall time of the drain-source voltage is called *rise time*.

7.1.2 Turn-off Delays

The timing of the turn-off transition is similarly broken into three components: propagation delay, turn-off delay and fall time. The first component is the propagation delay of the driver from when the input goes low to when the GaN FET starts turning off. The turn-off delay is the delay from when the FET starts turning of (represented by the drain rising above 10 V) to when the drain voltage swings up by 20 percent. Finally, the fall time is the time it takes the drain voltage to slew between 20 percent and 80 percent of the bus voltage. The turn-off delays of the LMG3410 are independent of the drive-strength resistor but the turn-off delay and the fall time are heavily dependent on the load current.

The propagation delay specification is comparable to MOSFET drivers while the turn-off delay and the fall time are comparable to the respective MOSFET specifications. Note that per industry standards, the rise time of the drain-source voltage is called *fall time*.

7.1.3 Drain Slew Rate

The slew rate, measured in volts per nanosecond, is measured on the turn-on edge of the LMG3410. The slew rate is considered over the rise time, where the drain falls from 80 percent to 20 percent of the bus voltage. The drain slew rate is thus given by 60 percent of the bus voltage divided by the rise time. This drain slew rate is dependent on the RDRV value and is only slightly affected by drain current.

7.1.4 Turn-on and Turn-off Energy

The turn-on and turn-off energy, shown in Figure 7, represent the energy absorbed by the low-side device during the turn-on and turn-off transients of the circuit in Figure 9, respectively. As this circuit represents a synchronous buck converter, with input shorted to output, the switching energy is dissipated in the low-side device. The turn-on transition is lossy, while the turn-off transition is essentially lossless; the output capacitance of the devices is charged by the inductor current. The turn-on and turn-off losses have been calculated from experimental waveforms by integrating the product of the drain current with the drain-source voltage over the turn-on and turn-off times, respectively.

The switching loss of the converter can be determined by adding the turn-on and turn-off energy in Figure 7, adjusting for the R_{DRV} value (shown in Figure 8). To obtain the switching loss, multiply this value by the switching frequency. The obtained loss is a sum of the V-I overlap loss (due to hard switching) and the loss caused by charging and discharging the C_{OSS} of both devices. Additional test-fixture capacitance, including PCB and inductor intra-winding capacitance, has not been removed from these measurements.

8 Detailed Description

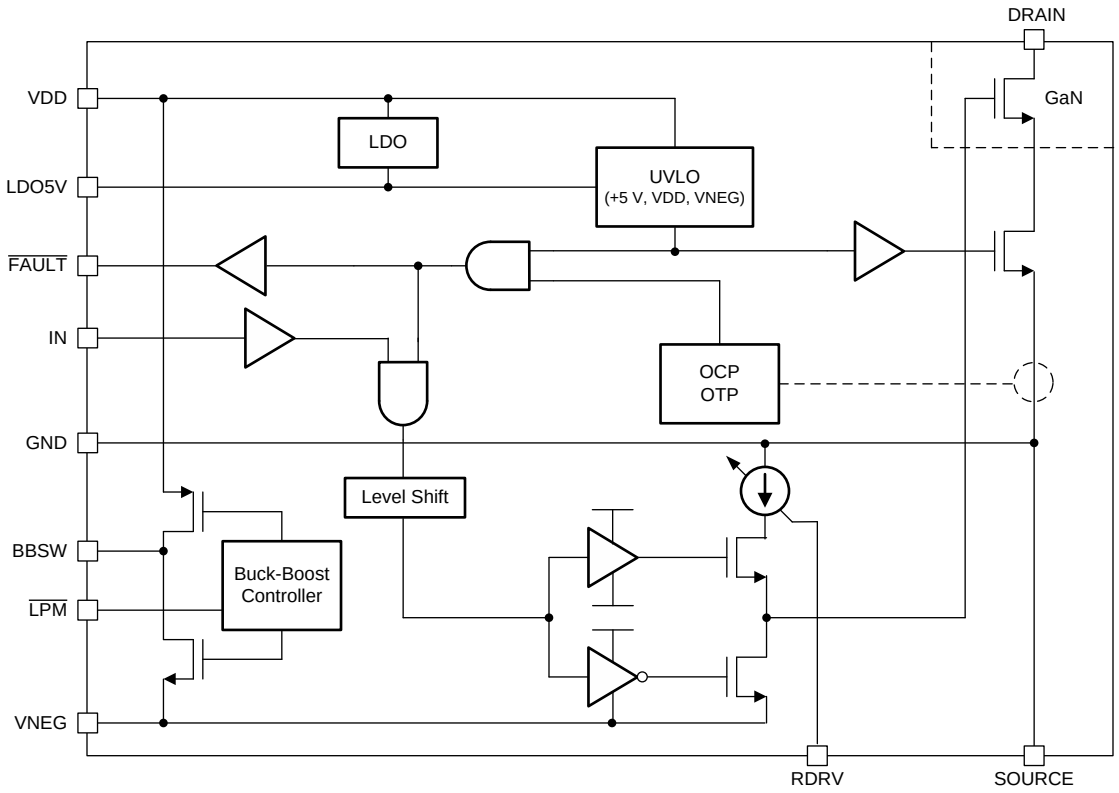
8.1 Overview

LMG3410 is a high-performance 600-V GaN transistor with integrated gate driver. The GaN transistor provides ultra-low input and output capacitance and zero reverse recovery. The lack of reverse recovery enables efficient operation in half-bridge and bridge-based topologies.

TI utilizes a Direct Drive architecture to control the GaN FET within the LMG3410. When the driver is powered up, the GaN FET is controlled directly with the integrated gate driver. This architecture provides superior switching performance compared with the traditional cascode approach.

The integrated driver solves a number of challenges using GaN devices. The LMG3410 contains a driver specifically tuned to the GaN device for fast driving without ringing on the gate. The driver ensures the device stays off for high drain slew rates up to 150 V/ns. In addition, the integrated driver protects against faults by providing over-current and over-temperature protection. This feature can protect the system in case of a device failure, or prevent a device failure in the case of a controller error or malfunction.

8.2 Functional Block Diagram



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8.3 Feature Description

The LMG3410 includes numerous features to provide increased switching performance and efficiency in customers' applications while providing an easy-to-use solution.

8.3.1 Direct-Drive GaN Architecture

The LMG3410 utilizes a series FET to ensure the GaN module stays off when V_{DD} is not applied. When this FET is off, the gate of the GaN transistor is held within a volt of the FET's source. This structure allows the LMG3410 to hold off voltage when the device is off by turning the GaN transistor off through its source. As the silicon FET blocks the drain voltage, the V_{GS} of the GaN transistor decreases until it passes its threshold voltage. Then, the GaN transistor turns off and blocks the remaining drain voltage.

When the LMG3410 is powered up, the internal buck-boost converter generates a negative voltage (V_{NEG}) that is sufficient to directly turn off the GaN transistor. In this case, the silicon FET is held on and the GaN transistor is gated directly with the negative voltage.

8.3.2 Internal Buck-Boost DC-DC Converter

An internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply of the GaN device. The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but may enter continuous-conduction mode during startup and overload conditions. The converter is controlled internally and requires only a single surface-mount inductor and output bypass capacitor. For recommendations on the required passives, see *Buck-Boost Converter Design*.

8.3.3 Internal Auxiliary LDO

An internal low-dropout regulator is provided to supply external loads, such as digital isolators for the high-side drive signal. It is capable of delivering up to 5 mA to an external load. A bypass capacitor with 1 µF typical is required for stability.

8.3.4 Fault Detection

The GaN driver includes built-in over-current protection (OCP), over-temperature protection (OTP) and under voltage lockout (UVLO).

The OCP circuit monitors the LMG3410's drain current through the integrated silicon MOSFET and compares that current signal with an internally-set limit. Upon actuation of the over-current detection circuit, the GaN FET is shut off and held off until power is reset or the fault is reset by holding the input low for more than 350 microseconds.

The over-temperature protection circuit measures the temperature of the driver die and trips if the temperature exceeds the over-temperature threshold (typically 165 °C). Upon an over-temperature condition, the GaN device is held off until temperature falls below the hysteresis limit, typically 15 degrees below the turn-off threshold.

The $\overline{\text{FAULT}}$ output is a push-pull output indicating the readiness and fault status of the driver. It is held low when starting up until the safety FET is turned on. In an OCP or OTP fault condition, it is held low until the fault latches are reset or fault is cleared. If the power supplies go below the UVLO thresholds, power transistor switching is disabled and $\overline{\text{FAULT}}$ is held low until the power supplies recover.

8.3.5 Drive Strength Adjustment

To allow for an adjustable slew rate to control stability and ringing in the circuit, as well as an adjustment to pass electro-magnetic compliance standards, LMG3410 allows the user to adjust its drive strength. A resistor is connected the RDRV pin and ground. The value of the resistor determines the slew rate of the device; see Figure 2 for the relationship between RDRV and the drain slew rate. The propagation delays vary with RDRV; consult Figure 1 for more details.

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8.4 Device Functional Modes

8.4.1 Low-Power Mode

In some applications, the primary-side power circuitry will be running off a high-voltage JFET until the converter has started. In this mode, it is important to dissipate little power. LMG3410 has a low-power mode (LPM) to enable the controller to start up before the part is enabled for switching.

The LMG3410 enters low-power mode when the $\overline{\text{LPM}}$ pin is pulled low. To enable standard operation of the LMG3410, the $\overline{\text{LPM}}$ must be pulled high. The supply current in the low-power mode is typically 80 µA. Once this pin is pulled high, the buck-boost converter will start up and LMG3410 will be ready to operate within 2 ms.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMG3410 is a single-channel GaN power stage targeting high-voltage applications. It targets hard-switched and soft-switched applications running from a 350 V to 480 V bus such as power-factor correction (PFC) applications. As GaN devices such as the LMG3410 have zero reverse-recovery charge, they are well-suited for hard-switched half-bridge applications, such as the totem-pole bridgeless PFC circuit. It is also well-suited for resonant DC-DC converters, such as the LLC and phase-shifted full-bridge. As both of these converters utilize the half-bridge building block, this section will describe how to use the LMG3410 in a half-bridge configuration.

9.2 Typical Application

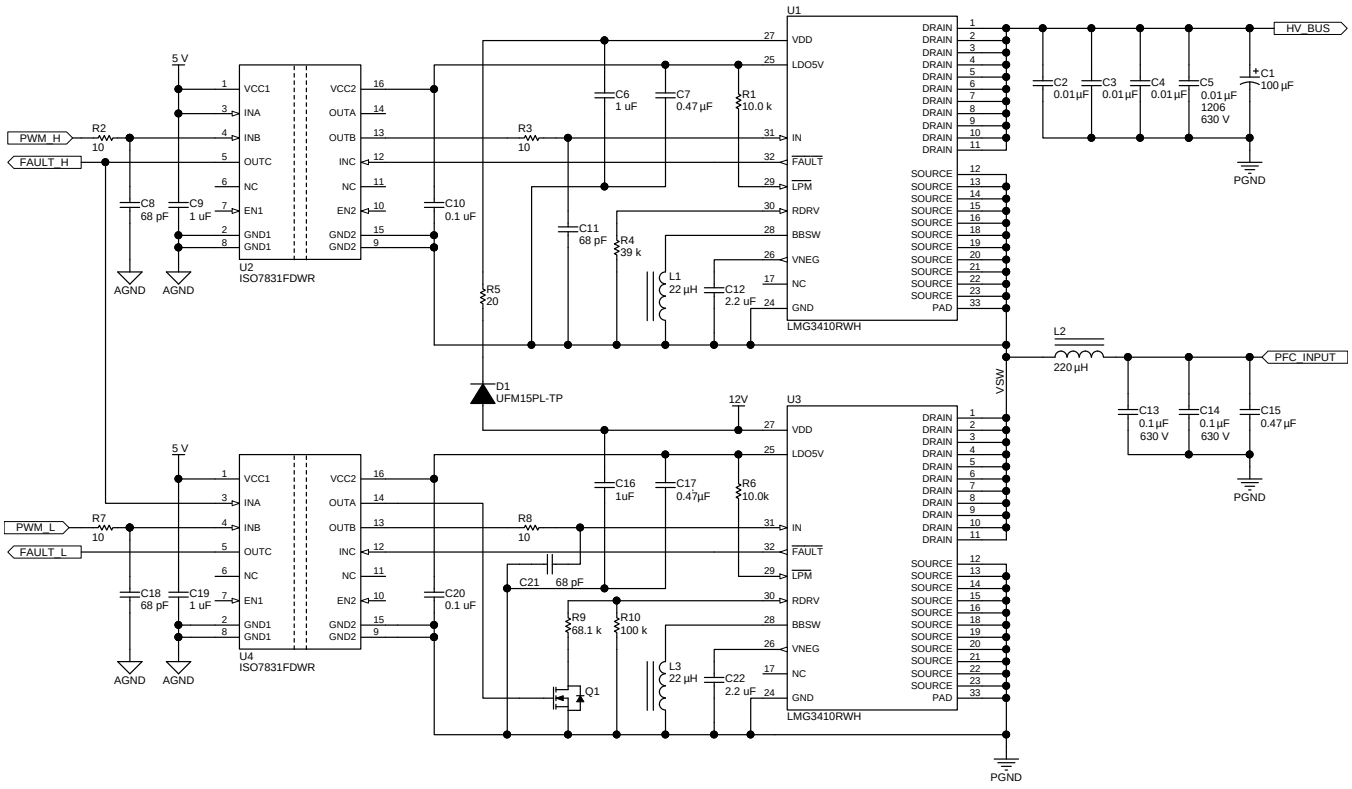

Figure 11. Typical Half-Bridge Application

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Typical Application (continued)

9.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. The system parameters considered are as follows.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	200 VDC
Output Voltage	400 VDC
Input (Inductor) Current	5 A
Switching Frequency	100 kHz

9.2.2 Detailed Design Procedure

In high-voltage power converters, correct circuit design and PCB layout is essential to obtaining a high-performance and even functional power converter. While the general procedure for designing a power converter is out of the scope of this document, this datasheet describes how to utilize the LMG3410 to build efficient, well-behaved power converters.

9.2.2.1 Slew Rate Selection

The LMG3410 supports slew rate adjustment through connecting a resistor from RDRV to GND. The choice of RDRV will control the slew rate of the drain voltage of the device between approximately 30 V/ns and 100 V/ns. The slew rate adjustment is used to control the following aspects of the power stage:

- Switching loss in a hard-switched converter
- Radiated and conducted EMI generated by the switching stage
- Interference elsewhere in the circuit coupled from the switch node
- Voltage overshoot and ringing on the switch node due to power loop inductance and other parasitics

When increasing the slew rate, the switching power loss will decrease, as the portion of the switching period where the switch simultaneous conducts high current while blocking high voltage is decreased. However, by increasing the slew rate of the device, the other three aspects of the power stage get worse. Following the design recommendations in this datasheet will help mitigate the system-related challenges related to high slew rate. Ultimately, it is up to the power designer to ensure the chosen slew rate provides the best performance in his or her end application.

9.2.2.1.1 Startup and Slew Rate with Bootstrap High-side Supply

Using a bootstrap supply for the high-side LMG3410 places additional constraints on the startup of the circuit. Before the high-side LMG3410 functions correctly, its VDD, LDO5V and VNEG power supplies must start up and be functional. Prior to the device powering up, the GaN device operates in cascode mode with reduced performance. In particular, under high drain slew rate (dv/dt), the transistor can conduct to a small extent and cause additional power dissipation. The correct startup procedure for a bootstrap-supplied half-bridge depends on the circuit used.

In a buck converter without pre-bias, where the initial output voltage is zero, the startup procedure is straightforward. In this case, before switching begins, turn on the low-side device to allow the high-side bootstrap transistor to charge up. When the $\overline{\text{FAULT}}$ signal goes high, the high-side device has powered up completely, and normal switching can begin.

In a boost converter or a buck converter with a pre-biased output, it is necessary to operate the circuit in switching PWM mode while the high-side LMG3410 is powering up. With a boost converter, if the low-side device is held on, the power inductor current will likely run away and the inductor will saturate. To start up a boost converter, the duty cycle has to be very low and gradually increase to charge the output to the desired value without the inductor current reaching saturation. This pulse sequence can be performed open-loop or using a current-mode controller. This startup mode is standard for boost-type converters.

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However, with the LMG3410, during the boost converter startup, significant shoot-through current can occur for high drain slew rates while starting up. This shoot-through current is approximately 1.25 µC per switching event at 50 V/ns, and is comparable to a reverse-recovery event. If this shoot-through current is undesirable, the drain slew rate of the low-side device must be reduced during startup. In Figure 11, the $\overline{\text{FAULT}}$ output from the high-side device is used to gate MOSFET Q1. When $\overline{\text{FAULT}}$ from the high-side is high, once the device is powered up, Q1 turns on and reduces the effective resistance connected to RDRV on the low-side LMG3410. With this circuit, the dv/dt of the low-side device can be held low to reduce power dissipation and reduce ringing during high-side startup, but then increase to reduce switching loss during normal operation.

9.2.2.2 Signal Level-Shifting

As the LMG3410 is a single-channel power stage, two devices are used to construct a half-bridge converter, such as the one shown in Figure 11. A high-voltage level shifter or digital isolator must be used to provide signals to the high-side device. Using an isolator for the low-side device is optional but will equalize propagation delays between the high-side and low-side signal path, as well as providing the ability to use different grounds for the power stage and the controller. If an isolator is not used on the low-side device, the control ground and the power ground must be connected at the LMG3410, as described in *Layout Guidelines*, and nowhere else on the board. With the high current slew rate of the fast-switching GaN device, any ground-plane inductance common with the power path may cause oscillation or instability in the power stage without the use of an isolator.

Choosing a digital isolator for level-shifting is an important consideration for fault-free operation. Because GaN switches very quickly, exceeding 50 V/ns in hard-switching applications, isolators with high common-mode transient immunity (CMTI) are required. If an isolator suffers from a CMTI issue, it can output a false pulse or signal which can cause shoot-through. In addition, choosing an isolator that is not edge-triggered can improve circuit robustness. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunctioning.

On/off keyed isolators are preferred, such as the TI ISO78xxF series, as a high CMTI event would only cause a short (few nanosecond) false pulse, which can be filtered out. To allow for filtering of these false pulses, an R-C filter at the driver input is recommended to ensure these false pulses can be filtered. If issues are observed, values of 1 kΩ and 22 pF can be used to filter out any false pulses.

9.2.2.3 Buck-Boost Converter Design

The Buck-boost converter generates the negative voltage necessary to turn off the direct-drive GaN FET. While it is controlled internally, it requires an external power inductor and output capacitor. The converter is designed to use a 22 µH inductor and a 2.2 µF output capacitor. As the peak current of the buck-boost is limited to less than 350 mA, the inductor chosen must have a saturation current above 350 mA. A Taiyo-Yuden BRC2518T220K 22 µH SMT inductor in a 0806 package is recommended. This inductor is connected between the BBSW pin and ground. A 2.2 µF, 25V 0805 bypass capacitor is required between V_{NEG} and ground. Due to the voltage coefficient of X7R capacitors, a 2.2 µF capacitor will provide the required minimum 1.0 µF capacitance when operating.

9.2.3 Application Curves

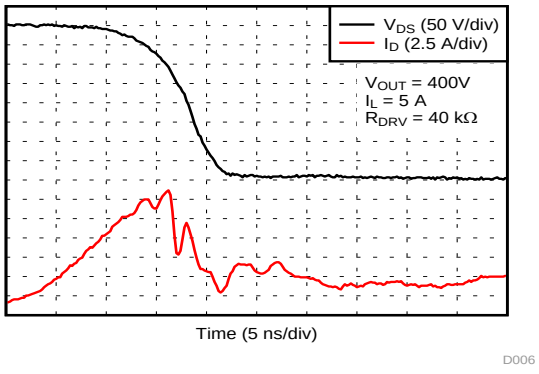

Figure 12. Turn-on Waveform in Application Example

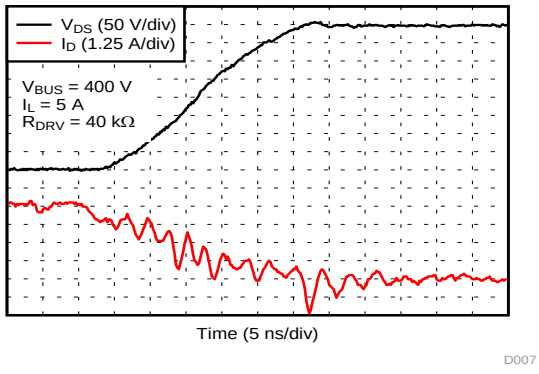

Figure 13. Turn-off Waveform in Application Example

9.3 Do's and Don'ts

The successful use of GaN devices in general and the LMG3410 in particular depends on proper use of the device. When using the LMG3410, **DO**:

- Read and fully understand the datasheet, including the application notes and layout recommendations
- Use a four-layer board and place the return power path on an inner layer to minimize power-loop inductance
- Use small, surface-mount bypass and bus capacitors to minimize parasitic inductance
- Use the proper size decoupling capacitors and locate them close to the IC as described in the *Layout Guidelines* section
- Use a signal isolator to supply the input signal for the low side device. If not, ensure the signal source is connected to the signal GND plane which is tied to the power source **only** at the LMG3410 IC
- Use the $\overline{\text{FAULT}}$ pin to determine power-up state and to detect over-current and over-temperature events and safely shut off the converter.

To avoid issues in your system when using the LMG3410, **DON'T**:

- Use a single-layer or two-layer PCB for the LMG3410 as the power-loop and bypass capacitor inductances will be excessive and prevent proper operation of the IC
- Reduce the bypass capacitor values below the recommended values
- Allow the device to experience drain transients above 600 V as they may damage the device
- Drive the IC from a controller with a separate ground connection than the GND pin of the IC
- Allow significant third-quadrant conduction when the device is OFF or unpowered, which may cause overheating
- Ignore the $\overline{\text{FAULT}}$ pin output.

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10 Power Supply Recommendations

The LMG3410 requires an unregulated 12-V supply to power its internal driver and fault protection circuitry. The low-side supply can be supplied from the local controller supply. The high-side device's supply must come from an isolated supply or bootstrap supply.

10.1 Using an Isolated Power Supply

Using an isolated power supply to power the high-side device has the advantage that it will work regardless of continued power-stage switching or duty cycle. It can also power the high-side device before power-stage switching begins, eliminating the power-loss concern of switching with an unpowered LMG3410 (see *Startup and Slew Rate with Bootstrap High-side Supply* for details). Finally, a properly-selected isolated supply will contribute fewer parasitics to the switching power stage, increasing power-stage efficiency. However, the isolated power supply solution is larger and more expensive than the bootstrap solution.

The isolated supply can be constructed from an output of a flyback or FlyBuck™ converter, or using an isolated power module. When using an unregulated supply, ensure that the input to the LMG3410 does not exceed the maximum supply voltage. If necessary, a 18 V zener to clamp the VDD voltage supplied by the isolated power converter. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications.

10.2 Using a Bootstrap Diode

When used in a half-bridge configuration, a floating supply is necessary for the top-side switch. Due to the switching performance of LMG3410, *a transformer-isolated power supply is recommended*. With caution, a bootstrap supply can be used with the recommendations in this section.

10.2.1 Diode Selection

LMG3410 has no reverse-recovery charge and little output charge. Hard-switched circuits using LMG3410 also exhibit high voltage slew rates. A compatible bootstrap diode must exhibit low output charge and, if used in a hard-switching circuit, very low reverse-recovery charge.

For soft-switching applications, the MCC UFM15PL ultra-fast silicon diode can be used. The output charge of 2.7 nC is small in comparison with the switching transistors, so it will have little influence on switching performance. In a hard-switching application, the reverse recovery charge of the silicon diode may contribute an additional loss to the circuit.

For hard-switched applications, a silicon carbide diode can be used to avoid reverse-recovery effects. The Cree C3D1P7060Q SiC diode has an output charge of 4.5 nC and a reverse recovery charge of about 5 nC. There will be some losses using this diode due to the output charge, but these will not dominate the switching stage's losses.

10.2.2 Managing the Bootstrap Voltage

In a synchronous buck, totem-pole PFC, or other converter where the low-side switch occasionally operates in third-quadrant mode, it is important to consider the bootstrap supply. During the dead time, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG3410. This third-quadrant drop can be large, which may over-charge the bootstrap supply in certain conditions. The V_{DD} supply of LMG3410 must not exceed 18 V in bootstrap operation.

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Using a Bootstrap Diode (continued)

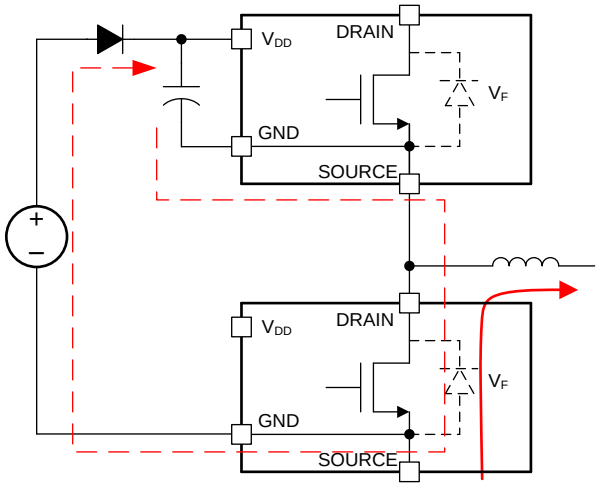


Figure 14. Charging Path for Bootstrap Diode

The recommended bootstrap supply connection includes a bootstrap diode and a series resistor with an optional zener as shown in Figure 15. The series resistor limits the charging current at startup and when the low-side device is operating in third-quadrant mode. This resistor must be chosen to allow sufficient current to power the LMG3410 at the desired operating frequency. At 100 kHz operation, a value of approximately 5.1 ohms is recommended. At higher frequencies, this resistor value should be reduced or the resistor omitted entirely to ensure sufficient supply current.

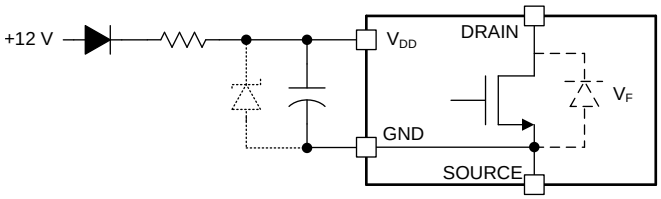


Figure 15. Suggested Bootstrap Regulation Circuit

Using a series resistor with the bootstrap supply will create a charging time constant in conjunction with the bypass capacitance on the order of a microsecond. When the dead time, or third-quadrant conduction time, is much lower than this time constant, the bootstrap voltage will be well-controlled and the optional zener clamp in Figure 15 will not be necessary. If a large deadtime is needed, a 14-V zener diode can be used in parallel with the V_{DD} bypass capacitor to prevent damaging the high-side LMG3410.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

The layout of the LMG3410 is critical to its performance and functionality. Because the half-bridge configuration is typically used with these GaN devices, layout recommendations will be considered with this configuration. A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance.

11.1.1 Power Loop Inductance

The power loop, comprising the two devices in the half bridge and the high-voltage bus capacitance, undergoes large *di/dt* during switching events. By minimizing the inductance of this loop, ringing and electro-magnetic interference (EMI) can be reduced, as well as reducing voltage stress on the devices.

This loop inductance is minimized by locating the power devices as close together as possible. The bus capacitance is positioned in line with the two devices, either below the low-side device or above the high-side device, on the same side of the PCB. The return path (PGND in this case) is located on the second layer on the PCB in close proximity to the top layer. By using an inner layer and not the bottom layer, the vertical dimension of the loop is reduced, thus minimizing inductance. A large number of vias near both the device terminal and bus capacitance carries the high-frequency switching current to the inner layer while minimizing impedance.

11.1.2 Ground Connection

The LMG3410 features a signal ground “GND” connection along with the source connection. The GND pin should be directly connected to SOURCE underneath the package on the PCB. In addition, the return path for the passives associated to the driver (e.g. bypass capacitance) must be connected to the GND plane. Isolate the GND plane from the high-current SOURCE plane except the connection at the GND pin and the thermal vias under the package. In Figure 16, local GND planes are located on the second copper layer to act as the return for the local circuitry.

11.1.3 Bypass Capacitors

The gate drive loop impedance must also be minimized to yield strong performance. Although the gate driver is integrated on package, the bypass capacitance for the driver is on board. As the GaN device is turned off to a negative voltage, the impedance of the negative source is included in the crucial turn-off path. As the critical hold-off path passes through this external bypass capacitor attached to V_{NEG}, this capacitor must be located close to the LMG3410. In the Figure 16, V_{NEG} bypass capacitors C12 and C22 are located immediately adjacent to the pins on the IC with a direct connection to the GND net.

The bypass capacitors for the input supply and the 5V regulator must also be located immediately next to the IC with a close connection to the ground plane.

11.1.4 Switch-Node Capacitance

GaN devices have very low output capacitance and switch quickly with a high *dv/dt*, yielding very low switching loss. To preserve this low switching loss, additional capacitance added to the output node must be minimized. The PCB capacitance at the switch node can be minimized by following these guidelines:

- Minimize overlap between the switch-node plane and other power and ground planes
- Thin the GND return path under the high-side device somewhat while still maintaining a low-inductance path
- Choose high-side isolator ICs and bootstrap diodes with low capacitance
- Locate the power inductor as close to the power stage as possible
- Power inductors should be constructed with a single-layer winding to minimize intra-winding capacitance
- If a single-layer inductor is not possible, consider placing a small inductor between the primary inductor and the power stage to effectively shield the power stage from the additional capacitance
- If a back-side heat-sink is used, restrict the switch-node copper coverage on the bottom copper layer to the minimum area necessary to extract the needed heat

Layout Guidelines (continued)

11.1.5 Signal Integrity

The control signals to the LMG3410 must be protected from the high *dv/dt* that the GaN power stage produces. Coupling between the control signals and the drain may cause circuit instability and potential destruction. Route the control signals (IN, $\overline{\text{FAULT}}$ and $\overline{\text{LPM}}$) over a ground plane located on an adjacent layer. For example, in the layout in Figure 16, all the signals are routed on the top layer directly over the GND plane on the first inner copper layer.

The signals for the high-side device are often particularly vulnerable. Coupling between these signals and system ground planes could cause issues in the circuit. Keep the traces associated with the control signals away from drain copper. For the high-side level shifter, ensure no copper from either the input or output side extends beneath the isolator or the device's CMTI may be compromised.

11.1.6 High-Voltage Spacing

Circuits using the LMG3410 involve high voltage, potentially up to 600V. When laying out circuits using the LMG3410, understand the creepage and clearance requirements in your application and how they apply to the power stage. Functional (or working) isolation is required between the source and drain of each transistor, and between the high-voltage power supply and ground. Functional isolation or perhaps stronger isolation (such as reinforced isolation) may be required between the input circuitry to the LMG3410 and the power controller. Choose signal isolators and PCB spacing (creepage and clearance) distances which meet your isolation requirements.

If a heatsink is used to manage thermal dissipation of the LMG3410, ensure necessary electrical isolation and mechanical spacing is maintained between the heatsink and the PCB.

11.1.7 Thermal Recommendations

LMG3410 may be used in applications with significant power dissipation, for example, hard-switched power converters. In these converters, cooling using just the PCB may not be sufficient to keep the part at a reasonable temperature. To improve the thermal dissipation of the part, TI recommends a heatsink is connected to the back of the PCB to extract additional heat. Using power planes and numerous thermal vias, the heat dissipated in the LMG3410(s) can be spread out in the PCB and effectively passed to the other side of the PCB. A heat sink can be applied to bare areas on the back of the PCB using an adhesive thermal interface material (TIM). The soldermask from the back of the board underneath the heatsink can be removed for more effective heat removal.

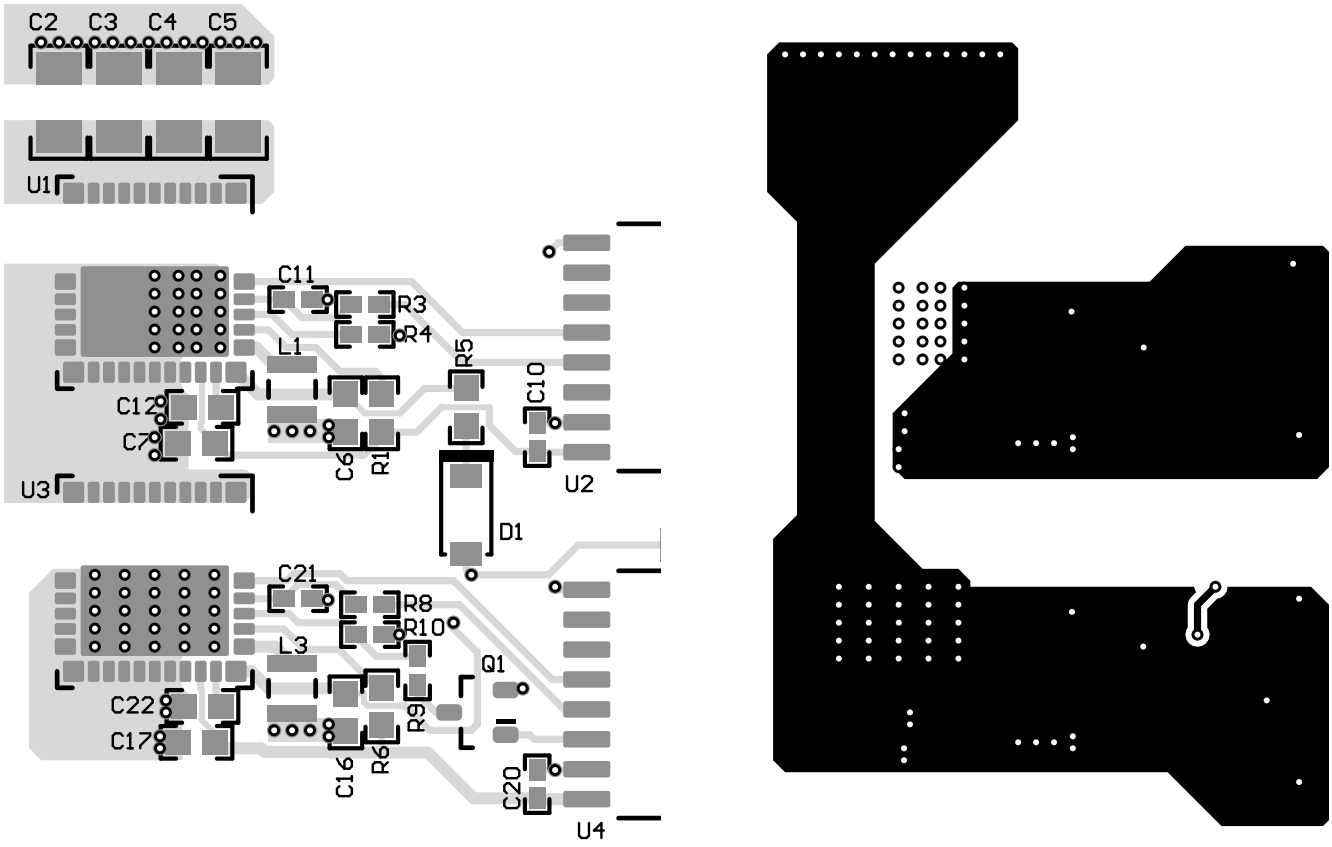
Please refer to the *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* application note for more recommendations and performance data on thermal layouts.

11.2 Layout Example

Correct layout of the LMG3410 and its surrounding components is essential for correct operation. The layout shown here reflects the power stage schematic in Figure 11. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

ADVANCE INFORMATION

Layout Example (continued)



Components and Top Copper **Mid Copper**

Figure 16. Example Half-Bridge Layout

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET application note.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

FlyBuck, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

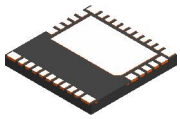
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

LMG3410 is targeted to release as MSL3. Products that exceed their floor life can be re-worked with a bake to drive out residual moisture. IPC/JEDEC J-STD-033C provides guidance about the baking procedure and where you should take care to ensure that the plastic housing (trays, tape and reel or tubes) can withstand the temperatures being considered.

ADVANCE INFORMATION

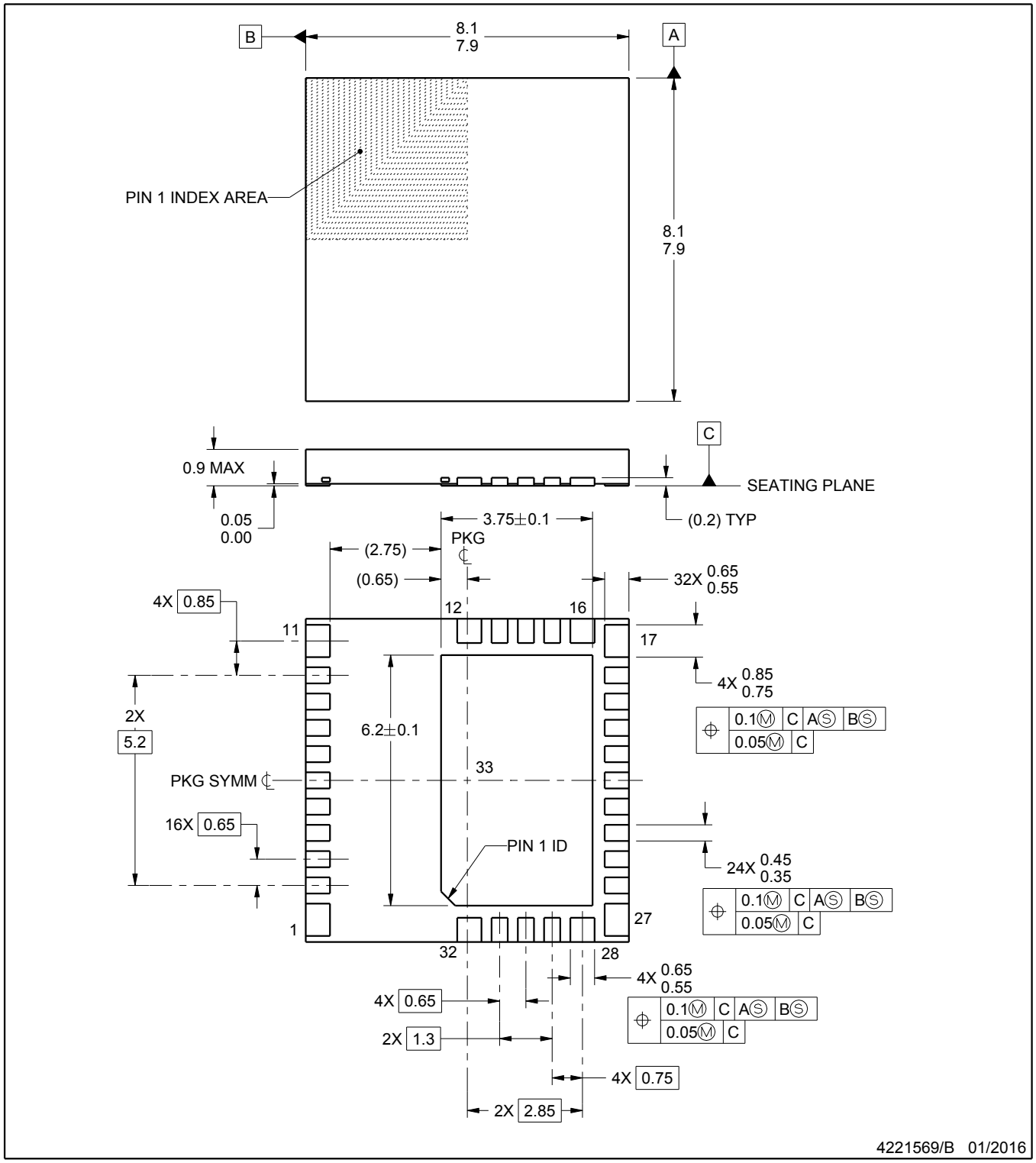


PACKAGE OUTLINE

RWH0032A

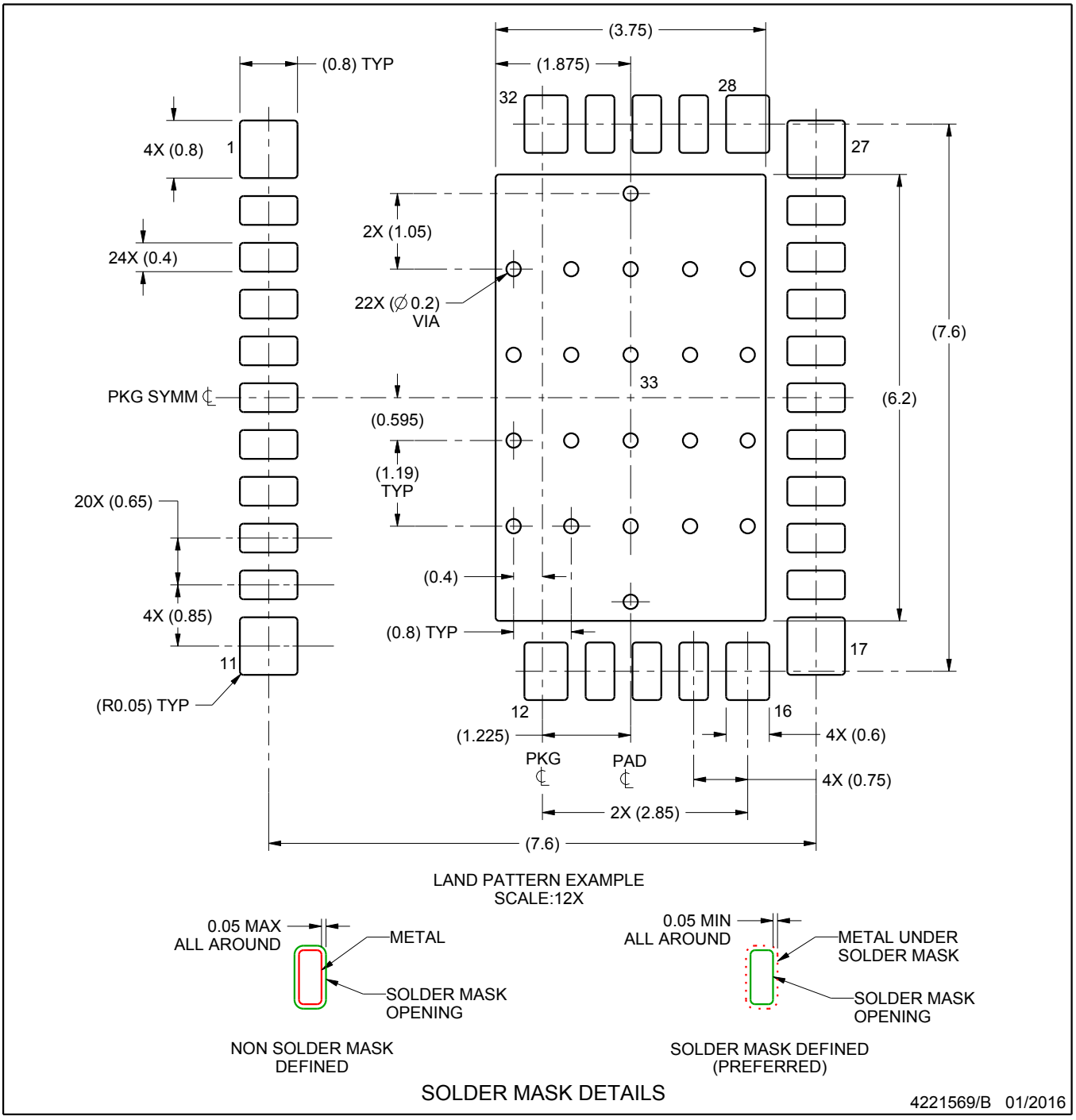
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



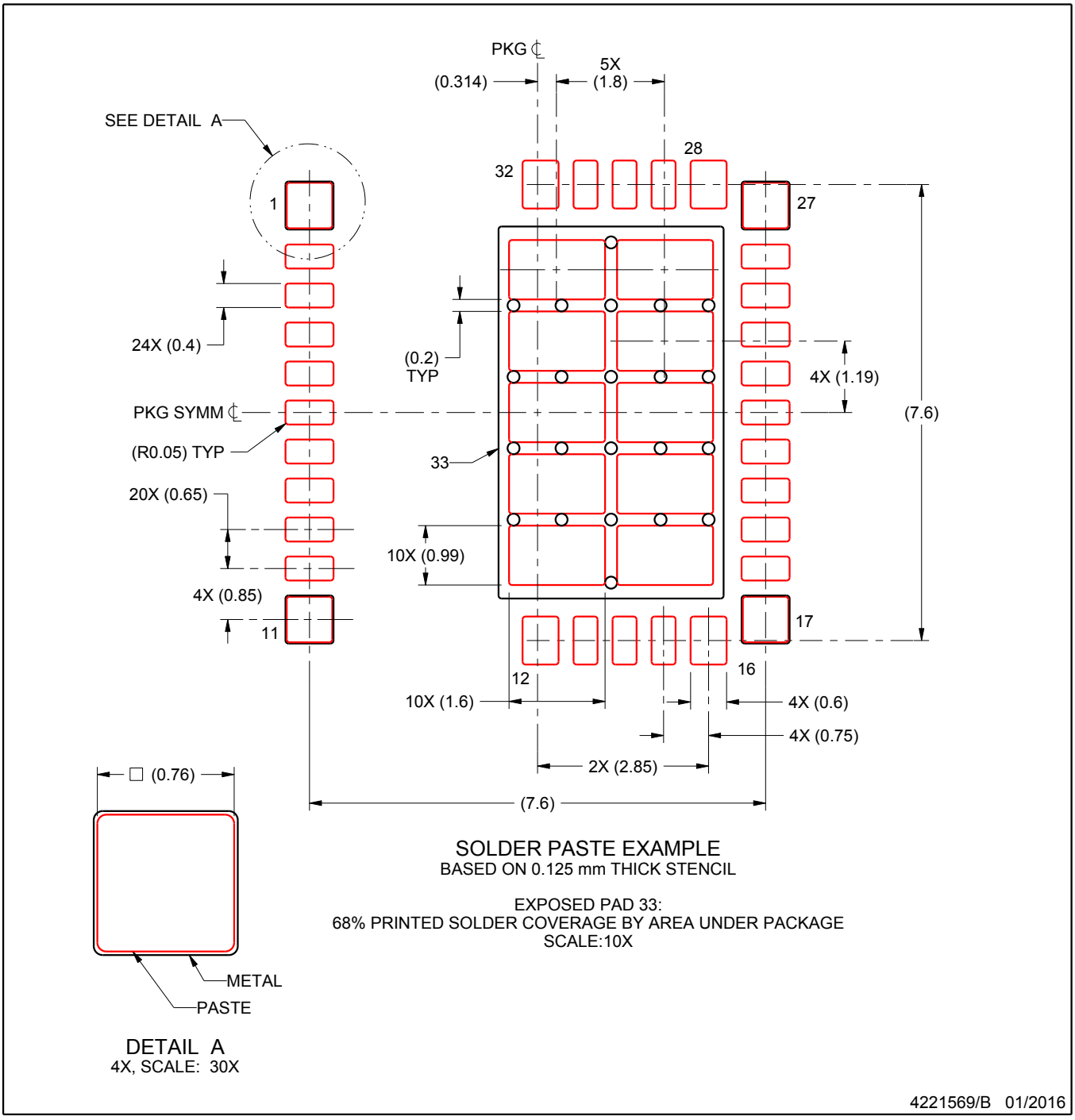
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XLMG3410RWHT	ACTIVE	VQFN	RWH	32	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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