TPIC2060A 用于 ODD、由串行接口控制的 9 通道电机驱动器

1 特性

- 串行端口数字接口
  - 串行外设接口 (SPI)
  - 4 线接口：SSZ、SCLK、SIMO、SOMI
  - 最大读写频率 35MHz
  - 3.3V 数字输入输出 (I/O)
- 执行器和电机驱动器
  - 具有 H 桥输出的脉冲宽度调制 (PWM) 控制
  - 具有 12 位数模转换器 (DAC) 控制的聚焦/跟踪/倾斜执行器驱动器
  - 具有电流模式、10 位 DAC 控制的滑动电机驱动器
  - 具有 12 位 DAC 控制的负载驱动器
  - 具有 8 位 PWM 控制的步进电机驱动器
- 主轴电机驱动器
  - 集成有电流感测电阻
  - 可通过寄存器集更改电流限值
  - 无传感器：通过电机反电动势 (BEMF) 感测转子位置
  - 通过串行端口编程设定的 12 位主轴 DAC
  - 独立的感应位置感测和启动
  - 通过自动控制制动实现急停：主动制动和短制动
  - 最大持续电流为 1.5A，不存在散热问题
  - 0.35Ω 低导通电阻、典型金属氧化物半导体场效应晶体管 (MOSFET) 输出
- 实用功能
  - 状态锁存器：执行器定时器、SIF 错误、电源监视器、热保护和短路保护 (SCP) 故障
  - 片上温度计（15°C 至 165°C/1.2°C）
- 9V LDO
  - 9V LDO 集成有前置驱动器
  - 根据电流要求选择外部 N 沟道场效应晶体管 (NFET)
  - 通过串行控制使能
- 保护
  - 同步永磁电机 (SPM)、滑动电机、步进准直透镜和执行器上均配有独立热保护电路
  - 两个警报级别：热保护中的预检测和检测
  - ACTTEMP：监视由过去累积的 DAC 值计算得出的执行器温度
  - SPM、滑动电机、负载、步进驱动器和执行器通道中具有短路保护
  - 硬件器件禁用引脚 XRSTIN
  - 具有欠压锁定 (UVLO) 和过压保护 (OVP) 的电源监视器
- 负载机制支持：
  - 滑动电机和步进电机通道中具有独立的端点检测机制
  - 托盘锁定检测
  - 检测托盘推事件

2 应用

光盘驱动器（Blu-ray™、数字化视频光盘 (DVD)、光盘 (CD)）

3 说明

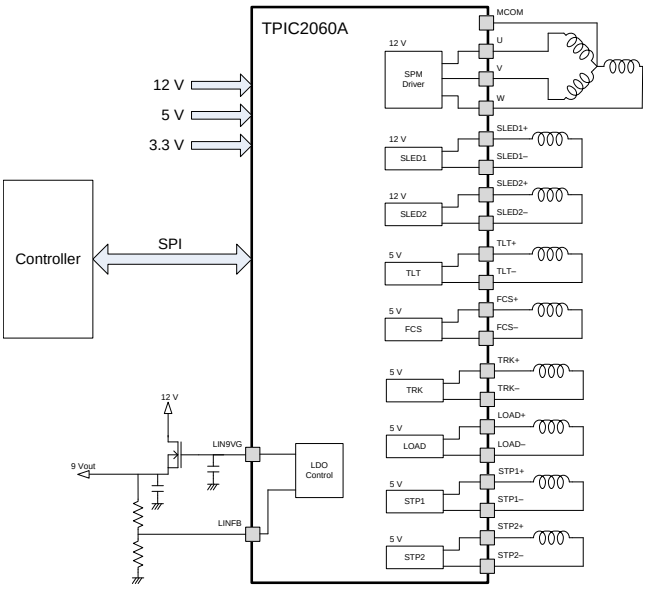
TPIC2060A 是一款适用于 12V ODD 的超低噪声电机驱动器集成电路 (IC)。该驱动器 IC 有 9 条通道且由串行接口控制，非常适用于驱动主轴电机、滑动电机（适用的步进电机）、负载电机以及针对准直透镜的聚焦/跟踪/倾斜执行器和步进电机。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPIC2060A	HTSSOP (56)	6.10mm x 14.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

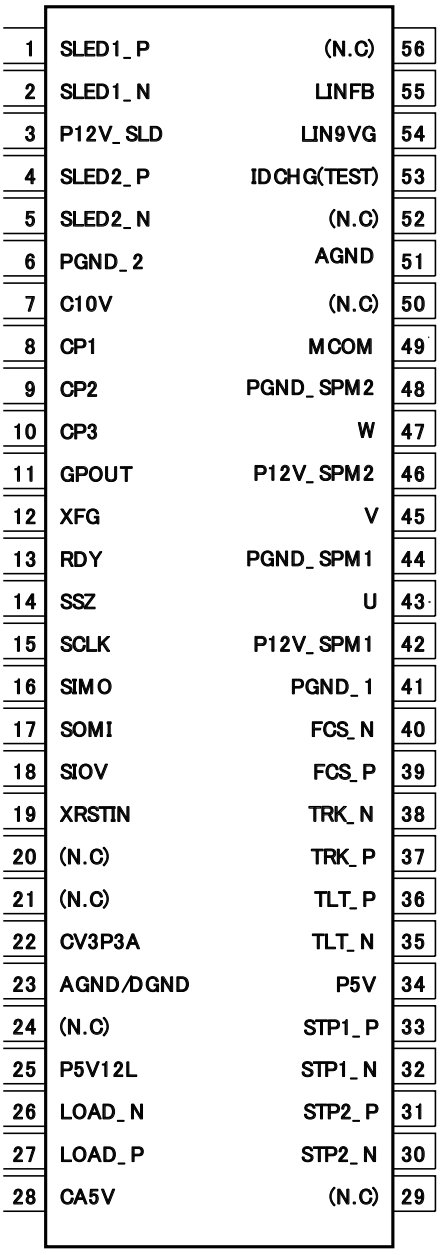
日期	修订版本	注释
2015 年 7 月	*	最初发布。

5 说明 （续）

该 IC 集成有电流感测电阻，能够测量 SPM 电流并降低驱动系统成本。主轴电机驱动器部分内置无传感器逻辑，可确保以低噪声启动和运行。用户无需使用启动电路使器件自启动或者通过电机或传感器（例如霍尔器件）的 BEMF 执行位置检测。由于所有通道的输出级均在高效的 PWM 驱动下工作，用户可通过 PWM 控制实现低功率运行。可以对聚焦/跟踪/倾斜执行器驱动器进行无死区控制。此外，该器件还内置有主轴部件输出电流限制电路、热关断电路、滑动结束位置检测电路、准直透镜结束检测电路、执行器保护和 9V LDO 的前置驱动器。新增的内置温度计可测量 IC 温度。

6 Pin Configuration and Functions

DFD Package
56-Pin HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	51	PS	Ground terminal for internal analog
AGND/DGND	23	PS	Ground terminal for internal digital and analog
CA5V	28	MISC	The capacitance connection terminal for control system power supply. Connect a 0.1-µF or lager decoupling capacitor.
CP1	8	MISC	Capacitance connections for charge pump
CP2	9		
CP3	10		
CV3P3	22	MISC	Capacitance terminal for internal 3.3-V core (typ 0.1 µF)
FCS_P	39	OUT	Focus positive output terminal
FCS_N	40	OUT	Focus negative output terminal
GPOUT	11	OUT	General-purpose output (test monitor)
IDCHG(TEST)	53	—	Test pin (leave open)
LIN9VG	54	—	9-V predriver output control signal for external NFET
LINFB	55	—	Voltage feedback of 9-V pre-driver (controlled to LINFB = 1.215 V)
LOAD_N	26	OUT	Load negative output terminal
LOAD_P	27	OUT	Load positive output terminal
MCOM	49	IN	Motor center tap connection
(N.C)	20, 21, 24, 29, 50, 52, 56	—	Leave open
P12V_SLD	3	PS	Power supply terminal for SLED drivers
P12V_SPM1	42	PS	Power supply terminal for SPM driver output stage
P12V_SPM2	46	PS	Power supply terminal for SPM driver output stage
P5V	34	PS	Power supply terminal for 5-V driver output
P5V12L	25	PS	Power supply terminal (5 or 12 V) for load driver output stages
PGND_1	41	PS	GND terminal
PGND_2	6	PS	GND terminal
PGND_SPM1	44	PS	Ground terminal for spindle driver
PGND_SPM2	48	PS	Ground terminal for spindle driver
RDY	13	OUT	Device ready signal internally pulled up to SIOV
SCLK	15	IN	SIO Serial clock input terminal
SIMO	16	IN	SIO slave input master output terminal
SIOV	18	PS	Power supply terminal for serial port 3.3 V typical
SLED1_N	2	OUT	Sled1 negative output terminal
SLED1_P	1	OUT	Sled1 positive output terminal
SLED2_N	5	OUT	Sled2 negative output terminal
SLED2_P	4	OUT	Sled2 positive output terminal
SOMI	17	OUT	SIO slave output master input terminal
SSZ	14	IN	SIO slave select active-low input terminal
STP1_N	32	OUT	STP1 negative output terminal for collimator lens motor
STP1_P	33	OUT	STP1 positive output terminal for collimator lens motor
STP2_N	30	OUT	STP2 negative output terminal for collimator lens motor
STP2_P	31	OUT	STP2 positive output terminal for collimator lens motor
TLT_N	35	OUT	Tilt negative output terminal
TLT_P	36	OUT	Tilt positive output terminal
TRK_P	37	OUT	Tracking positive output terminal
TRK_N	38	OUT	Tracking negative output terminal
U	43	OUT	U phase output terminal for spindle motor

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V	45	OUT	V phase output terminal for spindle motor
W	47	OUT	W phase output terminal for spindle motor
XFG	12	OUT	Motor speed signal output, internally pulled up to SIOV
XRSTIN	19	IN	RESET input terminal to reset the driver IC (optional)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
	5-V supply voltage P5V		6	V
	12-V supply voltage P12V		15	
	Load supply P5V12 voltage		15	
	Spindle output peak voltage		15	
	Spindle output current		2.5	A
	Spindle output peak current、(PW ≤ 2 ms、Duty ≤ 30%)		3.5	
	Sled output peak current		1.0	
	Focus/tracking/tilt driver output peak current		1.0	
	Load driver output peak current		1.0	
	Input/output voltage	–0.3	V_{CC} + 0.3	V
	Power dissipation (2)		1344	mW
	Operating temperature	–20	75	°C
	Lead temperature 1.6 mm from case for 10 s		260	
T_{stg}	Storage temperature	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A lower $R_{\theta JC}$ is attainable if the exposed pad is connected to a large copper ground plane. $R_{\theta JC}$ and $R_{\theta JA}$ are values for 56-pin TSSOP without a exposed heat slug (HSL) on bottom. Actual thermal resistance would be better than the above values.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating supply voltage (apply for P5V)	4.5	5.0	5.5	V
Driver 12-V supply voltage (apply for P12V)(1)	10.8	12.0	13.2	
Load operating supply voltage (apply for P5V12L)	4.5	5.0	5.5	
	10.8	12.0	13.2	
SIOV voltage	3.0	3.3	3.6	
Operating temperature range	–20	25	75	°C
SCLK frequency	30	33.8688	35	MHz
SIMO, SSZ, SCLK pin 'H' level input voltage range	2.2		SIOV + 0.2	V
SIMO, SSZ, SCLK pin 'L' level input voltage range	–0.2		0.8	
XRSTIN pin 'H' level input voltage	2.2		P5V + 0.1	
XRSTIN pin 'L' level input voltage range	–0.1		0.8	
Spindle output current (U, V, W average total)			1.7	A
Spindle output current [peak]			3.0	
Focus / tracking / tilt / loading / sled output current [average]			0.4	
Focus / tracking / tilt / loading / sled output current [peak]			0.8	
STP output average current		300		mA

(1) (P5V = 4.5 to 5.5 V, P12V = 10.8 to 13.2 V, CATA ≈ –20℃ to 75℃, unless otherwise noted)

7.4 Thermal Information

THERMAL METRIC(1)		TPIC2060A DFD (HTSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.9	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PART						
I_{STBY}	Stand by supply current	Standby mode (XSLEEP = 0)		0.6	1.2	mA
V_{CV3}	CV3P3 output voltage	Iload = 25 mA	3.1	3.3	3.5	V
R_{XM}	XRSTIN pulldown resistor		80	200	320	kΩ
R_{RDY}	RDY pullup resistor		13.2	33	52.8	
V_{RDY}	RDY low level output voltage	SIOV = 3.3 V, IOL = –100 µA			0.3	V
R_{XFG}	XFG output resistor		100	200	300	Ω
V_{XFGH}	XFG high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, IOH = 100 µA	SIOV – 0.3			V
V_{SFGL}	XFG low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, IOL = -100 µA			0.3	
R_{GPO}	GPOUT output resistor		100	200	300	Ω
V_{GPOH}	GPOUT high-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1,GPOUT_HL = 1, IOH = 100 µA	SIOV – 0.3			V
V_{GPOL}	GPOUT low-level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1,GPOUT_HL = 0, IOH = 100 µA			0.3	V
T_{TSD}	Thermal protection on temperature	Design value	135	150	165	°C
T_{TSDhys}	Thermal protection hysteresis temperature		5	15	25	
V_{onvcc}	P5V reset on voltage		3.6	3.7	3.8	V
V_{offvcc}	P5V reset off voltage		3.6	3.8	4.0	
V_{onvcc}	P12V reset on voltage		7.9	8.4	8.9	
V_{offvcc}	P12V reset off voltage		8.3	8.8	9.3	
V_{onCV3}	CV3P3 reset on voltage		2.55	2.7	2.85	
V_{offCV3}	CV3P3 reset off voltage		2,65	2,8	2,95	
V_{onSIOV}	SIOV reset on voltage (1)		1.9	2	2.1	
$V_{offSIOV}$	SIOV reset off voltage (1)		2	2.1	2.2	
$V_{ovpspmOn}$	OVP detection voltage (spindle)(1)		14.2	14.9	15.6	
$V_{ovpspmOff}$	OVP release voltage (spindle)(1)		13.8	14.5	15.2	
V_{ovpOn}	OVP detection voltage (except spindle) (1)		5.9	6.2	6.5	
V_{ovpOff}	OVP release voltage (except spindle) (1)		5.7	6.0	6.3	
CHARGE PUMP PART						
F_{CHGP}	Frequency	XSLEEP = 1	132.6	156	179.4	kHz
V_{CHGP}	Output voltage	Ccp1 = Ccp3 = 0.1 µF Io = –1 mA	15.6	18.5	21.4	V
SPINDLE MOTOR DRIVER PART						
R_{ttlSPM}	Total output resistance high side + low side	IOUT = 500 mA		0.4	0.7	Ω
ResSPM	Resolution			12		bit
VoutSPM	Spindle grain	Magnification to 1.0 inputs	12.4	14.0	15.6	times
WidDZSPM	Spindle dead band	Forward	12h	52h	92h	
		Reverse	–92h	–52h	–12h	

(1) These values are protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPMClim	Current limit	SPM_RCOM_SEL = 00 SPM_TQAJST = 00	1019.7	1133	1246.3	mA
		SPM_RCOM_SEL = 01 SPM_TQAJST = 00	694.8	772	849.2	
		SPM_RCOM_SEL = 10 SPM_TQAJST = 00	1274.4	1416	1557.6	
		SPM_RCOM_SEL = 11 SPM_TQAJST = 00	1530.0	1700	1870.0	
SPMClimF	Current limit fine adjust	SPM_RCOM_SEL = xx SPM_TQAJST = 01	–4%	–5%	–6%	
		SPM_RCOM_SEL = xx SPM_TQAJST = 10	–8%	–10%	–12%	
		SPM_RCOM_SEL = xx SPM_TQAJST = 11	–12%	–15%	–18%	
SLED MOTOR DRIVER PART						
R_{ttlSLD}	Total output resistance high side + low side	P12 V = 10.8 to 13.2 V, IO = 500 mA		1.6	2.5	Ω
ResSLD	Resolution			10		bit
WidDZSLD	input dead band	Forward		+1Fh		
		Reverse		–20h		
G_{nSLD}	Sled current gain	P5V = 5 V,P12V = 12 V VSLED = 7FFh	760	880	1000	mA
$V_{thEdetSLD}$	END_DET BEMF threshold voltage	SLD_ENA = 1, SLD_ENDDET_ENA = 1, SLEDENDTH <1:0> = 00	62	124	186	mV
		SLEDENDTH<1:0> = 01	35	72	105	
		SLEDENDTH<1:0> = 11	80	168	250	
FOCUS/TILT/TRACKING DRIVER PART						
R_{ttlAct}	Each channel total output resistance high side + low side	P5V = 4.5 to 5.5 V、IO = 500 mA		0.7	1.1	Ω
ResACT	Resolution			12		bit
$V_{OfstACT}$	Each channel output offset voltage	DAC_code = 000h	–20	0	20	mV
G_{nAct}	Each channel voltage gain	Magnification to 1.0 inputs	5	6	7	times
DifOff	FCS, TLT differential output offset voltage	DIFF_TLT = 1, FCS-TLT	–40	0	40	mV
G_{nDAct}	FCS, TLT differential gain ratio	DIFF_TLT = 1, FCS-TLT (Typ = 1)	0.89	1	1.13	
LOAD DRIVER PART						
R_{ttlLOD}	Total output resistance high side + low side	P5V12L = 4.5 V to 5.5 V、IO = 500 mA		1.2	1.9	Ω
		P5V12L = 10.8 V to 13.2 V、IO = 500 mA				
ResLOD	Resolution			12		bit
G_{nLOD}	Voltage gain	P5V12L = 4.5 to 5.5 V	5.1	6.0	6.9	times
		P5V12L = 10.8 to 13.2 V	12.6	14.0	15.4	
WidDZLOD	Dead band	Forward		20h		
		Reverse		–21h		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LockDth	Tray lock detect threshold current	P5V12L = 5 V, TRAY_LOCKDET[2:0] = 1	80	100	120	mA
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 1	80	100	120	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 2	120	150	180	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 2	120	150	180	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 3	160	200	240	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 3	160	200	240	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 4	212	250	287	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 4	212	250	287	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 5	255	300	345	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 5	255	300	345	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 6	297	350	402	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 6	297	350	402	
		P5V12L = 5 V, TRAY_LOCKDET[2:0] = 7	340	400	460	
		P5V12L = 12 V, TRAY_LOCKDET[2:0] = 7	340	400	460	
PushDVth	Tray push detect voltage threshold	LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH[1:0] = 01	0.8	1.0	1.2	V
		LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH[1:0] = 10	0.52	0.75	0.96	
		LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH[1:0] = 11	0.27	0.5	0.63	
PushDTth	Tray push detect time threshold	LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH_TIME[1:0] = 00	78	104	130	ms
		LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH_TIME[1:0] = 01	156	208	260	
		LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH_TIME[1:0] = 10	312	416	520	
		LOAD_ENA = 0, P5V12L = 12V, PUSHDETTH_TIME[1:0] = 11		0	25	
STEPPING MOTOR DRIVER PART						
R_{ttlSTP}	Total output resistance high side + low side	IO = 100 mA		1.0	1.5	Ω
ResSTP	Resolution			8		bit
$V_{thEdetSTP}$	END_DET threshold level	STP_ENA = 1, STP_ENDDET_ENA = 1, STPDENDTH<1:0> = 00	19	39	59	mV
9-V LDO DRIVER PART						
LINFBVth	LINFB threshold voltage		1.165	1.215	1.265	V
THERMOMETER PART						
ResTEMP	Resolution			7		bit

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{rng}	Temperature range	CHIPTEMP[6:0] = 00	8	15	22	°C
		CHIPTEMP[6:0] = 7Fh	155	165	175	
F_{TEMP}	Update cycle			10		kHz
ACTUATOR PROTECTION						
$t_{intACTTEMP}$	Update cycle			26		ms
SERIAL PORT VOLTAGE LEVELS						
SOMI	High-level output voltage, VOH	IOH = 1 mA	80% SIOV			V
SOMI	Low-level output voltage, VOL	IOL = 1 mA			20% SIOV	
SIMO	High-level input voltage, VIH		70% SIOV			
SIMO	Low level input voltage, VIL				20% SIOV	
t_{SIMO}	Input rise/fall time	20% to 80% of SIOV			3.5	ns
t_{SOMI}	Output rise/fall time	Cload = 30 pF, 20% to 80% of SIOV			10	
R_{SCLK}	Internal pulldown resistance		80	200	320	kΩ
R_{SSZ}	Internal pullup resistance		80	200	320	
R_{SIMO}	Internal pulldown resistance		80	200	320	

7.6 Serial I/F Write Timing Requirements

		MIN	NOM	MAX	UNIT
f_{ck}	SCLK clock frequency (SIOV = 3.3 V)			35	MHz
t_{ckl}	SCLK low time	11			ns
t_{ckh}	SCLK high time	11			ns
t_{sens}	SSZ setup time	7			ns
t_{senh}	SSZ hold time	7			ns
t_{sl}	SSZ disable high time	11			ns
t_{ds}	SIMO setup time (Write)	7			ns
t_{dh}	SIMO hold time (Write)	7			ns

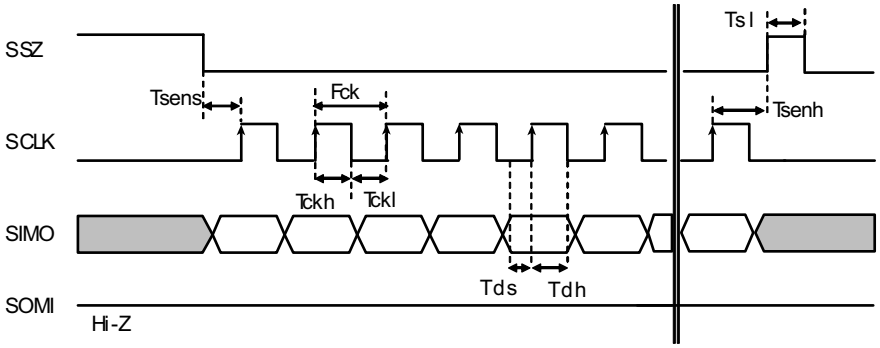


Figure 1. Serial Port Write Timing

7.7 Serial I/F Read Timing Requirements

		MIN	NOM	MAX	UNIT
f_{ck}	SCLK clock frequency (SIOV = 3.3 V)			35	MHz
t_{ckl}	SCLK low time	11			ns
t_{ckh}	SCLK high time	11			ns
t_{sens}	SSZ setup time	7			ns
t_{senh}	SSZ hold time	7			ns
t_{sl}	SSZ disable high time	11			ns
t_{ds}	SIMO setup time (Write)	7			ns
t_{dh}	SIMO hold time (Write)	7			ns
t_{rdly}	SOMI delay time (Read) - (CLOAD = 10 pF, SIOV = 3.3 V)	2		9	ns
t_{sendl}	SOMI hold time (Read) - (CLOAD = 10 pF, SIOV = 3.3 V)	2		9	ns
t_{rls}	SOMI release time (Read) - (CLOAD = 10 pF, SIOV = 3.3 V) From SSZ rise to SOMI HIZ	0		9	ns

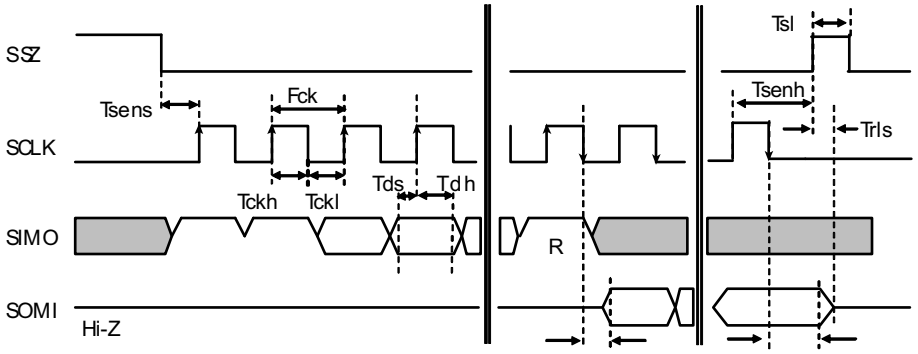


Figure 2. Serial Port Read Timings

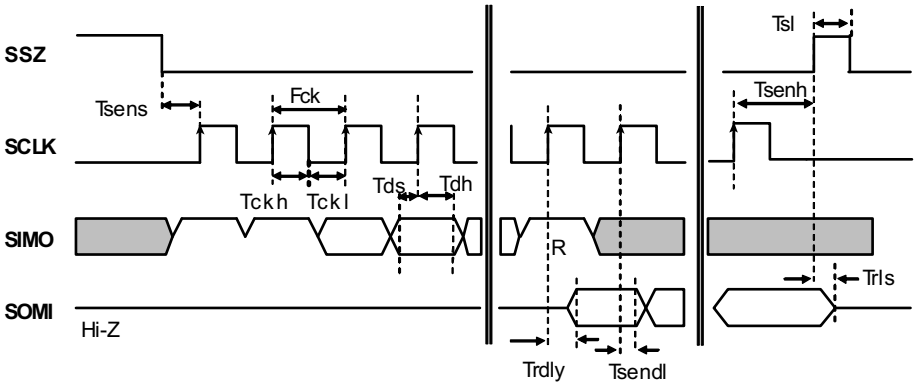


Figure 3. Serial Port Read Timings (Advanced Read Mode)

7.8 Typical Characteristics

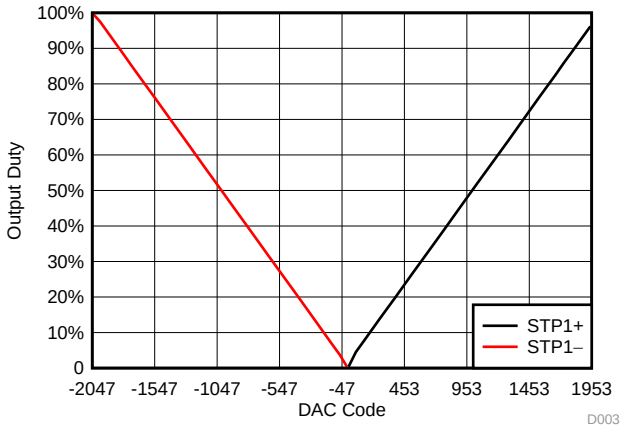


Figure 4. STP1 Driver: DAC Code vs Output On Duty

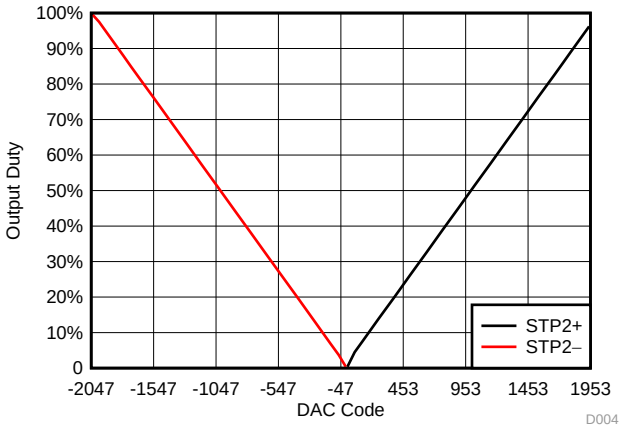


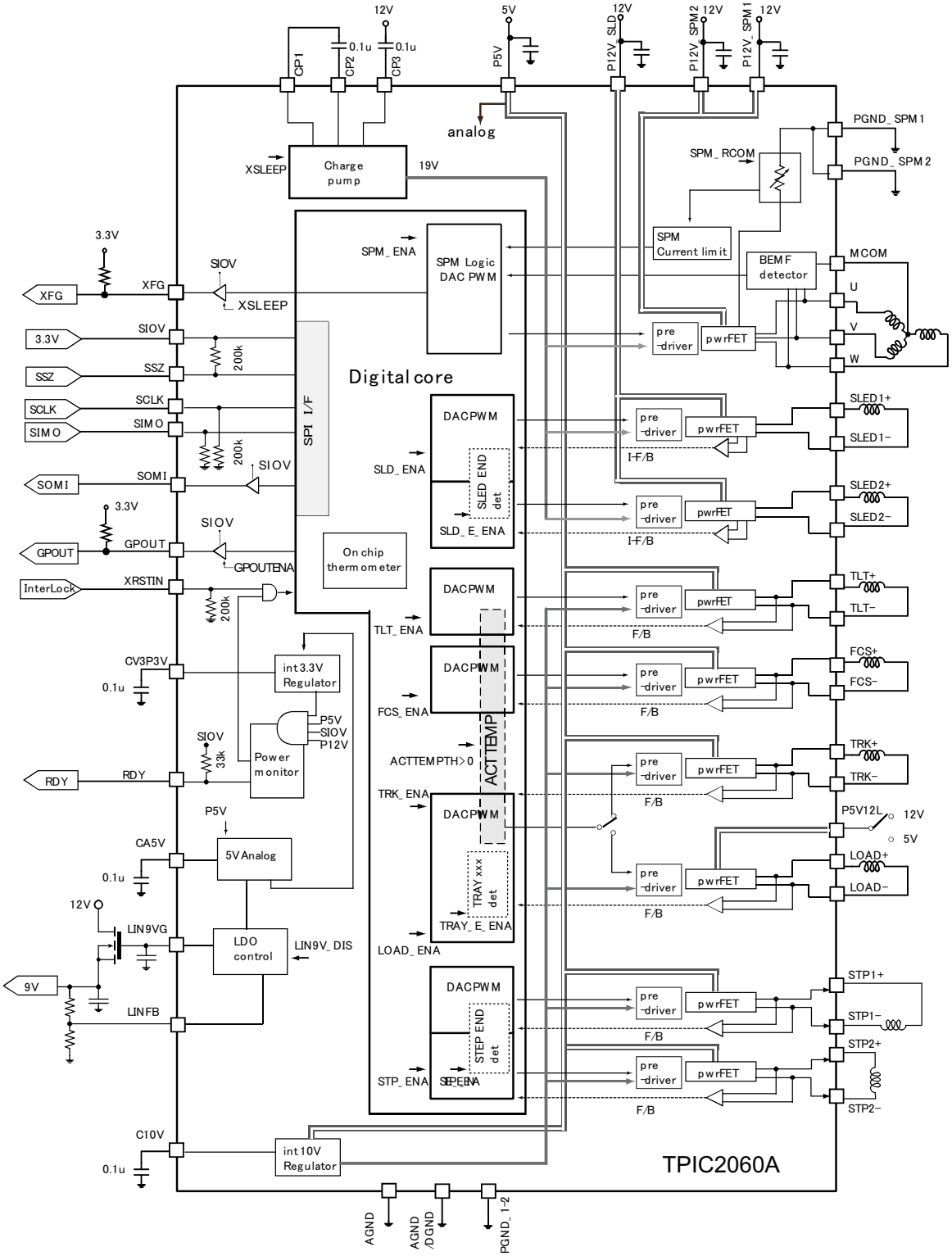
Figure 5. STP2 Driver: DAC Code vs Output On Duty

8 Detailed Description

8.1 Overview

The TPIC2060A is a low-noise motor driver IC suitable for 12-V ODD. The 9-channel driver IC controlled by a serial interface is optimized for driving a spindle motor, a sled motor (stepping motor applicable), a load motor, focus / tracking / tilt actuators, and stepping motor for collimator lens. This IC has an integrated current sense resistance that measures SPM current, which reduces drive system costs. The spindle motor driver part builds in sensorless logic, which attains low-noise operation at the start and run times. The user does not need to self-start the device using the starting circuit or perform position detection by BEMF of a motor or sensors such as a Hall device. As the output stage of all channels works in efficient PWM driving, the user can attain low-power operation by PWM control. Dead-zone-less control is possible for a focus / tracking / tilt actuator driver. In addition, the spindle part output current limiting circuit, the thermal shutdown circuit, the sled-end detection circuit, collimator-lens-end detection circuit, actuator protection, and pre-driver for a 9-V LDO are built in. The newly added, built-in thermometer measures IC temperature.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection Functions

The TPIC2060A has four protection features to protect target equipment: overvoltage protection (OVP), short-circuit protection (SCP), thermal protection (TSD), and actuator temperature protection (ACTTIMER).

8.3.1.1 OVP

The OVP function protects the unit from the supplying high voltage. When the supply voltage exceeds 6.2 V (for P5V), all driver output goes Hi-Z. SPM, sled, and load channels put Hi-Z when P12V is over 14.9 V. Regardless of the input voltage of P5V12L, the load channel become Hi-Z at the time of OVP_P5V or OVP_P12V. When the supply voltage falls below a typical 6.0 V, all outputs start to operate again. (14.5 V for 12-V driver channel) The OVP and POR (RDY) function is not interlocking.

OVP is intended to protect the device in evaluation stage as temporary and back-up solution.

8.3.1.2 SCP

SCP protects the device from breakdown by large current. Each behavior is indicated on Table 1.

Table 1. Protection Threshold Table

BLOCK	FUNCTION	DETECTION CURRENT	DETECT TIME	HI-Z HOLD TIME
STEP driver	SCP	Monitor driver output voltage Hi side FET output V = GND Lo side FET output V = Supply voltage	0.8 to 1.6 µs	1.6 ms
SPM driver				
Sled driver				
Load driver				
Actuator driver				

When the large current is detected on each block, the device puts the output FET to Hi-Z.

When SCP occurs, it returns automatically after expiring set Hi-Z hold time. The OCPSCPERR (REG7F) and SCP flag (REG7B) are set at detection.

The SCP function always monitors the output voltage of the high-side and low-side FET of the output driver. When the setting voltage is not outputted, the device recognizes it as SCP and changes output Hi-Z. The device returns to the original state automatically after 1.6 ms.

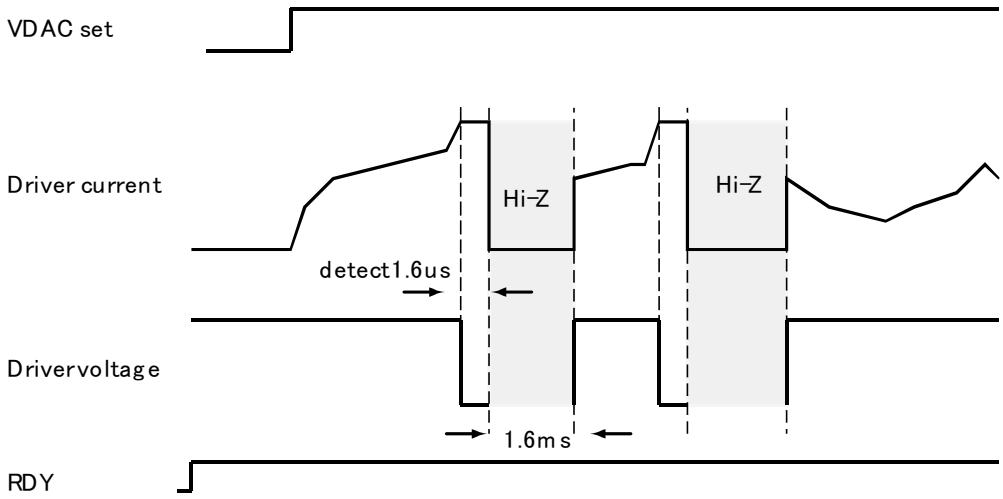


Figure 6. Example of SCP (Driver Short to GND)

8.3.1.3 Temperature Shutdown (TSD)

TSD is a protection function which intercepts an output and suspends an operation when the IC temperature exceeds a maximum permissible on a safety. TSD makes an output Hi-Z when the temperature rises up and a threshold value is exceeded. There are two levels for threshold: Alert and Trip. An alarm is given by status register TSD_FAULT_ on Alert level with 135°C. If it the temperature continues to rise, the register TSD_ is set at 150°C, and the driver output changes HI-Z. If the temperature falls and reaches 135°C, it will output again. The TPIC2060A has 11 temperature sensors in each circuit block. Particular sensors are assigned to the appropriate status flags in Table 2.

Table 2. Thermal Sensor Assignment

CIRCUIT	ALERT (°C)	TRIP (°C)	RELEASE (°C)	ALERT FLAG	TRIP FLAG
U	135	150	135	TSD_FAULT_SPM	TSD_SPM
V	135	150	135	TSD_FAULT_SPM	TSD_SPM
W	135	150	135	TSD_FAULT_SPM	TSD_SPM
TLT	135	150	135	TSD_FAULT_ACT	TSD_ACT
FCS	135	150	135	TSD_FAULT_ACT	TSD_ACT
TRK	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED1	135	150	135	TSD_FAULT_ACT	TSD_ACT
SLED2	135	150	135	TSD_FAULT_ACT	TSD_ACT
STP	135	150	135	TSD_FAULT_ACT	TSD_ACT
LOAD	135	150	135	TSD_FAULT_ACT	TSD_ACT
P12DCHG	135	150	135	TSD_FAULT_P12DCHG	TSD_P12DCHG

8.3.1.4 ACTTIMER

The TPIC2060A has an actuator protection function named ACTTIMER. This function sets the actuator channel output to Hi-Z when the actuator coil current exceeds a specific value. Some other devices use a simple actuator protection function that detects if max current is exceeded with time; however, this other type of actuator protection function lacks accuracy. This new protection calculates heat accumulation and judges accordingly. When this function operates, the load driver channel output will be Hi-Z, the spindle channel is forced to “Auto short brake” and the disc motor stops.

Observe if the protection has occurred by checking the Fault register ACTTIMER_FAULT and ACT_TIMER_PROT. ACTTIMER_FAULT has a character for advance notice, set before detecting ACT_TIMER_PROT. After an ACT_TIMER_PROT is set, even if the temperature falls, it will not release the protection automatically. It is necessary to clear the flag by setting RST_ERR_FLAG or setting 0 to ACTTEMPTH. The ACTTIMER function is disabled by setting H to ACTPROT_OFF or setting 0 to ACTTEMPTH.

To acquire the optimal value for ACTTEMPTH, set the device into the condition of the detection level, and read the value of ACTTEMP. The present value can be read from ACTTEMP. The ACTTEMP data is updated in the register in ACTPROT_OFF = 0 and ACTTEMPTH > 0.

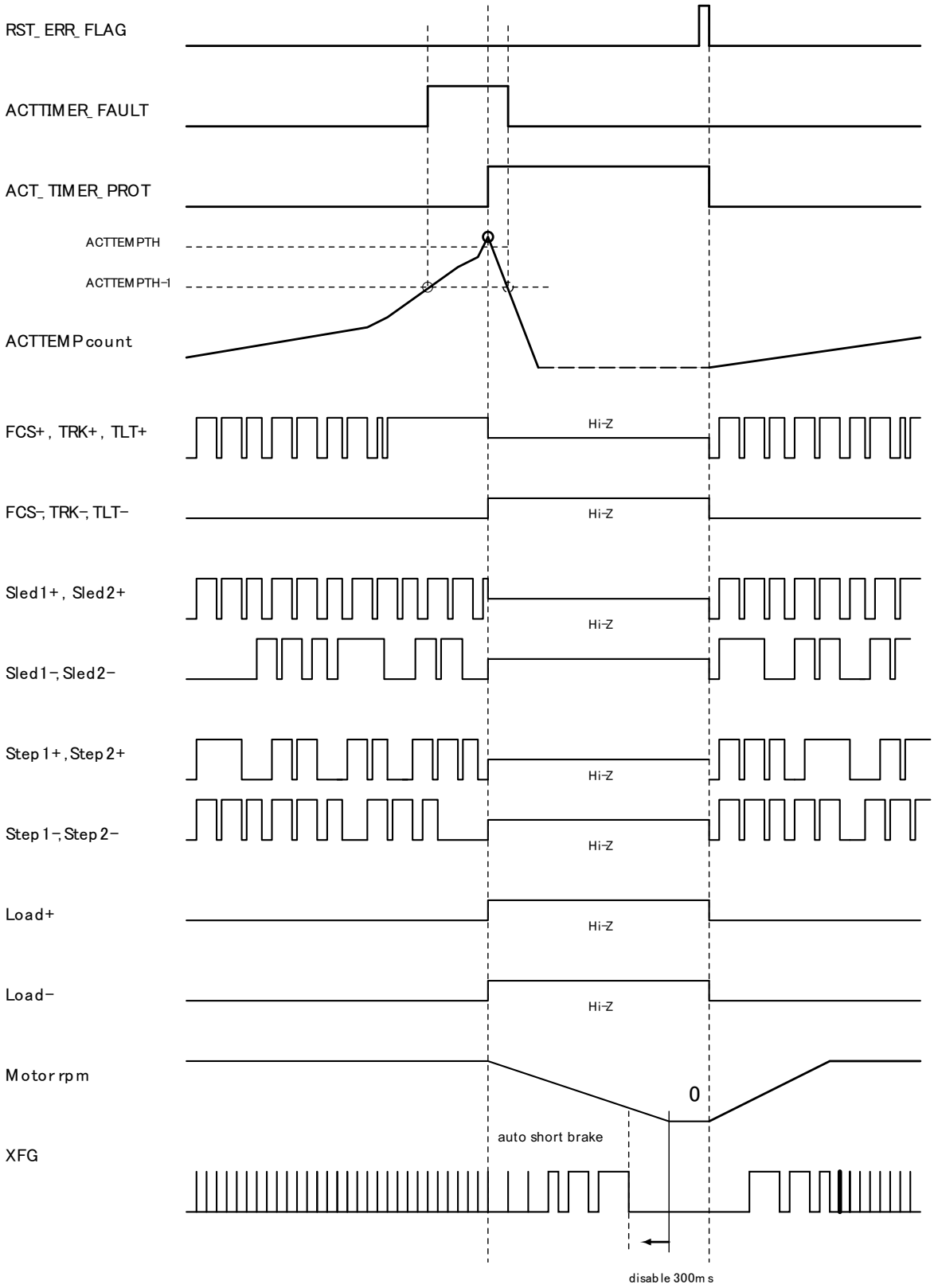


Figure 7. Actuator Temperature Protections

8.4 Device Functional Modes

8.4.1 Differential Tilt Mode

The TPIC2060A supports differential tilt mode, which outputs the value calculated from focus and tilt. Focus and tilt can be set in differential mode by DIFF_TLT (REG74) = 1. Because focus and tilt are updated at the same time, the update interval of tilt can be thinned out. Output data changes at after writing VFCS data. Therefore, it is necessary to write VFCS data when setting VTLT. In differential mode, the output value is calculated as follows.

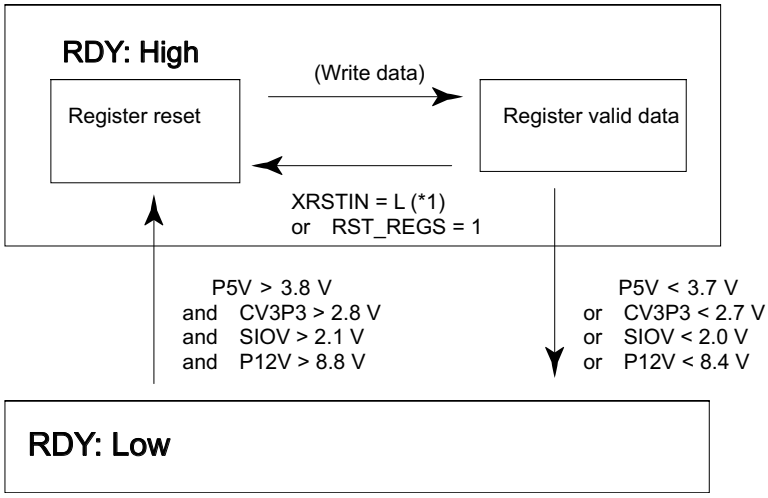
FCS_OUT = (VFCS + VTLT) × 6 (1)

TLT_OUT = (VFCS – VTLT) × 6 (2)

8.4.2 Power-On Reset (POR)

8.4.2.1 RDY (Power Ready)

The TPIC2060A prepares the RDY pin to show a power status to the host controller. A device sets RDY output to high (= POR), if the supply voltage and internal regulator voltage reach a rated value. All registers are initialized at the time of POR operation. Figure 8 shows the behavior of RDY.



A. *1 = The period of XRSTIN cannot be communicated with the device.

Figure 8. 10 RDY Pin Behavior

8.4.2.2 Voltage Monitoring

Power faults are reported in the UVLOMon register. Each UVLOMon bit is initialized to 0 upon a cold power-up. After a fault is detected, the appropriate fault bit is latched high. Writing to the RST_ERR_FLG (REG77) clears all UVLOMon bits. Table 3 summarizes the power device faults and actions.

Table 3. Power Fault Monitor

FAULT TYPE	LATCHED REGISTER	POR	CRITERIA	DRIVER OUTPUT AT DETECTION				
				SPM	SLED	LOAD	STEP	ACT
P5V under voltage	UVLO_P5V	Yes	<3.7 V	Hi-Z				
Internal 3.3 V under voltage	UVLO_INT3P3	Yes	<2.7 V	Hi-Z				
P12V under voltage	UVLO_P12V	Yes(1)	<8.4 V	Hi-Z				
SIOV under voltage	UVLO_SIOV	Yes	<2.0 V	Hi-Z				
P5V over voltage	OVP_P5V		>6.2 V	Hi-Z				
P12V over voltage	OVP_P12V		>14.9 V	Hi-Z			—	—

(1) P12VMUTE_NORST = 0: force POR, P12VMUTE_NORST = 1: no POR

8.5 Programming

8.5.1 Serial Port Functional Description

The serial communication of the TPIC2060A is based on a SPI communications protocol. TPIC2060A is put on the slave side. All 16-bit transmission data is effective in SSZ = L period.

The bit stream sent through SIMO from a master (DSP) is latched to an internal shift register by the rising edge of SCLK. All data is transmitted in a 16-bit format of a command and data. A format has two types of data, 8 bits and 12 bits in length. To access specific registers, an address and R/W flag are specified as a command part. In addition, 12-bit data types do not have a R/W flag in the packet, as the DAC register (= 12-bit data form) is Write only. A transfer packet, command and data, is transmitted sequentially from MSB to LSB. A packet is distinguished in MSB 2 bits of command. In the case of 11, it handles a packet for control register access, and the other processed as a packet for a DAC data setting.

These are the four kinds of serial-data communication packets:

- Write 12 bits DAC data (MSB two bit ≠ 11)
- Write 8 bits control register (MSB two bit = 11)
- Read 8 bits control register (MSB two bit = 11)
- Write 12 bits Focus DAC data + Read 8 bits status register at the same time (MSB two bit ≠ 11)

8.5.2 Write Operation

For write operations, DSP transmits 16-bit (command + address + data) data in an order from MSB. Only the 16-bit data, 16 SCLK sent from the master during SSZ = L, is effective. If >17 or <15 SCLK pulses are received during the time that SSZ is low, the whole packet is ignored. For all valid write operations, the data of the shift register is latched into its designated internal register at the rising edge of the 16th SCLK. All internal register bits, except as indicated otherwise, are reset to their default states upon power-on reset.

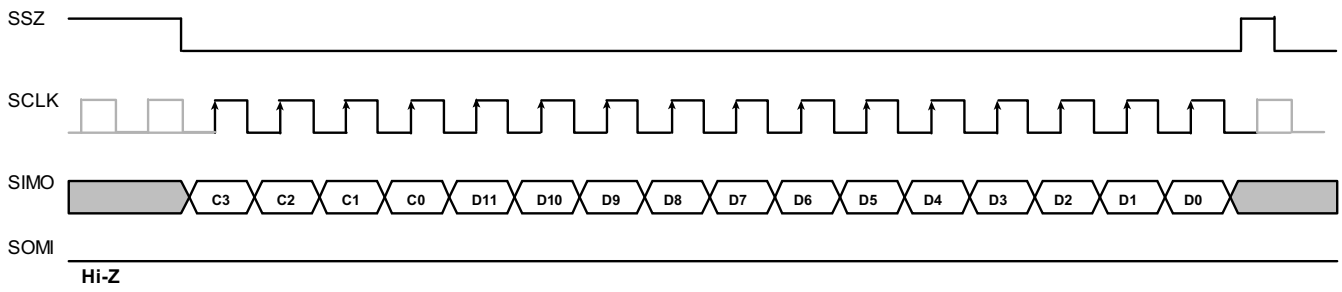


Figure 9. Write 12 Bits DAC Data

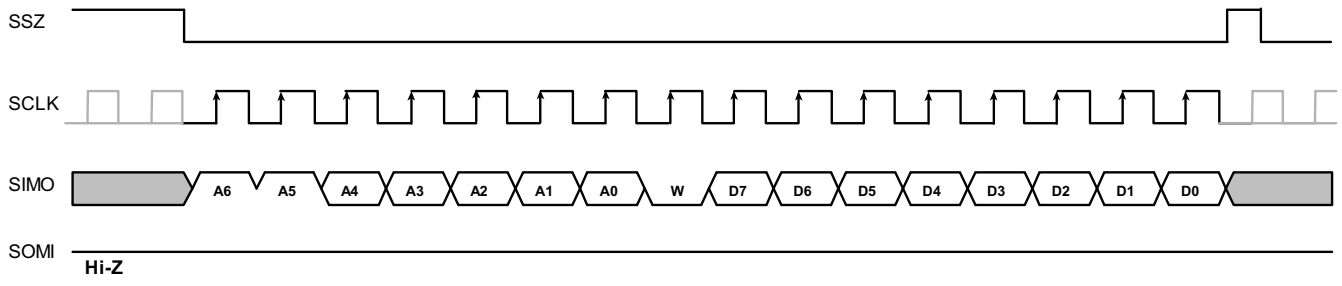


Figure 10. Write 8 Bits Control Register

Programming (continued)

8.5.3 Read Operation

DSP sends an 8-bit header through SIMO to perform the Read operation. The TPIC2060A starts to drive the SOMI line upon the eighth falling edge of SCLK and shifts out eight data bits. The master DSP inputs 8 bits of data from SOMI after the ninth rising edge of SCLK.

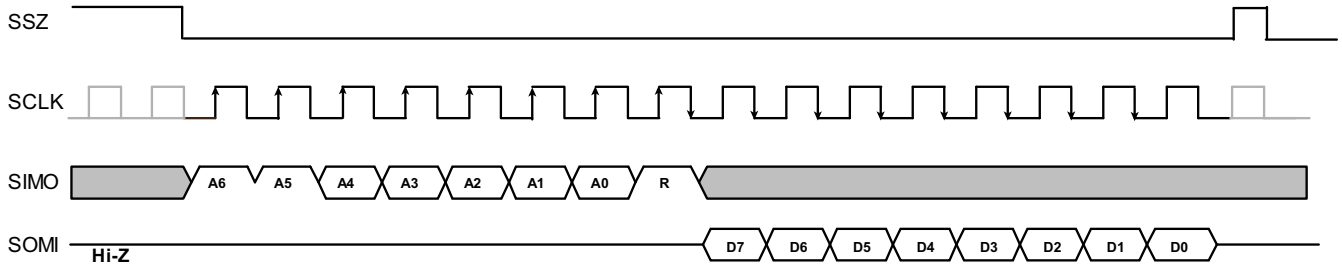


Figure 11. Read 8 Bits Control Register

8.5.4 Write and Read Operation

Optionally, the master DSP can read the Status register during writing a 12 bits DAC (Focus DAC) packet. It is enabled by setting bit RDSTAT_ON_VFCS (REG74) = H.

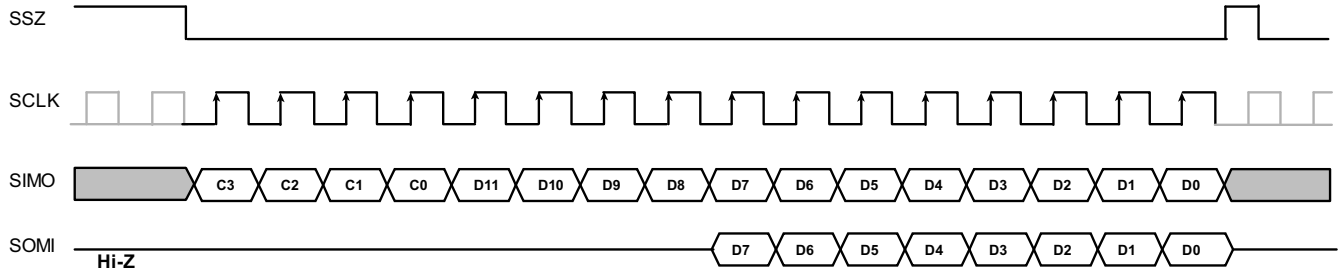


Figure 12. Write 12 Bits Focus DAC Data + Read 8 Bits Status Data

8.6 Register Maps

All registers are in WRITE-protect mode after XRSTIN release. WRITE_ENA bit (REG76) = 1 is required before writing data in register.

8.6.1 Register State Transition

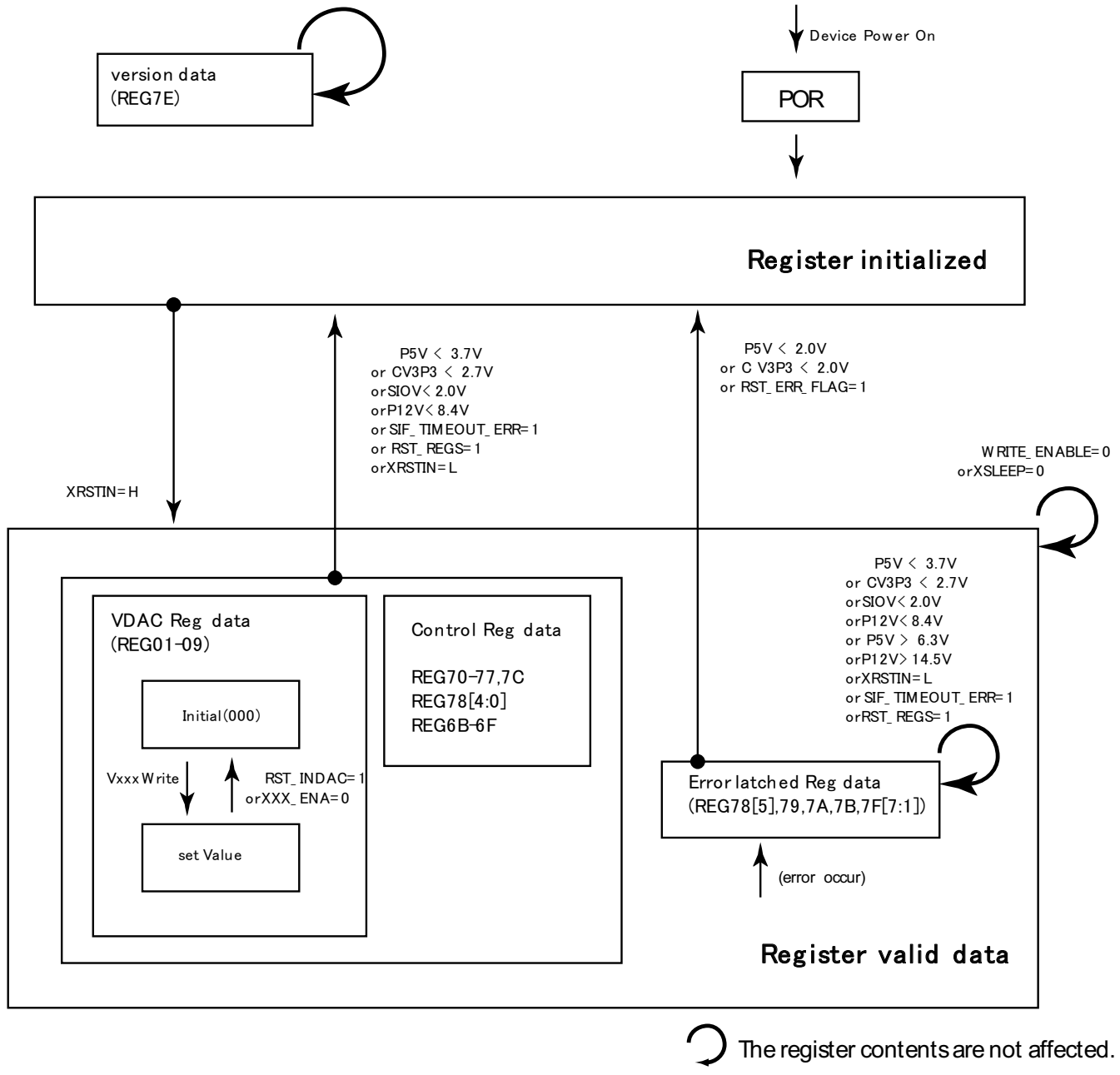


Figure 13. Register Behavior

Register Maps (continued)

8.6.2 DAC Register (12-Bit Write Only)

Two different forms are prepared in the 12-bit DAC register. The forms are selected by setting VDAC_MAPSW (REG74h).

Table 4. List 2 DAC Register (VDAC_MAPSW = 0)

REG	NAME	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	N/A											
01h	VTLT	VTLT [11]	VTLT [10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
02h	VFCS	VFCS [11]	VFCS [10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTRK	VTRK [11]	VTRK [10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
04h	VSLD1	VSLD1 [11]	VSLD1 [10]	VSLD1 [9]	VSLD1 [8]	VSLD1 [7]	VSLD1 [6]	VSLD1 [5]	VSLD1 [4]	VSLD1[3]	VSLD1[2]	VSLD1[1](1)	VSLD1[0](1)
05h	VSLD2	VSLD2 [11]	VSLD2 [10]	VSLD2 [9]	VSLD2 [8]	VSLD2 [7]	VSLD2 [6]	VSLD2 [5]	VSLD2 [4]	VSLD2[3]	VSLD2[2]	VSLD2[1](1)	VSLD2[0](1)
06h	VSTP1	VSTP1 [11]	VSTP1 [10]	VSTP1 [9]	VSTP1 [8]	VSTP1 [7]	VSTP1 [6]	VSTP1 [5]	VSTP1 [4]	VSTP1[3](1)	VSTP1[2](1)	VSTP1[1](1)	VSTP1[0](1)
07h	VSTP2	VSTP2 [11]	VSTP2 [10]	VSTP2 [9]	VSTP2 [8]	VSTP2 [7]	VSTP2 [6]	VSTP2 [5]	VSTP2 [4]	VSTP2[3](1)	VSTP2[2](1)	VSTP2[1](1)	VSTP2[0](1)
08h	VSPM	VSPM [11]	VSPM [10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
09h	VLOAD	VLOAD [11]	VLOAD [10]	VLOAD[9]	VLOAD[8]	VLOAD[7]	VLOAD[6]	VLOAD[5]	VLOAD[4]	VLOAD[3]	VLOAD[2]	VLOAD[1]	VLOAD[0]
0Ah	N/A	N/A											
0Bh	N/A	N/A											

(1) TPIC2060A process as 0 even if set as 1.

Table 5. List 3 DAC Register (VDAC_MAPSW=1)

REG	NAME	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	N/A											
01h	VTRK	VTRK [11]	VTRK [10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
02h	VFCS	VFCS [11]	VFCS [10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTLT	VTLT [11]	VTLT [10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
04h	VSLD1	VSLD1 [11]	VSLD1 [10]	VSLD1 [9]	VSLD1 [8]	VSLD1 [7]	VSLD1 [6]	VSLD1 [5]	VSLD1 [4]	VSLD1 [3]	VSLD1 [2]	VSLD1 [1](1)	VSLD1 [0](1)
05h	VSLD2	VSLD2 [11]	VSLD2 [10]	VSLD2 [9]	VSLD2 [8]	VSLD2 [7]	VSLD2 [6]	VSLD2 [5]	VSLD2 [4]	VSLD2 [3]	VSLD2 [2]	VSLD2 [1](1)	VSLD2 [0](1)
06h	VSPM	VSPM [11]	VSPM [10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
07h	N/A	N/A											
08h	N/A	N/A											
09h	VLOAD	N/A				VLOAD [11]	VLOAD [10]	VLOAD [9]	VLOAD [8]	VLOAD [7]	VLOAD [6]	VLOAD [5]	VLOAD [4]
0Ah	VSTP1	N/A				VSTP1 [11]	VSTP1 [10]	VSTP1 [9]	VSTP1 [8]	VSTP1 [7]	VSTP1 [6]	VSTP1 [5]	VSTP1 [4]
0Bh	VSTP2	N/A				VSTP2 [11]	VSTP2 [10]	VSTP2 [9]	VSTP2 [8]	VSTP2 [7]	VSTP2 [6]	VSTP2 [5]	VSTP2 [4]

(1) TPIC2060A process as 0 even if set as 1.

8.6.3 Control Register (8-Bit Read/Write)

Table 6. List 4 Control Register (8-Bit Read/Write)

REG	NAME	F	7	6	5	4	3	2	1	0
70h	DriverEna	R/W	TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
71h	FuncEna	R/W	TI Rsvd	SLD _ENDDET _ENA	STP _ENDDET _ENA	TI Rsvd	LIN9V _DISABLE	SPM_RCOM_SEL		TEMPMON _ENA
72h	ACTCfg	R/W	P12VMUTE _NORST	RSTIN_OFF	ACTPROT _OFF	ACTTEMPTH				
73h	Parm0	R/W	SIF_TIMEOUT_TH		SLEDEND _HZTIME	SLDENDTH		STPEND _HZTIME	STPENDTH	
74h	SIFCfg	R/W	DIFF_TLT	TI Rsvd	STATUS _ON_VFCS	VSLD2 _POL	VSTP2 _POL	ADVANCE _RD	SOMI_HIZ	VDAC _MAPSW
75h	Parm1	R/W	TRAY_LOCKDET			TI Reserved		SPM_FAST _BRK	SPM_SLNT _BRK	SPM _HIZMODE
76h	WriteEna	R/W	WRITE _ENABLE	TI Reserved					REG6X _Write	TI Rsvd
77h	ClrReg	W	RST_INDAC	RST_REGS	RST_ERR _FLAG	TI Reserved				
78h	ActTemp	R	TI Reserved		ACT_TIMER _PROT	ACTTEMP				
79h	UVLOMon	R	LIN9V_RDY	TI Rsvd	UVLO_P5V	UVLO _INT3P3	UVLO _P12V	UVLO_SIOV	OVP_P5V	OVP_P12V
7Ah	TSDMon	R	TI Rsvd	TSD _FAULT _SPM	TSD _FAULT _ACT	TSD _FAULT _P12DCHG	TI Rsvd	TSD_SPM	TSD_ACT	TSD _P12DCHG
7Bh	SCPMon	R	TI Reserved			SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT	SCP_STP
7Ch	TempMon	R	CHIPTEMP _STATUS	CHIPTEMP						
7Dh	Monitor	R	SIF_TIMEO UTERR	XRSTIN _DET	TI Rsvd	TRAY_LOC KDETECT	TRAY_PUS HDETP	TRAY_PUS HDETN	STP _ENDDET	SLD _ENDDET
7Eh	Version	R	Version							
7Fh	Status	R	ACTTIMER _FAULT	MONITOR	TI Rsvd	PWRERR	TSDERR	SCPERR	TSDFAULT	FG
60h	SPMCfg	R/W	TI Rsvd	FG_SBRK _OFF	TI Reserved				IS_NZONE _OFF	TI Rsvd
61h	SPMCfg	R/W	TI Reserved						PWMmaxDu ty_R_SEL	TI Rsvd
62h	SPMCfg	R/W	TI Reserved				TIME_BASE_SEL		TI Reserved	
63h	Protect	R/W	TI Reserved							
64h	Protect	R/W	TI Reserved				FG5M_OFF	TI Reserved		
65h	SPMCfg	R/W	TI Reserved			HZSVR_SEL		TI Reserved		
66h	Protect	R/W	TI Reserved							
67h	Protect	R/W	TI Reserved							
68h	Protect	R/W	TI Reserved						SPM_TQAJST	
6Bh	DisProt	R/W	SCP_SPM _OFF	SCP_SLED _OFF	SCP_LOAD _OFF	SCP_ACT _OFF	SCP_STP _OFF	SPM _RCDDIS	TI Reserved	
6Ch	ENDCfg	R/W	PUSHDETTH		PUSHDET_TIME		TI Reserved			
6Dh	Protect	R/W	TI Reserved							
6Eh	UtilCfg	R/W	GPOUT_HL	GPOUT _ENA	TI Reserved					
6Fh	GPOUTSet	R/W	ACTTIMER _FLT_MON	MONITOR _MON	TI Rsvd	PWRERR _MON	TSDERR _MON	OCPSCPER R_MON	TSDFAULT _MON	SPMRCD _BRK_MON

VTRK and VLOAD is exclusive, using the same DAC circuit block.

8.6.4 Detailed Register Description

8.6.4.1 REG01 12-Bit DAC for Tilt (offset = 01h)

(VDAC_MAPSW = 0)

Figure 14. REG01 12-Bit DAC for Tilt

				11	10	9	8
				VTLT			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTLT							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. REG01 12-Bit DAC for Tilt Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VTLT	W	0h	Digital input code for tilt. 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by "differential tilt mode (REG74[7])" TLT_OUT = VTLT × (6.0/2048) (DIFF_TLT = 0) TLT_OUT = (VFCS-VTLT) × (6.0/2048) (DIFF_TLT = 1) TLT_OUT should be changed after writing VFCS. In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.

8.6.4.2 REG02 12-Bit DAC for Focus (offset = 02h)

(VDAC_MAPSW = 0)

Figure 15. REG02 12-Bit DAC for Focus

				11	10	9	8
				VFCS			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VFCS							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. REG02 12-Bit DAC for Focus Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VFCS	W	0h	Digital input code for focus. 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by differential tilt mode (REG74[7]) FCS_OUT = VFCS × (6.0/2048) (DIFF_TLT = 0) FCS_OUT = (VFCS + VTLT) × (6.0 / 2048) (DIFF_TLT = 1)

8.6.4.3 REG03 12-Bit DAC for Tracking (offset = 03h)

(VDAC_MAPSW = 0)

Figure 16. REG03 12-Bit DAC for Tracking

				11	10	9	8
				VTRK			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTRK							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. REG03 12-Bit DAC for Tracking Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VTRK	W	0h	Digital input code for tracking. 2's complement format 0x800(-2048) to 0x7ff(+2047) TRK_OUT = VTRK × (6.0 / 2048)

8.6.4.4 REG04 12-Bit DAC for Sled1 (offset = 04h)

(VDAC_MAPSW = 0)

Figure 17. REG04 12-Bit DAC for Sled1

				11	10	9	8
				VSLD1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REG04 12-Bit DAC for Sled1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VSLD1	W	0h	Digital input code for sled1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD1[1:0], will be handled with 0. SLD1_OUT = VSLD1 × (880 mA / 2048)

8.6.4.5 REG05 12-Bit DAC for Sled2 (offset = 05h)

(VDAC_MAPSW = 0)

Figure 18. REG05 12-Bit DAC for Sled2

				11	10	9	8
				VSLD2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REG05 12-Bit DAC for Sled2 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VSLD2	W	0h	Digital input code for sled2. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD2[1:0], will be handled with 0. SLD2_OUT = VSLD2 × (880 mA / 2048)

8.6.4.6 REG06 12-Bit DAC for Stepping1 (offset = 06h)

(VDAC_MAPSW = 0)

Figure 19. REG06 12-Bit DAC for Stepping1

				11	10	9	8
				VSTP1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REG06 12-Bit DAC for Stepping1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VSTP1	W	0h	Digital input code for stepping1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Although VSTP1 is 12-bit width, MSB 8 bits is effective. Four bits on LSB, VSTP1[3:0], will be handled with 0. VSTP1_OUT = VSTP1 × (P5V/2048)

8.6.4.7 REG07 12-Bit DAC for Stepping2 (offset = 07h)

(VDAC_MAPSW = 0)

Figure 20. REG07 12-Bit DAC for Stepping2

				11	10	9	8
				VSTP2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REG07 12-Bit DAC for Stepping2 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VSTP2	W	0h	Digital input code for stepping2. 2's complement format 0x800(-2048) to 0x7ff(+2047) Although VSTP2 is 12-bit width, MSB 8 bits is effective. Four bits on LSB, VSTP2[3:0], will be handled with 0. VSTP2_OUT = VSTP2 × (P5V/2048)

8.6.4.8 REG08 12-Bit DAC for Spindle (offset = 08h)

(VDAC_MAPSW = 0)

Figure 21. REG08 12-Bit DAC for Spindle

				11	10	9	8
				VSPM			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSPM							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REG08 12-Bit DAC for Spindle Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VSPM	W	0h	Digital input code for spindle. 2's complement format 0x800(-2048) to 0x7ff(+2047) SPM_OUT = VSPM × (14.0/2048)

8.6.4.9 REG09 12-Bit DAC for Load (offset = 09h)

(VDAC_MAPSW = 0)

Figure 22. REG09 12-Bit DAC for Load

				11	10	9	8
				VLOAD			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VLOAD							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REG09 12-Bit DAC for Load Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	VLOAD	W	0h	Digital input code for load. 2's complement format 0x800(-2048) to 0x7ff(+2047) LOAD_OUT = VLOAD × (6.0 / 2048) at P5V12L = 5.0 V LOAD_OUT = VLOAD × (14.0 / 2048) at P5V12L = 12.0 V

8.6.4.10 REG70 8-Bit Control Register for DriverEna (offset = 70h)

Figure 23. REG70 8-Bit Control Register for DriverEna

7	6	5	4	3	2	1	0
TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REG70 8-Bit Control Register for DriverEna Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	TLT_ENA	RW	0h	1h = Tilt enable (with XSLEEP = 1)
6	FCS_ENA	RW	0h	1h = Focus enable (with XSLEEP = 1)
5	TRK_ENA	RW	0h	1h = Track enable (with XSLEEP = 1)
4	SPM_ENA	RW	0h	1h = Spindle enable (with XSLEEP = 1)
3	SLD_ENA	RW	0h	1h = Sled enable (with XSLEEP = 1)
2	STP_ENA	RW	0h	1h = Step enable (with XSLEEP = 1)
1	LOAD_ENA	RW	0h	1h = LOAD enable (with XSLEEP = 1) Track (bit5:TRK_ENA) will be disabled at LOAD_ENA = 1 because of sharing the DAC PWM module. Load priority is higher than TRK_ENA.
0	XSLEEP	RW	0h	1h = Operation mode (need 1 ms) 0h = Standby mode Charge pump enable bit. All driver enable bit (Bit[7:1]) change disabled and output change to Hi-Z (regardless of setting xxx_ENA bit is 1) when setting XSLEEP to 0. Therefore, set 1 to XSLEEP before setting each enable bit.

8.6.4.11 REG71 8-Bit Control Register for FuncEna (offset = 71h)

Figure 24. REG71 8-Bit Control Register for FuncEna

7	6	5	4	3	2	1	0
Reserved	SLD_ENDDET_ENA	STP_ENDDET_ENA	Reserved	LIN9V_DISABLE	SPM_RCOM_SEL		TEMPMON_ENA
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0		rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REG71 8-Bit Control Register for FuncEna Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	RW	0h	
6	SLD_ENDDET_ENA	RW	0h	1h = Enable SLED channel end position detection (with XSLEEP = 1, SLD_ENA)
5	STP_ENDDET_ENA	RW	0h	1h = Enable STEP channel end position detection (with XSLEEP = 1, STP_ENA)
4	Reserved	RW	0h	
3	LIN9V_DISABLE	RW	0h	1h = Disable LDO predriver
2-1	SPM_RCOM_SEL	RW	0h	Select resistor value of spindle current sense resistor. Current limit is set as following current (with SPM_TQAJST = 00) 00: 1133 mA 01: 772 mA 10: 1416 mA 11: 1700 mA
0	TEMPMON_ENA	RW	0h	1h = Enable chip temperature monitoring (with XSLEEP = 1)

8.6.4.12 REG72 8-Bit Control Register for ACTCfg (offset = 72h)

Figure 25. REG72 8-Bit Control Register for ACTCfg

7	6	5	4	3	2	1	0
P12VMUTE_NORST	RSTIN_OFF	ACTPROT_OFF	ACTTEMPTH				
rw-0	rw-0	rw-0	rw-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. REG72 8-Bit Control Register for ACTCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	P12VMUTE_NORST	RW	0h	0h = System reset at P12V low voltage 1h = Output High-Z only at P12V low-voltage detection
6	RSTIN_OFF	RW	0h	0h = XRSTIN input enable 1h = Ignored XRSTIN pin input (do not reset device when XRSTIN = L)
5	ACTPROT_OFF	RW	0h	0h = Actuator protection ON 1h = Actuator fault monitor disable (no protection for ACT channel)
4-0	ACTTEMPTH	RW	0h	Actuator thermal protection (= ACT Timer) threshold level ACT Timer Protection enable except ACTTEMPTH[4:0] = 0x00 ACTTEMPTH = 0x00 equal to ACTPROT_OFF = 1 By writing value 0x00, ACTTIMER_PROT flag is cleared.

8.6.4.13 REG73 8-Bit Control Register for Parm0 (offset = 73h)

Figure 26. REG73 8-Bit Control Register for Parm0

7	6	5	4	3	2	1	0
SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH		STPEND_HZTIME	STPENDTH	
rw-0		rw-0	rw-0		rw-0	rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. REG73 8-Bit Control Register for Parm0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	SIF_TIMEOUT_TH	RW	0h	Watch dog timer for Serial communication 0h = Disable 1h = 1 ms 2h = 100 µs 3h = 10 µs Set SIF_TIMEOUTERR (REG7D) if communication is suspended for this time period. Reset register processing is performed if a SIF_TIMEOUTERR occurs.
5	SLEDEND_HZTIME	RW	0h	Time window for sled end detection. 0h = 400 µs 1h = 200 µs Note: The user must recycle SLD_ENDDET_ENA = 0 → 1 after writing this bit.
4-3	SLDENDTH	RW	0h	Sled end detection sensibility setting. Detection threshold for motor BEMF 00: 124 mV 01: 168 mV 11: 72 mV 10: 0 mV (use for test purpose)
2	STPEND_HZTIME	RW	0h	Step High-Z detection period in end detection 0h = 400 µs 1h = 200 µs Note: The user must recycle STP_ENDDET_ENA = 0→1 after writing this bit.
1-0	STPENDTH	RW	0h	Step end detection sensibility setting 00: 39 mV 01: 61 mV 11: 19 mV 10: 0 mV (use for test purpose)

8.6.4.14 REG74 8-Bit Control Register for SIFCfg (offset = 74h)

Figure 27. REG74 8-Bit Control Register for SIFCfg

7	6	5	4	3	2	1	0
DIFF_TLT	Reserved	STATUS_ON_VFCS	VSLD2_POL	VSTP2_POL	ADVANCE_RD	SOMI_HIZ	VDAC_MAPSW
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. REG74 8-Bit Control Register for SIFCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	DIFF_TLT	RW	0h	1h = Differential tilt mode enable (with TLT_ENA = FCS_ENA = 1) Differential tilt mode (DIFF_TLT = 1), DAC value setting as follows FCS_OUT = (VFCS + VTLT) × 6 / 2048 TLT_OUT = (VFCS – VTLT) × 6 / 2048 In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.
6	Reserved	RW	0h	
5	STATUS_ON_VFCS	RW	0h	Set Read status data (REG7F) at VFCS write command (REG02) 1h = enable Write and Read mode (Write 12 bits Focus DAC data + Read 8 bits status data)
4	VSLD2_POL	RW	0h	Change direction of SLED rotation
3	VSTP2_POL	RW	0h	Change direction of STEP rotation
2	ADVANCE_RD	RW	0h	0h = Normal read timing 1h = Read timing is advanced half clock cycle
1	SOMI_HIZ	RW	0h	0h = SOMI line High-Z at bus idling time. 1h = SOMI line Pull down at bus idling time.
0	VDAC_MAPSW	RW	0h	1h = Change channel assignments of DAC register (REG01~0A)

8.6.4.15 REG75 8-Bit Control Register for Parm1 (offset = 75h)

Figure 28. REG75 8-Bit Control Register for Parm1

7	6	5	4	3	2	1	0
TRAY_LOCKDET			Reserved		SPM_FAST_BRK	SPM_SLNT_BRK	SPM_HIZMODE
rw-0			rw-0		rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. REG75 8-Bit Control Register for Parm1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	TRAY_LOCKDET	RW	0H	Load tray locking detection control 0h = Disable detection 1-7: Detection threshold 1h = 100 mA 2h = 150 mA 3h = 200 mA 4h = 250 mA 5h = 300 mA 6h = 350 mA 7h = 400 mA
4-3	Reserved	RW	0h	
2	SPM_FAST_BRK	RW	0h	Fast brake mode selection 0h = Normal brake mode perform auto short brake sequence in specific speed 1h = No short brake under 5500 rpm
1	SPM_SLNT_BRK	RW	0h	Silent brake mode selection 0h = Normal brake mode 1h = No active brake under 5500 rpm Active brake mode is not performed inputting any value into VSPIN.
0	SPM_HIZMODE	RW	0h	Spindle output Hi-Z mode 0h = Normal operation 1h = Spindle output (UVW) put Hi-Z (use for test purpose)

8.6.4.16 REG76 8-Bit Control Register for WriteEna (offset = 76h)

Figure 29. REG76 8-Bit Control Register for WriteEna

7	6	5	4	3	2	1	0
WRITE_ENABLE	Reserved					REG6X_Write	Reserved
rw-0	rw-0					rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. REG76 8-Bit Control Register for WriteEna Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	WRITE_ENABLE	RW	0h	0h = Register Write disable except REG76 1h = Write enable for registers REG01~09, REG70~7F
6-2	Reserved	RW	0h	
1	REG6X_Write	RW	0h	0h = Disable Write access REG6X bank 1h = Enable Write access REG6X bank

8.6.4.17 REG77 8-Bit Control Register for ClrReg (offset = 77h)

Figure 30. REG77 8-Bit Control Register for ClrReg

7	6	5	4	3	2	1	0
RST_INDAC	RST_REGS	RST_ERR_FLAG	Reserved				
w-0	w-0	w-0	w-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. REG77 8-Bit Control Register for ClrReg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RST_INDAC	W	0h	1h = Reset all 12-bit input DAC register (REG01~09) *Self clear bit
6	RST_REGS	W	0h	1h = Reset all 8-bit R/W registers (REG70h~77h, 60h-6Fh) *Self clear bit
5	RST_ERR_FLAG	W	0h	1h = Reset fault flag latch (REG7F, REG79~REG7D) *Self clear bit
4-0	Reserved	W	0h	

8.6.4.18 REG78 8-Bit Control Register for ActTemp (offset = 78h)

Figure 31. REG78 8-Bit Control Register for ActTemp

7	6	5	4	3	2	1	0
Reserved		ACT_TIMER_PROT	ACTTEMP				
r-0		r-0	r-0				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. REG78 8-Bit Control Register for ActTemp Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R	0h	
5	ACT_TIMER_PROT	R	0h	ACT timer protection flag 1h = ACT Timer Protection has detected and latched. (ACTTEMP > ACTTEMPTH) This bit holds data after temperature change to low since this is a latch bit. Also driver output keep Hi-Z until setting RST_ERR_FLAG or ACTTEMPTH = 0.
4-0	ACTTEMP	R	0h	An integrated value of ACT_TIMER counters at present.

8.6.4.19 REG79 8-Bit Control Register for UVLOMon (offset = 79h)

Figure 32. REG79 8-Bit Control Register for UVLOMon

7	6	5	4	3	2	1	0
LIN9V_RDY	RCD_BRK	UVLO_P5V	UVLO_INT3P3	UVLO_P12V	UVLO_SIOV	OVP_P5V	OVP_P12V
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. REG79 8-Bit Control Register for UVLOMon Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LIN9V_RDY	R	0h	LIN9V output status. LINFB voltage over 92% (typical) of target voltage.
6	RCD_BRK	R	0h	
5	UVLO_P5V	R	0h	UVLO flag for detection Low P5V supply (1)
4	UVLO_INT3P3	R	0h	UVLO flag for detection Low internal 3.3-V regulator(1)
3	UVLO_P12V	R	0h	UVLO flag for detection Low P12V supply (1)
2	UVLO_SIOV	R	0h	UVLO flag for detection Low SIOV supply (1)
1	OVP_P5V	R	0h	OVP flag for P5V supply (1)
0	OVP_P12V	R	0h	OVP flag for P12V supply (1)

(1) Latched first reset event only. Cleared by RST_ERR_FLG (REG77)

8.6.4.20 REG7A 8-Bit Control Register for TSDMon (offset = 7Ah)

Figure 33. REG7A 8-Bit Control Register for TSDMon

7	6	5	4	3	2	1	0
Reserved	TSD_FAULT _SPM	TSD_FAULT _ACT	TSD_FAULT _P12DCHG	Reserved	TSD_SPM	TSD_ACT	TSD_ P12DCHG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. REG7A 8-Bit Control Register for TSDMon Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	0h	
6	TSD_FAULT_SPM	R	0h	Prealert of thermal protection of Spindle block(1)
5	TSD_FAULT_ACT	R	0h	Prealert of thermal protection of focus /track /tilt sled1 /sled2 /step1 /step2 /load(1)
4	TSD_FAULT_P12DCHG	R	0h	Prealert of thermal protection of P12V discharge block (1)
3	Reserved	R	0h	
2	TSD_SPM	R	0h	Thermal protection flag for spindle(1) SPM output Hi-Z until temperature falls on release level 1h = Detect (latch)
1	TSD_ACT	R	0h	Thermal protection flag for focus /track /tilt sled1 /sled2 /step1 /step2 /load(1) Actuator output Hi-Z until temperature falls on release level 1h = Detect (latch)
0	TSD_ P12DCHG	R	0h	Thermal protection flag for P12V discharge block(1) IDCHG output Hi-Z until temperature falls on release level 1h = Detect (latch)

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.21 REG7B 8-Bit Control Register for SCPMon (offset = 7Bh)

Figure 34. REG7B 8-Bit Control Register for SCPMon

7	6	5	4	3	2	1	0
Reserved			SCP_SPM	SCP_SLED	SCP_LOAD	SCP_ACT	SCP_STP
r-0			r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. REG7B 8-Bit Control Register for SCPMon Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	R	0h	
4	SCP_SPM	R	0h	Short protection flag bit for spindle block(1)
3	SCP_SLED	R	0h	Short protection flag bit for sled block(1)
2	SCP_LOAD	R	0h	Short protection flag bit for load block(1)
1	SCP_ACT	R	0h	Short protection flag bit for Actuator block(1)
0	SCP_STP	R	0h	Short protection flag bit for step block(1)

(1) Cleared by RST_ERR_FLAG bit (REG77)

8.6.4.22 REG7C 8-Bit Control Register for TempMon (offset = 7Ch)

Figure 35. REG7C 8-Bit Control Register for TempMon

7	6	5	4	3	2	1	0
CHIPTEMP_STATUS	CHIPTEMP						
r-0	r-0						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. REG7C 8-Bit Control Register for TempMon Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CHIPTEMP_STATUS	R	0h	1h = New data CHIPTEMP[6:0] is updated It will be cleared after reading.
6-0	CHIPTEMP	R	0h	Chip temperature monitor (1.2°/LSB) 15° (0) to 165° (127) For monitoring, TEMPMON_ENA = 1 and XSLEEP = 1 is required

8.6.4.23 REG7D 8-Bit Control Register for Status Monitor (offset = 7Dh)

Figure 36. REG7D 8-Bit Control Register for Status Monitor

7	6	5	4	3	2	1	0
SIF_TIMEOUTERR	XRSTIN_DET	Reserved	TRAY_LOCKDETECT	TRAY_PUSHDETP	TRAY_PUSHDETN	STP_ENDDET	SLD_ENDDET
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. REG7D 8-Bit Control Register for Status Monitor Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	SIF_TIMEOUTERR	R	0h	Error flag of serial I/F watch dog timer 1h = SIF communication was interrupted, expired watch dog timer
6	XRSTIN_DET	R	0h	XRSTIN event flag 1h = Detect low event in XRSTIN pin
5	Reserved	R	0h	
4	TRAY_LOCKDETECT	R	0h	TRAY lock detection flag 1h = Detect tray lock detection
3	TRAY_PUSHDETP	R	0h	TRAY push event detection flag in LOAD_P pin 1h = Detect tray push event in LOAD_P pin
2	TRAY_PUSHDETN	R	0h	TRAY push event detection flag in LOAD_N pin 1h = Detect tray push event in LOAD_N pin
1	STP_ENDDET	R	0h	Step end event flag 1h = Detect step end event
0	SLD_ENDDET	R	0h	Sled end event flag 1h = Detect sled end event

8.6.4.24 REG7E 8-Bit Control Register for Version (offset = 7Eh)

Figure 37. REG7E 8-Bit Control Register for Version

7	6	5	4	3	2	1	0
Version							
r-0							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. REG7E 8-Bit Control Register for Version Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Version	R	0h	Version[7:4] = revision number of TPIC2060A Version[3:0] = option

8.6.4.25 REG7F 8-Bit Control Register for Status (offset = 7Fh)

Figure 38. REG7F 8-Bit Control Register for Status

7	6	5	4	3	2	1	0
ACTTIMER_FAULT	MONITOR	Reserved	PWRERR	TSDERR	SCPERR	TSDFAULT	FG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. REG7F 8-Bit Control Register for Status Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ACTTIMER_FAULT	R	0h	Status flag of ACTTIMER protection 1h = Prealert of ACTTIMER protection. It is close to the threshold level. The user can get current ACTTIMER value in REG78. Both this bit and ACT_TIMER_PROT (REG78) will be set when over the threshold.
6	MONITOR	R	0h	Event flag of any monitor event in REG7D 1h = Event occurred, details in REG7Dh
5	Reserved	R	0h	
4	PWRERR	R	0h	Error flag of power 1h = Voltage problem occurred, details in REG79
3	TSDERR	R	0h	Error flag of any overthermal protections 1h = Dispatched thermal protection, details in REG7A
2	SCPERR	R	0h	Error flag of any SCP 1h = Dispatched SCP, details in REG7Bh
1	TSDFAULT	R	0h	Warning of TSD of any thermal protection 1h = Detect pre-thermal protection, details in REG7A
0	FG	R	0h	FG signal. Spindle rotation pulse for speed monitor

8.6.4.26 REG60 8-Bit Control Register for SPMCfg (offset = 60h)

Figure 39. REG60 8-Bit Control Register for SPMCfg

7	6	5	4	3	2	1	0
Reserved	FG_SBRK_OFF	Reserved				IS_NZONE_OFF	Reserved
rw-0	rw-0	rw-0				rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. REG60 8-Bit Control Register for SPMCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	RW	0h	
6	FG_SBRK_OFF	RW	0h	FG Jitter setting in short brake period. Should be set to 1
5-2	Reserved	RW	0h	
1	IS_NZONE_OFF	RW	0h	Inductive position sense (IS) timing control. Should be set to 1
0	Reserved	RW	0h	

8.6.4.27 REG61 8-Bit Control Register for SPMCfg (offset = 61h)

Figure 40. REG61 8-Bit Control Register for SPMCfg

7	6	5	4	3	2	1	0
Reserved						PWMmaxDuty_R_SEL	Reserved
rw-0						rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. REG61 8-Bit Control Register for SPMCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	RW	0h	
1	PWMmaxDuty_R_SEL	RW	0h	PWM duty maximum setting in active brake mode 0h = Maximum PWM duty 12.5% 1h = Maximum PWM duty 25% (Recommend to set 0 if using in no-disk because it may not stop in a specific motor setting 25%.)
0	Reserved	RW	0h	

8.6.4.28 REG62 8-Bit Control Register for SPMCfg (offset = 62h)

Figure 41. REG62 8-Bit Control Register for SPMCfg

7	6	5	4	3	2	1	0
Reserved				TIME_BASE_SEL		Reserved	
rw-0				rw-0		rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. REG62 8-Bit Control Register for SPMCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	Reserved	RW	0h	
3-2	TIME_BASE_SEL	RW	0h	Spindle waveform selection. Should be set to 11
1-0	Reserved	RW	0h	

8.6.4.29 REG64 8-Bit Control Register for Protect (offset = 64h)

Figure 42. REG64 8-Bit Control Register for Protect

7	6	5	4	3	2	1	0
Reserved				FG5M_OFF	Reserved		
rw-0				rw-0	rw-0		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. REG64 8-Bit Control Register for Protect Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	Reserved	RW	0h	
3	FG5M_OFF	RW	0h	Spindle FG filter selection. Should be set to 1
2-0	Reserved	RW	0h	

8.6.4.30 REG65 8-Bit Control Register for SPMCfg (offset = 65h)

Figure 43. REG65 8-Bit Control Register for SPMCfg

7	6	5	4	3	2	1	0
Reserved			HZSVR_SEL		Reserved		
rw-0			rw-0		rw-0		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. REG65 8-Bit Control Register for SPMCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	RW	0h	
4-3	HZSVR_SEL	RW	0h	Spindle waveform silent mode selection. Should be set to 11
2-0	Reserved	RW	0h	

8.6.4.31 REG68 8-Bit Control Register for Protect (offset = 68h)

Figure 44. REG68 8-Bit Control Register for Protect

7	6	5	4	3	2	1	0
Reserved						SPM_TQAJST	
rw-0						rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. REG68 8-Bit Control Register for Protect Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	RW	0h	
1-0	SPM_TQAJST	RW	0h	Select fine adjust value of spindle limit current which is set by SPM_RCOM_SEL 00: No adjust 01: –5% 10: –10% 11: –15%

8.6.4.32 REG6B 8-Bit Control Register for DisProt (offset = 6Bh)

Figure 45. REG6B 8-Bit Control Register for DisProt

7	6	5	4	3	2	1	0
SCP_SPM_OFF	SCP_SLED_OFF	SCP_LOAD_OFF	SCP_ACT_OFF	SCP_STP_OFF	SPM_RCDDIS	Reserved	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. REG6B 8-Bit Control Register for DisProt Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	SCP_SPM_OFF	RW	0h	Control bit of SCP function for spindle block. 0h = Enable SCP function 1h = Disable SCP function Caution(1) TI recommends using it only for test purposes.
6	SCP_SLED_OFF	RW	0h	For Sled driver block. Caution(1) TI recommends using it only for test purposes.
5	SCP_LOAD_OFF	RW	0h	For Load driver block Caution(1) TI recommends using it only for test purposes.
4	SCP_ACT_OFF	RW	0h	For Actuator driver block Caution(1) TI recommends using it only for test purposes.
3	SCP_STP_OFF	RW	0h	For Step driver block Caution(1) TI recommends using it only for test purposes.
2	SPM_RCDDIS	RW	0h	Spindle block reverse current detect function. 0h = Enable 1h = Disable
1-0	Reserved	RW	0h	

(1) Caution: Device will be fatally damaged if short circuit occurs in the xxx_OFF = 1.

8.6.4.33 REG6C 8-Bit Control Register for ENDCfg (offset = 6Ch)

Figure 46. REG6C 8-Bit Control Register for ENDCfg

7	6	5	4	3	2	1	0
PUSHDETTH		PUSHDET_TIME		Reserved			
rw-0		rw-0		rw-0			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. REG6C 8-Bit Control Register for ENDCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	PUSHDETTH	RW	0h	Detection voltage threshold for PUSH detection 00: Disable function 01: 1 V 10: 0.75 V 11: 0.5 V
5-4	PUSHDET_TIME	RW	0h	Duration of PUSH detection 00: 104 ms 01: 208 ms 10: 416 ms 11: 0 ms (immediately at the exceeding threshold)
3-0	Reserved	RW	0h	

8.6.4.34 REG6E 8-Bit Control Register for UtilCfg (offset = 6Eh)

Figure 47. REG6E 8-Bit Control Register for UtilCfg

7	6	5	4	3	2	1	0
GPOUT_HL	GPOUT_ENA	Reserved					
rw-0	rw-0	rw-0					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. REG6E 8-Bit Control Register for UtilCfg Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	GPOUT_HL	RW	0h	General-purpose output (GPOUT) pin output selection 0h = Low output 1h = High output Valid only if REG6F = 00h
6	GPOUT_ENA	RW	0h	Enable monitor signal output to GPOUT pin 0h = No signal output, Hi-Z 1h = Output signal selected in REG6F with CMOS output Output is logical OR when selected two more signals
5-0	Reserved	RW	0h	

8.6.4.35 REG6F 8-Bit Control Register for GPOUTSet (offset = 6Fh)

Figure 48. REG6F 8-Bit Control Register for GPOUTSet

7	6	5	4	3	2	1	0
ACTTIMER_FLT_MON	MONITOR_MON	Reserved	PWRERR_MON	TSDERR_MON	SCPERR_MON	TSDFAULT_MON	SPMRCD_BRK_MON
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. REG6F 8-Bit Control Register for GPOUTSet Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ACTTIMER_FLT_MON	RW	0h	1h = ACTTIMER fault output to GPOUT pin
6	MONITOR_MON	RW	0h	1h = ENDDET monitor output to GPOUT pin
5	Reserved	RW	0h	
4	PWRERR_MON	RW	0h	1h = PWRERR monitor output to GPOUT pin
3	TSDERR_MON	RW	0h	1h = TSDERR fault output to GPOUT pin
2	SCPERR_MON	RW	0h	1h = SCPERR fault output to GPOUT pin
1	TSDFAULT_MON	RW	0h	1h = TSDFAULT fault output to GPOUT pin
0	SPMRCD_BRK_MON	RW	0h	1h = SPMRCD_BRK fault output to GPOUT pin

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DAC Type

The TPIC2060A has nine-channel drivers and each channel is assigned to the most suitable DAC engine with a different type. ACT (FCS/TRK/TLT) has a 12-bit DAC. The upper 8 (MSB sign bit) are sampled in 5 MHz, and LSB 4 bits are output in sequence with 1.25-MHz PWM. SPIN and load DAC have the same types and sampling rate with 312 kHz. The SPM channel has 14× gain, and other channels (except SLED and STP) have 6× gain. The DAC for STP is 8-bit resolution output with 40-kHz PWM, and no feedback. The gain for STP is 5× relative to P5V voltage. Table 42 shows the configuration of each driver.

Table 42. DAC Type

	FCS/TRK/TLT	SLED	SPIN	LOAD	STP
Resolution	12 bit	10 bit	12 bit	12 bit	8 bit
Type	8-bit oversampling	10-bit voltage DAC	8-bit oversampling	8-bit oversampling	1-bit direct duty PWM
Sampling	1.25M / 10 bit 312K / 12 bit		312K	312K	40 kHz
PWM frequency	312 kHz	About 156 kHz (variable)	156 kHz	312 kHz	40 kHz
Out range	±6 V	±880 mA	±14 V	±6V	±(P5V*1)
Feedback	Voltage F/B	Current F/B	Power supply compensation	Voltage F/B shared with TRK	Direct PWM No F/B

9.1.2 Example of 12-Bit DAC Sampling Rate for FCS/TRK/TLT

The input data is separated in the upper 8 bits and the lower 4 bits. Upper 8 bits (MSB sign 1 bit) are put into 8-bit current DAC in every 5 MHz. The lower 4 bits are put into one bit current DAC in sequence from upper to lower bit. This is a one-bit DAC output with PWM in 1.25 MHz. Any PWM duty, 100%, 75%, 50%, 25%, or 0%, is summed in 8-bit current DAC every 1.25 MHz. Thus, it takes 3.2 µs for all lower 4 bits summing to the PWM output. As a result, 12-bit data is sampled in every PWM cycle. Figure 49 shows an example of the sampling rate for FCS/TRK/TLT.

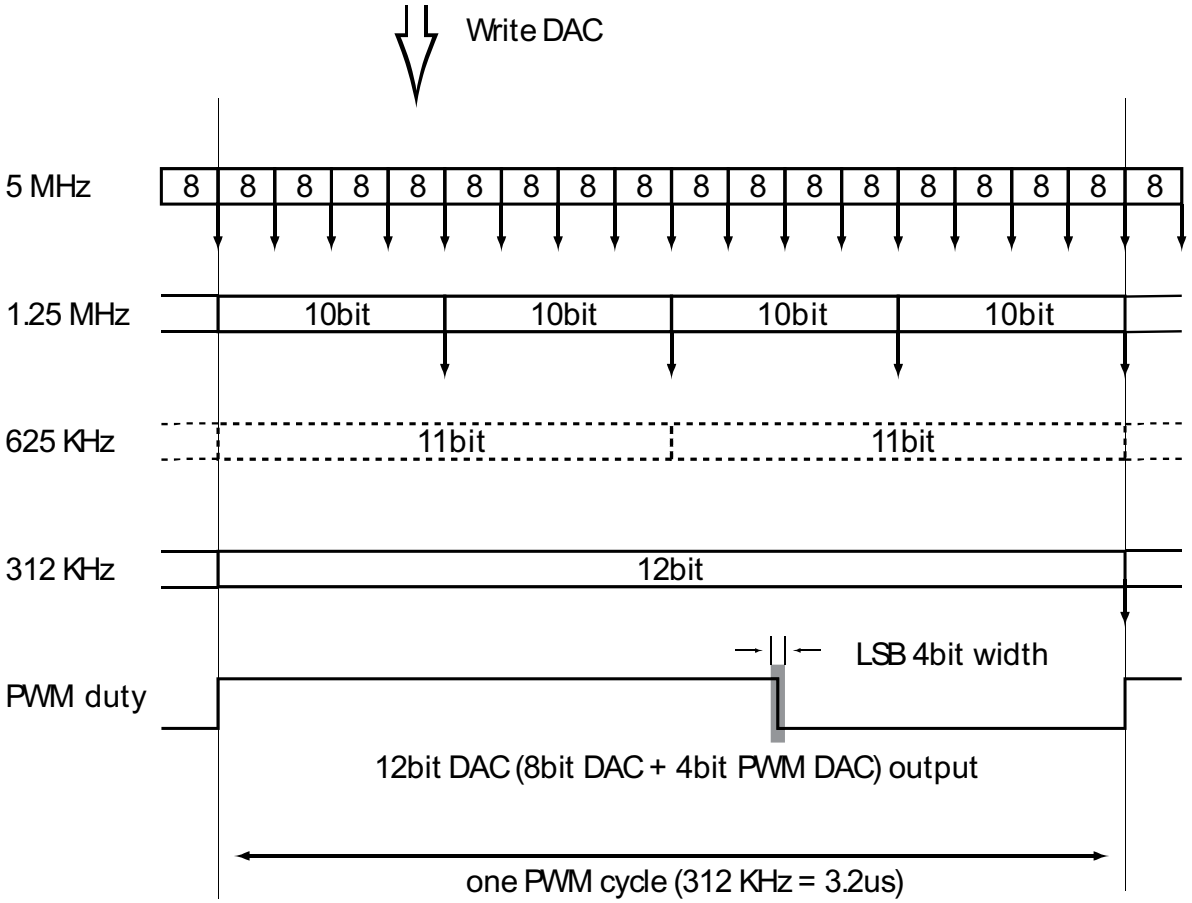


Figure 49. Example of 12-Bit DAC Conversion Time (FCS/TRK/TLT)

9.1.3 Digital Input Coding

The output voltage (current) is commanded through programming to the DAC. All of the DAC input format is 12 bit in complements of 2's, though some DAC has a low resolution. When 12 bits of data is input as 8-bits DAC, the TPIC2060A recognizes four subordinate position bits (LSB) as 0. To arrange for 12-bit DAC format, DSP should shift 8-bit or 10-bit data to an appropriate bit position. The full scale is ±1.0 V and driver gain is set to 6 or 14. The output voltage (V_{out}) is given by the following equation:

$$Vout = DACcode \times \frac{6.0}{2048}$$

$$VSPMout = DACcode \times \frac{14.0}{2048}$$

Calculation by fixed point number :

$$Vdac = 1.0 \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + ... + bit[0] \times 0.5^{11}\right)$$

$$Vdac = (-1.0) \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + ... + bit[0] \times 0.5^{11} + 0.5^{12}\right)$$

$$Vout = Vdac \times 6.0 \ (V)$$

$$VSPMout = Vdac \times 14.0 \ (V)$$

$$STPVout = Vdac \times (P5V) \ (V)$$

$$SLEDIout = Vdac \times 0.88 \ (A)$$

where bit[11:0] is the digital input value, range 000000000000b to 111111111111b (3)

Table 43. DAC Format

MSB Digital input (BIN) LSB	Hex	Dec	Vdac	Analog Output (5 V)	Analog Output (12 V)
1000_0000_0000	0x800	–2048	–0.9995	–5.997	–13.993
1000_0000_0001	0x801	–2047	–0.9995	–5.997	–13.993
1111_1111_1111	0xFFF	–1	–0.0005	–0.003	–0.007
0000_0000_0000	0x000	0	0	0.000	0.000
0000_0000_0001	0x001	1	0.0005	0.003	0.007
0111_1111_1110	0x7FE	2046	0.9990	5.994	13.986
0111_1111_1111	0x7FF	2047	0.9995	5.997	13.993

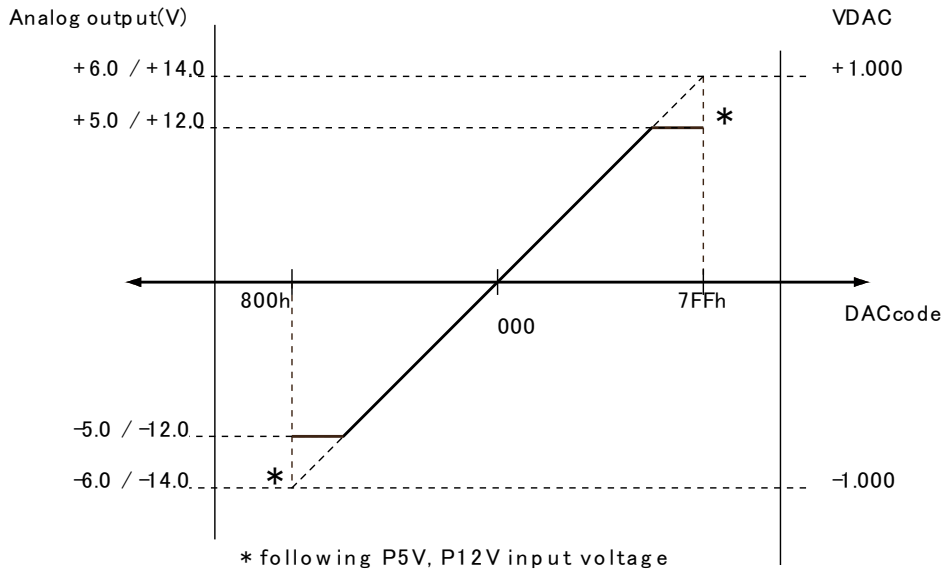


Figure 50. Output Voltage vs DAC Code

9.1.4 Example Timing of Target Control System

The TPIC2060A is designed to meet the requirements for updating control data in 400 kHz. Table 44 lists an example of a control system parameter. It takes 0.51 µs to transmit a 16-bit data packet to the TPIC2060A with a 35-MHz SCLK. Therefore, DSP can be sent four packets at 400-kHz intervals. If the SCLK is lower than 28.8 MHz, the user must reduce packet quantity to less than three. For example, the Focus/Truck command updates every 2.5 µs (400 kHz), and can send another two kinds of packets during this time. Figure 51 shows an example of the control timing when using the TPIC2060A.

Table 44. Example Timing of Target Control System

SIGNAL	BIT	UPDATE CYCLE (kHz)
Focus	12	400
Track	12	400
Tilt	12	100
Sled1	10	100
Sled2	10	100
Spindle	12	100
Load	12	—
Step1	8	40
Step2	8	40

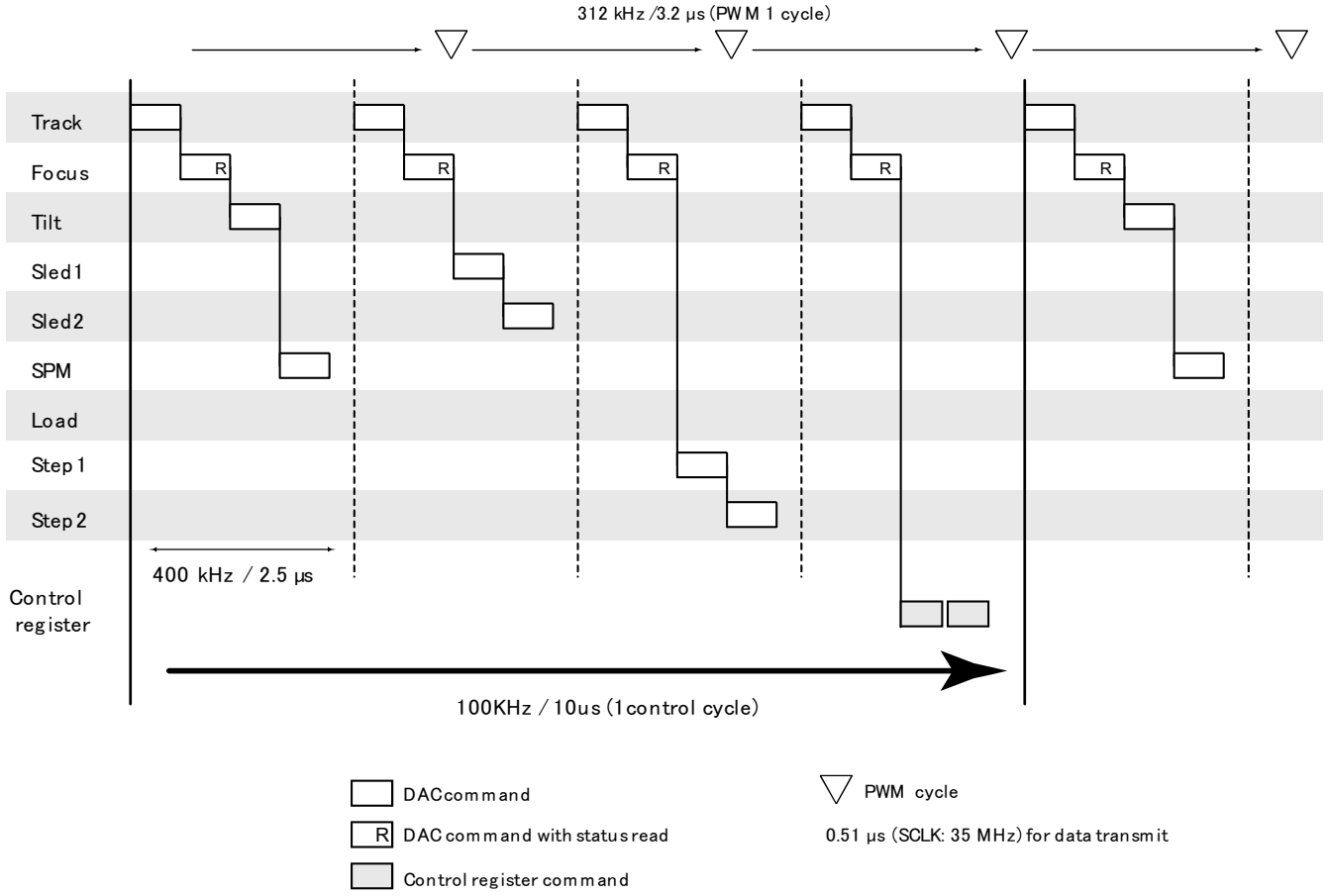


Figure 51. Example DAC Control

9.1.5 Spindle Motor Driver Operating Sequence

When the VSPM is set to a positive DAC code, it goes into acceleration mode. Initial position sense (IS) mode then operates, the start-up circuits offer a start-up pattern sequence to the driver, and then switch to spin-up mode by detecting the rotor position through BEMF signal from the spindle motor coil.

The spin-down and brake functions are also controlled by the DAC value, VSPM. When the brake command to VSPM is set, the driver goes into active-brake mode, switches to short-brake mode in slow revolution speed, and then stops automatically. The FG signal is composed from EXOR of a three-phase signal and is output from XFG pin shown in Figure 52.

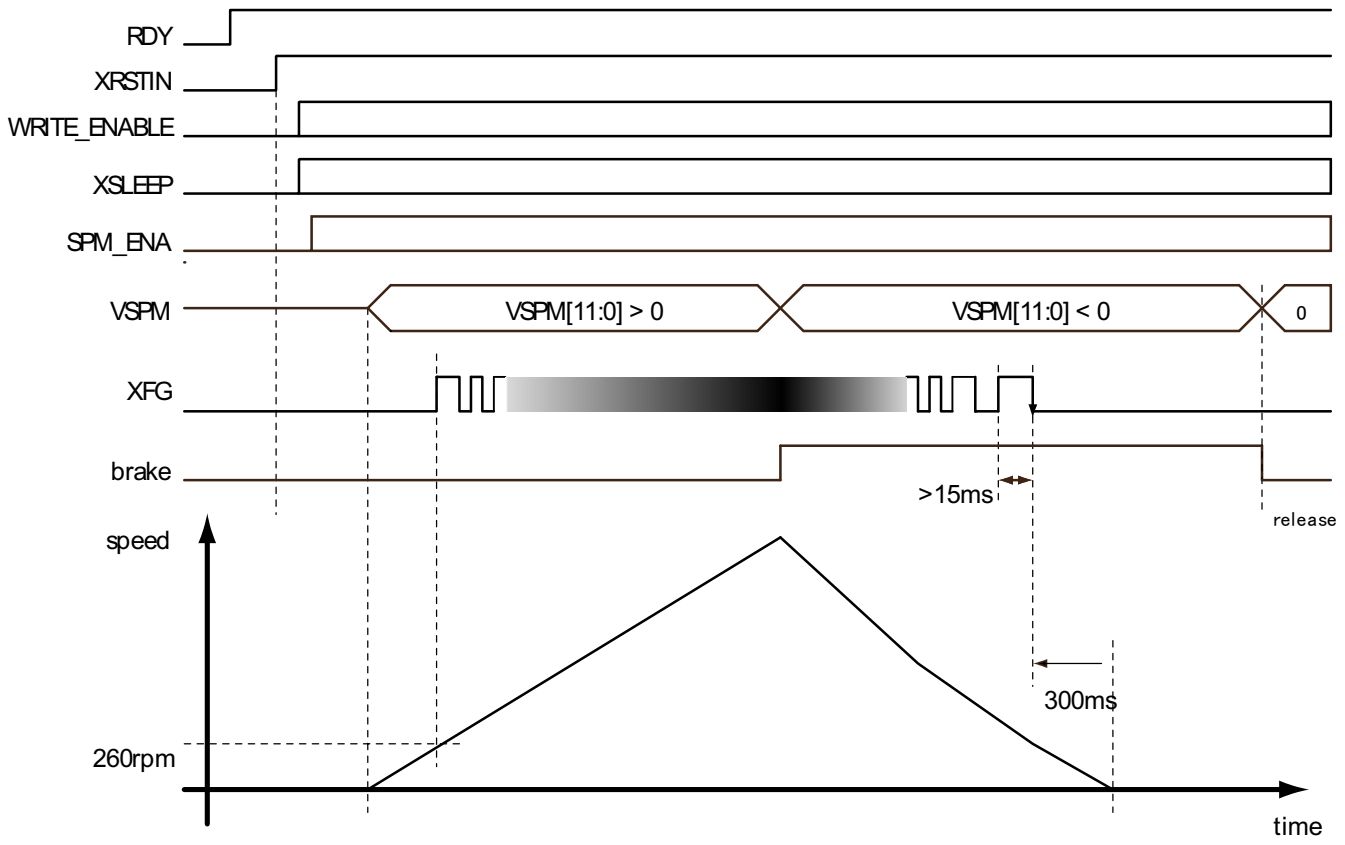


Figure 52. Spindle Operating Sequence

Use the down-edge of the FG signal for monitoring the FG frequency.

Short brake mode is asserted after 300 ms of FG signal stays L-level in deceleration.

This value is the nominal number of using a 12-pole motor.

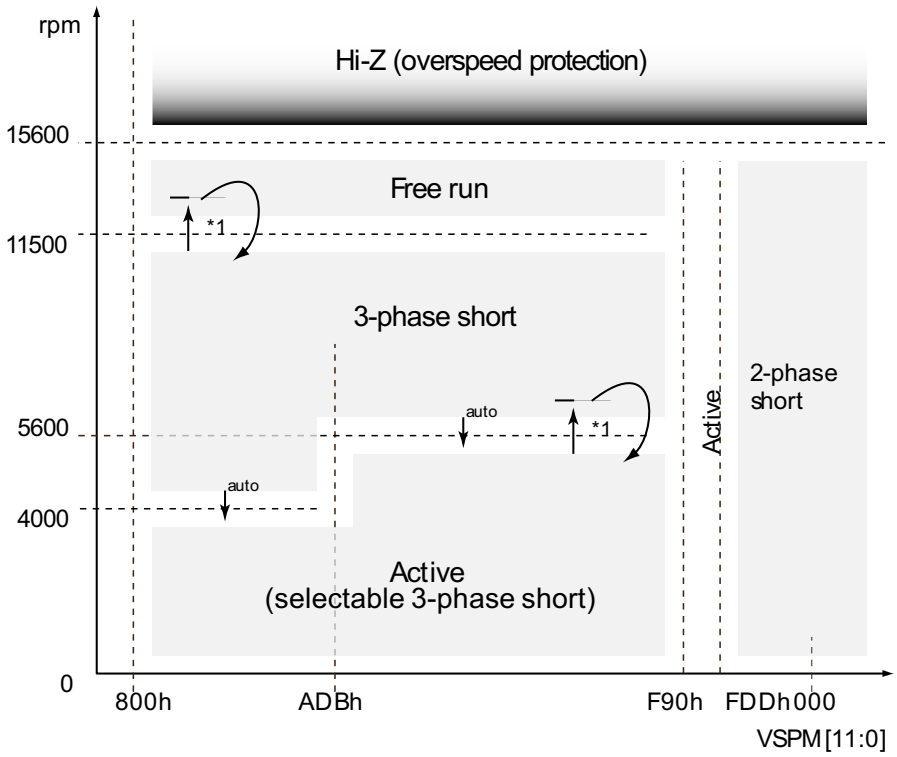
9.1.6 Auto Short Brake Function

The TPIC2060A provides an auto short brake function that selects the brake mode automatically by motor speed. The auto short brake is an intelligent brake function that includes two modes, short brake and active brake. If a value of 0xF90 or less is set to VSPM, brake mode automatically changes at rotation speed. This function enables low-power consumption and silent braking. Table 45 shows the relation between brake mode and speed. The overspeed protection function suspends the SPM driver output at 15000 or more revolutions.

Table 45. Brake Mode

VSPM[11:0]	MODE	ROTATION SPEED (RPM)(1)			
		ABOUT 11500	ABOUT 11500 TO 5600	ABOUT 5600 TO 4000	ABOUT 4000 TO 0
0x000 - 0xFDD	Manual	2-phase short brake			
0xFDC - 0xF90	Manual	Active brake			
0xF8F - 0xADB	Auto short	Free run	3-phase short brake(2)	Active brake	
0xADA - 0x800	Auto short	Free run	3-phase short brake(3)		Active brake

(1) Typical value using 12-pole motor.
(2) Active brake is chosen when it does not exceed 6400 rpm once from a rotation start.
(3) Active brake is chosen when it does not exceed 4600 rpm once from a rotation start.



A. 1* = Each threshold value has hysteresis. Brake mode changes to a specific mode at the threshold speed when it reaches a speed about 15% higher than the threshold speed. These speed values are the nominal number of using a 12-pole motor. In applying to the 16-pole motor, the rotations speed becomes 75% of indicated rpm values.

Figure 53. Brake Mode

9.1.7 Spindle PWM Control

The output PWM duty of the spindle is controlled by DAC code (VSPM). The gain in acceleration setting is always 14 times, while the maximum output is restricted to P12V voltage. A dead band which outputs = 0 exists in the width of plus or minus 0x52, focusing on zero.

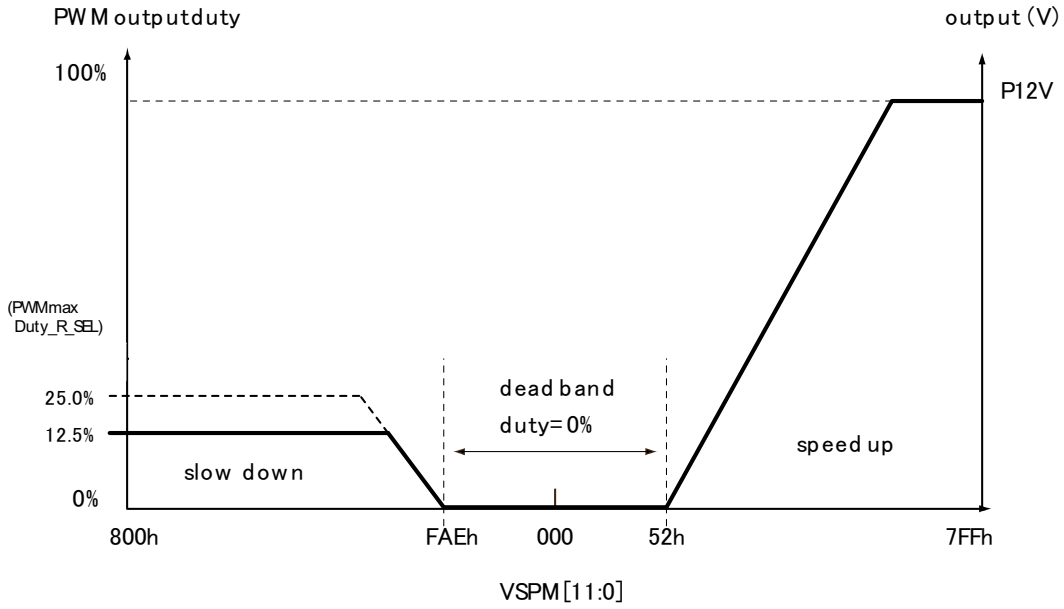


Figure 54. Spindle PWM Control

9.1.8 Spindle Driver Current Limit Circuit

This IC builds in the SPM current sense resistor, which can select the resistor value. The spindle current limit circuit monitors motor current (which flows through this resistance) and limits the output current by reducing PWM duty when detecting overcurrent conditions. Table 46 shows resistor value. A limit current value can be calculated from following formula, where the resistor value is the equivalent resistance for a current limit calculation:

Limit current = 160 mV / resistor value (4)

Table 46. SPM Current Sense Resistor

SPM_RCOM_SEL[1:0]	RESISTANCE VALUE (Ω)(1)	LIMIT CURRENT (mA)
00	0.15	1133
01	0.22	772
10	0.12	1416
11	0.10	1700

(1) The equivalent resistance for current limit calculation.

9.1.9 Sled Driver Part

The sled driver outputs the PWM pulse set as DAC code (VSLDx) with current feedback. The maximum output is restricted to 880 mA at 0x7FF and 0x800. A dead band with output = 0 exists in the width of plus or minus 0x1F focusing on zero.

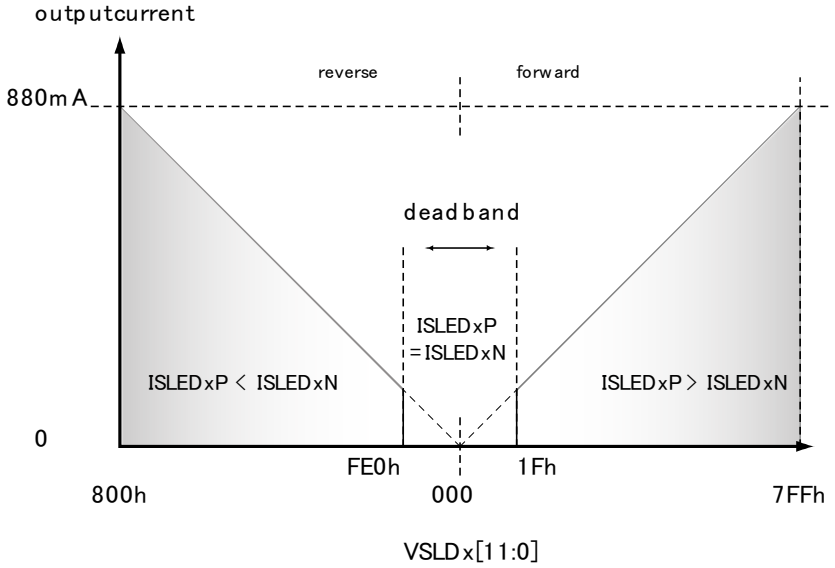


Figure 55. Sled Output Current

Both outputs of SLED1/2 are 'L' when the input code is in the dead band.

9.1.10 Stepping Driver Part

The step driver outputs the PWM pulse set as 8-bit DAC code (VSTPx) using VSTP[11:4]. There is no feedback monitor for output. The pulse duration according to the P5V power supply voltage is outputted.

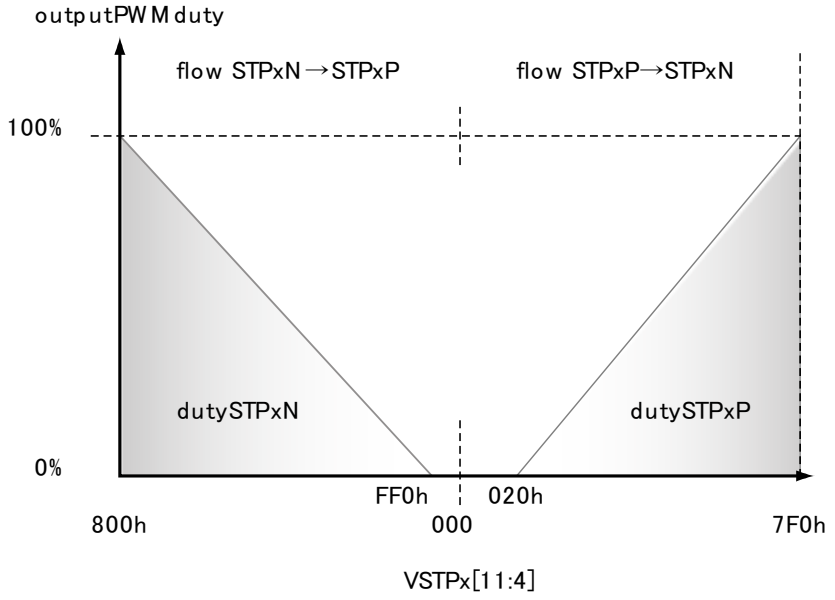


Figure 56. Step Output Duty

9.1.11 Focus/Track/Tilt Driver Part

9.1.11.1 Input VS Output Duty

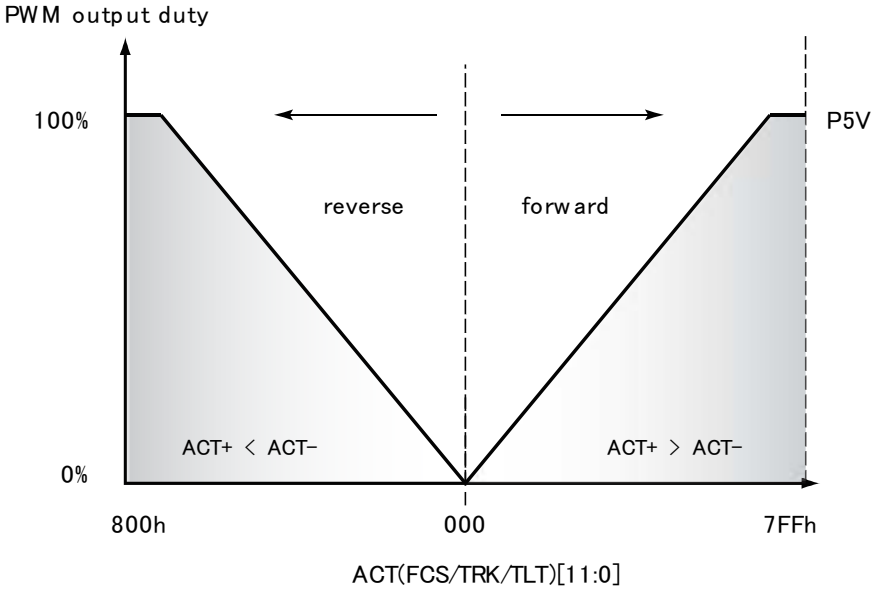


Figure 57. FCS/TRK/TLT Output Duty

9.1.12 Load Driver Part

The load driver outputs the voltage, with voltage feedback corresponding to the input DAC value. This channel has power voltage compensation and therefore is suited for slot-in type load control. This channel becomes active exclusively to other actuator channels. The load driver is shared with the TRK driver.

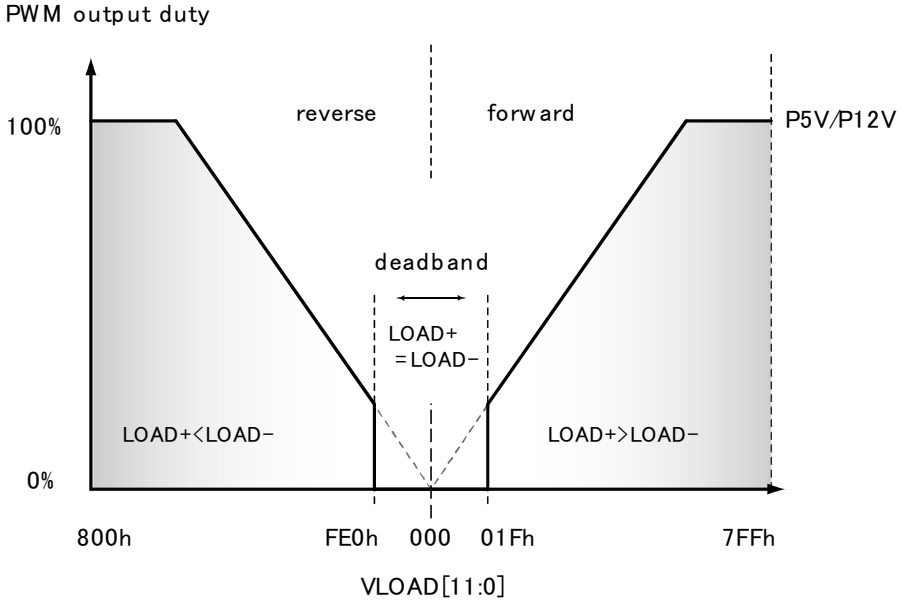


Figure 58. Load Output Duty

9.1.13 End Detect Function

This device has the function of end position detection for sled and collimator lens. This function eliminates the position switch at the PUH inner and collimator lens end position. Sled channel and step channel can be used independently by setting XXX_ENDDET_ENA = 1. When this function is enabled, internal logic detects the sled out zero-cross point, then the internal BEMF detect circuit measures the BEMF level of the stepping motor. There are four threshold levels. If the BEMF is lower than the selected threshold, the device causes the motor to stop and sets the XXX_ENDDET bit to 1. The ENDDET bit is then cleared at the BEMF voltage exceed threshold.

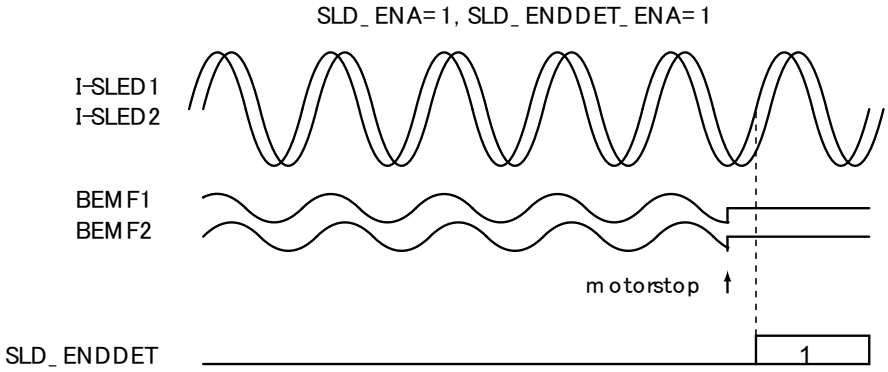


Figure 59. Timing of Sled End Detection

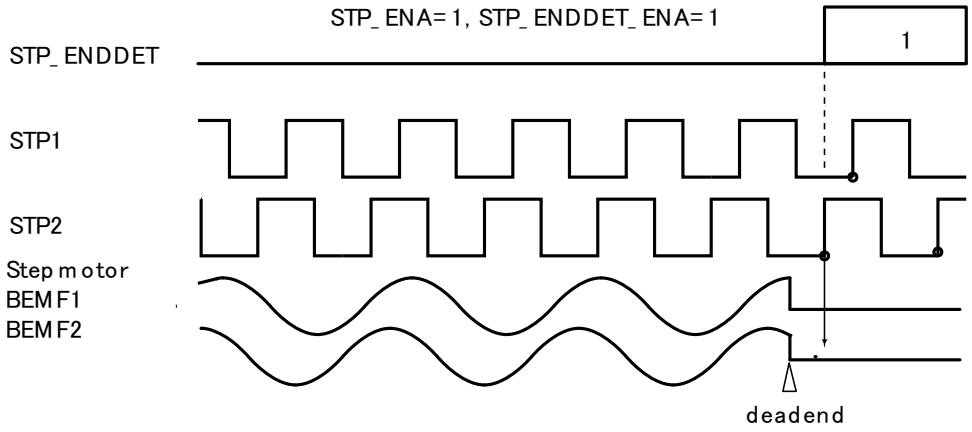


Figure 60. Timing of Step End Detection

9.1.14 Load Tray Lock Detect Function

The tray lock detect function detects inserted obstacles at the time of tray opening and closing, using the load motor BEMF. The user must adjust the TRAY_LOCKDET [2:0] for the optimal threshold level by the characteristics of the motor. By setting TRAY_LOCKDET, the user can select a threshold level from 100 to 400 mA, with a 50-mA step. Observe the lock detection by reading the TRAY_LOCKDETECT flag where LOAD_ENA = 1 is set.

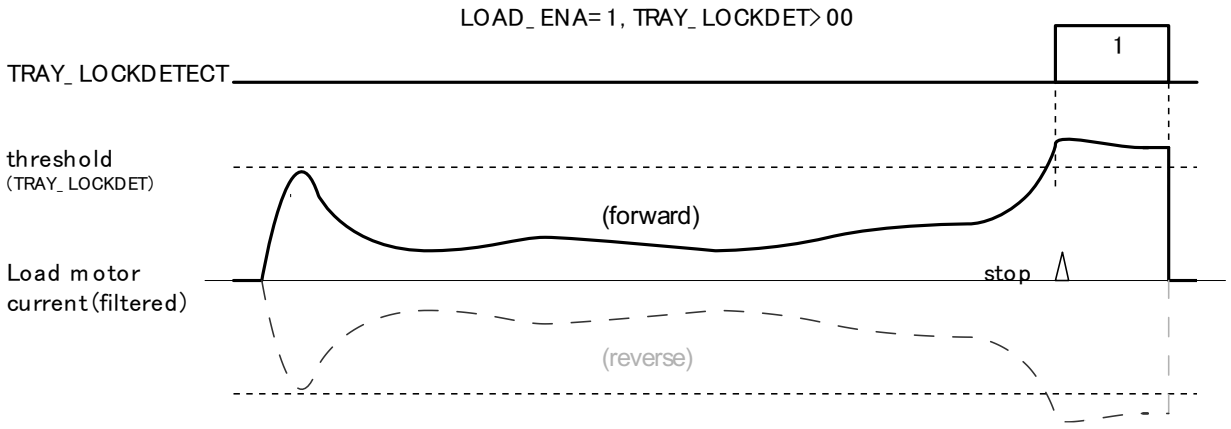


Figure 61. Load Tray Lock Detect

9.1.15 Load Tray Push Detect Function

The load tray can detect the event of push or pull using the TRAY_PUSHDETx flag. The push detect function monitors the motor BEMF voltage of LOAD_P and LOAD_N in the LOAD_ENA = 0. If the motor BEMF voltage exceeds the threshold level, the detection terminal flag is set where the voltage appeared. A detection threshold is determined by voltage (PUSHDETTH) and time (PUSHDET_TIME). Observe the push event by reading the TRAY_PUSHDETP or TRAY_PUSHDETN flags, where LOAD_ENA = 0 is set. Because TRAY_PUSHDETx is a latch flag, it is necessary to reset by RST_ERR_FLAG = 1.

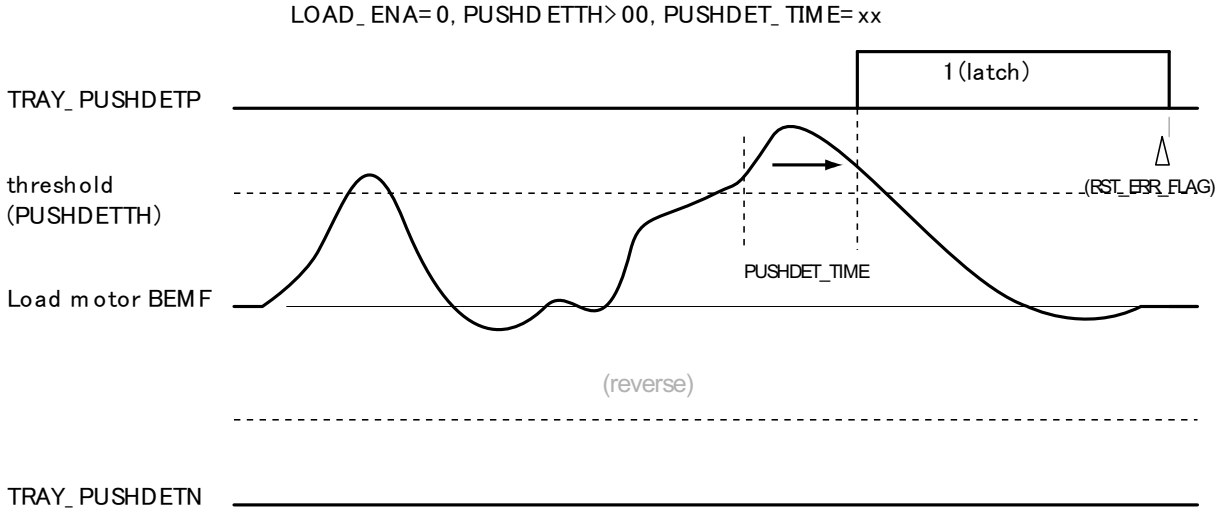


Figure 62. Load Tray Push Detect

9.1.16 Monitor Signal on GPOUT

The device can output a specific signal to the GPOUT pin. To output a signal, choose a signal from REG6F by enabling first, then enable GPOUT_ENA. When two or more signals are set for GPOUT, an output is a logical sum.

9.1.17 9-V LDO

The TPIC2060A has a built-in predriver for 9-V LDO. An arbitrary current can be supplied to the LDO by selecting the external NFET according to required current capacity. LIN9VG output (= NFET gate control) is controlled to the feedback voltage and LINFB is set as 1.215 V. The 220-nF capacitor for phase compensation is installed, and the division resistance for FB is chosen so that it may total less than 11 kΩ. Figure 63 shows an example of external components. The accuracy of the output voltage depends on the tolerance of the resistance. When not using the LDO, open both LIN9VG and LINFB with LIN9V_DISABLE = 1.

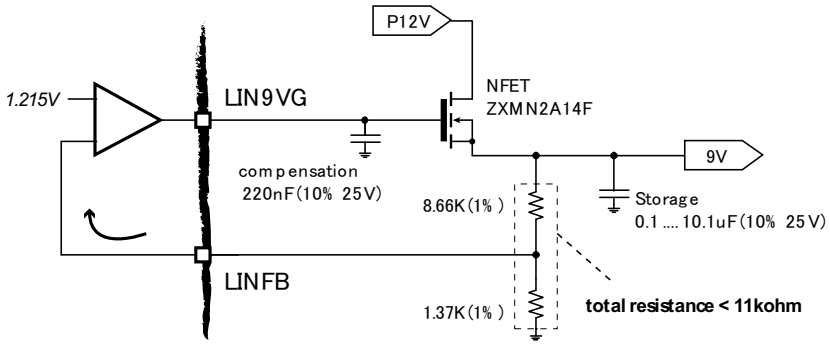


Figure 63. Example Circuit of 9-V LDO

9.2 Typical Application

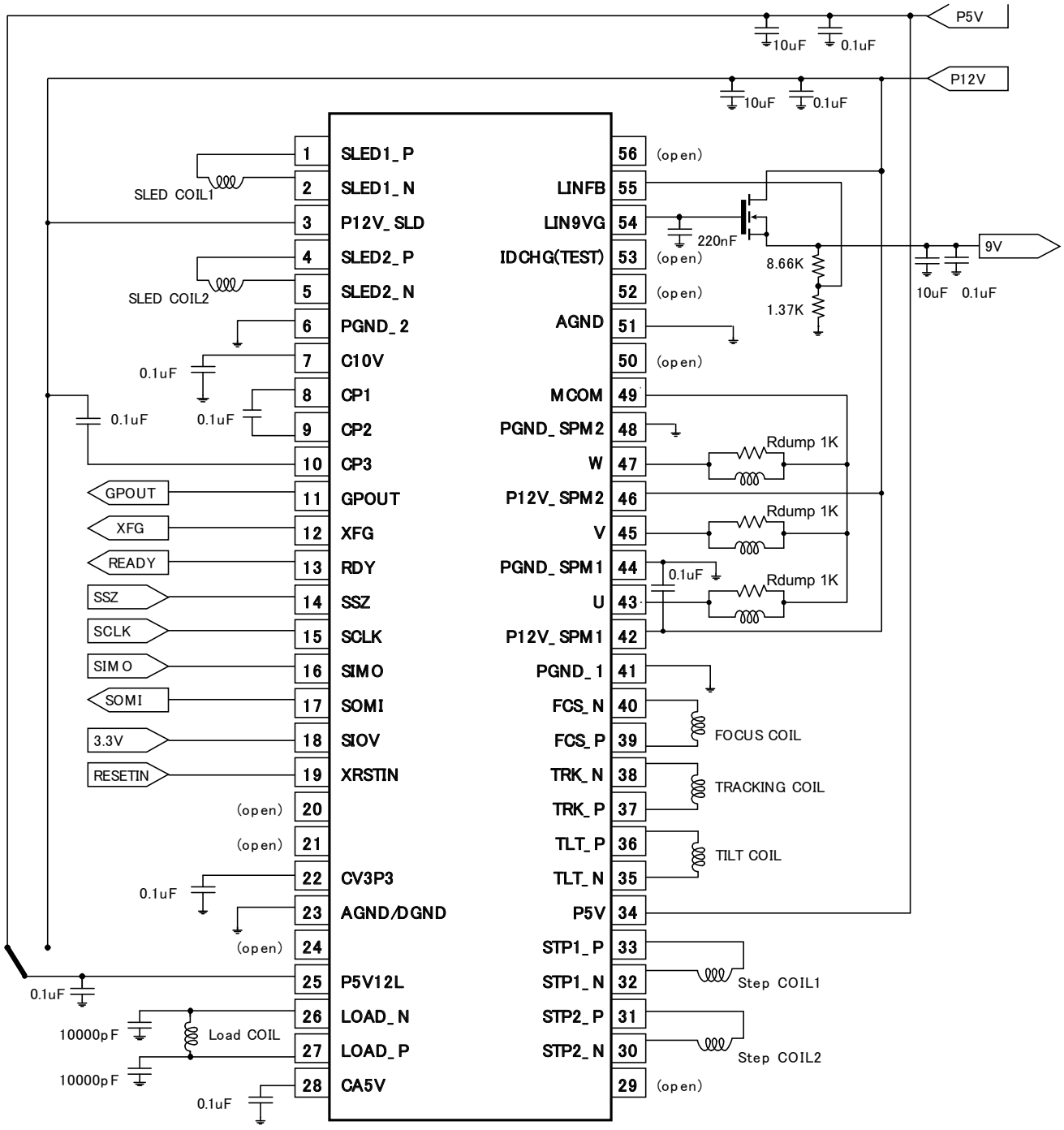


Figure 64. Example of Application Circuit

9.2.1 Design Requirements

To begin the design process, determine the following:

1. Motor configuration. Can use all motor channels or part of them.
2. Usage for 9V LDO predriver. Can be disabled.
3. RDY pin can be connected to Host CPU. Then Host CPU can know the power supply status of TPIC2060A

Typical Application (continued)

9.2.2 Detailed Design Procedure

After power up on 5V and 12V supply, register can be changed following way and enabling motors.

1. Set WRITE_ENABLE=1 on REG76 via SPI.
2. Set XSLEEP=1 at REG70
3. Enable motor channel by ENA_XXX bits on REG70
4. Change the DAC settings for the motor on REG01-0B. Then output channels start driving load.

9.2.3 Application Curves

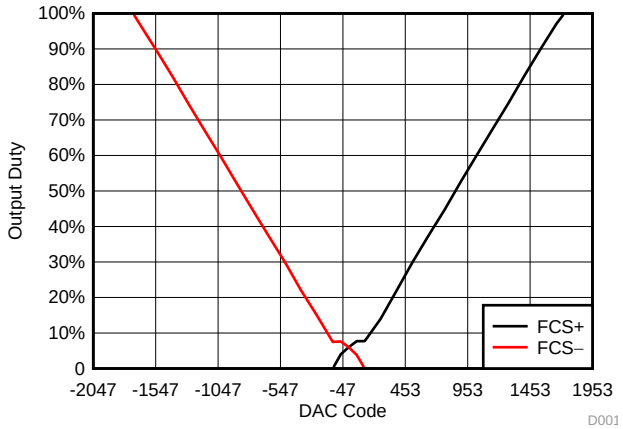


Figure 65. FCS Driver: DAC Code vs Output On Duty

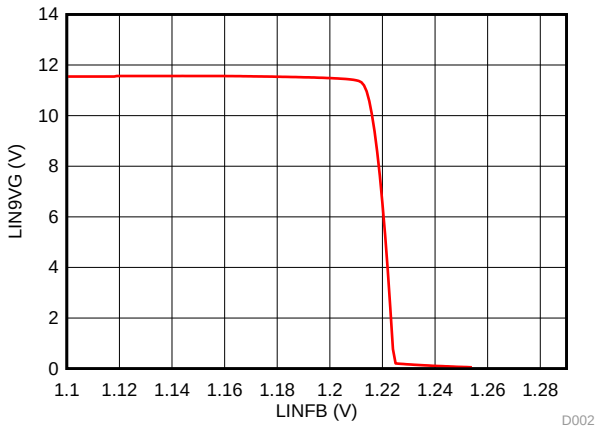


Figure 66. LDO Control: LINFB vs LIN9VG Output

10 Power Supply Recommendations

All driver channels should be operated after the required power is supplied and stable.

The appropriate capacity of the decoupling capacitor requires a value over 10 µF to reduce the influence of PWM switching noise. The P5V pin must connect to a 1-µF filter. Place a bypass capacitor (about 0.1 µF) near the power pin (P5V, P5V12L, P12V_SPM, P12V_SLD) for PWM switching noise reduction on the power and GND lines.

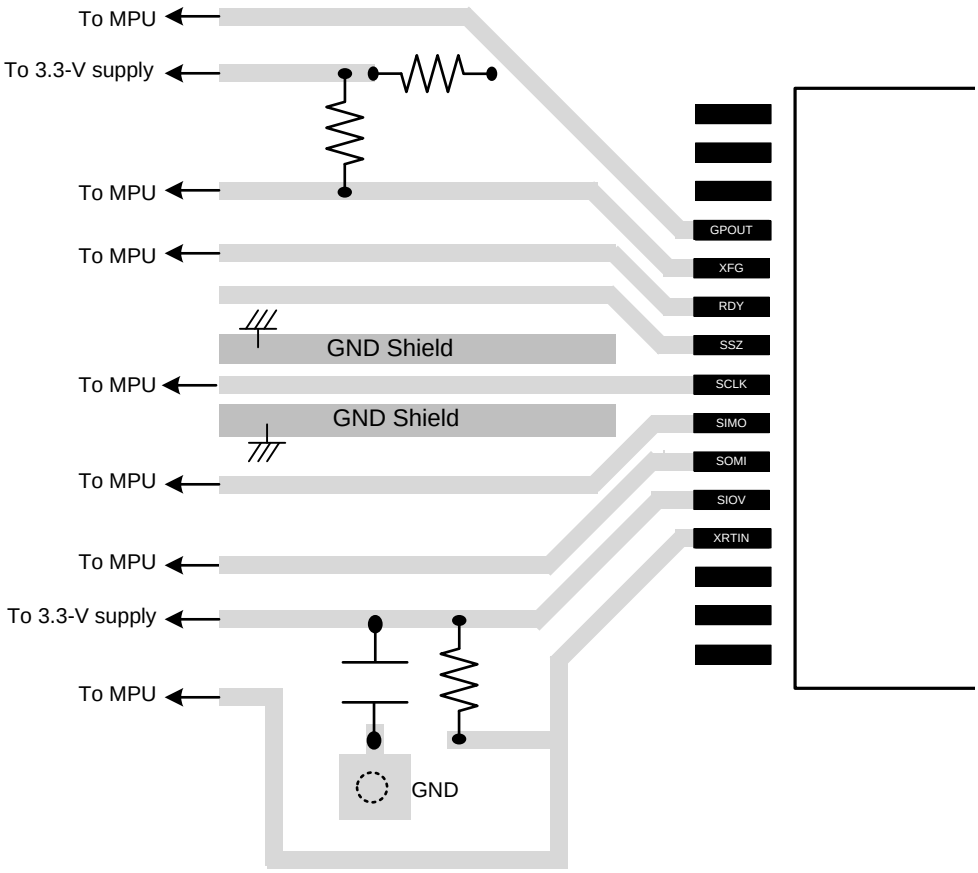
Current flow to the driver circuits takes both pattern-layout, line-impedance, and noise influence from the supply line into consideration.

11 Layout

11.1 Layout Guidelines

1. CV3P3V, CA5V, and C10V requires external capacitor. Because these are reference voltage for device, locate the capacitor as close to device as possible. Keep away from noise source.
2. TI recommends SCLK ground shielding.
3. LINFB is feedback pin for LDO. External divided resistors should be located closer to LINFB pin.

11.2 Layout Example



A. GND shield is recommend for SCLK.

Figure 67. Layout Example between TPIC2060A and MPU

12 器件和文档支持

12.1 社区资源

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC2060ADFDRG4	ACTIVE	HTSSOP	DFD	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 75	2060A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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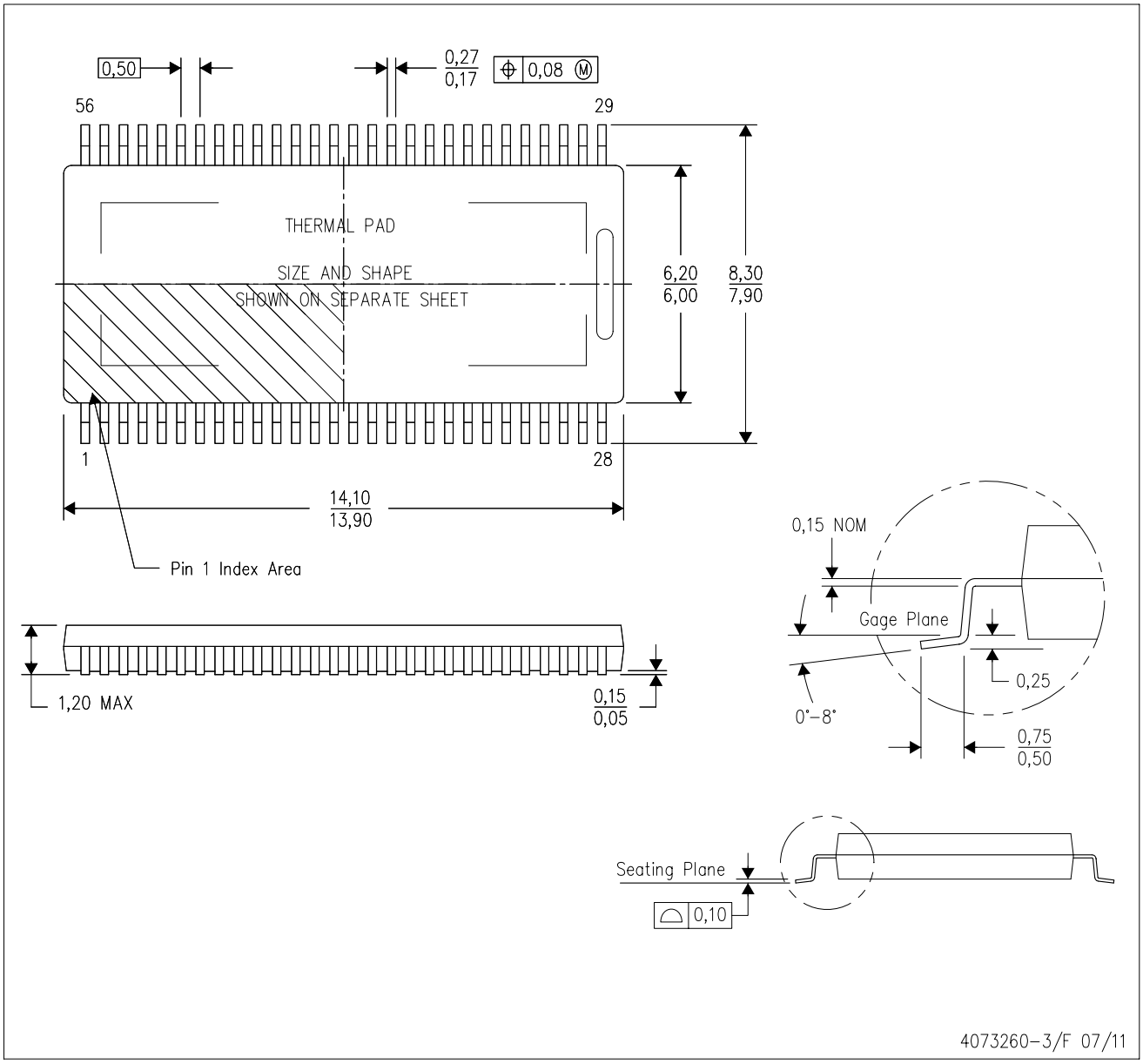


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

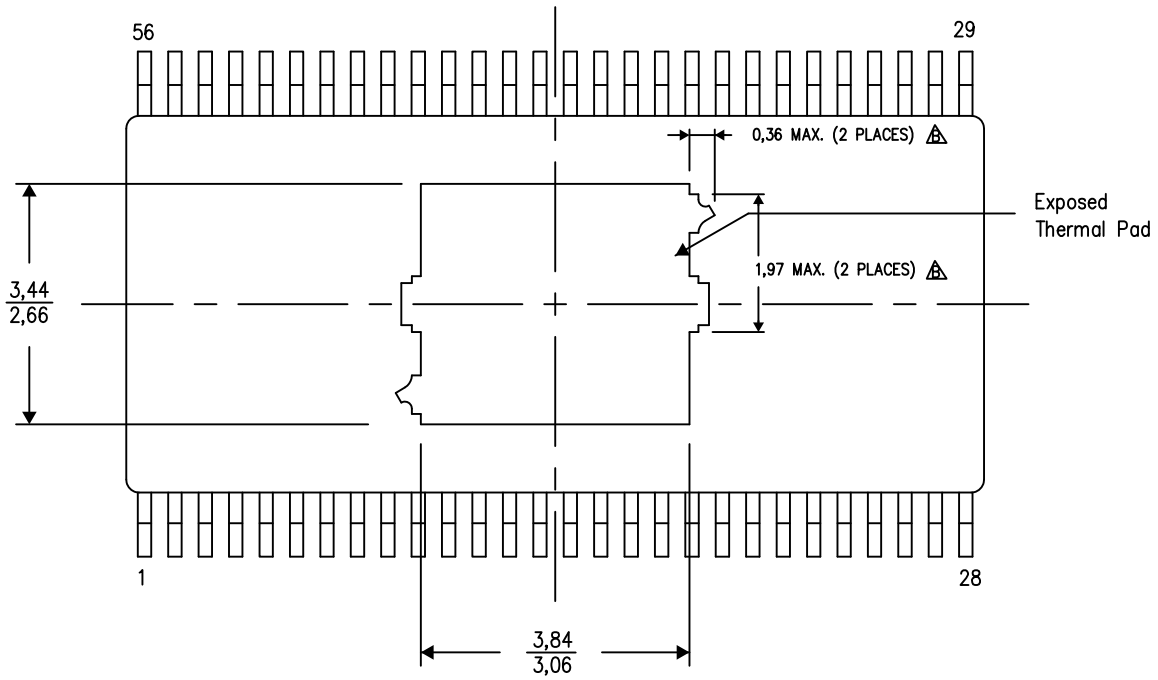
DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4210501–2/G 07/12

NOTES: A. All linear dimensions are in millimeters

B Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

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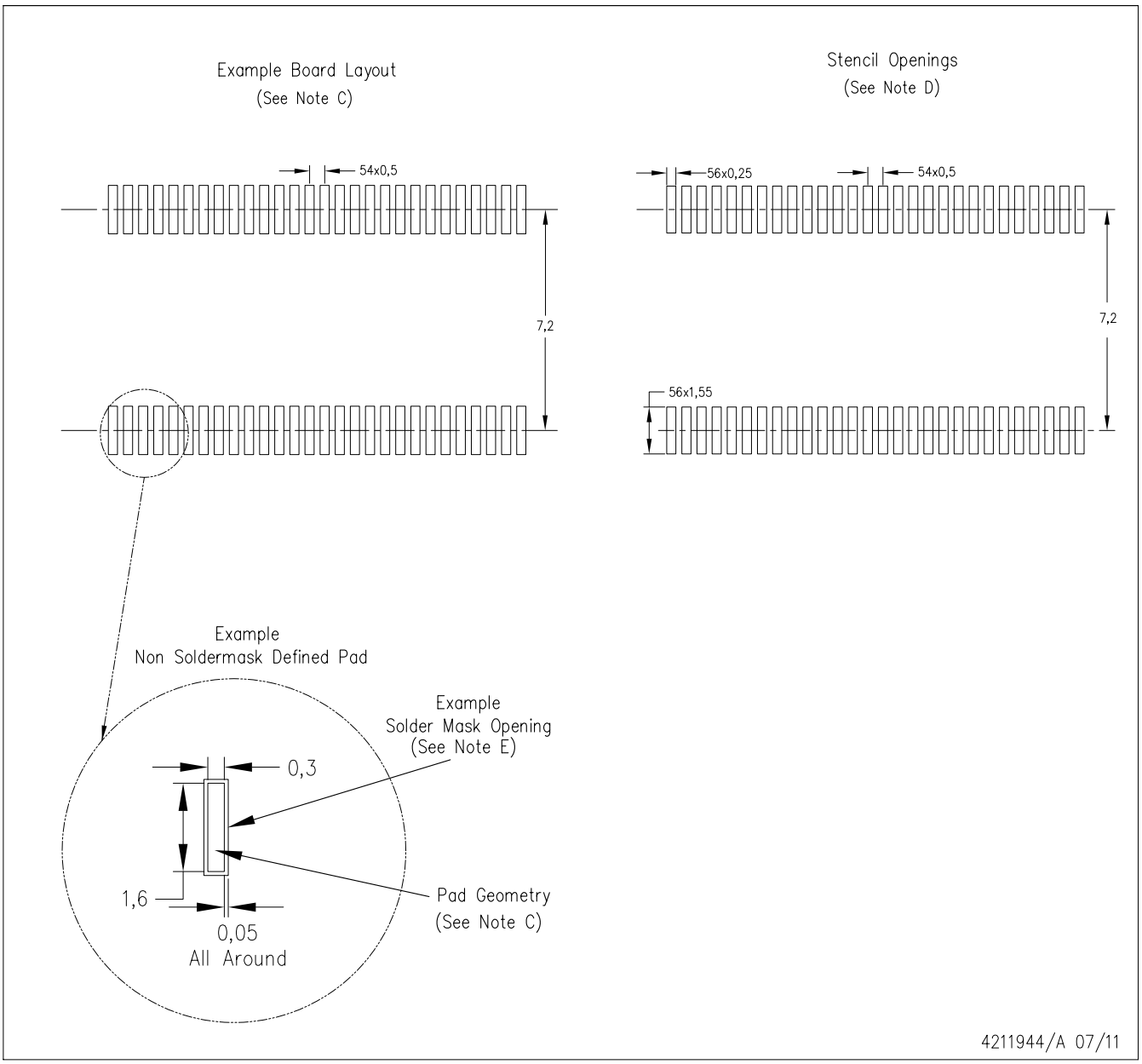

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D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
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