bq78350 补偿放电终点电压 (CEDV) 锂离子电量监测计和电池管理控制器（与 bq769x0 电池监控模拟前端 (AFE) 配套）

1 特性

- 补偿放电终点电压 (CEDV) 电量计量算法
- 支持 SMBus 主机通信
- 可灵活配置 3 到 5 节 (bq76920)、6 到 10 节 (bq76930) 以及 9 到 15 节 (bq76940) 锂离子和磷酸铁锂电池
- 支持高达 320Ahr 的电池配置
- 支持高达 320A 的充放电电流
- 通过配套 AFE 支持外部负温度系数 (NTC) 热敏电阻
- 可编程保护特性的完全阵列
  - 电压
  - 电流
  - 温度
  - 系统元件
- 使用寿命的数据记录
- 支持 CC-CV 充电，包括预充电、充电禁止和充电暂停
- 为多达八个不同的总线地址提供一个可选电阻器可编程 SMBus 从地址
- 最多可驱动一个 5 段 LED 或 LCD 显示屏，以指示充电状态
- 提供安全散列算法 (SHA-1) 认证

2 应用

- 轻型电动车辆 (LEV)：电动自行车 (eBike)、电动踏板车 (eScooter)、脚踏电动自行车 (Pedelec) 和踏板辅助自行车
- 电动和园艺工具
- 备用电池和不间断电源 (UPS) 系统
- 无线基站后备系统
- 电信电源系统

3 说明

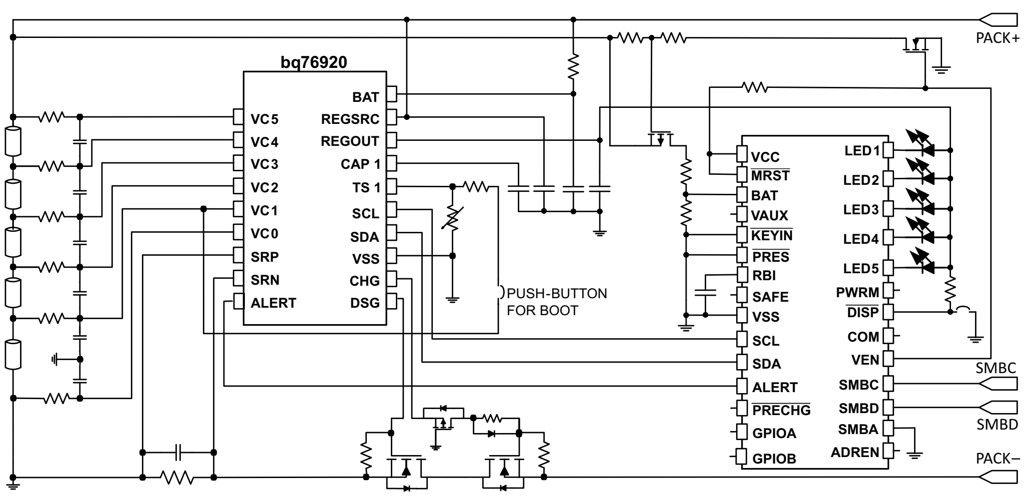
德州仪器 (TI) bq78350 锂离子和磷酸铁锂电池管理控制器与 bq769x0 系列模拟前端 (AFE) 保护器件配套，可提供全套电池管理系统 (BMS) 子系统，有助于加快产品开发、缩短上市时间。

器件信息(1)

部件号	封装	封装尺寸（标称值）
bq78350	TSSOP (30)	7.80mm x 6.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



English Data Sheet: SLUSB48

目录

1 特性 1
2 应用 1
3 说明 1
4 简化电路原理图 1
5 修订历史记录 2
6 说明（续） 3
7 **Pin Configuration and Functions** 4
8 **Specifications** 6
8.1 Absolute Maximum Ratings 6
8.2 Handling Ratings 6
8.3 Recommended Operating Conditions 6
8.4 Thermal Information 7
8.5 Electrical Characteristics: Supply Current 7
8.6 Electrical Characteristics: I/O 7
8.7 Electrical Characteristics: ADC 8
8.8 Electrical Characteristics: Power-On Reset 8
8.9 Electrical Characteristics: Oscillator 8
8.10 Electrical Characteristics: Data Flash Memory 8
8.11 Electrical Characteristics: Register Backup 9
8.12 SMBus Timing Specifications 10
8.13 Typical Characteristics 11
9 **Detailed Description** 12
9.1 Overview 12
9.2 Functional Block Diagram 12
9.3 Feature Description 12
9.4 Device Functional Modes 14
9.5 Programming 15
10 **Application and Implementation** 16
10.1 Application Information 16
10.2 Typical Applications 16
11 **Power Supply Recommendations** 25
12 **Layout** 26
12.1 Layout Guidelines 26
12.2 Layout Example 27
13 器件和文档支持 28
13.1 相关文档 28
13.2 商标 28
13.3 静电放电警告 28
13.4 术语表 28
14 机械封装和可订购信息 28

5 修订历史记录

日期	修订版本	注释
2014 年 7 月	*	最初发布版本

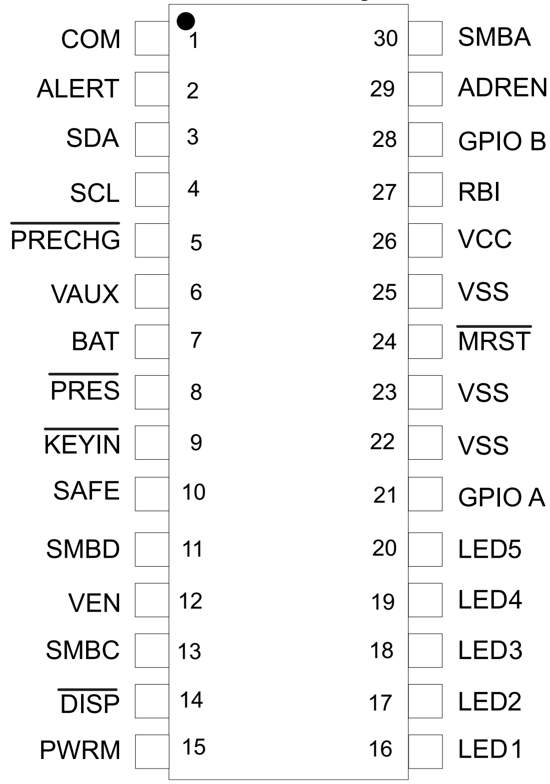
6 说明（续）

bq78350 控制器和 bq769x0 AFE 支持 3 节到 15 节电池应用。 bq78350 提供了精确的电量监测计和健康状况 (SoH) 监控器，还提供了电池平衡功能以及一套完整的电压、电流和温度保护功能。

bq78350 提供了用于报告容量的选配 LED 或 LCD 显示屏配置。 它还可通过 SMBus 1.1 接口传输数据。 电池历史记录和诊断数据也保存在器件的非易失性存储器中，并且可通过同一接口获取。

7 Pin Configuration and Functions

30-Pin DBT Package



Pin Functions

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
1	COM	O	Open Drain Output LCD common connection
2	ALERT	I/O	Input/Output to the bq769x0 AFE
3	SDA	I/O	Data transfer to and from the bq769x0 AFE. Requires a 10-k pullup to VCC.
4	SCL	I/O	Communication clock to the bq769x0 AFE. Requires a 10-k pullup to VCC.
5	$\overline{\text{PRECHG}}$	O	Programmable polarity (default is active low) output to enable an optional precharge FET. This pin has an internal pullup to 2.5 V when configured as active high, and is open drain when configured as active low.
6	VAUX	AI	Auxiliary voltage input
7	BAT	AI	Translated battery voltage input
8	$\overline{\text{PRES}}$	I	Active low input to sense system insertion. This typically requires additional ESD protection. If this pin is not used, then it should be tied to VSS.
9	$\overline{\text{KEYIN}}$	I	A low level indicates application key-switch is inactive on position. A high level causes the DSG protection FET to open.
10	SAFE	O	Active high output to enforce an additional level of safety protection (for example, fuse blow)
11	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer an address and data to and from the bq78350
12	VEN	O	Active high voltage translation enable. This open drain signal is used to switch the input voltage divider on/off to reduce the power consumption of the BAT translation divider network.
13	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq78350
14	$\overline{\text{DISP}}$	I	Display control for the LEDs. This pin is typically connected to bq78350 REGOUT via a 100-KΩ resistor and a push-button switch connect to VSS. Not used with LCD display enabled and can be tied to VSS.

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
15	PWRM	O	Power mode state indicator open drain output
16	LED1	O	LED1/LCD1 display segment that drives an external LED/LCD, depending on the firmware configuration
17	LED2	O	LED2/LCD2 display segment that drives an external LED/LCD, depending on the firmware configuration
18	LED3	O	LED3/LCD3 display segment that drives an external LED/LCD, depending on the firmware configuration
19	LED4	O	LED4/LCD4 display segment that drives an external LED/LCD, depending on the firmware configuration
20	LED5	O	LED5/LCD5 display segment that drives an external LED/LCD, depending on the firmware configuration
21	GPIO A	I/O	Configurable Input or Output. If not used, tie to VSS.
22	VSS	—	Negative supply voltage
23	VSS	—	Negative supply voltage
24	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. This pin must be held high for normal operation.
25	VSS	—	Negative supply voltage
26	VCC	P	Positive supply voltage
27	RBI	P	RAM backup input. Connect a capacitor to this pin and VSS to protect loss of RAM data in case of short circuit condition.
28	GPIO B	I/O	Configurable Input or Output. If not used, tie to VSS.
29	ADREN	O	Optional digital signal enables address detection measurement to reduce power consumption.
30	SMBA	IA	Optional SMBus address detection input

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC} relative to V_{SS}	Supply voltage range	–0.3	2.75	V
$V_{(IOD)}$ relative to V_{SS}	Open-drain I/O pins	–0.3	6	V
V_I relative to V_{SS}	Input voltage range to all other pins	–0.3	VCC + 0.3	V
T_A	Operating free-air temperature range	–40	85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

8.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
V_{ESD}[1]	Human Body Model (HBM) ESD stress voltage[2]	–2	2	kV
	Charged Device Model (CDM) ESD stress voltage[3]	–500	500	V

(1) Electrostatic discharge (ESD) that measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM enables safe manufacturing with a standard ESD control process. Pins listed as 1000 V may actually have a higher performance.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM enables safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have a higher performance.

8.3 Recommended Operating Conditions

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.4	2.5	2.6	V
V_O	Output voltage range	SAFE			V_{CC}	V
		SMBC, SMBD, VEN			5.5	
		ADREN, GPIO A, GPIO B, SDATA, SCLK, PWRM, LED1...5 (when used as GPO)			V_{CC}	
V_{IN}	Input voltage range	BAT, VAUX, SMBA			1	V
		SMBD, SMBC, ALERT, $\overline{DISP}$, $\overline{PRES}$, KEYIN			5.5	
		SDATA, GPIO A, GPIO B, LED1...5 (when used as GPI)			V_{CC}	
T_{OPR}	Operating Temperature		–40		85	°C

8.4 Thermal Information

THERMAL METRIC[1]		bq78350 TSSOP (DBT) 30 PINS	bq78350 QFN (RSM) 32 PINS	UNIT
$R_{JA, High K}$	Junction-to-ambient thermal resistance[2]	81.4	37.4	°C/W
$R_{JC(top)}$	Junction-to-case(top) thermal resistance[3]	16.2	30.6	
R_{JB}	Junction-to-board thermal resistance[4]	34.1	7.7	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.4	0.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	33.6	7.5	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance[7]	n/a	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

8.5 Electrical Characteristics: Supply Current

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating mode current	No flash programming		650[1]		μA
$I_{(SLEEP)}$	Low-power storage mode current	SLEEP mode		300[2]		μA
$I_{(SHUTDOWN)}$	Low-power SHUTDOWN mode current	SHUTDOWN mode		0.1	1	μA

(1) The actual current consumption of this mode fluctuates during operation over a 1-s period. The value shown is an average using the default data flash configuration.
(2) The actual current consumption of this mode fluctuates during operation over a user-configurable period. The value shown is an average using the default data flash configuration.

8.6 Electrical Characteristics: I/O

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage low SMBC, SMBD, SDATA, SCLK, SAFE, ADREN, VEN, GPIO A, GPIO B, PWRM	I_{OL} = 0.5 mA			0.4	V
	Output voltage low LED1, LED2, LED3, LED4, LED5	I_{OL} = 3 mA			0.4	
V_{OH}	Output voltage high SMBC, SMBD, SDATA, SCLK, SAFE, ADREN, VEN, GPIO A, GPIO B, PWRM	I_{OH} = –1 mA	V_{CC} – 0.5			V
V_{IL}	Input voltage low SMBC, SMBD, SDATA, SCLK, $\overline{ALERT}$, $\overline{DISP}$, SMBA, GPIO A, GPIO B, $\overline{PRES}$, KEYIN		–0.3		0.8	V
V_{IH}	Input voltage high SMBC, SMBD, SDATA, SCLK, ALERT, SMBA, GPIO A, GPIO B		2		6	V
	Input voltage high $\overline{DISP}$, $\overline{PRES}$, KEYIN		2		V_{CC} + 0.3	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	μA

8.7 Electrical Characteristics: ADC

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	BAT, VAUX	–0.2		1	V
Conversion time		31.5			ms
Resolution (no missing codes)		16			bits
Effective resolution		14		15	bits
Integral nonlinearity		±0.03%			FSR[1]
Offset error[2]		140		250	µV
Offset error drift[2]	T_A = 25°C to 85°C	2.5		18	V/°C
Full-scale error[3]		±0.1%		±0.7%	
Full-scale error drift		50			PPM/°C
Effective input resistance[4]		8			MΩ

(1) Full-scale reference
(2) Post-calibration performance and no I/O changes during conversion with SRN as the ground reference
(3) Uncalibrated performance. This gain error can be eliminated with external calibration.
(4) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

8.8 Electrical Characteristics: Power-On Reset

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input		1.7	1.8	1.9	V
V_{HYS}	Power-on reset hysteresis		50	125	200	mV

8.9 Electrical Characteristics: Oscillator

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency				4.194	MHz
$f_{(EIO)}$	Frequency error[1][2]		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2	0.25	2	
$t_{(SXO)}$	Start-up time[3]			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error[2][4]		–2.5%	0.25%	2.5%	
		TA = 20°C to 70°C	–1.5	0.25	1.5	
$t_{(LSXO)}$	Start-up time[5]				500	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{CC} = 2.5 V, TA = 25°C.
(3) The start-up time is defined as the time it takes for the oscillator output frequency to be within 1% of the specified frequency.
(4) The frequency error is measured from 32.768 kHz.
(5) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.

8.10 Electrical Characteristics: Data Flash Memory

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention	See note[1]	10			Years
	Flash programming write-cycles	See note[1]	20,000			Cycles
$t_{(WORDPROG)}$	Word programming time	See note[1]			2	ms
$I_{(DDdPROG)}$	Flash-write supply current	See note[1]		5	10	mA

(1) Specified by design. Not production tested.

8.11 Electrical Characteristics: Register Backup

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RB)}$	RB data-retention input current	$V_{(RB)} > V_{(RBMIN)}$, VCC < VIT–			1500	nA
		$V_{(RB)} > V_{(RBMIN)}$, VCC < VIT–, TA = 0°C to 50°C		40	160	
$V_{(RB)}$	RB data-retention voltage (1)		1.7			V

8.12 SMBus Timing Specifications

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		
t_{BUF}	Bus free time between start and stop		4.7			ms
$t_{HD:STA}$	Hold time after (repeated) start		4			
$t_{SU:STA}$	Repeated start setup time		4.7			
$t_{SU:STO}$	Stop setup time		4			
$t_{HD:DAT}$	Data hold time	RECEIVE mode	0			
		TRANSMIT mode	300			ns
$t_{SU:DAT}$	Data setup time		250			
$t_{TIMEOUT}$	Error signal/detect	See note (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See note (2)	4		50	
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See note (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See note (4)			10	
t_F	Clock/data fall time	(V_{ILMAX} – 0.15 V) to (V_{IHMIN} + 0.15 V)			300	ns
t_R	Clock/data rise time	0.9 VCC to (V_{ILMAX} – 0.15 V)			1000	

(1) The bq78350 times out when any clock low exceeds $t_{TIMEOUT}$.
(2) $t_{HIGH:MAX}$ is minimum bus idle time. SMBC = 1 for t > 50 µs causes a reset of any transaction in progress involving the bq78350.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to stop.

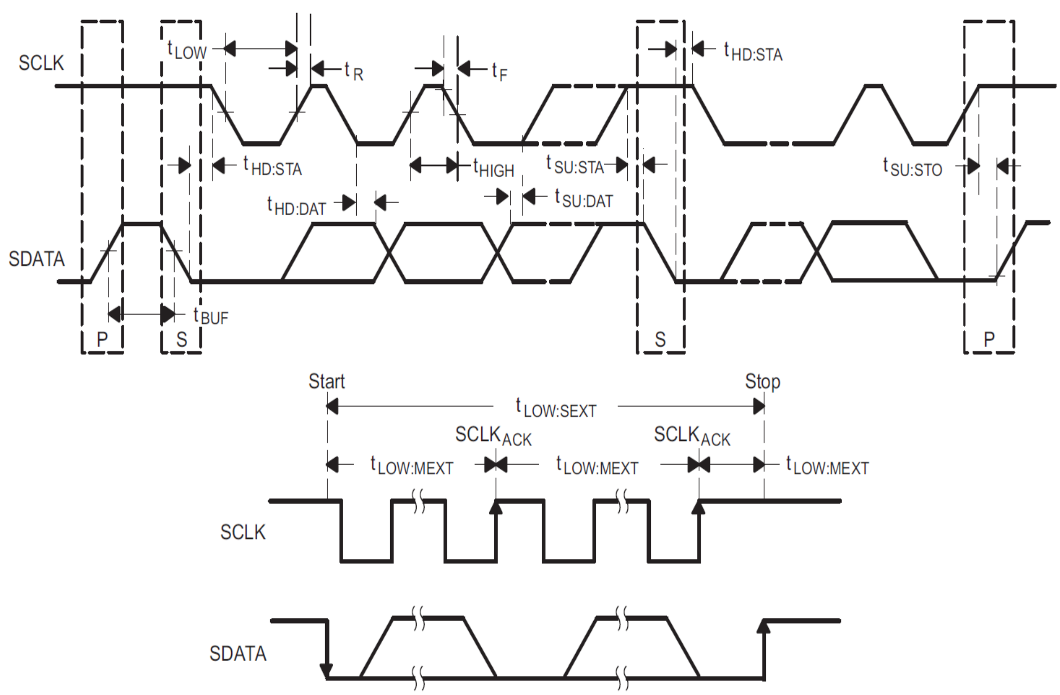


图 1. SMBus Timing Diagram

8.13 Typical Characteristics

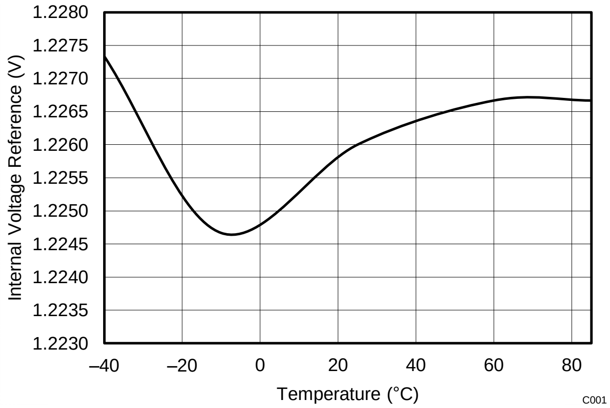


图 2. Internal Voltage Reference

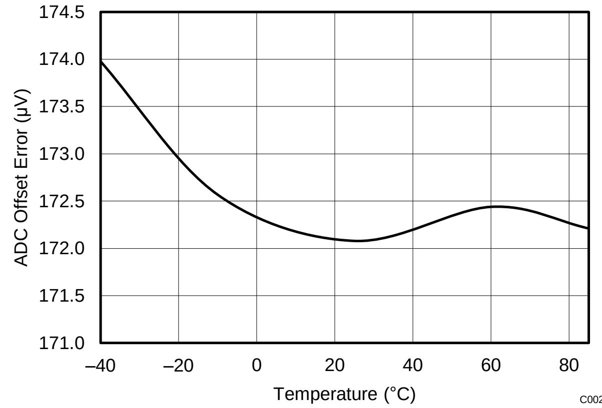


图 3. ADC Offset Error

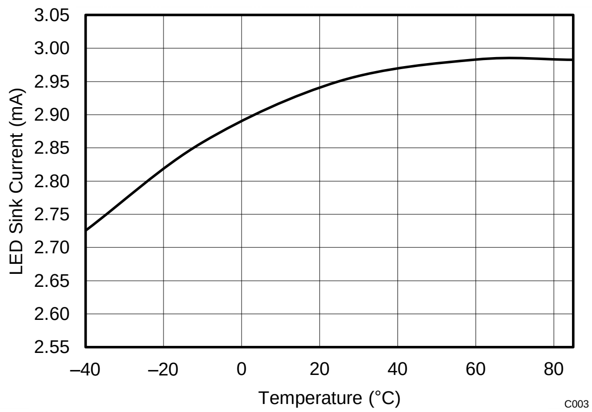


图 4. LED Sink Current

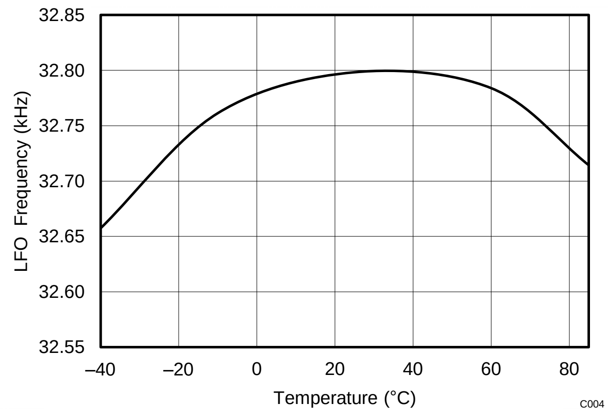


图 5. LFO Frequency

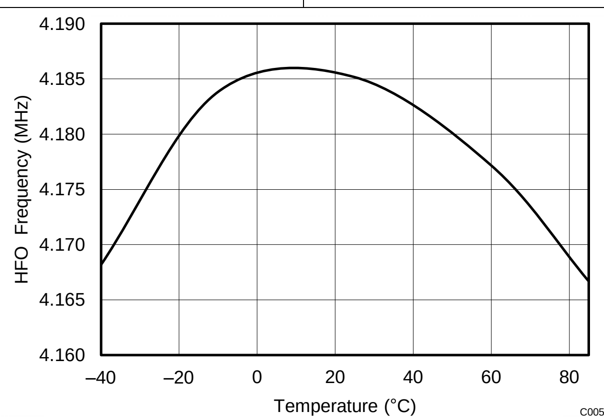


图 6. HFO Frequency

9 Detailed Description

9.1 Overview

The bq78350 Li-Ion and LiFePO4 Battery Management Controller is the companion to the bq769x0 family of Analog Front End (AFE) protection devices. This chipset supports from 3-series to 15-series cell applications with capacities up to 320 Ahr, and is suitable for a wide range of portable or stationary battery applications. The bq78350 provides an accurate fuel gauge and state-of-health (SoH) monitor, as well as the cell balancing algorithm and a full range of voltage-, current-, and temperature-based protection features.

The battery data that the bq78350 gathers can be accessed via an SMBus 1.1 interface and state-of-charge (SoC) data can be displayed through optional LED or LCD display configurations. Battery history and diagnostic data is also kept within the device in non-volatile memory and is available over the same SMBus interface.

9.2 Functional Block Diagram

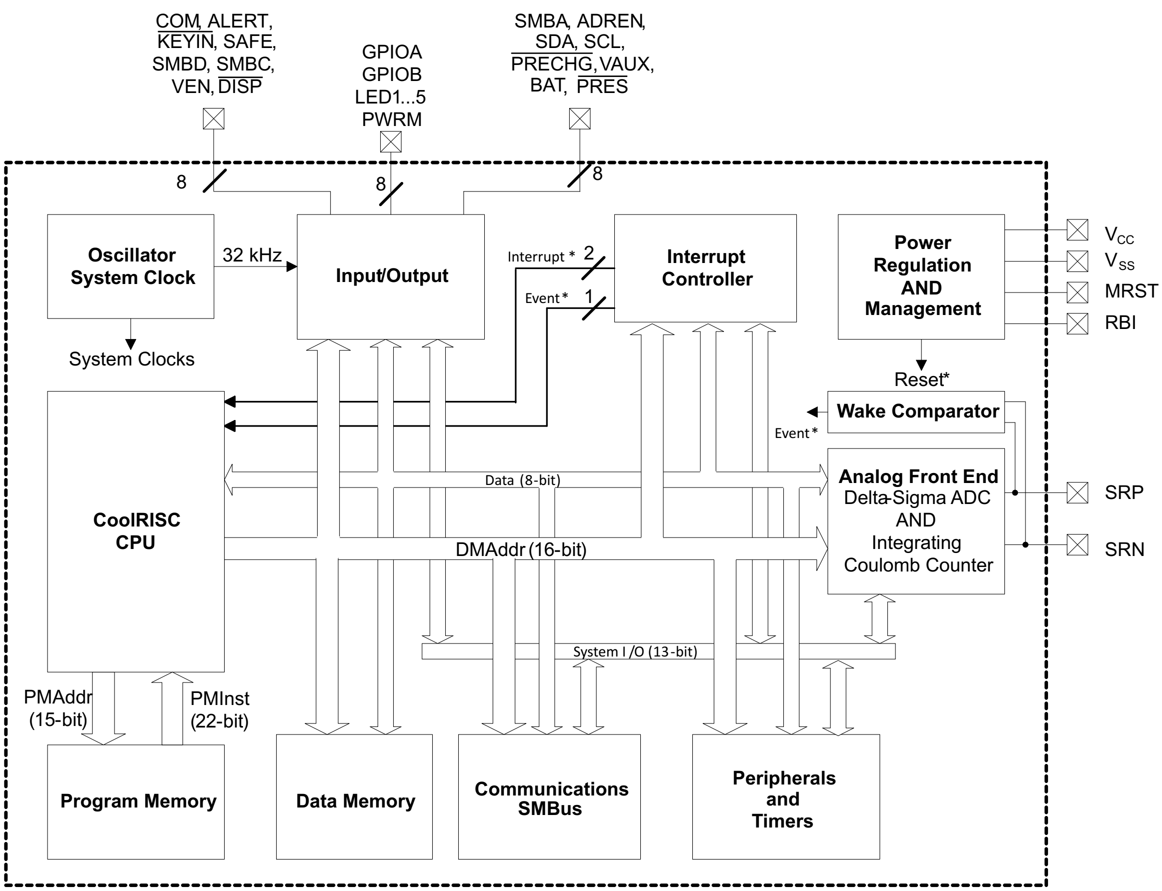


图 7. Functional Block Diagram

9.3 Feature Description

The following section provides an overview of the device features. For full details on the bq78350 features, refer to the *bq78350 Technical Reference Manual* (SLUUAN7).

9.3.1 Primary (1st Level) Safety Features

The bq78350 supports a wide range of battery and system protection features that can be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent

Feature Description (接下页)

- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor

9.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq78350 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge FET and Precharge FET fault
- Discharge FET fault
- Cell imbalance detection
- Open thermistor detection
- AFE communication fault

9.3.3 Charge Control Features

The bq78350 charge control features include:

- Provides a range of options to configure the charging algorithm and its actions based on the application requirements
- Reports the appropriate charging current needed for constant current charging, and the appropriate charging voltage needed for constant voltage charging
- Supports pre-charging/0-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range

9.3.4 Fuel Gauging

The bq78350 uses Compensated End-of-Discharge Voltage (CEDV) technology to measure and calculate the available charge in battery cells. The bq78350 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq78350 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature.

9.3.5 Lifetime Data Logging

The bq78350 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored includes:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage per cell
- Lifetime minimum battery cell voltage per cell
- Cycle count
- Maximum charge current
- Maximum discharge current
- Safety events that trigger *SafetyStatus()* updates. (The 12 most common are tracked.)

9.3.6 Authentication

The bq78350 supports authentication by the host using SHA-1.

Feature Description (接下页)

9.3.7 Battery Parameter Measurements

The bq78350 digitally reads bq769x0 registers containing recent values from the integrating analog-to-digital converter (CC) for current measurement and a second delta-sigma ADC for individual cell and temperature measurements.

9.3.7.1 Current and Coulomb Counting

The integrating delta-sigma ADC (CC) in the companion bq769x0 AFE measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The 15-bit integrating ADC measures bipolar signals from –0.20 V to 0.20 V with 15-µV resolution. The AFE reports charge activity when VSR = $V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when VSR = $V_{(SRP)} – V_{(SRN)}$ is negative. The bq78350 continuously monitors the measured current and integrates the digital signal from the AFE over time, using an internal counter.

To support large battery configurations, the current data can be scaled to ensure accurate reporting through the SMBus. The data reported is scaled based on the setting of the *SpecificationInfo()* command.

9.3.7.2 Voltage

The bq78350 updates the individual series cell voltages through the bq769x0 at 1-s intervals. The bq78350 configures the bq769x0 to connect to the selected cells in sequence and uses this information for cell balancing and individual cell fault functions. The internal 14-bit ADC of the bq769x0 measures each cell voltage value, which is then communicated digitally to the bq78350 where they are scaled and translated into unit mV. The maximum supported input range of the ADC is 6.075 V.

The bq78350 also separately measures the average cell voltage through an external translation circuit at the BAT pin. This value is specifically used for the fuel gauge algorithm. The external translation circuit is controlled via the VEN pin so that the translation circuit is only enabled when required to reduce overall power consumption. For correct operation, VEN requires an external pull-up to VCC, typically 100 k.

In addition to the voltage measurements used by the bq78350 algorithms, there is an optional auxiliary voltage measurement capability via the VAUX pin. This feature measures the input on a 1-s update rate and provides the programmable scaled value through an SMBus command.

To support large battery configurations, the voltage data can be scaled to ensure accurate reporting through the SMBus. The data reported is scaled based on the setting of the *SpecificationInfo()* command.

9.3.7.3 Temperature

The bq78350 receives temperature information from external or internal temperature sensors in the bq769x0 AFE. Depending on the number of series cells supported, the AFE will provide one, two, or three external thermistor measurements.

9.4 Device Functional Modes

The bq78350 supports three power modes to optimize the power consumption:

- In NORMAL mode, the bq78350 performs measurements, calculations, protection decisions, and data updates in 1-s intervals. Between these intervals, the bq78350 is in a reduced power mode.
- In SLEEP mode, the bq78350 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq78350 is in a reduced power mode.
- In SHUTDOWN mode, the bq78350 is completely powered down.

The bq78350 indicates through the PWRM pin which power mode it is in. This enables other circuits to change based on the power mode detection criteria of the bq78350.

9.5 Programming

9.5.1 Physical Interface

The bq78350 uses SMBus 1.1 with packet error checking (PEC) as an option and is used as a slave only.

9.5.2 SMBus Address

The bq78350 determines its SMBus 1.1 slave address through a voltage on SMBA, Pin 30. The voltage is set with a pair of high value resistors if an alternate address is required and is measured either upon exit of POR or when system present is detected. ADREN, Pin 29, may be used to disable the voltage divider after use to reduce power consumption.

9.5.3 SMBus On and Off State

The bq78350 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

10 Application and Implementation

10.1 Application Information

The bq78350 Battery Management Controller companion to the bq769x0 family of battery monitoring AFEs enables many standard and enhanced battery management features in a 3-series to 15-series Li-Ion/Li Polymer battery pack.

To design and implement a complete solution, users need the Battery Management Studio (bqSTUDIO) tool to configure a "golden image" set of parameters for a specific battery pack and application. The bqSTUDIO tool is a graphical user-interface tool installed on a PC during development. The firmware installed in the product has default values, which are summarized in the *bq78350 Technical Reference Manual* (SLUUAN7). With the bqSTUDIO tool, users can change these default values to cater to specific application requirements. Once the system parameters are known (for example, fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, among others), the data can be saved. This data is referred to as the "golden image.”

10.2 Typical Applications

The bq78350 can be used with the bq76920, bq76930, or bq76940 device, but as default it is setup for a 5-series cell, 4400-mA battery application using the bq76920 AFE.

Typical Applications (接下页)

10.2.1 Schematic

The schematic is split into two sections: the gas gauge section (图 8) and the AFE section (图 9).

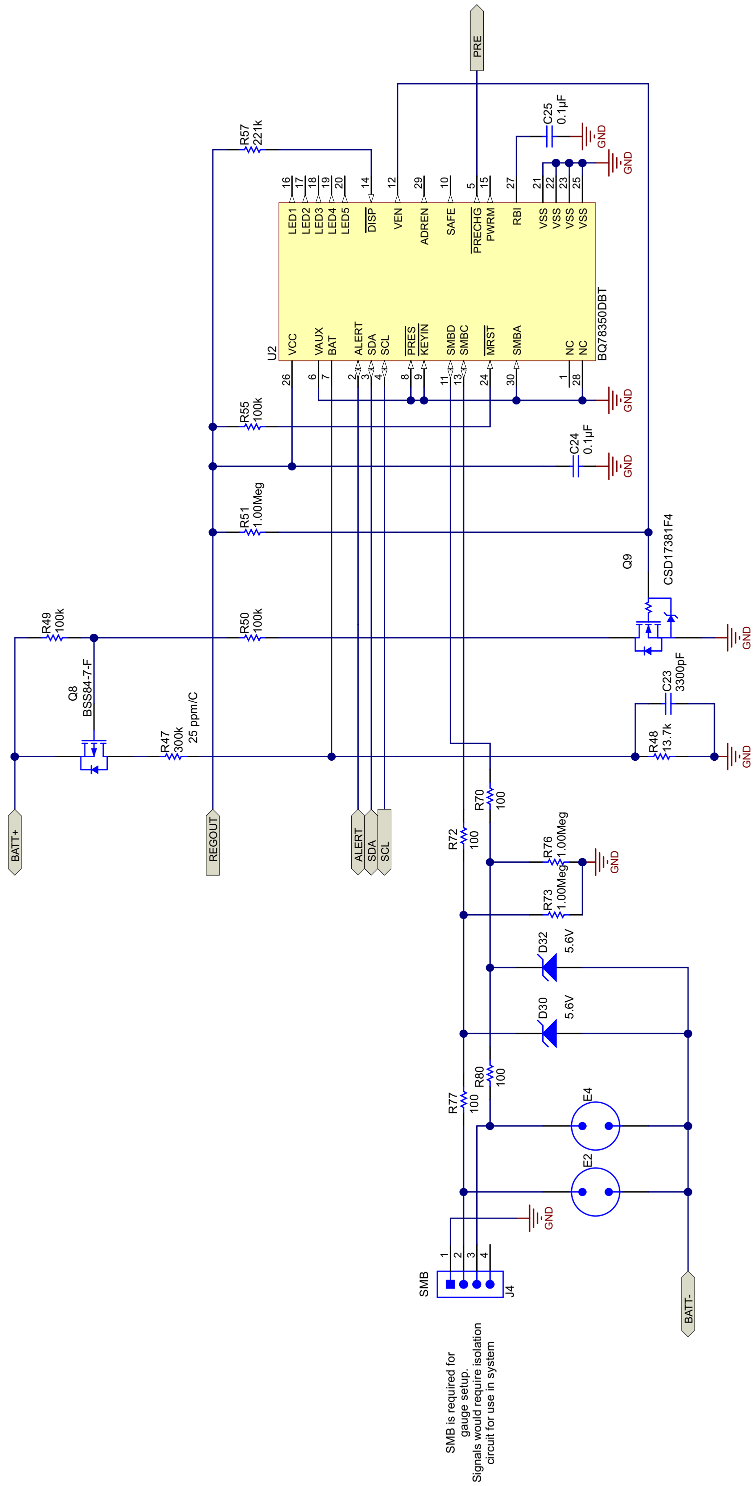


图 8. 5-Series Cell Typical Schematic, Gas Gauge (bq78350)

Typical Applications (接下页)

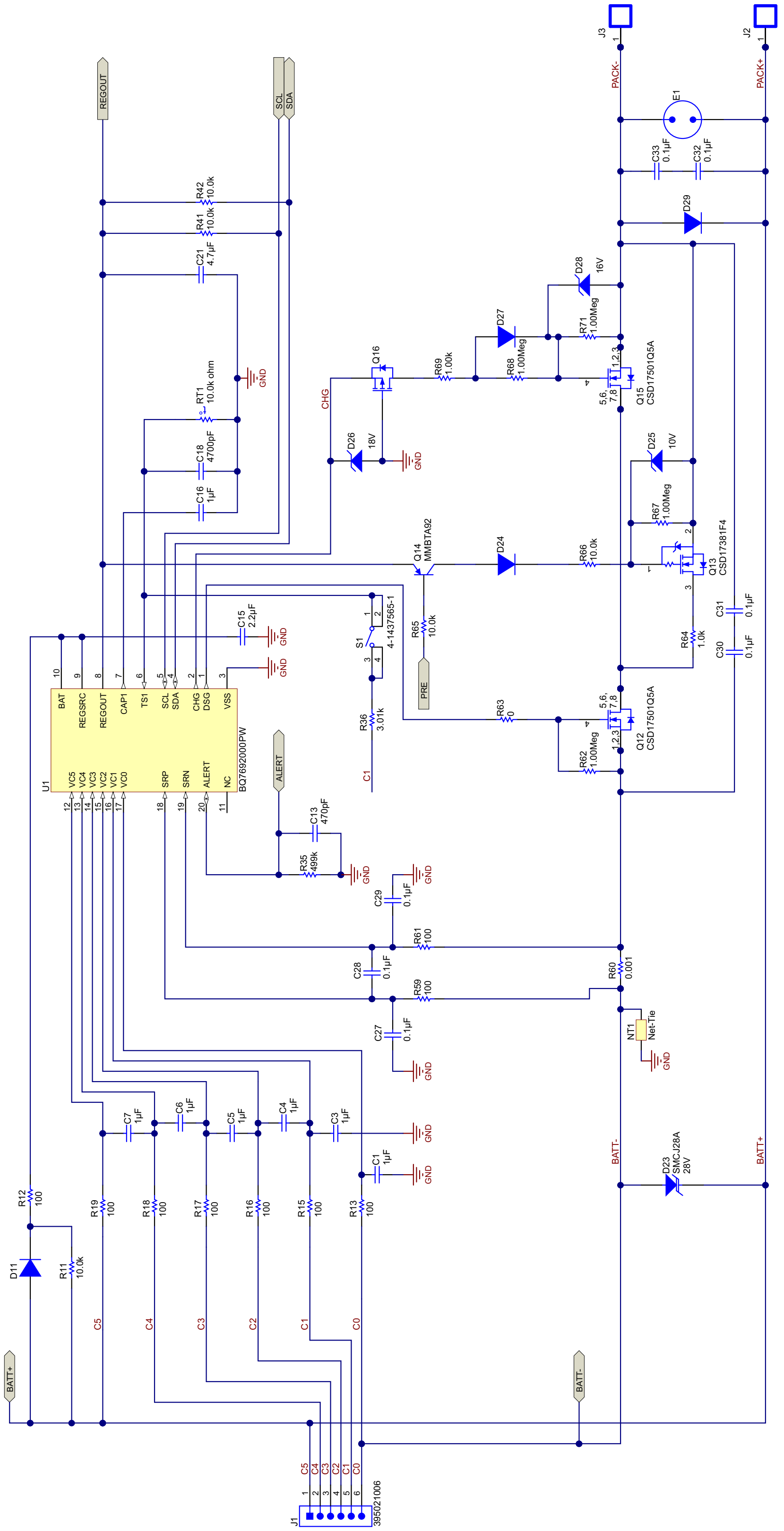


图 9. 5-Series Cell Typical Schematic, AFE (bq76920)

Typical Applications (接下页)

10.2.2 Design Requirements

表 1 lists the device's default settings and feature configurations when shipped from Texas Instruments.

表 1. TI Default Settings

Design Parameter	Value or State
Cell Configuration	5s2p (5-series with 1 Parallel)
Design Capacity	4400 mAh
Device Chemistry	Chem ID 1210 (LiCoO2/graphitized carbon)
Cell Overvoltage (per cell)	4250 mV
Cell Undervoltage (per cell)	2500 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Over Load Current	0.017 V/Rsense across SRP, SRN
Short Circuit in DISCHARGE Mode	0.44 V/Rsense across SRP, SRN
Over Temperature in CHARGE Mode	55°C
Over Temperature in DISCHARGE Mode	55°C
SAFE Pin Activation Enabled	No
Safety Over Voltage (per cell)	4400 mV
Safety Under Voltage (per cell)	2500 mV
Shutdown Voltage	2300 mV
Cell Balancing Enabled	Yes
Internal or External Temperature Sensor	External Enabled
SMB BROADCAST Mode	Disabled
Display Mode (# of Bars and LED or LCD)	5-bar LED
Dynamic SMB Address Enabled	No (SMB Address = 0x16)
KEYIN Feature Enabled	No
$\overline{\text{PRES}}$ Feature Enabled	No

10.2.3 Detailed Design Procedure

By default, the bq78350 is initially setup to keep the CHG, DSG, and PCHG FETs OFF and many other features disabled until the appropriate *ManufacturingStatus()* bit that enables *ManufacturerAccess()* commands are received, or when the default Manufacturing Status is changed.

In the first steps to evaluating the bq78350 and bq769x0 AFE, use the *ManufacturerAccess()* commands to ensure correct operation of features, and if they are needed in the application. Then enable features' reading for more in-depth application evaluation.

Prior to using the bq78350, the default settings should be evaluated as the device has many configuration settings and options. These can be separated into five main areas:

- Measurement System
- Gas Gauging
- Charging
- Protection
- Peripheral Features

The key areas of focus are covered in the following sections.

10.2.3.1 Measurement System

10.2.3.1.1 Cell Voltages

The bq78350 is required to be configured in the AFE Cell Map register to determine which cells to measure based on the physical connections to the bq76920 AFE. The cell voltage data is available through *CellVoltage1()*…*CellVoltage5()*. The cell voltages are reported as they are physically stacked. For example, if the device is configured for 3-series cells connected to VC1, VC2, and VC5 per the AFE Cell Map, then the cell voltages are still reported via *CellVoltage1()*, *CellVoltage2()*, and *CellVoltage3()*, respectively.

For improved accuracy, offset calibration is available for each of these values and can be managed through the bqSTUDIO tool. The procedure for calibration is described in the *bq78350 Technical Reference Manual* (SLUUAN7) in the "Calibration" chapter.

10.2.3.1.2 External Average Cell Voltage

This is enabled by default (***DA Configuration [ExtAveEN]*** = 1) and uses the external resistor divider connected to the VEN and BAT pins to determine the average cell voltage of the battery pack. The average cell voltage is available through *ExtAveCellVoltage()*.

CAUTION

Care should be taken in the selection of the resistor and FETs used in this divider circuit as the tolerance and temperature drift of these components can cause increased measurement error and a gas gauging error if ***CEDV Gauging Config [ExtAveCell]*** = 1 (default = 1).

For improved accuracy, offset and Gain calibration is available for this value and can be managed through the bqSTUDIO tool. The procedure for calibration is described in the *bq78350 Technical Reference Manual* (SLUUAN7) in the "Calibration" chapter.

10.2.3.1.3 Current

Current data is taken from the bq76920 and made available through *Current()*. The selection of the current sense resistor connected to SRP and SRN of the bq76920 is very important and there are several factors involved.

The aim of the sense resistor selection is to use the widest ADC input voltage range possible.

To maximize accuracy, the sense resistor value should be calculated based on the following formula:

$$RSNS_{(min)} = V_{(SRP)} – V_{(SRN)} / I_{(max)} \quad (1)$$

Where: $|V_{(SRP)} – V_{(SRN)}| = 200$ mV

$I_{(max)}$ = Maximum magnitude of charge of discharge current (transient or DC)

注

$RSNS_{(min)}$ should include tolerance, temperature drift over the application temperature, and PCB layout tolerances when selecting the actual nominal resistor value.

When selecting the RSNS value, be aware that when selecting a small value, for example, 1 mΩ, then the resolution of the current measurement will be > 1 mA. In the example of RSNS = 1 mΩ, the current LSB will be 8.44 mA.

For improved accuracy, offset and gain calibration are available for this value and can be managed through the bqSTUDIO tool. The procedure for calibration is described in the *bq78350 Technical Reference Manual* (SLUUAN7) in the "Calibration" chapter.

10.2.3.1.4 Temperature

By default, the 78350 uses an external negative temperature coefficient (NTC) thermistor connected to the bq76920 as the source for the *Temperature()* data. The measurement uses a polynomial expression to transform the bq76920 ADC measurement into 0.1°C resolution temperature measurement. The default polynomial coefficients are calculated using the Semitec 103AT, although other resistances and manufacturers can be used.

To calculate the ***External Temp Model*** coefficients, use the bq78350 Family Thermistor Coefficient Calculator shown in the application note, *Using the bq78350* (SLUA726).

For improved accuracy, offset calibration is available for this value and can be managed through the bqSTUDIO tool. The procedure for calibration is described in the *bq78350 Technical Reference Manual* (SLUUAN7) in the "Calibration" chapter.

10.2.3.2 Gas Gauging

The default battery chemistry (Chem ID) is 1210, which is a Li-CoO2 type chemistry. Other secondary Li-Ion based Chem IDs can be obtained from *MathCAD Chemistry Selection Tool* (SLUC138).

The default maximum capacity of the battery is 4400 mAh and this should be changed based on the cell and battery configuration chosen.

QMAX = Design Capacity of the Cell × # of parallel cells

Where: Design Capacity of the Cell can be taken from the manufacturer data sheet.

The CEDV gas gauging algorithm requires seven coefficients to enable accurate gas gauging. The default values are generic for Li-CoO2 chemistry, but for accurate gas gauging these coefficients should be re-calculated. The procedure to gather the required data and generate the coefficients can be found at http://www.ti.com/tool/GAUGEPARCAL.

10.2.3.3 Charging

The charging algorithm in the bq78350 is configured to support Constant Voltage/Constant Current (CC/CV) charging of a nominal 18-V, 4400-mAh battery.

10.2.3.3.1 Fast Charging Voltage

The charging voltage is configured (Fast Charging: Voltage) based on an individual cell basis (for example, 4200 mV), but the *ChargingVoltage()* is reported as the required battery voltage (for example, 4200 mV × 5 = 21000 mV).

10.2.3.3.2 Fast Charging Current

The fast charging current is configured to 2000 mA (Fast Charging: Current) by default, which is conservative for the majority of 4400-mAh battery applications. This should be configured based on the battery configuration, cell manufacturer's data sheet, and system power design requirements.

10.2.3.3.3 Other Charging Modes

The bq78350 is configured to limit, through external components, and report either low or 0 *ChargingVoltage()* and *ChargingCurrent()*, based on temperature, voltage, and fault status information.

The "Charge Algorithm" section of the *bq78350 Technical Reference Manual* (SLUUAN7) details these features and settings.

10.2.3.4 Protection

The safety features and settings of the bq78350 are configured conservatively and are suitable for bench evaluation. However, in many cases, users will need to change these values to meet system requirements. These values should not be changed to exceed the safe operating limits provided by the cell manufacturer and any industry standard.

For details on the safety features and settings, see the "Protections" and "Permanent Fail" sections of the bq78350 *Technical Reference Manual* (SLUUAN7).

10.2.3.5 Peripheral Features

10.2.3.5.1 LED Display

The bq78350 is configured by default to display up to five LEDs in a bar graph configuration based on the value of *RemainingStateOfCharge()* (RSOC). Each LED represents 20% of RSOC and is illuminated when the bq78350 $\overline{\text{DISP}}$ pin transitions low, and remains on for a programmable period of time.

In addition to many other options, the number of LEDs used and the percentage at which they can be illuminated are configurable.

10.2.3.5.2 SMBus Address

Although the SMBus slave address is a configurable value in the bq78350, this feature is disabled by default and the slave address is 0x16. The SMBus Address feature can allow up to nine different addresses based on external resistor value variation per address.

The default setup of the bq78350 is generic, but there are many additional features that can be enabled and configured to support a variety of system requirements. These are detailed in the *bq78350 Technical Reference Manual* (SLUUAN7).

10.2.4 Application Performance Plots

When the bq78350 is powered up, there are several signals that are enabled at the same time. 图 10 shows the rise time of each of the applicable signals.

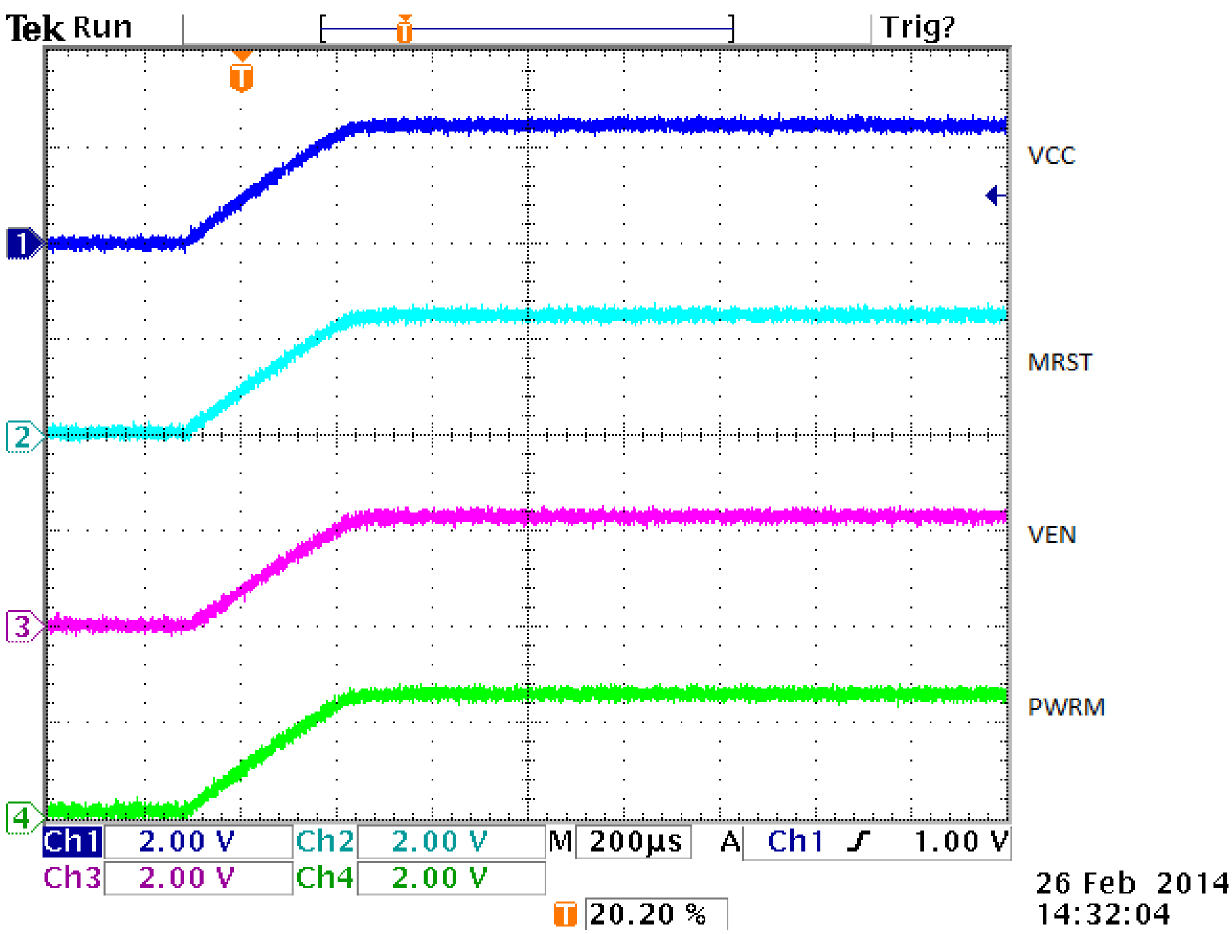


图 10. VCC, $\overline{\text{MRST}}$, VEN, and PWRM Upon Power Up

The bq78350 takes a short period of time to boot up before the device can begin updating battery parameter data that can be then reported via the SMBus or the optional display. Normal operation after boot-up is indicated by the VEN pin pulsing to enable voltage data measurements for the *ExtAveCell( )* function. 图 11 shows the timing of these signals.

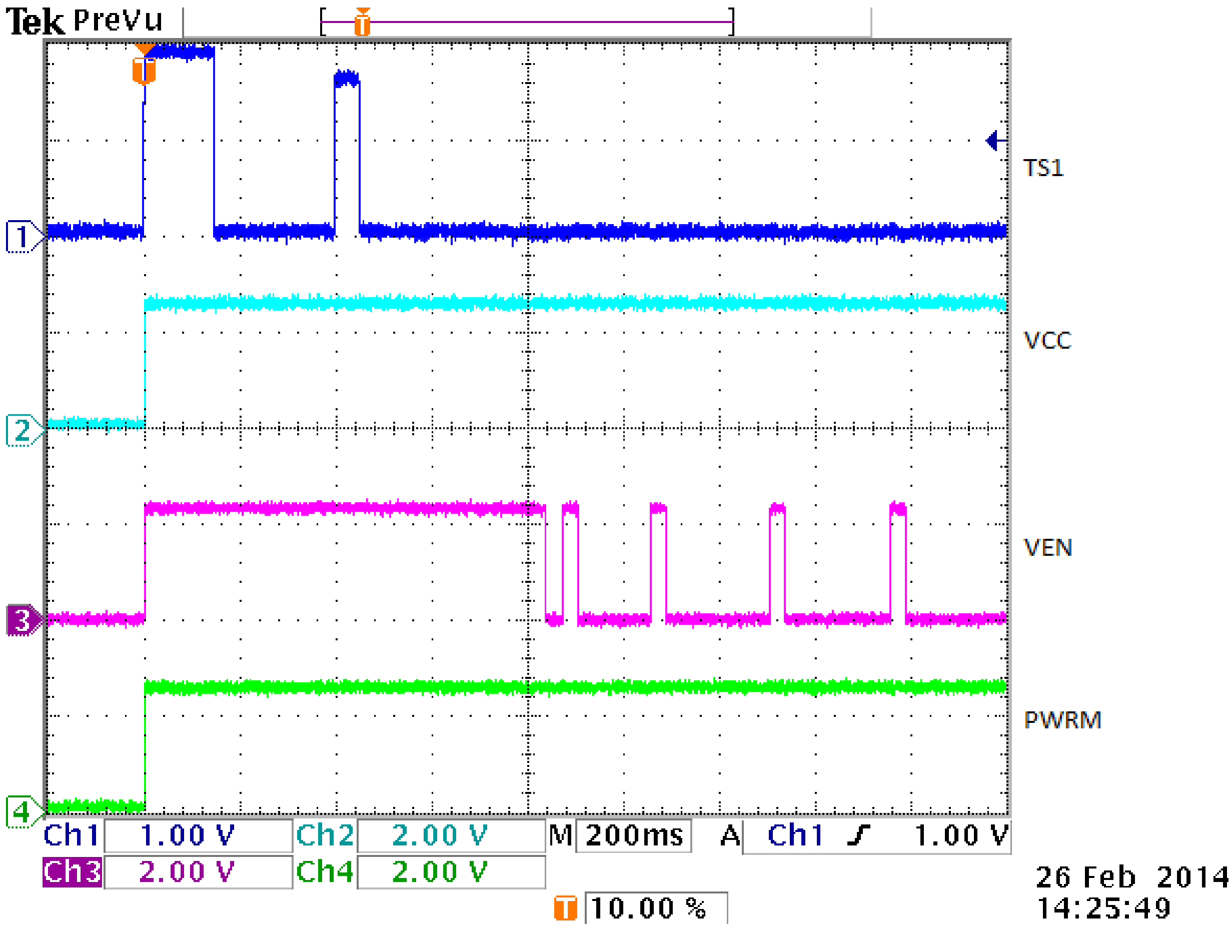


图 11. Valid VCC to Full FW Operation

图 12, 图 13, 图 14, and 图 15 show Measurement System Performance Data of the bq78350 + the bq76920 EVM. This data was taken using a standard bq76920 EVM with power supplies providing the voltage and current reference inputs.

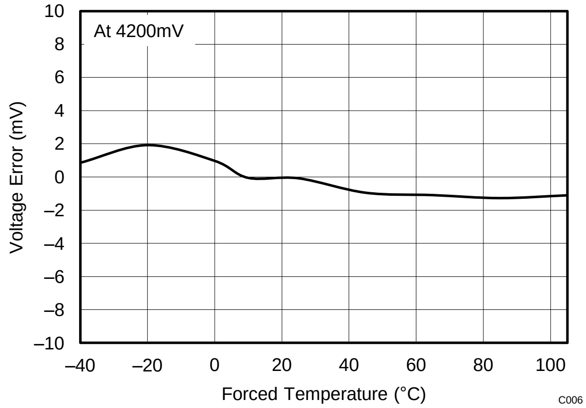


图 12. Cell Voltage Error Reported Through *CellVoltage1…5()*

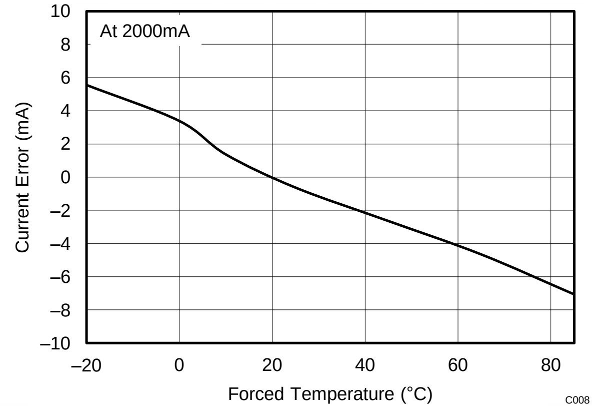


图 13. Battery Charge Current Error Reported Through *Current()*

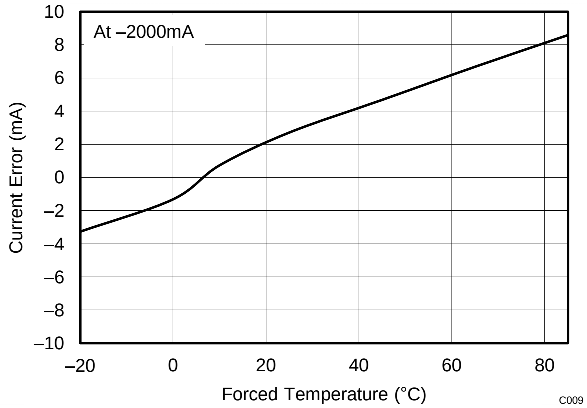


图 14. Battery Discharge Current Error Reported Through *Current()*

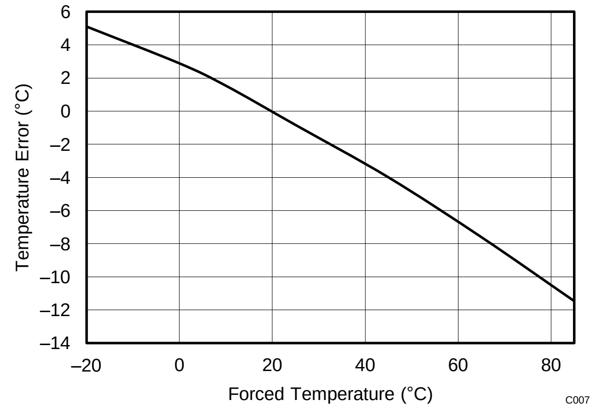


图 15. Battery Temperature (External) Error Reported Through *Temperature()*

11 Power Supply Recommendations

The bq78350 is powered directly from the 2.5-V REGOUT pin of the bq769x0 companion AFE. An input capacitor of 0.1 µF is required between VCC and VSS and should be placed as close to the bq78350 as possible.

To ensure correct power up of the bq78350, a 100-k resistor between $\overline{\text{MRST}}$ and VCC is also required. See the schematic for further details.

12 Layout

12.1 Layout Guidelines

12.1.1 Power Supply Decoupling Capacitor

Power supply decoupling from VCC to ground is important for optimal operation of the bq78350. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large-loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor must be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

Placement of the RBI capacitor is not as critical. It can be placed further away from the IC.

12.1.2 MRST Connection

The $\overline{\text{MRST}}$ pin controls the gas gauge reset state. The connections to this pin must be as short as possible in order to avoid any incoming noise. Direct connection to VCC is possible if the reset functionality is not desired or necessary.

If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-μF capacitor between MRST and ground.
- Provide a 1-kΩ pull up resistor to VCC at $\overline{\text{MRST}}$.
- Surround the entire circuit with a ground pattern.

If a test point is added at MRST, it must be provided with a 10-kΩ series resistor.

12.1.3 Communication Line Protection Components

The 5.6-V Zener diodes, which protect the bq78350 communication pins from ESD, must be located as close as possible to the pack connector. The grounded end of these Zener diodes must be returned to the PACK(–) node, rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

12.1.4 ESD Spark Gap

Protect the SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The following pattern is recommended, with 0.2-mm spacing between the points.

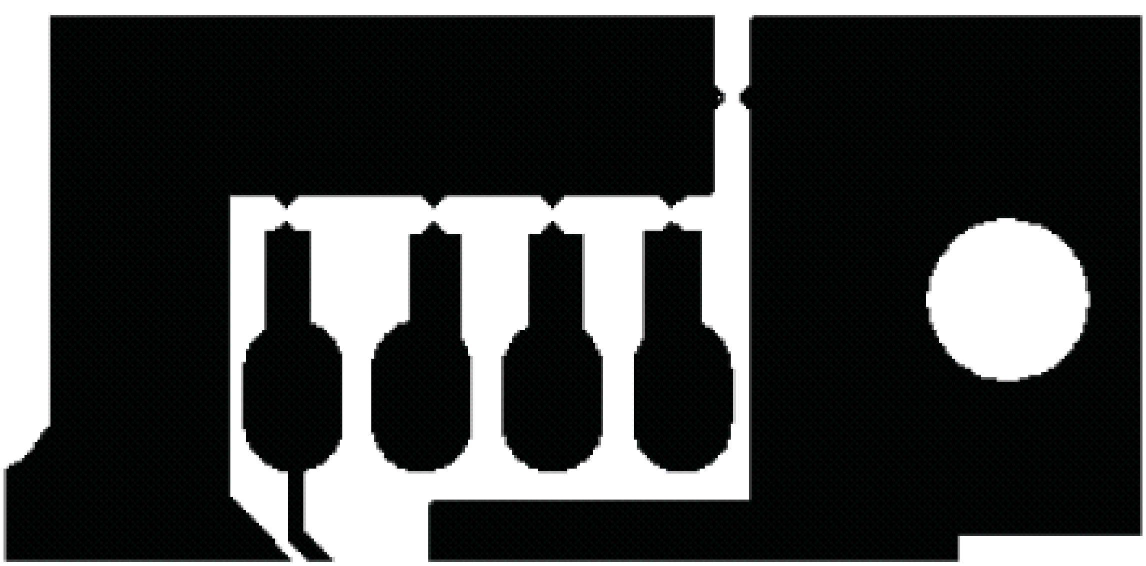


图 16. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD

12.2 Layout Example

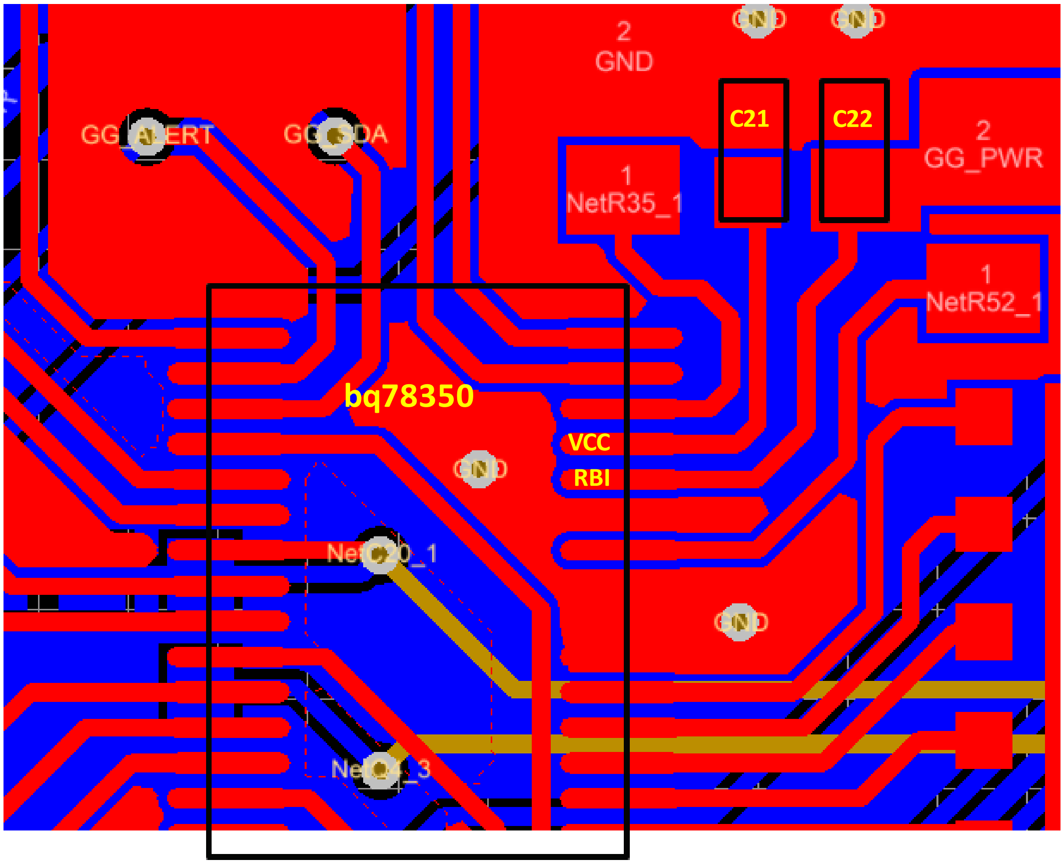


图 17. bq78350 Layout

13 器件和文档支持

13.1 相关文档

相关文档如下：

- *《bq78350 技术参考》手册* (SLUUAN7)
- *《使用 bq78350》应用手册* (SLUA726)
- *《bq769x0 用于锂离子和磷酸盐应用的 3 节到 15 节电池监控器系列》数据手册* (SLUSBK2)

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ78350DBT	NRND	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ78350	
BQ78350DBTR	NRND	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ78350	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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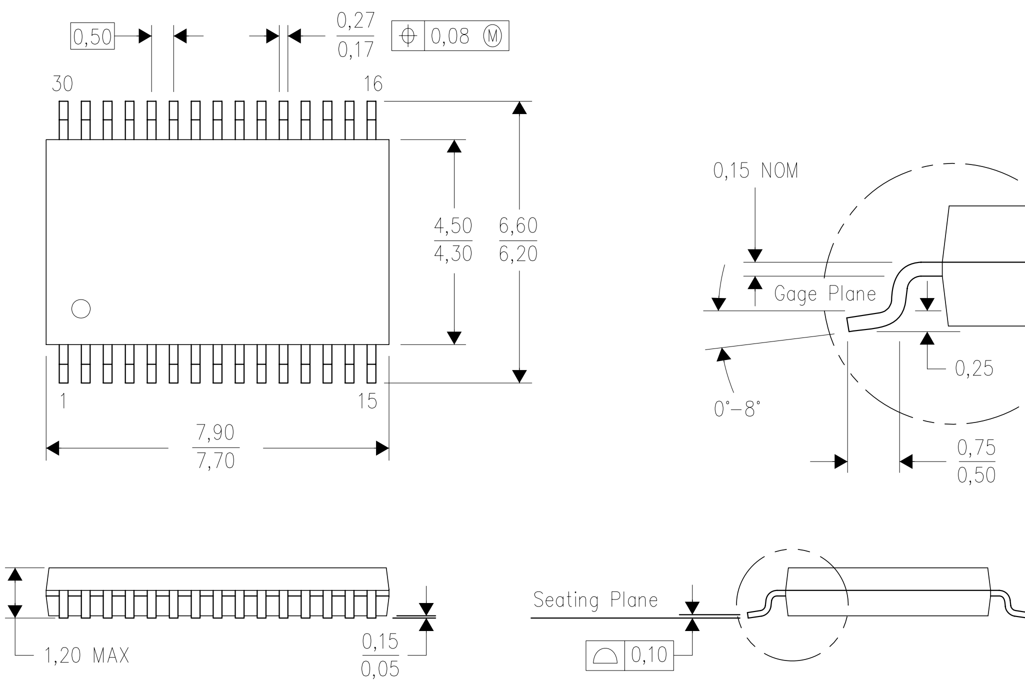
DBT (R-PDSO-G30) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

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