bq24725A 具有 N 通道功率 MOSFET 选择器和高级电路保护功能的 1-4 节锂离子电池 SMBus 充电控制器

1 特性

- SMBus 主机控制的 NMOS-NMOS 同步降压转换器，开关频率可编程为 615kHz、750kHz 和 885kHz
- N 通道 MOSFET 可自动选择适配器供电或内部电荷泵驱动式电池供电的系统电源
- 增强了过压保护、过流保护、电池、电感器和 MOSFET 短路保护等安全特性
- 可编程的输入电流、充电电压、充电电流限值
  - 高达 19.2V 的充电电压精度为 ±0.5%
  - 高达 8.128A 的充电电流精度为 ±3%
  - 高达 8.064A 的输入电流精度为 ±3%
  - 20x 适配器电流或充电电流放大器输出精度为 ±2%
- 可编程的电池损耗阈值，支持电池 LEARN（学习）功能
- 可编程的适配器检测和指示器
- 集成软启动
- 集成环路补偿
- 可对 ILIM 引脚进行实时系统控制以限制充电电流
- 交流适配器工作范围为 4.5V 至 24V
- 5µA 断开状态电池放电电流
- 0.65mA（最大 0.8mA）适配器待机静态电流
- 20 引脚 3.5mm x 3.5mm^2 超薄四方扁平无引线 (VQFN) 封装

2 应用

- 便携式笔记本电脑、超便携个人计算机 (UMPC)、超薄笔记本和上网本
- 手持式终端
- 工业用和医疗用设备
- 便携式设备

3 说明

bq24725A 是一款高效同步电池充电器，所含元件数较少，适用于空间受限的多化合物电池充电应用。

bq24725A 利用两个电荷泵分别驱动各 N 通道 MOSFET（ACFET、RBFET 和 BATFET），以便自动选择系统电源。

SMBus 控制的输入电流、充电电流和充电电压数模转换器 (DAC) 具有很高的调节精度，该精度可通过系统电源管理微控制器轻松编程。

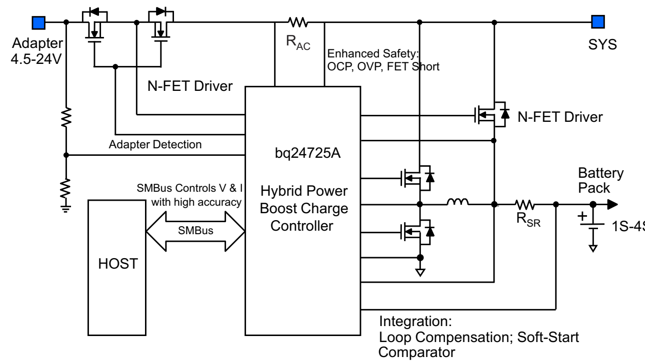
bq24725A 使用内部输入电流寄存器或外部 ILIM 引脚来调节 PWM 调制，以减小充电电流。

bq24725A 可对 1 节、2 节、3 节或 4 节锂电子电池充电。

器件信息(1)

部件号	封装	封装尺寸（标称值）
bq24725A	VQFN (20)	3.50mm x 3.50mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



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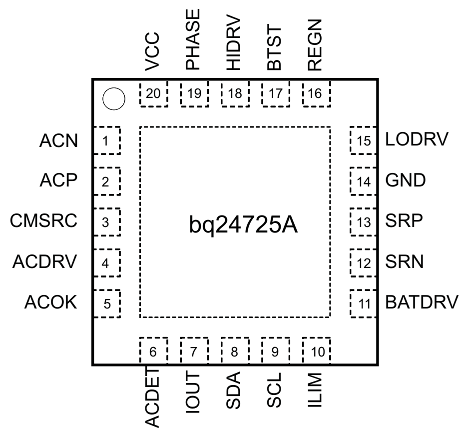
4 修订历史记录

Changes from Original (September 2011) to Revision A **Page**

- 更改了格式以满足新的 TI 标准 ... 1
- 已添加器件信息表 ... 1
- Added LODRV, HIDRV, and PHASE (2% duty cycle) to the Abs Max Table ... 4
- Added the Handling Ratings table ... 5

5 Pin Configuration and Functions

RGR Package
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	ACN	Input current sense resistor negative input. Place an optional 0.1µF ceramic capacitor from ACN to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential mode filtering.
2	ACP	Input current sense resistor positive input. Place a 0.1µF ceramic capacitor from ACP to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential-mode filtering.
3	CMSRC	ACDRV charge pump source input. Place a 4kΩ resistor from CMSRC to the common source of ACFET (Q1) and RBFET (Q2) limits the in-rush current on CMSRC pin.
4	ACDRV	Charge pump output to drive both adapter input n-channel MOSFET (ACFET) and reverse blocking n-channel MOSFET (RBFET). ACDRV voltage is 6V above CMSRC when voltage on ACDET pin is between 2.4V to 3.15V, voltage on VCC pin is above UVLO and voltage on VCC pin is 275mV above voltage on SRN pin so that ACFET and RBFET can be turned on to power the system by AC adapter. Place a 4kΩ resistor from ACDRV to the gate of ACFET and RBFET limits the in-rush current on ACDRV pin.
5	ACOK	AC adapter detection open drain output. It is pulled HIGH to external pull-up supply rail by external pull-up resistor when voltage on ACDET pin is between 2.4V and 3.15V, and voltage on VCC is above UVLO and voltage on VCC pin is 275mV above voltage on SRN pin, indicating a valid adapter is present to start charge. If any one of the above conditions can not meet, it is pulled LOW to GND by internal MOSFET. Connect a 10kΩ pull up resistor from ACOK to the pull-up supply rail.
6	ACDET	Adapter detection input. Program adapter valid input threshold by connecting a resistor divider from adapter input to ACDET pin to GND pin. When ACDET pin is above 0.6V and VCC is above UVLO, REGN LDO is present, ACOK comparator and IOUT are both active.
7	IOUT	Buffered adapter or charge current output, selectable with SMBus command ChargeOption(). IOUT voltage is 20 times the differential voltage across sense resistor. Place a 100pF or less ceramic decoupling capacitor from IOUT pin to GND.
8	SDA	SMBus open-drain data I/O. Connect to SMBus data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
9	SCL	SMBus open-drain clock input. Connect to SMBus clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
10	ILIM	Charge current limit input. Program ILIM voltage by connecting a resistor divider from system reference 3.3V rail to ILIM pin to GND pin. The lower of ILIM voltage or DAC limit voltage sets charge current regulation limit. To disable the control on ILIM, set ILIM above 1.6V. Once voltage on ILIM pin falls below 75mV, charge is disabled. Charge is enabled when ILIM pin rises above 105mV.
11	BATDRV	Charge pump output to drive Battery to System n-channel MOSFET (BATFET). BATDRV voltage is 6V above SRN to turn on BATFET to power the system from battery. BATDRV voltage is SRN voltage to turn off BATFET to power system from AC adapter. Place a 4kΩ resistor from BATDRV to the gate of BATFET limits the in-rush current on BATDRV pin.

Pin Functions (continued)

PIN NO.	PIN NAME	DESCRIPTION
12	SRN	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin to a 7.5 Ω resistor first then from resistor another terminal connect a 0.1µF ceramic capacitor to GND for common-mode filtering and connect to current sensing resistor. Connect a 0.1µF ceramic capacitor between current sensing resistor to provide differential mode filtering. See application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection by adding small resistor.
13	SRP	Charge current sense resistor positive input. Connect SRP pin to a 10 Ω resistor first then from resistor another terminal connect to current sensing resistor. Connect a 0.1µF ceramic capacitor between current sensing resistor to provide differential mode filtering. See application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection by adding small resistor.
14	GND	IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through the power pad underneath IC.
15	LODRV	Low side power MOSFET driver output. Connect to low side n-channel MOSFET gate.
16	REGN	Linear regulator output. REGN is the output of the 6V linear regulator supplied from VCC. The LDO is active when voltage on ACDET pin is above 0.6V and voltage on VCC is above UVLO. Connect a 1µF ceramic capacitor from REGN to GND.
17	BTST	High side power MOSFET driver power supply. Connect a 0.047µF capacitor from BTST to PHASE, and a bootstrap Schottky diode from REGN to BTST.
18	HIDRV	High side power MOSFET driver output. Connect to the high side n-channel MOSFET gate.
19	PHASE	High side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
20	VCC	Input supply, diode OR from adapter or battery voltage. Use 10Ω resistor and 1µF capacitor to ground as low pass filter to limit inrush current.
PowerPAD™		Exposed pad beneath the IC. Analog ground and power ground star-connected only at the PowerPAD plane. Always solder PowerPad to the board, and have vias on the PowerPAD plane connecting to analog ground and power ground planes. It also serves as a thermal pad to dissipate the heat.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE MIN	VALUE MAX	UNIT
Voltage range	SRN, SRP, ACN, ACP, CMSRC, VCC	–0.3	30	V
	PHASE	–2	30	
	ACDET, SDA, SCL, LODRV, REGN, IOUT, ILIM, ACOK	–0.3	7	
	BTST, HIDRV, ACDRV, BATDRV	–0.3	36	
	LODRV (2% duty cycle)	–4	7	
	HIDVR (2% duty cycle)	–4	36	
	PHASE (2% duty cycle)	–4	30	
Maximum difference voltage	SRP–SRN, ACP–ACN	–0.5	0.5	
Junction temperature range, T_J		–40	155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	155	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	SRN, SRP, ACN, ACP, CMSRC, VCC	0		24	V
	PHASE	-2		24	
	ACDET, SDA, SCL, LODRV, REGN, IOUT, ILIM, ACOK	0		6.5	
	BTST, HIDRV, ACDRV, BATDRV	0		30	
Maximum difference voltage	SRP–SRN, ACP–ACN	–0.2		0.2	V
Junction temperature range, T_J		0		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq24725A RGR (20 PIN)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	56.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	46.6	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	15.3	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistanc	4.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

4.5 V ≤ V_{VCC} ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC Input voltage operating range		4.5		24	V
CHARGE VOLTAGE REGULATION						
$V_{BAT\_REG\_RNG}$	Battery voltage range		1.024		19.2	V
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	ChargeVoltage() = 0x41A0H	16.716	16.8	16.884	V
			-0.5%		0.5%	
		ChargeVoltage() = 0x3130H	12.529	12.592	12.655	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x20D0H	8.350	8.4	8.45	V
			–0.6%		0.6%	
		ChargeVoltage() = 0x1060H	4.163	4.192	4.221	V
			–0.7%		0.7%	
CHARGE CURRENT REGULATION						
$V_{IREG\_CHG\_RNG}$	Charge current regulation differential voltage range	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$	0		81.28	mV
$I_{CHRG\_REG\_ACC}$	Charge current regulation accuracy 10mΩ current sensing resistor	ChargeCurrent() = 0x1000H	3973	4096	4219	mA
			–3%		3%	
		ChargeCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		ChargeCurrent() = 0x0200H	410	512	614	mA
			–20%		20%	
		ChargeCurrent() = 0x0100H	172	256	340	mA
			–33%		33%	
		ChargeCurrent() = 0x0080H	64	128	192	mA
			–50%		50%	
INPUT CURRENT REGULATION						
$V_{IREG\_DPM\_RNG}$	Input current regulation differential voltage range	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$	0		80.64	mV
$I_{DPM\_REG\_ACC}$	Input current regulation accuracy 10mΩ current sensing resistor	InputCurrent() = 0x1000H	3973	4096	4219	mA
			–3%		3%	
		InputCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		InputCurrent() = 0x0400H	870	1024	1178	mA
			–15%		15%	
		InputCurrent() = 0x0200H	384	512	640	mA
			–25%		25%	
INPUT CURRENT OR CHARGE CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	4.5		24	V
V_{SRP/N_OP}	Output common mode range	Voltage on SRP/SRN	0		19.2	V
V_{IOUT}	IOUT output voltage range		0		3.3	V
I_{IOUT}	IOUT output current		0		1	mA
A_{IOUT}	Current sense amplifier gain	$V_{(ICOUT)}/V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$		20		V/V
V_{IOUT_ACC}	Current sense output accuracy	$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 40.96mV	–2%		2%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 20.48mV	–4%		4%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 10.24mV	–15%		15%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 5.12mV	–20%		20%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 2.56mV	–33%		33%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 1.28mV	–50%		50%	
C_{IOUT_MAX}	Maximum output load capacitance	For stability with 0 to 1mA load			100	pF
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 6.5V, V_{ACDET} > 0.6V (0-45mA load)	5.5	6	6.5	V

Electrical Characteristics (接下页)

4.5 V ≤ V_{VCC} ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0V, V_{VCC} > UVLO charge enabled and not in TSHUT	50	75		mA
		V_{REGN} = 0V, V_{VCC} > UVLO charge disabled or in TSHUT	7	14		mA
C_{REGN}	REGN output capacitor required for stability	I_{LOAD} = 100µA to 50mA		1		µF
INPUT UNDERVOLTAGE LOCKOUT COMPARATOR (UVLO)						
UVLO	Under voltage rising threshold	V_{VCC} rising	3.5	3.75	4	V
	Under voltage hysteresis, falling	V_{VCC} falling		340		mV
FAST DPM COMPARATOR (FAST_DPM)						
V_{FAST_DPM}	Fast DPM comparator stop charging rising threshold with respect to input current limit, voltage across input sense resistor rising edge		103%	107%	111%	
QUIESCENT CURRENT						
$I_{BAT\_BATFET\_OFF}$	Battery BATFET OFF STATE Current, BATFET off, I_{SRP} + I_{SRN} + I_{PHASE} + I_{ACP} + I_{ACN}	V_{VBAT} = 16.8V, VCC disconnect from battery, BATFET charge pump off, BATFET turns off, T_J = 0 to 85°C			5	µA
$I_{BAT\_BATFET\_ON}$	Battery BATFET ON STATE Current, BATFET on, I_{SRP} + I_{SRN} + I_{PHASE} + I_{VCC} + I_{ACP} + I_{ACN}	V_{VBAT} = 16.8V, VCC connect from battery, BATFET charge pump on, BATFET turns on, T_J = 0 to 85°C			25	µA
$I_{STANDBY}$	Standby quiescent current, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > UVLO, V_{ACDET} > 0.6V, charge disabled, T_J = 0 to 85°C		0.65	0.8	mA
I_{AC_NOSW}	Adapter bias current during charge, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > UVLO, 2.4V < V_{ACDET} < 3.15V, charge enabled, no switching, T_J = 0 to 85°C		1.5	3	mA
I_{AC_SW}	Adapter bias current during charge, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > UVLO, 2.4V < V_{ACDET} < 3.15V, charge enabled, switching, MOSFET Sis412DN		10		mA
ACOK COMPARATOR						
V_{ACOK_RISE}	ACOK rising threshold	V_{VCC} > UVLO, V_{ACDET} rising	2.376	2.4	2.424	V
$V_{ACOK\_FALL\_HYS}$	ACOK falling hysteresis	V_{VCC}> UVLO, V_{ACDET} falling	35	55	75	mV
$V_{ACOK\_RISE\_DEG}$	ACOK rising deglitch (Specified by design)	V_{VCC}> UVLO, V_{ACDET} rising above 2.4V, First time OR ChargeOption() bit [15] = 0	100	150	200	ms
		V_{VCC}> UVLO, V_{ACDET} rising above 2.4V, (NOT First time) AND ChargeOption() bit [15] = 1 (Default)	0.9	1.3	1.7	s
V_{WAKEUP_RISE}	WAKEUP detect rising threshold	V_{VCC}> UVLO, V_{ACDET} rising		0.57	0.8	V
V_{WAKEUP_FALL}	WAKEUP detect falling threshold	V_{VCC}> UVLO, V_{ACDET} falling	0.3	0.51		V
VCC to SRN COMPARATOR (VCC_SRN)						
$V_{VCC\text{-}SRN\_FALL}$	VCC-SRN falling threshold	V_{VCC} falling towards V_{SRN}	70	125	200	mV
$V_{VCC\text{-}SRN\ \_RHYS}$	VCC-SRN rising hysteresis	V_{VCC} rising above V_{SRN}	100	150	200	mV
ACN to SRN COMPARATOR (ACN_SRN)						
$V_{ACN\text{-}SRN\_FALL}$	ACN to BAT falling threshold	V_{ACN} falling towards V_{SRN}	120	200	280	mV
$V_{ACN\text{-}SRN\_RHYS}$	ACN to BAT rising hysteresis	V_{ACN} rising above V_{SRN}	40	80	120	mV
HIGH SIDE IFAULT COMPARATOR (IFAULT_HI) (1)						
$V_{IFAULT\_HI\_RISE}$	ACP to PHASE rising threshold	ChargeOption() bit [8] = 1 (Default)	450	750	1200	mV
		ChargeOption() bit [8] = 0 Disable function				
LOW SIDE IFAULT COMPARATOR (IFAULT_LOW) (1)						
$V_{IFAULT\_LOW\_RISE}$	PHASE to GND rising threshold	ChargeOption() bit [7] = 0 (Default)	70	135	220	mV
		ChargeOption() bit [7] = 1	140	230	340	
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	ACDET over voltage rising threshold	V_{ACDET} rising	3.05	3.15	3.25	V
V_{ACOV_HYS}	ACDET over voltage falling hysteresis	V_{ACDET} falling	50	75	100	mV
INPUT OVER-CURRENT COMPARATOR (ACOC) (1)						
V_{ACOC}	Adapter over current rising threshold with respect to input current limit, voltage across input sense resistor rising edge	ChargeOption() bit [1] = 1 (Default)	300%	333%	366%	
		ChargeOption() bit [1] = 0 Disable function				

(1) User can adjust threshold via SMBus ChargeOption() REG0x12.

Electrical Characteristics (接下页)

4.5 V ≤ V_{VCC} ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACOC_min}	Min ACOC threshold clamp voltage	ChargeOption() Bit [1] = 1 (333%), InputCurrent () = 0x0400H (10.24mV)	40	45	50	mV
V_{ACOC_max}	Max ACOC threshold clamp voltage	ChargeOption() Bit [1] = 1 (333%), InputCurrent () = 0x1F80H (80.64mV)	135	150	165	mV
t_{ACOC_DEG}	ACOC deglitch time (Specified by design)	Voltage across input sense resistor rising to disable charge	2.3	4.2	6.6	ms
BAT OVER-VOLTAGE COMPARATOR (BAT_OVP)						
V_{OVP_RISE}	Over voltage rising threshold as percentage of V_{BAT_REG}	V_{SRN} rising	103%	104%	106%	
V_{OVP_FALL}	Over voltage falling threshold as percentage of V_{BAT_REG}	V_{SRN} falling		102%		
CHARGE OVER-CURRENT COMPARATOR (CHG_OCP)						
V_{OCP_RISE}	Charge over current rising threshold, measure voltage drop across current sensing resistor	ChargeCurrent()=0x0xxxH	54	60	66	mV
		ChargeCurrent()=0x1000H – 0x17C0H	80	90	100	mV
		ChargeCurrent()=0x1800 H– 0x1FC0H	110	120	130	mV
CHARGE UNDER-CURRENT COMPARATOR (CHG_UCP)						
V_{UCP_FALL}	Charge under-current falling threshold	V_{SRP} falling towards V_{SRN}	1	5	9	mV
LIGHT LOAD COMPARATOR (LIGHT_LOAD)						
V_{LL_FALL}	Light load falling threshold	Measure the voltage drop across current sensing resistor		1.25		mV
$V_{LL\_RISE\_HYST}$	Light load rising hysteresis			1.25		mV
BATTERY DEPLETION COMPARATOR (BAT_DEPL) [1]						
$V_{BATDEPL\_FALL}$	Battery depletion falling threshold, percentage of voltage regulation limit, V_{SRN} falling	ChargeOption() bit [12:11] = 00	55.53%	59.19%	63.5%	
		ChargeOption() bit [12:11] = 01	58.68%	62.65%	67.5%	
		ChargeOption() bit [12:11] = 10	62.17%	66.55%	71.5%	
		ChargeOption() bit [12:11] = 11 (Default)	66.06%	70.97%	77%	
$V_{BATDEPL\_RHYST}$	Battery depletion rising hysteresis, V_{SRN} rising	ChargeOption() bit [12:11] = 00	225	305	400	mV
		ChargeOption() bit [12:11] = 01	240	325	430	mV
		ChargeOption() bit [12:11] = 10	255	345	450	mV
		ChargeOption() bit [12:11] = 11 (Default)	280	370	490	mV
$t_{BATDEPL\_RDEG}$	Battery Depletion Rising Deglitch (Specified by design)	Delay to turn off ACFET and turn on BATFET during LEARN cycle		600		ms
BATTERY LOWV COMPARATOR (BAT_LOWV)						
V_{BATLV_FALL}	Battery LOWV falling threshold	V_{SRN} falling	2.4	2.5	2.6	V
V_{BATLV_RHYST}	Battery LOWV rising hysteresis	V_{SRN} rising		200		mV
I_{BATLV}	Battery LOWV charge current limit	10 mΩ current sensing resistor		0.5		A
THERMAL SHUTDOWN COMPARATOR (TSHUT)						
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling	Temperature falling		20		°C
ILIM COMPARATOR						
V_{ILIM_FALL}	ILIM as CE falling threshold	V_{ILIM} falling	60	75	90	mV
V_{ILIM_RISE}	ILIM as CE rising threshold	V_{ILIM} rising	90	105	120	mV
LOGIC INPUT (SDA, SCL)						
V_{IN_LO}	Input low threshold				0.8	V
V_{IN_HI}	Input high threshold		2.1			V
I_{IN_LEAK}	Input bias current	V = 7 V	–1		1	μA
LOGIC OUTPUT OPEN DRAIN (ACOK, SDA)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			500	mV
I_{OUT_LEAK}	Leakage current	V = 7 V	–1		1	μA
ANALOG INPUT (ACDET, ILIM)						
I_{IN_LEAK}	Input bias current	V = 7 V	–1		1	μA
PWM OSCILLATOR						
F_{SW}	PWM switching frequency	ChargeOption () bit [9] = 0 (Default)	600	750	900	kHz

Electrical Characteristics (接下页)

4.5 V ≤ V_{VCC} ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW+}	PWM increase frequency	ChargeOption() bit [10:9] = 11	665	885	1100	kHz
F_{SW-}	PWM decrease frequency	ChargeOption() bit [10:9] = 01	465	615	765	kHz
BATFET GATE DRIVER (BATDRV)						
I_{BATFET}	BATDRV charge pump current limit		40	60		µA
V_{BATFET}	Gate drive voltage on BATFET	V_{BATDRV} - V_{SRN} when V_{SRN} > UVLO	5.5	6.1	6.5	V
R_{BATDRV_LOAD}	Minimum load resistance between BATDRV and SRN		500			kΩ
R_{BATDRV_OFF}	BATDRV turn-off resistance	I = 30 µA	5	6.2	7.4	kΩ
ACFET GATE DRIVER (ACDRV)						
I_{ACFET}	ACDRV charge pump current limit		40	60		µA
V_{ACFET}	Gate drive voltage on ACFET	V_{ACDRV}–V_{CMSRC} when V_{VCC}> UVLO	5.5	6.1	6.5	V
R_{ACDRV_LOAD}	Minimum load resistance between ACDRV and CMSRC		500			kΩ
R_{ACDRV_OFF}	ACDRV turn-off resistance	I = 30 µA	5	6.2	7.4	kΩ
V_{ACFET_LOW}	ACDRV Turn-Off when Vgs voltage is low (Specified by design)			5.9		V
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High side driver turn-on resistance	V_{BTST} – V_{PH} = 5.5 V, I = 10 mA		6	10	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance	V_{BTST} – V_{PH} = 5.5 V, I = 10 mA		0.65	1.3	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{PH} when low side refresh pulse is requested	3.85	4.3	4.7	V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low side driver turn-on resistance	V_{REGN} = 6 V, I = 10 mA		7.5	12	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance	V_{REGN} = 6 V, I = 10 mA		0.9	1.4	Ω
PWM DRIVER TIMING						
t_{LOW_HIGH}	Driver dead time from low side to high side			20		ns
t_{HIGH_LOW}	Driver dead time from high side to low side			20		ns
INTERNAL SOFT START						
I_{STEP}	Soft start current step	In CCM mode 10mΩ current sensing resistor		64		mA
t_{STEP}	Soft start current step time			240		µs
SMBus TIMING CHARACTERISTICS						
t_R	SCLK/SDATA rise time				1	µs
t_F	SCLK/SDATA fall time				300	ns
$t_{W(H)}$	SCLK pulse width high		4		50	µs
$t_{W(L)}$	SCLK Pulse Width Low		4.7			µs
$t_{SU(STA)}$	Setup time for START condition		4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated		4			µs
$t_{SU(DAT)}$	Data setup time		250			ns
$t_{H(DAT)}$	Data hold time		300			ns
$t_{SU(STOP)}$	Setup time for STOP condition		4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition		4.7			µs
$F_{S(CL)}$	Clock Frequency		10		100	kHz
HOST COMMUNICATION FAILURE						
$t_{timeout}$	SMBus bus release timeout(2)		25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal		10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01(3)		35	44	53	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 10(3)		70	88	105	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 11(3) (Default)		140	175	210	s

(2) Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(3) User can adjust threshold via SMBus ChargeOption() REG0x12.

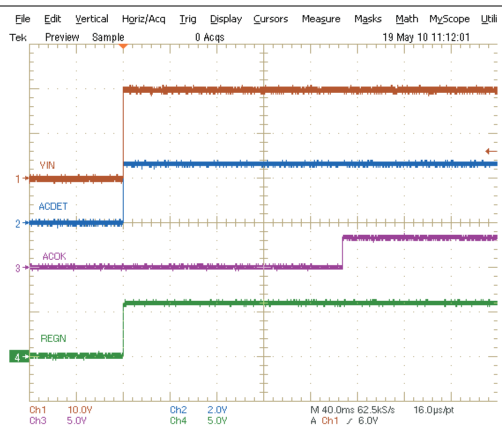
6.6 Timing Characteristics

4.5 V ≤ V_{VCC} ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS					
t_R	SCLK/SDATA rise time			1	μs
t_F	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	4		50	μs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			μs
$t_{SU(STA)}$	Setup time for START condition	4.7			μs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			μs
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			μs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			μs
$F_{S(CL)}$	Clock Frequency	10		100	kHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout(1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01(2)	35	44	53	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 10(2)	70	88	105	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 11(2) (Default)	140	175	210	s

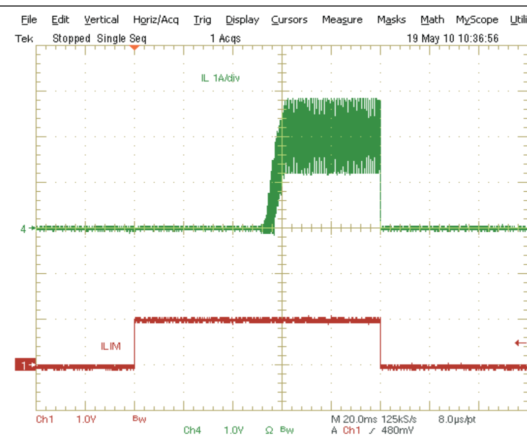
(1) Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(2) User can adjust threshold via SMBus ChargeOption() REG0x12.

6.7 Typical Characteristics



,
CH1: VCC, 10V/div, CH2: ACDET 2V/div, CH3: ACOK, 5V/div
CH4: REGN, 5V/div, 40ms/div

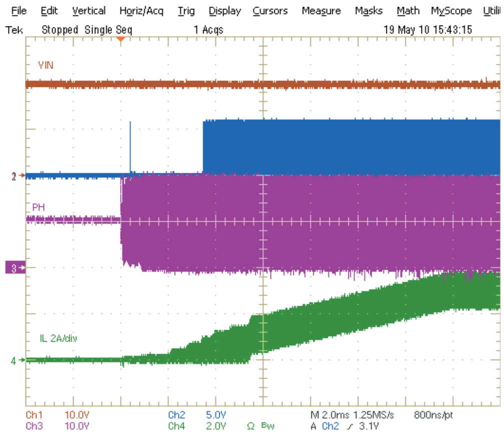
图 1. VCC, ACDET, REGN and ACOK Power Up



CH1: ILIM, 1V/div
CH4: inductor current 1A/div, 20ms/div

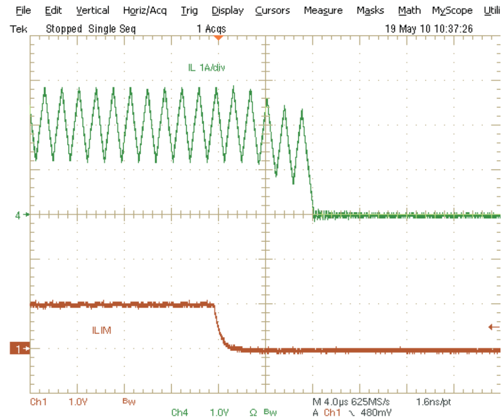
图 2. Charge Enable by ILIM

Typical Characteristics (接下页)



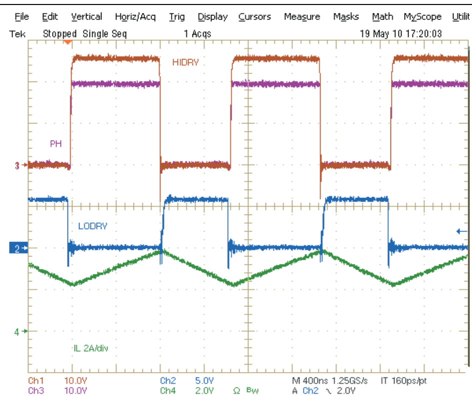
CH1: Vin, 10V/div , CH2: LODRV, 5V/div, CH3: PHASE, 10V/div
CH4: inductor current, 2A/div, 2ms/div

图 3. Current Soft-Start



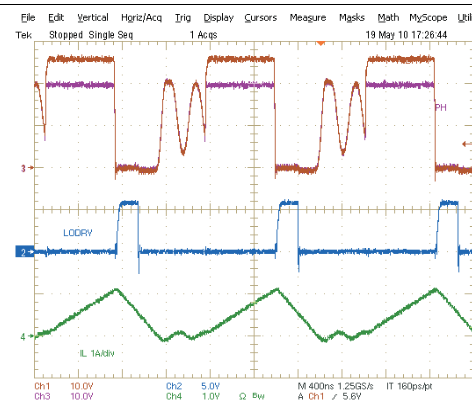
CH1: ILIM, 1V/div
CH4: inductor current, 1A/div, 4us/div

图 4. Charge Disable by ILIM



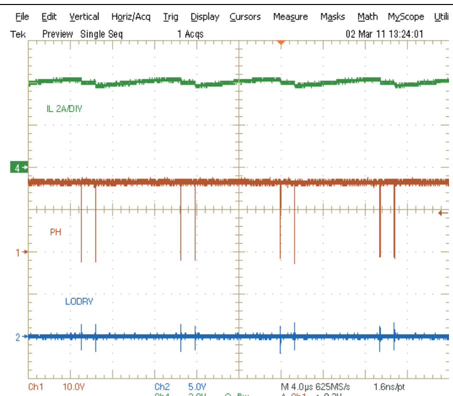
CH1: PHASE, 10V/div, CH2: LODRV, 5V/div
CH3: HIDRV, 10V/div
CH4: inductor current, 2A/div, 400ns/div

图 5. Continuous Conduction Mode Switching Waveforms



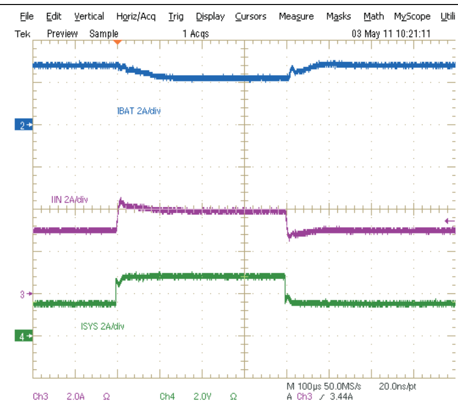
CH1: PHASE, 10V/div, CH2: LODRV, 5V/div
CH3: HIDRV, 10V/div
CH4: inductor current, 1A/div, 400ns/div

图 6. Cycle-by-Cycle Synchronous to Non-synchronous



CH1: PHASE, 10V/div, CH2: LODRV, 5V/div
CH4: inductor current, 2A/div, 4us/div

图 7. 100% Duty and Refresh Pulse



CH2: battery current, 2A/div, CH3: adapter current, 2A/div
CH4: system load current, 2A/div, 100us/div

图 8. System Load Transient (Input DPM)

7 Parameter Measurement Information

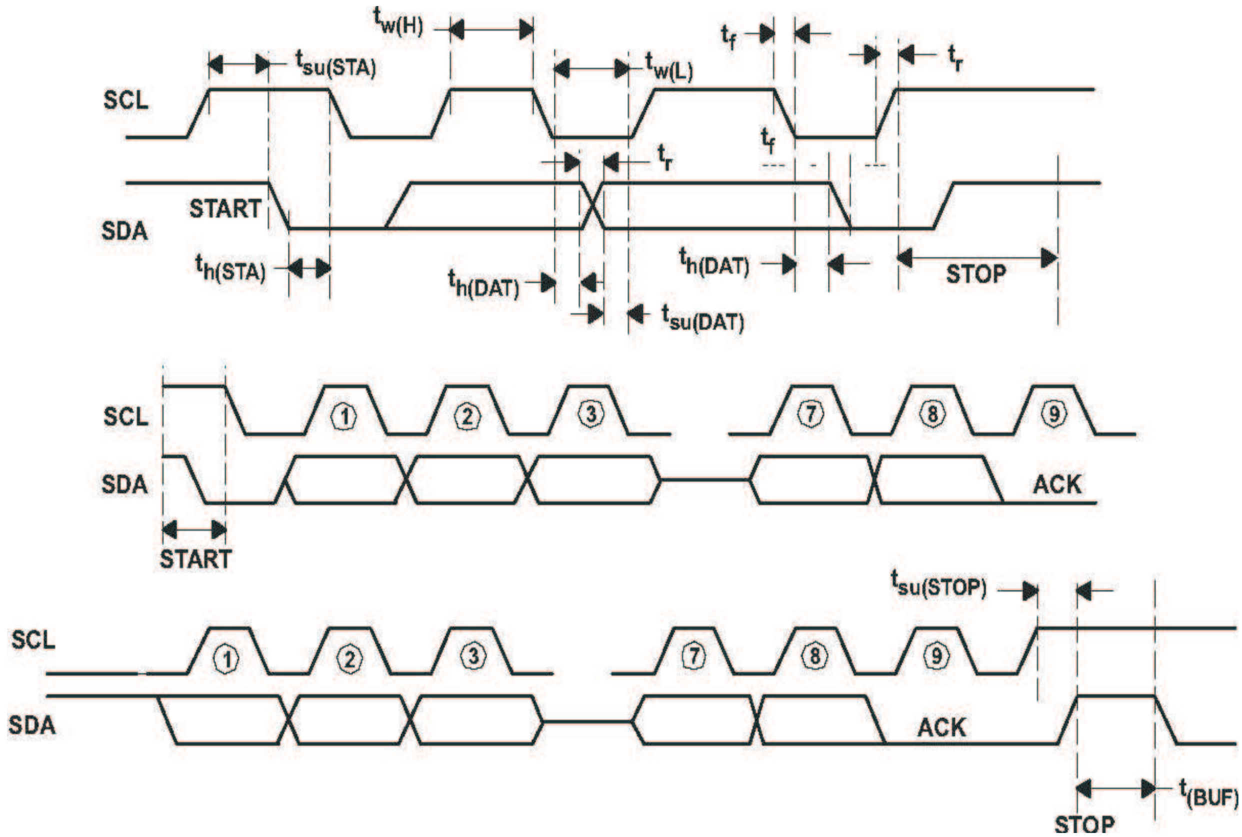


图 9. SMBus Communication Timing Waveforms

8 Detailed Description

8.1 Overview

The bq24725A is a 1-4 cell battery charge controller with power selection for space-constrained, multi-chemistry portable applications such as notebook and detachable ultrabook. It supports wide input range of input sources from 4.5V to 24V, and 1-4 cell battery for a versatile solution.

The bq24725A supports automatic system power source selection with separate drivers for n-channel MOSFETS on the adapter side and battery side.

The bq24725A features Dynamic Power Management (DPM) to limit the input power and avoid AC adapter over-loading. During battery charging, as the system power increases, the charging current will reduce to maintain total input current below adapter rating.

The SMBus controls input current, charge current and charge voltage registers with high resolution, high accuracy regulation limits.

8.2 Functional Block Diagram

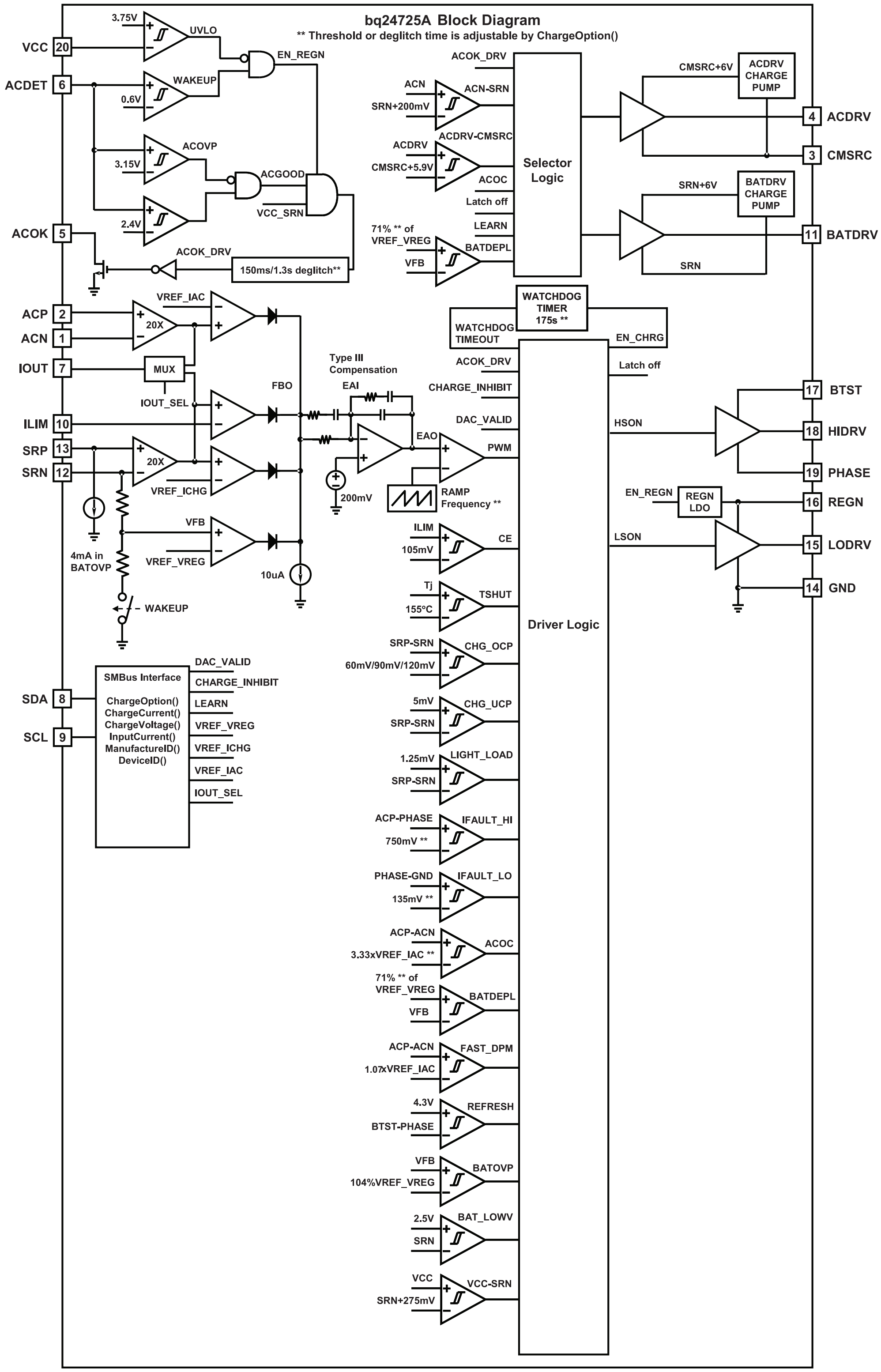


图 10. Functional Block Diagram for bq24725A

8.3 Feature Description

8.3.1 SMBus Interface

The bq24725A operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. The bq24725A uses a simplified subset of the commands documented in System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The bq24725A uses the SMBus Read-Word and Write-Word protocols (see 图 11) to communicate with the smart battery. The bq24725A performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the bq24725A has two identification registers a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus communication is enabled with the following conditions:

- V_{VCC} is above UVLO;
- V_{ACDET} is above 0.6V;

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors (10kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. 图 12 and 图 13 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the bq24725A because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The bq24725A supports the charger commands as described in 表 2.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

Preset to 0b0001001 — ChargeCurrent() = 0x14H, ChargeVoltage() = 0x15H, InputCurrent() = 0x3FH, ChargeOption() = 0x12H — D7 D0 — D15 D8

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001 — DeviceID() = 0xFFH, ManufacturerID() = 0xFEH, ChargeCurrent() = 0x14H, ChargeVoltage() = 0x15H, InputCurrent() = 0x3FH, ChargeOption() = 0x12H — Preset to 0b0001001 — D7 D0 — D15 D8

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE (white cells)
SLAVE TO MASTER (shaded cells)

图 11. SMBus Write-Word and Read-Word Protocols

Feature Description (接下页)

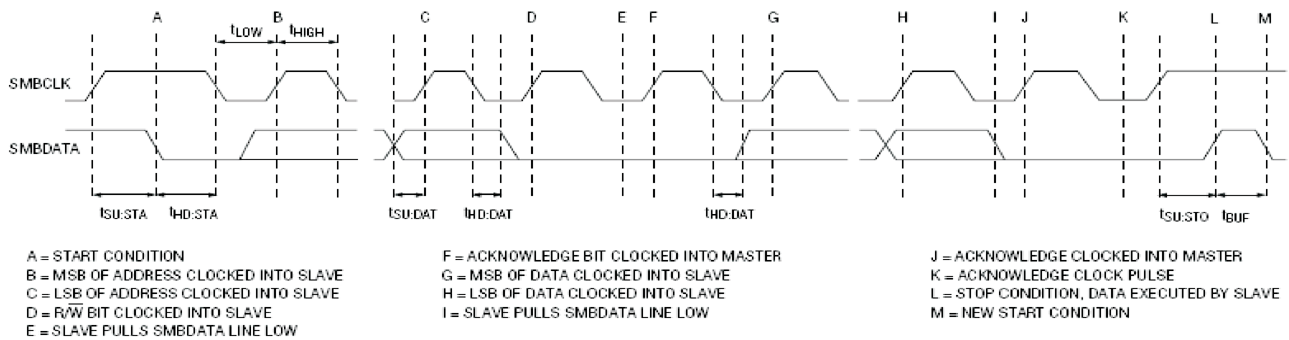


图 12. SMBus Write Timing

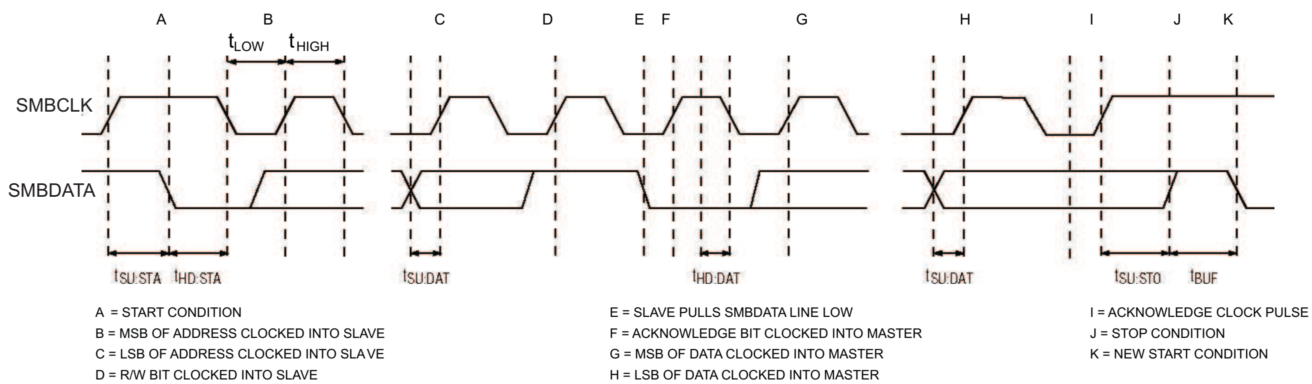


图 13. SMBus Read Timing

8.4 Device Functional Modes

8.4.1 Adapter Detect and ACOK Output

The bq24725A uses an ACOK comparator to determine the source of power on VCC pin, either from the battery or adapter. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage, but lower than the maximum allowed adapter voltage.

The open drain ACOK output requires external pull up resistor to system digital rail for a high level. It can be pulled to external rail under the following conditions:

- V_{VCC} > UVLO;
- 2.4V < V_{ACDET} < 3.15V (not in ACOVP condition, nor in low input voltage condition);
- V_{VCC}–V_{SRN} > 275mV (not in sleep mode);

The first time after IC POR always gives 150ms ACOK rising edge delay no matter what the ChargeOption register value is. Only after the ACDET pin voltage is pulled below 2.4V (but not below 0.6V, which resets the IC and forces the next ACOK rising edge deglitch time to be 1.3s) and the ACFET has been turned off at least one time, the 1.3s (or 150ms) delay time is effective for the next time the ACDET pin voltage goes above 2.4V. To change this option, the VCC pin voltage must above UVLO, and the ACDET pin voltage must be above 0.6V which enables the IC SMBus communication and sets ChargeOption() bit[15] to 0 which sets the next ACOK rising deglitch time to be 150ms. The purpose of the default 1.3s rising edge deglitch time is to turn off the ACFET long enough when the ACDET pin is pulled below 2.4V by excessive system current, such as over current or short circuit.

Device Functional Modes (接下页)

8.4.2 Adapter Over Voltage (ACOVP)

When the ACDET pin voltage is higher than 3.15V, it is considered as adapter over voltage. ACOK will be pulled low, and charge will be disabled. ACFET will be turned off to disconnect the high voltage adapter to system during ACOVP. BATFET will be turned on if turns on conditions are valid. See the *System Power Selection* section for details.

When ACDET pin voltage falls below 3.15V and above 2.4V, it is considered as adapter voltage returns back to normal voltage. ACOK will be pulled high by external pull up resistor. BATFET will be turned off and ACFET and RBFET will be turned on to power the system from adapter. The charge can be resumed if enable charge conditions are valid. See the *Enable and Disable Charging* section for details.

8.4.3 System Power Selection

The bq24725A automatically switches adapter or battery power to system. The battery is connected to system at POR if battery exists. The battery is disconnected from system and the adapter is connected to system after default 150ms delay (first time, the next time default is 1.3s and can be changed to 150ms) if ACOK goes HIGH. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The ACDRV drives a pair of common-source (CMSRC) n-channel power MOSFETs (ACFET and RBFET) between adapter and ACP (see 图 18 for details). The ACFET separates adapter from battery or system, and provides a limited di/dt when plugging in adapter by controlling the ACFET turn-on time. Meanwhile it protects adapter when system or battery is shorted. The RBFET provides negative input voltage protection and battery discharge protection when adapter is shorted to ground, and minimizes system power dissipation with its low $R_{DS(on)}$ compared to a Schottky diode.

When the adapter is not present, ACDRV is pulled to CMSRC to keep ACFET and RBFET off, disconnecting adapter from system. BATDRV stays at V_{SRN} + 6V to connect battery to system if all the following conditions are valid:

- V_{VCC} > UVLO;
- V_{SRN} > UVLO;
- V_{ACN} < 200mV above V_{SRN} (ACN_SRN comparator);

Approximately 150ms (first time; the next time default is 1.3s and can be changed to 150ms) after the adapter is detected (ACDET pin voltage between 2.4V and 3.15V), the system power source begins to switch from battery to adapter if all the following conditions are valid:

- Not in LEARN mode or in LEARN mode and V_{SRN} is lower than battery depletion threshold;
- ACOK high

The gate drive voltage on ACFET and RBFET is V_{CMSRC} + 6V. If the ACFET/RBFET have been turned on for 20ms, and the voltage across gate and source is still less than 5.9V, ACFET and RBFET will be turned off. After 1.3s delay, it resumes turning on ACFET and RBFET. If such a failure is detected seven times within 90 seconds, ACFET/RBFET will be latched off and an adapter removal and system shut down is required to force ACDET < 0.6V to reset the IC. After IC reset from latch off, ACFET/RBFET can be turned on again. After 90 seconds, the failure counter will be reset to zero to prevent latch off. With ACFET/RBFET off, charge is disabled.

To turn off ACFET/RBFET, one of the following conditions must be valid:

- In LEARN mode and V_{SRN} is above battery depletion threshold;
- ACOK low

To limit the in-rush current on ACDRV pin, CMSRC pin and BATDRV pin, a 4kΩ resistor is recommended on each of the three pins.

To limit the adapter inrush current when ACFET is turned on to power system from adapter, the Cgs and Cgd external capacitor of ACFET must be carefully selected. The larger the Cgs and Cgd capacitance, the slower turn on of ACFET will be and less inrush current of adapter. However, if Cgs or Cgd is too large, the ACDRV-CMSRC voltage may still go low after the 20ms turn on time window is expired. To make sure ACFET will not be turned on when adapter is hot plugged in, the Cgs value should be 20 times or higher than Cgd. The most cost effective way to reduce adapter in-rush current is to minimize system total capacitance.

Device Functional Modes (接下页)

8.4.4 Battery LEARN Cycle

A battery LEARN cycle can be activated via SMBus command (ChargeOption() bit[6]=1 enable LEARN cycle, bit[6]=0 disable LEARN cycle). When LEARN is enabled with ACFET/RBFET connected, the system power selector logic is over-driven to switch to battery by turning off ACFET/RBFET and turning on BATFET. LEARN function allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge/charge cycle. The controller automatically exits LEARN cycle when the battery voltage is below battery depletion threshold, and the system switches back to adapter input by turning off BATFET and turning on ACFET/RBFET. After LEARN cycle, the LEARN bit is automatically reset to 0. The battery depletion threshold can be set to 59.19%, 62.65%, 66.55%, and 70.97% of voltage regulation level via SMBus command (ChargeOption() bit[12:11]).

8.4.5 Enable and Disable Charging

In Charge mode, the following conditions have to be valid to start charge:

- Charge is enabled via SMBus (ChargeOption() bit [0]=0, default is 0, charge enabled);
- ILIM pin voltage higher than 105mV;
- All three regulation limit DACs have valid value programmed;
- ACOK is valid (See the Adapter Detect and ACOK Output section for details);
- ACFET and RBFET turns on and gate voltage is high enough (See the *System Power Selection* section for details);
- V_{SRN} does not exceed BATOVP threshold;
- IC Temperature does not exceed TSHUT threshold;
- Not in ACOC condition (See the *Input Over Current Protection (ACOC)* section for details);

One of the following conditions will stop on-going charging:

- Charge is inhibited via SMBus (ChargeOption() bit[0]=1);
- ILIM pin voltage lower than 75mV;
- One of three regulation limit DACs is set to 0 or out of range;
- ACOK is pulled low (See the *Adapter Detect and ACOK Output* section for details);
- ACFET turns off;
- V_{SRN} exceeds BATOVP threshold;
- TSHUT IC temperature threshold is reached;
- ACOC is detected (See the *Input Over Current Protection (ACOC)* section for details);
- Short circuit is detected (See the *Inductor Short, MOSFET Short Protection* section for details);
- Watchdog timer expires if watchdog timer is enabled (See the *Charger Timeout* section for details);

8.4.6 Automatic Internal Soft-Start Charger Current

Every time the charge is enabled, the charger automatically applies soft-start on charge current to avoid any overshoot or stress on the output capacitors or the power converter. The charge current starts at 128mA, and the step size is 64mA in CCM mode for a 10mΩ current sensing resistor. Each step lasts around 240µs in CCM mode, till it reaches the programmed charge current limit. No external components are needed for this function. During DCM mode, the soft start up current step size is larger and each step lasts for longer time period due to the intrinsic slow response of DCM mode.

8.4.7 High Accuracy Current Sense Amplifier

As an industry standard, high accuracy current sense amplifier (CSA) is used to monitor the input current or the charge current, selectable via SMBUS (ChargeOption() bit[5]=0 select the input current, bit[5]=1 select the charge current) by host. The CSA senses voltage across the sense resistor by a factor of 20 through the IOUT pin. Once VCC is above UVLO and ACDET is above 0.6V, CSA turns on and IOUT output becomes valid. To lower the voltage on current monitoring, a resistor divider from IOUT to GND can be used and accuracy over temperature can still be achieved.

A 100pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay.

Device Functional Modes (接下页)

8.4.8 Charge Timeout

The bq24725A includes a watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175s (adjustable via ChargeOption() command). If a watchdog timeout occurs all register values keep unchanged but charge is suspended. Write ChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. The watchdog timer can be disabled, or set to 44s, 88s or 175s via SMBus command (ChargeOption() bit[14:13]). After watchdog timeout write ChargeOption() bit[14:13] to disable watchdog timer also resume charging.

8.4.9 Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage mode control scheme and internal type III compensation network. The LC output filter gives a characteristic resonant frequency

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \tag{1}$$

The resonant frequency fo is used to determine the compensation to ensure there is sufficient phase margin and gain margin for the target bandwidth. The LC output filter should be selected to give a resonant frequency of 10–20 kHz nominal for the best performance. Suggest component value as charge current of 750kHz default switching frequency is shown in 表 1.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

表 1. Suggest Component Value as Charge Current of Default 750kHz Switching Frequency

Charge Current	2A	3A	4A	6A	8A
Output Inductor Lo (µH)	6.8 or 8.2	5.6 or 6.8	3.3 or 4.7	3.3	2.2
Output Capacitor Co (µF)	20	20	20	30	40
Sense Resistor (mΩ)	10	10	10	10	10

The bq24725A has three loops of regulation: input current, charge current and charge voltage. The three loops are brought together internally at the error amplifier. The maximum voltage of the three loops appears at the output of the error amplifier EAO. An internal saw-tooth ramp is compared to the internal error control signal EAO (see 图 10) to vary the duty-cycle of the converter. The ramp has offset of 200mV in order to allow 0% duty-cycle.

When the battery charge voltage approaches the input voltage, EAO signal is allowed to exceed the saw-tooth ramp peak in order to get a 100% duty-cycle. If voltage across BTST and PHASE pins falls below 4.3V, a refresh cycle starts and low-side n-channel power MOSFET is turned on to recharge the BTST capacitor. It can achieve duty cycle of up to 99.5%.

8.4.10 Continuous Conduction Mode (CCM)

With sufficient charge current the bq24725A's inductor current never crosses zero, which is defined as continuous conduction mode. The controller starts a new cycle with ramp coming up from 200mV. As long as EAO voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds EAO voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM mode, the inductor current is always flowing and creates a fixed two-pole system. Having the LSFET turn-on keeps the power dissipation low, and allows safely charging at high currents.

8.4.11 Discontinuous Conduction Mode (DCM)

During the HSFET off time when LSFET is on, the inductor current decreases. If the current goes to zero, the converter enters Discontinuous Conduction Mode. Every cycle, when the voltage across SRP and SRN falls below 5mV (0.5A on 10mΩ), the under current-protection comparator (UCP) turns off LSFET to avoid negative inductor current, which may boost the system via the body diode of HSFET.

During the DCM mode the loop response automatically changes. It changes to a single pole system and the pole is proportional to the load current.

Both CCM and DCM are synchronous operation with LSFET turn-on every clock cycle. If the average charge current goes below 125mA on 10mΩ current sensing resistor or the battery voltage falls below 2.5V, the LSFET keeps turn-off. The battery charger operates in non-synchronous mode and the current flows through the LSFET body diode. During non-synchronous operation, the LSFET turns on only for a refreshing pulse to charge the BTST capacitor. If the average charge current goes above 250mA on 10mΩ current sensing resistor, the LSFET exits non-synchronous mode and enters synchronous mode to reduce LSFET power loss.

8.4.12 Input Over Current Protection (ACOC)

The bq24725A cannot maintain the input current level if the charge current has been already reduced to zero. After the system current continues increasing to the 3.33X of input current DAC set point (with 4.2ms blank out time), ACFET/RBFET is latches off and an adapter removal and system shutdown is required to force ACDET < 0.6V to reset IC. After IC reset from latch off, ACFET/RBFET can be turned on again.

The ACOC function threshold can be set to 3.33x of input DPM current or disable this function via SMBus command (ChargeOption() bit [1]).

8.4.13 Charge Over Current Protection (CHGOCP)

The bq24725A has a cycle-by-cycle peak over current protection. It monitors the voltage across SRP and SRN, and prevents the current from exceeding of the threshold based on the DAC charge current set point. The high-side gate drive turns off for the rest of the cycle when the over current is detected, and resumes when the next cycle starts.

The charge OCP threshold is automatically set to 6A, 9A, and 12A on a 10mΩ current sensing resistor based on charge current register value. This prevents the threshold to be too high which is not safe or too low which can be triggered in normal operation. Proper inductance should be selected to prevent OCP triggered in normal operation due to high inductor current ripple.

8.4.14 Battery Over Voltage Protection (BATOVP)

The bq24725A will not allow the high-side and low-side MOSFET to turn-on when the battery voltage at SRN exceeds 104% of the regulation voltage set-point. If BATOVP last over 30ms, charger is completely disabled. This allows quick response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A 4mA current sink from SRP to GND is on only during BATOVP and allows discharging the stored output inductor energy that is transferred to the output capacitors. Set ChargeVoltage() register value to 0V will not trigger BATOVP function.

8.4.15 Battery Shorted to Ground (BATLOWV)

The bq24725A will limit inductor current if the battery voltage on SRN falls below 2.5V. After 1ms charge is reset. After 4-5 ms the charge is resumed with soft-start if all the enable conditions in the “Enable and Disable Charging” sections are satisfied. This prevents any overshoot current in inductor which can saturate inductor and may damage the MOSFET. The charge current is limited to 0.5A on 10mΩ current sensing resistor when BATLOWV condition persists and LSFET keeps off. The LSFET turns on only for a refreshing pulse to charge BTST capacitor.

8.4.16 Thermal Shutdown Protection (TSHUT)

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO current limit is reduced to 16mA. Once the temperature falls below 135°C, charge can be resumed with soft start.

8.4.17 EMI Switching Frequency Adjust

The charger switching frequency can be adjusted ±18% to solve EMI issue via SMBus command. ChargeOption() bit [9]=0 disable the frequency adjust function. To enable frequency adjust function, set ChargeOption() bit[9]=1. Set ChargeOption() bit [10]=0 to reduce switching frequency, set bit[10]=1 to increase switching frequency.

If frequency is reduced, for a fixed inductor the current ripple is increased. Inductor value must be carefully selected so that it will not trig cycle-by-cycle peak over current protection even for the worst condition such as higher input voltage, 50% duty cycle, lower inductance and lower switching frequency.

8.4.18 Inductor Short, MOSFET Short Protection

The bq24725A has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across $R_{DS(on)}$ of the MOSFETs after a certain amount of blanking time. In case of MOSFET short or inductor short circuit, the over current condition is sensed by two comparators and two counters will be triggered. After seven times of short circuit events, the charger will be latched off and ACFET and RBFET are turned off to disconnect adapter from system. BATFET is turned on to connect battery pack to system. To reset the charger from latch-off status, the IC VCC pin must be pulled below UVLO or the ACDET pin must be pulled below 0.6V. This can be achieved by removing the adapter and shut down the operation system. The low side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[7] =0, 1 set the low side threshold 135mV and 230mV respectively. The high side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[8] = 0, 1 disable the function and set the threshold 750mV respectively.

Due to the certain amount of blanking time to prevent noise when MOSFET just turn on, the cycle-by-cycle charge over-current protection may detect high current and turn off MOSFET first before the short circuit protection circuit can detect short condition because the blanking time has not finished. In such a case the charger may not be able to detect short circuit and counter may not be able to count to seven then latch off. Instead the charger may continuously keep switching with very narrow duty cycle to limit the cycle-by-cycle current peak value. However, the charger should still be safe and will not cause failure because the duty cycle is limited to a very short of time and MOSFET should be still inside the safety operation area. During a soft start period, it may takes long time instead of just seven switching cycles to detect short circuit based on the same blanking time reason.

8.5 Register Maps

8.5.1 Battery-Charger Commands

The bq24725A supports six battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in 表 2. ManufacturerID() and DeviceID() can be used to identify the bq24725A. The ManufacturerID() command always returns 0x0040H and the DeviceID() command always returns 0x000BH.

表 2. Battery Charger Command Summary

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	POR STATE
0x12H	ChargeOption()	Read or Write	Charger Options Control	0xF902H
0x14H	ChargeCurrent()	Read or Write	7-Bit Charge Current Setting	0x0000H
0x15H	ChargeVoltage()	Read or Write	11-Bit Charge Voltage Setting	0x0000H
0x3FH	InputCurrent()	Read or Write	6-Bit Input Current Setting	0x1000H
0XFEH	ManufacturerID()	Read Only	Manufacturer ID	0x0040H
0xFFH	DeviceID()	Read Only	Device ID	0x000BH

8.5.2 Setting Charger Options

By writing ChargeOption() command (0x12H or 0b00010010), bq24725A allows users to change several charger options after POR (Power On Reset) as shown in 表 3.

图 14. Charge Options Register (0x12H)

15	14	13	12	11	10	9	8
ACOK Deglitch Time Adjust	WATCHDOG Timer Adjust		BAT Depletion Comparator Threshold Adjust		EMI Switching Frequency Adjust	EMI Switching Frequency Enable	IFAULT_HI Comparator Threshold Adjust
R/W	R/W		R/W R/W		R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IFAULT_LOW Comparator Threshold Adjust	LEARN Enable	IOUT Selection	AC Adapter Indication (Read Only)	Not in use	Not in use	ACOC Threshold Adjust	Charge Inhibit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 3. Charge Options Register (0x12H)

Bit	Field	Type	Reset	Description
[15]	ACOK Deglitch Time Adjust		R/W	Adjust ACOK deglitch time. After POR, the first time the adapter plug in occurs, deglitch time is always 150ms no matter if this bit is 0 or 1. This bit only sets the next ACOK deglitch time after ACFET turns off at least one time. To change this option, VCC pin voltage must be above UVLO and ACDET pin voltage must be above 0.6V to enable IC SMBus communication. 0: ACOK rising edge deglitch time 150ms **1: ACOK rising edge deglitch time 1.3s <default at POR>**
[14:13]	WATCHDOG Timer Adjust		R/W	Set maximum delay between consecutive SMBus Write charge voltage or charge current command. The charge will be suspended if IC does not receive write charge voltage or write charge current command within the watchdog time period and watchdog timer is enabled. The charge will be resumed after receive write charge voltage or write charge current command when watchdog timer expires and charge suspends. 00: Disable Watchdog Timer 01: Enabled, 44 sec 10: Enabled, 88 sec **11: Enable Watchdog Timer (175s) <default at POR>**

表 3. Charge Options Register (0x12H) (接下页)

Bit	Field	Type	Reset	Description
[12:11]	BAT Depletion Comparator Threshold Adjust		R/W	This is used for LEARN function battery over discharge protection. During LEARN cycle, when the IC detects battery voltage is below depletion voltage threshold, the IC turns off BATFET and turned on ACFET to power the system from AC adapter instead of the battery. The rising edge hysteresis is 340mV. Set ChargeVoltage() register value to 0V will disable this function. 00: Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell) 01: Falling Threshold = 62.65% of voltage regulation limit (~2.631V/cell) 10: Falling Threshold = 66.55% of voltage regulation limit (~2.795V/cell) **11: Falling Threshold = 70.97% of voltage regulation limit (~2.981V/cell) < default at POR>**
[10]	EMI Switching Frequency Adjust		R/W	**0: Reduce PWM switching frequency by 18% <default at POR>** 1: Increase PWM switching frequency by 18%
[9]	EMI Switching Frequency Enable		R/W	**0: Disable adjust PWM switching frequency <default at POR>** 1: Enable adjust PWM switching frequency
[8]	IFAULT_HI Comparator Threshold Adjust		R/W	Short circuit protection high side MOSFET voltage drop comparator threshold. 0: function is disabled **1: 750mV <default at POR>**
[7]	IFAULT_LOW Comparator Threshold Adjust		R/W	Short circuit protection low side MOSFET voltage drop comparator threshold. **0: 135mV <default at POR>** 1: 230mV
[6]	LEARN Enable		R/W	Set this bit 1 start battery learn cycle. IC turns off ACFET and turns on BATFET to discharge battery capacity. When battery voltage reaches threshold defined in bit [12;11], the BATFET is turned off and ACFET is turned on to finish battery learn cycle. After finished learn cycle, this bit is automatically reset to 0. Set this bit 0 will stop battery learn cycle. IC turns off BATFET and turns on ACFET. **0: Disable LEARN Cycle <default at POR>** 1: Enable LEARN Cycle
[5]	IOUT Selection		R/W	**0: IOUT is the 20x adapter current amplifier output <default at POR>** 1: IOUT is the 20x charge current amplifier output
[4]	AC Adapter Indication (Read Only)		R/W	**0: AC adapter is not present (ACDET < 2.4V) <default at POR>** 1: AC adapter is present (ACDET > 2.4V)
[3]	Not in use		R/W	**0 at POR**
[2]	Not in use		R/W	**0 at POR**
[1]	ACOC Threshold Adjust		R/W	0: function is disabled **1: 3.33x of input current regulation limit <default at POR>**
[0]	Charge Inhibit		R/W	**0: Enable Charge <default at POR>** 1: Inhibit Charge

8.5.3 Setting the Charge Current

To set the charge current, write a 16bit ChargeCurrent() command (0x14H or 0b00010100) using the data format listed in 表 4. With 10mΩ sense resistor, the bq24725A provides a charge current range of 128mA to 8.128A, with 64mA step resolution. Sending ChargeCurrent() below 128mA or above 8.128A clears the register and terminates charging. Upon POR, charge current is 0A. A 0.1µF capacitor between SRP and SRN for differential mode filtering is recommended, 0.1µF capacitor between SRN and ground for common mode filtering, and an optional 0.1µF capacitor between SRP and ground for common mode filtering. Meanwhile, the capacitance on SRP should not be higher than 0.1µF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle under-current and over current detection.

The SRP and SRN pins are used to sense R_{SR} with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. If the current sensing resistor value is too high, it may trigger an over current protection threshold because the current ripple voltage is too high. In such a case, either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value no more than 20mΩ is suggested.

To provide secondary protection, the bq24725A has an ILIM pin with which the user can program the maximum allowed charge current. Internal charge current limit is the lower one between the voltage set by ChargeCurrent(), and voltage on ILIM pin. To disable this function, the user can pull ILIM above 1.6V, which is the maximum charge current regulation limit. 公式 2 shows the voltage set on ILIM pin with respect to the preferred charge current limit:

$$V_{ILIM} = 20 \times (V_{SRP} - V_{SRN}) = 20 \times I_{CHG} \times R_{SR} \quad (2)$$

图 15. Charge Current Register (0x14H), Using 10mΩ Sense Resistor

15	14	13	12	11	10	9	8
Not in use	Not in use	Not in use	Charge Current, DACICHG 6	Charge Current, DACICHG 5	Charge Current, DACICHG 4	Charge Current, DACICHG 3	Charge Current, DACICHG 2
R/W	R/W		R/W R/W		R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Charge Current, DACICHG 1	Charge Current, DACICHG 0	Not in use	Not in use	Not in use	Not in use	Not in use	Not in use
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 4. Charge Current Register (0x14H), Using 10mΩ Sense Resistor

Bit	Field	Type	Reset	Description
[15]	Not in use		R/W	Not used.
[14]	Not in use		R/W	Not used.
[13]	Not in use			Not used.
[12]	Charge Current, DACICHG 6		R/W	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
[11]	Charge Current, DACICHG 5		R/W	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
[10]	Charge Current, DACICHG 4		R/W	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
[9]	Charge Current, DACICHG 3		R/W	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
[8]	Charge Current, DACICHG 2		R/W	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
[7]	Charge Current, DACICHG 1		R/W	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
[6]	Charge Current, DACICHG 0		R/W	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
[5]	Not in use		R/W	Not used.
[4]	Not in use		R/W	Not used.
[3]	Not in use		R/W	Not used.
[2]	Not in use		R/W	Not used.
[1]	Not in use		R/W	Not used.
[0]	Not in use		R/W	Not used.

8.5.4 Setting the Charge Voltage

To set the output charge regulation voltage, write a 16bit ChargeVoltage() command (0x15H or 0b00010101) using the data format listed in 表 5. The bq24725A provides charge voltage range from 1.024V to 19.200V, with 16mV step resolution. Sending ChargeVoltage() below 1.024V or above 19.2V clears the register and terminates charging. Upon POR, charge voltage limit is 0V.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, and place a decoupling capacitor (0.1µF recommended) as close to the IC as possible to decouple high frequency noise.

图 16. Charge Voltage Register (0x15H)

15	14	13	12	11	10	9	8
Not in use	Charge Voltage, DACV 10	Charge Voltage, DACV 9	Charge Voltage, DACV 8	Charge Voltage, DACV 7	Charge Voltage, DACV 6	Charge Voltage, DACV 5	Charge Voltage, DACV 4
R/W	R/W		R/W R/W		R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Charge Voltage, DACV 3	Charge Voltage, DACV 2	Charge Voltage, DACV 1	Charge Voltage, DACV 0	Not in use	Not in use	Not in use	Not in use
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 5. Charge Voltage Register (0x15H)

Bit	Field	Type	Reset	Description
[15]	Not in use		R/W	Not used.
[14]	Charge Voltage, DACV 10		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
[13]	Charge Voltage, DACV 9		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
[12]	Charge Voltage, DACV 8		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
[11]	Charge Voltage, DACV 7		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
[10]	Charge Voltage, DACV 6		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
[9]	Charge Voltage, DACV 5		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
[8]	Charge Voltage, DACV 4		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.
[7]	Charge Voltage, DACV 3		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
[6]	Charge Voltage, DACV 2		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
[5]	Charge Voltage, DACV 1		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage
[4]	Charge Voltage, DACV 0		R/W	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
[3]	Not in use		R/W	Not used.
[2]	Not in use		R/W	Not used.
[1]	Not in use		R/W	Not used.
[0]	Not in use		R/W	Not used.

8.5.5 Setting Input Current

System current normally fluctuates as portions of the system are powered up or put to sleep. With the input current limit, the output current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current, from a wall cube or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the bq24725A decreases the charge current to provide priority to system load current. As the system current rises, the available charge current drops linearly to zero. Thereafter, all input current goes to system load and input current increases.

During DPM regulation, the total input current is the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, and can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \left[\frac{I_{BATTERY} \times V_{BATTERY}}{V_{IN} \times \eta}\right] + I_{BIAS} \quad (3)$$

where η is the efficiency of the charger buck converter (typically 85% to 95%).

To set the input current limit, write a 16-bit InputCurrent() command (0x3FH or 0b00111111) using the data format listed in 表 6. When using a 10mΩ sense resistor, the bq24725A provides an input-current limit range of 128mA to 8.064A, with 128mA resolution. The suggested input current limit is set to no less than 512mA. Sending InputCurrent() below 128mA or above 8.064A clears the register and terminates charging. Upon POR, the default input current limit is 4096mA.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss.

If input current rises above FAST_DPM threshold, the charger will reduce charging current to allow the input current drop. After a typical 260-µs delay time, if input current is still above FAST_DPM threshold, the charger will shut down. The charger will soft restart to charge the battery if the adapter still has power to charge the battery. This prevents a crash if the adapter is overloaded when the system has a high and fast loading transient. The waiting time between shut down and restart charging is a natural response time of the input current limit loop.

图 17. Input Current Register (0x3FH), Using 10mΩ Sense Resistor

15	14	13	12	11	10	9	8
Not in use	Not in use	Not in use	Input Current, DACIIN 5	Input Current, DACIIN 4	Input Current, DACIIN 3	Input Current, DACIIN 2	Input Current, DACIIN 1
R/W	R/W		R/W R/W		R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Input Current, DACIIN 0	Not in use	Not in use	Not in use	Not in use	Not in use	Not in use	Not in use
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 6. Input Current Register (0x3FH), Using 10mΩ Sense Resistor

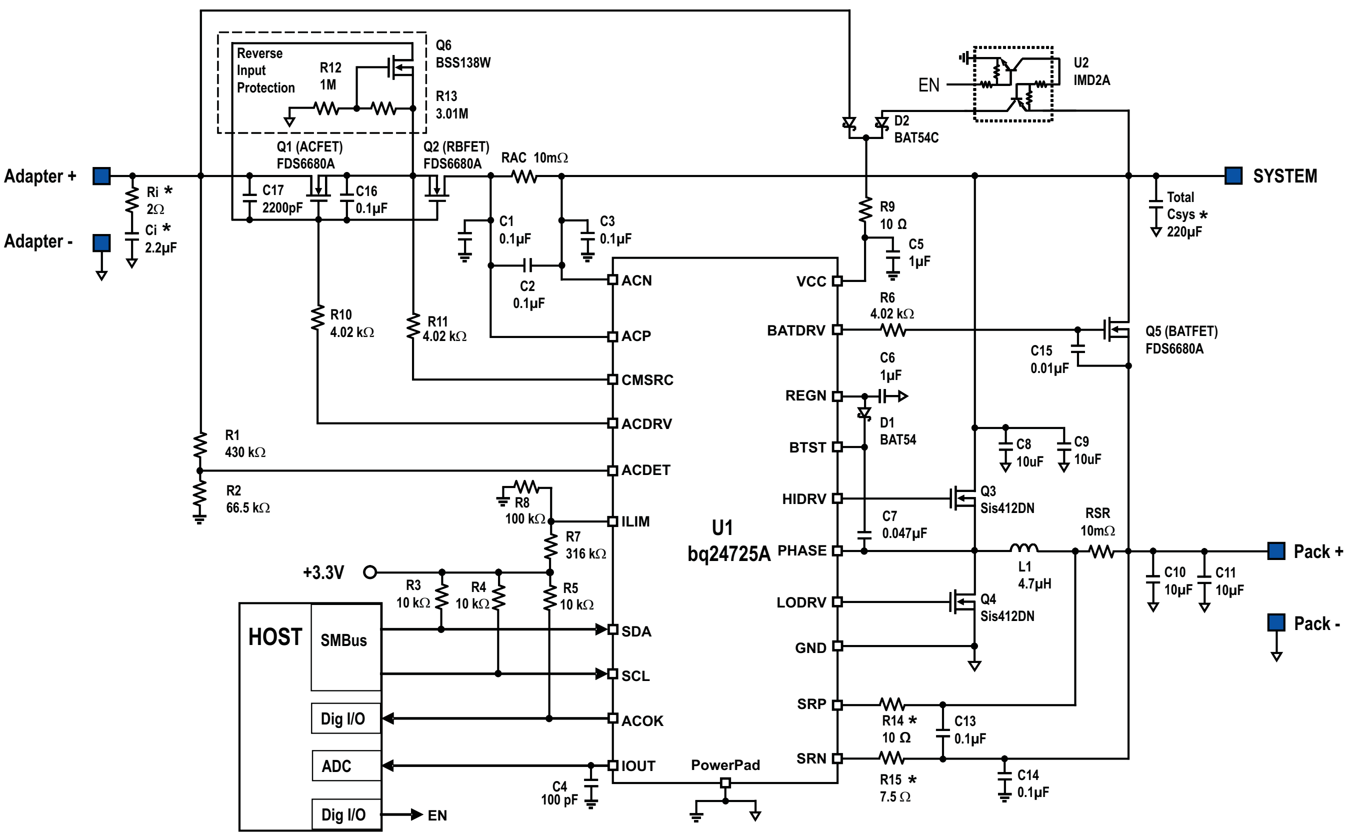
Bit	Field	Type	Reset	Description
[15]	Not in use		R/W	Not used.
[14]	Not in use		R/W	Not used.
[13]	Not in use		R/W	Not used.
[12]	Input Current, DACIIN 5		R/W	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current.
[11]	Input Current, DACIIN 4		R/W	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
[10]	Input Current, DACIIN 3		R/W	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
[9]	Input Current, DACIIN 2		R/W	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
[8]	Input Current, DACIIN 1		R/W	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
[7]	Input Current, DACIIN 0		R/W	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.
[6]	Not in use		R/W	Not used.
[5]	Not in use		R/w	Not used.
[4]	Not in use		R/W	Not used.
[3]	Not in use		R/W	Not used.
[2]	Not in use		R/W	Not used.
[1]	Not in use		R/W	Not used.
[0]	Not in use		R/W	Not used.

9 Application and Implementation

9.1 Application Information

The bq24725AEVM-710 evaluation module (EVM) is a complete charger module for evaluating the bq24725A. The application curves were taken using the bq24725AEVM-710. Refer to the EVM user's guide (SLUU507) for EVM information.

9.2 Typical Application



F_s = 750kHz, I_{ADPT} = 4.096A, I_{CHRG} = 2.944A, I_{LIM} = 4A, V_{CHRG} = 12.592V, 90W adapter and 3S2P battery pack

Use 0Ω for better current sensing accuracy, use 10Ω/7.5Ω resistor for reversely battery connection protection. See application information about negative output voltage protection for hard shorts on battery to ground or battery reversely connection.

The total Csys is the lump sum of system capacitance. It is not required by charger IC. Use Ri and Ci for adapter hot plug-in voltage spike damping. See application information about input filter design.

图 18. Typical System Schematic with Two NMOS Selector

Typical Application (接下页)

表 7. Component List for Typical System Circuit of 图 18

PART DESIGNATOR	QTY	DESCRIPTION
C1, C2, C3, C13, C14, C16	6	Capacitor, Ceramic, 0.1µF, 25V, 10%, X7R, 0603
C4	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0603
C5, C6	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 0603
C7	1	Capacitor, Ceramic, 0.047µF, 25V, 10%, X7R, 0603
C8, C9, C10, C11	4	Capacitor, Ceramic, 10µF, 25V, 10%, X7R, 1206
C15	1	Capacitor, Ceramic, 0.01µF, 25V, 10%, X7R, 0603
C17	1	Capacitor, Ceramic, 2200pF, 25V, 10%, X7R, 0603
Ci	1	Capacitor, Ceramic, 2.2µF, 25V, 10%, X7R, 1210
Csys	1	Capacitor, Electrolytic, 220µF, 25V
D1	1	Diode, Schottky, 30V, 200mA, SOT-23, Fairchild, BAT54
D2	1	Diode, Dual Schottky, 30V, 200mA, SOT-23, Fairchild, BAT54C
Q1, Q2, Q5	3	N-channel MOSFET, 30V, 12.5A, SO-8, Fairchild, FDS6680A
Q3, Q4	2	N-channel MOSFET, 30V, 12A, PowerPAK 1212-8, Vishay Siliconix, SiS412DN
Q6	1	N-channel MOSFET, 50V, 0.2A, SOT-323, Diodes, BSS138W
L1	1	Inductor, SMT, 4.7µH, 5.5A, Vishay Dale, IHLP2525CZER4R7M01
R1	1	Resistor, Chip, 430kΩ, 1/10W, 1%, 0603
R2	1	Resistor, Chip, 66.5kΩ, 1/10W, 1%, 0603
R3, R4, R5	3	Resistor, Chip, 10kΩ, 1/10W, 1%, 0603
R6, R10, R11	3	Resistor, Chip, 4.02kΩ, 1/10W, 1%, 0603
R7	1	Resistor, Chip, 316kΩ, 1/10W, 1%, 0603
R8	1	Resistor, Chip, 100kΩ, 1/10W, 1%, 0603
R9	1	Resistor, Chip, 10Ω, 1/4W, 1%, 1206
R12	1	Resistor, Chip, 1.00MΩ, 1/10W, 1%, 0603
R13	1	Resistor, Chip, 3.01MΩ, 1/10W, 1%, 0603
R14	1	Resistor, Chip, 10Ω, 1/10W, 5%, 0603
R15	1	Resistor, Chip, 7.5Ω, 1/10W, 5%, 0603
RAC, RSR	2	Resistor, Chip, 0.01Ω, 1/2W, 1%, 1206
Ri	1	Resistor, Chip, 2Ω, 1/2W, 1%, 1210
U1	1	Charger controller, 20 pin VQFN, TI, bq24725ARGR
U2	1	Dual digital transistor, 40V, 30mA, SC-74, Rohm, IMD2A

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (1)	17.7V < Adapter Voltage < 24V
Input Current Limit (1)	3.2A for 65W adapter
Battery Charge Voltage (2)	12592mV for 3s battery
Battery Charge Current (2)	4096mA for 3s battery
Battery Discharge Current (2)	6144mA for 3s battery

(1) Refer to adapter specification for settings for Input Voltage and Input Current Limit.
(2) Refer to battery specification for settings.

9.2.2 Detailed Design Procedure

9.2.2.1 Negative Output Voltage Protection

Reversely insert the battery pack into the charger output during production or hard shorts on battery to ground will generate negative output voltage on SRP and SRN pin. IC internal electrostatic-discharge (ESD) diodes from GND pin to SRP or SRN pins and two anti-parallel (AP) diodes between SRP and SRN pins can be forward biased and negative current can pass through the ESD diodes and AP diodes when output has negative voltage. Insert two small resistors for SRP and SRN pins to limit the negative current level when output has negative voltage. Suggest resistor value is 10 ohm for SRP pin and 7-8 Ω for SRN pin. After adding small resistors, the suggested pre-charge current is at least 192mA for a 10m ohm current sensing resistor. Another method is using a small diode parallel with output capacitor, when battery connection is reversed the diode turns on and limits the negative voltage level. Using diode protection method without insertion of small resistors into SRP and SRN pin can get the best charging current accuracy.

9.2.2.2 Reverse Input Voltage Protection

Q6, R12 and R13 in 图 18 gives system and IC protection from reversed adapter voltage. In normal operation, Q6 is turned off by negative Vgs. When adapter voltage is reversed, Q6 Vgs is positive. As a result, Q6 turns on to short gate and source of Q2 so that Q2 is off. Q2 body diode blocks negative voltage to system. However, CMSRC and ACDRV pins need R10 and R11 to limit the current due to the ESD diode of these pins when turned on. Q6 must has low Vgs threshold voltage and low Qgs gate charge so it turns on before Q2 turns on. R10 and R11 must have enough power rating for the power dissipation when the ESD diode is on. In 图 25, the Schottky diode D3 gives the reverse adapter voltage protection, no extra small MOSFET and resistors are needed.

In 图 26, the Schottky diode Din is used for the reverse adapter voltage protection.

9.2.2.3 Reduce Battery Quiescent Current

When the adapter is not present, if VCC is powered with voltage higher than UVLO directly or indirectly (such as through a LDO or switching converter) from battery, the internal BATFET charge pump gives the BATFET pin 6V higher voltage than the SRN pin to drive the n-channel BATFET. As a result, the battery has higher quiescent current. This is only necessary when the battery powers the system due to a high system current that goes through the MOSFET channel instead of the body diode to reduce conduction loss and extend the battery working life. When the system is totally shutdown, it is not necessary to let the internal BATFET charge pump work. The host controller can use a digital signal EN to disconnect the battery power path to the VCC pin by U2 in 图 18. As a result, battery quiescent current can be minimized. The host controller still can get power from BATFET body diode because the total system current is the lowest when the system is shutdown, so there is no high conduction loss of the body diode.

9.2.2.4 Inductor Selection

The bq24725A has three selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12V to 16.8V, and 12V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq24725A has charge under current protection (UCP) by monitoring charging current sensing resistor cycle-by-cycle. The typical cycle-by-cycle UCP threshold is 5mV falling edge corresponding to 0.5A falling edge for a 10mΩ charging current sensing resistor. When the average charging current is less than 125mA for a 10mΩ charging current sensing resistor, the low side MOSFET is off until BTST capacitor voltage needs to refresh the charge. As a result, the converter relies on low side MOSFET body diode for the inductor freewheeling current.

9.2.2.5 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by 公式 6:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (6)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 19-20V input voltage. 10-20µF capacitance is suggested for typical of 3-4A charging current.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.6 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

The bq24725A has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25V X7R or X5R for output capacitor. 10-20µF capacitance is suggested for a typical of 3-4A charging current. Place the capacitors after charging current sensing resistor to get the best charge current regulation accuracy.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.7 Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 19-20V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; \; FOM_{bottom} = R_{DS(on)} \times Q_G \quad (8)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \quad (9)$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (10)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (11)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (12)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (13)$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \quad (14)$$

The maximum charging current in non-synchronous mode can be up to 0.25A for a 10mΩ charging current sensing resistor or 0.5A if battery voltage is below 2.5V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

9.2.2.8 Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in 图 19. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin. C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10us time constant to limit the dv/dt on VCC pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

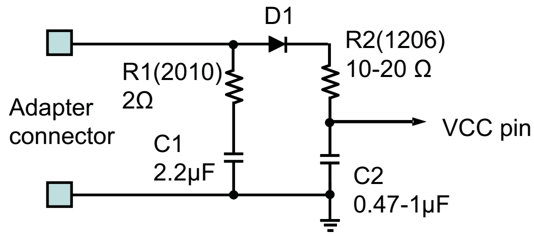


图 19. Input Filter

9.2.2.9 bq24725A Design Guideline

The bq24725A has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across $R_{DS(on)}$ of the MOSFETs after a certain amount of blanking time. For a MOSFET short or inductor short circuit, the over current condition is sensed by two comparators, and two counters are triggered. After seven occurrences of a short circuit event, the charger will be latched off. To reset the charger from latch-off status, reconnect the adapter. 图 20 shows the bq24725A short circuit protection block diagram.

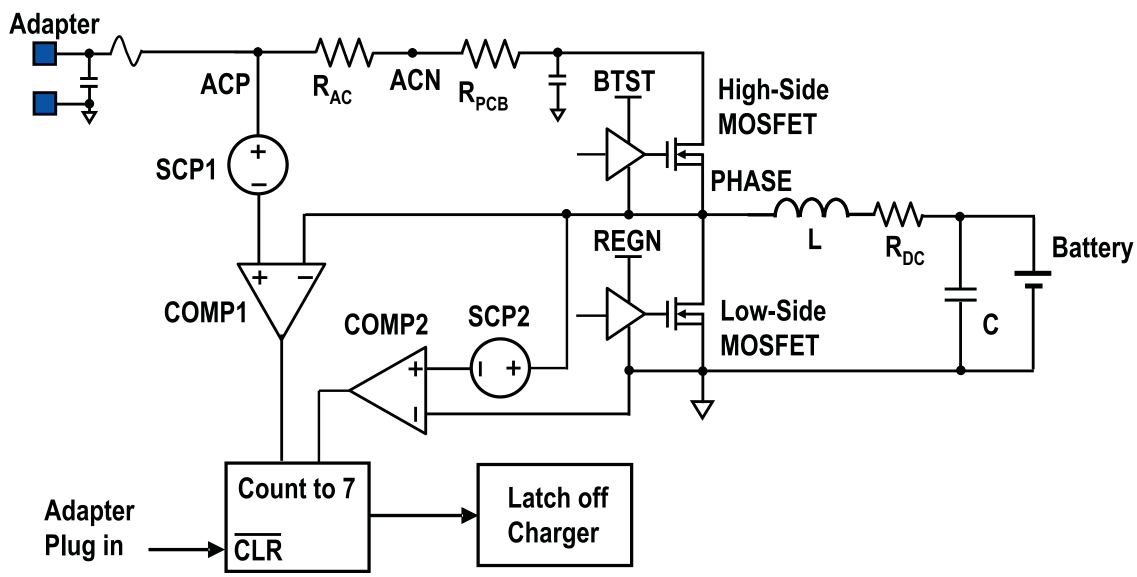


图 20. Block Diagram of bq24725A Short Circuit Protection

In normal operation, the low side MOSFET current is from source to drain which generates a negative voltage drop when it turns on, as a result the over current comparator can not be triggered. When the high side switch short circuit or inductor short circuit happens, the large current of low side MOSFET is from drain to source and can trig low side switch over current comparator. bq24725A senses the low side switch voltage drop through the PHASE pin and GND pin.

The high-side FET short is detected by monitoring the voltage drop between ACP and PHASE. As a result, it not only monitors the high side switch voltage drop, but also the adapter sensing resistor voltage drop and PCB trace voltage drop from ACN terminal of R_{AC} to charger high side switch drain. Usually, there is a long trance between input sensing resistor and charger converting input, a careful layout will minimize the trace effect.

To prevent unintentional charger shut down in normal operation, MOSFET $R_{DS(on)}$ selection and PCB layout is very important. 图 21 shows a improvement PCB layout example and its equivalent circuit. In this layout, the system current path and charger input current path is not separated, as a result, the system current causes voltage drop in the PCB copper and is sensed by the IC. The worst layout is when a system current pull point is after charger input; as a result all system current voltage drops are counted into over current protection comparator. The worst case for IC is when the total system current and charger input current sum equals the DPM current. When the system pulls more current, the charger IC tries to regulate the R_{AC} current as a constant current by reducing the charging current.

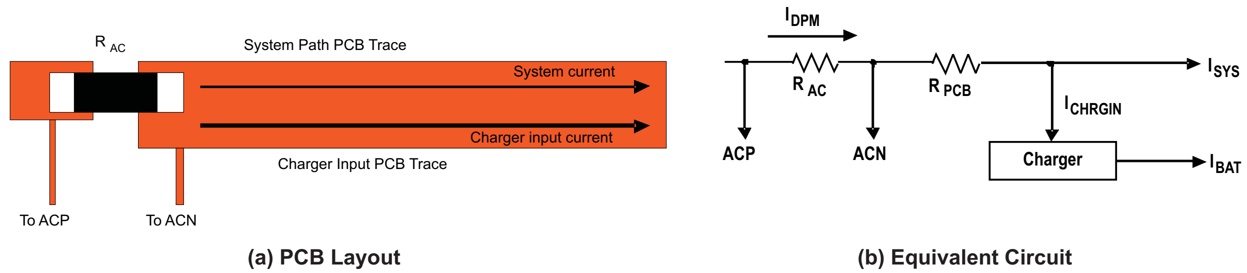


图 21. Need improve PCB layout example.

图 22 shows the optimized PCB layout example. The system current path and charge input current path is separated, as a result the IC only senses charger input current caused PCB voltage drop and minimized the possibility of unintentional charger shut down in normal operation. This also makes PCB layout easier for high system current application.

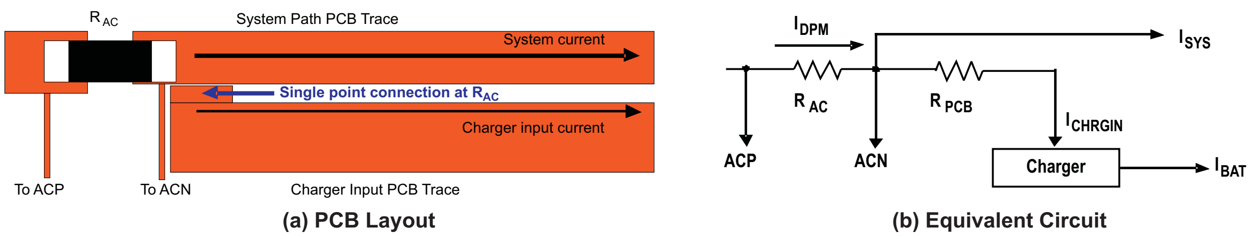


图 22. Optimized PCB layout example.

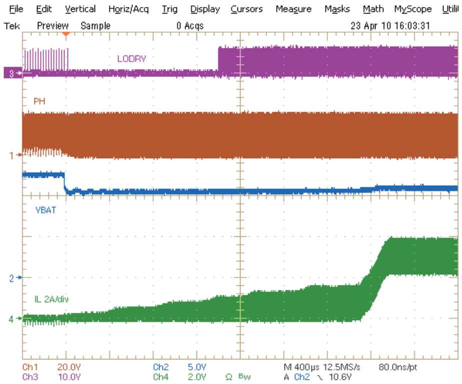
The total voltage drop sensed by IC can be express as the following equation.

$$V_{top} = R_{AC} \times I_{DPM} + R_{PCB} \times (I_{CHRGIN} + (I_{DPM} - I_{CHRGIN}) \times k) + R_{DS(on)} \times I_{PEAK} \quad (15)$$

where the R_{AC} is the AC adapter current sensing resistance, I_{DPM} is the DPM current set point, R_{PCB} is the PCB trace equivalent resistance, I_{CHRGIN} is the charger input current, k is the PCB factor, $R_{DS(on)}$ is the high side MOSFET turn on resistance and I_{PEAK} is the peak current of inductor. Here the PCB factor k equals 0 means the best layout shown in 图 22 where the PCB trace only goes through charger input current while k equals 1 means the worst layout shown in 图 21 where the PCB trace goes through all the DPM current. The total voltage drop must below the high side short circuit protection threshold to prevent unintentional charger shut down in normal operation.

The low side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[7] =0, 1 set the low side threshold 135mV and 230mV respectively. The high side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[8] = 0, 1 disable the function and set the threshold 750mV respectively. For a fixed PCB layout, host should set proper short circuit protection threshold level to prevent unintentional charger shut down in normal operation.

9.3 Application Curves



CH1: PHASE, 20V/div, CH2: battery voltage, 5V/div

CH3: LODRV, 10V/div

CH4: inductor current, 2A/div, 400us/div

图 23. Battery Insertion

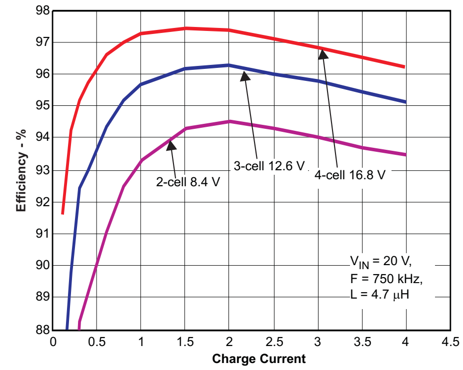
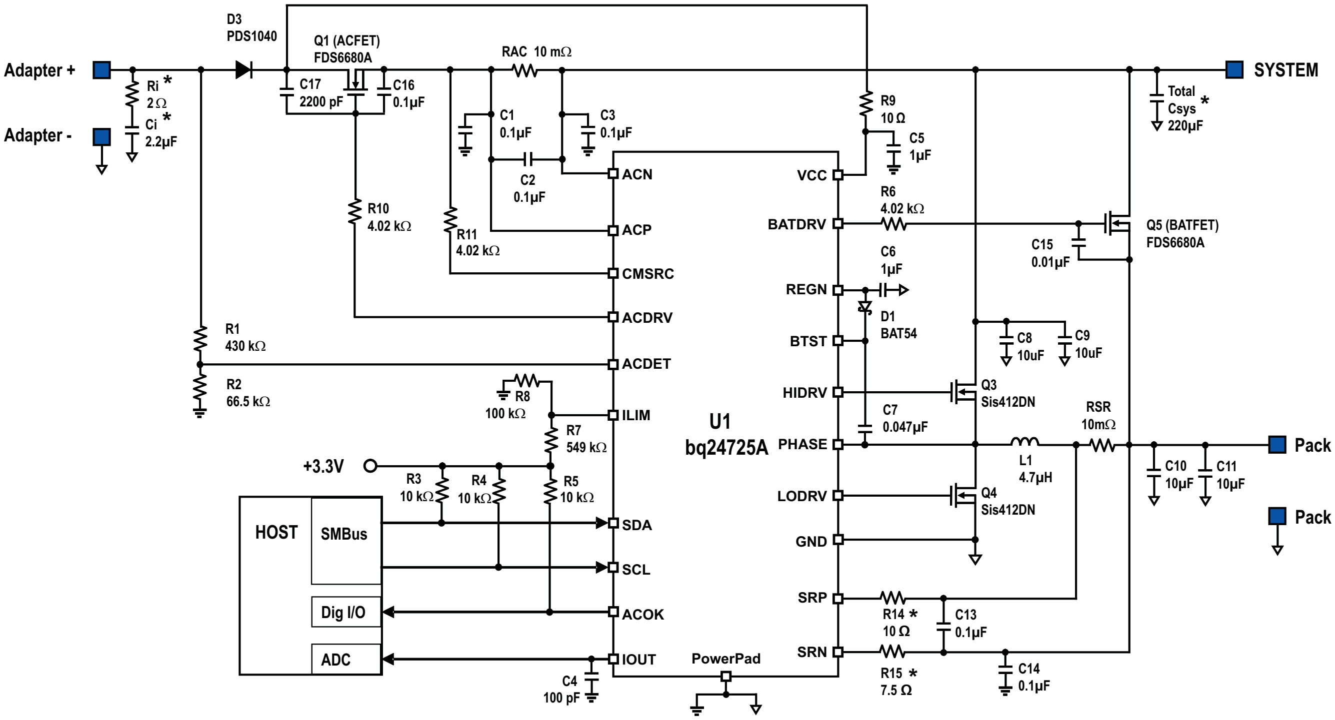


图 24. Efficiency vs Output Current

9.4 System Examples



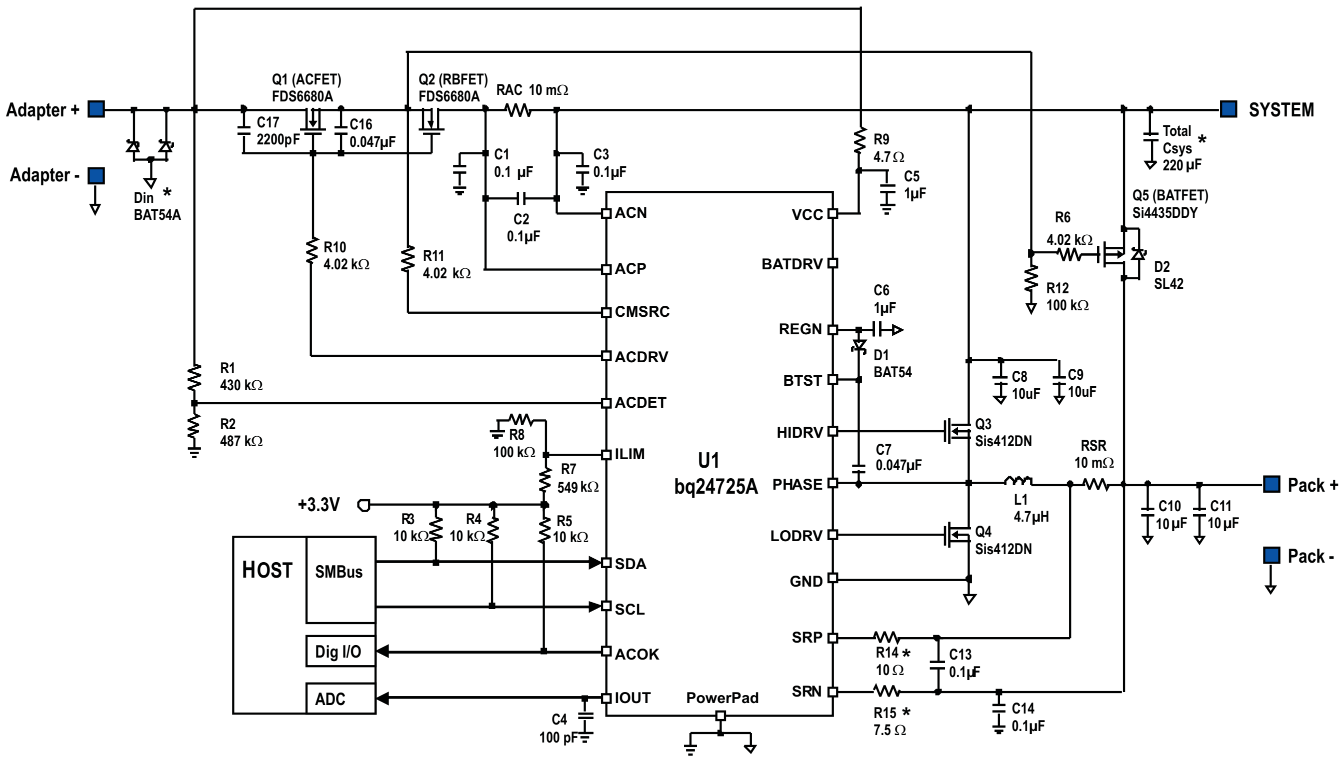
F_S = 750kHz, I_{ADPT} = 2.816A, I_{CHRG} = 1.984A, I_{LIM} = 2.54A, V_{CHRG} = 12.592V, 65W adapter and 3S2P battery pack

Use 0Ω for better current sensing accuracy, use 10Ω/7.5Ω resistor for reversely battery connection protection. See application information about negative output voltage protection for hard shorts on battery to ground or battery reversely connection.

The total Csys is the lump sum of system capacitance. It is not required by charger IC. Use Ri and Ci for adapter hot plug in voltage spike damping. See application information about input filter design.

图 25. Typical System Schematic with One NMOS Selector and Schottky Diode

System Examples (接下页)



F_S = 750kHz, I_{ADPT} = 2.048A, I_{CHRG} = 1.984A, I_{LIM} = 2.54A, V_{CHRG} = 4.200V, 12W adapter and 1S2P battery pack

Use 0Ω for better current sensing accuracy, use 10Ω/7.5Ω resistor for reversely battery connection protection. See application information about negative output voltage protection for hard shorts on battery to ground or battery reversely connection.

The total Csys is the total lump sum of system capacitance. It is not required by charger IC. Use Din for reverse input voltage protection. See application information about reverse input voltage protection.

图 26. Typical System Schematic for 5V Input 1S Battery

10 Power Supply Recommendations

When adapter is attached, and ACOK goes HIGH, the system is connected to adapter through ACFET/RBFET. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage, but lower than the IC maximum allowed input voltage and system maximum allowed voltage.

When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the minimum system voltage so that the battery capacity can be fully utilized for maximum battery life.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 图 27) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see 图 28 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC
5. Place output capacitor next to the sensing resistor output and ground
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible
10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
11. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, See SCBA017 and SLUA271.

11.2 Layout Example

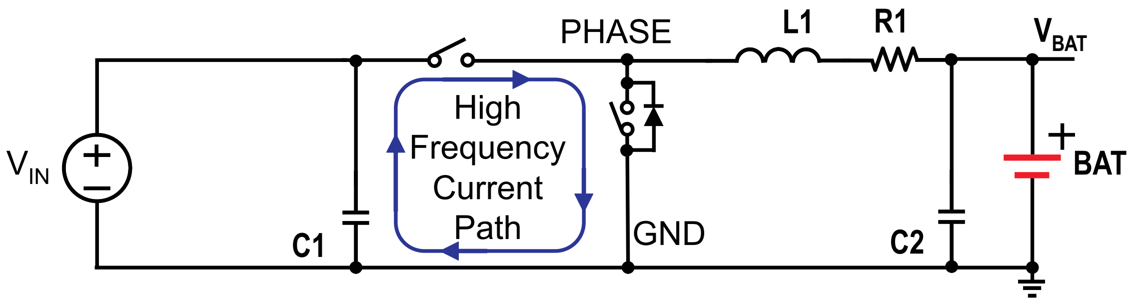


图 27. High Frequency Current Path

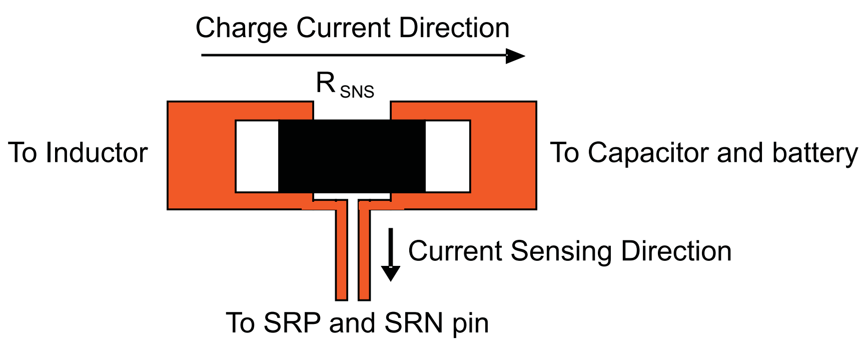


图 28. Sensing Resistor PCB Layout.

12 器件和文档支持

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12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24725ARGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25A	Samples
BQ24725ARGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25A	Samples
HPA01163RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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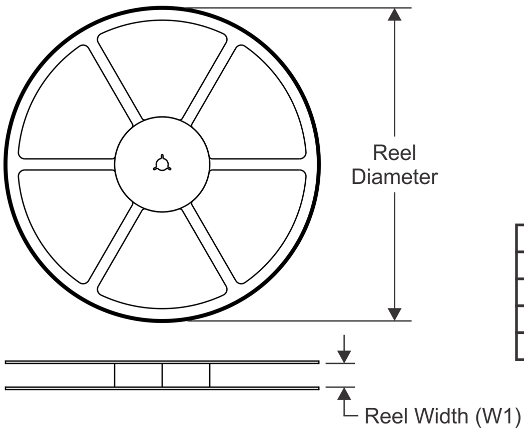
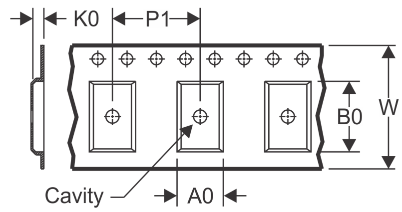
TAPE AND REEL INFORMATION

REEL DIMENSIONS

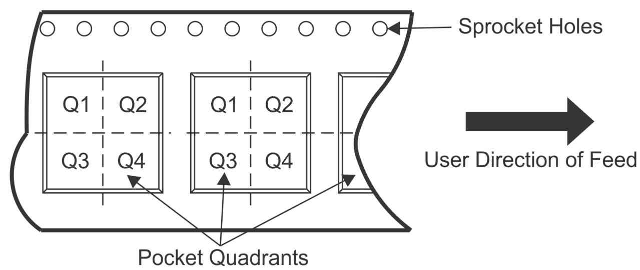


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

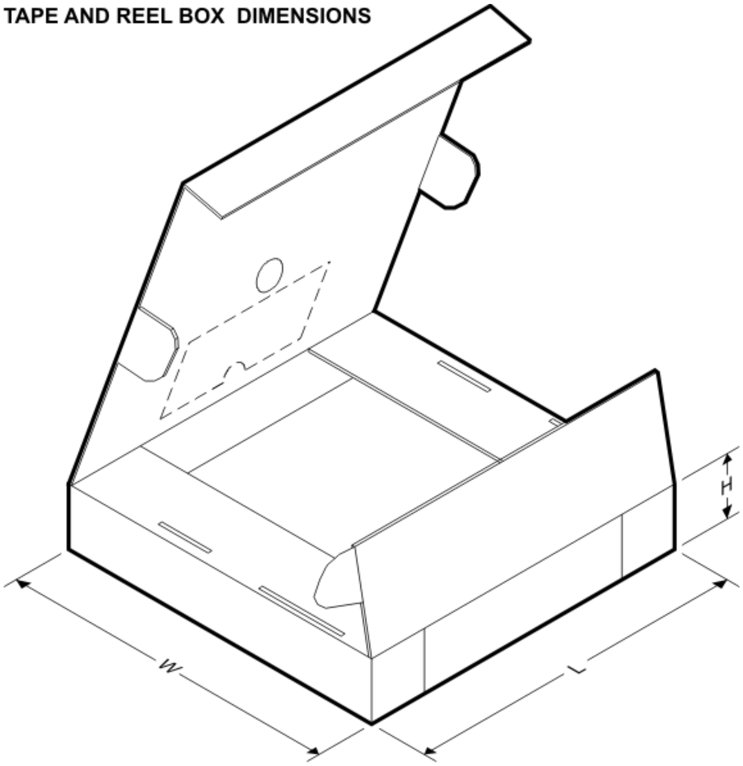
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24725ARGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24725ARGRR	VQFN	RGR	20	3000	330.0	12.4	3.8	3.8	1.1	8.0	12.0	Q1
BQ24725ARGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24725ARGRT	VQFN	RGR	20	250	180.0	12.5	3.8	3.8	1.1	8.0	12.0	Q1

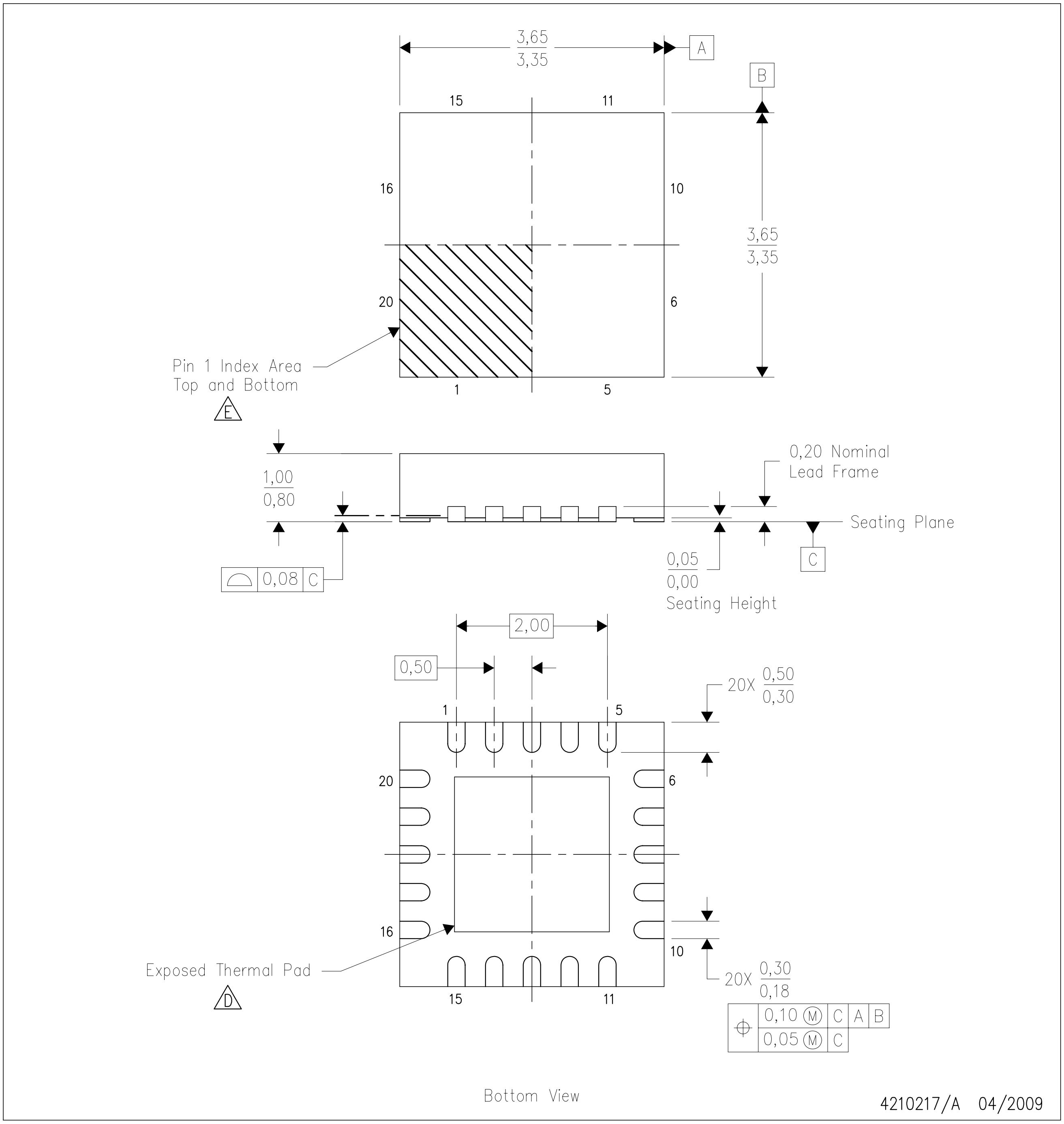
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24725ARGRR	VQFN	RGR	20	3000	552.0	367.0	36.0
BQ24725ARGRR	VQFN	RGR	20	3000	338.0	355.0	50.0
BQ24725ARGRT	VQFN	RGR	20	250	552.0	185.0	36.0
BQ24725ARGRT	VQFN	RGR	20	250	338.0	355.0	50.0

RGR (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

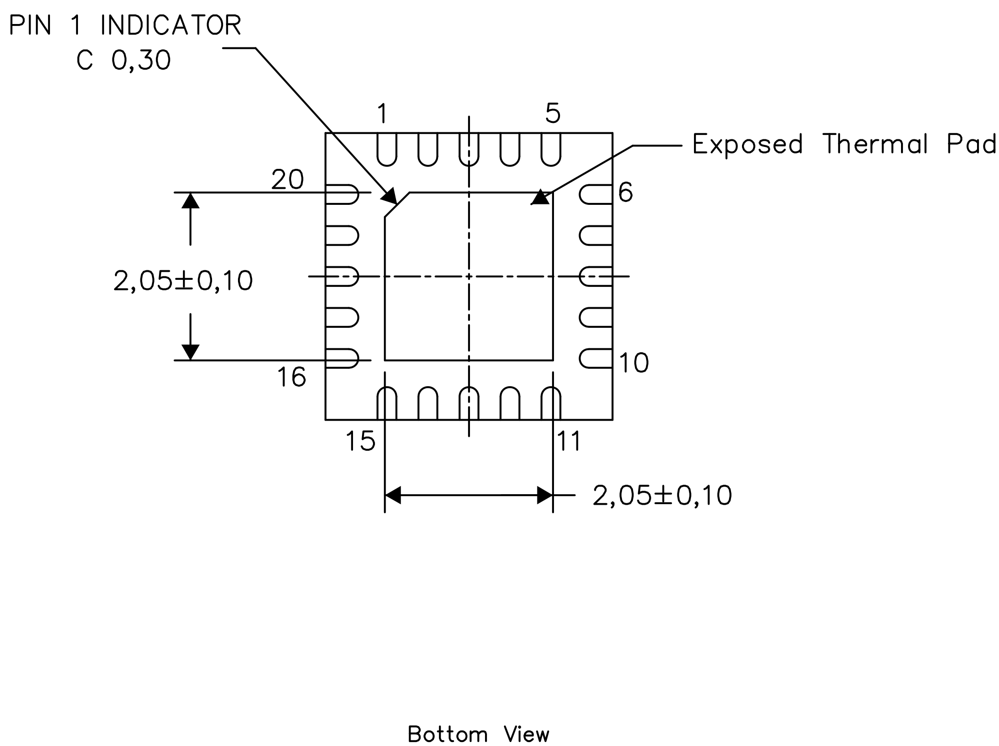
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

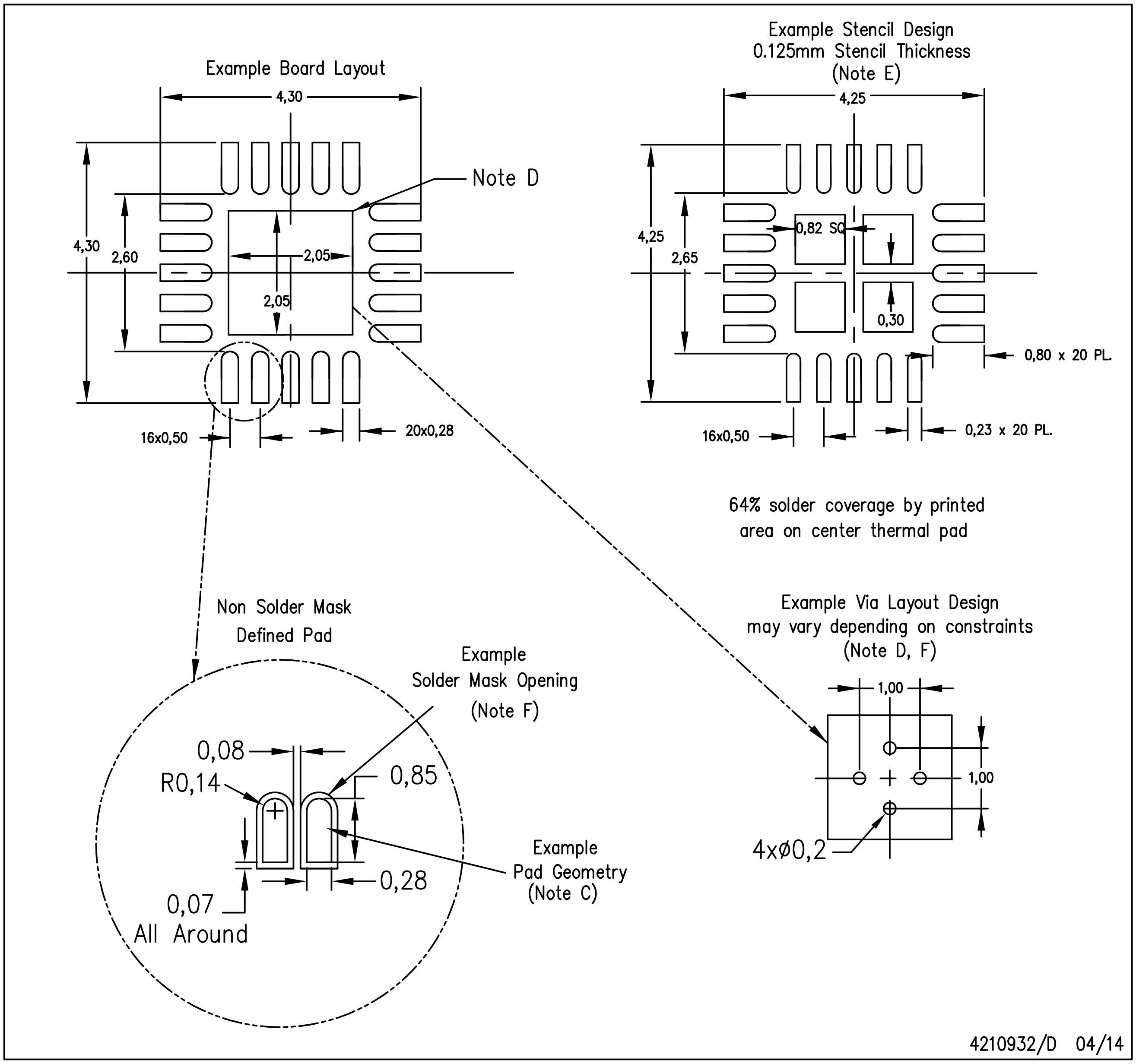


Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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