bq5102x 5W (WPC) 单芯片无线电源接收器

1 特性

- 功耗减少 50% 的强健 5W 解决方案，以改进热性能
  - 针对最薄解决方案的无电感器接收器
  - 可调节输出电压（4.5 至 8V），以实现线圈和热性能优化
  - 完全同步整流器的效率达 96%
  - 效率 97% 的高效后置稳压器
  - 功率 5W 时，系统效率 79%
- 符合 WPC v1.1 标准的通信
- 已获专利的发射器垫 (Transmitter Pad) 检测功能提升了用户体验
- 通过 I^2C 实现的对齐特性使得用户协商能够在 TX 表面找到最佳位置

2 应用范围

- 智能手机、平板电脑和头戴式耳机
- Wi-Fi 热点
- 移动电源
- 其他手持式器件

3 说明

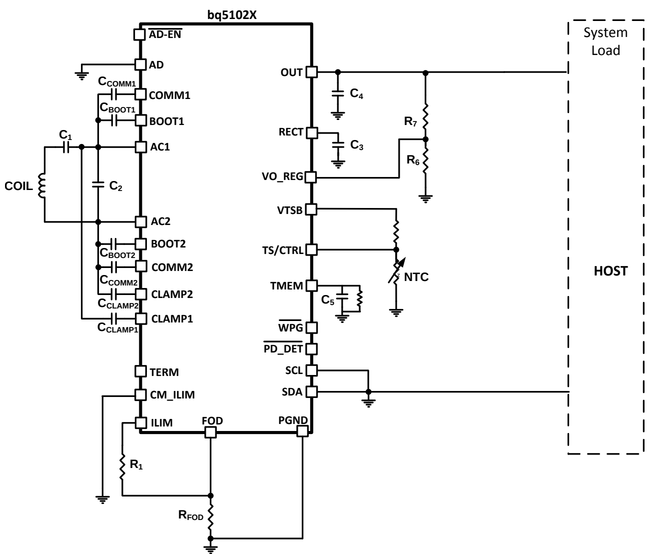
bq5102x 器件是一款全封闭无线电源接收器，此接收器能够在 WPC v1.1 协议下运行，这使得无线电源系统在与 Qi 感应发射器一同使用时能够向系统传送高达 5W 的功率。 bq5102x 器件提供针对这 WPC 技术规格的单个器件功率转换（整流和稳压），以及数字控制和通信。 借助市场领先的效率和可调输出电压，bq5102x 器件可实现独一无二的效率和系统优化。 I^2C 还使得系统设计人员能够执行有趣的全新特性，诸如发射器表面的接收器对齐，或者检测接收器上的异物。 此接收器可在市场领先的封装尺寸、效率和解决方案尺寸中同时实现同步整流、稳压和控制与通信。

器件信息(1)

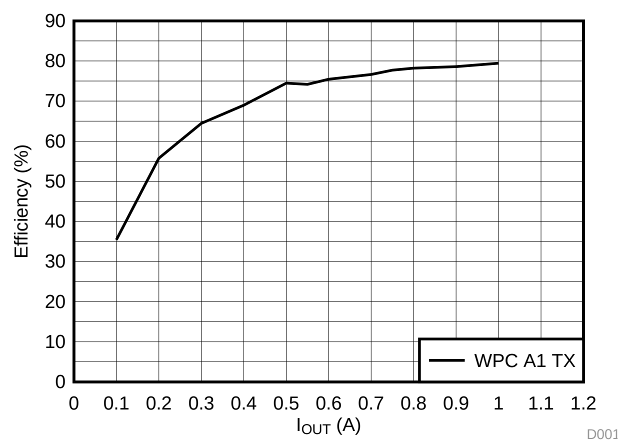
产品型号	封装	封装尺寸（标称值）
bq51020	芯片尺寸球状引脚栅格阵列 (DSBGA) (42)	3.60mm x 2.89mm^2
bq51021		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



bq5102x 系统效率 5V 输出



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5 修订历史记录

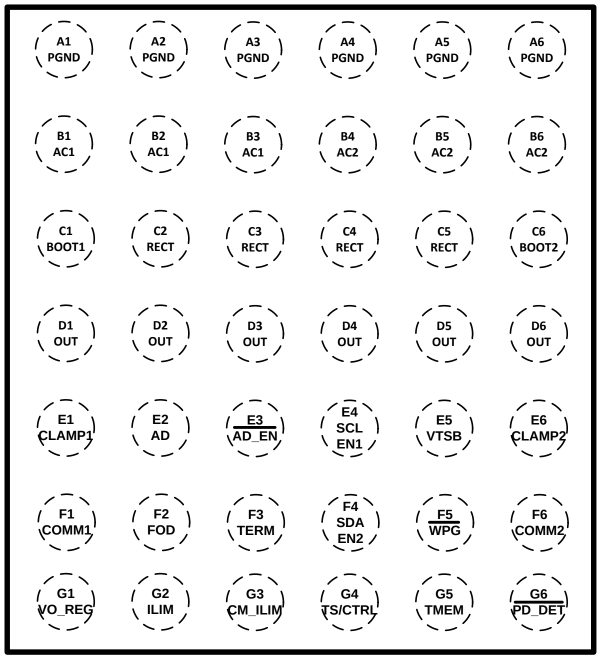
日期	修订版本	注释
2014 年 5 月	*	最初发布版本

Device Comparison Table

Device	Mode	More
bq51221	Dual (WPC v1.1, PMA)	Adjustable output voltage, highest system efficiency, I^2C
bq51021	WPC v1.1	Adjustable output voltage, highest system efficiency, I^2C
bq51020	WPC v1.1	Adjustable output voltage, highest system efficiency, standalone

6 Pin Configuration and Functions

YFP (42 PINS)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AC1	B1, B2, B3	I	AC input power from receiver resonant tank
AC2	B4, B5, B6	I	
AD	E2	I	Adapter sense pin
$\overline{\text{AD-EN}}$	E3	O	Push-pull driver for dual PFET circuit that can pass AD input to the OUT pin; used for adapter mux control
BOOT1	C1	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier
BOOT2	C6	O	
CLAMP1	E1	O	Open-drain FETs used to clamp the secondary voltage by providing low impedance across secondary
CLAMP2	E6	O	
COMM1	F1	O	Open-drain FETs used to communicate with primary by varying reflected impedance
COMM2	F6	O	
CM_ILIM	G3	I	Enables or disables communication current limit; can be pulled high to disable or pull low enable communication current limit
EN1	E4	I	EN1 and EN2 are used for I^2C communication in bq5020. Ground if not needed. SCL and SDA are used in bq51021.
EN2	F4	I	
FOD	F2	I	Input that is used for scaling the received power message
ILIM	G2	I/O	Output current or overcurrent level programming pin
OUT	D1, D2, D3, D4, D5, D6	O	Output pin, used to deliver power to the load

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
$\overline{\text{PD\_DET}}$	G6	O	Open drain output that allows user to sense when receiver is on transmitter surface
PGND	A1, A2, A3, A4, A5, A6	–	Power and logic ground
RECT	C2, C3, C4, C5	O	Filter capacitor for the internal synchronous rectifier
SCL	E4	I	SCL and SDA are used for I^{2}C communication in bq5021. Ground if not needed. EN1 and EN2 are used in bq51020.
SDA	F4	I	
TERM	F3	I	Unused. Float in all WPC receivers
TMEM	G5	O	TMEM allows capacitor to be connected to GND so energy from transmitter ping can be stored to retain memory of state
TS/CTRL	G4	I	Temperature sense. Can be pulled high to send end power transfer (EPT – charge complete) to TX. Can be pulled low to send EPT – Overtemperature
VO_REG	G1	I	Sets the regulation voltage for output. Default value is 0.5 V
VTSB	E5	I	Voltage bias for temperature sense
$\overline{\text{WPG}}$	F5	O	Open-drain output that allows user to sense when power is transferred to load

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

	PIN	MIN	MAX	UNIT
Input voltage	AC1, AC2	–0.8	20	V
	RECT, COMM1, COMM2, OUT, , CLAMP1, CLAMP2, $\overline{WPG}$, $\overline{PD\_DET}$	–0.3	20	
	AD, $\overline{AD\text{-}EN}$	–0.3	30	
	BOOT1, BOOT2	–0.3	20	
	SCL, SDA, TERM, CM_ILIM, FOD, TS/CTRL, ILIM, TMEM, VTSB, VO_REG, LPRBEN	–0.3	7	
Input current	AC1, AC2 (RMS)	2.5		A
Output current	OUT	1.5		A
Output sink current	$\overline{WPG}$, $\overline{PD\_DET}$	15		mA
Output sink current	COMM1, COMM2	1.0		A
T_J, junction temperature		–40	150	°C

(1) All voltages are with respect to the PGND pin, unless otherwise noted.
(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD} [(1)]	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(2)], 100 pF, 1.5 kΩ	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(3)]	–500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{RECT}	RECT voltage	4.0	10.0	V
I_{OUT}	Output current		1.0	A
$I_{AD\text{-}EN}$	Sink current		1	mA
I_{COMM}	COMMx sink current		500	mA
T_J	Junction temperature	0	125	ºC

7.4 Thermal Information

THERMAL METRIC[1]		bq5102x	UNIT
		YFP (42 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	6.1	
ψ_{JT}	Junction-to-top characterization parameter[5]	1.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	6.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) , $I_{LOAD} = I_{OUT}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Undervoltage lockout	V_{RECT}: 0 to 3 V		2.8	2.9	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{RECT}: 3 to 2 V		393		mV
$V_{RECT-OVP}$	Input overvoltage threshold	V_{RECT}: 5 to 16 V	14.6	15.1	15.6	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{RECT}: 16 to 5 V		1.5		V
$V_{RECT(REG)}$	Voltage at RECT pin set by communication with primary		V_{OUT} + 0.120		V_{OUT} + 2.0	V
$V_{RECT(TRACK)}$	V_{RECT} regulation above V_{OUT}	V_{ILIM} = 1.2 V		140		mV
$I_{LOAD-HYS}$	I_{LOAD} hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		4		
$V_{RECT-DPM}$	Rectifier under voltage protection, restricts I_{OUT} at $V_{RECT-DPM}$		3	3.1	3.2	V
$V_{RECT-REV}$	Rectifier reverse voltage protection with a supply at the output	$V_{RECT-REV} = V_{OUT} – V_{RECT}$, V_{OUT} = 10 V		8.8	9.2	V
QUIESCENT CURRENT						
$I_{OUT(standby)}$	Quiescent current at the output when wireless power is disabled	V_{OUT} ≤ 5 V, 0°C ≤ T_J ≤ 85°C		20	35	µA
ILIM SHORT CIRCUIT						
$R_{ILIM-SHORT}$	Highest value of R_{ILIM} resistor considered a fault (short). Monitored for I_{OUT} > 100 mA	R_{ILIM}: 200 to 50 Ω. I_{OUT} latches off, cycle power to reset		209	235	Ω
$t_{DGL-Short}$	Deglitch time transition from ILIM short to I_{OUT} disable			1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the ILIM short comparator when I_{OUT} is greater than this value	I_{LOAD}: 0 to 200 mA	110	125	140	mA
$I_{LIM-SHORT,OK}$ HYSTERESIS	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{LOAD}: 200 to 0 mA		20		mA
I_{OUT-CL}	Maximum output current limit	Maximum I_{LOAD} that can be delivered for 1 ms when ILIM is shorted		3.7		A
OUTPUT						
V_{O_REG}	Feedback voltage set point	I_{LOAD} = 1000 mA	0.4950	0.5013	0.5075	V
		I_{LOAD} = 1 mA	0.4951	0.5014	0.5076	
K_{ILIM}	Current programming factor for hardware short circuit protection	$R_{ILIM} = K_{ILIM} / I_{ILIM}$, where I_{ILIM} is the hardware current limit I_{OUT} = 850 mA		842		AΩ
I_{OUT_RANGE}	Current limit programming range				1500	mA
I_{COMM}	Output current limit during communication	I_{OUT} ≥ 320 mA		I_{OUT} – 50		mA
		100 mA ≤ I_{OUT} < 320 mA		I_{OUT} + 50		
		I_{OUT} < 100 mA		200		
$t_{HOLD-OFF}$	Hold off time for the communication current limit during startup			1		s

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) , $I_{LOAD} = I_{OUT}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS/CTRL						
$V_{TS-Bias}$	TS bias voltage (internal)	$I_{TS-Bias}$ < 100 µA and communication is active (periodically driven, see $t_{TS/CTRL-Meas}$)		1.8		V
$V_{CTRL-HI}$	CTRL pin threshold for a high	$V_{TS/CTRL}$: 50 to 150 mV	90	105	120	mV
$T_{TS/CTRL-Meas}$	Time period of TS/CTRL measurements, when TS is being driven	TS bias voltage is only driven when power packets are sent			1700	ms
V_{TS-HOT}	Voltage at TS pin when device shuts down			0.38		V
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
OUTPUT LOGIC LEVELS ON $\overline{WPG}$						
V_{OL}	Open drain $\overline{WPG}$ pin	I_{SINK} = 5 mA			550	mV
$I_{OFF,STAT}$	$\overline{WPG}$ leakage current when disabled	V_{WPG} = 20 V			1	µA
COMM PIN						
$R_{DS-ON(COMM)}$	COMM1 and COMM2	V_{RECT} = 2.6 V		1.0		Ω
f_{COMM}	Signaling frequency on COMMx pin for WPC			2.00		Kb/s
$I_{OFF,COMM}$	COMMx pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V			1	µA
CLAMP PIN						
$R_{DS-ON(CLAMP)}$	CLAMP1 and CLAMP2			0.5		Ω
ADAPTER ENABLE						
V_{AD-EN}	V_{AD} rising threshold voltage	V_{AD} 0 V to 5 V	3.5	3.6	3.8	V
$V_{AD-EN-HYS}$	V_{AD-EN} hysteresis	V_{AD} 5 V to 0 V		450		mV
I_{AD}	Input leakage current	V_{RECT} = 0 V, V_{AD} = 5 V			50	µA
R_{AD_EN-OUT}	Pullup resistance from $\overline{AD-EN}$ to OUT when adapter mode is disabled and $V_{OUT} > V_{AD}$	V_{AD} = 0 V, V_{OUT} = 5 V		230	350	Ω
V_{AD_EN-ON}	Voltage difference between V_{AD} and V_{AD-EN} when adapter mode is enabled	V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C	4	4.5	5	V
		V_{AD} = 9 V, 0°C ≤ T_J ≤ 85°C	3	6	7	V
SYNCHRONOUS RECTIFIER						
$I_{SYNC-EN}$	I_{OUT} at which the synchronous rectifier enters half synchronous mode	I_{OUT}: 200 to 0 mA		100		mA
$I_{SYNC-EN-HYST}$	Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled)	I_{OUT} 0 to 200 mA		40		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA, and T_J = 25°C		0.7		V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) , $I_{LOAD} = I_{OUT}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C (ONLY FOR bq51021)						
V_{IL}	Input low threshold level SDA	V(PULLUP) = 1.8 V, SDA			0.4	V
V_{IH}	Input high threshold level SDA	V(PULLUP) = 1.8 V, SDA	1.4			V
V_{IL}	Input low threshold level SCL	V(PULLUP) = 1.8 V, SCL			0.4	V
V_{IH}	Input high threshold level SCL	V(PULLUP) = 1.8 V, SCL	1.4			V
I^2C speed		Typical		100		kHz

7.6 Typical Characteristics

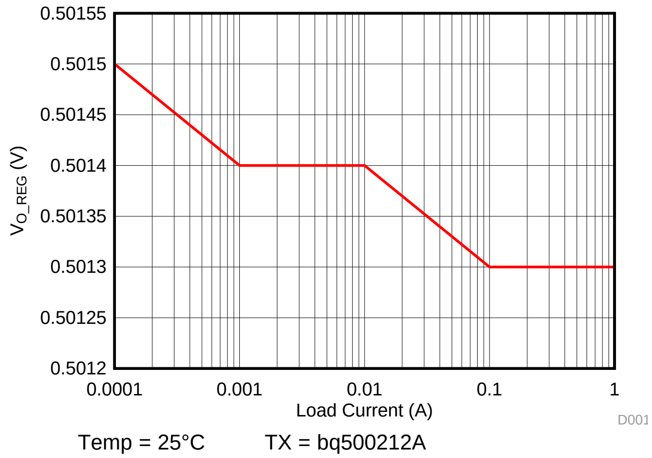


Figure 1. Output Regulation as a Function of Load

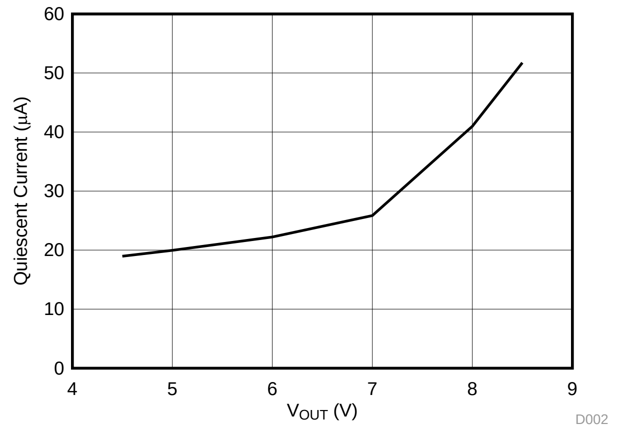


Figure 2. Quiescent Current as a Function of Output Voltage

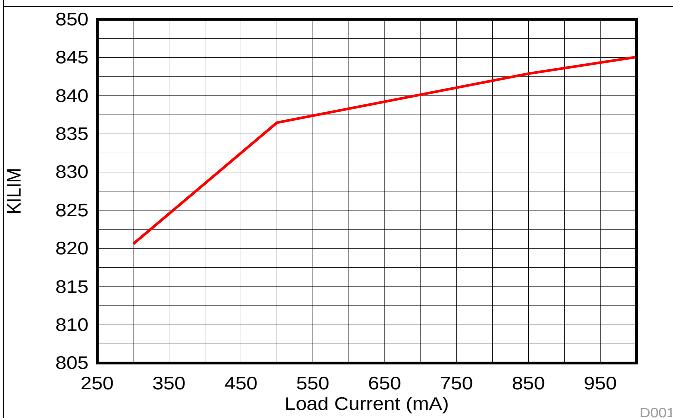


Figure 3. KILIM as a Function of Load Current

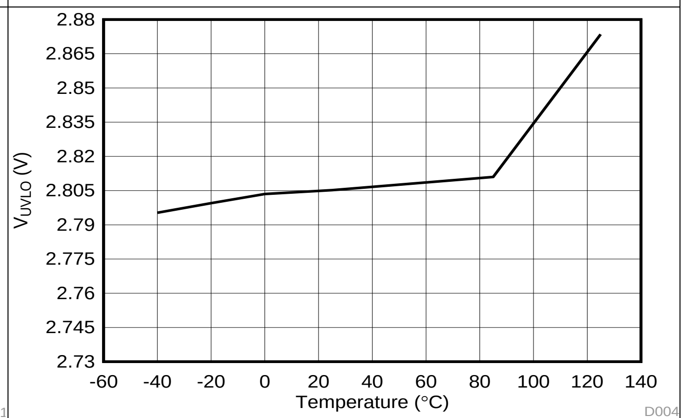


Figure 4. UVLO as a Function of Junction Temperature

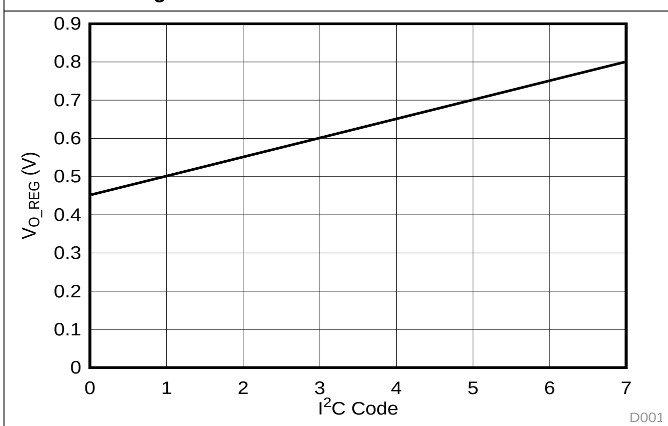


Figure 5. VO_REG by Different I²C Codes, 1-mA Load

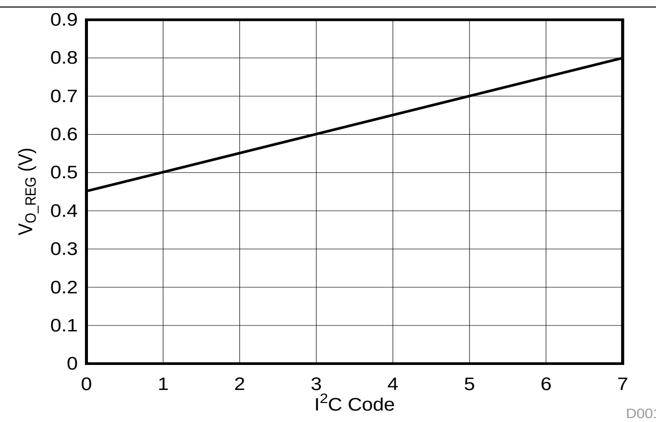


Figure 6. VO_REG by Different I²C Codes, 1-A Load

8 Detailed Description

8.1 Overview

WPC-based wireless power systems consist of a charging pad (primary, transmitter) and the secondary-side equipment (receiver). There are coils placed in the charging pad and secondary equipment, which magnetically couple to each other when the receiver is placed on the transmitter. Power is transferred from the primary to the secondary by transformer action between the coils. The receiver can achieve control over the amount of power transferred by requesting the transmitter to change the field strength by changing the frequency, or duty cycle, or voltage rail energizing the primary coil.

The receiver equipment communicates with the primary by modulating the load seen by the primary. This load modulation results in a change in the primary coil current or primary coil voltage, or both, which is measured and demodulated by the transmitter.

A WPC system communication is digital — packets are transferred from the secondary to the primary. Differential bi-phase encoding is used for the packets. The bit rate is 2 kb/s. Various types of communication packets are defined. These include identification and authentication packets, error packets, control packets, power usage packets, and end power transfer packets, among others.

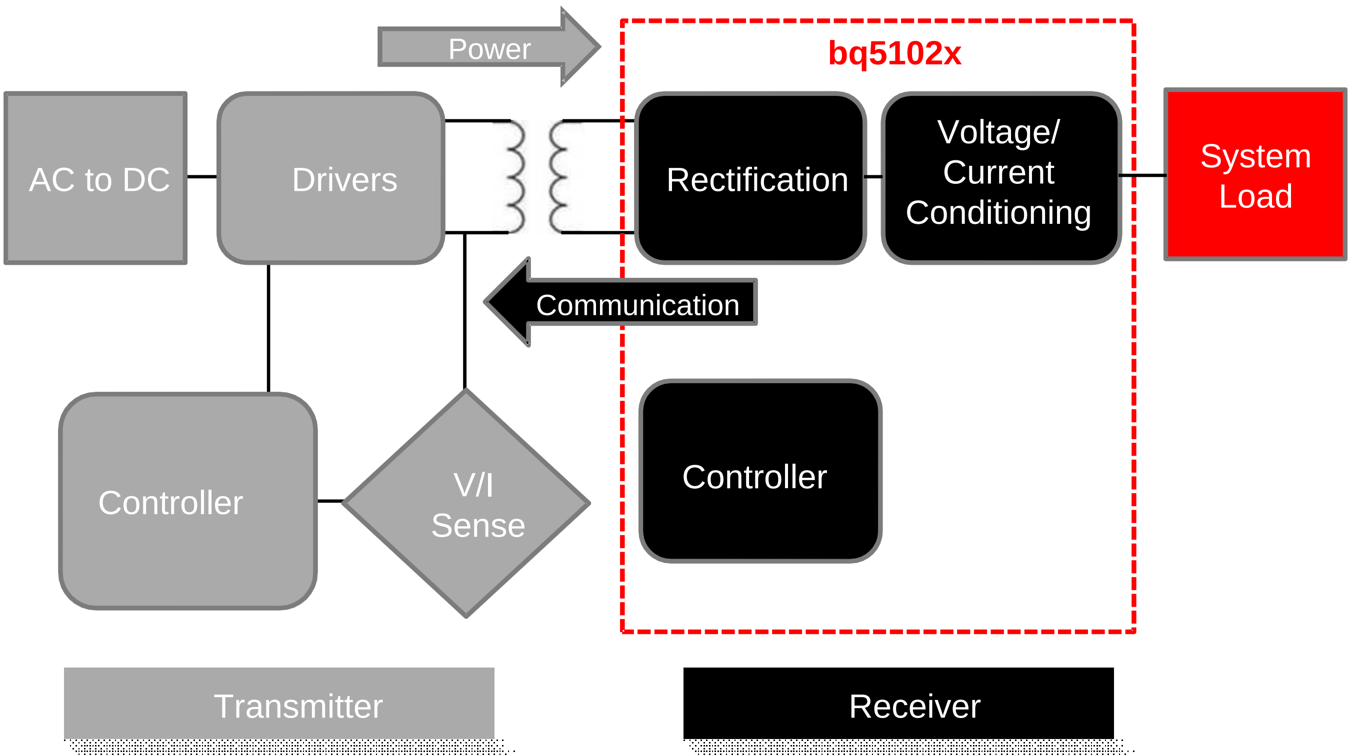


Figure 7. Dual Mode Wireless Power System Indicating the Functional Integration of the bq5102x Family

The bq5102x device integrates fully-compliant WPC v1.1 communication protocol in order to streamline the wireless power receiver designs (no extra software development required). Other unique algorithms such as *Dynamic Rectifier Control* are integrated to provide best-in-class system efficiency while keeping the smallest solution size of the industry.

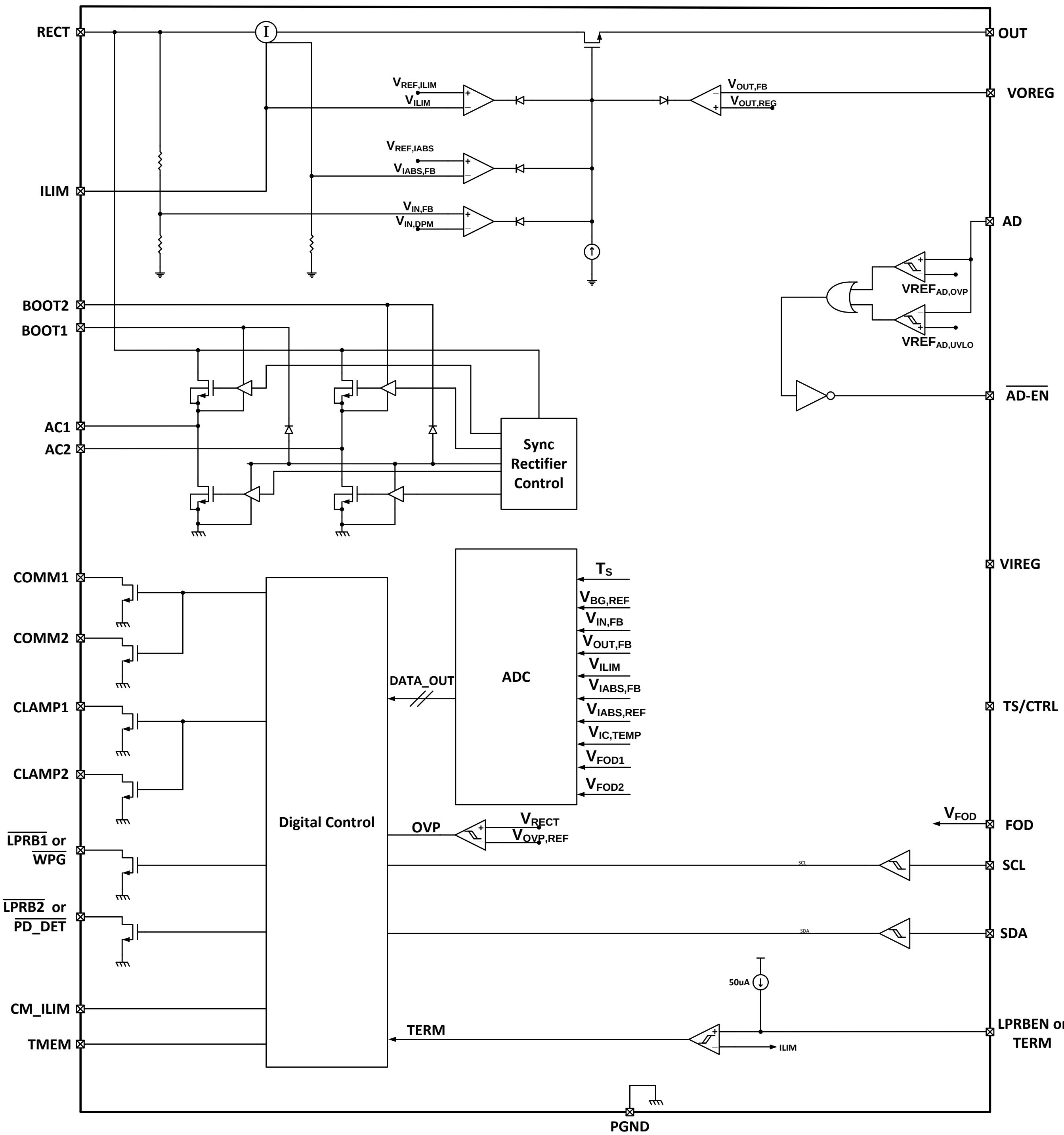
As a WPC system, when the receiver (shown in Figure 7) is placed on the charging pad, the secondary coil couples to the magnetic flux generated by the coil in the transmitter, which consequently induces a voltage in the secondary coil. The internal synchronous rectifier feeds this voltage to the RECT pin, which in turn feeds the LDO which feeds the output.

Overview (continued)

The bq5102x device identifies itself to the primary using the COMMx pins, switching on and off the COMM FETs, and hence switching in and out COMM capacitors. If the authentication is successful, the primary remains powered-up. The bq5102x device measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT(REG)}$, and sends back error packets to the transmitter. This process goes on until the input voltage settles at $V_{RECT(REG)\ MAX}$. During a load change, the dynamic rectifier algorithm sets the targets specified by targets between $V_{RECT(REG)\ MAX}$ and $V_{RECT(REG)\ MIN}$ shown in Table 1. This algorithm enhances the transient response of the power supply while still allowing for very high efficiency at high loads.

After the voltage at the RECT pin is at the desired value, an internal pass FET (LDO) is enabled. The voltage control loop ensures that the output voltage is maintained at $V_{OUT(REG)}$, powering the downstream charger. The bq5102x device meanwhile continues to monitor the RECT voltage, and keeps sending control error packets (CEP) to the primary on average every 250 ms. If a large transient occurs, the feedback to the primary speeds up to 32-ms communication periods to converge on an operating point in less time.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Rectifier Control

The *Dynamic Rectifier Control* algorithm offers the end-system designer optimal transient response for a given maximum output current setting. This is achieved by providing enough voltage headroom across the internal regulator (LDO) at light loads in order to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take up to 150 ms to converge on a new rectifier voltage target. Therefore, a transient response is dependent on the loosely coupled transformer's output impedance profile. The *Dynamic Rectifier Control* allows for a 1.5-V change in rectified voltage before the transient response is observed at the output of the internal regulator (output of the bq5102x device). A 1-A application allows up to a 2-Ω output impedance. The *Dynamic Rectifier Control* behavior is illustrated in Figure 12.

8.3.2 Dynamic Power Scaling

The *Dynamic Power Scaling* feature allows for the loss characteristics of the bq5102x device to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the K_{ILIM} term and the R_{ILIM} resistance (where R_{ILIM} = K_{ILIM} / I_{ILIM}). The flow diagram in Figure 12 shows how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the I_{ILIM} setting. Table 1 summarizes how the rectifier behavior is dynamically adjusted based on two different R_{ILIM} settings. Table 1 shows I_{MAX}, which is typically lower than I_{ILIM} (about 20% lower). See section *RILIM Calculations* about setting the ILIM resistor for more details.

Table 1. Dynamic Rectifier Regulation

Output Current Percentage	R_{ILIM} = 1400 Ω I_{MAX} = 0.5 A	R_{ILIM} = 700 Ω I_{MAX} = 1.0 A	V_{RECT}
0 to 10%	0 to 0.05 A	0 to 0.1 A	V_{OUT} + 2.0
10 to 20%	0.05 to 0.1 A	0.1 to 0.2 A	V_{OUT} + 1.68
20 to 40%	0.1 to 0.2 A	0.2 to 0.4 A	V_{OUT} + 0.56
> 40%	> 0.2 A	> 0.4 A	V_{OUT} + 0.12

Table 1 shows the shift in the *Dynamic Rectifier Control* behavior based on the two different R_{ILIM} settings. With the rectifier voltage (V_{RECT}) as the input to the internal LDO, this adjustment in the *Dynamic Rectifier Control* thresholds dynamically adjusts the power dissipation across the LDO where,

$$P_{DIS} = (V_{RECT} - V_{OUT}) \cdot I_{OUT} \quad (1)$$

Figure 21 shows how the system efficiency is improved due to the *Dynamic Power Scaling* feature. Note that this feature balances efficiency with optimal system transient response.

8.3.3 VO_REG Calculations

The bq5102x device allows the designer to set the output voltage by setting a feedback resistor divider network from the OUT pin to the VO_REG pin, as seen in Figure 8. The resistor divider network should be chosen so that the voltage at the VO_REG pin is 0.5 V at the desired output voltage. For the device bq51021 which has I^2C enabled, this applies to the default I^2C code for VO_REG shown in I^2C register in Figure 8.

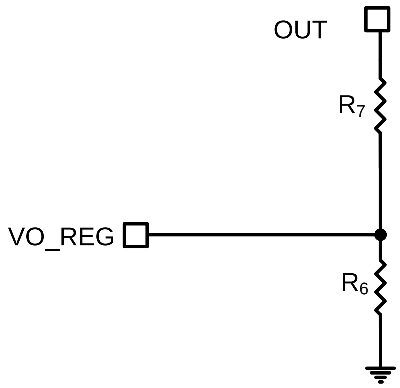


Figure 8. VO_REG Network

Choose the desired output voltage V_{OUT} and R_6:

$$K_{VO} = \frac{0.5\ V}{V_{OUT}} \tag{2}$$

$$R_6 = \frac{K_{VO} \times R_7}{1 - K_{VO}} \tag{3}$$

8.3.4 RILIM Calculations

The bq5102x device includes a means of providing hardware overcurrent protection (I_{ILIM}) through an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (for example, current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = K_{ILIM} / I_{ILIM} \tag{4}$$

$$R_1 = R_{ILIM} - R_{FOD} \tag{5}$$

R_{ILIM} allows for the ILIM pin to reach 1.2 V at an output current equal to I_{ILIM}. When choosing R_{ILIM}, two options are possible.

If the user's application requires an output current equal to or greater than the external I_{ILIM} that the circuit is designed for (input current limit on the charger where the receiver device is tied higher than the external I_{ILIM}), ensure that the downstream charger is capable of regulating the voltage of the input into which the receiver device output is tied to by lowering the amount of current being drawn. This ensures that the receiver output does not drop to 0. Such behavior is referred to as VIN DPM in TI chargers. Unless such behavior is enabled on the charger, the charger will pull the output of the receiver device to ground when the receiver device enters current regulation. If the user's applications are designed to extract less than the I_{ILIM} (1-A maximum), typical designs should leave a design margin of at least 10%, so that the voltage at ILIM pin reaches 1.2 V when 10% more than maximum current is drawn from the output. Such a design would have input current limit on the charger lower than the external ILIM of the receiver device. In both cases, the charger must be capable of regulating the current drawn from the device to allow the output voltage to stay at a reasonable value. This same behavior is also necessary during the WPC communication. The following calculations show how such a design is achieved:

$$R_{ILIM} = K_{ILIM} / (1.1 \times I_{ILIM}) \tag{6}$$

$$R_1 = R_{ILIM} - R_{FOD}$$

where I_{LIM} is the hardware current limit (7)

When referring to the application diagram shown in *Typical Applications*, R_{ILIM} is the sum of the R_1 and R_{FOD} resistance (that is, the total resistance from the ILIM pin to GND). R_{FOD} is chosen according to the application. The tool for calculating R_{FOD} can be obtained by contacting your TI representative. Use R_{FOD} to allow the receiver implementation to comply with WPC v1.1 requirements related to received power accuracy. For the device bq51021 which has I^2C enabled, this applies to the default I^2C code for IO_REG (100%) shown in I^2C register in Figure 8.

8.3.5 Adapter Enable Functionality

The bq5102x device can also help manage the multiplexing of adapter power to the output and can turn off the TX when the adapter is plugged in and is above the $V_{AD\text{-}EN}$. After the adapter is plugged in and the output turns off, the RX device sends an EOC to the TX. In this case, the $\overline{AD\_EN}$ pins are then pulled to approximately 4 V below AD, which allows the device turn on the back-to-back PMOS connected between AD and OUT (Figure 28).

Both the AD and $\overline{AD\text{-}EN}$ pins are rated at 30 V, while the OUT pin is rated at 20 V. It must also be noted that it is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled, no load can be pulled from the RECT pin as this could cause an internal device overvoltage in the bq5102x device.

For the device bq51021, the wired power will always take priority over wireless power, and thus when the adapter is plugged in, the device will first send an EPT to the TX and then will send allow for up to 30 ms after disabling the output allowing the $\overline{WPG}$ to go high impedance. It will then allow the wired power to be delivered to the output by pulling the $\overline{AD\_EN}$ below the AD pin to allow the adapter power to be passed on the output.

For the device bq51020, the EN1 and EN2 pins will determine the preference of wired or wireless power. Table 2 shows the EN1 and EN2 state and the corresponding device selection.

Table 2. Adapter Functionality EN1 and EN2

EN1	EN2	Adapter Insert	$\overline{AD\_EN}$	EPT Message	Preference
0	0	5 V	V_{AD} – 4 V	EPT 0x00	Wired preference
0	1	5 V	V_{OUT} / V_{AD}	No EPT	Wireless preference
1	0	5 V	V_{AD} – 4 V	EPT 0x00	Wired preference (1)
1	1	5 V	V_{OUT} / V_{AD}	EPT 0x00	Neither wired nor wireless (1)

(1) Only valid when wireless power is present.

8.3.6 Turning Off the Transmitter

WPC v1.1 specification allows the receiver to turn off the transmitter and put the system in a low-power standby mode. There are two different ways to accomplish this with the bq5102x device. The first method is by using the TS/CTRL pin. By pulling the pin high or low, EPT can be sent to the transmitter.

Pulling the TS/CTRL pin high will send EPT (code 0x01), which corresponds to charge complete. The transmitter will then respond to this EPT code as per the transmitter's design. After this EPT code is sent, some transmitters will then periodically check to make sure that the receiver is not looking for a refresh charge on the battery. The period of how often the transmitter checks varies based on the transmitter design. The transmitter will use the digital ping or a shortened version of it to check the receiver status. It is this energy on the digital ping that the receiver uses to indicate whether it is still sitting on the transmitter surface by storing the energy from the digital ping on the capacitor attached to the TMEM pin. The cap voltage (determined by the periodicity of the digital ping and the bleed off resistor attached in parallel to the TMEM cap) determine when the receiver indicates that it is no longer on the surface of the transmitter by allowing the $\overline{PD\_DET}$ pin to go high impedance.

The TS/CTRL pin can also be pulled low. This will allow the receiver to determine that the host processor would like to shut down the transmitter because of thermal reasons. Therefore, the receiver will send EPT (code 0x03) indicating an overtemperature event.

8.3.6.1 End Power Transfer (EPT)

The WPC allows for a special command to terminate power transfer from the TX termed EPT packet. The v1.1 specifies the following reasons and their responding data field value in Table 3.

Table 3. End Power Transfer Codes in WPC

Reason	Value	Condition (1)
Unknown	0x00	AD > 3.6 V
Charge complete	0x01	TS/CTRL > 1.4V

(1) The *Condition* column corresponds to the case where the bq5102x device will send the WPC EPT command.

Table 3. End Power Transfer Codes in WPC (continued)

Reason	Value	Condition (1)
Internal fault	0x02	T_J > 150°C or R_{ILIM} < 100 Ω
Over temperature	0x03	TS < V_{HOT}, or TS/CTRL < 100 mV
Over voltage	0x04	V_{RECT} target does not converge and stays higher or lower than target
Battery failure	0x06	Not sent
Reconfigure	0x07	Not sent
No response	0x08	Not sent

8.3.7 Communication Current Limit

Communication current limit is a feature that allows for error free communication to happen between the RX and TX in the WPC mode. This is done by decoupling the coil from the load transients by limiting the output current during communication with the TX. The communication current limit is set according to the Table 4. The communication current limit can be disabled by pulling CM_ILIM pin high (> 1.4 V) or enabled by pulling the CM_ILIM pin low. There is an internal pulldown that enables communication current limit when the CM_ILIM pin is left floating.

Table 4. Communication Current Limit

I_{OUT}	Communication Current Limit
0 mA < I_{OUT} < 100 mA	None
100 mA < I_{OUT} < 320 mA	I_{OUT} + 50 mA
320 mA < I_{OUT} < Max current	I_{OUT} – 50 mA

When the communication current limit is enabled, the amount of current that the load can draw is limited. If the charger in the system does not have a VIN-DPM feature, the output of the receiver will collapse if communication current limit is enabled. To disable communication current limit, pull CM_ILIM pin high.

8.3.8 $\overline{\text{PD\_DET}}$ and TMEM

$\overline{\text{PD\_DET}}$ is an open-drain pin that goes low based on the voltage of the TMEM pin. When the voltage of TMEM is higher than 1.6 V, $\overline{\text{PD\_DET}}$ will be low. The voltage on the TMEM pin depends on capturing the energy from the digital ping from the transmitter and storing it on the C_5 capacitor in Figure 9. After the receiver sends an EPT (charge complete), the transmitter shuts down and goes into a low-power mode. After this EPT code is sent, some transmitters will then periodically check to make sure that the receiver is not looking for a refresh charge on the battery. The period of how often the transmitter checks varies based on the transmitter design. The transmitter will use the digital ping or a shortened version of it to check the receiver status. It is this energy on the digital ping that the receiver uses to indicate whether it is still sitting on the transmitter surface by storing the energy from the digital ping on the capacitor attached to the TMEM pin. The cap voltage (determined by the periodicity of the digital ping and the bleed off resistor attached in parallel to the TMEM cap) determine when the receiver indicates that it is no longer on the surface of the transmitter by allowing the $\overline{\text{PD\_DET}}$ pin to go high impedance. The energy from the digital ping can be stored on the TMEM pin until the next digital ping refreshes the capacitor. A bleedoff resistor R_{MEM}can be chosen in parallel with C_5 that sets the time constant so that the TMEM pin will fall below 1.6 V once the next ping timer expires. The duration between digital pings is indeterminate and depends on each transmitter manufacturer.

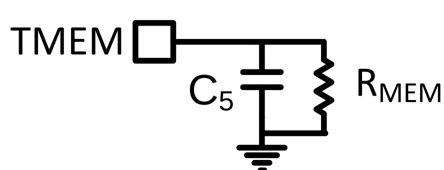


Figure 9. TMEM Configuration

Set capacitor on C_5 = TMEM to 2.2 µF. Resistor R_{MEM} across C_5 can be set by understanding the duration between digital pings (tping). Set the resistor such that:

$$R_{MEM} = \frac{tping}{4 \times C_5} \quad (8)$$

$\overline{PD\_DET}$ typically requires a pullup resistor to an external source. The choice of the pullup resistor determines load regulation; the suggested values for the pullup resistor are between 5.6 and 100 kΩ. The higher values offer better load regulation.

8.3.9 TS/CTRL

The bq5102x device includes a ratio metric external temperature sense function. The temperature sense function has a low ratio metric threshold which represents a hot condition. TI recommends an external temperature sensor in order to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (for example, place the negative temperature coefficient (NTC) resistor closest to the user touch point on the back cover). A resistor in series or parallel can be inserted to adjust the NTC to match the trip point of the device. The implementation in Figure 10 shows the series-parallel resistor implementation for setting the threshold at which $V_{TS\text{-}HOT}$ is reached. Once the $V_{TS\text{-}HOT}$ threshold is reached, the device will send an EPT – overtemperature signal for a WPC transmitter.

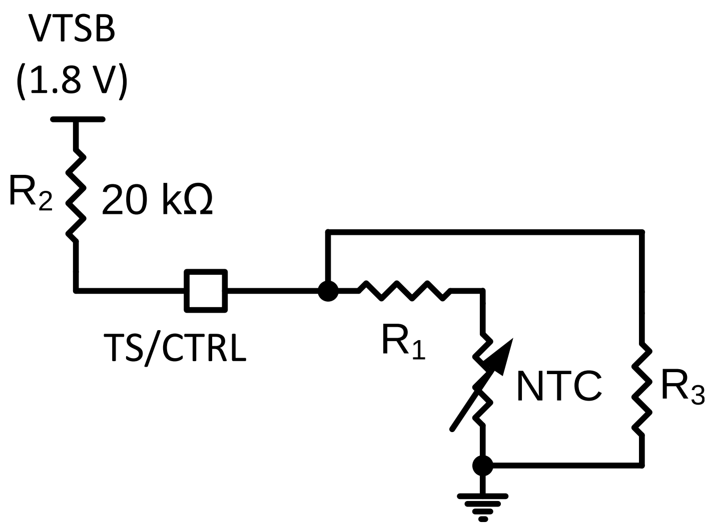


Figure 10. NTC Resistor Setup

Figure 10 shows a parallel resistor setup that can be used to adjust the trip point of $V_{TS\text{-}HOT}$. $T_{S\text{-}HOT}$ is VS. After the NTC is chosen and R_{NTCHOT} at $V_{TS\text{-}HOT}$ is determined from the data sheet of the NTC, Equation 9 can be used to calculate R_1 and R_3. In many cases depending on the NTC resistor, R_1 or R_3 can be omitted. To omit R_1, set R_1 to 0, and to omit R_3, set R_3 to 10 MΩ.

$$T_{S-HOT} = 1.8\ V \times \frac{(R_{NTCHOT} + R_1) \times R_3 \div ((R_{NTCHOT} + R_1) + R_3)}{(R_{NTCHOT} + R_1) \times R_3 \div ((R_{NTCHOT} + R_1) + R_3) + R_2} \quad (9)$$

8.3.10 I²C Communication

Only bq51021

The bq5102x device allows for I²C communication with the internal CPU. In case the I²C is not used, ground SCL and SDA. See *Register Maps* for more information.

8.3.11 Input Overvoltage

If the input voltage suddenly increases in potential for some condition (for example, a change in position of the equipment on the charging pad), the voltage-control loop inside the bq5102x device becomes active, and prevents the output from going beyond $V_{OUT(REG)}$. The receiver then starts sending back error packets every 30 ms until the input voltage comes back to an acceptable level, and then maintains the error communication every 250 ms.

If the input voltage increases in potential beyond $V_{RECT\text{-}OVP}$, the device switches off the LDO and informs the primary to bring the voltage back to $V_{RECT(REG)}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the device from voltages beyond the maximum rating of the device.

8.4 Device Functional Modes

At startup operation, the bq5102x device must comply with proper handshaking to be granted a power contract from the WPC transmitter. The transmitter initiates the handshake by providing an extended digital ping after analog ping detects an object on the transmitter surface. If a receiver is present on the transmitter surface, the receiver then provides the signal strength, configuration, and identification packets to the transmitter (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the transmitter. The only exception is if there is a true shutdown condition on the AD, or TS/CTRL pins where the receiver shuts down the transmitter immediately. See Table 3 for details. After the transmitter has successfully received the signal strength, configuration, and identification packets, the receiver is granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq5102x device *Dynamic Rectifier Control* algorithm, the receiver will inform the transmitter to adjust the rectifier voltage approximately 8V prior to enabling the output supply. This method enhances the transient performance during system startup. For the startup flow diagram details, see Figure 11.

Device Functional Modes (continued)

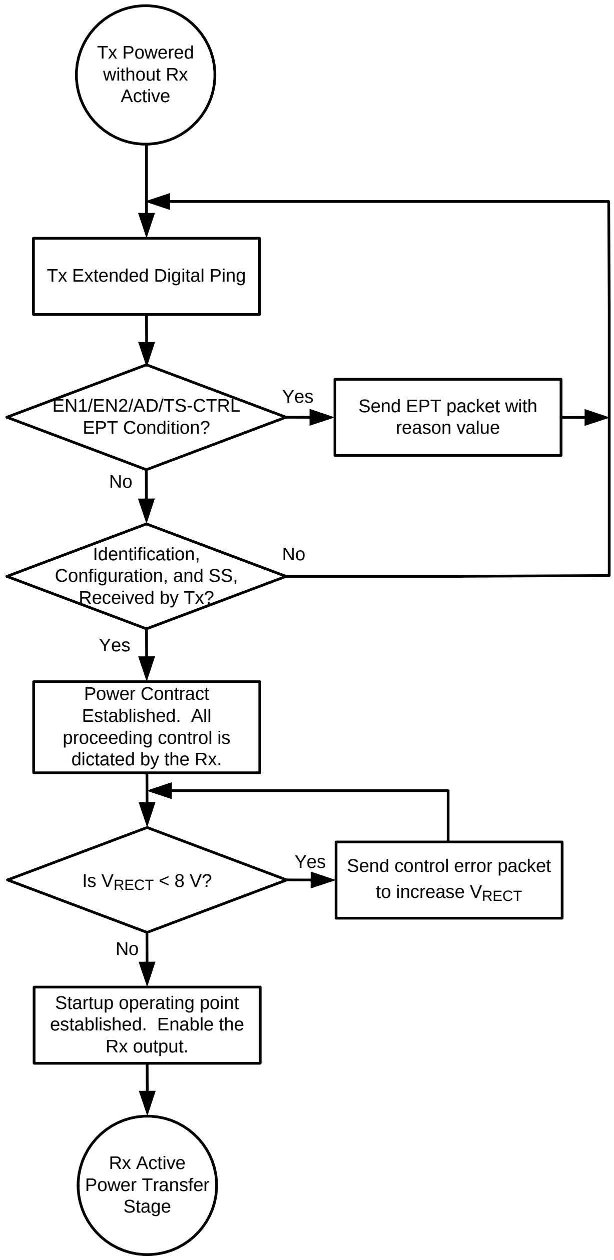


Figure 11. Wireless Power Startup Flow Diagram on WPC TX

After the startup procedure is established, the receiver will enter the active power transfer stage. This is considered the main loop of operation. The *Dynamic Rectifier Control* algorithm determines the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{ILIM} and the R_{ILIM}). The receiver will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target dynamically changes. As a note, the feedback loop of the WPC system is relatively slow, it can take up to 150 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the receiver coil output impedance at that operating point. The main loop also determines if any conditions in Table 3 are true in order to discontinue power transfer. Figure 12 shows the active power transfer loop.

Device Functional Modes (continued)

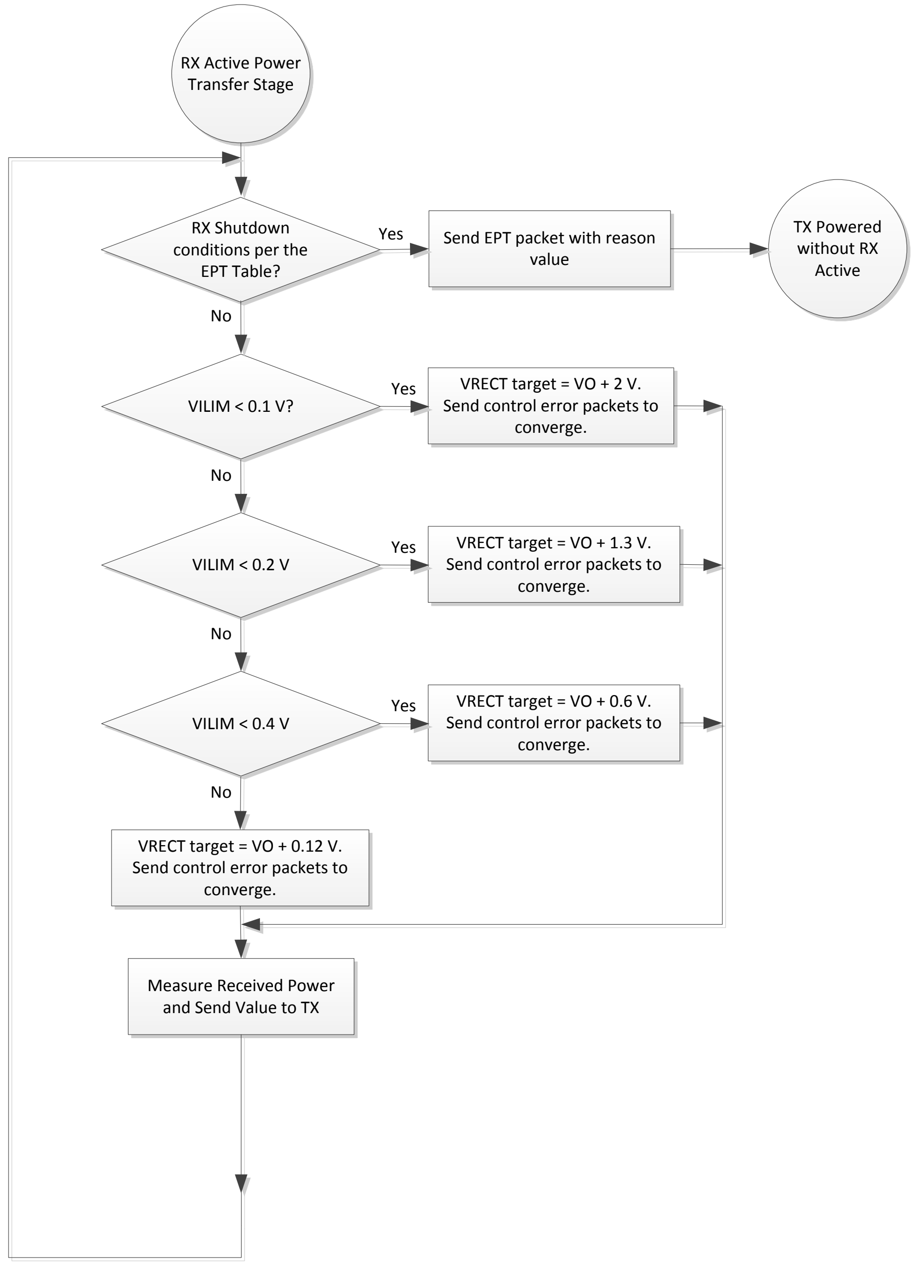


Figure 12. Active Power Transfer Flow Diagram on WPC

8.5 Register Maps

Locations 0x01 and 0x02 can be written to any time. Locations 0xE0 to 0xFF are only functional when $V_{RECT} > V_{UVLO}$. When V_{RECT} goes below V_{UVLO}, locations 0xE0 to 0xFF are reset.

Table 5. Wireless Power Supply Current Register 1 (READ / WRITE)

Memory Location: 0x01, Default State: 00000001			
BIT	NAME	READ / WRITE	FUNCTION
B7 (MSB)		Read / Write	Not used
B6		Read / Write	Not used
B5		Read / Write	Not used
B4		Read / Write	Not used
B3		Read / Write	Not used
B2	V_{OREG2}	Read / Write	450, 500, 550, 600, 650, 700, 750, or 800 mV Changes VO_REG target Default value 001
B1	V_{OREG1}	Read / Write	
B0	V_{OREG0}	Read / Write	

Table 6. Wireless Power Supply Current Register 2 (READ / WRITE)

Memory Location: 0x02, Default State: 00000111			
BIT	NAME	READ / WRITE	FUNCTION
B7 (MSB)	JEITA	Read / Write	Not used
B6		Read / Write	Not used
B5	I_{TERM2}	Read / Write	Not used for bq5102x
B4	I_{TERM1}	Read / Write	
B3	I_{TERM0}	Read / Write	
B2	I_{OREG2}	Read / Write	10%, 20%, 30%, 40%, 50%, 60%, 90%, and 100% of I_{ILIM} current based on configuration 000, 001, …111
B1	I_{OREG1}	Read / Write	
B0	I_{OREG0}	Read / Write	

Table 7. I²C Mailbox Register (READ / WRITE)

Memory Location: 0xE0, Reset State: 10000000			
BIT	NAME	READ / WRITE	FUNCTION
B7	USER_PKT_DONE	Read	Set bit to 0 to send proprietary packet with header in 0xE2. CPU checks header to pick relevant payload from 0xF1 to 0xF4 This bit will be set to 1 after the user packet with the header in register 0xE2 is sent.
B6	USER_PKT_ERR	Read	00 = No error in sending packet 01 = Error: no transmitter present 10 = Illegal header found (packet will not be sent) 11 = Error: not defined yet
B5			
B4	FOD Mailer	Read / Write	Not used
B3	ALIGN Mailer	Read / Write	Setting this bit to 1 will enable alignment aid mode where the CEP = 0 will be sent until this bit is set to 0 (or CPU reset occurs) – see register 0xED
B2	FOD Scaler	Read / Write	Not used
B1	Reserved	Read / Write	
B0	Reserved	Read / Write	

Table 8. Wireless Power Supply FOD RAM (READ / WRITE)

Memory Location: 0xE1, Reset State: 00000000 (1)				
BIT	NAME	READ / WRITE	FUNCTION	
B7 (MSB)	ESR_ENABLE	Read / Write	Enables I^2C based ESR in received power, Enable = 1, Disable = 0	
B6	OFF_ENABLE	Read / Write	Enables I^2C based offset power, Enable = 1, Disable = 0	
B5	Ro_{FOD5}	Read / Write	000 – 0 mW 001 – +39 mW 010 – +78 mW 011 – +117 mW 100 – +156 mW	101 – +195 mW 110 – +234 mW 111 – +273 mW The value is added to received power message
B4	Ro_{FOD4}	Read / Write		
B3	Ro_{FOD3}	Read / Write		
B2	Rs_{FOD2}	Read / Write	000 – ESR 001 – ESR 010 – ESR × 2 011 – ESR × 3 100 – ESR × 4	101 – Not used 110 – Not used 111 – ESR/2
B1	Rs_{FOD1}	Read / Write		
B0	Rs_{FOD0}	Read / Write		

(1) A non-zero value will change the I^2R calculation resistor and offset in the received power calculation by a factor shown in the table.

Table 9. Wireless Power User Header RAM (WRITE)

Memory Location: 0xE2, Reset State: 00000000 (1)	
BIT	READ / WRITE
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

(1) Must write a valid header to enable proprietary package. As soon as mailer (0xE0) is written, payload bytes are sent on the next available communication slot as determined by CPU. After payload is sent, the mailer (USER_PKT_DONE) is set to 1.

Table 10. Wireless Power USER V_{RECT} Status RAM (READ)(1)

Memory Location: 0xE3, Reset State: 00000000 Range – 0 to 12 V This register reads back the V_{RECT} voltage with LSB = 46 mV			
BIT	NAME	READ / WRITE	FUNCTION
B7 (MSB)	V_{RECT7}	Read	LSB = 46 mV
B6	V_{RECT6}	Read	
B5	V_{RECT5}	Read	
B4	V_{RECT4}	Read	
B3	V_{RECT3}	Read	
B2	V_{RECT2}	Read	
B1	V_{RECT1}	Read	
B0	V_{RECT0}	Read	

(1) V_{RECT} is above UVLO.

Table 11. Wireless Power V_{OUT} Status RAM (READ)(1)

Memory Location: 0xE4, Reset State: 00000000 This register reads back the V_{OUT} voltage with LSB = 46 mV			
BIT	**NAME**	**Read / Write**	**FUNCTION**
B7 (MSB)	VOUT7	Read / Write	LSB = 46 mV
B6	VOUT6	Read / Write	
B5	VOUT5	Read / Write	
B4	VOUT4	Read / Write	
B3	VOUT3	Read / Write	
B2	VOUT2	Read / Write	
B1	VOUT1	Read / Write	
B0	VOUT0	Read / Write	

(1) Ouput is enabled.

Table 12. Wireless Power REC PWR Most Significant Byte Status RAM (READ)

Memory Location: 0xE8, Reset State: 00000000 This register reads back the received power with LSB = 39 mW	
BIT	**Read / Write**
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

Table 13. Wireless Power Prop Packet Payload RAM Byte 0 (WRITE)

Memory Location: 0xF1, Reset State: 00000000	
BIT	**Read / Write**
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

Table 14. Wireless Power Prop Packet Payload RAM Byte 1 (WRITE)

Memory Location: 0xF2, Reset State: 00000000	
BIT	**Read / Write**
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write

Table 14. Wireless Power Prop Packet Payload RAM Byte 1 (WRITE) (continued)

Memory Location: 0xF2, Reset State: 00000000	
BIT	**Read / Write**
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

Table 15. Wireless Power Prop Packet Payload RAM Byte 2 (WRITE)

Memory Location: 0xF3, Reset State: 00000000	
BIT	**Read / Write**
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

Table 16. Wireless Power Prop Packet Payload RAM Byte 3 (WRITE)

Memory Location: 0xF4, Reset State: 00000000	
BIT	**Read / Write**
B7 (MSB)	Read / Write
B6	Read / Write
B5	Read / Write
B4	Read / Write
B3	Read / Write
B2	Read / Write
B1	Read / Write
B0	Read / Write

9 Applications and Implementation

9.1 Application Information

The bq5102x device complies with the WPC v1.1 standard. There are several tools available for the design of the system. These tools may be obtained by checking the product page at www.ti.com. The following sections detail how to design a WPC v1.1 mode RX system.

9.2 Typical Applications

9.2.1 WPC Power Supply 5-V Output With 1-A Maximum Current and I²C

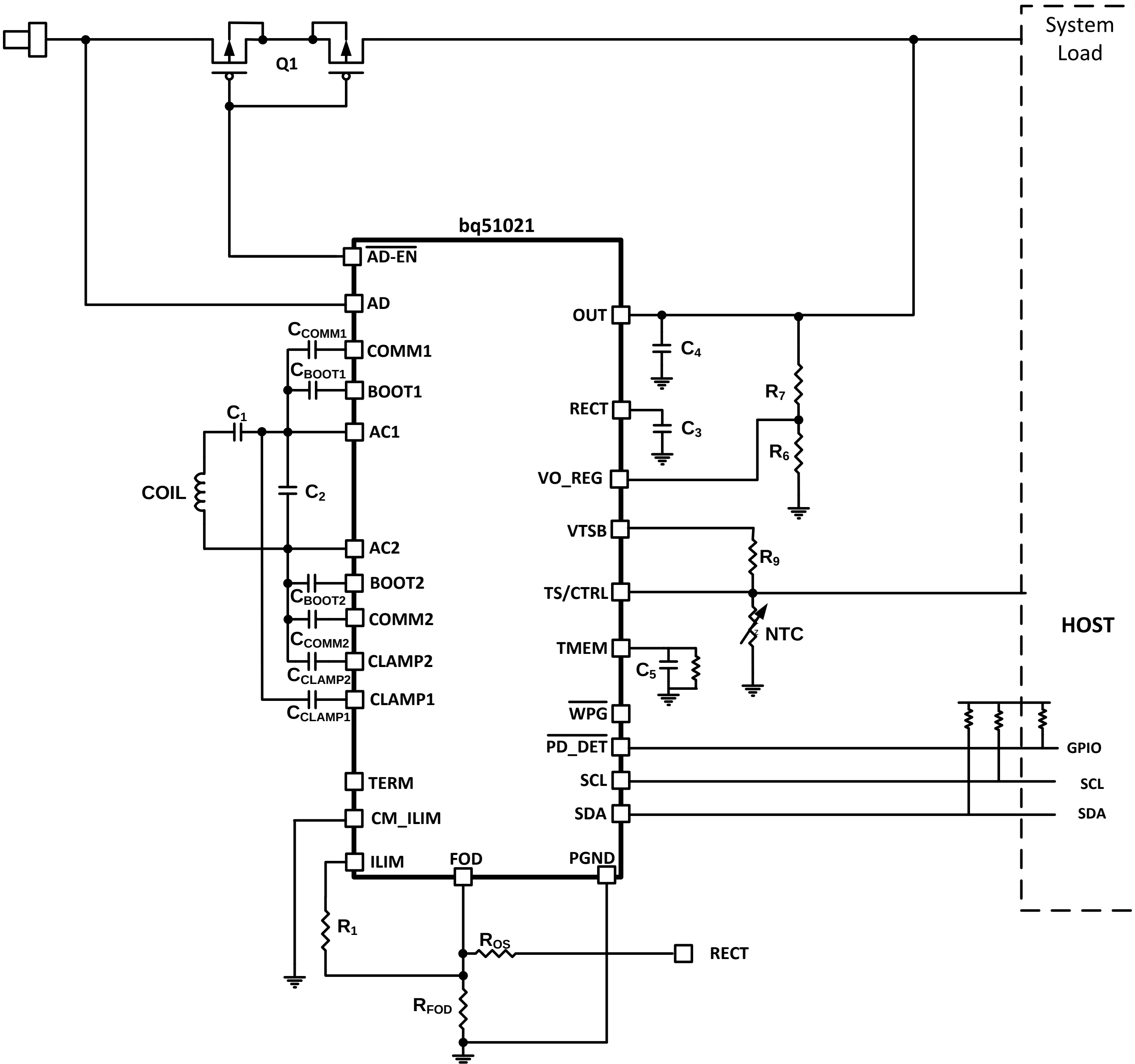


Figure 13. WPC 5-W Schematic Using bq5102x

Typical Applications (continued)

9.2.1.1 Design Requirements

Table 17. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{OUT}	5 V
I_{OUT} MAXIMUM	1 A
MODE	WPC v1.1

9.2.1.2 Detailed Design Procedure

To begin the design procedure, start by determining the following:

- Mode of operation – in this case WPC v1.1
- Output voltage
- Maximum output current

9.2.1.2.1 Output Voltage Set Point

The output voltage of the bq5102x device can be set by adjusting a feedback resistor divider network. The resistor divider network is used to set the voltage gain at the VO_REG pin. The device is intended to operate where the voltage at the VO_REG pin is set to 0.5 V. This value is the default setting and can be changed through I^2C (for the device bq51021). In Figure 14, R_6 and R_7 are the feedback network for the output voltage sense.

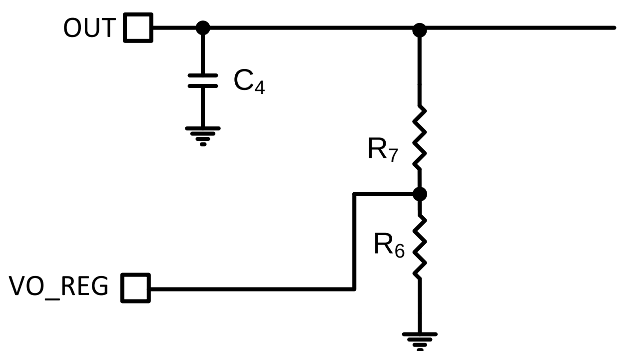


Figure 14. Voltage Gain for Feedback

$$K_{VO} = \frac{0.5\ V}{V_{OUT}} \tag{10}$$

$$R_6 = \frac{K_{VO} \times R_7}{1 - K_{VO}} \tag{11}$$

Choose R_7 to be a standard value. In this case, take care to choose R_6 and R_7 to be large values in order to avoid dissipating excessive power in the resistors, and thereby lowering efficiency.

K_{VO} is set to be 0.5 / 5 = 0.1, choose R_7 to be 102 kΩ, and thus R_6 to be 11.3 kΩ.

9.2.1.2.2 Output and Rectifier Capacitors

Set C_4 between 1 and 4.7 µF. This example uses 1 µF.

Set C_3 between 4.7 and 22 µF. This example uses 20 µF.

9.2.1.2.2.1 TMEM

Set C_5 to 2.2 µF. In order to determine the bleed off resistor, the WPC transmitters for which the $\overline{PD\_DET}$ is being set for needs to be determined. After the ping timing (time between two consecutive digital pings after EPT charge complete is sent) is determined, the bleedoff resistor can be determined. This example uses TI transmitter EVMs for the use case. In this case, the time between pings is 5 s. To set the time constant using the Equation 8, it is set to 5600 kΩ.

9.2.1.2.3 Maximum Output Current Set Point

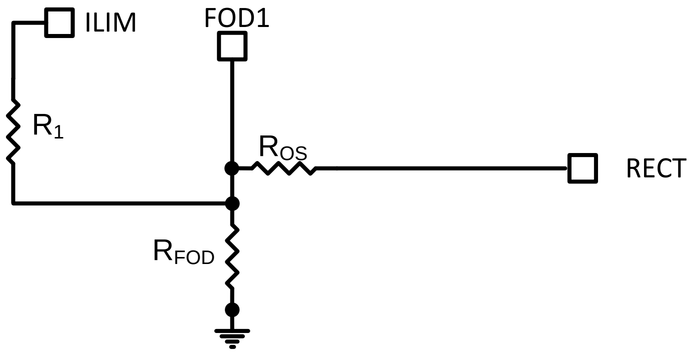


Figure 15. Current Limit Setting for bq5102x

The bq5102x device includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides a level of safety by clamping the maximum allowable output current (for example, a current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{ILIM}} \quad (12)$$

$$R_1 = R_{ILIM} - R_{FOD} \quad (13)$$

The R_{ILIM} will allow for the ILIM pin to reach 1.2 V at an output current equal to I_{ILIM}. When choosing R_{ILIM}, two options are possible.

If the application requires an output current equal to or greater than external ILIM that the circuit is designed for (input current limit on the charger where the RX is delivering power to is higher than the external ILIM), ensure that the downstream charger is capable of regulating the voltage of the input into which the RX device output is tied to by lowering the amount of current being drawn. This will ensure that the RX output does not collapse.

Such behavior is referred to as VIN DPM in TI chargers. Unless such behavior is enabled on the charger, the charger will pull the output of the RX device to ground when the RX device enters current regulation.

If the applications are designed to extract less than the ILIM (1-A maximum), typical designs should leave a design margin of at least 20% so that the voltage at ILIM pin reaches 1.2 V when 20% more than maximum current of the system is drawn from the output of the RX. Such a design would have input current limit on the charger lower than the external ILIM of the RX device.

In both cases, the charger must be capable of regulating the current drawn from the device to allow the output voltage to stay at a reasonable value. This same behavior is also necessary during the WPC V1.1 Communication. See *Communication Current Limit* for more details. The following calculations show how such a design is achieved:

$$R_{ILIM} = \frac{K_{ILIM}}{1.2 \times I_{ILIM}} \quad (14)$$

$$R_1 = R_{ILIM} - R_{FOD} \quad (15)$$

When referring to the application diagram shown in Figure 15, R_{ILIM} is the sum of the R_1 and R_{FOD} resistance (that is, the total resistance from the ILIM pin to GND). R_{FOD} is chosen according to the FOD application note that can be obtained by contacting your TI representative. This is used to allow the RX implementation to comply with WPC v1.1 requirements related to received power accuracy.

In many applications, the resistor R_{OS} is needed in order to comply with WPC V1.1 requirements. In such a case, the offset on the FOD pin from the voltage on R_{FOD} can cause a shift in the calculation that can reduce the expected current limit. Therefore, it is always a good idea to check the output current limit after FOD calibration is performed according to the FOD application note. Because the RECT voltage is not deterministic, and depends on transmitter operation to a certain degree, it is not possible to determine R_1 with R_{OS} present in a deterministic manner.

In this example, set maximum current for the example to be 1000 mA. Set I_{ILIM} = 1.2 A to allow for the 20% margin.

$$R_{ILIM} = \frac{840}{1.2} = 700\ \Omega \tag{16}$$

9.2.1.2.4 TERM Pin

The term pin is not used for bq5102x. Leave the pin floating.

9.2.1.2.5 I^2C

The I^2C lines are used to communicate with the device. To enable the I^2C, they can be pulled up to an internal host bus. The device address is 0x6C. I^2C is enabled only for the device bq51021.

9.2.1.2.6 Communication Current Limit

Communication current limit allows the device to communicate with the transmitter in an error free manner by decoupling the coil from load transients on the OUT pin during WPC communication. This is done by setting the current limit in a manner that is consistent with Table 4. However, this will require the downstream charger to have a function such as VIN_DPM. In some cases this communication current limit feature is not desirable if the charger does not have this feature. In this design, the user enables the communication current limit by tying the CM_ILIM pin to GND. In the case that this is not needed, the CM_ILIM pin can be tied to OUT pin to disable the communication current limit. In this case, take care that the voltage on the CM_ILIM pin does not exceed the maximum rating of the pin which is 7 V.

9.2.1.2.7 Receiver Coil

The receiver coil design is the most open part of the system design. The choice of the receiver inductance, shape, and materials all intimately influence the parameters themselves in an intertwined manner. This design can be complicated and involves optimizing many different aspects; refer to the user's guide for the EVM (SLUUAX6).

The typical choice of the inductance of the receiver coil for a WPC only 5-V solution is between 8 to 11 µH depending on the mutual inductance between the transmitter coil and the receiver coil.

9.2.1.2.8 Series and Parallel Resonant Capacitors

Resonant capacitors C_1 and C_2 are set according to WPC specification.

The equations for calculating the values of the resonant capacitors are shown:

$$C_1 = \left[\left(f_S \cdot 2\pi \right)^2 \cdot L'_S \right]^{-1}$$

$$C_2 = \left[\left(f_D \cdot 2\pi \right)^2 \cdot L_S - \frac{1}{C_1} \right]^{-1} \tag{17}$$

9.2.1.2.9 Communication, Boot, and Clamp Capacitors

Set C_{COMMx} to a value ranging from C_1 / 8 to C_1 / 3. Note that higher capacitors lower the overall efficiency of the system. Make sure these are X7R ceramic material and have at least a minimum voltage rating of 25 V; TI recommends a minimum voltage rating of 50 V.

Set C_{BOOTx} to be 15 nF. Make sure these are X7R ceramic material and have at least a minimum voltage rating of 25 V; TI recommends a minimum voltage rating of 50 V.

Set C_{CLAMPx} to be 470 nF. Make sure these are X7R ceramic material and have at least a minimum voltage rating of 25 V; TI recommends a minimum voltage rating of 50 V.

9.2.1.3 Application Performance Plots

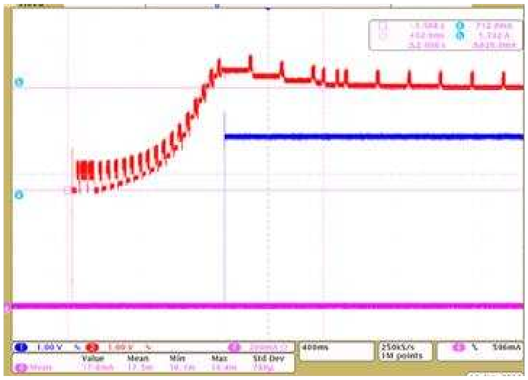


Figure 16. bq5102x No Load Start-up on a WPC TX

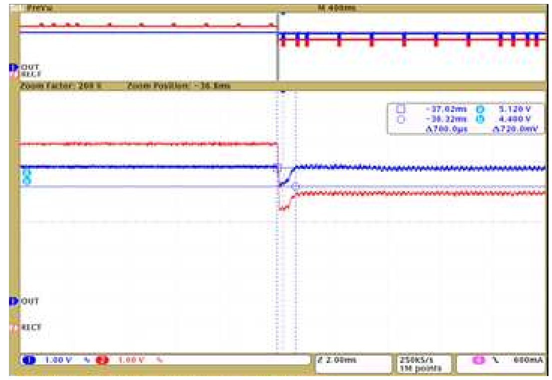


Figure 17. 0- to 1000-mA Step on a WPC TX

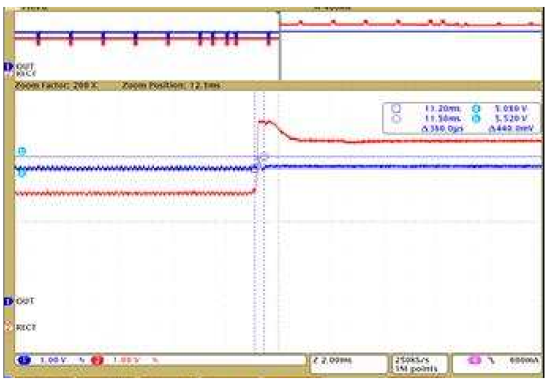


Figure 18. 1000 to 0 mA Load Dump on a WPC TX

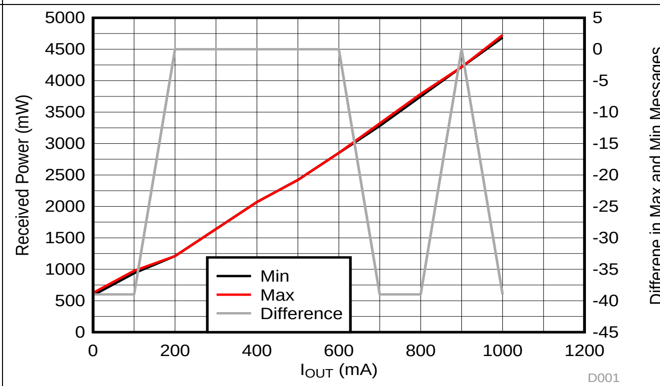


Figure 19. Received Power Variation (mW) vs I_{OUT} (mA) on a WPC TX

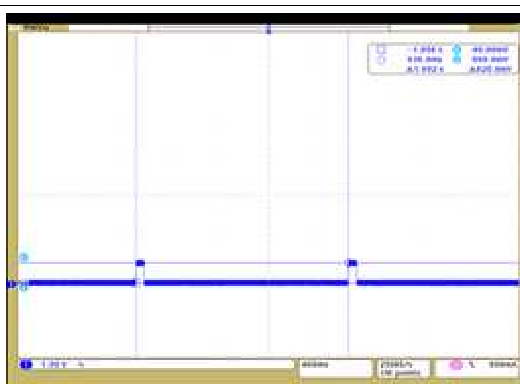


Figure 20. TS Voltage Bias Without TS Resistor

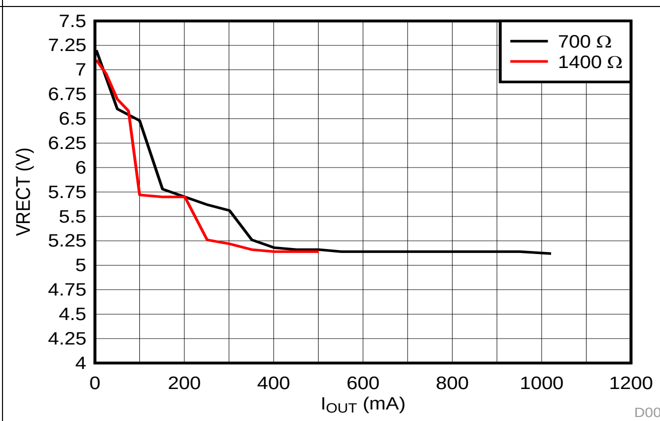


Figure 21. Rectifier Regulation as a Function or R_{ILIM} on a WPC TX

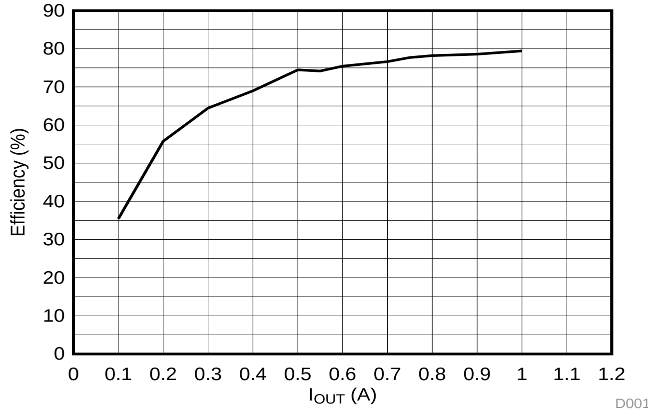


Figure 22. bq5102x WPC Efficiency 5 V, 1 A on a WPC TX

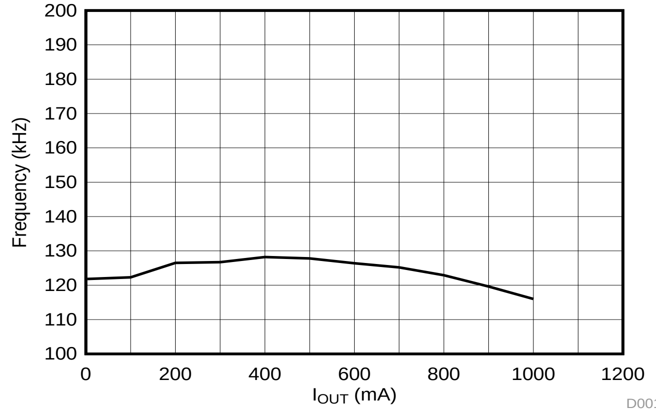


Figure 23. Frequency Range of 5-V, 1-A RX on a WPC TX

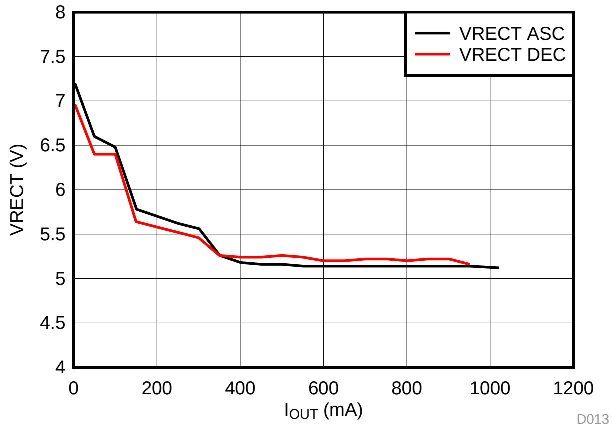


Figure 24. Dynamic Regulation, RILIM = 700 Ω on a WPC TX

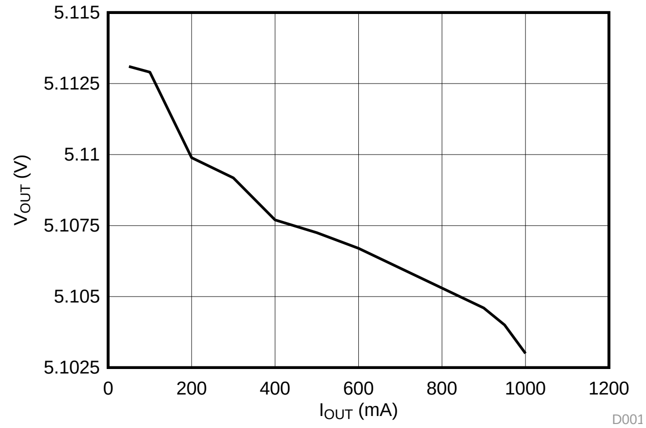


Figure 25. Output Regulation on a WPC TX

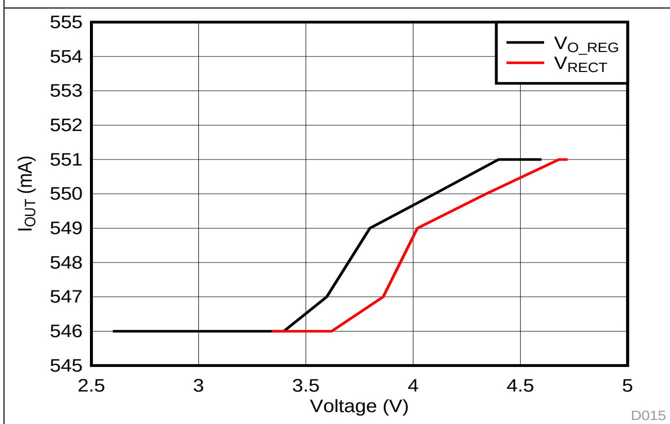


Figure 26. Rect Foldback in Current Limit on a WPC TX

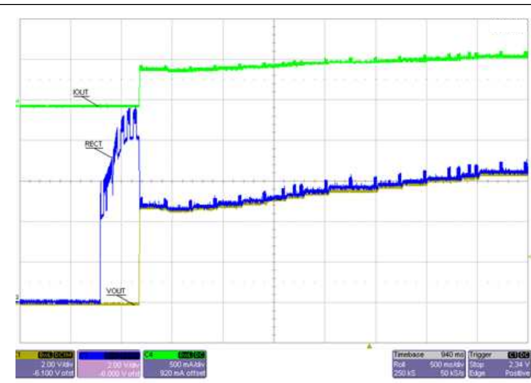


Figure 27. Start-Up WPC TX 7-V Out

9.2.2 bq5102x Standalone in System Board or Back Cover

When the bq5102x device is implemented as an embedded device on the system board, the EN1 and EN2 pins are the only differences from the previous design using I^2C.

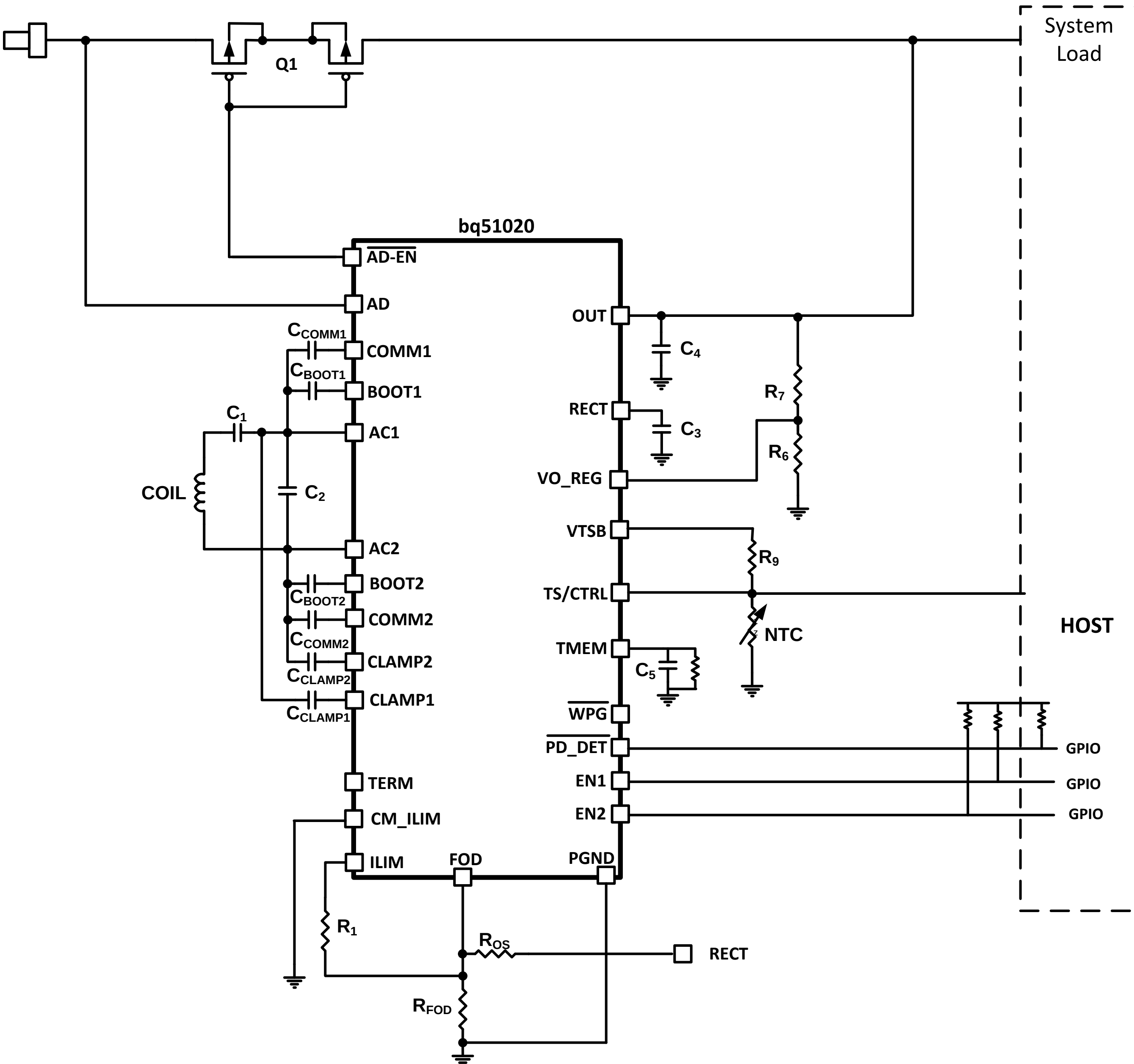


Figure 28. bq5102x Embedded in a System Board

Refer to *WPC Power Supply 5-V Output With 1-A Maximum Current and I^2C* for all design and application details.

10 Power Supply Recommendations

These devices are intended to be operated within the ranges shown in the *Recommended Operating Conditions*. Because the system involves a loosely coupled inductor setup, the voltages produced on the receiver are a function of the inductances and the available magnetic field. Ensure that the design in the worst case keeps the voltages within the *Absolute Maximum Ratings*.

11 Layout

11.1 Layout Guidelines

- Keep the trace resistance as low as possible on AC1, AC2, and OUT.
- Detection and resonant capacitors need to be as close to the device as possible.
- COMM, CLAMP, and BOOT capacitors need to be placed as close to the device as possible.
- Via interconnect on GND net is critical for appropriate signal integrity and proper thermal performance.
- High frequency bypass capacitors need to be placed close to RECT and OUT pins.
- ILIM and FOD resistors are important signal paths and the loops in those paths to GND must be minimized.

  Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude. Make sure that these traces are not being interfered by the noisy and power traces. AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components.

  For a 1-A fast charge current application, the current rating for each net is as follows:
  - AC1 = AC2 = 1.2 A
  - OUT = 1 A
  - RECT = 100 mA (RMS)
  - COMMx = 300 mA
  - CLAMPx = 500 mA
  - All others can be rated for 10 mA or less

11.2 Layout Example

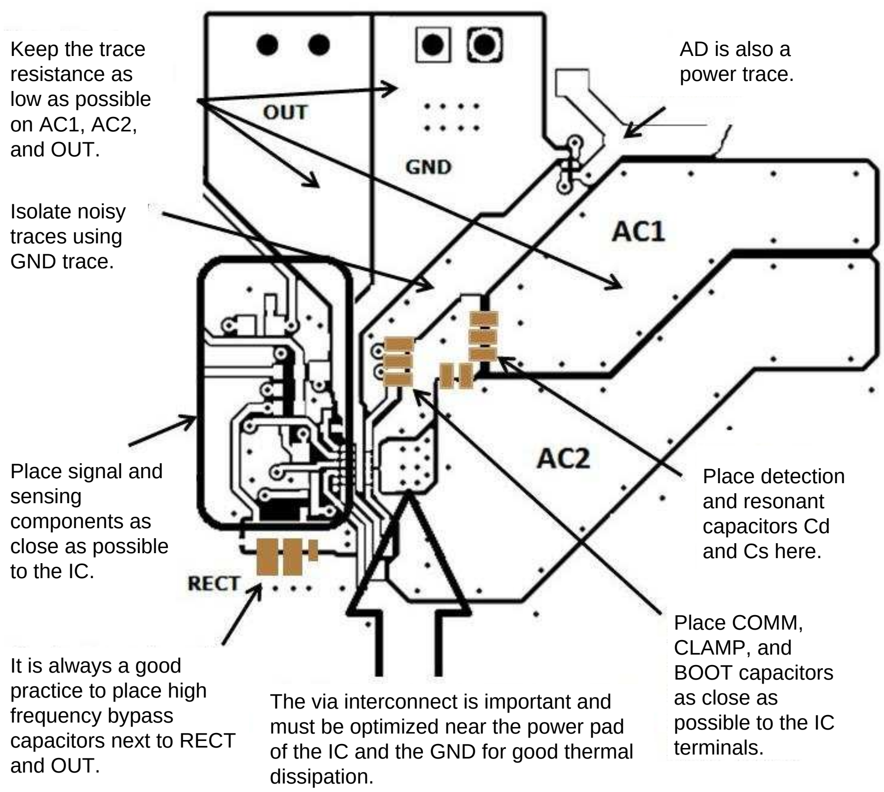


Figure 29. Layout Example for bq5102x

12 器件和文档支持

12.1 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

Table 18. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
bq51020	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq51021	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51020YFPR	ACTIVE	DSBGA	YFP	42	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51020	Samples
BQ51020YFPT	ACTIVE	DSBGA	YFP	42	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51020	Samples
BQ51021YFPR	ACTIVE	DSBGA	YFP	42	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51021	Samples
BQ51021YFPT	ACTIVE	DSBGA	YFP	42	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	BQ51021	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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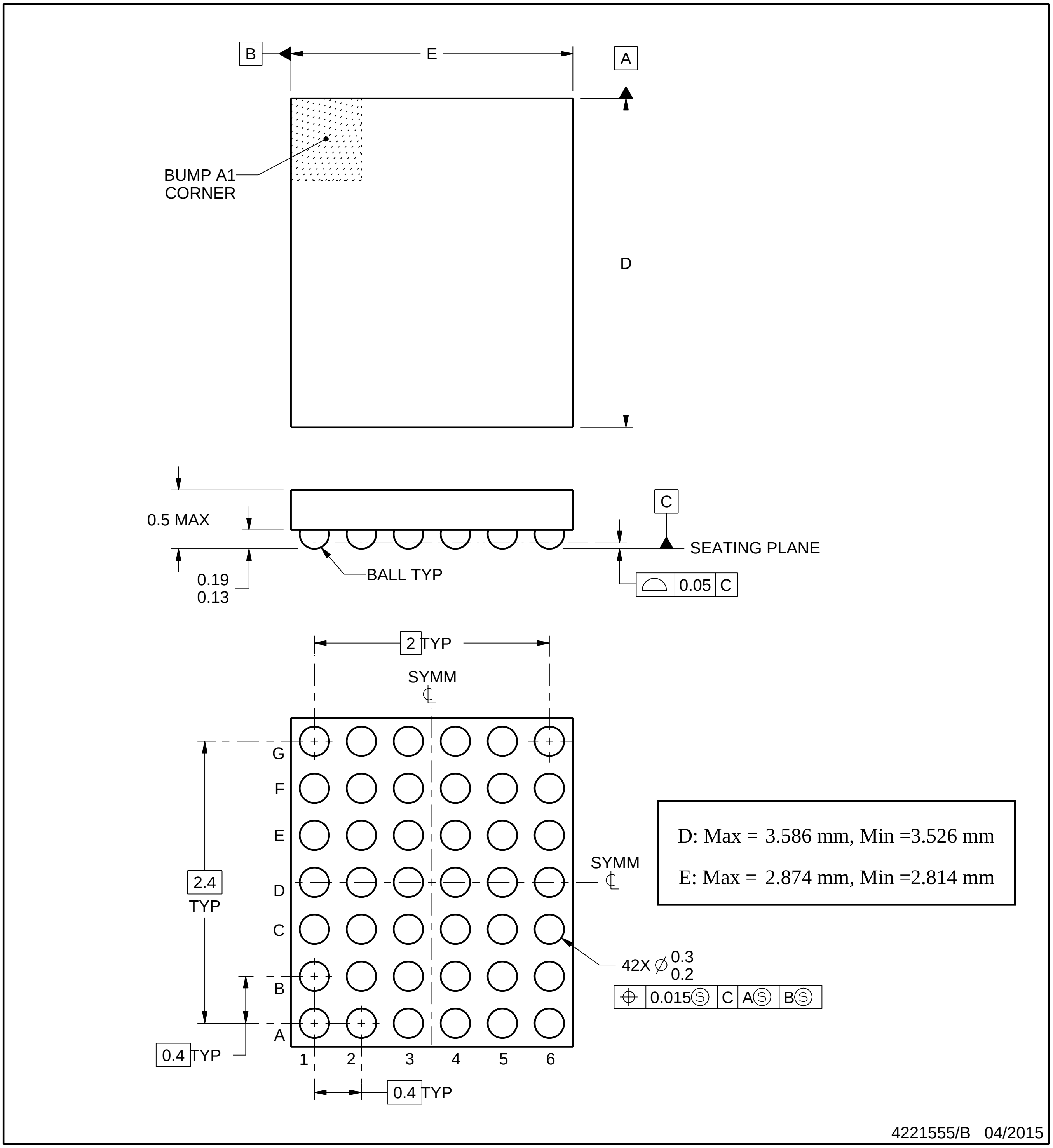
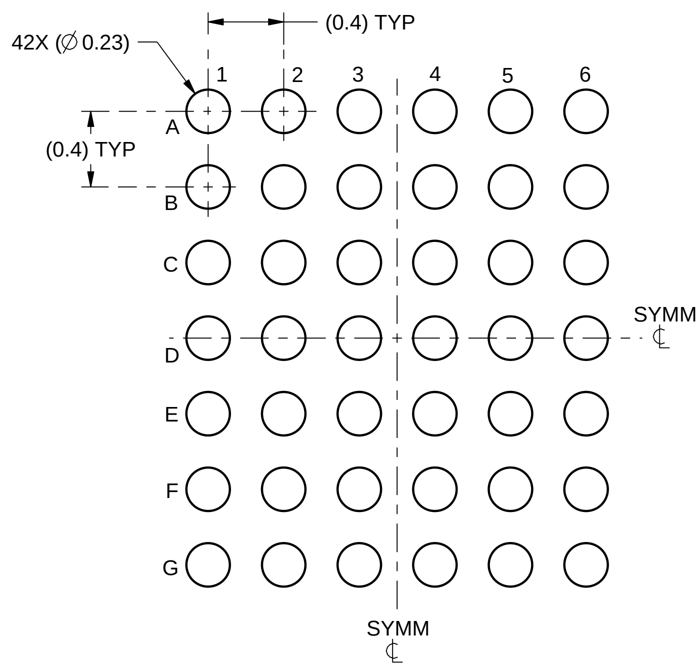
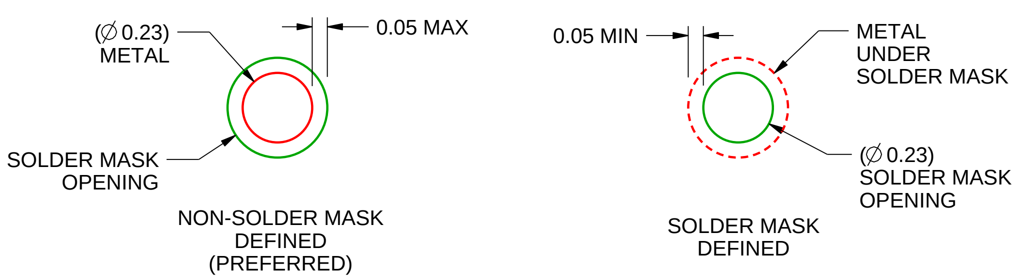


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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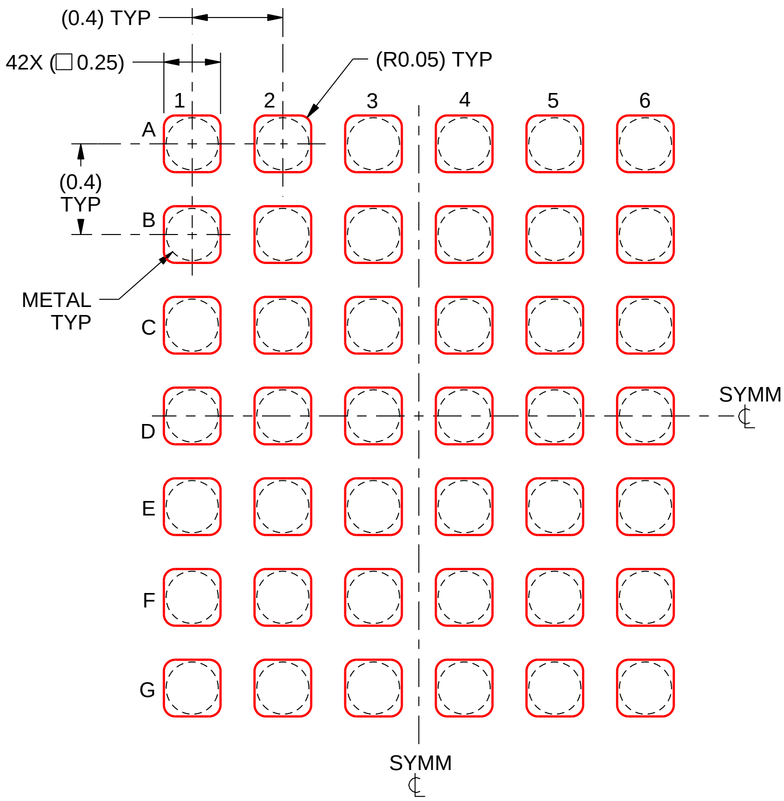
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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