带有双集成比较器的 INA30x 36V 过流保护高速精密电流传感放大器

1 特性

- 宽共模输入范围：–0.1V 至 36V
- 双比较器输出：
  - INA302：两个独立的超限警报
  - INA303：窗口比较器
  - 阈值水平单独设置
  - 比较器 1 警报响应：1µs
  - 比较器 2 可调延迟：2µs 至 10s
  - 具有独立锁存控制模式的开漏极输出
- 高精度放大器：
  - 偏移电压：30µV（最大值，A3 版本）
  - 偏移电压漂移：0.5µV/°C（最大值）
  - 增益误差：0.15%（最大值，A3 版本）
  - 增益误差漂移：10ppm/°C
- 可用放大器增益：
  - INA302A1、INA303A1：20V/V
  - INA302A2、INA303A2：50V/V
  - INA302A3、INA303A3：100V/V

2 应用范围

- 过流保护
- 电机控制
- 电源保护
- 计算机和服务器
- 电信设备

3 说明

INA302 和 INA303 器件具有一个高共模、双向电流传感放大器和两个高速比较器，用于检测超出范围的电流状况。INA302 比较器配置为检测和响应过流状况。INA303 比较器配置为在窗口配置中响应过流和欠流状况。该器件 每个 一个可调节限制阈值范围，该范围通过一个外部限值设定电阻进行设置。这些电流分流监控器可在独立于电源的 –0.1V 至 36V 共模电压范围内测量差动电压信号。

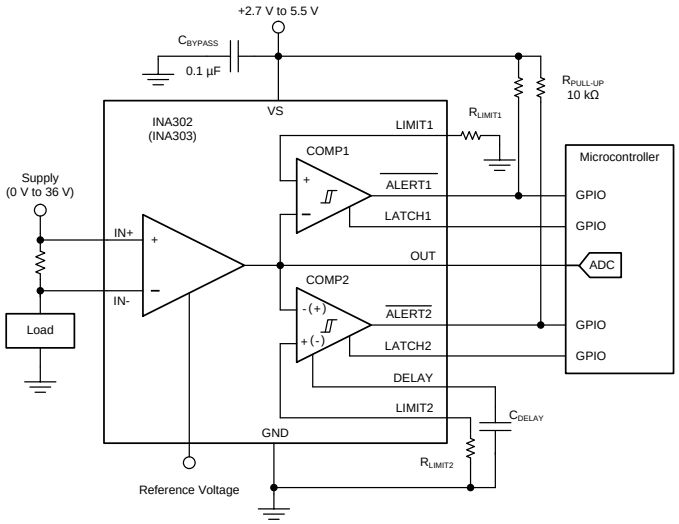
开漏极警报输出可配置为在透明模式（输出状态与输入状态保持一致）或锁存模式（警报输出在锁存复位时清除）下运行。比较器 1 的警报响应时间小于 1µs，而比较器 2 的警报响应时间通过外部电容器进行设置，范围介于 2µs 至 10s 之间。

此器件由 2.7V 至 5.5V 的单个电源供电，消耗的最大电源电流为 950µA。该器件具有扩展级工作温度范围（–40°C 至 +125°C），并且采用 14 引脚 TSSOP 封装。

器件信息

器件编号	封装	封装尺寸
INA302	TSSOP (14)	4.40mm × 5.00mm
INA303	TSSOP (14)	4.40mm × 5.00mm

典型应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2017) to Revision B **Page**

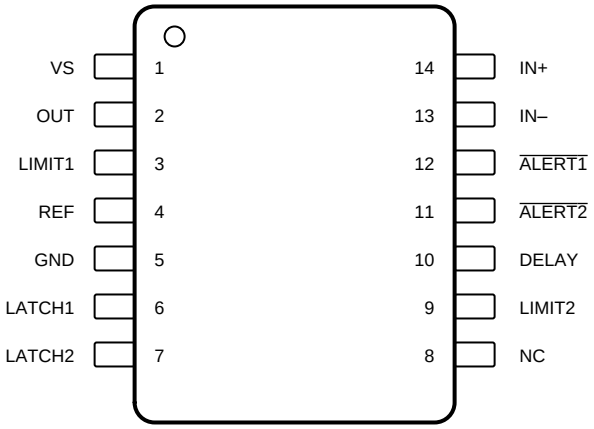
- 已更改 y-axis units from *0.5 V/div* to *1 V/div* and changed *(INA30xA1)* to *(INA30x)* in title of *Comparator 1 Total Propagation Delay* figure ... 12
- 已更改 y-axis units from *0.5 V/div* to *1 V/div* and changed *(INA303A1)* to *(INA303)* in title of *Comparator 2 Total Propagation Delay* figure ... 12
- 已删除 *Comparator 1 Total Propagation Delay (INA30xA2)*, *Comparator 1 Total Propagation Delay (INA30xA3)*, *Comparator 2 Total Propagation Delay (INA303A2)*, and *Comparator 2 Total Propagation Delay (INA303A3)* figures ... 12
- 已更改 *(INA303A1)* to *(INA303)* in title of *Comparator 2 Total Propagation Delay* figure ... 12
- 已删除 *Comparator 2 Total Propagation Delay (INA303A2)* and *Comparator 2 Total Propagation Delay (INA303A3)* figures ... 12
- 已添加 *Comparator 2 Total Propagation Delay (INA302A1)* and *Comparator 2 Total Propagation Delay (INA302A1)* figures ... 12

Changes from Original (September 2016) to Revision A **Page**

- 投入生产 ... 1

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VS	Analog	Power supply, 2.7 V to 5.5 V
2	OUT	Analog output	Output voltage
3	LIMIT1	Analog input	$\overline{\text{ALERT1}}$ threshold limit input; see the *Setting Alert Thresholds* section for details on setting the limit threshold
4	REF	Analog input	Reference voltage, 0 V to VS
5	GND	Analog	Ground
6	LATCH1	Digital input	Transparent or latch mode selection input
7	LATCH2	Digital input	Transparent or latch mode selection input
8	NC	—	No internal connection
9	LIMIT2	Analog input	$\overline{\text{ALERT2}}$ threshold limit input; see the *Setting Alert Thresholds* section for details on setting the limit threshold
10	DELAY	Analog input	Delay timing input; see the *Alert Outputs* section for details on setting the delayed alert response for comparator 2
11	$\overline{\text{ALERT2}}$	Analog output	Open-drain output; active-low. This pin is an overlimit alert for the INA302 and an underlimit alert for the INA303.
12	$\overline{\text{ALERT1}}$	Analog output	Open-drain output, active-low overlimit alert
13	IN–	Analog input	Connect to load side of the current-sensing resistor
14	IN+	Analog input	Connect to supply side of the current-sensing resistor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–40	40	V
	Common-mode(3)	GND – 0.3	40	
Analog input	LIMIT1, LIMIT2, DELAY, V_{REF}	GND – 0.3	(V_S) + 0.3	V
Analog output	OUT	GND – 0.3	(V_S) + 0.3	V
Digital input	LATCH1, LATCH2	GND – 0.3	(V_S) + 0.3	V
Digital output	$\overline{ALERT1}$, $\overline{ALERT2}$	GND – 0.3	6	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage can exceed the voltage shown without causing damage to the device if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA30x PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = 0 V, V_{REF} = V_S / 2, V_S = 5 V, V_{IN+} = 12 V, V_{LIMIT1} = 3 V, and V_{LIMIT2} = 3 V (INA302) or V_{LIMIT2} = 2 V (INA303) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage range		–0.1		36	V
V_{IN}	Differential input voltage range	V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A1 versions	0		±125	mV
		V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A2 versions	0		±50	
		V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A3 versions	0		±25	
CMRR	Common-mode rejection ratio	V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC, A1 versions	100	114		dB
		V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC, A2 versions	106	118		
		V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC, A3 versions	110	120		
V_{OS}	Offset voltage, RTI(1)	A1 versions		±15	±80	µV
		A2 versions		±10	±50	
		A3 versions		±5	±30	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A= –40ºC to +125ºC		0.02	0.25	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A = –40ºC to +125ºC		±0.3	±5	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$		115		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.01		µA
OUTPUT						
G	Gain	A1 versions		20		V/V
		A2 versions		50		
		A3 versions		100		
	Gain error	V_{OUT} = 0.5 V to V_S – 0.5 V, A1 versions		±0.02%	±0.075%	
		V_{OUT} = 0.5 V to V_S – 0.5 V, A2 versions		±0.05%	±0.1%	
		V_{OUT} = 0.5 V to V_S – 0.5 V, A3 versions		±0.1%	±0.15%	
		T_A= –40ºC to +125ºC		3	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		500		pF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40ºC to +125ºC		V_S – 0.05	V_S – 0.1	V
	Swing to GND	R_L = 10 kΩ to GND, T_A = –40ºC to +125ºC		V_{GND} + 15	V_{GND} + 30	mV
FREQUENCY RESPONSE						
BW	Bandwidth	A1 versions, C_{OUT} = 500 pF		550		kHz
		A2 versions, C_{OUT} = 500 pF		440		
		A3 versions, C_{OUT} = 500 pF		400		
SR	Slew rate			4		V/µs
NOISE, RTI(1)						
	Voltage noise density			30		nV/√Hz

(1) RTI = referred-to-input.

Electrical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = 0 V, V_{REF} = V_S / 2, V_S = 5 V, V_{IN+} = 12 V, V_{LIMIT1} = 3 V, and V_{LIMIT2} = 3 V (INA302) or V_{LIMIT2} = 2 V (INA303) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPARATOR						
t_p	Total alert propagation delay	Comparator 1, input overdrive = 1 mV		0.6	1	µs
		Comparator 2, input overdrive = 1 mV, delay = 100 kΩ to V_S		1.25	2	
	Slew-rate-limited t_p	Comparator 1, V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V		1	1.5	µs
		Comparator 2 (INA302), V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V, delay = 100 kΩ to V_S		1.5	2.5	
		Comparator 2 (INA303), V_{OUT} step = 4.5 V to 0.5 V, V_{LIMIT} = 1 V, delay = 100 kΩ to V_S		1.5	2.5	
I_{LIMIT1}	Limit threshold output current, comparator 1	T_A = 25ºC, V_{LIMIT1} < V_S – 0.6 V	79.2	80	80.8	µA
		T_A = –40ºC to +125ºC, V_{LIMIT1} < V_S – 0.6 V	78.4		81.6	
I_{LIMIT2}	Limit threshold output current, comparator 2	T_A = 25ºC, V_{LIMIT2} < V_S – 0.6 V	79.7	80	80.4	µA
		T_A = –40ºC to +125ºC, V_{LIMIT2} < V_S – 0.6 V	79.2		80.8	
V_{OS}	Offset voltage, both comparators	A1 versions		0.5	3.5	mV
		A2 versions		0.5	3.5	
		A3 versions		0.5	4.0	
HYS	Hysteresis	comparator 1, comparator 2		100		mV
	Internal programmable delay error	T_A = –40ºC to +125ºC			4%	
V_{TH}	Delay threshold voltage	T_A = –40ºC to +125ºC	1.21	1.22	1.23	V
I_D	Delay charging current	T_A = –40ºC to +125ºC, V_{DELAY} = 0.6 V	4.85	5	5.15	µA
R_D	Delay discharge resistance			70		Ω
V_{IH}	LATCH1, LATCH2 high-level input voltage	T_A = –40ºC to +125ºC	1.4		6	V
V_{IL}	LATCH1, LATCH2 low-level input voltage	T_A = –40ºC to +125ºC	0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA, T_A = –40ºC to +125ºC		70	400	mV
	$\overline{ALERT1}$, $\overline{ALERT2}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	LATCH1, LATCH2 digital leakage input current	0 V ≤ V_{LATCH1} , V_{LATCH2} ≤ V_S		1		µA
POWER SUPPLY						
V_S	Operating supply range	T_A = –40ºC to +125ºC	2.7		5.5	V
I_Q	Quiescent current	T_A = 25ºC		850	950	µA
		T_A = –40ºC to +125ºC			1150	
TEMPERATURE RANGE						
	Specified range		–40		125	°C

6.6 Typical Characteristics

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

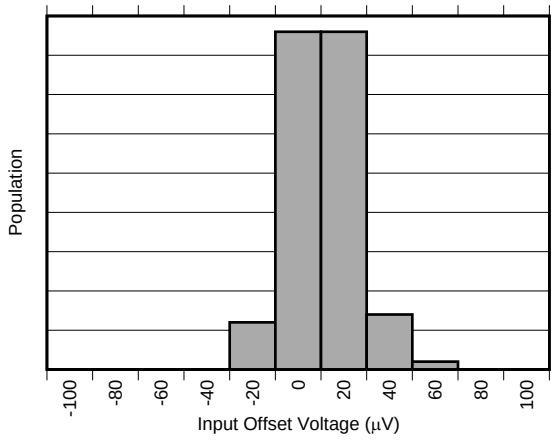


图 1. Input Offset Voltage Distribution (INA30xA1)

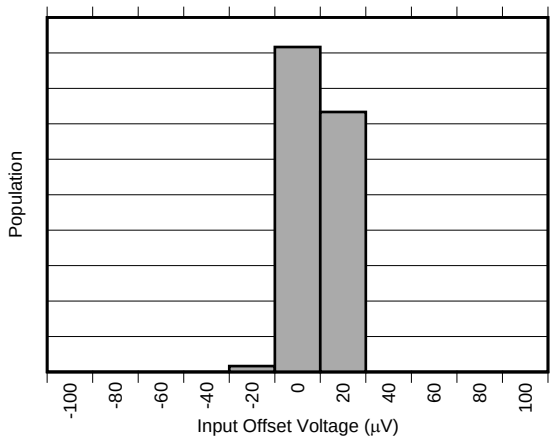


图 2. Input Offset Voltage Distribution (INA30xA2)

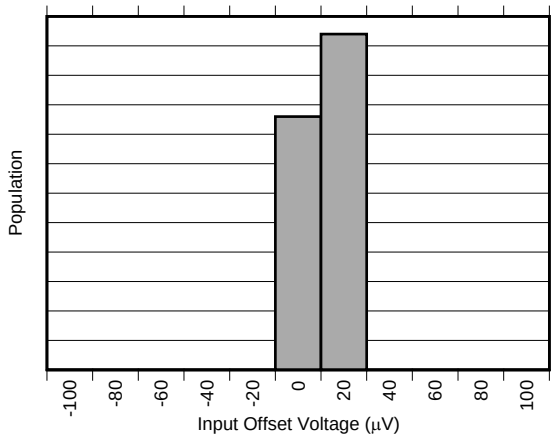


图 3. Input Offset Voltage Distribution (INA30xA3)

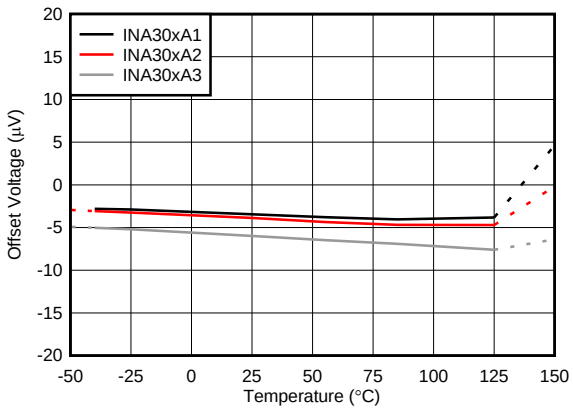


图 4. Input Offset Voltage vs Temperature

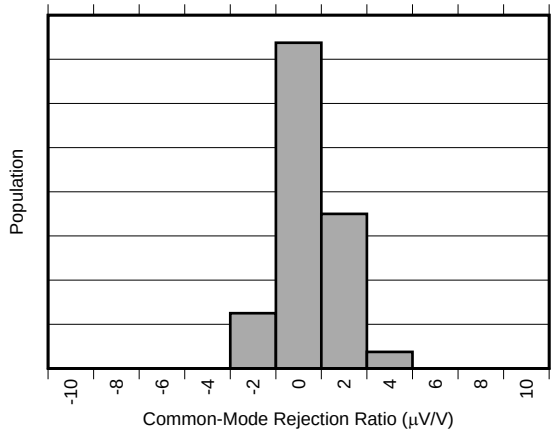


图 5. CMRR Distribution (INA30xA1)

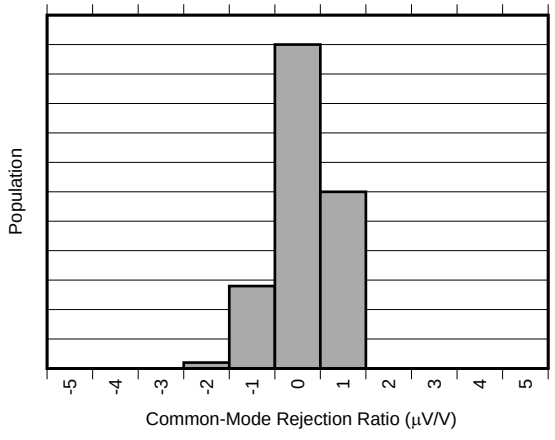


图 6. CMRR Distribution (INA30xA2)

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

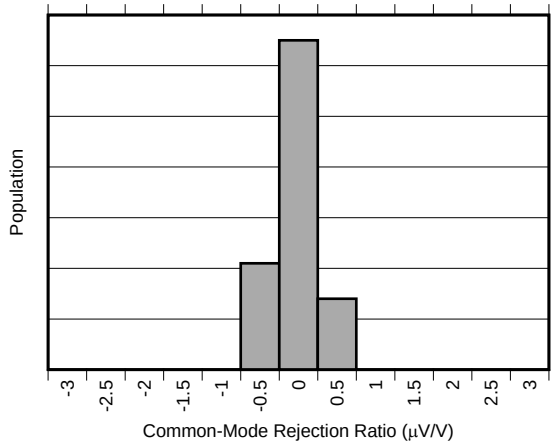


图 7. CMRR Distribution (INA30xA3)

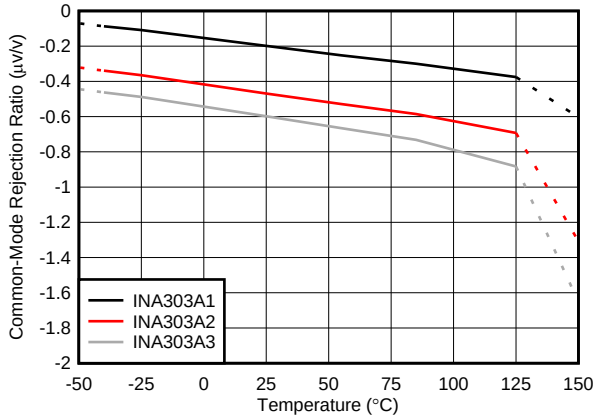


图 8. CMRR vs Temperature

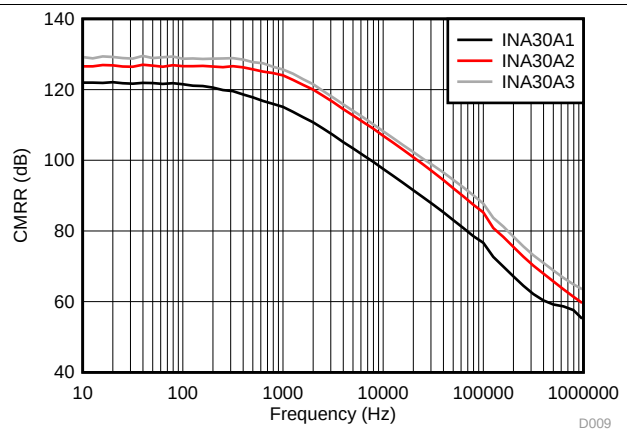


图 9. CMRR vs Frequency

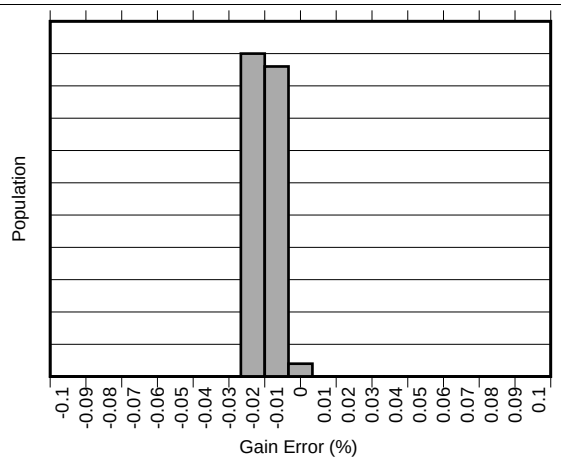


图 10. Gain Error Distribution (INA30xA1)

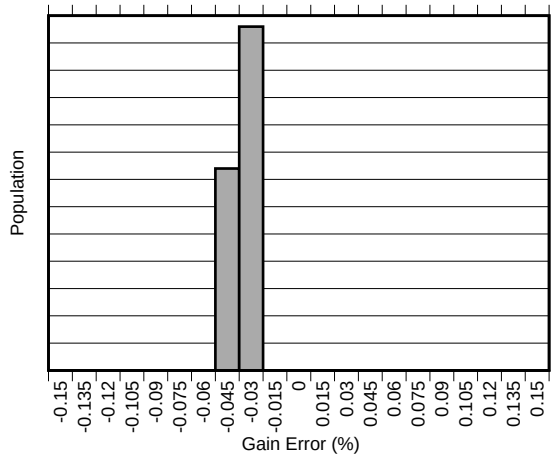


图 11. Gain Error Distribution (INA30xA2)

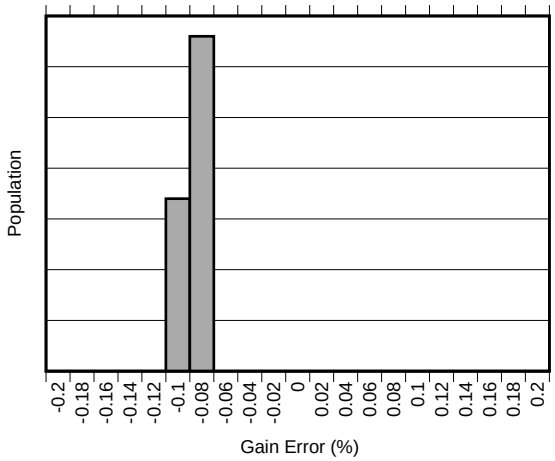


图 12. Gain Error Distribution (INA30xA3)

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

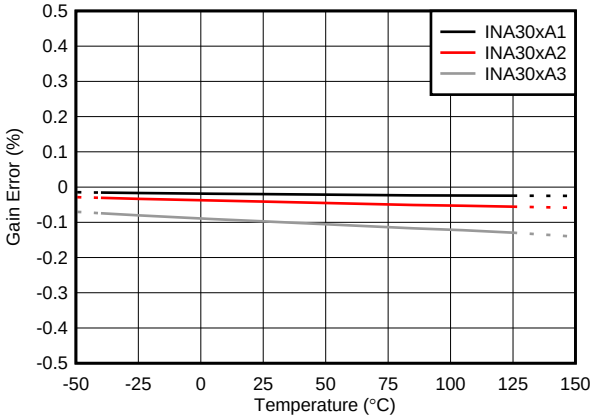


图 13. Gain Error vs Temperature

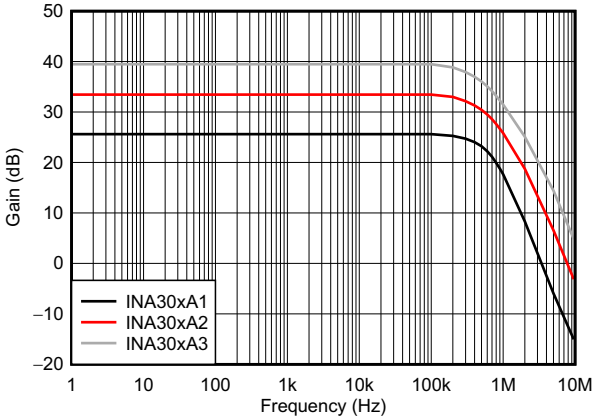


图 14. Gain vs Frequency

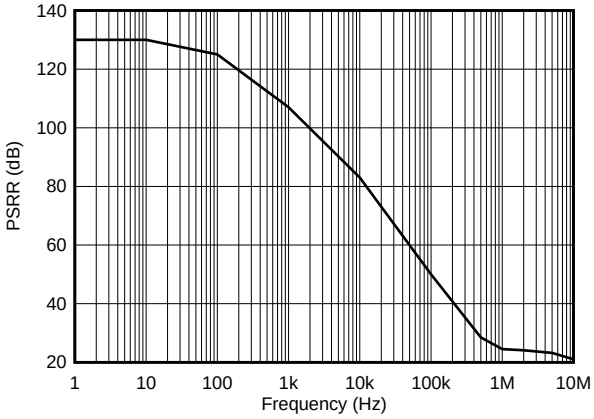


图 15. PSRR vs Frequency

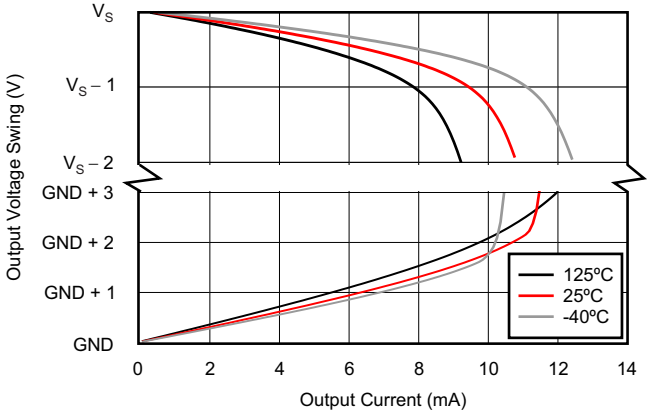


图 16. Output Voltage Swing vs Output Current

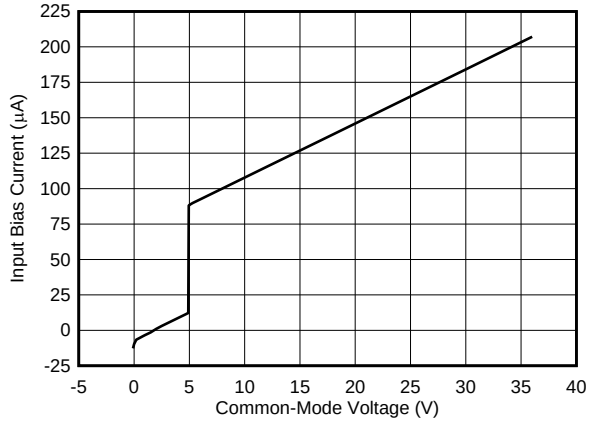


图 17. Input Bias Current vs Common-Mode Voltage (V_S = 5 V)

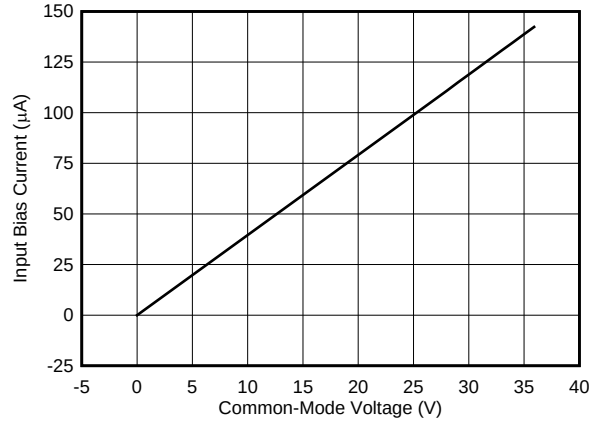


图 18. Input Bias Current vs Common-Mode Voltage (V_S = 0 V)

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

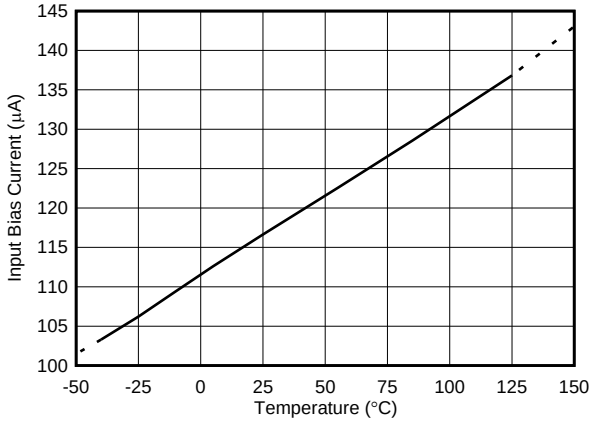


图 19. Input Bias Current vs Temperature

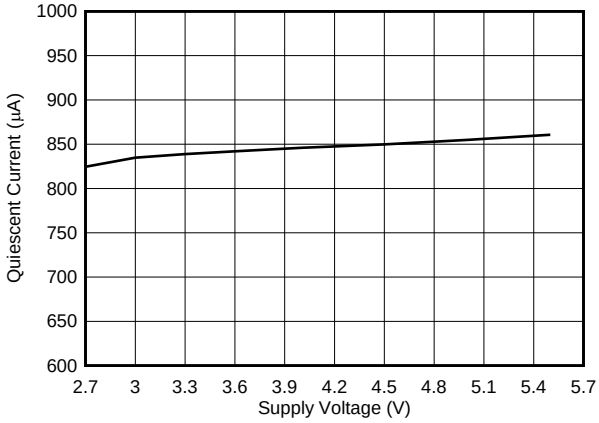


图 20. Quiescent Current vs Supply Voltage

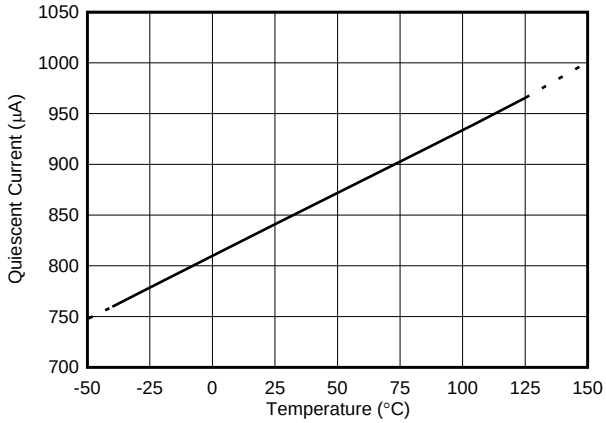


图 21. Quiescent Current vs Temperature

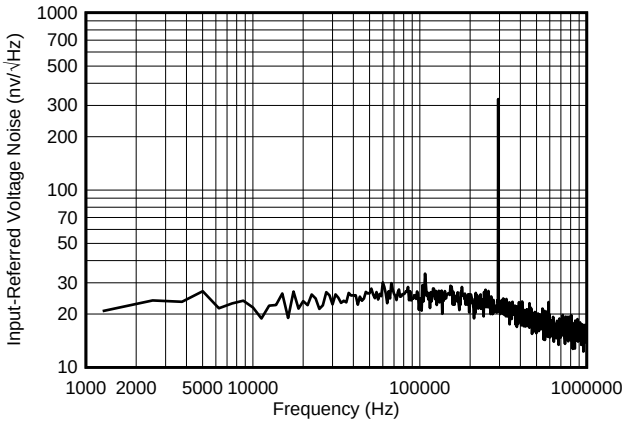


图 22. Input-Referred Voltage Noise vs Frequency

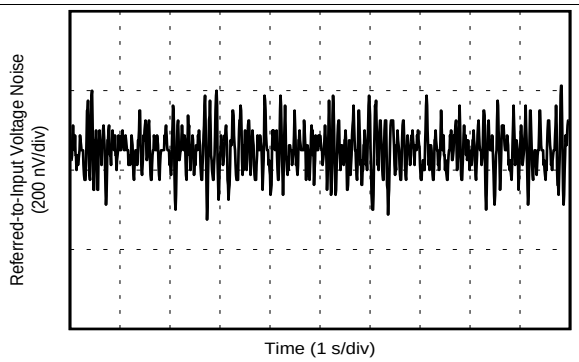


图 23. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

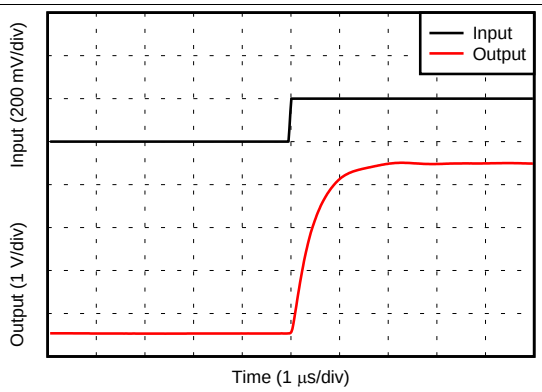


图 24. Voltage Output Rising Step Response (4-V_{PP} Output Step)

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

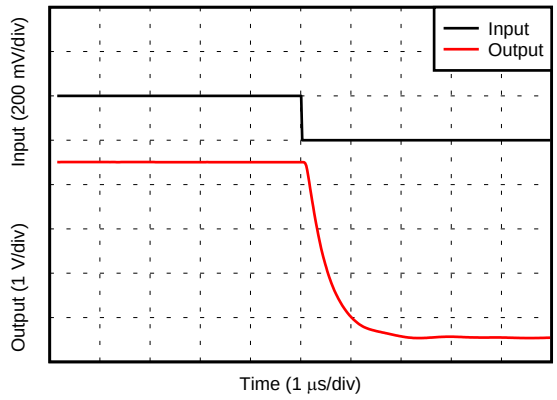


图 25. Voltage Output Falling Step Response (4-V_{PP} Output Step)

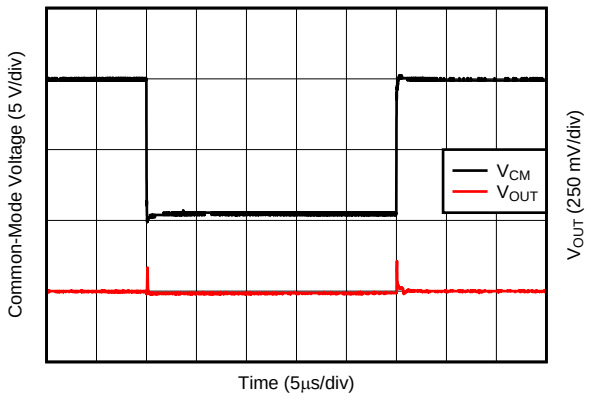


图 26. Common-Mode Voltage Transient Response

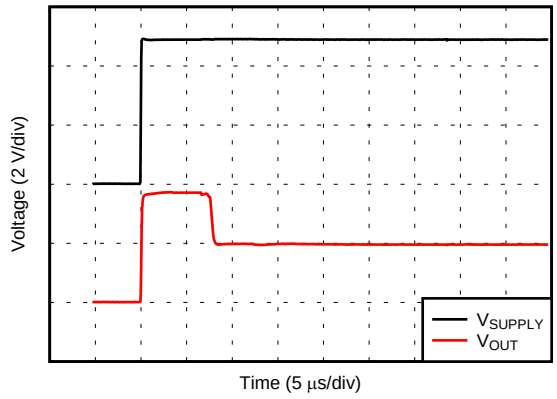


图 27. Start-Up Response

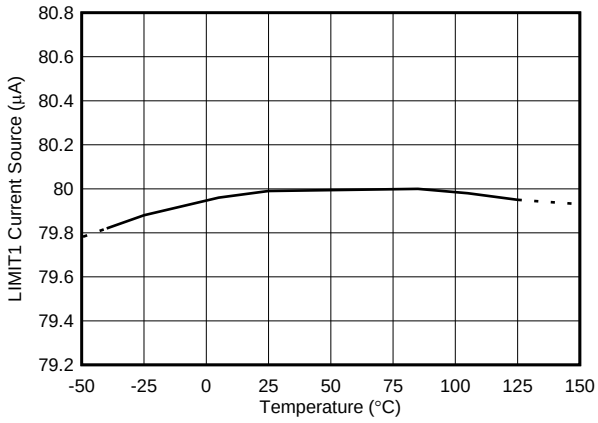


图 28. LIMIT1 Current Source vs Temperature

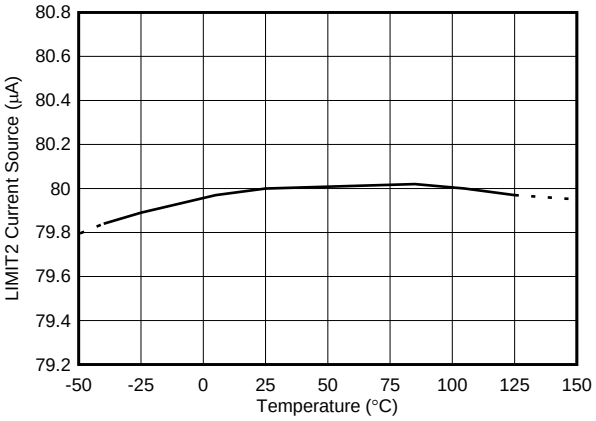


图 29. LIMIT2 Current Source vs Temperature

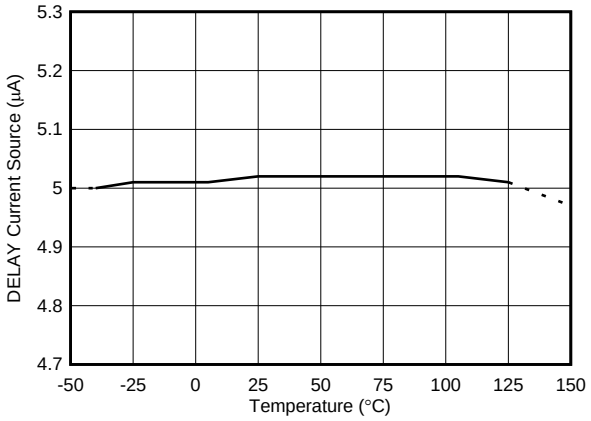


图 30. DELAY Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

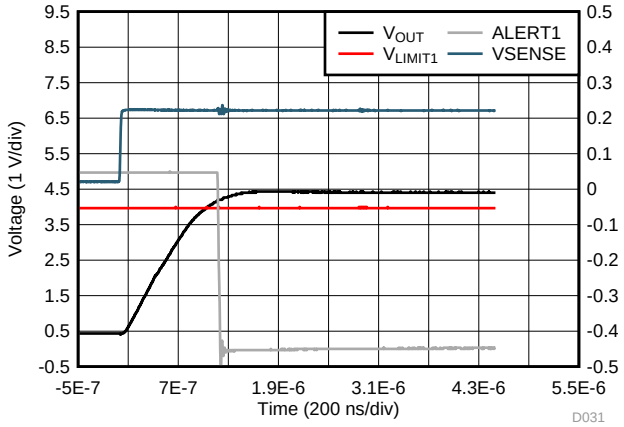


图 31. Comparator 1 Total Propagation Delay (INA30x)

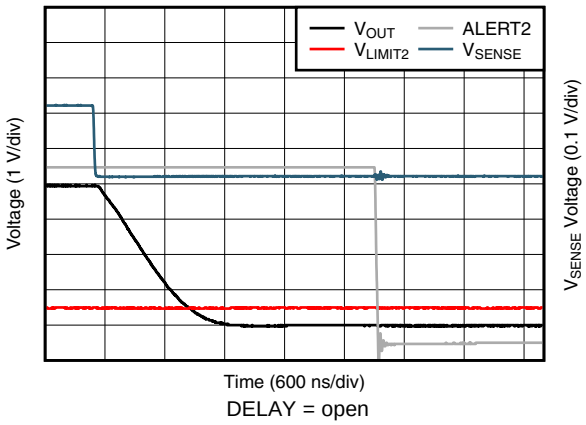


图 32. Comparator 2 Total Propagation Delay (INA303)

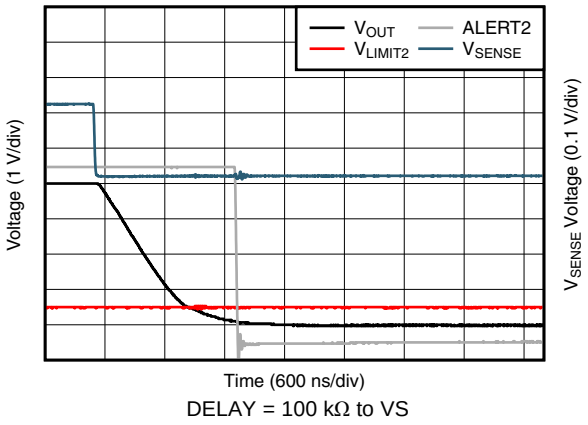


图 33. Comparator 2 Total Propagation Delay (INA303)

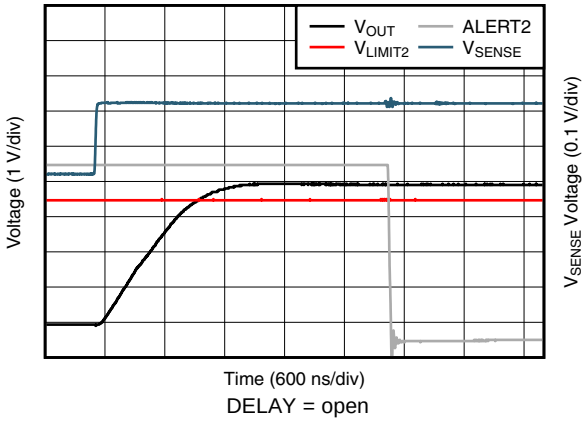


图 34. Comparator 2 Total Propagation Delay (INA302)

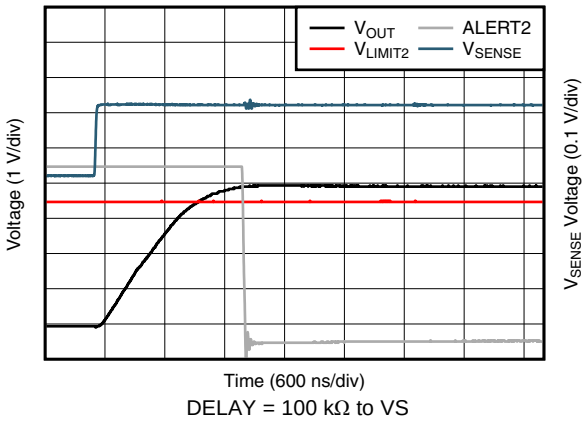


图 35. Comparator 2 Total Propagation Delay (INA302)

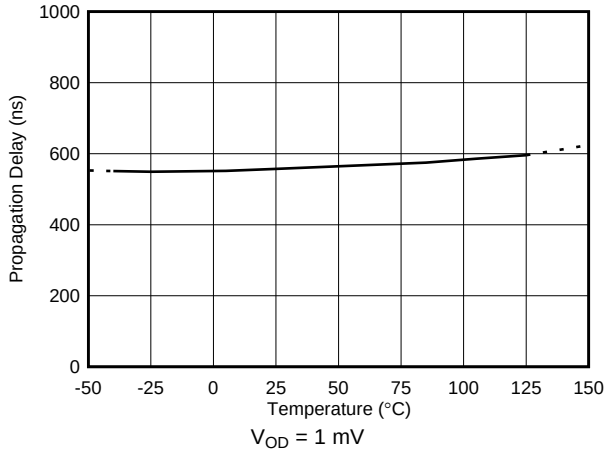


图 36. Comparator 1 Propagation Delay vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistor = 10 kΩ (unless otherwise noted)

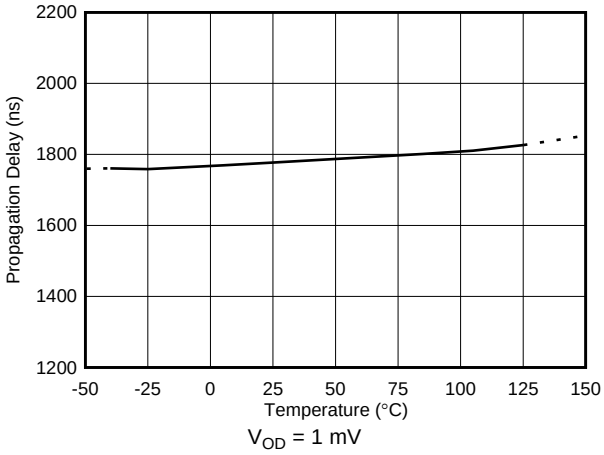


图 37. Comparator 2 Propagation Delay vs Temperature

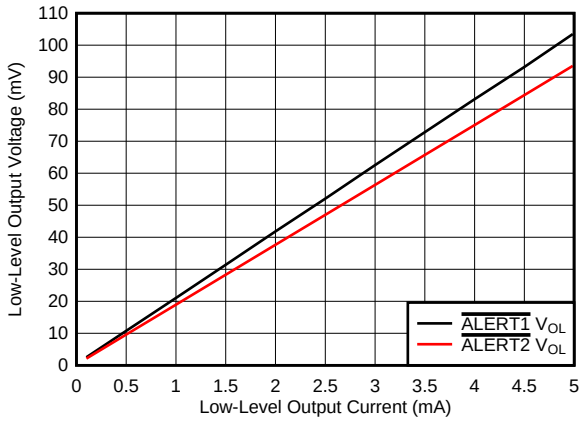


图 38. Comparator Alert V_{OL} vs I_{OL}

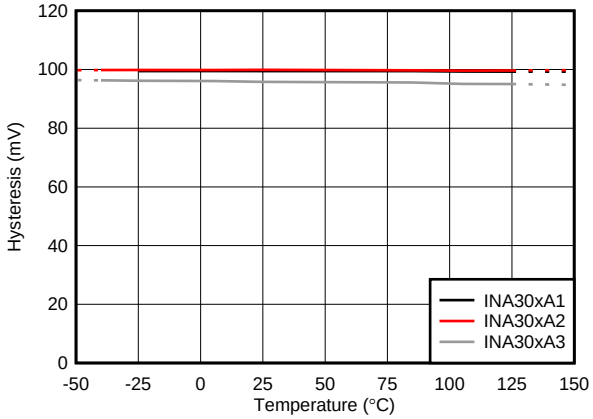


图 39. Comparator 1 Hysteresis vs Temperature

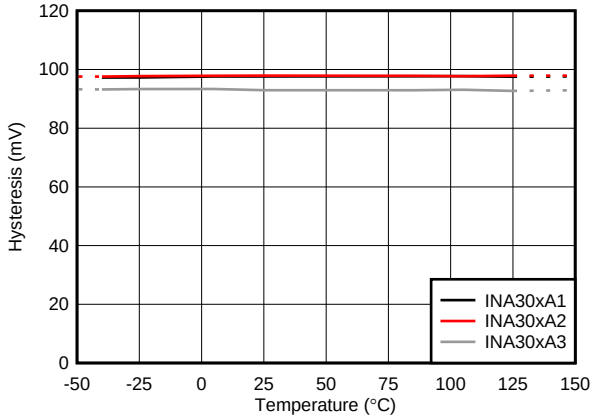


图 40. Comparator 2 Hysteresis vs Temperature

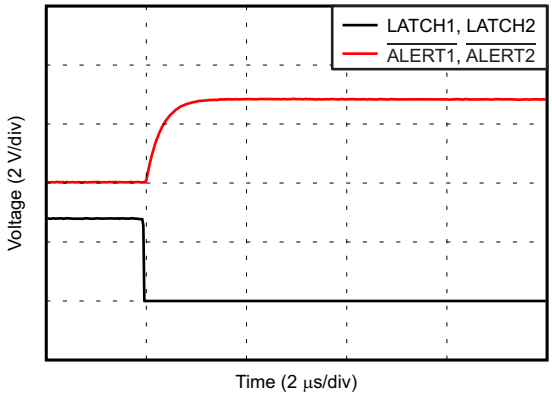


图 41. Comparator Latch Response

7 Detailed Description

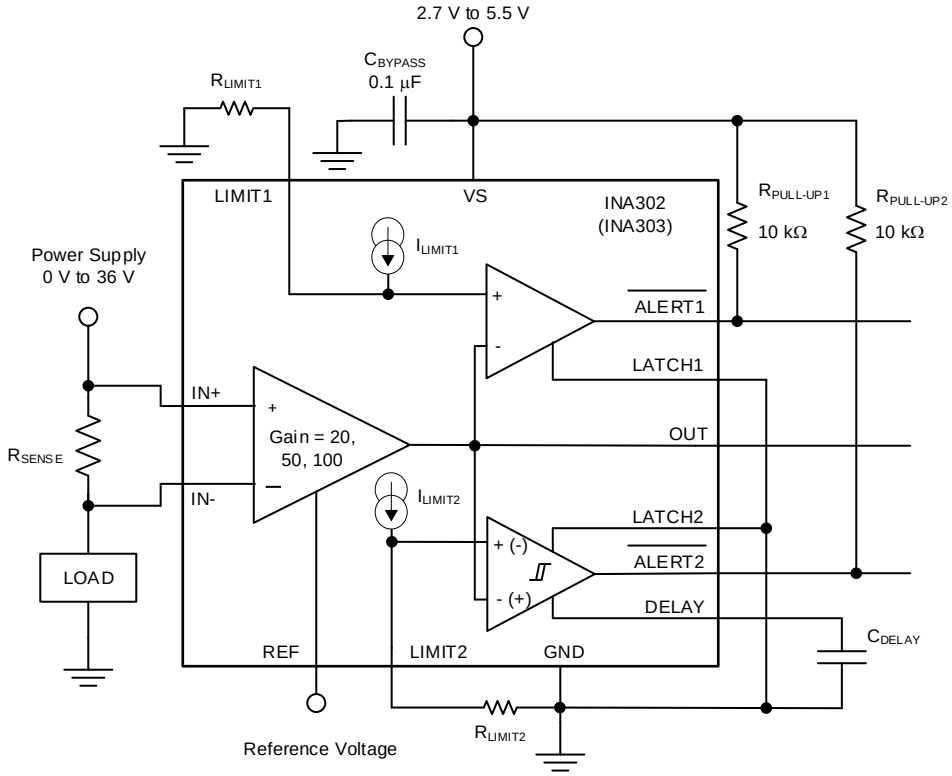
7.1 Overview

The INA30x features a zero-drift, 36-V, common-mode, bidirectional, current-sensing amplifier and two high-speed comparators that can detect multiple out-of-range current conditions. The specially designed, current-sensing amplifier can be used in both low-side or high-side applications where common-mode voltages far exceed the supply voltage of the device. Currents are measured by accurately sensing voltages developed across current-sensing resistors (also known as *current-shunt resistors*). Current can be measured on input voltage rails as high as 36 V, and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 30 μV (max) with a temperature contribution of only 0.25 μV/°C (max) over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA302 enables smaller current-sense resistor values to be used, improving power-efficiency without sacrificing measurement accuracy resulting from the smaller input signal.

Both the INA302 and INA303 use a single external resistor to set each out-of-range threshold. The INA302 allows for two overcurrent thresholds and the INA303 allows for both an under- and overcurrent threshold. The response time of the ALERT1 threshold is fixed and is less than 1 μs. The response time of the ALERT2 threshold can be set with an external capacitor. The combination of a precision current-sense amplifier with onboard comparators creates a highly-accurate solution that is capable of fast detection of multiple out-of-range conditions. The ability to detect when currents are out-of-range allows the system to take corrective actions to prevent potential component or system-wide damage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bidirectional Current Sensing and Out-of-Range Detection

The INA302 and INA303 can sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is above the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is below the applied reference voltage. The equation for the output voltage of the current-sense amplifier is shown in 公式 1.

$$V_{OUT} = \left(I_{LOAD} \times R_{SENSE} \times GAIN\right) + V_{REF}$$

where

- I_{LOAD} is the load current to be monitored
- R_{SENSE} is the current-sense resistor
- GAIN is the gain option of the device selected and
- V_{REF} is the voltage applied to the REF pin (1)

The INA303 can detect when negative currents are out-of-range by setting a voltage at the LIMIT2 pin that is below the applied reference voltage. The limit voltage can be set with an external resistor or externally driven by a voltage source or digital-to-analog converter (DAC); see the *Setting Alert Thresholds* section for additional information. A typical application using the INA303 to detect negative overcurrent conditions is illustrated in the *Typical Application* section.

7.3.2 Alert Outputs

Both $\overline{\text{ALERTx}}$ pins are active-low, open-drain outputs that pull low when the sensed current is detected to be out-of-range. Both open-drain $\overline{\text{ALERTx}}$ pins require an external pullup resistor to an external supply. The external supply for the pullup voltage can exceed the supply voltage, V_S, but is restricted from operating above 5.5 V. The pullup resistance is selected based on the capacitive load and required rise time; however, a 10-kΩ resistor value is typically sufficient for most applications. The response time of the $\overline{\text{ALERT1}}$ output to an out-of-range event is less than 1 µs, and the response time of the $\overline{\text{ALERT2}}$ output is proportional to the value of the external C_{DELAY} capacitor. The equation to calculate the delay time for the $\overline{\text{ALERT2}}$ output is given in 公式 2:

$$t_{DELAY} = \begin{cases} 1.5\ \mu s & \text{If DELAY is connected to VS with 100 k}\Omega \\ \dfrac{C_{DELAY} \times V_{TH}}{I_D} + 2.5\ \mu s & \text{If } C_{DELAY} \geq 47\ pF \end{cases}$$

where,

- C_{DELAY} is the external delay capacitor
- V_{TH} is the delay threshold voltage and
- I_D is the DELAY pin current for comparator 2 (2)

For example, if a delay time of 10 µs is desired, the calculated value for C_{DELAY} is 492 pF. The closest standard capacitor value to the calculated value is 500 pF. If a delay time greater than 2.5 µs on the $\overline{\text{ALERT2}}$ output is not needed, the C_{DELAY} capacitor can be omitted. To achieve minimum delay on the $\overline{\text{ALERT2}}$ output, connecting a 100-kΩ resistor from the DELAY pin to the VS pin is recommended. Both comparators in the INA30x have hysteresis to avoid oscillations in the $\overline{\text{ALERTx}}$ outputs. The effect hysteresis has on the comparator behavior is described in the *Hysteresis* section.

Feature Description (接下页)

图 42 shows the alert output response of the internal comparators for the INA302. When the output voltage of the current-sense amplifier is lower than the voltage developed on either limit pin, both ALERTx outputs are in the default high state. When the current sense amplifier output is greater than the threshold voltage set by the LIMIT2 pin, the ALERT2 output pulls low after a delay time set by the external delay capacitor. The lower overcurrent threshold is commonly referred to as the *overcurrent warning threshold*. If the current continues to rise until the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin, then the ALERT1 output becomes active and immediately pulls low. The low voltage on ALERT1 indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent condition has occurred. The upper threshold is commonly referred to as the *fault* or *system critical threshold*. Systems often initiate protection procedures (such as a system shutdown) when the current exceeds this threshold.

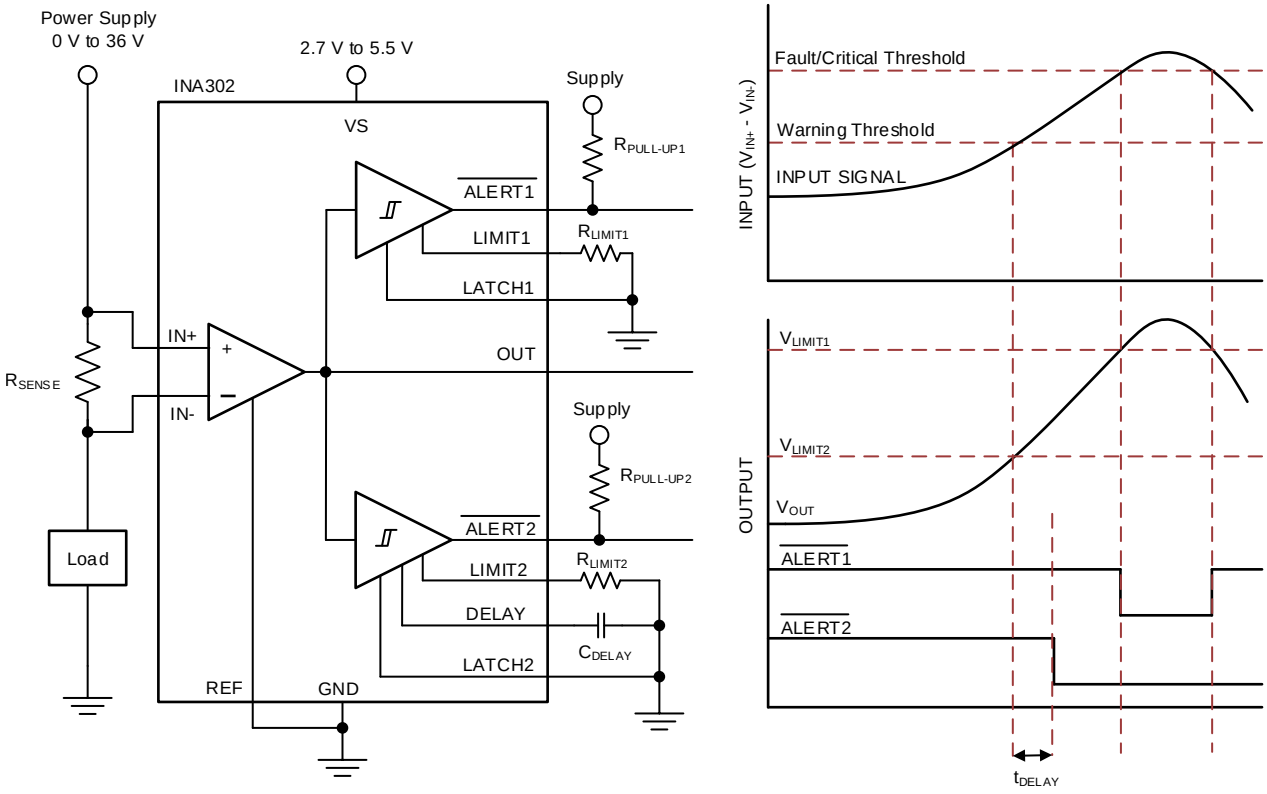


图 42. Out-of-Range Alert Responses for the INA302

Feature Description (接下页)

图 43 shows the alert output response of the internal comparators for the INA303. Both $\overline{\text{ALERT}}$x outputs are in the default high state when the output voltage of the current-sense amplifier is lower than the voltage developed at the LIMIT1 pin and is greater than the voltage developed at the LIMIT2 pin. The $\overline{\text{ALERT1}}$ output becomes active and pulls low when the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin. The low voltage on $\overline{\text{ALERT1}}$ indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred. When the current-sense amplifier output is less than the threshold voltage set by the LIMIT2 pin, the $\overline{\text{ALERT2}}$ output pulls low after the delay time set by the external delay capacitor expires. The delay time for the $\overline{\text{ALERT2}}$ output is proportional to the value of the external C_{DELAY} capacitor and can be calculated by 公式 2.

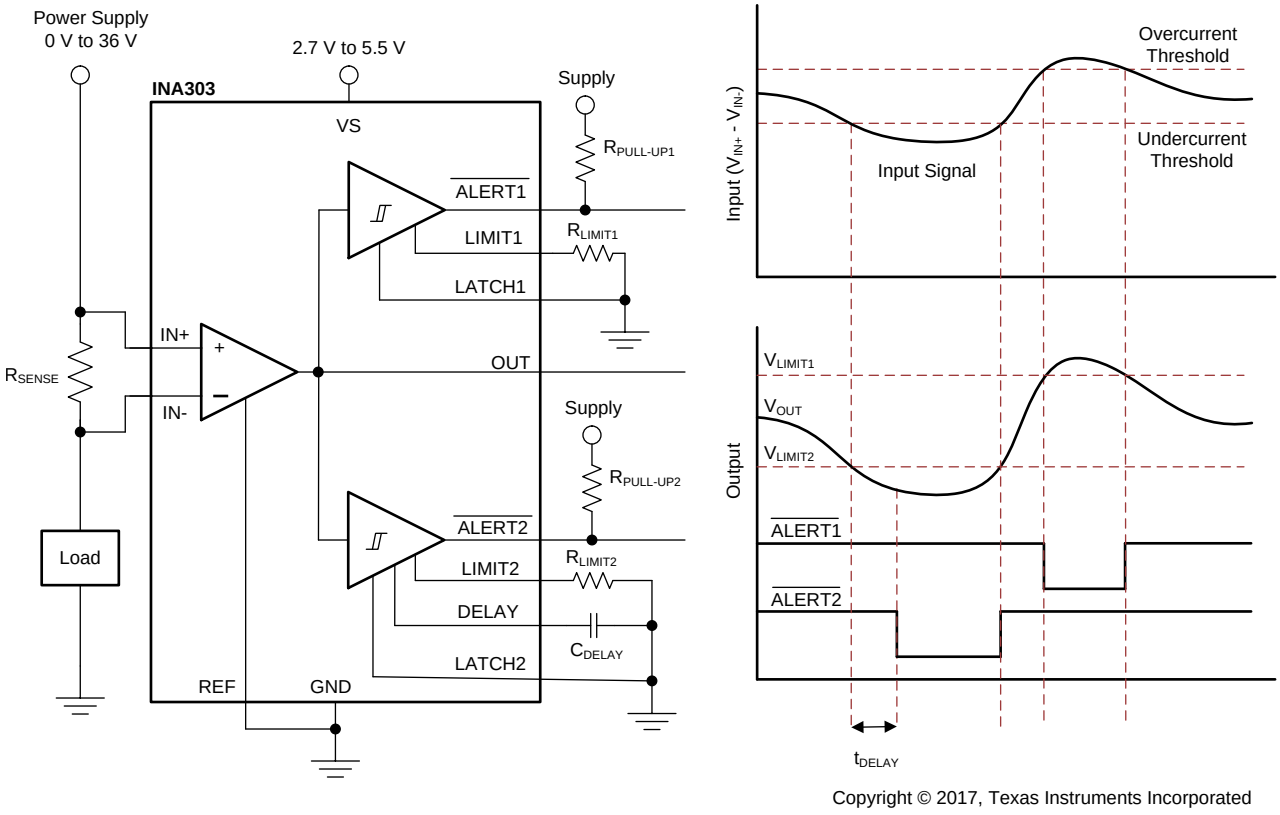


图 43. Out-of-Range Alert Responses for the INA303

Feature Description (接下页)

图 44 shows the alert output response of the INA303 when the two $\overline{\text{ALERT}}$x pins are connected together. When configured in this manner, the INA303 can provide a single signal to indicate when the sensed current is operating either outside the normal operating bands or within a normal operational window. Both $\overline{\text{ALERT1}}$ and $\overline{\text{ALERT2}}$ outputs behave the same in regard to the alert mode. The difference with $\overline{\text{ALERT2}}$ is that the transition of the output state is delayed by the time set by the external delay capacitor. If the over- or undercurrent event is not present when the delay time expires, $\overline{\text{ALERT2}}$ does not respond.

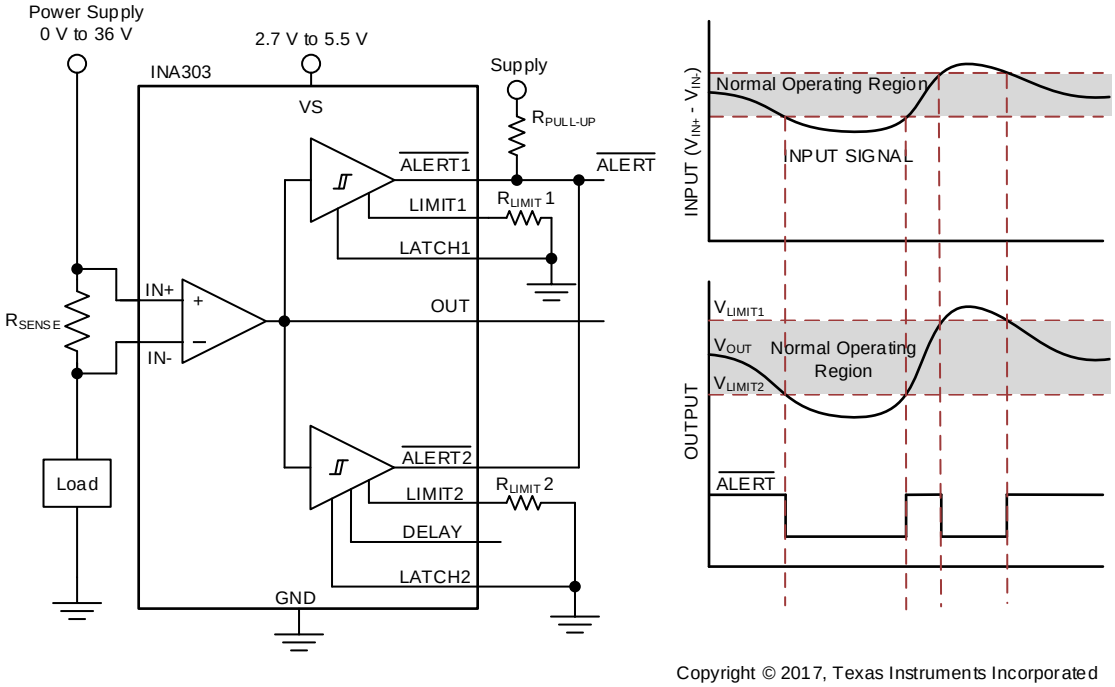


图 44. Current Window Comparator Implementation with the INA303

7.3.3 Alert Operating Mode

Each comparator has two output operating modes (transparent and latched) that are selected based on how the LATCHx pins are connected. These modes determine how the $\overline{\text{ALERT}}$x pins respond when an out-of-range condition is removed.

7.3.3.1 Transparent Output Mode

The comparators are set to transparent mode when the corresponding LATCHx pin is pulled low. When set to the transparent state, the output of the comparators changes and follows the input signal with respect to the programmed alert threshold. For example, when the amplifier output violates the set limit value, the $\overline{\text{ALERT}}$x output pin is pulled low. As soon as the differential input signal drops below the alert threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the $\overline{\text{ALERT}}$x pins to a hardware interrupt input on a microcontroller. The $\overline{\text{ALERT}}$x pin is pulled low as soon as an out-of-range condition is detected, notifying the microcontroller of the out-of-range condition. The microcontroller begins taking action to address the overcurrent condition because the microcontroller immediately reacts to the alert. There is no need to latch the state of the alert output in this mode of operation because the microcontroller responds as soon as the out-of-range condition occurs.

Feature Description (接下页)

7.3.3.2 Latch Output Mode

Some applications do not have the ability to continuously monitor the state of the ALERTx pins as described in the *Transparent Output Mode* section. A typical example of this application is a system that is only able to poll the state of the ALERTx pins periodically. If the device is set to transparent mode in this type of application, then the transition of the ALERTx pins can be missed if the out-of-range condition is not present during one of these periodic polling events. Latch mode allows the output of the comparators to latch the output of the range condition so that the transition of the ALERTx pins is not missed when the status of the comparator ALERTx pins is polled.

The device is placed into either transparent or latched state based on the voltage applied to the corresponding LATCHx pin, as shown in 表 1. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent condition is removed. In transparent mode (LATCH1, LATCH2 = low), when the differential input signal drops to within normal operating range, the ALERTx pin returns to the default high setting to indicate that the overcurrent event has ended.

表 1. Output Mode Settings

OUTPUT MODE	LATCHx PINS SETTINGS
ALERTx transparent mode	LATCHx = low
ALERTx latch mode	LATCHx = high

In latch mode (LATCHx = high), when an out-of-range condition is detected and the corresponding ALERTx pin is pulled low; the ALERTx pin does not return to the default high state when the out-of-range condition is removed. In order to clear the alert, the corresponding LATCHx pin must be pulled low for at least 100 ns. Pulling the LATCHx pins low allows the corresponding ALERTx pin to return to the default high level, provided the out-of-range condition is no longer present. If the out-of-range condition is still present when the LATCHx pins are pulled low, then the corresponding ALERTx pin remains low. The ALERTx pins can be cleared (reset to high) by toggling the corresponding LATCHx pin when the alert condition is detected by the system controller.

The latch and transparent modes are illustrated in 图 45. As illustrated in this figure, at time t_1 the current-sense amplifier exceeds the limit threshold. During this time the LATCH1 pin is toggled with no affect to the ALERT1 output. The state of the LATCH1 pin only matters when the output of the current-sense amplifier returns to the normal operating region, as shown at t_2. At this time the LATCH1 pin is high and the overcurrent condition is latched on the ALERT1 output. As shown in the time interval between t_2 and t_3, the latch condition is cleared when the LATCHx pin is pulled low. At time t_4, the LATCH1 pin is already pulled low when the amplifier output drops below the limit threshold for the second time. The device is set to transparent mode at this point and the ALERT1 pin is pulled back high as soon as the output of the current-sense amplifier drops below the alert threshold.

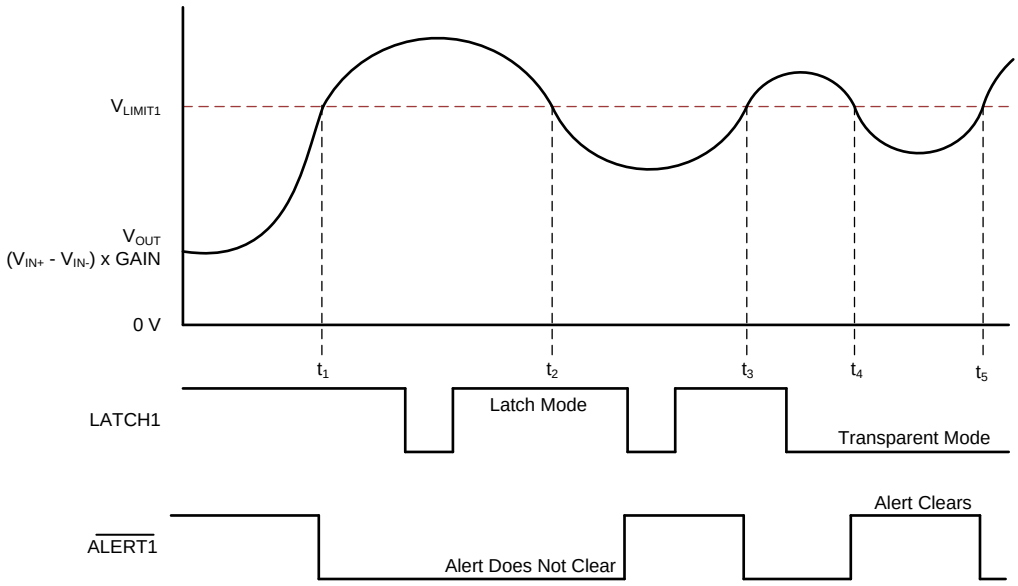


图 45. Transparent versus Latch Mode

7.3.4 Setting Alert Thresholds

The INA30x family of devices determines if an out-of-range event is present by comparing the amplifier output voltage to the voltage at the corresponding LIMITx pin. The threshold voltage for the LIMITx pins can be set using a single external resistor or by connecting an external voltage source to each pin. The INA302 allows setting limits for two overcurrent conditions. Generally, the lower overcurrent threshold is referred to as a *warning limit* and the higher overcurrent threshold is referred to as the *critical* or *fault limit*. The INA303 allows setting thresholds to detect both under- and overcurrent limit conditions.

7.3.4.1 Resistor-Controlled Current Limit

The typical approach to set the limit threshold voltage is to connect resistors from the two LIMITx pins to ground. The voltage developed across the R_{LIMIT1}, R_{LIMIT2} resistors represents the desired fault current value at which the corresponding $\overline{ALERT}$x pin becomes active. The values for the R_{LIMIT1}, R_{LIMIT2} resistors can be calculated using 公式 3:

$$R_{LIMIT} = \frac{\left(I_{TRIP} \times R_{SENSE} \times GAIN\right) + V_{REF}}{I_{LIMIT}} \quad (3)$$

where,

- I_{TRIP} is the desired out-of-range current threshold
- R_{SENSE} is the current-sensing resistor
- GAIN is the gain option of the device selected
- V_{REF} is the voltage applied to the REF pin
- I_{LIMIT} is the limit threshold output current for the selected comparator, typically 80 µA

注

When solving for the value of R_{LIMIT}, the voltage at the corresponding LIMITx pin as determined by the product of R_{LIMIT} and I_{LIMIT} must not exceed the compliance voltage of VS – 0.6 V.

7.3.4.1.1 Resistor-Controlled Current Limit: Example

For example, if the current level indicating an out-of-range condition (I_{TRIP}) is 20 A and the current-sense resistor value (R_{SENSE}) is 10 mΩ, then the input threshold signal is 200 mV. The INA302A1 has a gain of 20, so the resulting output voltage at the 20-A input condition is 4 V at the output of the current-sense amplifier when the REF pin is grounded. The value for R_{LIMIT} is selected to allow the device to detect this 20-A threshold, indicating that an overcurrent event has occurred. When the INA302 detects this out-of-range condition, the $\overline{ALERT}$x pin asserts and pulls low. For this example, the value of R_{LIMIT} to detect a 4-V level is calculated to be 50 kΩ.

7.3.4.2 Voltage-Source-Controlled Current Limit

The second method for setting the out-of-range threshold is to directly drive the LIMITx pins with a programmable DAC or other external voltage source. The benefit of this method is the ability to adjust the current-limit threshold to account for different threshold voltages used for different system operating conditions. For example, this method can be used in a system with one current-limit threshold level that must be monitored during a power-up sequence but different threshold levels must be monitored during other system operating modes.

The voltage applied at the LIMITx pins sets the threshold voltage for out-of-range detection. The value of the voltage for a given desired current trip point can be calculated using 公式 4:

$$V_{SOURCE} = \left(I_{TRIP} \times R_{SENSE} \times GAIN\right) + V_{REF} \quad (4)$$

where,

- I_{TRIP} is the desired out-of-range current threshold
- R_{SENSE} is the current-sensing resistor
- GAIN is the gain option of the device selected
- V_{REF} is the voltage applied to the REF pin

注

The maximum voltage that can be applied to the LIMIT2 pin is VS – 0.6 V and the maximum voltage that can be applied to the LIMIT1 pin must not exceed VS.

7.3.5 Selecting a Current-Sensing Resistor (R_{SENSE})

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through the use of larger input signals for improving measurement accuracy. Increasing the current-sense resistor value results in an increase in power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down as low as 200 μΩ or lower with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

7.3.5.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 2.5% accuracy for detecting a 10-A overcurrent event where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit-setting resistor (R_{LIMIT}) is a 1% component and the maximum tolerance specification for the internal threshold setting current source (1%) is used. Given the total error budget of 2.5%, up to 0.5% of error can be attributed to the measurement error of the device under these conditions.

As shown in 表 2, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and to further reduce power dissipation. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and stays within the accuracy region.

表 2. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
DESIGN TARGETS				
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
	Allowable current threshold accuracy		2.5%	
DEVICE PARAMETERS				
V_{OS}	Offset voltage		30	µV
E_G	Gain error		0.15%	
CALCULATIONS				
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE\_MAX} \times I_{MAX}) \times 100$	0.12%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS\_ERROR}^2 + E_G^2)}$	0.19%	
$ERROR_{INITIAL}$	Initial threshold error	I_{LIMIT} tolerance + R_{LIMIT} tolerance	2%	
$ERROR_{AVAILABLE}$	Maximum allowable measurement error	Maximum error – $ERROR_{INITIAL}$	1%	
$V_{OS\_ERROR\_MAX}$	Maximum allowable offset error	$\sqrt{(ERROR_{AVAILABLE}^2 - E_G^2)}$	0.48%	
V_{DIFF_MIN}	Minimum differential voltage	$V_{OS} / V_{OS\_ERROR\_MAX\ (1\%)}$	6.3	mV
R_{SENSE_MIN}	Minimum sense resistor value	V_{DIFF_MIN} / I_{MAX}	0.63	mΩ
P_{D_MIN}	Lowest-possible power dissipation	$R_{SENSE\_MIN} \times I_{MAX}^2$	63	mW

7.3.6 Hysteresis

The hysteresis included in the comparators of the INA302 and INA303 reduces the possibility of oscillations in the alert outputs when the measured signal level is near the overlimit threshold level. For overrange events, the corresponding ALERTx pin is asserted when the output voltage (V_{OUT}) exceeds the threshold set at either LIMITx pin. The output voltage must drop below the LIMITx pin threshold voltage by the hysteresis value in order for the ALERTx pin to deassert and return to the nominal high state. Likewise for underrange events, the corresponding ALERTx pin is also pulled low when the output voltage drops below the threshold set by either LIMITx pin. The ALERTx pin is released when the output voltage of the current-sense amplifier rises above the set threshold plus hysteresis. Hysteresis functionality for both over- and underrange events is shown in 图 46 and 图 47 for the INA302 and INA303, respectively.

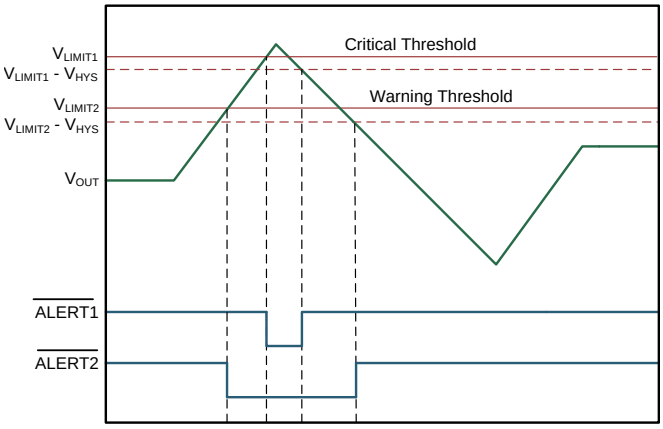


图 46. Comparator Hysteresis Behavior (INA302)

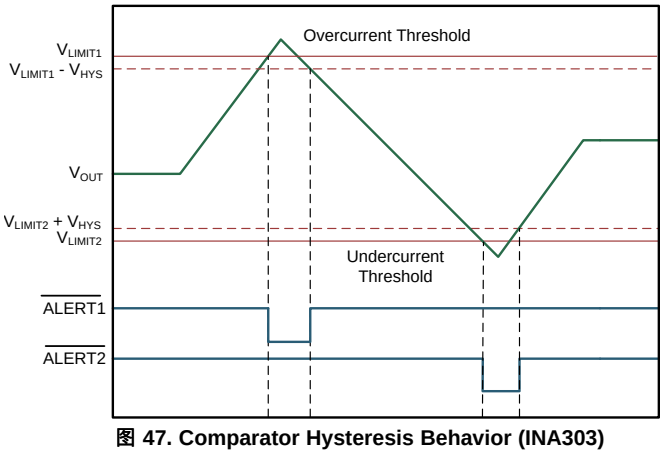


图 47. Comparator Hysteresis Behavior (INA303)

7.4 Device Functional Modes

7.4.1 Input Filtering

The integrated comparators in the INA302 and INA303 are very accurate in detecting out-of-range events because of their low offset voltage; however, noise present at the input of the current-sense amplifier and noise internal to the device can make the offset appear larger than specified. The most obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily falsely interpret this transient as an overrange condition.

Device Functional Modes (接下页)

External filtering can help reduce the amount of noise that reaches the comparator and reduce the likelihood of a false alert from occurring because of external noise. The tradeoff to adding this noise filter is that the alert response time is increased because the input signal and the noise are filtered. 图 48 shows the implementation of an input filter for the device.

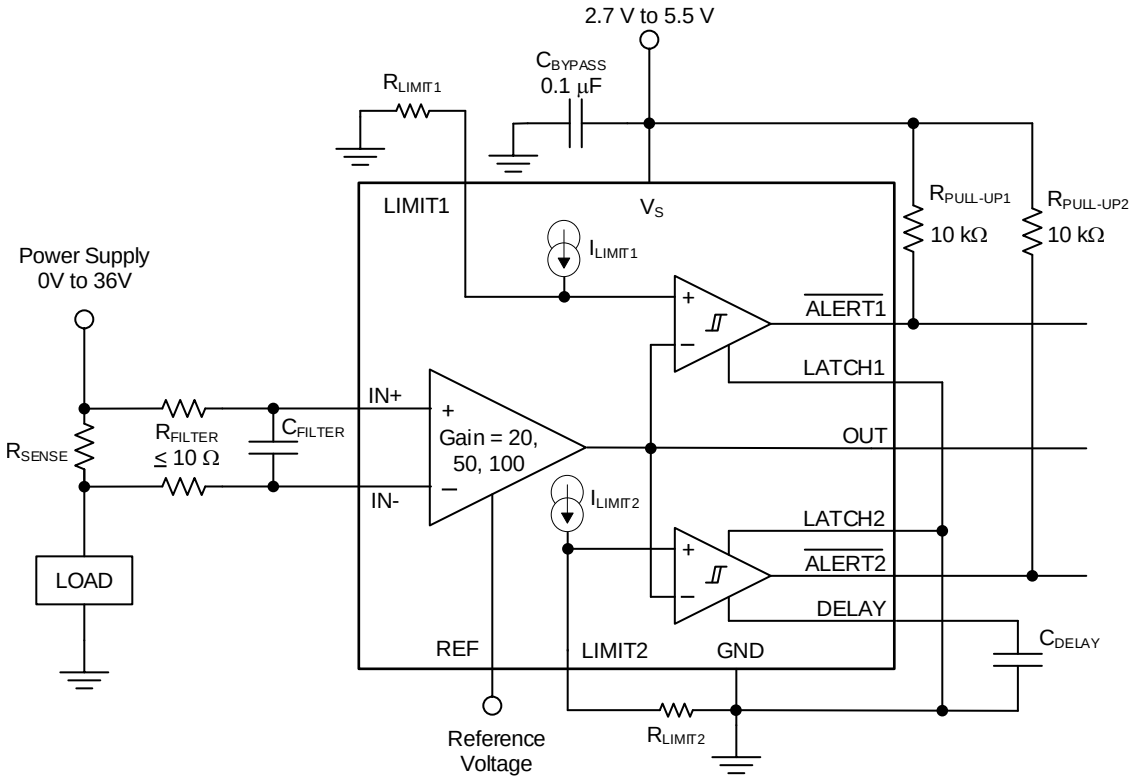


图 48. Input Filter Implementation

Limiting the amount of input resistance used in this filter is important because this resistance can have a significant effect on the input signal that reaches the device input pins by adversely affecting the gain error of the device. A typical system implementation involves placing the current-sensing resistor very near the device so the traces are very short and the trace impedance is very small. This layout helps reduce coupling of additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal effect on device performance.

Device Functional Modes (接下页)

As shown in 图 49, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device that allows common-mode input voltages to far exceed the device supply voltage range. When input filter resistors are placed in series with the unequal input bias currents, unequal voltage drops are developed across the input resistors. The difference between these two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input pins. Smaller-value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

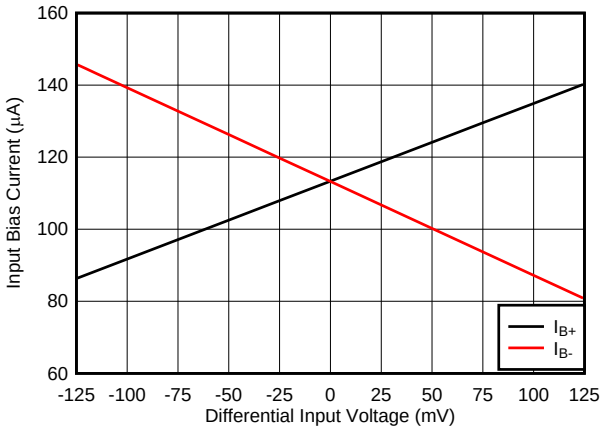
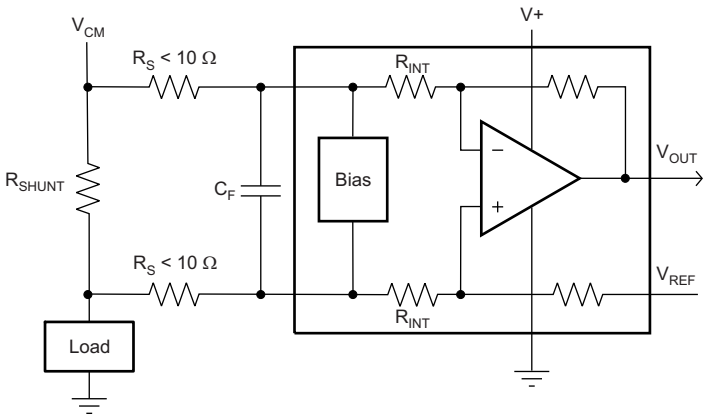


图 49. Input Bias Current vs Differential Input Voltage

The internal bias network shown in 图 50 present at the input pins is responsible for the mismatch in input bias currents that is shown in 图 49. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using 公式 6 where the gain error factor is calculated using 公式 5.



NOTE: Comparators omitted for simplicity.

图 50. Filter at Input Pins

Device Functional Modes (接下页)

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as illustrated in 图 50). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in 公式 5:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (5)$$

where:

- R_{INT} is the internal input resistor (R3 and R4), and
- R_S is the external series resistance.

With the adjustment factor from 公式 5, including the device internal input resistance, this factor varies with each gain version, as shown in 表 3. Each individual device gain error factor is shown in 表 4.

表 3. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA30xA1	20	12.5
INA30xA2	50	5
INA30xA3	100	2.5

表 4. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA30xA1	$\frac{12{,}500}{(11 \times R_S) + 12{,}500}$
INA30xA2	$\frac{1000}{R_S + 1000}$
INA30xA3	$\frac{2500}{(3 \times R_S) + 2500}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on 公式 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

For example, using an INA302A2 and the corresponding gain error equation from 表 4, a series resistance of 10 Ω results in a gain error factor of 0.99. The corresponding gain error is then calculated using 公式 6, resulting in a gain error of approximately 1% solely because of the external 10-Ω series resistors.

7.4.2 Using The INA30x With Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in 图 51, as a working impedance for the zener diode. Keeping these resistors as small as possible is best, preferably 10 Ω or less. Larger values can be used with an additional induced error resulting from a reduced signal that actually reaches the device input pins. Many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating available because this circuit limits only short-term transients. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

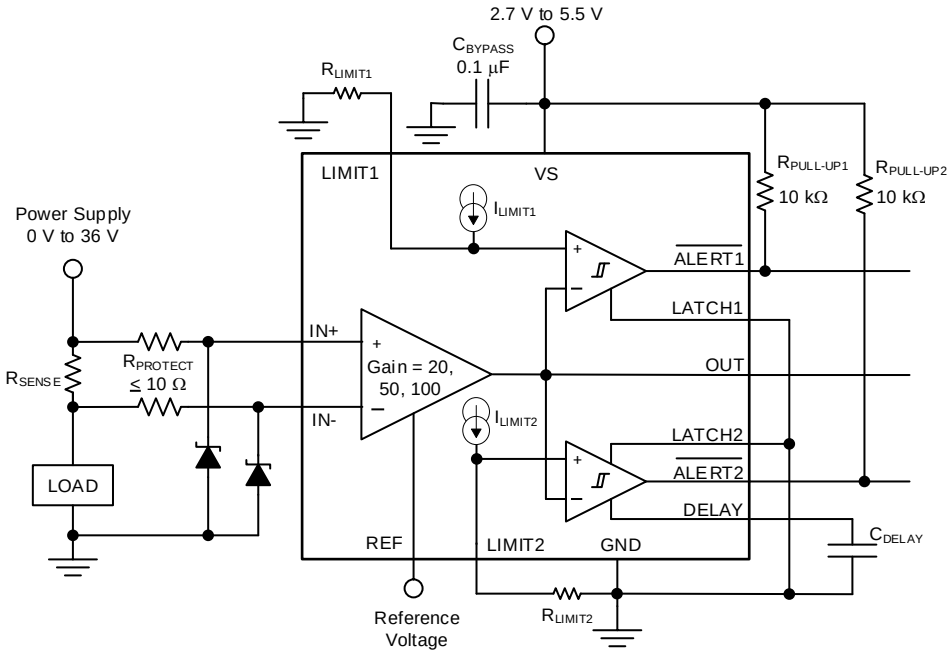


图 51. Transient Protection

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA302 and INA303 are designed to be easily configured for detecting multiple out-of-range current conditions in an application. This device is capable of monitoring and providing overcurrent detection of bidirectional currents. By using the REF pin of the INA303, both positive and negative overcurrent events can be detected.

8.2 Typical Application

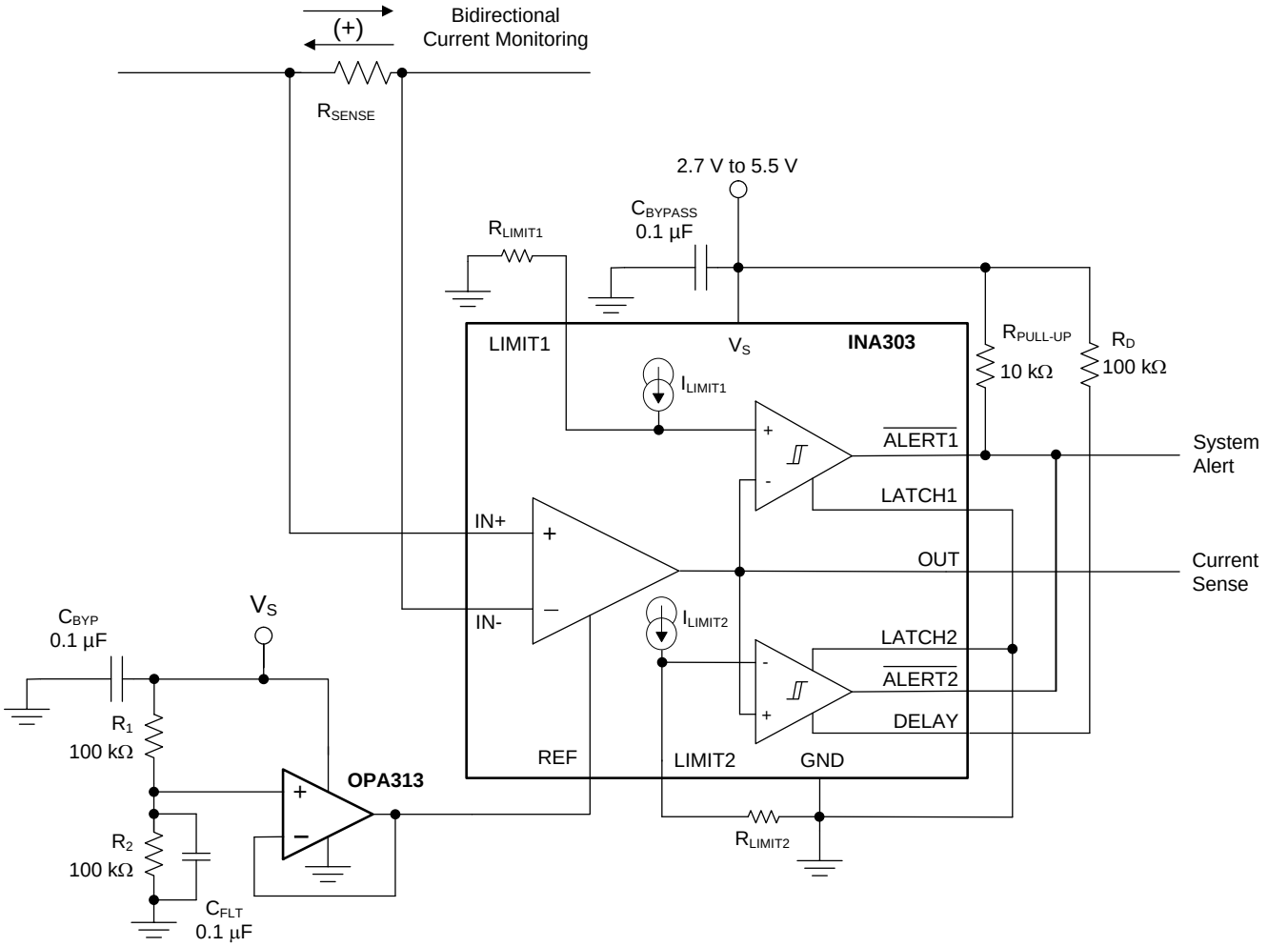


图 52. Bidirectional Application

Typical Application (接下页)

8.2.1 Design Requirements

To allow for bidirectional monitoring, the INA303 requires a voltage applied to the REF pin. A voltage that is half of the supply voltage is usually preferred to allow for maximum output swing in both the positive and negative current direction. To reduce the errors in the reference voltage, drive the REF pin with a low-impedance source (such as an operational amplifier (op-amp) or external reference). A low-value resistor divider can be used at the expense of quiescent current and accuracy. For this design a single alert output is preferred, so both $\overline{\text{ALERT1}}$ and $\overline{\text{ALERT2}}$ are connected together and use a single pullup resistor.

8.2.2 Detailed Design Procedure

To achieve bidirectional monitoring, the reference pin is driven half way between the supply with a resistor divider buffered by an op-amp, as shown in 表 5. To reduce the current draw from the supply, 100-kΩ resistors were used to create the divide-by-two voltage divider. The OPA313 was selected to buffer the voltage divider because this device can operate from a single-supply rail with low IQ and offset voltage. To minimize the response time of the $\overline{\text{ALERT2}}$ output, a 100-kΩ pullup resistor was added from the DELAY pin to the VS pin. Select values for R_{SENSE}, R_{LIMIT2}, and R_{LIMIT1} based on the desired current-sense levels and trip thresholds using the information in the *Resistor-Controlled Current Limit* and *Selecting a Current-Sensing Resistor (R_{SENSE})* sections. For this example, the values of R_{LIMIT1} and R_{LIMIT2} were selected such that the positive and negative overcurrent thresholds are the same. 表 5 shows the alert output of the INA303 application circuit with the capability to detect both positive and negative overcurrent conditions.

表 5. Bidirectional Overcurrent Output Status

OVERCURRENT PROTECTION (OCP) STATUS	OUTPUT
Positive overcurrent detection (OCP+)	0
Negative overcurrent detection (OCP–)	0
Normal operation (no OCP)	1

8.2.3 Application Curve

图 53 shows the INA303 device being used in a bidirectional configuration to detect both negative and positive overcurrent events.

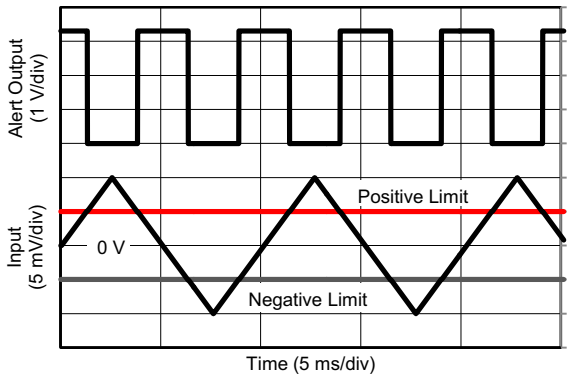


图 53. Bidirectional Application Curve

9 Power Supply Recommendations

The device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 36 V. At power-up, for applications where the common-mode voltage (V_{CM}) slew rate is greater than 6 V/µs with a final common-mode voltage greater than 20 V, the V_S supply is recommended to be present before V_{CM}. If the use case requires V_{CM} to be present before V_S with V_{CM} under these same slewing conditions, then a 331-Ω resistor must be added between the V_S supply and the VS pin bypass capacitor.

Power-supply bypass capacitors are required for stability and must be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

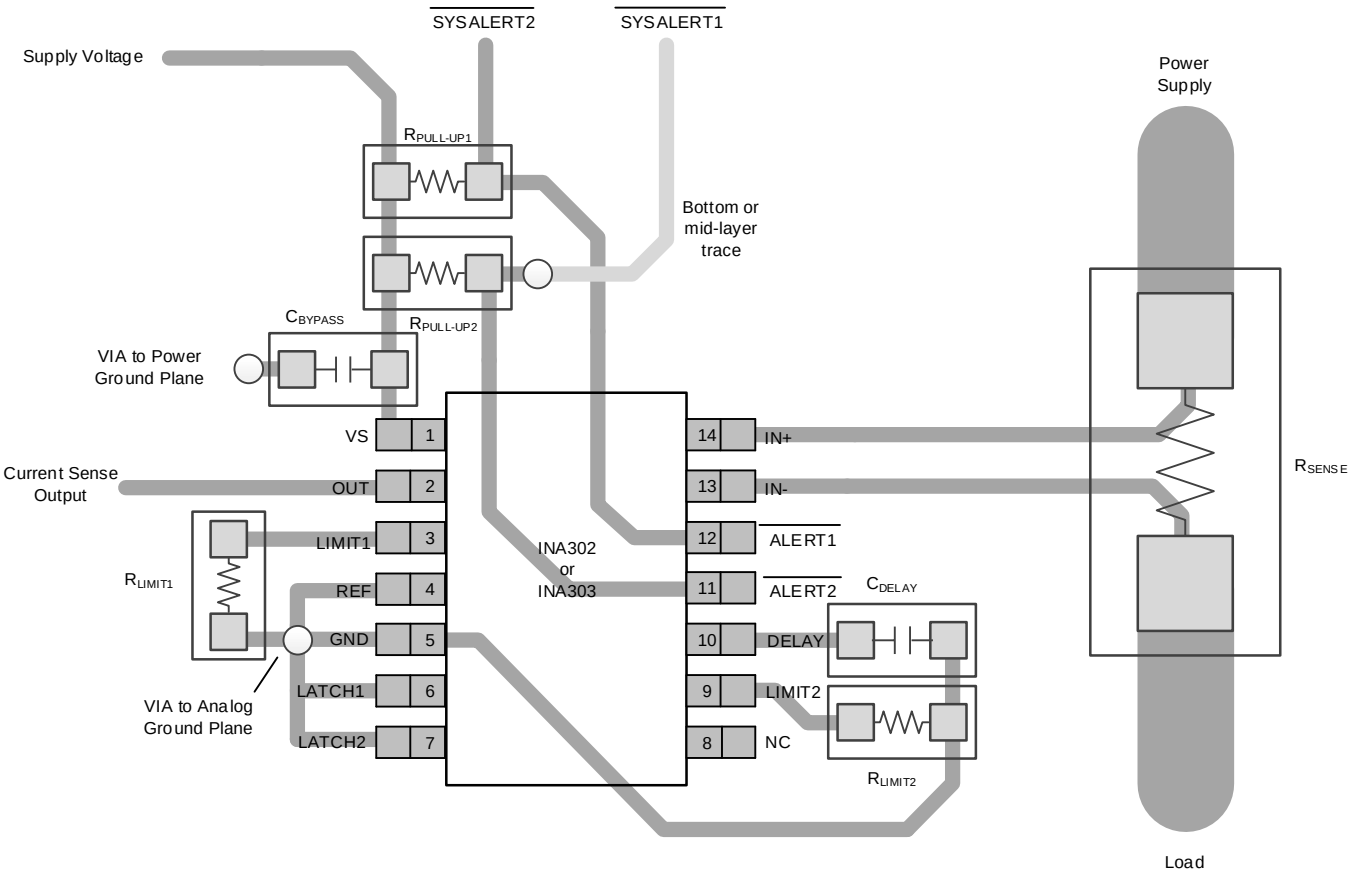
During slow power-up events, current flow through the sense resistor or voltage applied to the REF pin can result in the output voltage momentarily exceeding the voltage at the LIMITx pins, resulting in an erroneous indication of an out-of-range event on the ALERTx output. When powering the device with a slow ramping power rail where an input signal is already present, all alert indications should be disregarded until the supply voltage has reached the final value.

10 Layout

10.1 Layout Guidelines

- Apply connections to the current-sense resistor, R_{SENSE}, on the inside of the resistor pads to avoid additional voltage losses incurred by the high current traces to the resistor. Route the traces from the current-sense resistor symmetrically and side-by-side back to the input of the INA to minimize common-mode errors and noise pickup.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Make the connection of R_{LIMIT} to the ground pin as direct as possible to limit additional capacitance on this node. Routing this connection must be limited to the same plane if possible to avoid vias to internal planes. If the routing can not be made on the same plane and must pass through vias, ensure that a path is routed from R_{LIMIT} back to the ground pin and that R_{LIMIT} is not simply connected directly to a ground plane.
- Routing to the delay capacitor must be short and direct. Keep the routing trace from the DELAY pin to the delay capacitor away from the ALERT2 trace (or any other noisy signals) to minimize any coupling effects. If no delay capacitor is used do not have any connection to the DELAY pin. Long trace lengths on the DELAY pin can cause noise to couple to the device, resulting in false trips.
- The open-drain output pins are recommended to be pulled up to the supply voltage rail through a 10-kΩ pullup resistor.

10.2 Layout Example



NOTE: Connect the limit resistors and delay capacitors directly to the GND pin; leave the DELAY pin unconnected or connected to VS through a pullup resistor if no delay is needed.

图 54. Recommended Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参阅以下部分：

- *《OPAx313 1 MHz、微功耗、低噪声、RRIO、1.8V CMOS 运算放大器精密超值系列》*
- *《监测电流以识别多种超出范围的状况》*

11.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可通过快速访问立刻订购。

表 6. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
INA302	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
INA303	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA302A1IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1	Samples
INA302A1IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1	Samples
INA302A2IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2	Samples
INA302A2IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2	Samples
INA302A3IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3	Samples
INA302A3IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3	Samples
INA303A1IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1	Samples
INA303A1IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1	Samples
INA303A2IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2	Samples
INA303A2IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2	Samples
INA303A3IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3	Samples
INA303A3IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

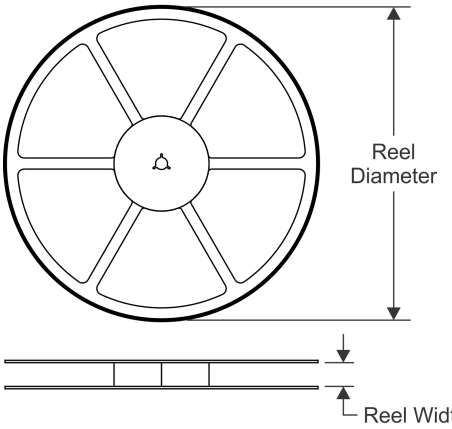
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

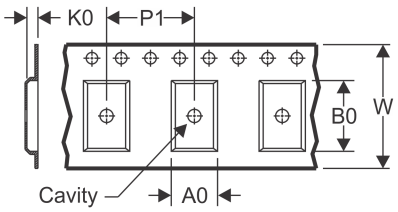
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

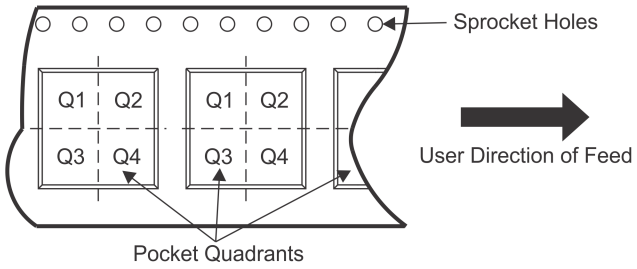


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

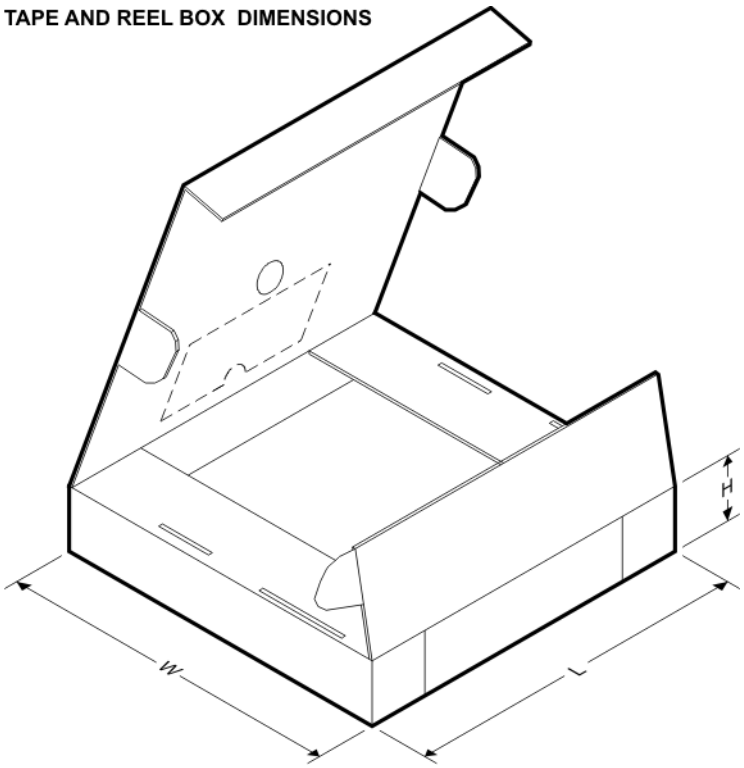
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA302A1IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA302A2IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA302A3IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A1IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A2IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A3IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

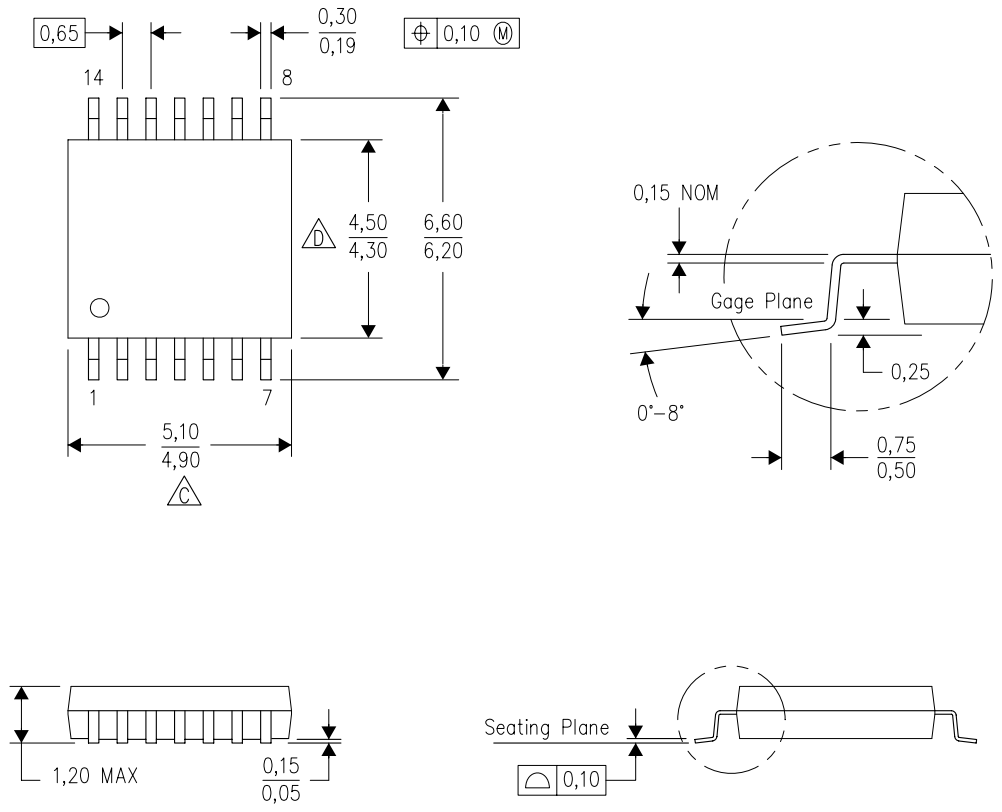
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA302A1IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA302A2IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA302A3IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA303A1IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA303A2IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA303A3IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

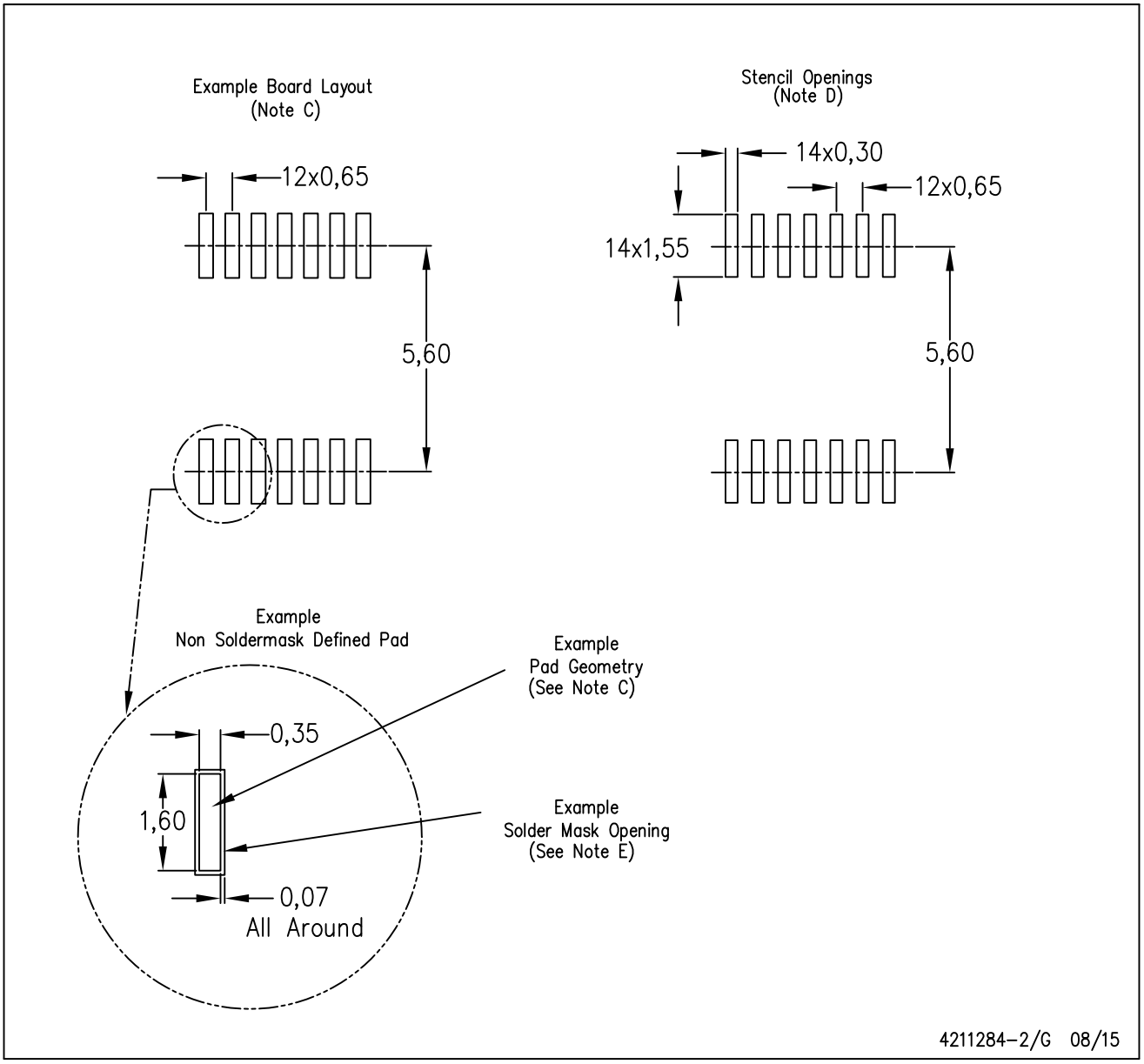
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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