bq25505 Ultra Low-Power Boost Charger With Battery Management and Autonomous Power Multiplexer for Primary Battery in Energy Harvester Applications

1 Features

- Ultra Low-Power With High-Efficiency DC-DC Boost Charger
  - Cold-Start Voltage: V_{IN} ≥ 330 mV
  - Continuous Energy Harvesting From Input Sources as Low as 100 mV
  - Ultra-Low Quiescent Current of 325 nA
  - Input Voltage Regulation Prevents Collapsing High-Impedance Input Sources
  - Ship Mode With < 5 nA From Battery
- Energy Storage
  - Energy can be Stored to Rechargeable Li-Ion Batteries, Thin-Film Batteries, Super-Capacitors, or Conventional Capacitors
- Battery Charging and Protection
  - Internally Set Undervoltage Level
  - User-Programmable Overvoltage Level
- Battery-Good Output Flag
  - Programmable Threshold and Hysteresis
  - Warn Attached Microcontrollers of Pending Loss of Power
  - Can be Used to Enable or Disable System Loads
- Programmable Maximum Power Point Tracking (MPPT)
  - Integrated MPPT for Optimal Energy Extraction From a Variety of Energy Harvesters
- Gate Drivers for Primary (Nonrechargeable) and Secondary (Rechargeable) Storage Element Multiplexing
  - Autonomous Switching Based on VBAT_OK
  - Break-Before-Make Prevents System Rail Droop

2 Applications

- Energy Harvesting
- Solar Chargers
- Thermal Electric Generator (TEG) Harvesting
- Wireless Sensor Networks (WSN)
- Industrial Monitoring
- Environmental Monitoring
- Bridge and Structural Health Monitoring (SHM)
- Smart Building Controls
- Portable and Wearable Health Devices
- Entertainment System Remote Controls

3 Description

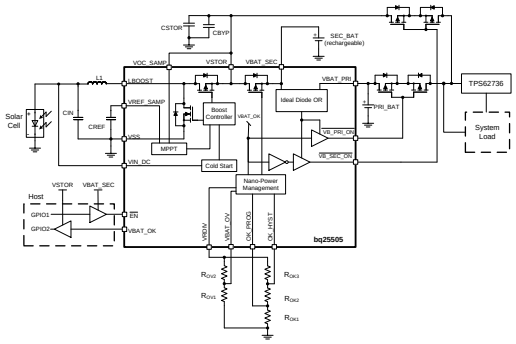
The bq25505 device is specifically designed to efficiently extract the microwatts (µW) to miliwatts (mW) of power generated from a variety of DC energy harvesting, high-impedance sources like photovoltaic (solar) or thermal electric generators (TEGs) without collapsing those sources. The battery-management features of the bq25505 ensure that a secondary rechargeable battery is not overcharged by this extracted power, with voltage boosted, nor depleted beyond safe limits by a system load. The integrated multiplexer gate drivers autonomously switch the system load to a primary nonrechargeable battery if the secondary battery voltage falls below the user-defined VBAT_OK threshold.

Device Information(1)

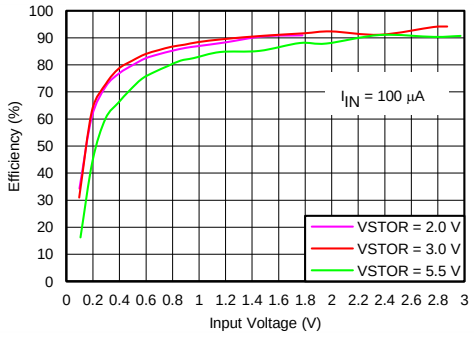
PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25505	VQFN (20)	3.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Charger Efficiency



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4 Revision History

Changes from Revision C (December 2014) to Revision D **Page**

- Moved the Storage temperature From: *ESD Ratings* to: *Absolute Maximum Ratings*(1) ... 5
- Changed the *Handling Ratings* to *ESD Ratings* ... 5
- Added clarification to PIN(CS) test condition in *Electrical Characteristics* table ... 6
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 21
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 24
- Added sentence in *Detailed Design Procedure* : "The rectifier diodes are Panasonic DB3X316F0L." ... 24
- Deleted the diode part numbers from Figure 34 ... 26
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 26
- Added text to *Detailed Design Procedure*, "The rectifier diodes are Panasonic DB3X316F0L" ... 26
- Changed Figure 40 ... 29

Changes from Revision B (January 2014) to Revision C **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable* Information section ... 1
- Changed the two paragraphs in the *Detailed Design Procedure* ... 24

Changes from Revision A (September 2013) to Revision B **Page**

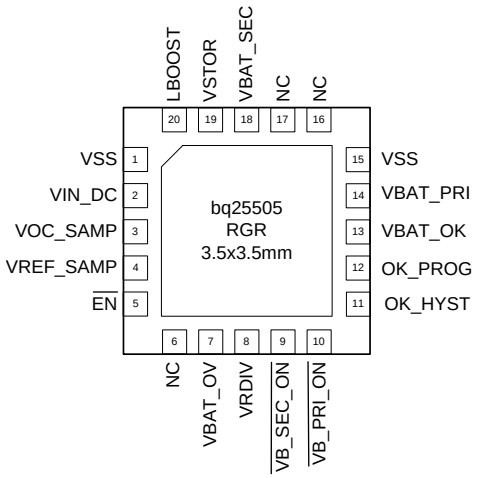
- Changed Feature: Continuous Energy Harvesting From Input Sources as low as 120 mV To: Continuous Energy Harvesting From Input Sources as low as 100 mV 1
- Changed Peak Input Power in the Absolute Maximum Ratings table From: MAX = 400 mW To: MAX = 510 mW 5
- Changed VIN(DC) in the Recommended Operating Conditions table From: MIN = 0.12 V MAX = 4 V To: MIN = 0.1 V MAX = 5.1 V 5
- Changed VINDC in the *Electrical Characteristics* table From: MIN = 120 MAX = 4000 mV To: MIN = 100 mV MAX = 5100 mV 6
- Changed PIN in the *Electrical Characteristics* table From: MAX = 400 mW To: MAX = 510 mW 6
- Added VDELTA, VBAT_OV - VIN(DC to the *Electrical Characteristics* table 7
- Changed VRDIV to VIN_DC. 11
- Changed "Refer to SLUC41 for a design example" To: "Refer to SLUC463 for a design example" in the Energy Harvester Selection section 18
- Changed "Refer to SLUC41 for a design example" To: "Refer to SLUC463 for a design example" in the Storage Element Selection section 19

Changes from Original (August 2013) to Revision A **Page**

- Changed from Product Preview to Production Data 1

5 Pin Configuration and Functions

RGT Package
20 Pins
Top View



Pin Functions

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
5	$\overline{\text{EN}}$	Input	Active low digital programming input for enabling/disabling the IC. Connect to GND to enable the IC.
20	LBOOST	Input	Inductor connection for the boost charger switching node. Connect a 22-µH inductor between this pin and pin 2 (VIN_DC).
6	NC	Input	Connect to VSS via the IC's PowerPad™.
16	NC	Input	Connect to ground using the IC's PowerPad.
17	NC	Input	Connect to ground using the IC's PowerPad.
11	OK_HYST	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK hysteresis threshold. If not used, connect this pin to GND.
12	OK_PROG	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK threshold. If not used, connect this pin to GND.
13	VBAT_OK	Output	Digital output for battery good indicator. Internally referenced to the VSTOR voltage. Leave floating if not used.
7	VBAT_OV		Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VSTOR = VBAT_SEC overvoltage threshold.
14	VBAT_PRI	Input	Primary (nonrechargeable) energy storage element HiZ sense input. Leave floating if not used.
18	VBAT_SEC	I/O	Connect a secondary (rechargeable) storage element with at least 100 µF of equivalent capacitance to this pin.
10	$\overline{\text{VB\_PRI\_ON}}$	Output	Active low push-pull driver for the primary (nonrechargeable) energy storage PMOS FET. Leave floating if not used.
9	$\overline{\text{VB\_SEC\_ON}}$	Output	Active low push-pull driver for the secondary (rechargeable) energy storage PMOS FET. Leave floating if not used.
2	VIN_DC	Input	DC voltage input from energy harvesters. Connect at least a 4.7-µF capacitor as close as possible between this pin and pin 1.
3	VOC_SAMP	Input	Sampling pin for MPPT network. Connect to VSTOR to sample at 80% of input soure open circuit voltage. Connect to GND for 50% or connect to the mid-point of external resistor divider between VIN_DC and GND.
4	VREF_SAMP	Input	Connect a 0.01-µF low-leakage capacitor from this pin to GND to store the voltage to which VIN_DC will be regulated. This voltage is provided by the MPPT sample circuit.
8	VRDIV	Output	Connect high side of resistor divider networks to this biasing voltage.
1	VSS	Input	General ground connection for the device
15	VSS	Supply	Signal ground connection for the device.
19	VSTOR	Output	Connection for the output of the boost charger, which is typically connected to the system load. Connect at least a 4.7-µF capacitor in parallel with a 0.1-µF capacitor as close as possible to between this pin and pin 1 (VSS).

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, $\overline{VB\_PRI\_ON}$, $\overline{VB\_SEC\_ON}$, VBAT_PRI, VBAT_SEC, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VSTOR, LBST(2)	–0.3	5.5	V
Peak Input Power, PIN_PK			510	mW
Operating junction temperature range, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}/ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VIN(DC)	DC input voltage into VIN_DC(1)	0.1		5.1	V
VBAT_SEC, VBAT_PRI	Battery voltage range(2)	2		5.5	V
CIN	Input capacitance	4.7			µF
CSTOR	Storage capacitance	4.7			µF
CBAT	Battery pin capacitance or equivalent battery capacity	100			µF
CREF	Sampled reference storage capacitance	9	10	11	nF
$R_{OC1} + R_{OC2}$	Total resistance for setting for MPPT reference.	18	20	22	MΩ
$R_{OK\ 1} + R_{OK\ 2} + R_{OK3}$	Total resistance for setting the VBAT_OK threshold voltage.	11	13	15	MΩ
$R_{OV1} + R_{OV2}$	Total resistance for setting VBAT_OV threshold voltage.	11	13	15	MΩ
L1	Input inductance	22			µH
T_J	Operating junction temperature	–40		105	°C

(1) Maximum input power ≤ 400 mW. Cold start has been completed
(2) VBAT_OV setting must be higher than VIN_DC

6.4 Thermal Information

THERMAL METRIC(1)		bq25505 RGR 20 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	34.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49.0	
θ_{JB}	Junction-to-board thermal resistance	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VSTOR = 4.2 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, CSTOR= 4.7 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CHARGER						
VIN(DC)	DC input voltage into VIN_DC	Cold-start completed	100		5100	mV
I-CHG(CBC_LIM)	Cycle-by-cycle current limit of charger	0.5V < V_{IN} < 4.0 V; VSTOR = 4.2 V		230	285	mA
PIN	Input power range for normal charging	VBAT_OV > VSTOR > VSTOR_CHGEN	0.005		510	mW
VIN(CS)	Minimum input voltage for cold start circuit to start charging VSTOR	VBAT_SEC < VBAT_UV; VSTOR = 0 V; 0°C < T_A < 85°C		330	400	mV
VSTOR_CHGEN	Voltage on VSTOR when cold start operation ends and normal charger operation commences		1.6	1.73	1.9	V
PIN(CS)	Minimum cold-start input power for VSTOR to reach $VSTOR_{(CHGEN)}$ and allow normal charging to commence	VSTOR < $VSTOR_{(CHGEN)}$and VIN_DC clamped to VIN(CS) by cold start circuit; VBAT with 100 µF ceramic capacitor		15		µW
$t_{BAT\_HOT\_PLUG}$	Time for which switch between VSTOR and VBAT_SEC closes when battery is hot plugged into VBAT_SEC	Battery resistance = 300 Ω, Battery voltage = 3.3V		50		ms
QUIESCENT and LEAKAGE CURRENTS						
I_Q	$\overline{EN}$ = GND - Full operating mode	VIN_DC = 0V; VSTOR = 2.1V; T_J = 25°C		325	400	nA
		VIN_DC = 0V; VSTOR = 2.1V; –40°C < T_J < 85°C			700	
	$\overline{EN}$ = VBAT_SEC - Ship mode	VBAT_SEC = VBAT_PRI = 2.1 V; T_J = 25°C; VSTOR = VIN_DC = 0 V		1	5	
		VBAT_SEC = VBAT_PRI = 2.1 V; –40°C < T_J < 85°C; VSTOR = VIN_DC = 0 V			20	
I-BATPRI(LEAK)	$\overline{EN}$ = VBAT_SEC - Ship mode	VBAT_PRI = VBAT_SEC = 2.1 V; T_J = 25°C; VIN_DC = 0 V; VSTOR floating		1	5	nA
		VBAT_PRI = VBAT_SEC = 2.1 V; –40°C < T_J < 85°C; VIN_DC = 0 V; VSTOR floating			20	nA
MOSFET RESISTANCES						
RDS(ON)-BAT	ON resistance of switch between VBAT_SEC and VSTOR	VBAT_SEC = 4.2 V		0.95	1.50	Ω
RDS(ON)_CHG	Charger low-side switch ON resistance	VBAT_SEC = 4.2 V		0.70	0.90	Ω
	Charger high-side switch ON resistance			2.30	3.00	Ω
	Charger low-side switch ON resistance	VBAT_SEC = 2.1 V		0.80	1.00	Ω
	Charger high-side switch ON resistance			3.70	4.80	Ω
f_{SW}	Maximum charger switching frequency			1.0		MHz
T_{TEMP_SD}	Junction temperature when charging is discontinued	VBAT_OV > VSTOR > 1.8V		125		°C

Electrical Characteristics (continued)

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VSTOR = 4.2 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, CSTOR= 4.7 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY MANAGEMENT						
VBAT_OV	Programmable voltage range for overvoltage threshold	VBAT_SEC increasing	2.2		5.5	V
VBAT_OV_HYST	Battery overvoltage hysteresis (internal)	VBAT_SEC decreasing; VBAT_OV = 5.25V		24	45	mV
VDELTA	VBAT_OV - VIN(DC)	Main boost charger on; MPPT not sampling VOC	400			mV
VBAT_UV	Undervoltage threshold	VBAT_SEC decreasing	1.91	1.95	2	V
VBAT_UV_HYST	Battery undervoltage hysteresis (internal)	VBAT_SEC increasing		15	32	mV
VBAT_OK_HYST	Programmable voltage range of digital signal indicating VSTOR (=VBAT_SEC) is OK	VBAT_SEC increasing	VBAT_UV		VBAT_ OV	V
VBAT_OK_PROG	Programmable voltage range of digital signal indicating VSTOR (=VBAT_SEC) is OK	VBAT_SEC decreasing	VBAT_UV		VBAT_OK_ HYST – 50	mV
VBAT_ACCURACY	Overall Accuracy for threshold values VBAT_OV, VBAT_OK	Selected resistors are 0.1% tolerance	-2%		2%	
VBAT_OK(H)	VBAT_OK (High) threshold voltage	Load = 10 µA			VSTOR – 200	mV
VBAT_OK(L)	VBAT_OK (Low) threshold voltage	Load = 10 µA			100	mV
ENABLE THRESHOLDS						
$\overline{EN}$(H)	Voltage for $\overline{EN}$ high setting. Relative to VBAT_SEC.	VBAT_SEC = 4.2V	VBAT_SEC – 0.2			V
$\overline{EN}$(L)	Voltage for $\overline{EN}$ low setting	VBAT_SEC = 4.2V			0.3	V
BIAS and MPPT CONTROL STAGE						
VOC_SAMPLE	Time period between two MPPT samples			16		s
VOC_STLG	Settling time for MPPT sample measurement of VIN_DC open circuit voltage	Device not switching		256		ms
VIN_REG	Regulation of VIN_DC during charging	0.5 V < VIN < 4 V; IIN(DC) = 10 mA			10%	
MPPT_80	Voltage on VOC_SAMP to set MPPT threshold to 0.80 of open circuit voltage of VIN_DC		VSTOR – 0.015			V
MPPT_50	Voltage on VOC_SAMP to set MPPT threshold to 0.50 of open circuit voltage of VIN_DC				15	mV
VBIAS	Internal reference for the programmable voltage thresholds	VSTOR ≥ VSTOR_CHGEN	1.205	1.21	1.217	V
MULTIPLEXER						
t_{DEAD}	Dead time between $\overline{VB\_SEC\_ON}$ and $\overline{VB\_PRI\_ON}$			5	8 (1)	us

(1) Specified by design.

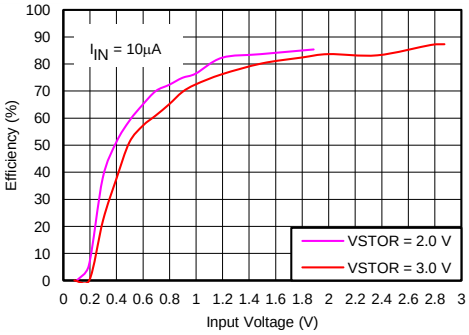
6.6 Typical Characteristics

Unless otherwise noted, graphs were taken using Figure 28 with CIN = 4.7 µF, L1 = Coilcraft 22 µH LPS4018, CSTOR = 4.7 µF, VBAT_OV = 5 V

Table 1. Table of Graphs

			FIGURE
Charger Efficiency (η)(1)	vs. Input Voltage	IN= 10 µA	Figure 1
		IN= 100 µA	Figure 2
		IIN = 10 mA	Figure 3
	vs. Input Current	VIN = 2.0 V	Figure 4
		VIN = 1.0 V	Figure 5
		VIN = 0.5 V	Figure 6
		VIN = 0.2 V	Figure 7
VBAT_SEC Quiescent Current	vs. VBAT_SEC Voltage	$\overline{EN}$ = VBAT_SEC (Active Mode)	Figure 8
		$\overline{EN}$ = GND (Ship Mode)	Figure 9
VBAT_PRI Leakage Current	vs. VBAT_PRI Voltage	$\overline{EN}$ = VBAT_SEC (Ship Mode)	Figure 10

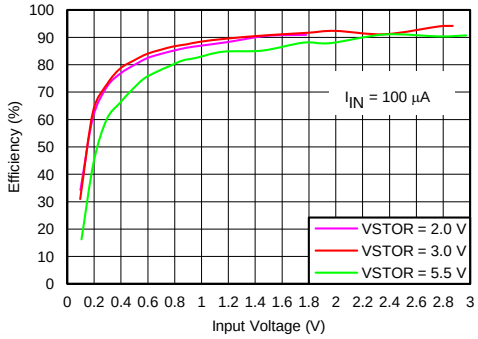
(1) See SLUA691 for an explanation on how to take these measurements. Because the MPPT feature cannot be disabled on the bq25505, these measurements need to be taken in the middle of the 16 s sampling period.



VIN_DC = Keithley Source Meter configured with I_{COMP} = 10 µA and outputing 0 to 3.0 V

VSTOR = Keithley Sourcemeter configured to measure current andvoltage source set to hold the VSTOR voltage = 2.0 V or 3.0 V

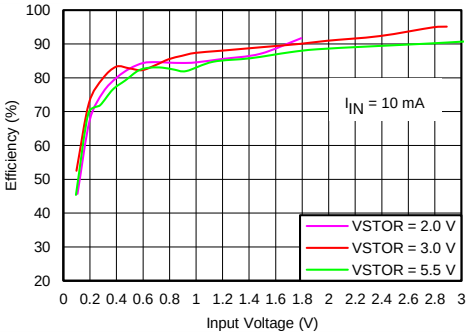
Figure 1. Charger Efficiency vs Input Voltage



VIN_DC = Keithley Source Meter configured with I_{COMP} = 100 µA and voltage source varied from 0.1 V to 3.0 V s

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

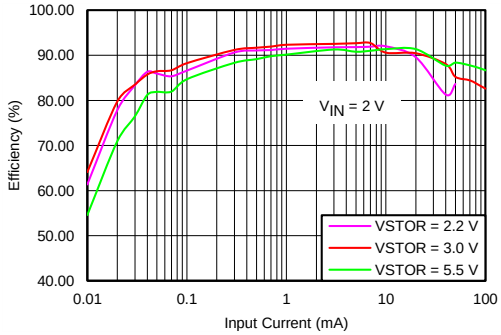
Figure 2. Charger Efficiency vs Input Voltage



VIN_DC = Keithley Source Meter configured with I_{COMP} = 10 mA and voltage source varied from 0.1 V to 3.0 V

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

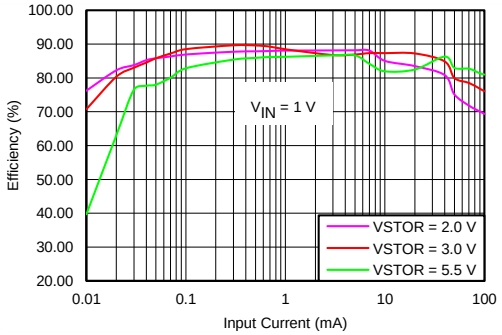
Figure 3. Charger Efficiency vs Input Voltage



VIN_DC = Keithley Source Meter configured with voltage source = 2.0 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.2 V , 3.0 V or 5.5 V

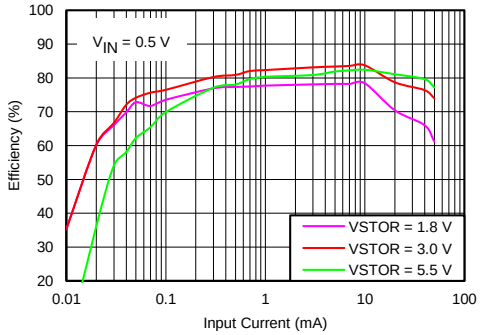
Figure 4. Charger Efficiency vs Input Current



VIN_DC = Keithley Source Meter configured with voltage source = 1.0 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

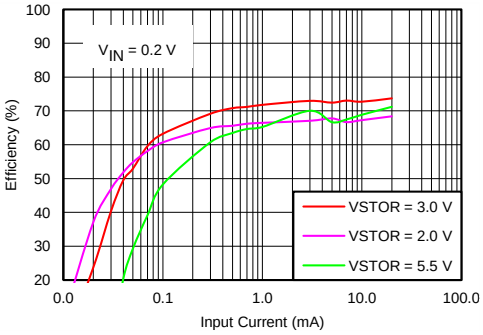
Figure 5. Charger Efficiency vs Input Current



VIN_DC = Keithley Source Meter configured with voltage source = 0.5 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 1.8 V, 3.0 V or 5.5 V

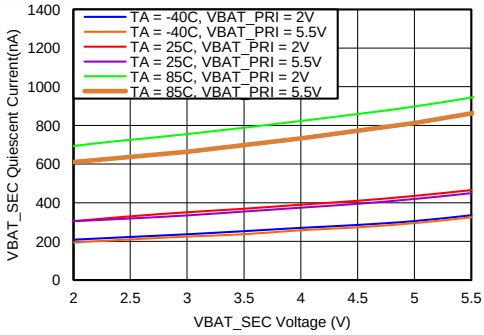
Figure 6. Charger Efficiency vs Input Current



VIN_DC = Keithley Source Meter configured with voltage source = 0.2 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

Figure 7. Charger Efficiency vs Input Current

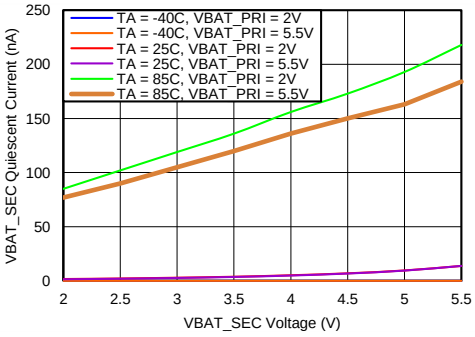


VIN_DC = floating and $\overline{EN}$ = GND

VBAT_SEC = Keithley Sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

VBAT_PRI = voltage source as indicated

Figure 8. Quiescent Current vs VBAT_SEC Voltage: Main Boost Charger Enabled but not Switching Mode

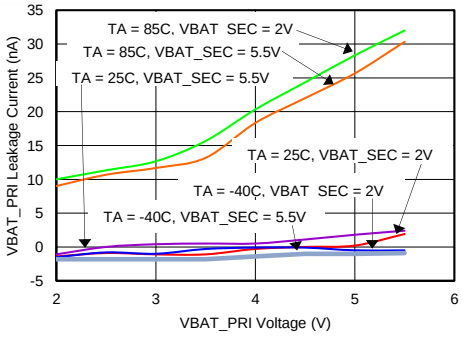


VIN_DC = floating and $\overline{EN}$ = VBAT_SEC

VBAT_SEC = Keithley Sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

VBAT_PRI = voltage source as indicated

Figure 9. Quiescent Current vs VBAT_SEC Voltage: Ship Mode



VIN_DC = floating and $\overline{EN}$ = VBAT_SEC or GND

VBAT_PRI = Keithley Sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

VBAT_SEC = voltage source as indicated

Figure 10. VBAT_PRI Leakage Current vs VBAT_PRI Voltage

7 Detailed Description

7.1 Overview

The bq25505 is the first of a new family of intelligent integrated energy harvesting Nano-Power management solutions that are well suited for meeting the special needs of ultra low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to miliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators (TEGs). The bq25505 is a highly efficient boost charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The design of the bq25505 starts with a DCDC boost charger that requires only microwatts of power to begin operating.

The main boost charger is powered from the boost output, VSTOR. Once the VSTOR voltage is above VSTOR_CHGEN (1.8 V typical), for example, after a partially discharged battery is attached to VBAT, the boost charger can effectively extract power from low voltage output harvesters such as TEGs or single or dual cell solar panels outputting voltages down to VIN(DC) (100 mV minimum). When starting from VSTOR=VBAT < 100 mV, the cold start circuit needs at least VIN(CS), 330 mV typical, to charge VSTOR up to 1.8 V.

The bq25505 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. Sampling of the VIN_DC open circuit voltage is programmed using external resistors, and that sample voltage is held with an external capacitor connected to the VREF_SAMP pin.

For example solar cells that operate at maximum power point (MPP) of 80% of their open circuit voltage, the resistor divider can be set to 80% of the VIN_DC voltage and the network will control the VIN_DC to operate near that sampled reference voltage. Alternatively, an external reference voltage can be applied directly to the VREF_SAMP pin by a MCU to implement a more complex MPPT algorithm.

The bq25505 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a rechargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that can not directly come from the input source. To prevent damage to the storage element, both maximum and minimum voltages are monitored against the internally programmed undervoltage (VBAT_UV) and user programmable overvoltage (VBAT_OV) levels.

To further assist users in the strict management of their energy budgets, the bq25505 toggles the battery good flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the shedding of load currents to prevent the system from entering an undervoltage condition. The OV and battery good (VBAT_OK) thresholds are programmed independently.

In addition to the boost charging front end, bq25505 provides the system with an autonomous power multiplexer gate drive. The gate drivers allow two storage elements to be multiplexed autonomously in order to provide a single power rail to the system load. This multiplexer is based off the VBAT_OK threshold which is resistor programmable by the user. This allows the user to set the level when the system is powered by the energy harvester storage element, for example, rechargable battery or super capacitor or a primary nonrechargeable battery (for example, two AA batteries). This type of hybrid system architecture allows for the run-time of a typical battery powered systems to be extended based on the amount of energy available from the harvester. If there is not sufficient energy to run the system due to extended "dark time", the primary battery is autonomously switched to the main system rail within 8 µsec in order to provide uninterrupted operation.

7.2 Functional Block Diagram

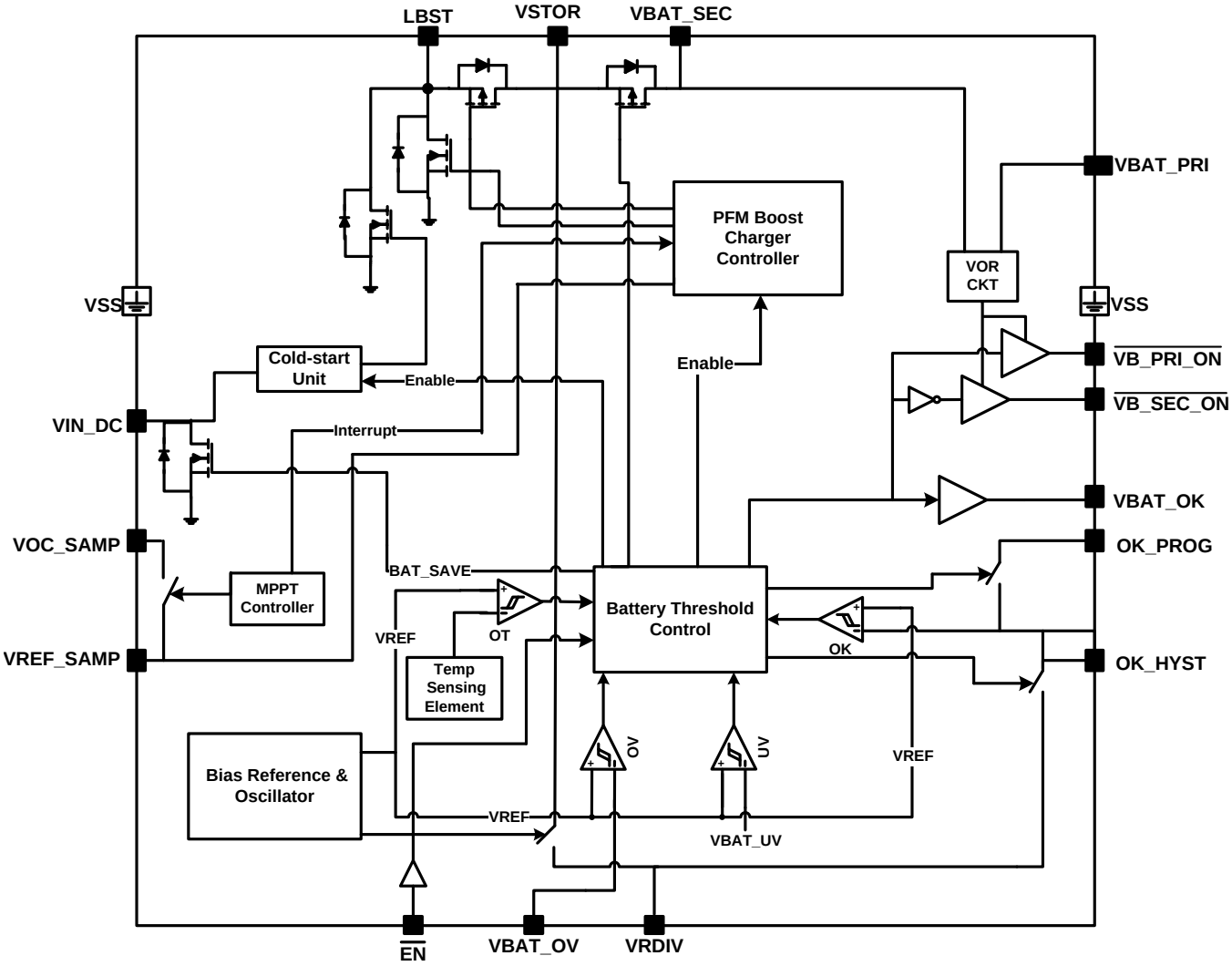


Figure 11. High-Level Functional Diagram

7.3 Feature Description

7.3.1 Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in order to maximize the power extracted from an energy harvester source. The boost converter indirectly modulates the input impedance of the main boost charger by regulating the charger's input voltage, as sensed by the VIN_DC pin, to the sampled reference voltage stored on the VREF_SAMP pin. The MPPT circuit obtains a new reference voltage every 16 s (typical) by periodically disabling the charger for 256 ms (typical) and sampling a fraction of the harvester's open-circuit voltage (VOC). For solar harvesters, the maximum power point is typically 70%-80% of VOC and for thermoelectric harvesters, the MPPT is typically 50%. Tying VOC_SAMP to VSTOR internally sets the MPPT regulation point to 80% of VOC. Tying VOC_SAMP to GND internally sets the MPPT regulation point to 50% of VOC. If input source does not have either 80% or 50% of VOC as its MPP point, the exact ratio for MPPT can be optimized to meet the needs of the input source being used by connecting external resistors R_{OC1} and R_{OC2} between VIN_DC and GND with mid-point at VOC_SAMP.

Feature Description (continued)

The reference voltage is set by Equation 1:

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

7.3.2 Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the IC has an internally set undervoltage (VBAT_UV) threshold plus an internal hysteresis voltage (VBAT_UV_HYST). The VBAT_UV threshold voltage when the battery voltage is decreasing is internally set to 1.95V (typical). The undervoltage threshold when the battery voltage is increasing is given by VBAT_UV plus an internal hystersis denoted by VBAT_UV_HYST. For the VBAT_UV feature to function properly, the system load should be connected to the VSTOR pin while the storage element should be connected to the VBAT_SEC pin. Once the VSTOR pin voltage goes above VBAT_UV plus VBAT_UV_HYST threshold, the VSTOR pin and the VBAT_SEC pins are effectively shorted through an internal PMOS FET. The switch remains closed until the VSTOR pin voltage falls below the VBAT_UV threshold. The VBAT_UV threshold should be considered a fail safe to the system. The system load should be removed or reduced based on the VBAT_OK threshold which should be set above the VBAT_UV threshold.

7.3.3 Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the overvoltage (VBAT_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT_SEC pin when the input has sufficient power. The VBAT_OV threshold when the battery voltage is rising is given by Equation 2:

$$VBAT\_OV = \frac{3}{2}VBIAS\left(1 + \frac{R_{OV2}}{R_{OV1}}\right) \quad (2)$$

The sum of the resistors is recommended to be no higher than 13 MΩ that is, $R_{OV1} + R_{OV2}$ = 13 MΩ. Spreadsheet provides help with sizing and selecting the resistors.

The overvoltage threshold when the battery voltage is decreasing is given by VBAT_OV - VBAT_OV_HYST. Once the voltage at the battery reaches the VBAT_OV threshold, the boost converter is disabled. The charger will start again once the battery voltage drop by VBAT_OV_HYST. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT_OV and the VBAT_OV - VBAT_OV_HYST levels.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is higher than VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

7.3.4 Battery Voltage in Operating Range (VBAT_OK Output)

The IC allows the user to set a programmable voltage in between the VBAT_UV and VBAT_OV settings to indicate whether the VSTOR voltage (and therefore the VBAT_SEC voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by Equation 3:

$$VBAT\_OK\_PROG = VBIAS\left(1 + \frac{R_{OK2}}{R_{OK1}}\right) \quad (3)$$

When the battery voltage is increasing, the threshold is set by Equation 4:

$$VBAT\_OK\_HYST = VBIAS\left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}}\right) \quad (4)$$

Feature Description (continued)

The sum of the resistors is recommended to be no higher than 13 MΩ, that is, R_{OK1} + R_{OK2} + R_{OK3}= 13 MΩ. SLUC484 provides help on sizing and selecting the resistors.

The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current to prevent MCU damage until it is fully powered. The VBAT_OK_PROG threshold must be greater than or equal to the UV threshold. Figure 21 shows VBAT_OK operation. Figure 12 shows the relative position of the various threshold voltages.

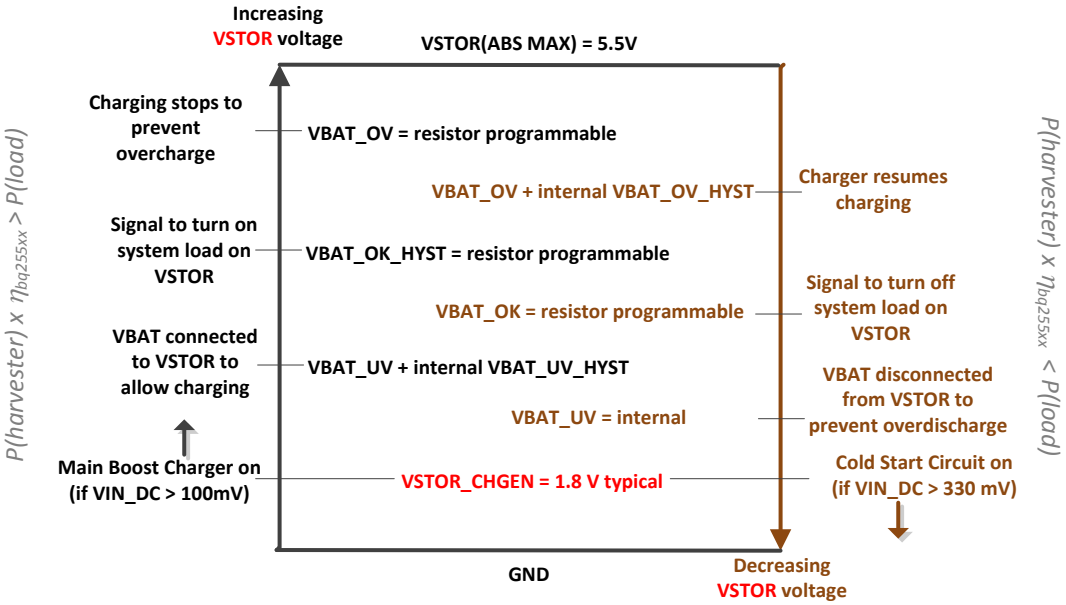


Figure 12. Summary of VSTOR Threshold Voltages

7.3.5 Push-Pull Multiplexer Drivers

There are two push-pull drivers intended to mulitplex between a primary nonrechargeable connected at VBAT_PRI and secondary storage element connected on VBAT_SEC based on the VBAT_OK signal. When the VBAT_OK signal goes high, indicating that the secondary rechargeable battery at VBAT_SEC is above the VBAT_OK_HYST threshold, the $\overline{\text{VB\_PRI\_ON}}$ output goes high followed by the $\overline{\text{VB\_SEC\_ON}}$ signal going low in order to connect VBAT_SEC to the system output (referred to as the VOR node). When VBAT_OK goes low, indicating that the secondary rechargeable battery at VBAT_SEC is below the VBAT_OK threshold, the $\overline{\text{VB\_SEC\_ON}}$ output goes high followed by the $\overline{\text{VB\_PRI\_ON}}$ signal going low in order to connect VBAT_PRI to the system. The drivers are powered by an ideal diode OR of the secondary battery at VBAT_SEC and the primary battery at VBAT_PRI, even during cold-start, giving each enough drive for up to 2 nF of gate capacitance of external back-to-back PMOS FETs. The switching characteristics follows a break-before-make model, wherein during a transition, the drivers both go high for a typical dead time of 5 us before one of the signals goes low. The figure below shows the FET gate voltages for the transition from the secondary battery being connected to the system to the primary battery being connected.

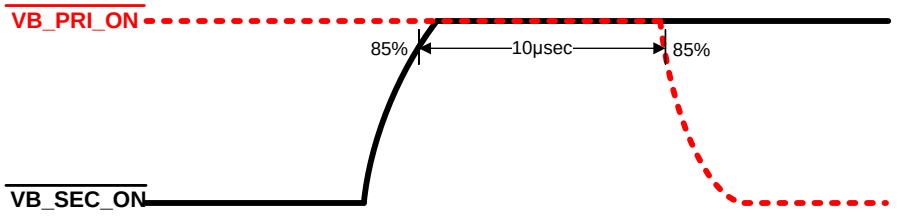


Figure 13. Break-Before-Make Operation of $\overline{\text{VB\_PRI\_ON}}$ and $\overline{\text{VB\_SEC\_ON}}$

Figure 24 through Figure 26 show multiplexer operation.

Feature Description (continued)

7.3.6 Nano-Power Management and Efficiency

The high efficiency of the bq25505 charger is achieved through the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds the VSTOR voltage to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in Figure 20 where the VRDIV node is monitored. Here the VRDIV node provides a connection to the VSTOR voltage (first pulse) and then generates the reference levels for the VBAT_OV and VBAT_OK resistor dividers for a short period of time. The divided down values at each pin are compared against VBIAS as part of the hysteretic control. Because this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection—hence reducing the overall quiescent current due to the resistors. This process repeats every 64 ms.

The efficiency of the bq25505 boost charger is shown for various input power levels in Figure 1 through Figure 7. All data points were captured by averaging the overall input current. This must be done due to the periodic biasing scheme implemented via the Nano-Power management circuitry. In order to properly measure the resulting input current when calculating the output to input efficiency, the input current efficiency data was gathered using a source meter set to average over at least 50 samples. Quiescent currents into VSTOR, VBAT_SEC and VBAT_PRI over temperature and voltage are shown at Figure 8 through Figure 10.

7.4 Device Functional Modes

The bq25505 has four functional modes: main boost charger disabled (ship mode), cold-start operation, main boost charger enabled and thermal shutdown. Figure 11 is a high-level functional block diagram which highlights most of the major functional blocks inside the bq25505. The cold start circuitry is powered from VIN_DC. The main boost charger circuitry is powered from VSTOR while the boost power stage is powered from VIN_DC. Details of entering and exiting each mode are explained below.

7.4.1 Main Boost Charger Disabled (Ship Mode) - (VSTOR > VSTOR_CHGEN and $\overline{EN}$ = HIGH)

When taken high relative to the voltage on VBAT_SEC, the $\overline{EN}$ pin shuts down the IC including the boost charger and battery management circuitry. It also turns off the PFET that connects VBAT_SEC to VSTOR. This can be described as ship mode, because it will put the IC in the lowest leakage state and provide a long storage period without significantly discharging the battery on VBAT_SEC. If there is no need to control $\overline{EN}$, it is recommended that this pin be tied to VSS, or system ground.

7.4.2 Cold-Start Operation (VSTOR < VSTOR_CHGEN, VIN_DC > VIN(CS) and PIN > PIN(CS))

Whenever VSTOR < VSTOR_CHGEN, VIN_DC ≥ VIN(CS) and PIN > PIN(CS), the cold-start circuit is on. This could happen when there is not input power at VIN_DC to prevent the load from discharging the battery or during a large load transient on VSTOR. During cold start, the voltage at VIN_DC is clamped to VIN(CS) so the energy harvester's output current is critical to providing sufficient cold start input power, PIN(CS) = VIN(CS) X IIN(CS). The cold-start circuit is essentially an unregulated, hysteretic boost converter with lower efficiency compared to the main boost charger. None of the other features, including the EN pin, function during cold start operation. The cold start circuit's goal is to charge VSTOR higher than VSTOR_CHGEN so that the main boost charger can operate. When a depleted storage element is initially attached to VBAT_SEC, as shown in Figure 14 and the harvester can provide a voltage > VIN(CS) and total power at least > PIN(CS), assuming no system load or leakage at VSTOR and VBAT_SEC, the cold start circuit can charge VSTOR above VSTOR_CHGEN. Once the VSTOR voltage reaches the VSTOR_CHGEN threshold, the IC

1. first performs an initialization pulse on VRDIV to reset the feedback voltages,
2. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
3. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

Device Functional Modes (continued)

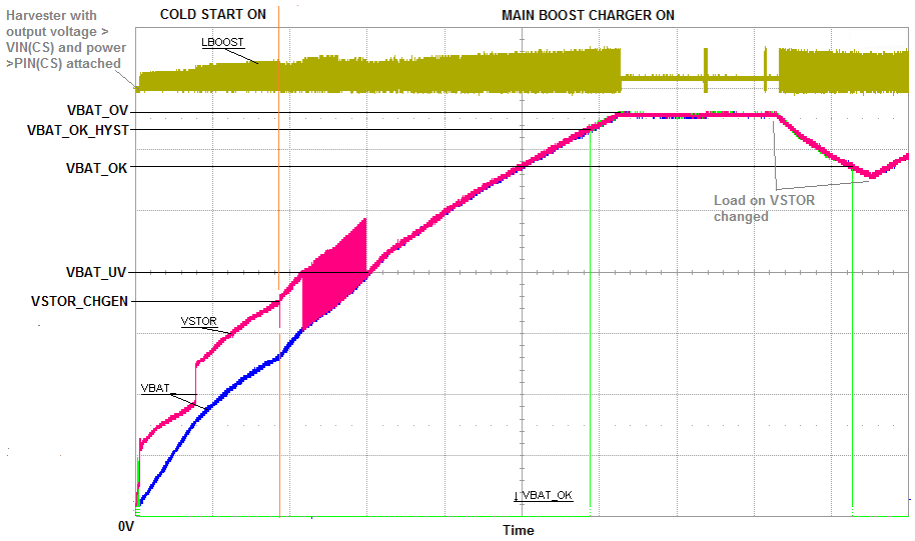


Figure 14. Charger Operation After a Depleted Storage Element is Attached and Harvester Power is Available

The energy harvester must supply sufficient power for the IC to exit cold start. Due to the body diode of the PFET connecting VSTOR and VBAT_SEC, the cold start circuit must charge both the capacitor on CSTOR up to the VSTOR_CHGEN and the storage element connected to VBAT_SEC up to VSTOR_CHGEN less a diode drop. When a rechargeable battery with an open protector is attached, the intial charge time is typically short due to the minimum charge needed to close the battery's protector FETs. When large, discharged super capacitors with high DC leakage currents are attached, the intial charge time can be signficant.

When the VSTOR voltage reaches VSTOR_CHGEN, the main boost charger starts up. When the VSTOR voltage rises to the VBAT_UV threshold, the PMOS switch between VSTOR and VBAT_SEC turns on, which provides additional loading on VSTOR and could result in the VSTOR voltage dropping below both the VBAT_UV threshold and the VSTOR_CHGEN voltage, especially if system loads on VSTOR or VBAT_SEC are active during this time. Therefore, it is not uncommon for the VSTOR voltage waveform to have incremental pulses (for example, stair steps) as the IC cycles between cold-start and main boost charger operation before eventually maintaing VSTOR above VSTOR_CHGEN.

The cold start circuit initially clamps VIN_DC to VIN(CS) = 330 mV typical. If sufficient input power (that is, output current from the harvester clamped to VIN(CS)) is not available, it is possible that the cold start circuit cannot raise the VSTOR voltage above VSTOR_CHGEN in order for the main boost conveter to start up. It is highly recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal provided by VB_SEC_ON can be used to drive the gate of this system-isolating, external PFET. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

Device Functional Modes (continued)

7.4.3 Main Boost Charger Enabled (VSTOR > VSTOR_CHGEN, VIN_DC > VIN(DC) and $\overline{EN}$ = LOW)

One way to avoid cold start is to attach a partially charged storage element as shown in Figure 15.

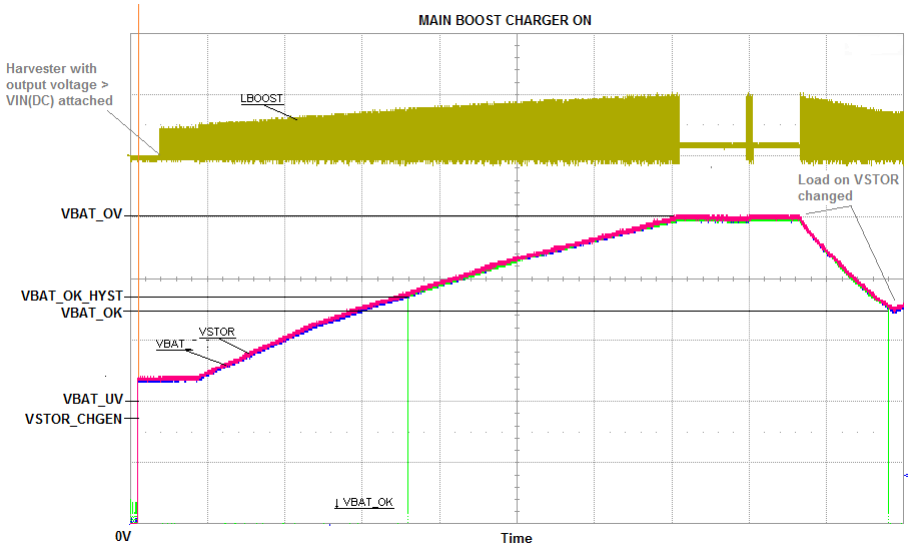


Figure 15. Charger Operation after a Partially Charged Storage Element is Attached and Harvester Power is Available

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (for example, the battery protector PFET is closed) and with the VSTOR node more than 100 mV above ground results in the PFET between VSTOR and VBAT_SEC remaining off until an input source is attached.

Assuming the voltages on VSTOR and VBAT_SEC are both below 100mV, when a charged storage element is attached (that is, hot-plugged) to VBAT_SEC, the IC

1. first turns on the internal PFET between the VSTOR and VBAT_SEC pins for $t_{BAT\_HOT\_PLUG}$ (45ms) in order to charge VSTOR to VSTOR_CHGEN then turns off the PFET to prevent the battery from overdischarge,
2. then performs an initialization pulse on VRDIV to reset the feedback voltages,
3. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
4. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

If the VSTOR pin voltage remains above the internal under voltage threshold (VBAT_UV) for the additional 64 ms after the VRDIV initialization pulse (following the 45-ms PFET on time), the internal PFET turns back on and the main boost charger begins to charge the storage element assuming there is sufficient power available from the harvester at the VIN_DC pin. If VSTOR does not reach the VBAT_UV threshold, then the PFET remains off until the main boost charger can raise the VSTOR voltage to VBAT_UV. If a system load tied to VSTOR discharges VSTOR below VSTOR_GEN or below VBAT_UV during the 32 ms initial MPPT reference voltage measurement or within 110 ms after hot plug, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal provided by $\overline{VB_SEC_ON}$can be used to drive the gate of this system-isolating, external PFET. Otherwise, the VSTOR voltage waveform will have incremental pulses as the IC turns on and off the internal PFET controlled by VBAT_UV or cycles between cold-start and main boost charger operation.

Once VSTOR is above VSTOR_CHGEN, the main boost charger employs pulse frequency modulation (PFM) mode of control to regulate the voltage at VIN_DC close to the desired reference voltage. The reference voltage is set by the MPPT control scheme as described in the features section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak

Device Functional Modes (continued)

current in the inductor is dithered internally to up to three pre-determined levels in order to maintain high efficiency of the charger across a wide input current range. The charger transfers up to a maximum of 100 mA average input current (230mA typical peak inductor current). The boost charger is disabled when the voltage on VSTOR reaches the user set VBAT_OV threshold to protect the battery connected at VBAT_SEC from overcharging. In order for the battery to charge to VBAT_OV, the input power must exceed the power needed for the load on VSTOR. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

Steady state operation for the boost charger is shown in Figure 18. These plots highlight the inductor current, the VSTOR voltage ripple, input voltage regulation and the LBOOST switching node. The cycle-by-cycle minor switching frequency is a function of each the converter's inductor value, peak current limit and voltage levels on each side of each inductor. Once the VSTOR capacitor, CSTOR, droops below a minimum value, the hysteretic switching repeats.

7.4.4 Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The bq25505 uses an integrated temperature sensor to monitor the junction temperature of the device. The temperature threshold for thermal protection is set to 125°C. Once the temperature threshold is exceeded, the boost charger is disabled and charging ceases. Once the temperature of the device drops below this threshold, the boost charger and buck converter resumes operation. To avoid unstable operation near the overtemp threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost charger is disabled. However, if the supply voltage drops to the VBAT_UV setting, then the switch between VBAT_SEC and VSTOR will open and protect the battery even if the device is in thermal shutdown.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Energy Harvester Selection

The energy harvesting source (for example, solar panel, TEG, vibration element) must provide a minimum level of power for the IC to operate as designed. The IC's minimum input power required to exit cold start can be estimated as:

$$PIN > PIN(CS) = VIN(CS) \times IIN(CS) > \frac{\left(I - STR\_ELM\_LEAK_{@1.8V} \times 1.8V\right) + \frac{(1.8V)^2}{RSTOR(CS)}}{0.05} \quad (5)$$

where I-STR_ELM_LEAK$_{@1.8V}$ is the storage element leakage current at 1.8V and

RSTOR(CS) is the equivalent resitive load on VSTOR during cold start and 0.05 is an estimate of the worst case efficiency of the cold start circuit.

Once the IC is out of cold start and the system load has been activated (for example, using the VBAT_OK signal), the energy harvesting element must provide the main boost charger with at least enough power to meet the average system load. Assuming RSTOR(AVG) represents the average resistive load on VSTOR, the simplified equation below gives an estimate of the IC's minimum input power needed during system operation:

$$PIN \times \eta_{EST} > PLOAD = \frac{(VBAT\_OV)^2}{RSTOR(AVG)} + VBAT\_OV \times I - STR\_ELM\_LEAK_{@VBAT\_OV} \quad (6)$$

where η_{EST} can be derived from the datasheet efficiency curves for the given input voltage and current and VBAT_OV. The simplified equation above assumes that, while the harvester is still providing power, the system goes into low power or sleep mode long enough to charge the storage element so that it can power the system when the harvester eventually is down. Refer to SLUC463 for a design example that sizes the energy harvester.

8.1.2 Storage Element Selection

In order for the charge management circuitry to protect the storage element from over-charging or discharging, the storage element must be connected to VBAT pin and the system load tied to the VSTOR pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100uF equivalent capacitance is required to filter the pulse currents of the PFM switching charger. The equivalent capacitance of a battery can be computed as computed as:

$$C_{EQ} = \frac{2 \times mAHr_{BAT(CHRGD)} \times 3600\ s/Hr}{V_{BAT(CHRGD)}} \quad (7)$$

In order for the storage element to be able to charge VSTOR capacitor (CSTOR) within the $t_{VB\_HOT\_PLUG}$ (50 ms typical) window at hot-plug; therefore preventing the IC from entering cold start, the time constant created by the storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than $t_{VB\_HOT\_PLUG}$. For example, a battery's resistance can be computed as:

$R_{BAT} = V_{BAT} / I_{BAT(CONTINUOUS)}$ from the battery specifications. (8)

The storage element must be sized large enough to provide all of the system load during periods when the harvester is no longer providing power. The harvester is expected to provide at least enough power to fully charge the storage element while the system is in low power or sleep mode. Assuming no load on VSTOR (that is, the system is in low power or sleep mode), the following equation estimates charge time from voltage VBAT1 to VBAT2 for given input power is:

Application Information (continued)

$$PIN \times \eta_{EST} \times t_{CHRG} = 1/2 \times CEQ \times (VBAT2^2 - VBAT1^2) \quad (9)$$

Refer to SLUC463 for a design example that sizes the storage element.

Note that if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7uF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. See *Capacitor Selection* for guidance on sizing capacitors.

8.1.3 Inductor Selection

The boost charger needs an appropriately sized inductor for proper operation. The saturation current of the inductor should be at least 25% higher than the expected peak inductor currents recommended below if system load transients on VSTOR are expected. Because this device uses hysteretic control, the boost charger is considered naturally stable systems (single-order transfer function).

For the boost charger to operate properly, an inductor of appropriate value must be connected between LBOOST, pin 20, and VIN_DC, pin 2. The boost charger internal control circuitry is designed to control the switching behavior with a nominal inductance of 22 µH ± 20%. The inductor must have a peak current capability of > 300 mA with a low series resistance (DCR) to maintain high efficiency.

A list of inductors recommended for this device is shown in Table 2.

Table 2. Recommended Inductors

INDUCTANCE (µH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER(1)
22	4.0x4.0x1.7	LPS4018-223M	Coilcraft
22	3.8x3.8x1.65	744031220	Wurth
22	2.8x2.8x2.8	744025220	Wurth

(1) See *Device Support* concerning recommended third-party products.

8.1.4 Capacitor Selection

In general, all the capacitors must be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

8.1.4.1 VREF_SAMP Capacitance

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, TI recommends that the capacitor be an X7R or COG low-leakage capacitor.

8.1.4.2 VIN_DC Capacitance

Energy from the energy harvester input source is initially stored on a capacitor, CIN, connected to VIN_DC, pin 2, and VSS, pin 1. For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but a minimum value of 4.7 µF is recommended.

8.1.4.3 VSTOR Capacitance

Operation of the bq25505 requires two capacitors to be connected between VSTOR, pin 19, and VSS, pin 1. A high-frequency bypass capacitor of at 0.01 µF should be placed as close as possible between VSTOR and VSS. In addition, a low ESR capacitor of at least 4.7 µF should be connected in parallel.

8.1.4.4 Additional Capacitance on VSTOR or VBAT_SEC

If there are large, fast system load transients and/or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT_UV threshold in response to the transient. This causes the bq25505 to turn off the PFET switch between VSTOR and VBAT_SEC and turn on the boost charger. The CSTOR capacitors may further discharge below the VSTOR_CHGEN threshold and cause the bq25505 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increasing the CSTOR capacitance or adding additional capacitance in parallel with the storage element is recommended. For example, if boost charger is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 µs duration infrequently occurs, then, solving I = C x dv/dt for CSTOR gives:

$$\text{CSTOR} \geq \frac{500\ \text{mA} \times 50\ \mu\text{s}}{(4.2\ \text{V} - 1.8\ \text{V})} = 10.5\ \mu\text{F} \tag{10}$$

Note that increasing CSTOR is the recommended solution but will cause the boost charger to operate in the less efficient cold start mode for a longer period at startup compared to using CSTOR = 4.7 µF. If longer cold start run times are not acceptable, then place the additional capacitance in parallel with the storage element.

For a recommended list of standard components, see the EVM User's Guide (SLUUAA8).

8.2 Typical Applications

8.2.1 Solar Application Circuit

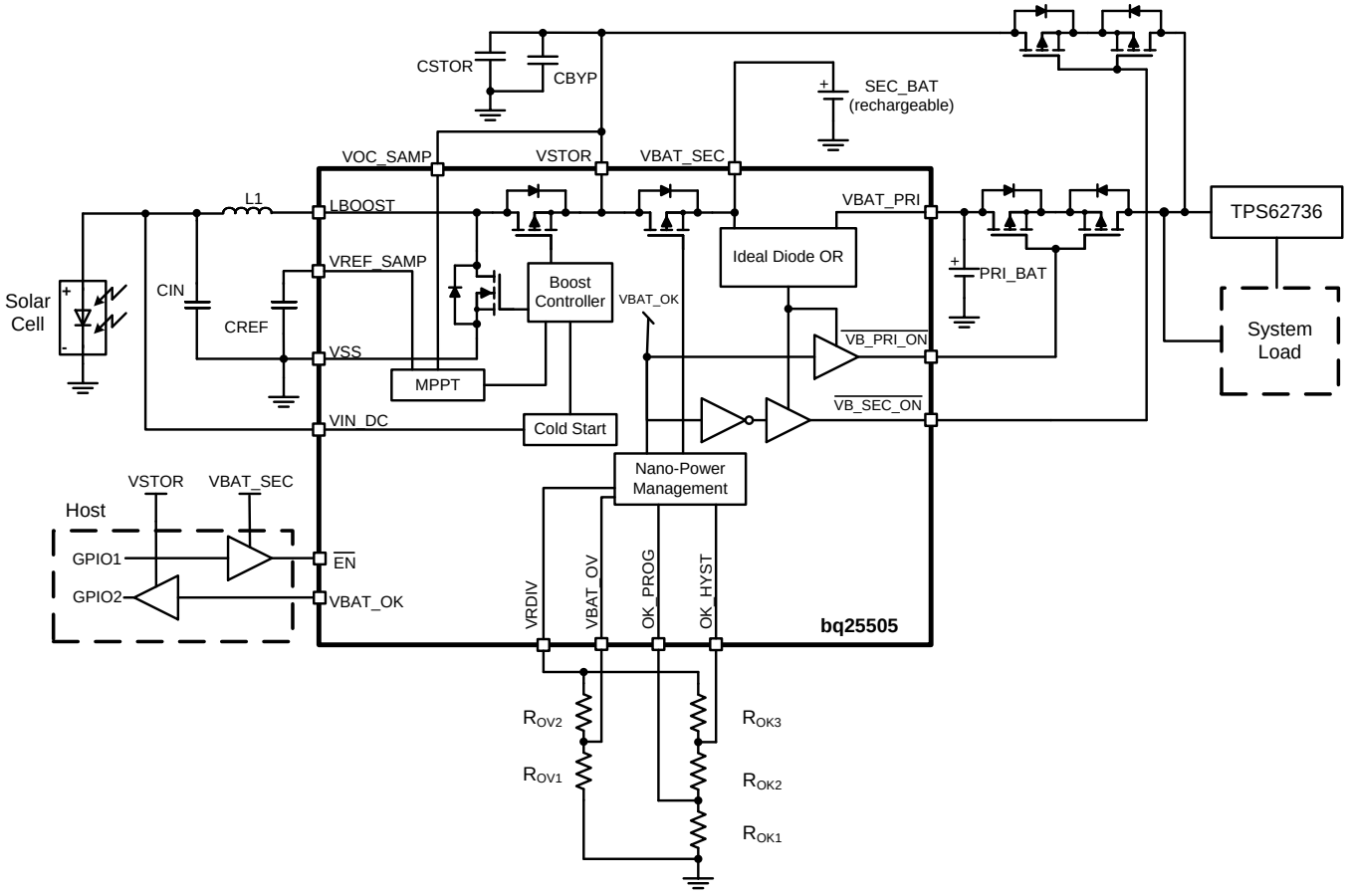


Figure 16. Typical Solar Application Circuit With Primary and Secondary Batteries

Typical Applications (continued)

8.2.1.1 Design Requirements

The desired voltage levels are VBAT_OV = 4.2 V, VBAT_OK = 2.39 V, VBAT_OK_HYST = 2.80 V and MPP (V_{OC}) = 80% which is typical for solar panels. There are no large load transients expected.

8.2.1.2 Detailed Design Procedure

The recommended L1 = 22 µH, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

No MPPT resistors are required because VOC_SAMP can be tied to VSTOR to give 80% MPPT.

- Keeing in mind VBAT_UV < VBAT_OV ≤ 5.5 V, to size the VBAT_OV resistors, first choose $RSUM_{OV} = R_{OV1} + R_{OV2}$ = 13 MΩ then solve Equation 2 for

$$R_{OV1} = \frac{3}{2} \times \frac{RSUM_{OV} \times VBIAS}{VBAT\_OV} \times \frac{3}{2} \frac{13\ M\Omega \times 1.21\ V}{4.2\ V} = 5.61\ M\Omega \rightarrow 5.62\ M\Omega \text{ closest 1\% value then} \quad (11)$$

- $R_{OV2} = RSUM_{OV} - R_{OV1}$ = 13 MΩ - 5.62 MΩ = 7.38 MΩ → 7.32 MΩ resulting in VBAT_OV = 4.18V due to rounding to the nearest 1% resistor.
- Keeping in mind VBAT_OV ≥ VBAT_OK_HYST > VBAT_OK ≥ VBAT_UV, to size the VBAT_OK and VBAT_OK_HYST resistors, first choose $RSUM_{OK} = R_{OK1} + R_{OK2} + R_{OK3}$ = 13 MΩ then solve Equation 3 and Equation 4 for

$$R_{OK1} = \frac{VBIAS \times RSUM_{OK}}{VBAT\_OK\_HYST} = \left(\frac{1.21\ V}{2.8\ V}\right) \times 13\ M\Omega = 5.62\ M\Omega \text{ then} \quad (12)$$

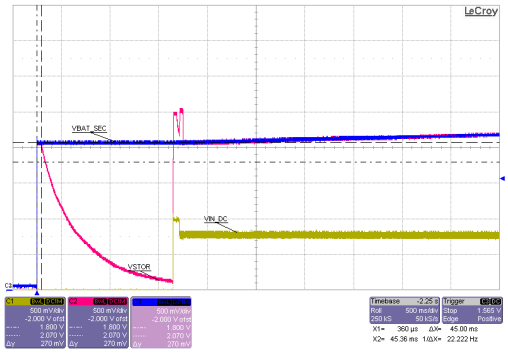
$$R_{OK2} = \left(\frac{VBAT\_OK}{VBIAS} - 1\right) \times R_{OK1} = \left(\frac{2.39\ V}{1.21\ V} - 1\right) \times 5.62\ M\Omega = 5.479\ M\Omega \rightarrow 5.49\ M\Omega, \text{ then} \quad (13)$$

- $R_{OK3} = RSUM_{OK} - R_{OK1} - R_{OK2}$ = 13 MΩ - 5.62 MΩ - 5.479 MΩ = 1.904 MΩ → 1.87 MΩ to give VBAT_OK = 2.39 V and VBAT_OK_HYST = 2.80 V.

SLUC484 provides help on sizing and selecting the resistors.

Typical Applications (continued)

8.2.1.3 Application Performance Plots

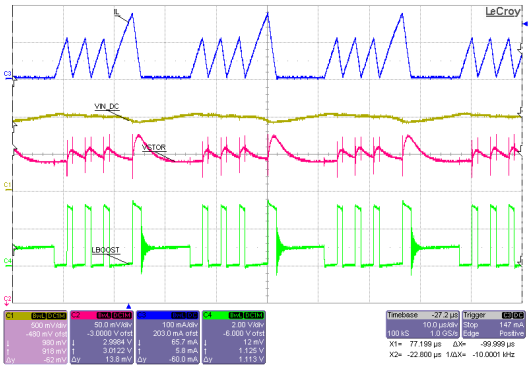


Sourcemeter with V_{SOURCE} = 1.0 V and compliance of 8.5 mA subsequently applied to VIN_DC

VBAT_SEC = 0.1 F capacitor charged to 2.0 V

Resistance on VSTOR = 100 kΩ

Figure 17. Startup by Battery Attach With Almost Depleted Storage Element

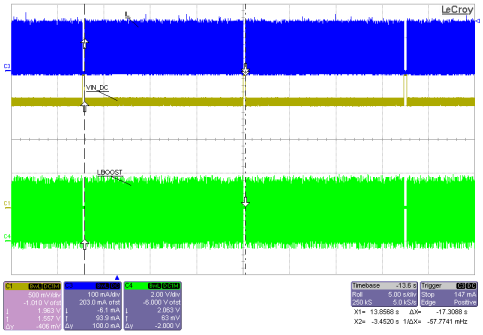


VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

IL = inductor current

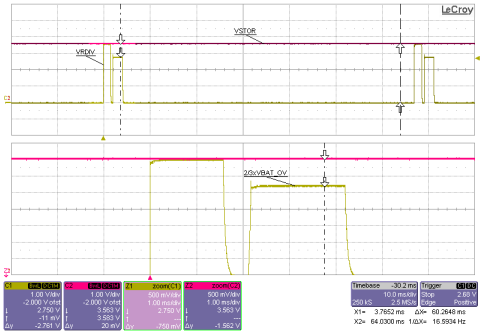
Figure 18. Boost Charger Operational Waveforms



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

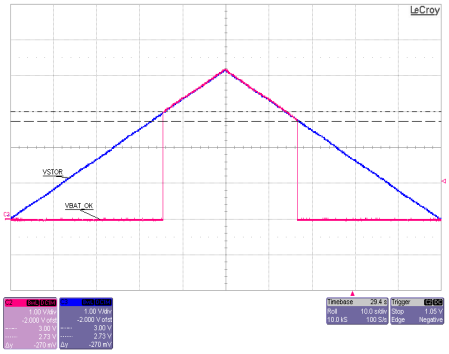
Figure 19. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.6 V and compliance of 1 A

Figure 20. VRDIV Waveform

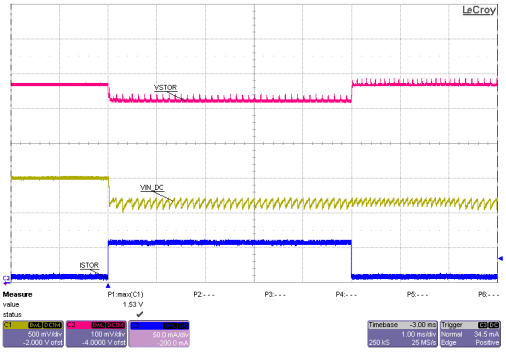


VIN_DC = 1.5 V with 75 Ω series resistance

No storage element on VBAT_SEC or VBAT_PRI

VSTOR artifically ramped from 0 V to 4.2 V to 0 V using a power amp driven by a function generator

Figure 21. VBAT_OK Operation



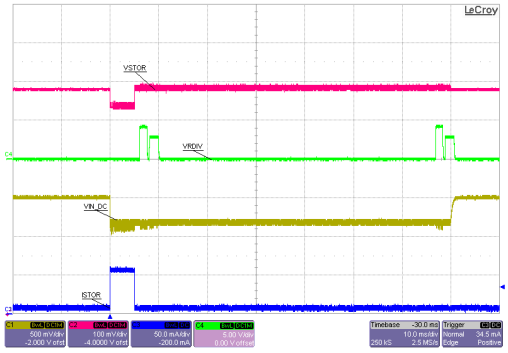
VIN_DC = 1.5 V with 75 Ω series resistance

VBAT = 4.2 V charged 0.5 F capacitor

R(VSTOR) = open to 84 Ω to open

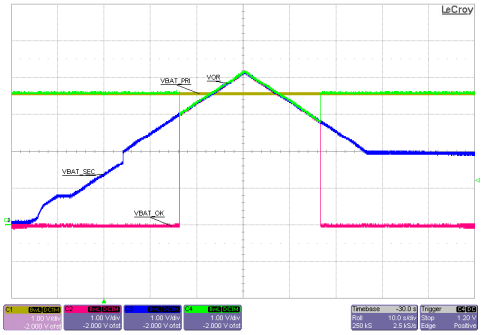
Figure 22. 50 mA Load Transient on VSTOR

Typical Applications (continued)



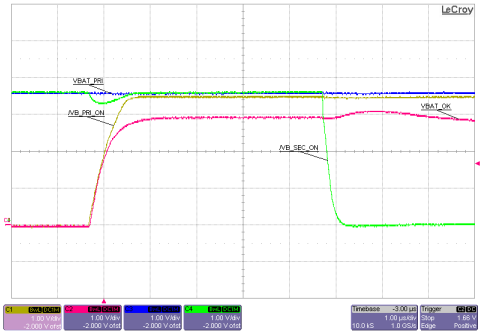
VIN_DC = 1.5 V with 75 Ω series resistance
VBAT = 4.2 V charged 0.5 F capacitor
R(VSTOR) = open to 84 Ω to open

Figure 23. 50 mA Load Transient on VSTOR - Zoom Out



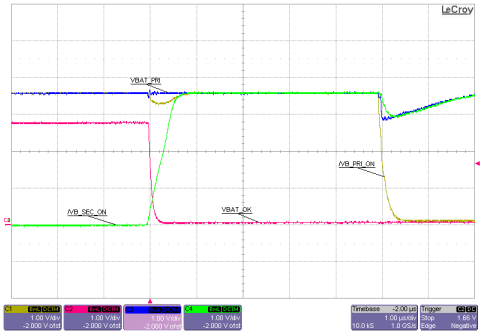
VIN_DC = 1.5 V with 75 Ω series resistance; VBAT _PRI = 3.6 V power supply
0.5 F super capacitor on VBAT_SEC; 1kΩ load on output of MUX FETs (VOR)
VSTOR artifically ramped from 0 V to 4.2 V to 0 V using a function generator

Figure 24. Multiplexer Output (VOR) as VBAT_SEC Crosses VBAT_OK Threshold



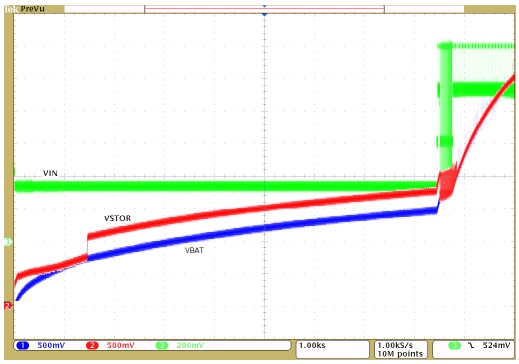
VIN_DC = 1.5 V with 75 Ω series resistance; VBAT _PRI = 3.6 V power supply
0.5 F super capacitor on VBAT_SEC; 1kΩ load on output of MUX FETs (VOR)
VSTOR artifically ramped from 0 V to 4.2 V using a function generator

Figure 25. MUX Signals When VBAT_SEC > VBAT_OK Threshold



VIN_DC = 1.5 V with 75 Ω series resistance; VBAT _PRI = 3.6 V power supply
0.5 F super capacitor on VBAT_SEC; 1kΩ load on output of MUX FETs (VOR)
VSTOR artifically ramped from 4.2 V to 0 V using a function generator

Figure 26. MUX Signals When VBAT_SEC < VBAT_OK Threshold



VIN_DC = source meter with 1.2 V compliance and ISC = 1 mA
120 mF super capacitor on VBAT_SEC

Figure 27. Charging a Super Capacitor on VBAT

Typical Applications (continued)

8.2.2 TEG Application Circuit

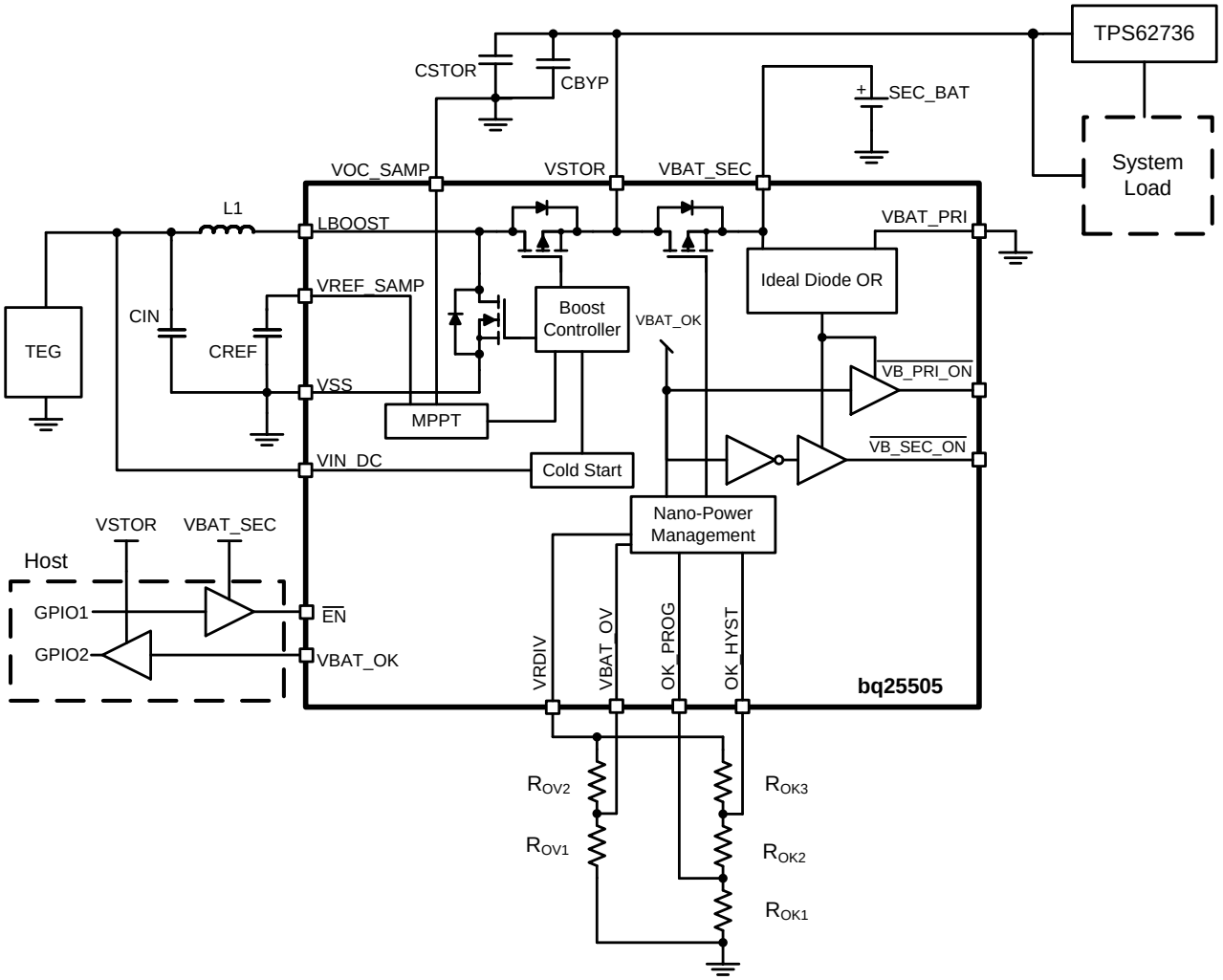


Figure 28. Typical TEG Application Circuit Without a Primary Battery

8.2.2.1 Design Requirements

The desired voltage levels are VBAT_OV = 5.0 V, VBAT_OK = 3.5 V, VBAT_OK_HYST = 3.7 V and MPP (V_{OC}) = 50% which is typical for TEG harvesters.

8.2.2.2 Detailed Design Procedure

The recommended L1 = 22 µH, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. The rectifier diodes are Panasonic DB3X316F0L. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

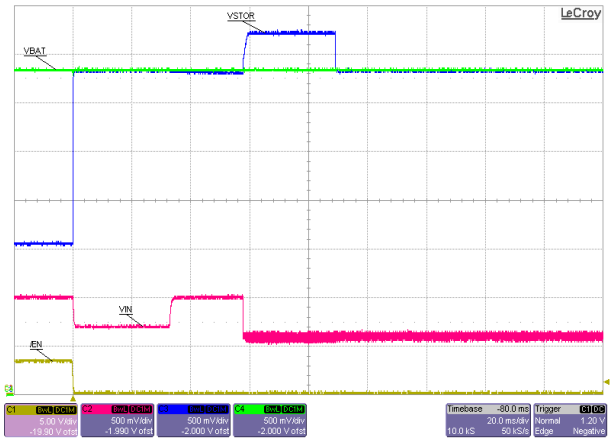
No MPPT resistors are required because VOC_SAMP can be tied to GND to give 50% MPPT.

Referring back to the procedure in *Typical Applications* or using the spreadsheet calculator at SLUC484 gives the following values:

- R_{OV1} = 4.75 MΩ, R_{OV2} = 8.25 MΩ resulting in VBAT_OV = 4.97 V due to rounding to the nearest 1% resistor.
- R_{OK1} = 4.22 MΩ, R_{OK2} = 8.06 MΩ, R_{OK3} = 0.698 MΩ resulting in VBAT_OK = 3.5 V and VBAT_OK_HYST = 3.7 V after rounding.

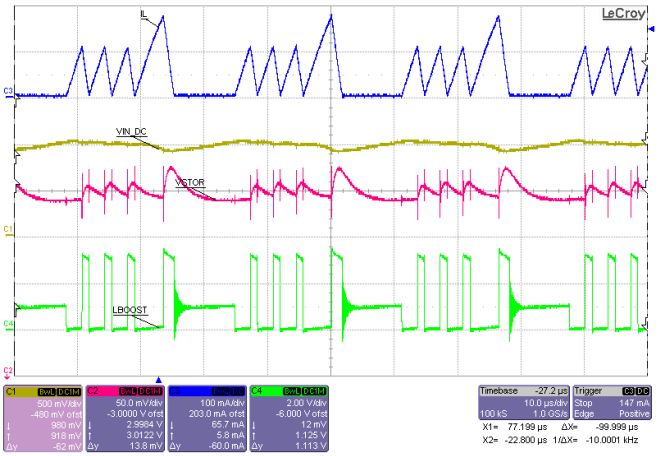
Typical Applications (continued)

8.2.2.3 Application Performance Plots



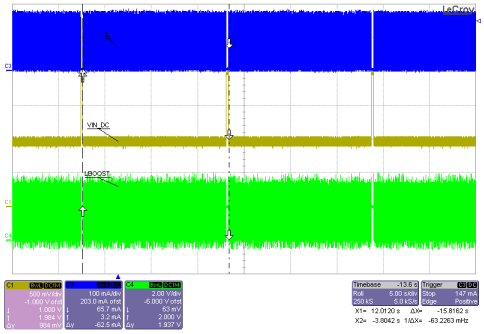
VIN_DC = 1.0 V power supply 100Ω series resistance
VBAT = 3.4-V charged Li coin cell

Figure 29. Startup by Taking $\overline{EN}$ Low (From Ship Mode)



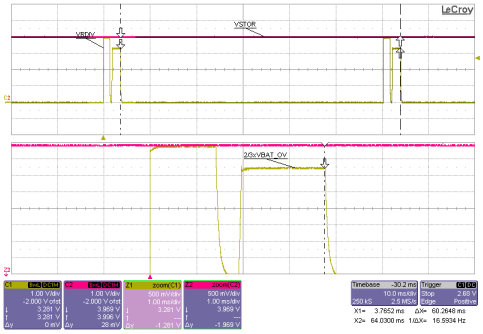
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 30. Boost Charger Operational Waveforms



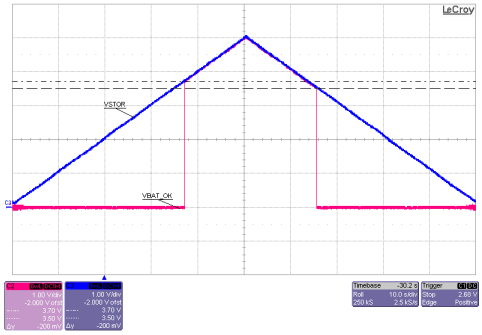
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 31. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT_SEC = sourcemeter with V_{SOURCE} = 4.0 V and compliance of 1 A

Figure 32. VRDIV Waveform



VIN_DC floating
No storage element on VBAT or VBAT_PRI
VSTOR artifically ramped from 0 V to 5 V to 0 V using a function generator

Figure 33. VBAT_OK Operation

Typical Applications (continued)

8.2.3 Piezoelectric Application Circuit

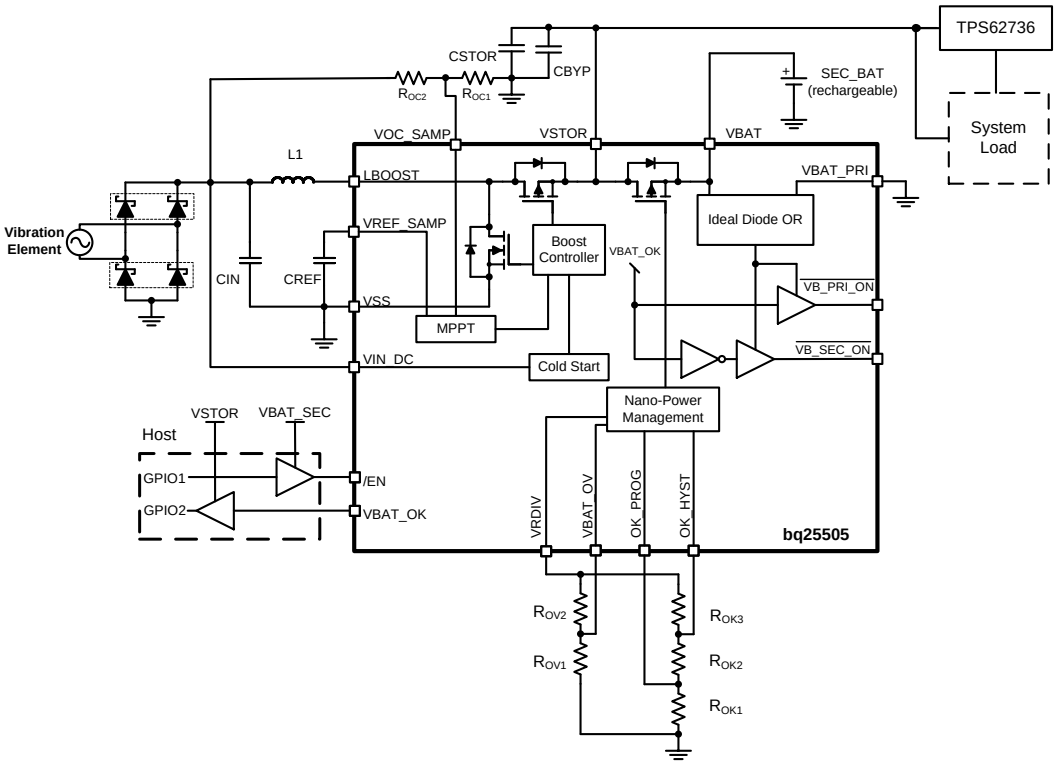


Figure 34. Typical Piezoelectric Application Circuit With Primary and Secondary Batteries

8.2.3.1 Design Requirements

The desired voltage levels are VBAT_OV = 3.30 V, VBAT_OK = 2.80 V, VBAT_OK_HYST = 3.10 V, and MPP (V_{OC}) = 40% for the selected piezoelectric harvester which provides a rectified V_{OC} = 1 V.

8.2.3.2 Detailed Design Procedure

The recommended L1 = 22 µH, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. The rectifier diodes are Panasonic DB3X316F0L. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

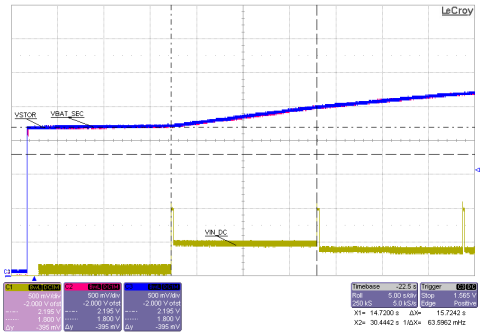
- Keeping in mind that VREF_SAMP stores the MPP voltage for the harvester, first choose $RSUM_{OC} = R_{OC1} + R_{OC2}$ = 20 MΩ then solve Equation 1 for

$$R_{OC1} = \left(\frac{VREF\_SAMP}{VIN\_DC(OC)}\right) \times RSUM_{OC} = \frac{0.14}{1V} \times 20\ M\Omega = 8\ M\Omega \rightarrow 8.06\ M\Omega \text{ closest 1\% resistor, then} \quad (14)$$

- R_{OC2} = $RSUM_{OC}$ x (1 - VREF_SAMP / VIN_DC(OC) = 20 MΩ x (1 - 0.4 V / 1 V) = 12 MΩ → series 10 MΩ and
  2 MΩ easy to obtain 1% resistors.
- Referring back to the procedure in *Typical Applications* or using the spreadsheet calculator at SLUC484 gives the following values
  - R_{OV1} = 7.15 MΩ, R_{OV2} = 5.90 MΩ resulting in VBAT_OV = 3.31V due to rounding to the nearest 1% resistor.
- R_{OK1} = 4.99 MΩ, R_{OK2} = 6.65 MΩ, R_{OK3} = 1.24 MΩ resulting in VBAT_OK = 2.82 V and VBAT_OK_HYST = 3.12 V after rounding to the nearest 1% resistor value.

Typical Applications (continued)

8.2.3.3 Application Curves

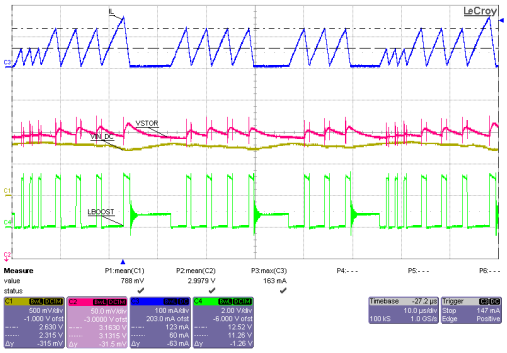


Sourcemeter with V_{SOURCE} = 1.0 V and compliance of 8.5 mA subsequently applied to VIN_DC

VBAT_SEC = 0.1 F capacitor charged to 2.2 V

Resistance on VSTOR = 100 kΩ

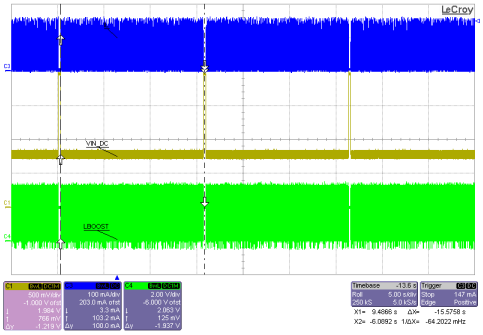
Figure 35. Startup by Battery Attach With Partially Charged Storage Element



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

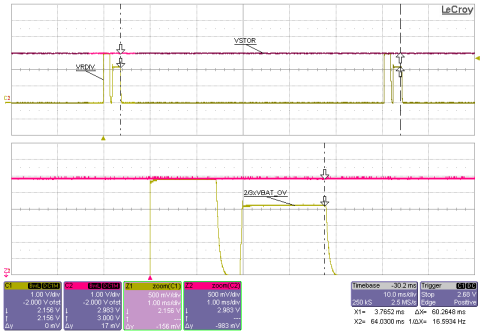
Figure 36. Boost Charger Operational Waveforms



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

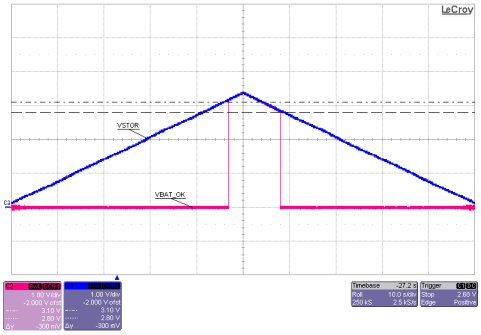
Figure 37. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT_SEC = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 38. VRDIV Waveform



VIN_DC floating

No storage element on VBAT or VBAT_PRI

VSTOR artifically ramped from 0 V to 3.3 V to 0 V using a function generator

Figure 39. VBAT_OK Operation

9 Power Supply Recommendations

See *Energy Harvester Selection* and *Storage Element Selection* for guidance on sizing the energy harvester and storage elements for the system load.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1 uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost charger inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. It is best to use vias and bottom traces for connecting the inductor to its respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example, from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPad should not be used as a power ground return path.

The remaining pins are either NC pins, that should be connected to the PowerPad as shown below, or digital signals with minimal layout restrictions. See the Figure 40 for an example layout.

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. In addition, the sample and hold circuit output capacitor on VREF_SAMP must hold the voltage for 16 s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 Mohm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

10.2 Layout Example

The VSS pins on each side of the IC are tied together using vias from top ground pours (red) down to the bottom ground plane (green).

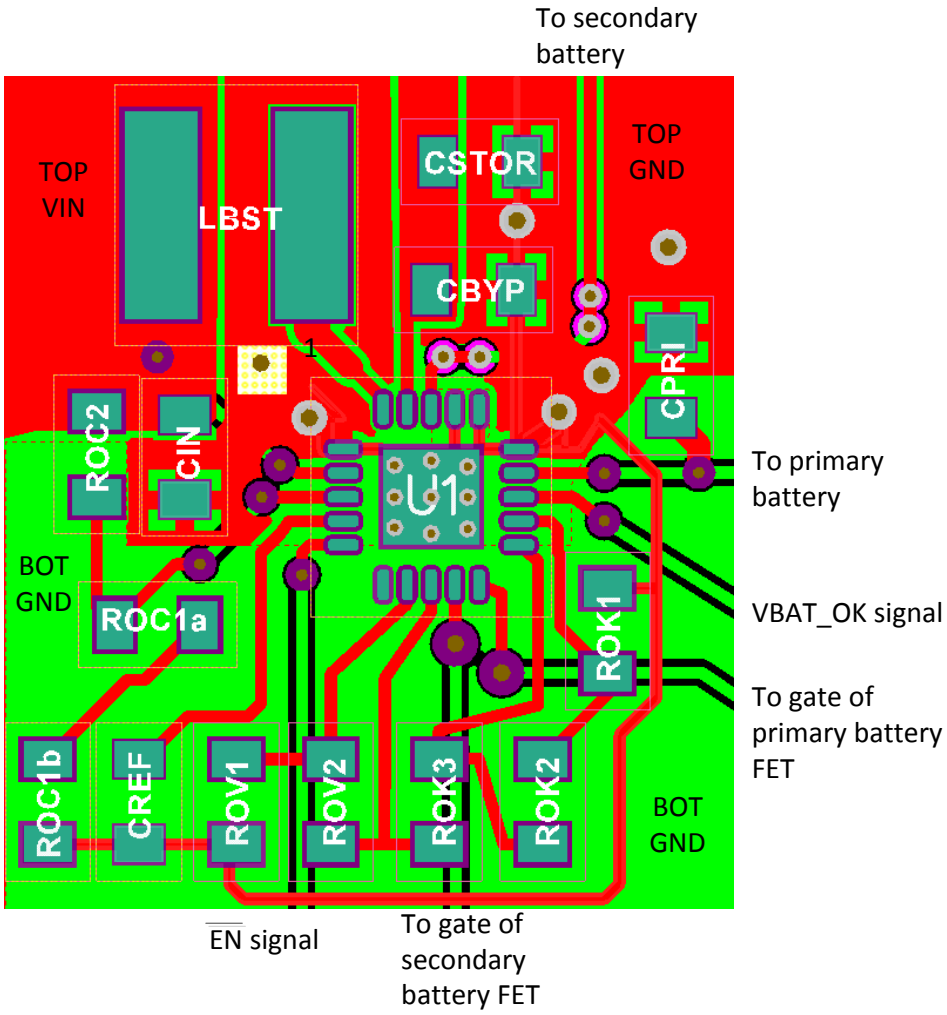


Figure 40. Layout Example

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Zip Files

- http://www.ti.com/lit/zip/SLUC484
- http://www.ti.com/lit/zip/SLUC463

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- EVM User's Guide, SLUUAA8
- Thermal Characteristics Application Note, SZZA017
- IC Package Thermal Metrics Application Note, SPRA953

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25505RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ505	Samples
BQ25505RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ505	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

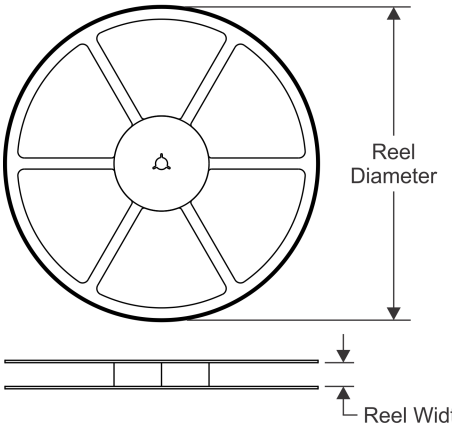
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

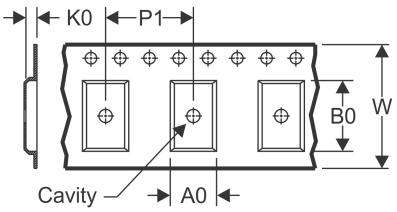
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

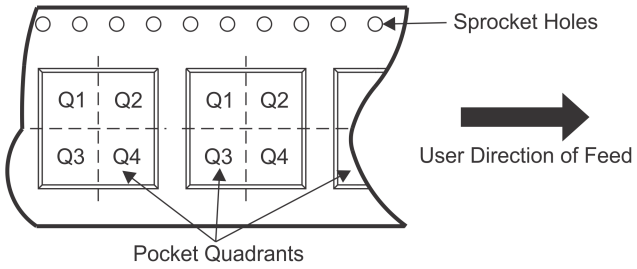


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

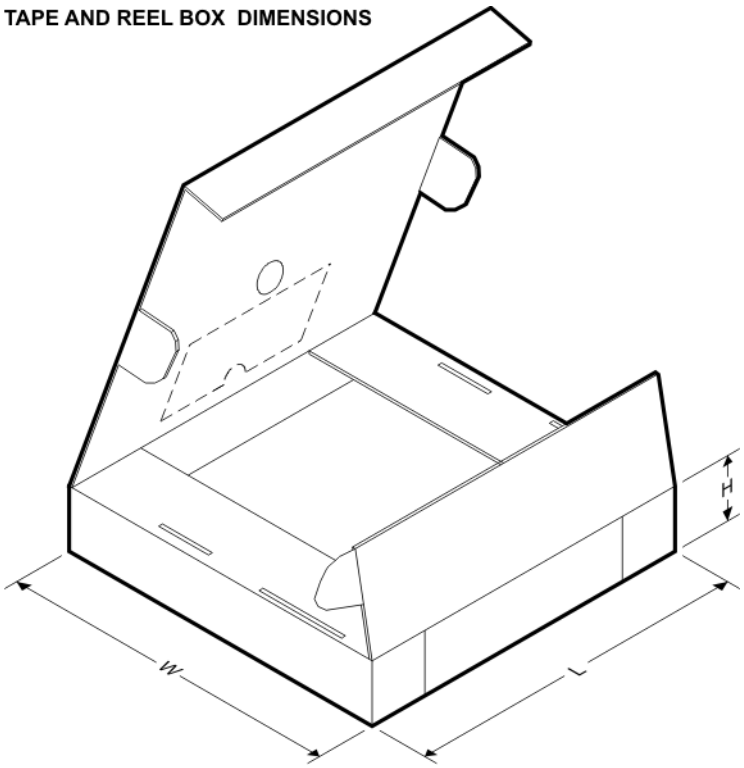
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25505RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ25505RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

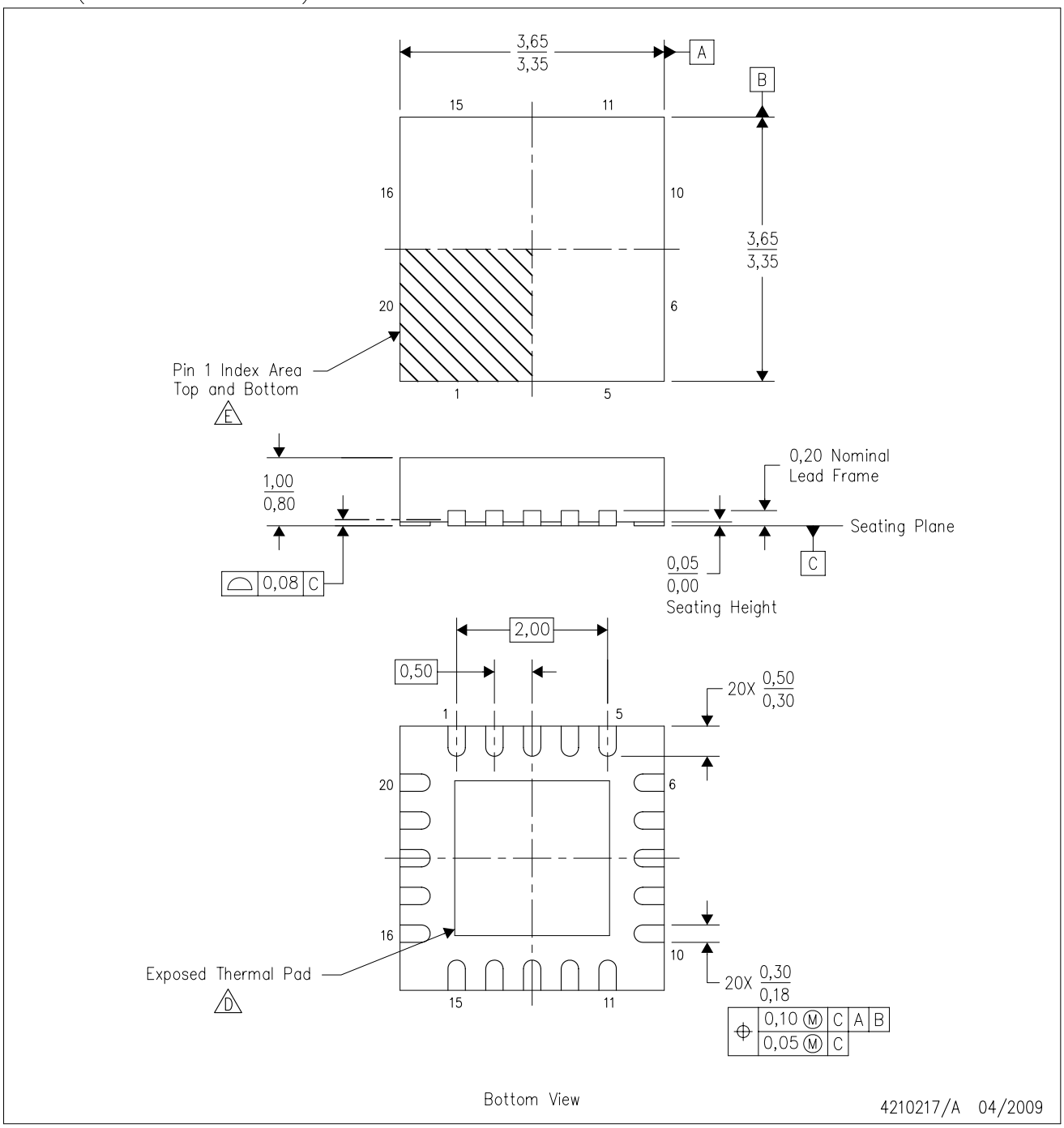
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25505RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
BQ25505RGRT	VQFN	RGR	20	250	210.0	185.0	35.0

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

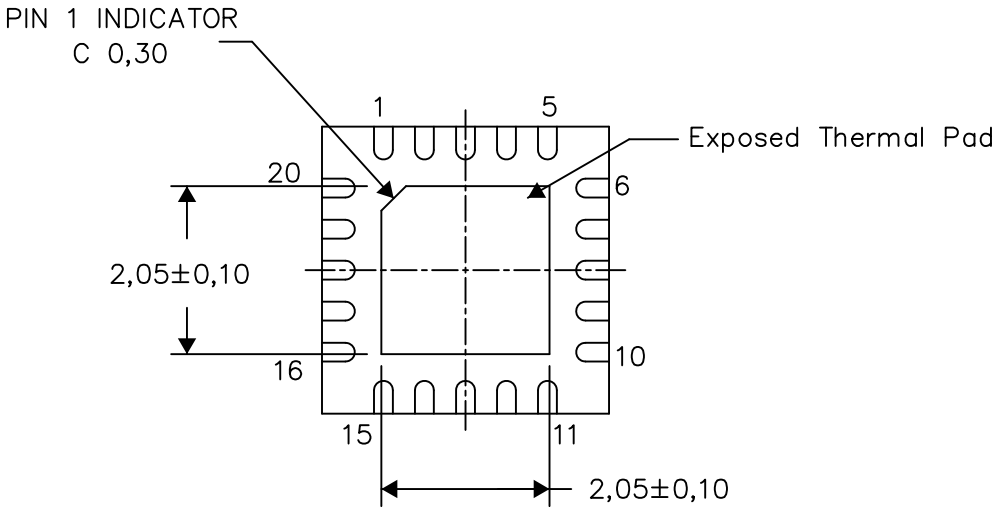
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



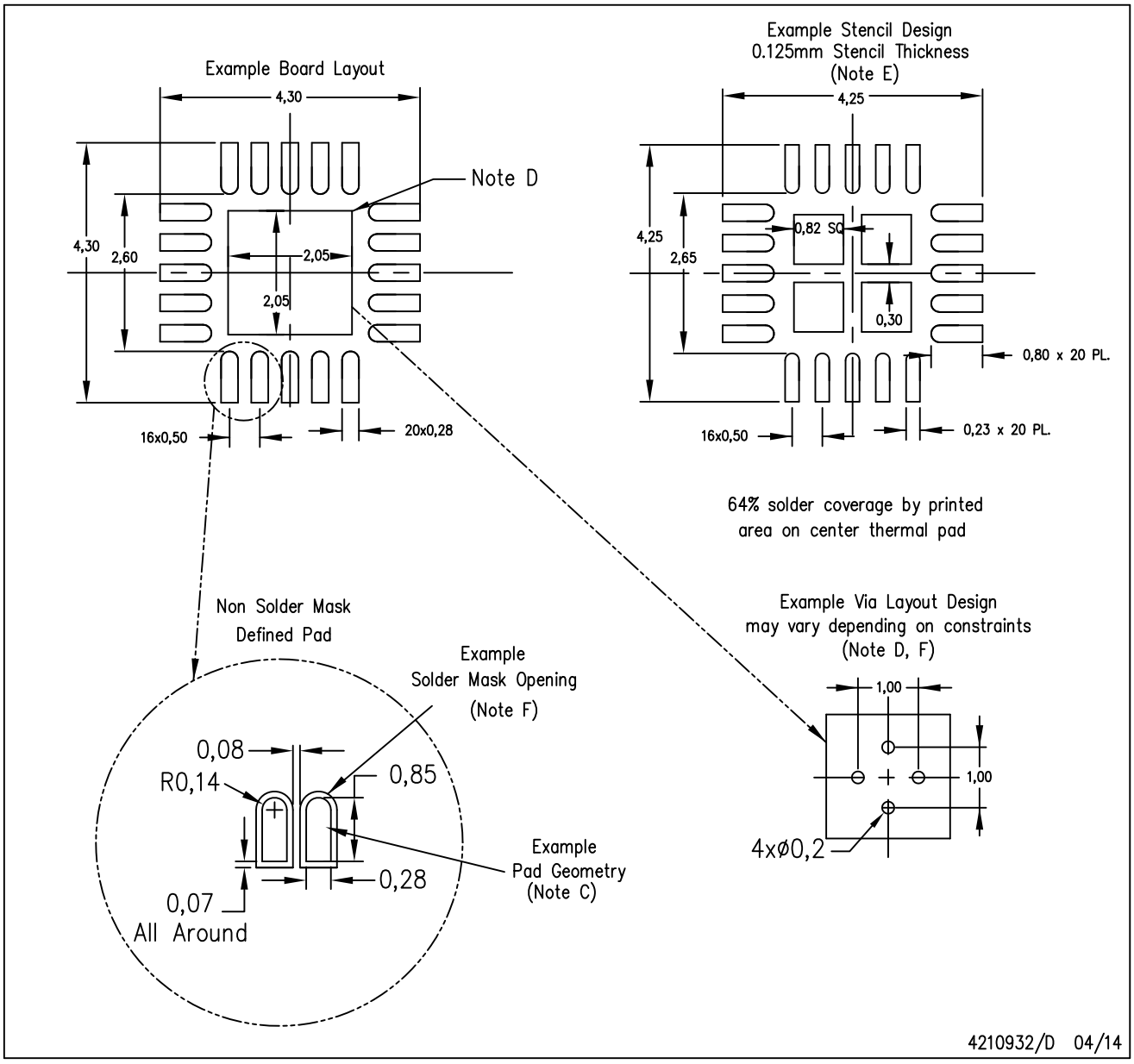
Bottom View

Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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