带有电源路径管理的 2.5A，单输入、单节开关模式锂离子电池充电器

查询样品: bq24278

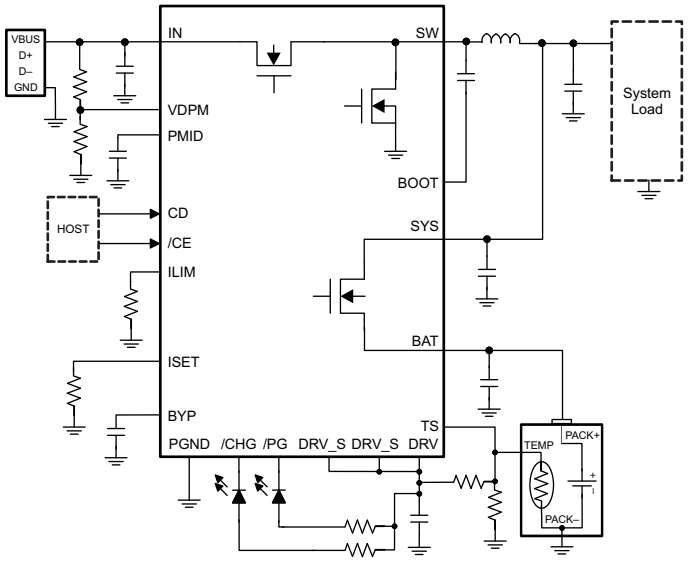
特性

- 具有独立电源路径控制的高效开关模式充电器
  - 从深度放电电池或者在无电池的情况下快速启动系统
- 额定 **20V** 输入，带有 **10.5V** 过压保护 **(OVP)**
- 集成场效应晶体管 **(FET)** 可使充电率高达 **2.5A**
- 用于电源路径管理的高度集成电池 **N** 通道金属氧化物半导体场效应晶体管 **(MOSFET)** 控制器
- 安全且准确的电池管理功能
  - 电池调节精度 **0.5%**
  - 充电电流精度 **10%**
- 基于电压的、负温度系数热敏电阻 **(NTC)** 监控输入 **(TS)**
  - 标准温度范围
- 用于输出电流控制的热调节保护
- 低电池漏电流，**BAT**（电池）短路保护
- 软启动特性以降低涌入电流
- 热关断和保护
- 采用小型 **49** 焊球晶圆级芯片封装 **(WCSP)** 或者四方扁平无引线 **(QFN)-24** 封装

应用范围

- 手持产品
- 便携式媒体播放器
- 便携式设备
- 上网本和便携式互联网器件

应用电路原理图



说明

bq24278 高度集成的单节锂离子电池充电器和系统电源路径管理器件针对空间有限且带有高容量电池的便携式应用。 单节充电器由一个诸如 AC（交流）适配器或者无线电源的专用充电源供电运行。

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

说明（继续）

此电源路径管理特性使得 bq24278 能够在为电池独立充电的同时从一个高效 DC 到 DC 转换器为系统供电。 此充电器一直监视电池电流并在系统负载所需电流超过输入电流限制时减少充电电流。 这样可实现正常的充电终止和定时器运行。 系统电压被调节至电池电压，但不会下降至低于 3.5V。 最小系统电压支持使得此系统能够与一个残次品或者有缺失的电池组一起运行并且即使在电池完全放电或者无电池的情况下也可实现瞬时系统启动。 当适配器不能传送峰值系统电流时，此电源路径管理架构还允许电池补充系统电流需要。 这样可使用较小的适配器。

电池充电经历以下三个阶段：充电，恒定电流和恒定电压。 在所有的充电阶段，一个内部控制环路监视 IC 结温并且在超过内部温度阀值的情况下减少充电电流。 此外，bq24278 提供一个基于电压的电池组热敏电阻器监控输入 (TS) 来监控电池温度以保证安全充电。

ORDERING INFORMATION

PART NUMBER	IN OVP	NTC MONITORING (TS)	JEITA COMPATIBLE	MINIMUM SYSTEM VOLTAGE	PACKAGE
bq24278YFFR	10.5 V	Yes	No	3.5 V	WCSP
bq24278YFFT	10.5 V	Yes	No	3.5 V	WCSP
bq24278RGER	10.5 V	Yes	No	3.5 V	QFN
bq24278RGET	10.5 V	Yes	No	3.5 V	QFN

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range (with respect to VSS)	IN	–2	20	V
	PMID, BYP, BOOT	–0.3	20	V
	SW	–0.7	12	V
	SYS, BAT, BGATE, DRV, $\overline{PG}$, $\overline{CHG}$, $\overline{CE}$, CD, TS, DRV_S, ILIM, ISET, VDPM	–0.3	7	V
BOOT to SW		–0.3	7	V
Output current (continuous)	SW		4.5	A
	SYS		3.5	A
Input current (continuous)	IN		2.75	A
Output sink current	$\overline{PG}$, $\overline{CHG}$		10	mA
Operating free-air temperature range		-40	85	°C
Junction temperature, T_J		-40	125	°C
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

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THERMAL INFORMATION

THERMAL METRIC(1)		bq24278		UNITS
		YFF (48 PINS)	QFN (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	49.8	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	30.5	
θ_{JB}	Junction-to-board thermal resistance	1.1	3.3	
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	6.6	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	2.6	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：SPRA953）。

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.2	18(1)	V
	IN operating range	4.2	10	
I_{IN}	Input current IN input		2.5	A
I_{SYS}	Ouput Current from SW, DC		3	A
I_{BAT}	Charging		2.5	A
	Discharging, using internal battery FET		2.5	
T_J	Operating junction temperature range	0	125	ºC

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of Figure 2, $VU_{VLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input quiescent current	$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM switching		15		mA
		$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM NOT switching			5	
		0°C < T_J < 85°C, High-Z Mode			175	µA
$I_{BATLEAK}$	Leakage current from BAT to the supply	0°C< T_J < 85°C, V_{BAT} = 4.2V, V_{IN} = 0 V			5	µA
I_{BAT_HIZ}	Battery discharge current in High Impedance mode (BAT, SW, SYS)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0 V or 5 V, High-Z Mode			55	µA
POWER PATH MANAGEMENT						
$V_{SYS(REG)}$	System regulation voltage	$V_{BAT} < V_{MINSYS}$	3.6	3.7	3.82	V
$V_{SYSREGFETOFF}$		Battery FET turned off, Charge disable or termination	4.26	4.33	4.37	
V_{MINSYS}	Minimum system regulation voltage	$V_{BAT} < V_{MINSYS}$, Input current limit or VINDPM active	3.4	3.5	3.62	V
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} > 2.5 V		V_{BAT} – 40mV		V
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} > 2.5 V		V_{BAT} – 10mV		V
$I_{LIM(Discharge)}$	Current limit, discharge or supplement mode	Current monitored in internal FET only		7		A
$t_{DGL(SC1)}$	Deglitch time, OUT short circuit during discharge or supplement mode	Measured from (V_{BAT} – V_{SYS}) = 300 mV to V_{BGATE} = (VBAT – 600 mV)		250		µs
$t_{REC(SC1)}$	Recovery time, OUT short circuit during discharge or supplement mode			60		ms
	Battery range for BGATE operation		2.5		4.5	V

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ELECTRICAL CHARACTERISTICS (continued)

Circuit of , $VU_{VLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BATTERY CHARGER							
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2 V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
V_{BATREG}	Battery regulation voltage	T_A = 25°C		4.179	4.2	4.221	V
		$V_{WARM} < V_{TS} < V_{COOL}$		4.160	4.2	4.24	
		T_A = 25°C		4.04	4.06	4.08	
		$V_{HOT} < V_{TS} < V_{WARM}$		4.02	4.06	4.1	
I_{CHARGE}	Charge current programmable range	$I_{CHARGE} = \frac{K_{ISET}}{R_{ISET}}$		550		2500	mA
K_{ISET}	Programmable fast charge current factor	T_A = 0°C to 125°C, $V_{WARM} < V_{TS} < V_{COOL}$		400	490	560	AΩ
		T_A = 0°C to 125°C, $V_{COLD} < V_{TS} < V_{COOL}$		225	245	270	
$V_{BATSHRT}$	Battery short threshold	V_{BAT} Rising		2.9	3.0	3.1	V
$V_{BATSHRThys}$	Battery short threshold hysteresis	V_{BAT} Falling			100		mV
$I_{BATSHRT}$	Battery short current	$V_{BAT} < V_{BATSHRT}$			50.0		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short to fast charge transition				32		ms
I_{TERM}	Termination charge current	$I_{CHARGE} \le$ 1A		7	10	11.5	$\%I_{CHARGE}$
		I_{CHARGE} >1A		8	10	11	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns			32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}			120		mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL} = 100 ns			32		ms
I_{DETECT}	Battery detection current before charge done (sink current)				2.5		mA
t_{DETECT}	Battery detection time				250		ms
INPUT PROTECTION							
I_{INLIM}	Maximum input current limit programmable range for IN input	$I_{INLIM} = \frac{K_{ILIM}}{R_{ILIM}}$		1000		2500	mA
K_{ILIM}	Maximum input current factor for IN input			238	251	264	AΩ
$V_{IN\_DPM\_IN}$	VIN_DPM threshold programmable range for IN Input			4.2		10	V
	VDPM threshold			1.18	1.2	1.22	V
V_{DRV}	Internal bias regulator voltage			5	5.2	5.45	V
I_{DRV}	DRV Output current			10			mA
V_{DO_DRV}	DRV Dropout voltage ($V_{IN} - V_{DRV}$)	I_{IN} = 1A, V_{IN} = 5 V, I_{DRV} = 10 mA				450	mV
V_{UVLO}	IC active threshold voltage	V_{IN} rising		3.6	3.8	4.0	V
V_{UVLO_HYS}	IC active hysteresis	V_{IN} falling from above V_{UVLO}			150		mV
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V ≤ V_{BAT} ≤ V_{OREG}, V_{IN} falling		0	40	100	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis	2.0 V ≤ V_{BAT} ≤ V_{OREG}		40	100	160	mV
	Deglitch time for supply rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns			30		ms
V_{OVP}	Input supply OVP threshold voltage	IN, V_{IN} Rising		10.3	10.5	10.7	V
$V_{OVP(HYS)}$	V_{OVP} hysteresis	Supply falling from V_{OVP}			100		mV
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge		1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
	VB_{OVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}			1		% of V_{BATREG}
$V_{BATUVLO}$	Battery UVLO threshold voltage				2.5		V
I_{LIMIT}	Cycle by Cycle current limit			4.1	4.9	5.6	A
$T_{SHUTDWN}$	Thermal shutdown	10C Hysteresis			165		C
T_{REG}	Thermal regulation threshold				120		C
	Safety Timer			324	360	396	min
$\overline{CE}$, CD, $\overline{PG}$, $\overline{CHG}$							
V_{IH}	Input high threshold			1.3			V
V_{IL}	Input low threshold					0.4	V
I_{IH}	High-level leakage current	$V_{\overline{CHG}}$ = $V_{\overline{PG}}$ = 5 V				1	µA
V_{OL}	Low-level output saturation voltage	I_O = 10 mA, sink current				0.4	V
PWM CONVERTER							

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ELECTRICAL CHARACTERISTICS (continued)

Circuit of , $VU_{VLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 500 mA, Measured from V_{IN} to PMIDU		95	175	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMIDU to SW		100	175	mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		65	115	mΩ
f_{OSC}	Oscillator frequency		1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0			
BATTERY-PACK NTC MONITOR						
V_{HOT}	High temperature threshold	V_{TS} falling	29.7	30	30.5	%VDRV
$V_{HYS(HOT)}$	Hysteresis on high threshold	V_{TS} rising		1		
V_{COLD}	Low temperature threshold	V_{TS} rising	59.5	60	60.4	
V_{WARM}	Warm temperature threshold	V_{TS} falling	37.9	38.3	39.6	
$V_{HYS(WARM)}$	Hysteresis on warm threshold	V_{TS} rising		1		
V_{COOL}	Cool temperature threshold	V_{TS} rising	56.0	56.5	56.9	
$V_{HYS(COOL)}$	Hysteresis on cool threshold	V_{TS} falling		1		
$V_{HYS(COLD)}$	Hysteresis on low threshold	V_{TS} falling		1		
TSOFF	TS Disable threshold	V_{TS} rising, 2% V_{DRV} Hysteresis	70		73	
$t_{DGL(TS)}$	Deglitch time on TS change			50		ms

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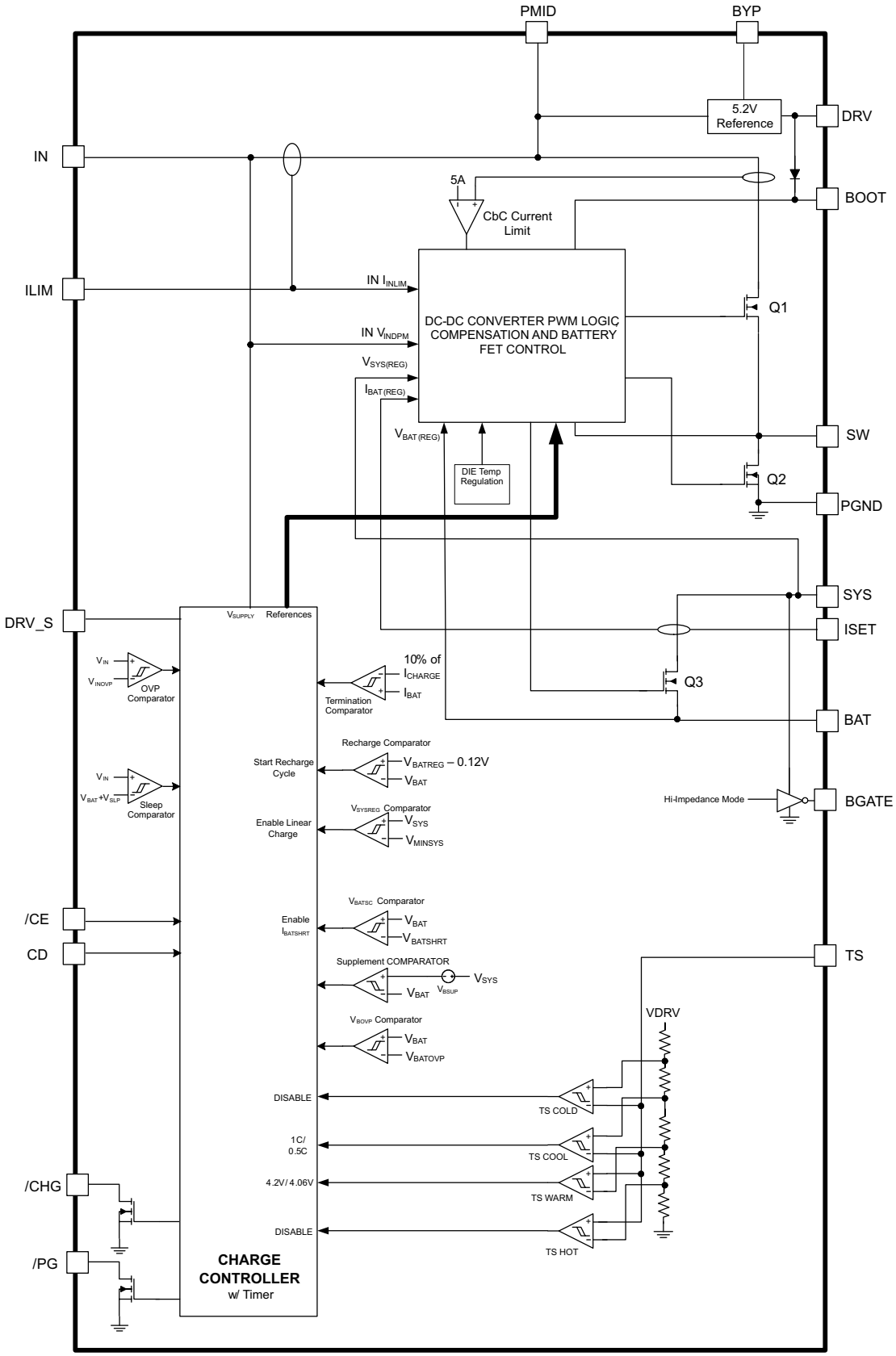
BLOCK DIAGRAM



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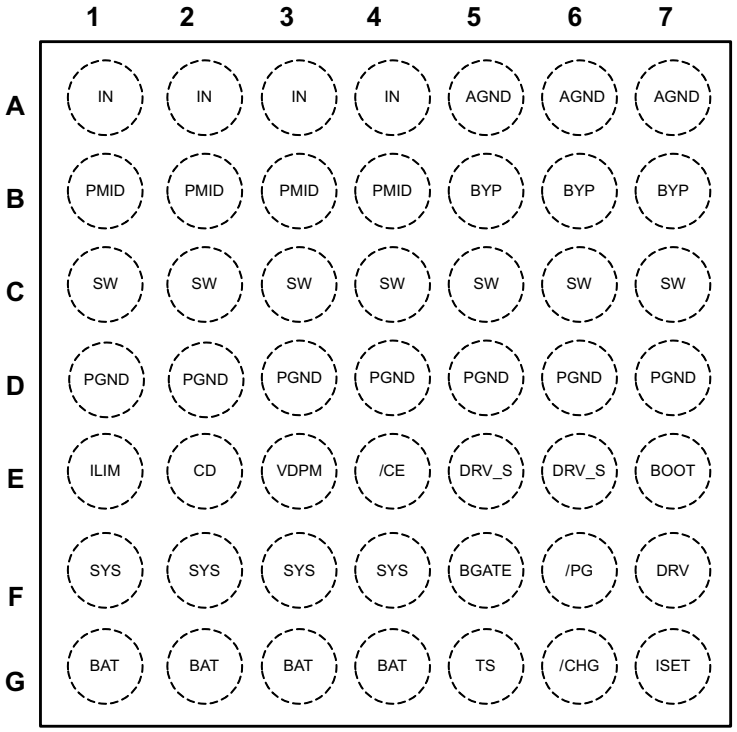
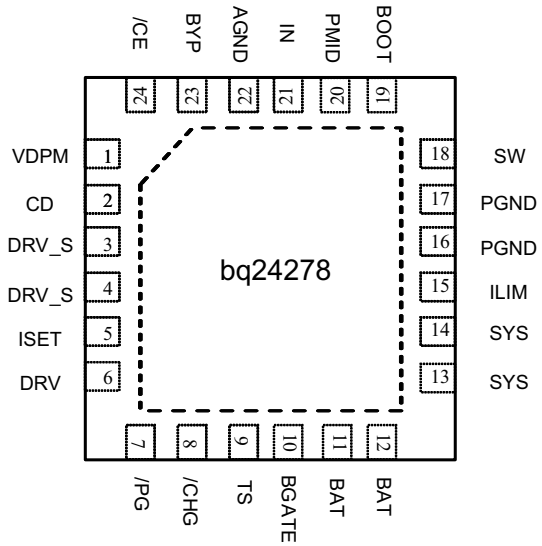
PIN CONFIGURATION

49-BALL WCSP
(TOP VIEW)



24-PIN QFN
(TOP VIEW)



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PIN FUNCTIONS

PIN			I/O	DESCRIPTION
NAME	NUMBER		I/O	
	YFF	RGE		
IN	A1-A4	21	I	Input power supply. IN is connected to the external DC supply (AC adapter or alternate power source). Bypass IN to PGND with at least a 1µF ceramic capacitor.
AGND	A5-A7	22	I	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
PMID	B1-B4	20	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for High Power Input. Bypass PMID to PGND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMID. The PMID output is not current limited. Any short on PMID will result in damage to the IC.
BYP	B5-B7	23	O	Bypass for internal supply. Bypass BYP to GND with at least a 0.1µF ceramic capacitor.
SW	C1–C7	18	O	Inductor Connection. Connect to the switched side of the external inductor.
PGND	D1–D7	16, 17	—	Ground terminal for Switching FET. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
ILIM	E1	15	I	IN Input Current Limit Programming Input. Connect a resistor from ILIM to GND to program the input current limit for IN. The current limit is programmable from 1A to 2.5A.
CD	E2	2	I	IC Hardware Disable Input. Drive CD high to place the bq24278 in high-z mode. Drive CD low for normal operation.
VDPM	E3	1	I	Input DPM Programming Input. Connect a resistor divider from IN to PGND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management (VIN_DPM) threshold. The input current is reduced to maintain the supply voltage at $V_{IN_}$DPM. *See the Input Voltage based Dynamic Power* Management section for a detailed explanation.
$\overline{CE}$	E4	24	I	Charge Enable Input. $\overline{CE}$ is used to disable or enable the charge process. A low logic level (0) enables charging and a high logic level (1) disables charging. When charging is disabled, the SYS output remains in regulation, but BAT is disconnected from SYS. Supplement mode is still available if the system load demands cannot be met by the supply.
DRV_S	E5, E6	3, 4	I	Supply for Internal Circuits. Connect DRV_S to DRV directly.
BOOT	E7	19	I	High Side MOSFET Gate Driver Supply. Connect a 0.01µF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
SYS	F1–F4	13,14	I/O	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with 1µF.
BGATE	F5	10	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during supplement mode and when no input is connected.
$\overline{PG}$	F6	7	I	Power Good Open Drain Output. /PG is pulled low when a valid supply is connected to IN. A valid supply is between V_{BAT}+V_{SLP} and V_{OVP}. If no supply is connected or the supply is out of this range, $\overline{PG}$ is high impedance.
DRV	F7	6	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{SUPPLY} > V_{UVLO}$ and $V_{SUPPLY} > (V_{BAT} + V_{SLP})$
BAT	G1–G4	11, 12	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with a 1µF capacitor.
TS	G5	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function in the bq24278 provides 2 thresholds for Hot/ Cold shutoff, with 2 additional thresholds for JEITA compliance. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
$\overline{CHG}$	G6	8	O	Charge Status Open Drain Output. $\overline{CHG}$ is pulled low when a charge cycle starts and remains low while charging. $\overline{CHG}$ is high impedance when the charging terminates and when no supply exists. $\overline{CHG}$ does not indicate recharge cycles.
ISET	G7	5	I	Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 550mA to 2.5A.
Thermal Pad	—	Pad	—	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

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TYPICAL APPLICATION CIRCUIT

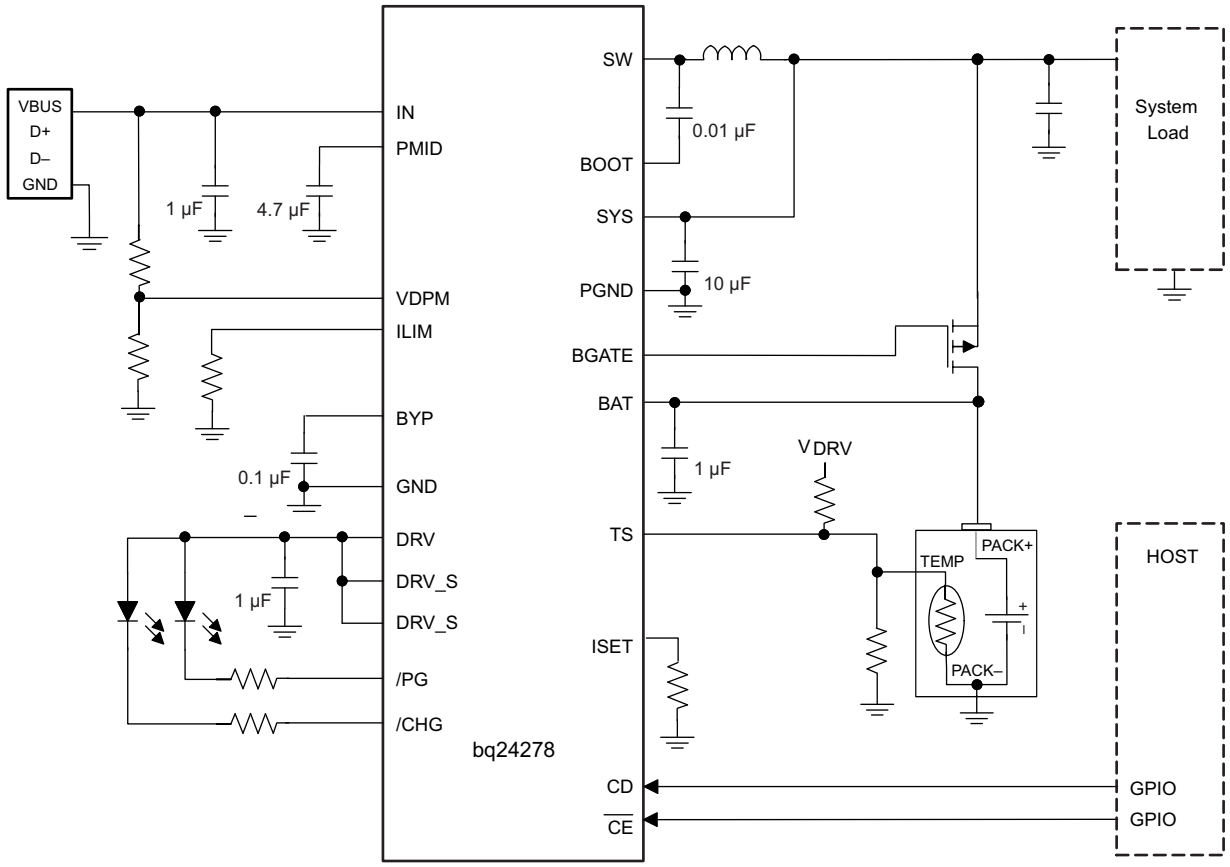

Figure 1. bq24278 Application Circuit, External Discharge FET Connected

DETAILED DESCRIPTION

The bq24278 is a highly integrated single cell Li-Ion battery charger and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The power path management feature allows the bq24278 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

Charge Mode Operation

Charge Profile

Charging is done through the internal battery MOSFET. When the battery voltage is above 3.5V, the system output (SYS) is connected to the battery to maximize the charging efficiency. There are 5 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), thermal regulation loop, minimum system voltage loop (MINSYS) and input voltage dynamic power management loop (V_{IN-DPM}). During the charging process, all five loops are enabled and the dominant one takes control. The bq24278 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The minimum system output feature regulates the system voltage to a minimum of $V_{SYS(REG)}$, so that startup is enabled even for a missing or deeply discharged battery. Figure 2 shows a typical charge profile including the minimum system output voltage feature.

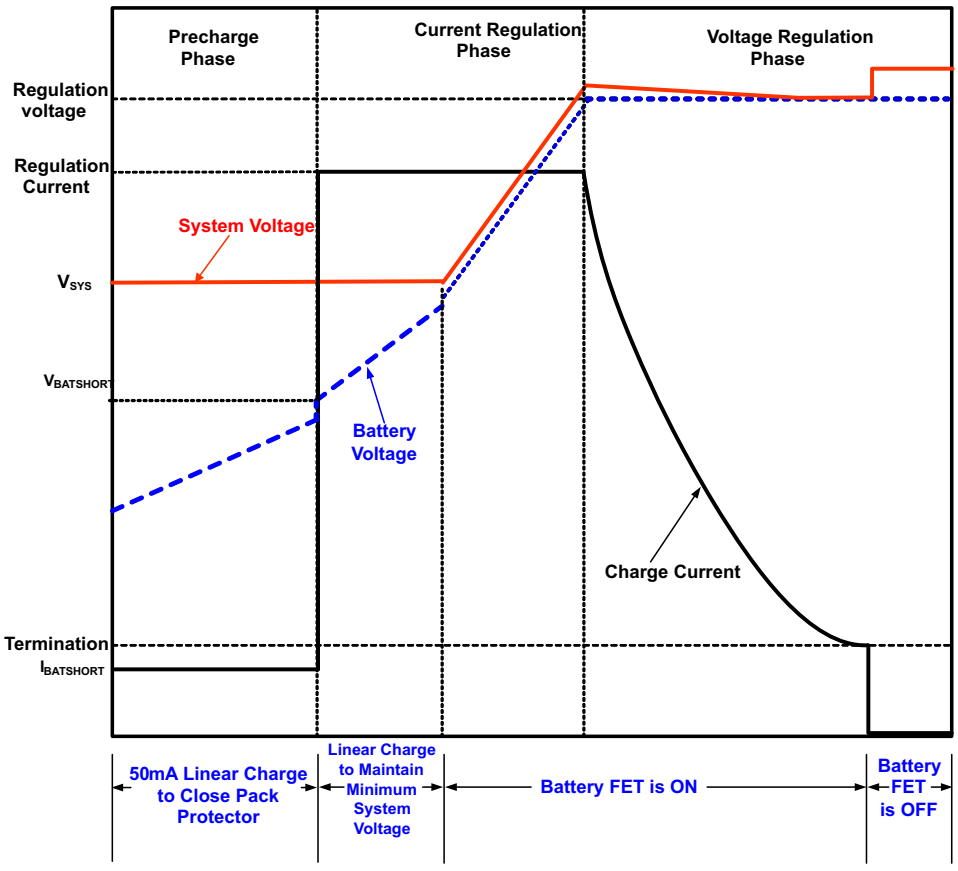

Figure 2. Typical Charging Profile of bq24278

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PWM Controller in Charge Mode

The bq24278 provides an integrated, fixed 1.5 MHz frequency voltage-mode controller with to power the system and supply the charge current. The converter is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR.

The bq24278 input scheme prevents battery discharge when the supply voltage is lower than V_{BAT}. The high-side N-MOSFET (Q1) switches to control the power delivered to SYS. The DRV LDO supplies the gate drive for the internal MOSFETs. The high-side MOSFET is supplied by a boot strap circuit with external boot-strap capacitor (BST).

The input is protected from short circuit by a cycle-by-cycle current limit that is sensed through the high-side MOSFET. The threshold is set to a nominal 5-A peak current. The input also utilizes an input current limit that limits the current from the power source.

Battery Charging Process

When the battery is deeply discharged or shorted, the bq24278 applies a 50mA current to charge the battery voltage up to acceptable charging levels. During this time, the battery FET is linearly regulated to maintain the system output regulation at $V_{SYS(REG)}$. Once the battery rises above V_{SHORT}, the charge current increases to the fastcharge current setting. The SYS voltage is regulated to $V_{SYS(REG)}$ while the battery is linearly charged through the battery FET. Additionally, the thermal regulation loop reduces the charge current to maintain the die temperature at safe levels. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so if the charge current is reduced, the reduced charge rate does not have a major negative effect on total charge time. If the current limit for the SYS output is reached (limited by the input current limit, or V_{IN_DPM}), the charge current is reduced to provide the system with all the current that is needed. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the "*Dynamic Power Path Management*" section for more details).

Once the battery is charged enough to where the system voltage begins to rise above V_{SYSREG} (depends on the charge current setting), the battery FET is turned on fully and the battery is charged with the programmed charge current programmed using the ISET input, I_{CHARGE}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The charge current is programmed by connecting a resistor from ISET to GND. The value for R_{ISET} is calculated using Equation 1.

$$R_{ISET} = \frac{K_{ISET}}{I_{CHARGE}} \quad (1)$$

Where I_{CHARGE} is the programmed fast charge current and K_{ISET} is the programming factor found in the Electrical Characteristics table.

The charge current is regulated to I_{CHARGE} until the battery is charged to the regulation voltage. Once the battery voltage is close to the regulation voltage, V_{BATREG}, the charge current is tapered down as shown in Figure 2 while the SYS output remains connected to the battery. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the BAT and PGND pins.

The bq24278 monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected and the battery voltage is above the recharge threshold, the bq24278 terminates charge and turns off the battery charging FET and begins battery detection. The system output is regulated to the $V_{BAT(REG)}$ voltage and supports the full current available from the input and the battery supplement mode (see the "*Dynamic Power Path Management*" section for more details) is still available.

A charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the $V_{BAT(REG)}$-V_{RCH} threshold.
2. V_{IN} Power-on reset (POR)
3. $\overline{CE}$ toggle
4. Toggle Hi-Impedance mode (using CD)

If the battery voltage is ever greater than $V_{BAT(REG)}$, the PWM converter is turned off and the battery is discharged to $V_{BAT(REG)}$. This prevents further overcharging the battery and allows the battery to discharge to safe operating levels.

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Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for t_{DETECT} to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of t_{DETECT}, a battery is determined to be present and the IC enters “Charge Done”. If V_{BAT} falls below V_{DETECT}, a “Battery Not Present” fault is signaled and battery detection continues. During the next cycle of battery detection, the bq24278 turns on $I_{BATSHORT}$ for t_{DETECT}. If V_{BAT} rises to V_{DETECT}, the current source is turned off and after t_{DETECT}, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is disabled when termination is disabled.

Dynamic Power Path Management

The bq24278 features a SYS output that powers the external system load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of SYS with a source connected to the supply or a battery source only.

Input Source Connected

When a source is connected to IN, and the bq24278 is enabled, the buck converter starts up. If charging is enabled using $\overline{CE}$, the charge cycle is initiated. When V_{BAT} > 3.5V, the SYS output is connected to V_{BAT}. If the SYS voltage falls to $V_{SYS(REG)}$, it is regulated to that point to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path management (DPPM) circuitry of the bq24278 monitors the SYS voltage continuously and if V_{SYS} falls to V_{MINSYS}, adjusts charge current to maintain the load on SYS while preventing the system voltage from crashing. If the charge current is reduced to zero and the load increases further, the bq24278 enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load. When the charge current is reduced by the DPPM regulation loop, the safety timer runs at half speed, so that it is twice a long. This prevents false safety timer faults. See the *Safety Timer* section for more details.

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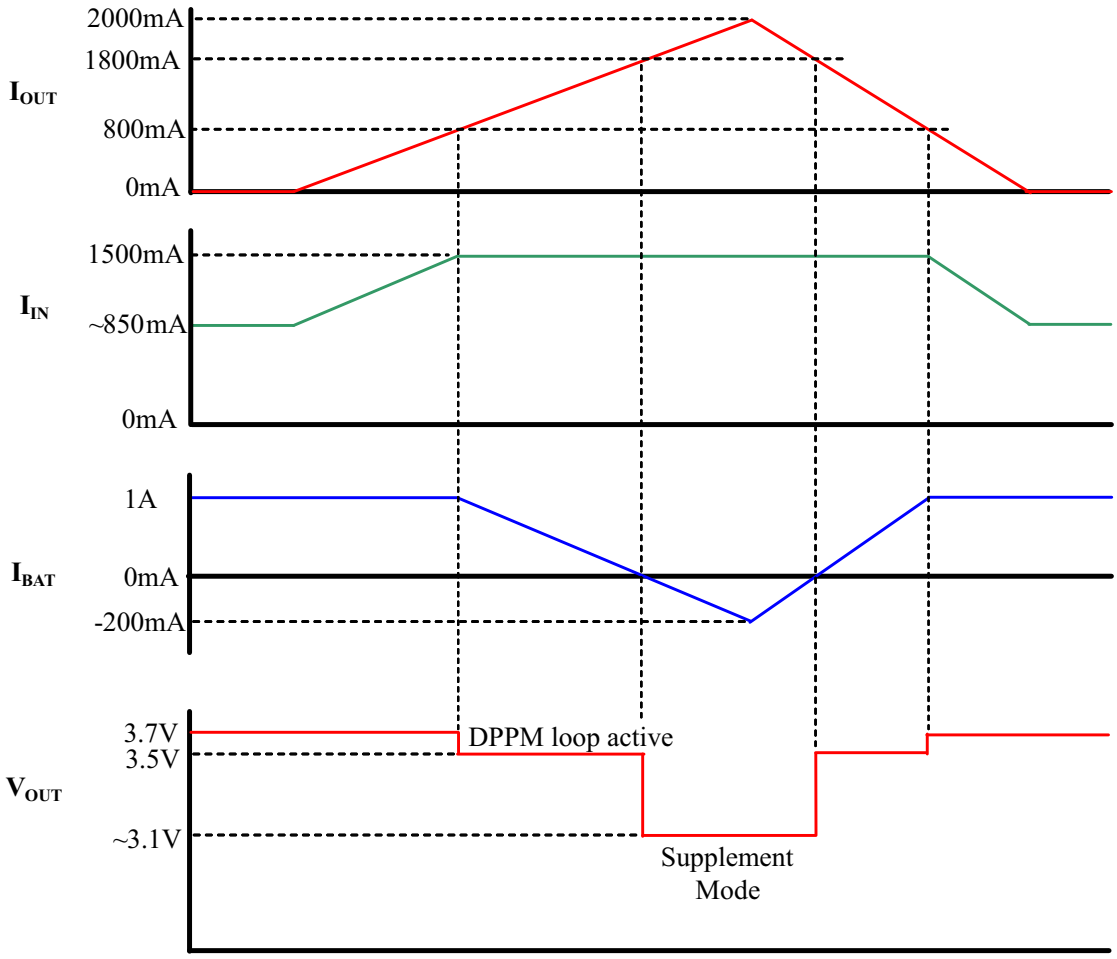

Figure 3. Example DPPM Response (V_{Supply}=5V, V_{BAT} = 3.1V, 1.5A Input current limit)

If the $V_{BAT(REG)}$ threshold is ever less than the battery voltage, the battery FET is turned off to allow the battery to relax down to $V_{BAT(REG)}$ and the SYS output is regulated to $V_{SYSREG(FETOFF)}$. If the battery is ever above V_{BOVP}, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels.

The input current limit for IN is programmable using the ILIM input. Connect a resistor from ILIM to GND to set the maximum input current limit. The programmable range for the IN input current limit is 1000mA to 2.5A. R_{ILIM} is calculated using Equation 2:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{IN\_LIM}} \quad (2)$$

Where I_{IN_LIM} is the programmed input current limit and K_{ILIM} is the programming factor found in the Electrical Characteristics table.

Battery Only Connected

When the battery is connected with no input source, the battery FET is turned on similar to supplement mode. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed.

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Battery Discharge FET (BGATE)

The bq24278 contains a MOSFET driver to drive an external P-Channel MOSFET between the battery and the system output. This external FET provides a low impedance path for supply the system from the battery. Connect BGATE to the gate of the external discharge MOSFET. BGATE is on under the following conditions:

1. No valid input supply connected.
2. CD=high (High-Impedance Mode)

This FET is optional and runs in parallel with the internal charge FET during discharge. Note that this FET is not protected by the short circuit current limit.

Safety Timer

At the beginning of charging process, the bq24278 starts the 6 hour safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the charge cycle is terminated and the battery FET is turned off. A new charge cycle must be entered using $\overline{CE}$ or High Impedance mode or input power must be toggled in order to clear the safety timer fault.

During the fast charge phase, several events increase the timer durations.

1. The system load current reduces the available charging current
2. The input current is reduced because the V_{INDPM} loop is preventing the supply from crashing.
3. The device has entered thermal regulation because the IC junction temperature has exceed $T_{J(REG)}$

During these events, the timer is slowed by half to extend the timer and prevent any false timer faults. Starting a new charge cycle by toggling the input, toggling the $\overline{CE}$ pin to disable/enable charge, resets the safety timer. Additionally, thermal shutdown events cause the safety timer to reset.

LDO Output (DRV)

The bq24278 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or other external circuitry. The LDO is on whenever a supply is connected to the input of the. The DRV is disabled under the following conditions:

1. V_{IN} < UVLO
2. $V_{IN} < V_{BAT} + V_{SLP}$
3. Thermal Shutdown

External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24278 provides a flexible, voltage-based TS input for monitoring the battery pack NTC thermistor, Figure 4. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The bq24278 enables the user to easily implement the JEITA standard for charging temperature. The JEITA specification is shown in Figure 5.

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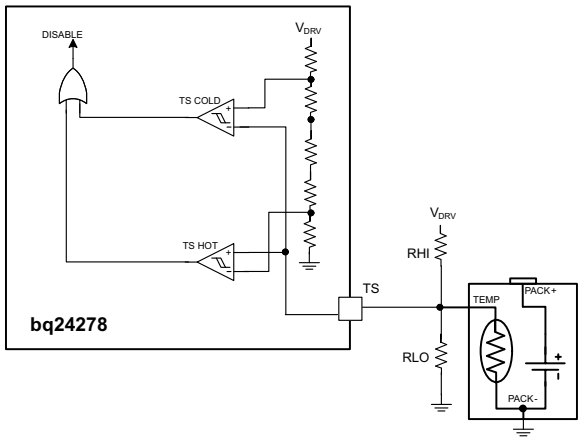

Figure 4. TS Circuit

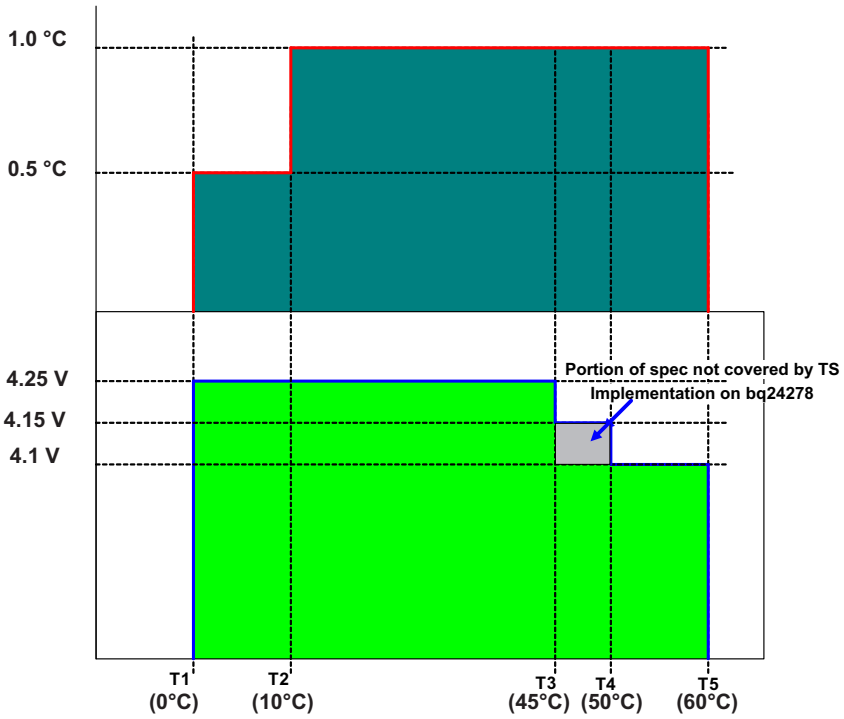

Figure 5. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{HOT} < V_{TS} < V_{WARM}, the battery regulation voltage is reduced by 140 mV from the programmed regulation threshold. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 10. The resistor values are calculated using the following equations:

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$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (3)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (4)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$
$V_{HOT} = 0.30 \times V_{DRV}$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

The WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using the following equations:

$$RCOOL = \frac{RLO \times 0.564 \times RHI}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (5)$$

$$RWARM = \frac{RLO \times 0.383 \times RHI}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (6)$$

Thermal Regulation and Protection

During the charging process, to prevent the IC from overheating, bq24278 monitor the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CF}. The charge current is reduced to zero when the junction temperature increases about 10°C above TCF. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the bq24278 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24278 suspends charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, and the timer is reset. The charging cycle resets when T_J falls below T_{SHTDWN} by approximately 10°C.

Input Voltage Protection in Charge Mode

Sleep Mode

The bq24278 enters the low-power sleep mode if the voltage on VIN falls below sleep-mode entry threshold, V_{BAT}+V_{SLP}, and V_{VBUS} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{IN}. When $V_{IN} < V_{BAT}$+ V_{SLP}, the bq24278 turns off the PWM converter, and turns the battery FET and BGATE on. Once $V_{IN} > V_{BAT}$+ V_{SLP}, the device initiates a new charge cycle.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage decreases. Once the supply drops to V_{IN_DPM} (set by VDPM), the input current limit is reduced down to prevent the further drop of the supply. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 6 shows the $V_{IN\text{-}DPM}$ behavior to a current limited source. In this figure the input source has a 750mA current limit and the charging is set to 750mA. The SYS load is then increased to 1.2A.

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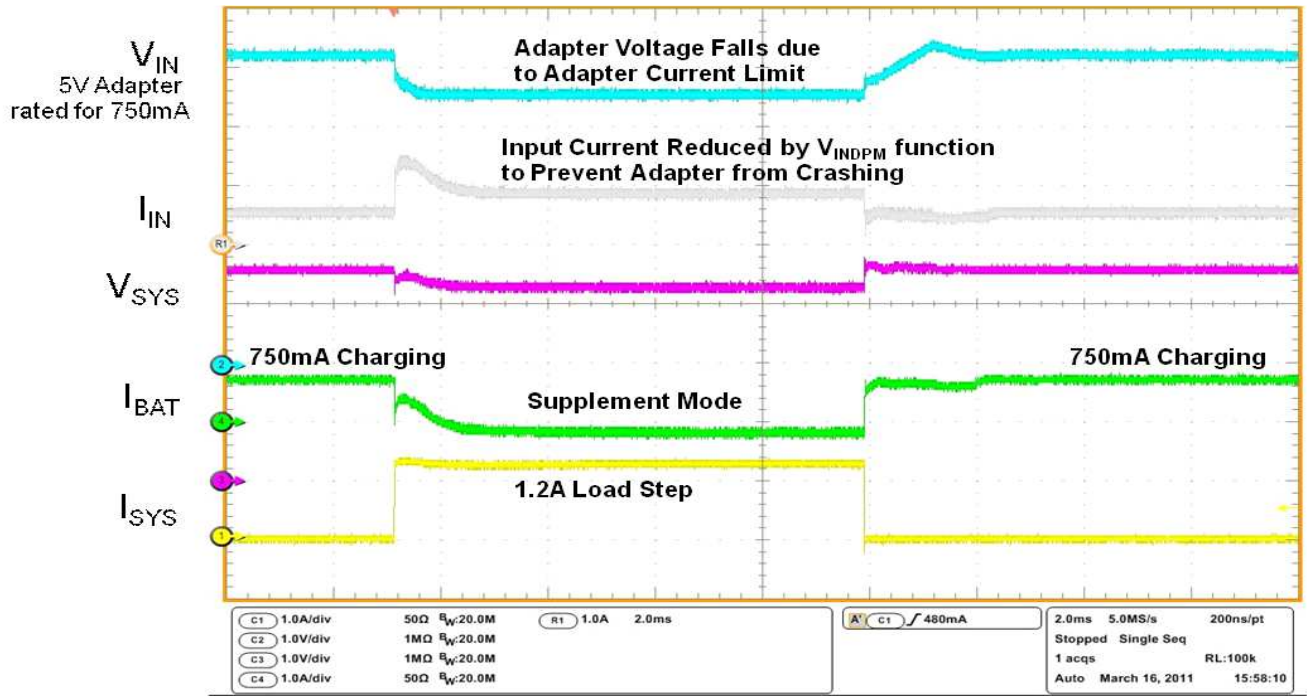

Figure 6. bq24278 V_{IN-DPM}

The VINDPM threshold for the IN input is set using a resistor divider with VDPM connected to the center tap. Select 10kΩ for the bottom resistor. The top resistor is selected using Equation 7:

$$RTOP = \frac{10k\Omega \times \left(V_{INDPM} - V_{DPM}\right)}{V_{DPM}} \quad (7)$$

Where V_{INDPM} is the desired V_{INDPM} threshold and V_{DPM} is the regulation threshold specified in the Electrical Characteristics table.

Bad Source Detection

When a source is connected to IN, the bq24278 runs a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (70mA) for 32ms. If the source is valid after the 32ms ($V_{BADSOURCE} < V_{IN} < V_{OVP}$), the buck converter starts up and normal operation continues. If the supply voltage falls below V_{BAD_SOURCE} during the detection, the current sink shuts off for 2s and then retries. The detection circuits retries continuously until a valid source is detected after the detection time. If during normal operation the source falls to V_{BAD_SOURCE}, the bq24278 turns off the PWM converter, turns the battery FET on and runs the bad source detection. Once a good source is detected, the device returns to normal operation.

Input Over-Voltage Protection

The bq24278 provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). When $V_{IN} > V_{OVP}$, the bq24278 turns off the PWM converter, suspends the charging cycle and turns the battery FET on. Once the OVP fault is removed, the device returns to the operation it was in prior to the OVP fault.

Status Indicators ($\overline{CHG}$, $\overline{PG}$)

The bq24278 contains two open-drain outputs that signal its status. The $\overline{PG}$ output indicates that a valid input source is connected to IN. $\overline{PG}$ is low when ($V_{BAT}+V_{SLP}$) < V_{IN} < V_{OVP}. When there is no supply connected to the input within this range, $\overline{PG}$ is high impedance. Table 1 illustrates the $\overline{PG}$ behavior under different conditions.

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The $\overline{CHG}$ output indicates new charge cycles. When a new charge cycle is initiated by $\overline{CE}$, toggling High Impedance mode or toggling the input power, $\overline{CHG}$ goes low and remains low until termination. After termination, $\overline{CHG}$ remains high impedance until a new charge cycle is initiated. $\overline{CHG}$ does not go low during recharge cycles. Table 2 illustrates the $\overline{CHG}$ behavior under different conditions.

Connect $\overline{PG}$ and $\overline{CHG}$ to the DRV output through an LED for visual indication, or connect through a 100kΩ pullup to the required logic rail for host indication.

Table 1. $\overline{PG}$ Status Indicator

CHARGE STATE	$\overline{PG}$ BEHAVIOR
$V_{IN} < V_{UVLO}$	High-Impedance
$V_{IN} < (V_{BAT}+V_{SLP})$	High-Impedance
$(V_{BAT}+V_{SLP}) < V_{IN} < V_{OVP}$	Low
$V_{IN} > V_{OVP}$	High-Impedance

Table 2. $\overline{CHG}$ Status Indicator

CHARGE STATE	$\overline{CHG}$ BEHAVIOR
Charge in progress	Low (first charge cycle) High-Impedance (recharge cycles)
Charging suspended by thermal loop	
Charge Done	High-Impedance
Recharge Cycle after Termination	
Timer Fault	
No Valid Supply, $V_{IN}>V_{OVP}$ or $V_{IN} < V_{SLEEP}$	
No Battery Present	

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APPLICATION INFORMATION

Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24278 is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 8 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (8)$$

The inductor selected must have a saturation current rating less than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24278, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times)I_{PEAK} - I_{LOAD}) = 1.5\ A + 0.2 \times (2.5\ A - 1.5\ A) = 1.7\ A \quad (9)$$

The bq24278 provides internal loop compensation. Using this scheme, the bq24278 is stable with 10µF to 200µF of local capacitance. The capacitance on the SYS rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS.

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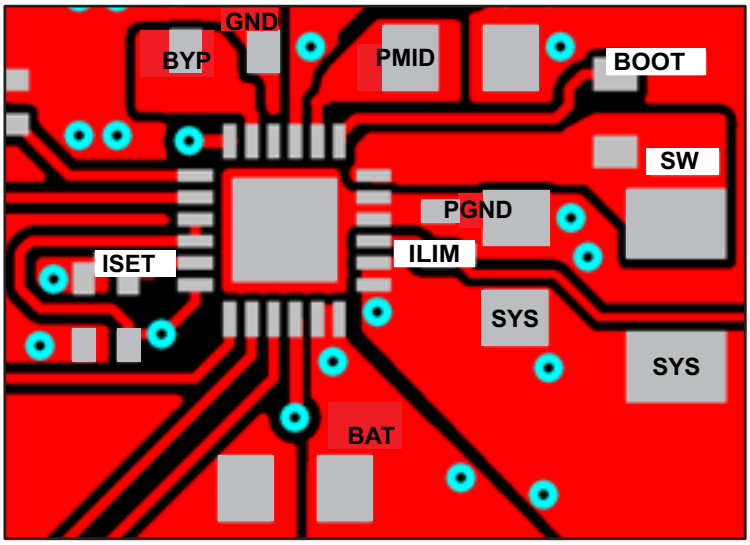
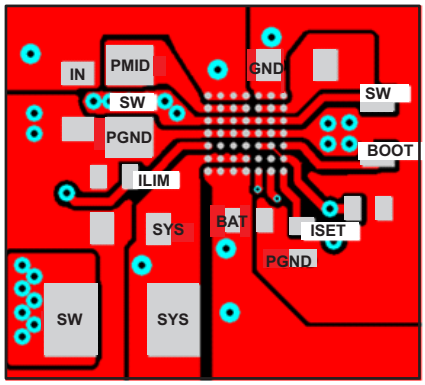
PCB Layout Guidelines

It is important to pay special attention to the PCB layout. Figure 7 provides a sample layout for the high current paths of the bq24278.



(RGE Package)

Figure 7. Recommended bq24278 PCB Layout for RGE Device



(YFF Package)

Figure 8. Recommended bq24278 PCB Layout for YFF Device

The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq24278
- Place 4.7µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID.
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place ISET resistor very close to the ISET pin.
- Place ILIM resistor very close to the ILIIM pin.
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is

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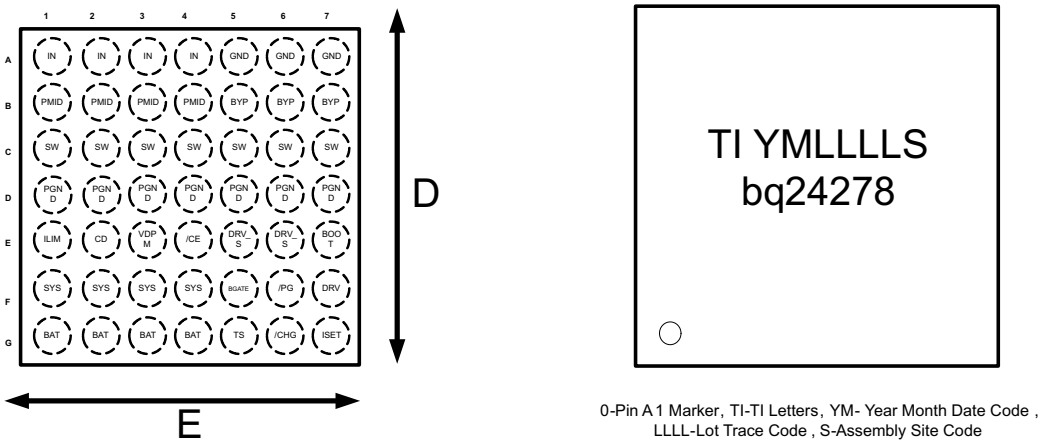
also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.

- The high-current charge paths into IN, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

PACKAGE SUMMARY



0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code , LLLL-Lot Trace Code , S-Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The bq2427x devices are available in a 49-bump chip scale package (YFF, NanoFree™). The package dimensions are :

D – 2.78mm ± 0.05mm
E – 2.78mm ± 0.05mm

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24278RGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24278	
BQ24278RGET	NRND	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24278	
BQ24278YFFR	NRND	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24278	
BQ24278YFFT	NRND	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24278	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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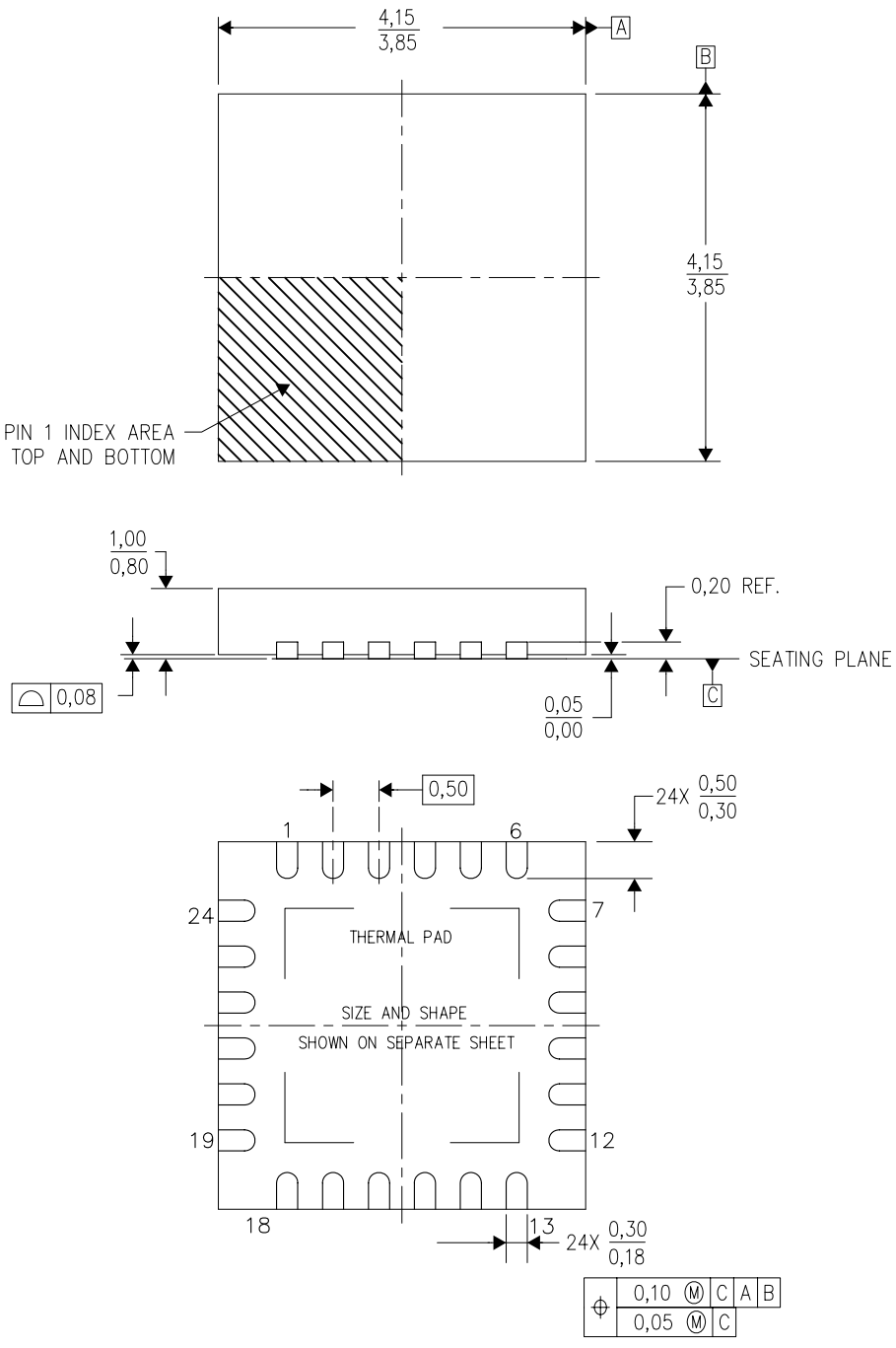
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

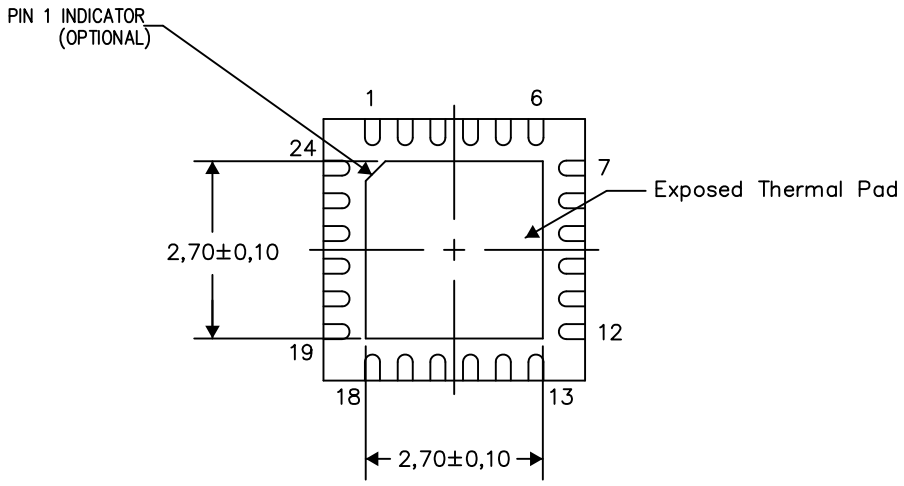
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



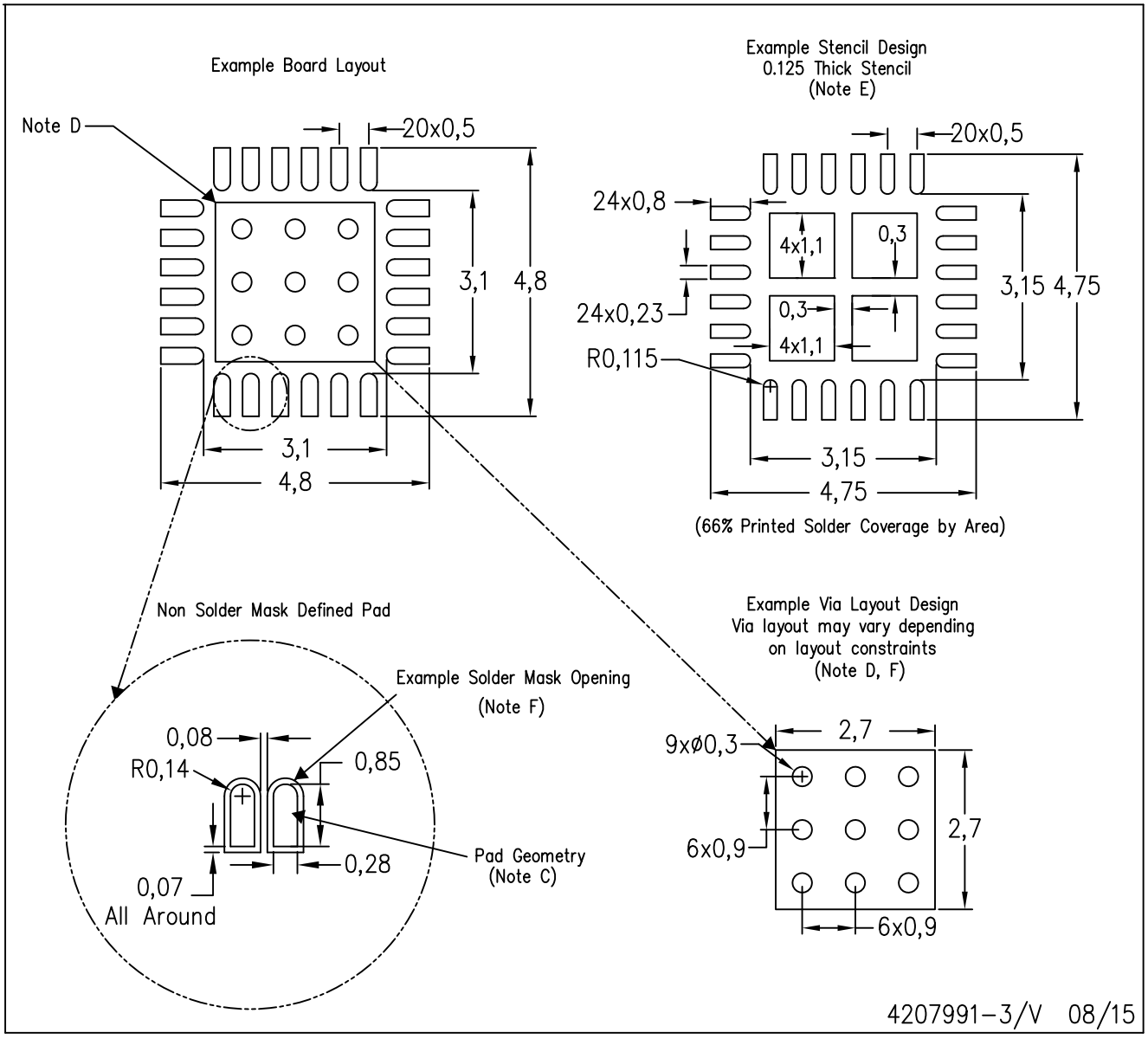
Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AK 08/15

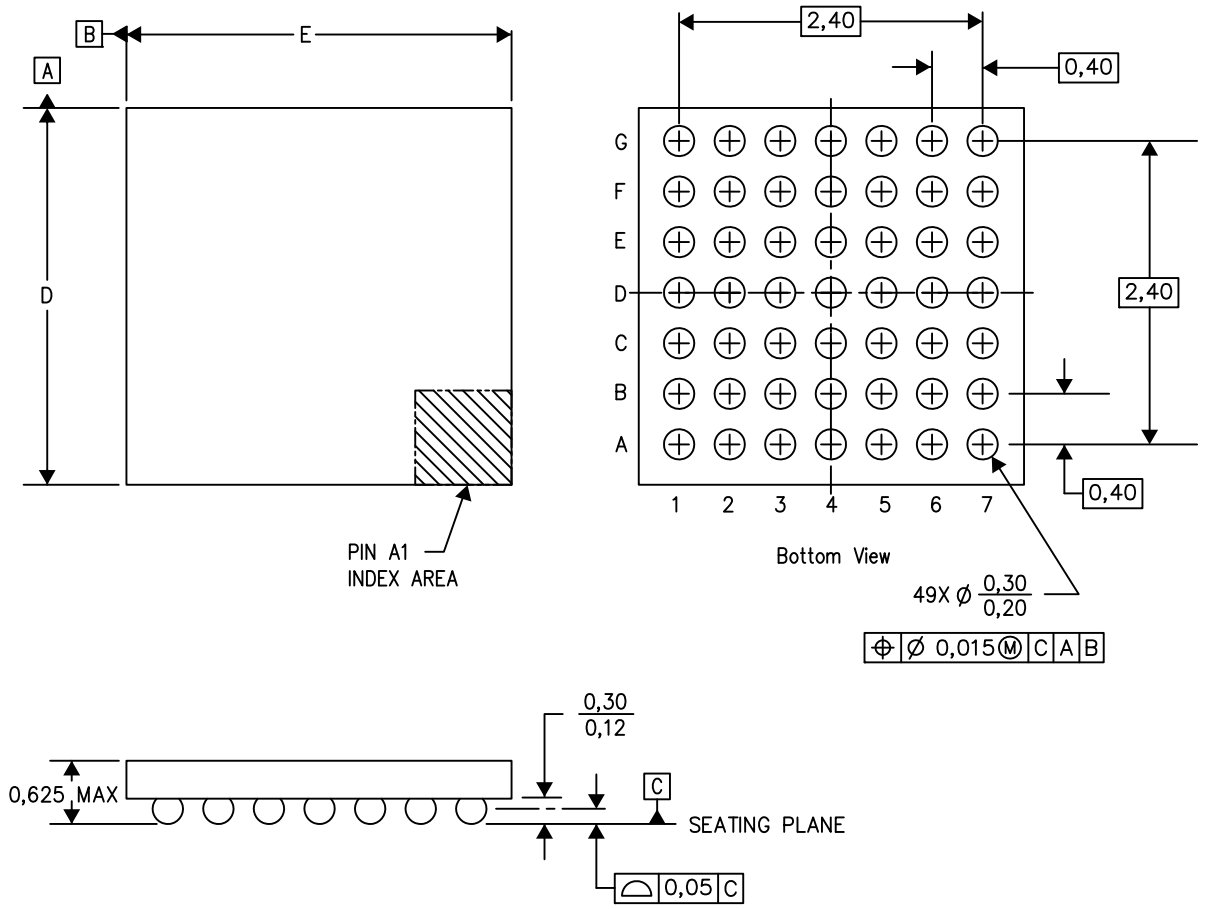
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



4207625–16/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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