bq2408x-Q1 1A 单芯片锂离子和锂聚合物汽车充电器

1 特性

- 集成了功率场效应晶体管 (FET) 和电流传感器，适用于采用交流适配器的 1A 充电应用
- 采用安全定时器实现预充电调节
- 充电和电源正常状态输出
- 自动休眠模式，可降低功耗
- 集成了充电电流监视器
- 固定 7 小时快速充电安全定时器
- 非常适合面向空间受限型便携式应用中单节锂离子电池或锂聚合物电池组的低压降充电器设计
- 小型 3mm x 3mm 小外形尺寸无引线 (SON) 封装

2 应用

- 汽车用线性充电器
- 紧急呼叫/备用呼叫电池
- 车用信息娱乐系统
- 汽车遥控钥匙

3 说明

bq24080-Q1 和 bq24081-Q1 是高度集成且灵活的锂离子线性充电器件，面向空间受限型充电器应用。 它们在单片器件中集成了功率 FET 和电流传感器、高精度电流和电压调节、充电状态以及充电终止功能。 可通过一个外部电阻设置充电电流幅值。

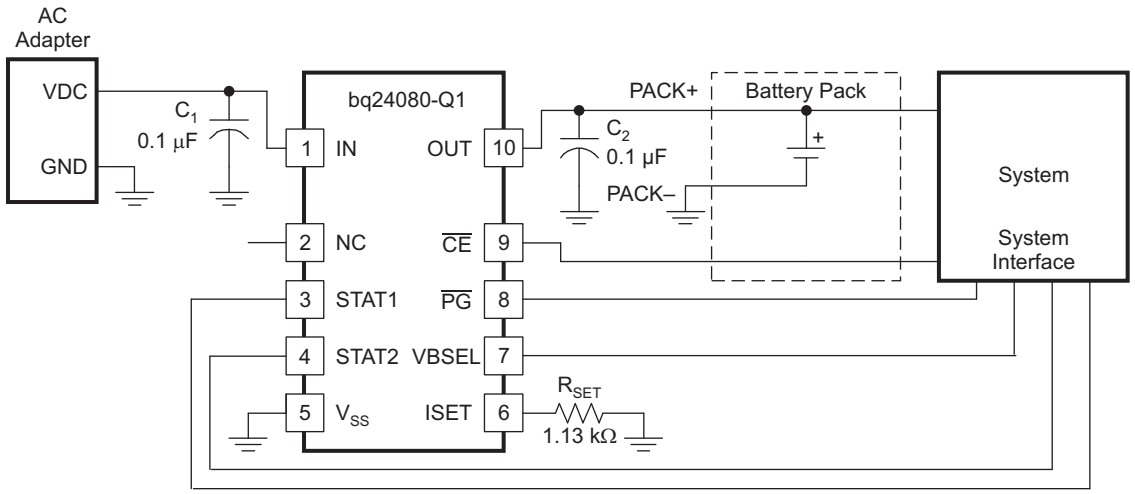
器件分三个阶段对电池进行充电：调节、恒流和恒压。当达到最低电流时，将终止充电。 内置的充电定时器针对充电终止提供了备用的安全性机制。 如果电池电压低于内部阈值，器件将自动重新启动充电。 移除交流适配器后，器件将自动进入休眠模式。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq24080-Q1(2)	VSON (10)	3.00mm x 3.00mm
bq24081-Q1		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。
(2) 产品预览

4 简化电路原理图



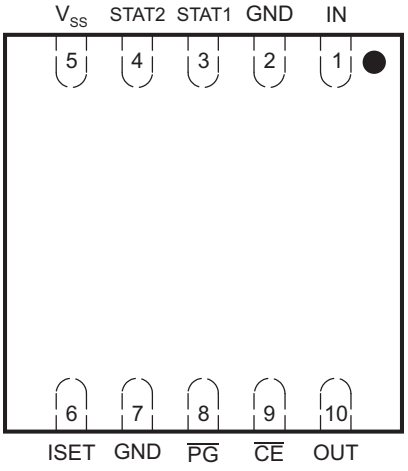
目录

5 修订历史记录

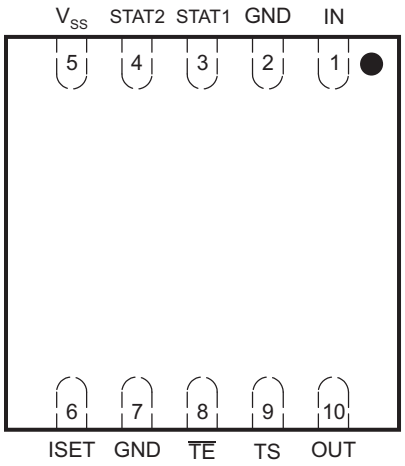
日期	修订版本	注释
2015 年 5 月	*	最初发布。

6 Pin Configuration and Functions

bq24080-Q1 DRC Package
10 Pin VSON
Top View



bq24081-Q1 DRC Package
10 Pin VSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	bq24080-Q1	bq24081-Q1		
$\overline{CE}$	9	–	I	Charge enable input (active-low)
GND	2, 7	2, 7	–	Ground
IN	1	1	I	Adapter dc voltage. Connect minimum 0.1-µF capacitor to V_{SS}.
ISET	6	6	I	Charge current. External resistor to V_{SS} sets precharge and fast-charge current, and also the termination current value. Can be used to monitor the charge current.
OUT	10	10	O	Charge current output. Connect minimum 0.1-µF capacitor to V_{SS}.
$\overline{PG}$	8	–	O	Power-good status output (open-drain)
STAT1	3	3	O	Charge status outputs (open-drain)
STAT2	4	4	O	
$\overline{TE}$	–	8	I	Timer-enable input (active-low)
TS	–	9	I/O	Temperature sense; connect to NTC in battery pack.
V_{SS}	5	5	–	Ground
Thermal pad	–	–	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The exposed thermal pad must be connected to the same potential as the V_{SS} pin on the printed-circuit board. ***Do not use the thermal pad as the primary ground input for the device***. The V_{SS} pin must be connected to ground at all times.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		bq24080-Q1, bq24081-Q1		UNIT
		MIN	MAX	
Input voltage(2)	IN, $\overline{CE}$, ISET, OUT, $\overline{PG}$, STAT1, STAT2, $\overline{TE}$, TS	–0.3	7	V
Output sink/source current	STAT1, STAT2, $\overline{PG}$		15	mA
Output current	OUT		1.5	A
Operating free-air temperature range, T_A		–40	125	°C
Junction temperature range, T_J				°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{SS}.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	6.5	V
T_J	Operating junction temperature range	0	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq24080-Q1, bq24081-Q1	UNIT
		DRC	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5034	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
$I_{CC(VCC)}$	V_{CC} current	$V_{CC} > V_{CC(min)}$		1.2	2	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT pin, $V_{CC} < V_{(SLP)}$		2	5	µA
$I_{CC(STBY)}$	Standby current	$\overline{CE}$ = High, 0°C ≤ T_J ≤ 85°C			150	
$I_{IB(OUT)}$	Input current on OUT pin	Charge DONE, $V_{CC} > V_{CC(MIN)}$		1	5	
VOLTAGE REGULATION $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$, $I_{(TERM)} < I_{O(OUT)} \le 1$ A						
$V_{O(REG)}$	Output voltage			4.2		V
	Voltage regulation accuracy	T_A = 25°C	−0.35%		0.35%	
			−1%		1%	
$V_{(DO)}$	Dropout voltage ($V_{(IN)} - V_{(OUT)}$)	$V_{O(OUT)} = V_{O(REG)}$, $I_{O(OUT)}$ = 1 A $V_{O(REG)} + V_{(DO)}) \le V_{CC}$		350	500	mV
CURRENT REGULATION						
$I_{O(OUT)}$	Output current range(1)	$V_{I(OUT)} > V_{(LOWV)}$, $V_{I(IN)} - V_{I(OUT)} > V_{(DO)}$, $V_{CC} \ge 4.5$ V	20		1000	mA
$V_{(SET)}$	Output current set voltage	Voltage on ISET pin, $V_{CC} \ge 4.5$ V, $V_I \ge 4.5$ V, $V_{I(OUT)} > V_{(LOWV)}$, $V_I - V_{I(OUT)} > V_{(DO)}$	2.463	2.5	2.538	V
$K_{(SET)}$	Output current set factor	50 mA ≤ $I_{O(OUT)}$ ≤ 1 A	307	322	337	
		10 mA ≤ $I_{O(OUT)}$ < 50 mA	296	320	346	
		1 mA ≤ $I_{O(OUT)}$ < 10 mA	246	320	416	
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	Voltage on OUT pin	2.8	3	3.2	V
$I_{O(PRECHG)}$	Precharge range(2)	0 V < $V_{I(OUT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	2		100	mA
$V_{(PRECHG)}$	Precharge set voltage	Voltage on ISET pin, $V_{O(REG)}$ = 4.2 V, 0 V < $V_{I(OUT)} > V_{(LOWV)}$, t < $t_{(PRECHG)}$	240	255	270	mV
TERMINATION DETECTION						
$I_{(TERM)}$	Charge termination detection range(3)	$V_{I(OUT)} > V_{(RCH)}$, t < $t_{(TRMDET)}$	2		100	mA
$V_{(TERM)}$	Charge termination detection set voltage	Voltage on ISET pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)} > V_{(RCH)}$, t < $t_{(TRMDET)}$	235	250	265	mV
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold		$V_{O(REG)}$ – 0.115	$V_{O(REG)}$ − 0.10	$V_{O(REG)}$ − 0.085	V
STAT1, STAT2, and $\overline{PG}$ OUTPUTS						
V_{OL}	Low-level output saturation voltage	I_O = 5 mA			0.25	V
$\overline{CE}$ and $\overline{TE}$ INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			
I_{IL}	Low-level input current		–1			µA
I_{IH}	High-level input current				1	
TIMERS						
$I_{(FAULT)}$	Timer fault recovery current			200		µA

(1) See Equation 2.
(2) See Equation 1.
(3) See Equation 4.

Electrical Characteristics (continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SLEEP COMPARATOR						
$V_{(SLP)}$	Sleep-mode entry threshold voltage	2.3 V ≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$			V_{CC} ≤ $V_{I(OUT)}$ + 80 mV	V
$V_{(SLPEXIT)}$	Sleep-mode exit threshold voltage		V_{CC} ≥ $V_{I(OUT)}$ + 190			
THERMAL SHUTDOWN THRESHOLDS						
$T_{(SHTDWN)}$	Thermal trip threshold	T_J increasing		165		°C
	Thermal hysteresis			15		
UNDERVOLTAGE LOCKOUT						
$_{UVLO}$	Undervoltage lockout	Decreasing V_{CC}	2.4	2.5	2.6	V
	Hysteresis			27		mV
TEMPERATURE SENSE COMPARATOR (bq24081-Q1)						
$V_{(TS1)}$	High-voltage threshold		2.475	2.5	2.525	V
$V_{(TS2)}$	Low-voltage threshold		0.485	0.5	0.515	
$I_{(TS)}$	TS pin current source		96	102	108	µA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION						
	Deglitch time for fast-charge to precharge transition	$V_{CC(MIN)}$ ≥ 4.5 V, t_{FALL} = 100 ns, 10-mV overdrive, $V_{I(OUT)}$ decreasing below threshold	250	375	500	ms
TERMINATION DETECTION						
t_{TRMDET}	Deglitch time for termination detection	$V_{CC(MIN)}$ ≥ 4.5 V, t_{FALL} = 100 ns charging current decreasing below 10-mV overdrive	250	375	500	ms
BATTERY RECHARGE THRESHOLD						
$t_{(DEGL)}$	Deglitch time for recharge detect	$V_{CC(MIN)}$ ≥ 4.5 V, t_{FALL} = 100 ns decreasing below or increasing above threshold, 10-mV overdrive	250	375	500	ms
TIMERS						
$t_{(PRECHG)}$	Precharge time		1,584	1,800	2,016	s
$t_{(CHG)}$	Charge time		22,176	25,200	28,224	s
SLEEP COMPARATOR						
	Sleep-mode entry deglitch time	$V_{(IN)}$ decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive	250	375	500	ms
TEMPERATURE SENSE COMPARATOR (bq24081-Q1)						
$t_{(DEGL)}$	Deglitch time for temperature fault		250	375	500	ms

7.7 Typical Characteristics

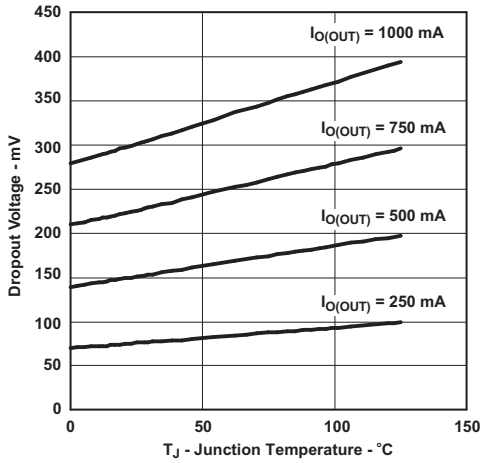


Figure 1. Dropout Voltage vs Junction Temperature

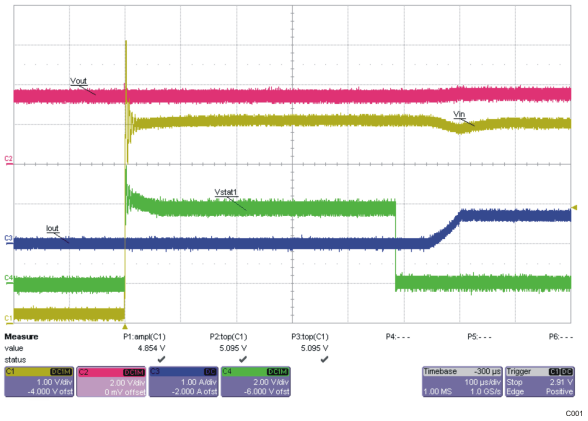


Figure 2. V_{IN} Hot-Plug Power-Up Sequence

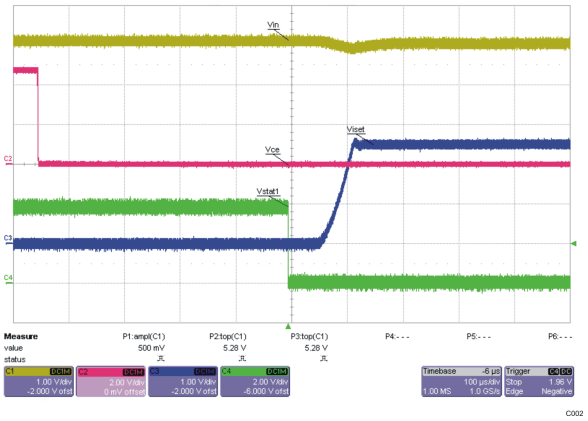


Figure 3. Charge Enable Power-Up Sequence ($\overline{CE}$ = High-to-Low)

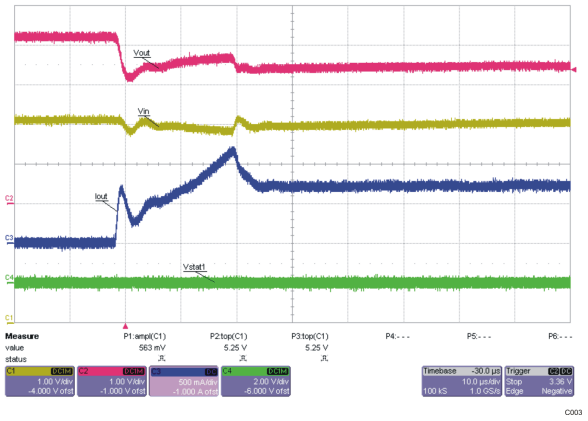
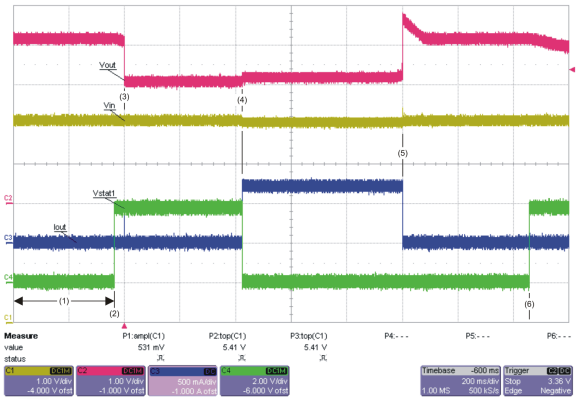


Figure 4. Battery Hot-Plug During Charging Phase



No battery – In termination deglitch prior to STAT1 going high. V_{OUT} (V_{BAT}) cycling between *charge* and *done* prior to screen capture
Stat1 goes high – In *done* state
2-V battery is inserted during the *charge done* state.
Charging is initiated – STAT1 goes low and charge current is applied.
Battery is removed – V_{OUT} goes into regulation, I_{OUT} goes to zero, and termination deglitch timer starts running (same as state 1).
Deglitch timer expires – *charge done* is declared.

Figure 5. Battery Hot-Plug and Removal Power Sequence

8 Detailed Description

8.1 Overview

The device supports a precision Li-Ion, Li-Pol charging system suitable for single cells. Figure 6 shows a typical charge profile, and Figure 7 shows an operational flow chart.

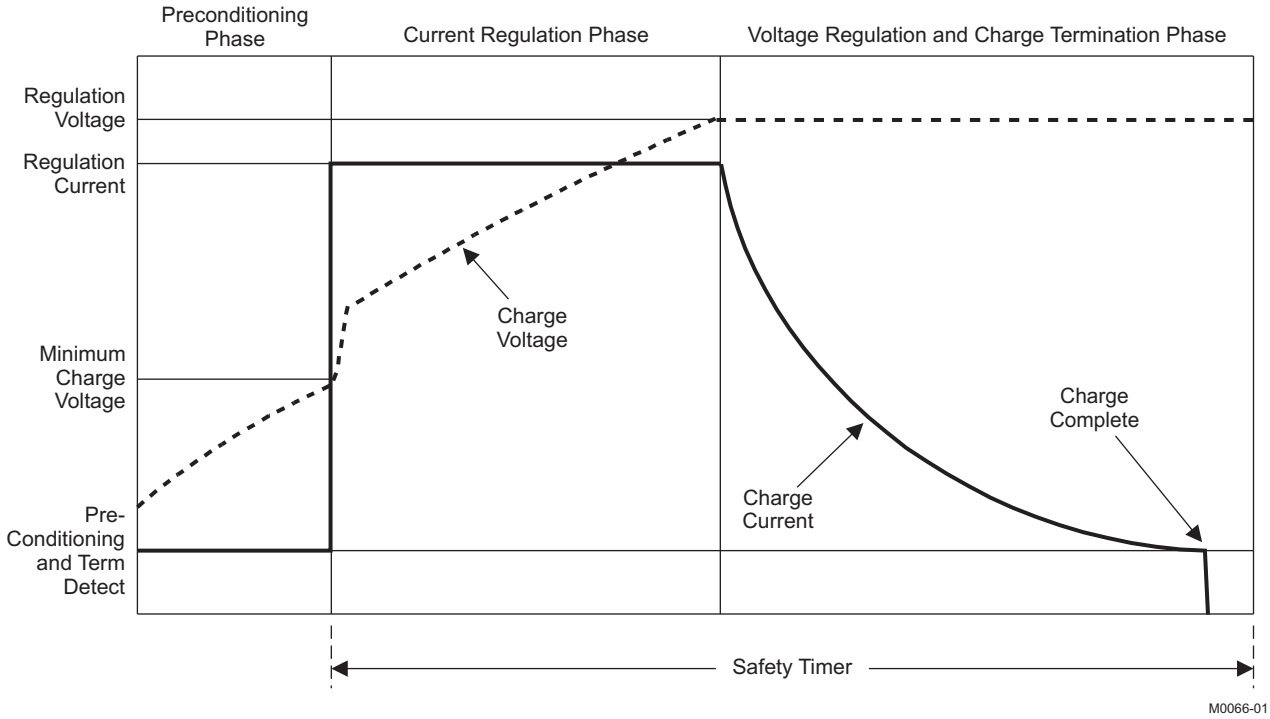


Figure 6. Typical Charging Profile

Overview (continued)

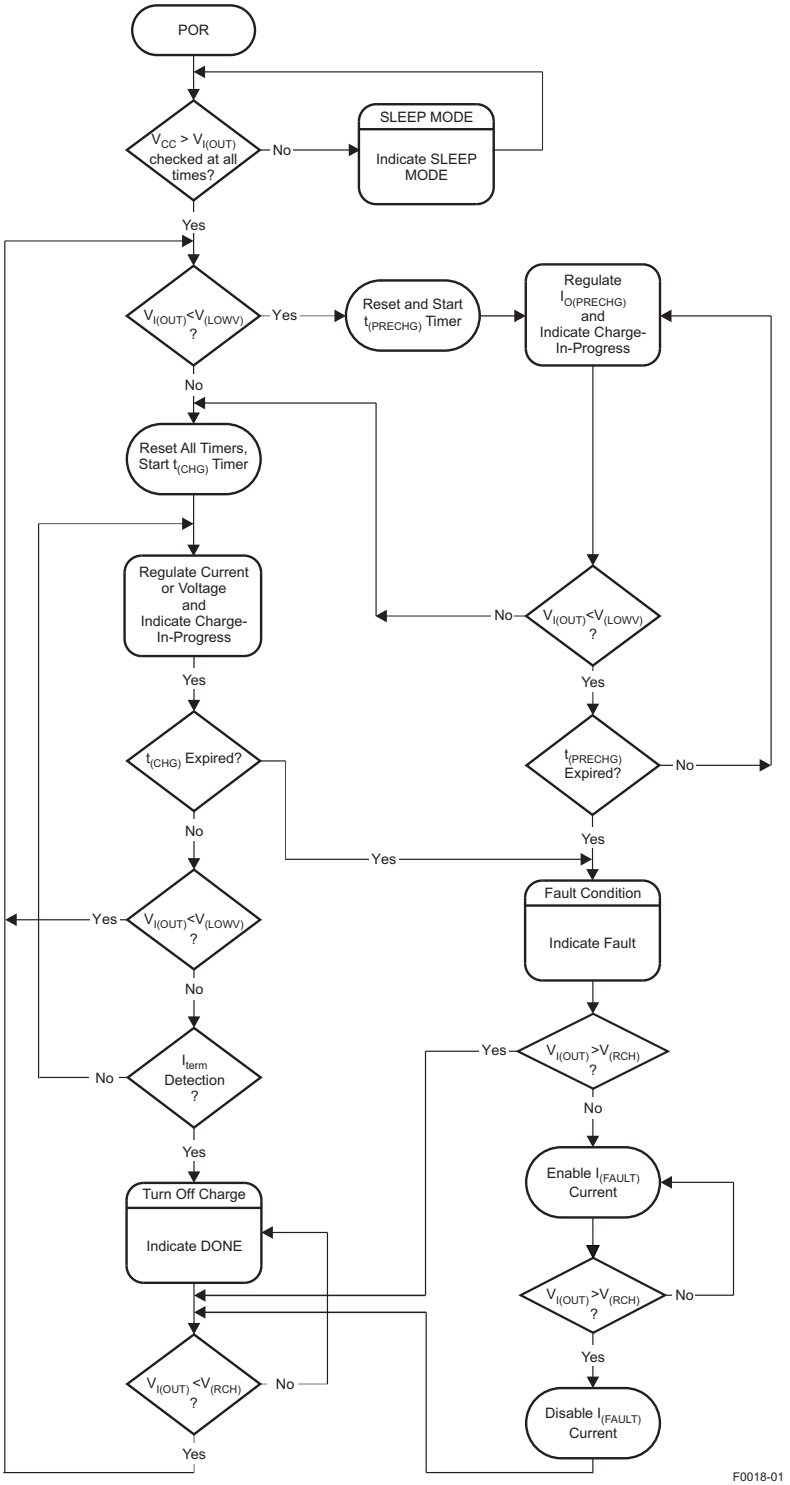
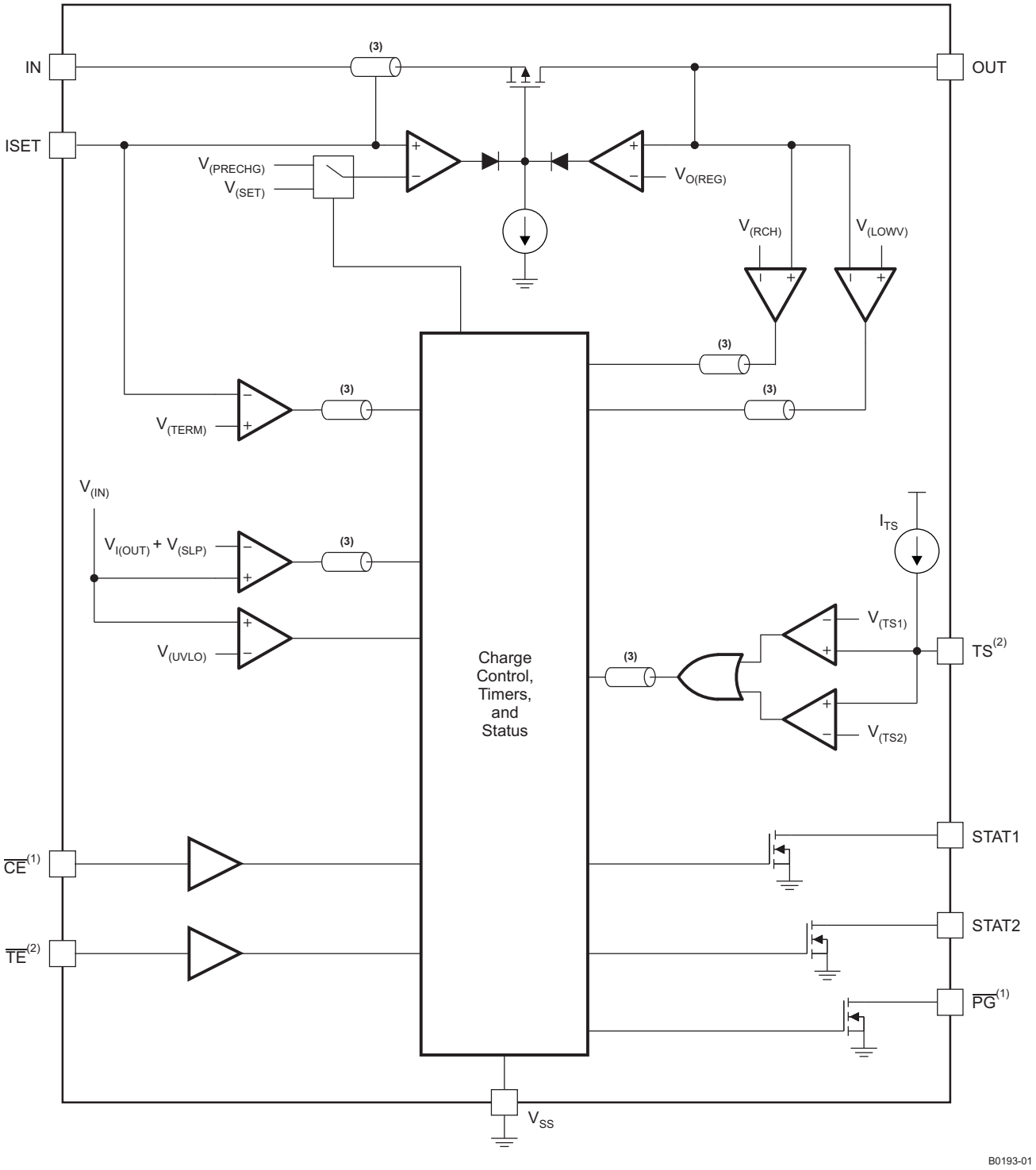


Figure 7. Operational Flow Chart

8.2 Functional Block Diagram



(1) bq24080-Q1 only
(2) bq24081-Q1 only
(3) Signal deglitched

8.3 Feature Description

8.3.1 Battery Preconditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the device applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. Resistor R_{SET}, connected between the ISET and V_{SS}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the *Electrical Characteristics* table.

$$I_{O(PRECHG)} = \frac{K_{(SET)} \times V_{(PRECHG)}}{R_{SET}} \quad (1)$$

The device activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If the $V_{(LOWV)}$ threshold is not reached within the timer period, the device turns off the charger and enunciates FAULT on the STATx pins. See the *Timer Fault and Recovery* section for additional details.

8.3.2 Battery Fast-Charge Constant Current

The device offers on-chip current regulation with programmable set point. Resistor R_{SET}, connected between the ISET and V_{SS}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}} \quad (2)$$

8.3.3 Charge-Current Monitor

When the charge function is enabled internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor R_{ISET} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V_{(ISET)} = I_{(OUT)} \times \frac{R_{(ISET)}}{K_{(ISET)}} \quad (3)$$

8.3.4 Battery Fast-Charge Voltage Regulation

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The device monitors the battery-pack voltage between the OUT and V_{SS} pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the device also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the charger is turned off and FAULT is set on the STATx pins. See the *Timer Fault and Recovery* section for additional details.

8.3.5 Charge Termination Detection and Recharge

The device monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, charge is terminated. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the *Electrical Characteristics* table.

$$I_{O(TERM)} = \frac{K_{(SET)} \times V_{(TERM)}}{R_{SET}} \quad (4)$$

After charge termination, the device restarts the charge once the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

The device monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, the charge is terminated immediately.

Resistor R_{SET}, connected between the ISET and V_{SS}, determines the current level at the termination threshold.

Feature Description (continued)

8.3.6 Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 1. These status pins can be used to drive LEDs or communicate to the host processor. Note that *OFF* indicates the open-drain transistor is turned off.

Table 1. Status Pin Summary

CHANGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature)	OFF	OFF
Timer fault		
Sleep mode		

8.3.7 $\overline{PG}$ Output (bq24080-Q1)

The open-drain power-good ($\overline{PG}$) output pulls low when a valid input voltage is present. This output is turned off (high-impedance) in sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor.

8.3.8 Charge-Enabled ($\overline{CE}$) Input (bq24080-Q1)

The $\overline{CE}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions.

8.3.9 Timer Enabled ($\overline{TE}$) Input (bq24081-Q1)

The $\overline{TE}$ digital input is used to disable or enable the fast-charge timer. A low-level signal on this pin enables the fast-charge timer, and a high-level signal disables this feature.

8.3.10 Temperature Qualification (bq24081-Q1)

The bq24081-Q1 continuously monitors battery temperature by measuring the voltage between the TS and V_{SS} pins. An internal current source provides the bias for common 10-kΩ negative-temperature-coefficient thermistors (NTC) (see the functional block diagram). The device compares the voltage on the TS pin with the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed. If a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected, the device immediately suspends the charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns within the normal range.

The allowed temperature range with a 103AT-type thermistor is 0°C to 45°C. However, the user may modify these thresholds by adding external resistors (see Figure 8 and Figure 9).

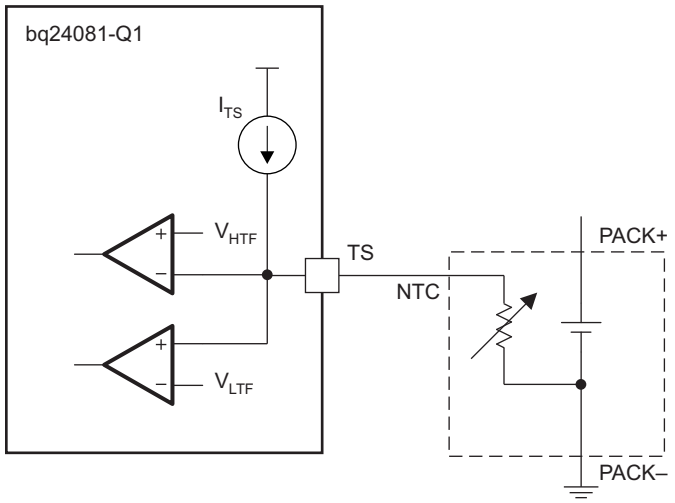


Figure 8. Default Temperature Thresholds

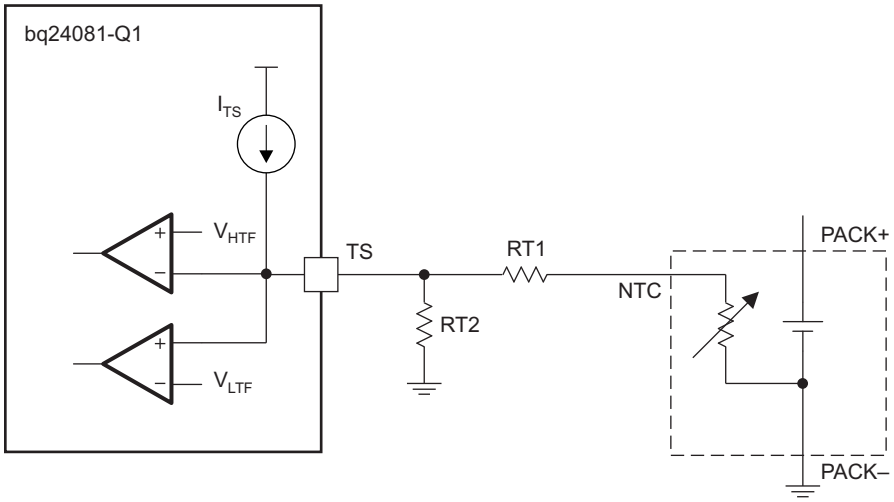


Figure 9. Temperature Thresholds Modified by External Resistors

8.3.11 Timer Fault and Recovery

As shown in Figure 7, the device provides a recovery method to deal with timer fault conditions. The following summarizes this method:

8.3.11.1 Condition Number 1

OUT pin voltage is above the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs.

Recovery method: the device waits for the OUT pin voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the OUT pin voltage falls below the recharge threshold, the device clears the fault and starts a new charge cycle. A POR, $\overline{TE}$, or $\overline{CE}$ toggle also clears the fault.

8.3.11.2 Condition Number 2

OUT pin voltage is below the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: Under this scenario, the device applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the OUT pin voltage goes above the recharge threshold, then the device disables the $I_{(FAULT)}$ current and executes the recovery method described for condition number 1. Once the OUT pin voltage falls below the recharge threshold, the bq24080-Q1 clears the fault and starts a new charge cycle. A POR, $\overline{TE}$, or $\overline{CE}$ toggle also clears the fault.

8.4 Device Functional Modes

8.4.1 Sleep Mode

The device enters the low-power sleep mode if the input power (IN) is removed from the circuit. This feature prevents draining the battery during the absence of input supply.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2408X-Q1 device is Lithium chemistry (Lithium Ion and Lithium Polymer) charger that is intended for automotive applications. The allows the designer to pick an automotive qualified charger for applications where the Li chemistry is needed. Such applications may involve E-Call (back up safety call) or infotainment systems within the automotive space. The device comes completely ready with an integrated charge current monitor and safety timers. The LDO based charger design allows for a cost optimized safe charging algorithm.

9.2 Typical Application

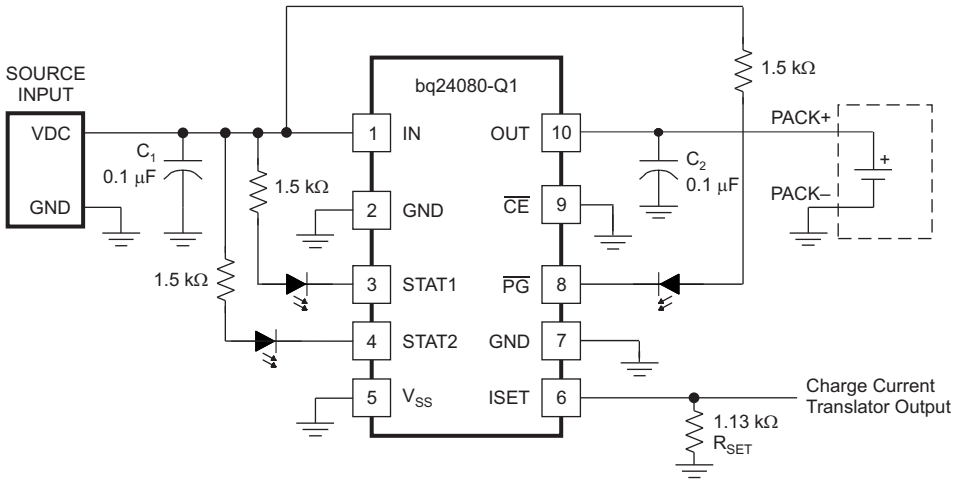


Figure 10. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Supply voltage	5 V
Fast-charge current	≈ 750 mA
Battery-Temperature sense (bq24081-Q1)	–2°C to 44.5°C (default setting)

9.2.2 Detailed Design Procedure

9.2.2.1 Calculations

Program the charge current for 750 mA:

$$R_{ISET} = [V_{(SET)} \times K_{(SET)} / I_{(OUT)}] \quad (5)$$

From *Electrical Characteristics* table, $V_{(SET)}$ = 2.5 V.

From *Electrical Characteristics* table, $K_{(SET)}$ = 322.

$$R_{ISET} = [2.5\ V \times 322 / 0.75\ A] = 1.073\ k\Omega \quad (6)$$

Selecting the closest standard value, use a 1.07-kΩ resistor connected between ISET (pin 6) and ground.

9.2.2.2 Battery Temperature Sense (bq24081-Q1):

Use a Semitec 103AT-4 NTC thermistor connected between TS (pin 9) and ground.

$$R_{THERM\text{-}cold} = [V_{(TS1)} / I_{(TS)}] = 2.5V / 100\ \mu A = 25\ k\Omega \quad (7)$$

$$R_{THERM\text{-}hot} = [V_{(TS2)} / I_{(TS)}] = 0.5V / 100\ \mu A = 5\ k\Omega \quad (8)$$

Look up the corresponding temperature value in the manufacturer's resistance-temperature table for the thermistor selected. For a 103AT-4 Semitec thermistor:

5 kΩ = 44.5°C

25 kΩ = 2°C

9.2.2.3 STAT Pins (All Devices) and PG Pin (bq24080-Q1):

Status pins Monitored by Processor:

Select a pullup resistor that can source more than the input bias (leakage) current of both the processor and status pins and still provide a logic high.

$$R_{PULLUP} \le [V_{(cc\text{-}pullup)} - V_{(logic\ hi\text{-}min)} / (I_{(\mu P\text{-}monitor)} + I_{(STAT\text{-}OpenDrain)})] = (3.3\ V - 1.9\ V) / (1\ \mu A + 1\ \mu A) \le 700\ k\Omega; \quad (9)$$

Connect a 100-kΩ pullup between each status pin and the V_{CC} of the processor. Connect each status pin to a µP monitor pin.

Status viewed by LED:

Select an LED with a current rating less than 10 mA and select a resistor to place in series with the LED to limit the current to the desired current value (brightness).

$$R_{LED} = [(V_{(IN)} - V_{(LED\text{-}on)}) / I_{(LED)}] = (5\ V - 2\ V) / 1.5\ mA = 2\ k\Omega. \quad (10)$$

Place an LED and resistor in series between the input and each status pin.

9.2.2.4 Selecting Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. A 0.1-µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works well. In some applications, it may be necessary to protect against a hot plug input voltage overshoot. This is done in three ways:

1. The best way is to add an input zener, 6.2 V, between the IN pin and V_{SS}.
2. A low-power zener is adequate for the single event transient. Increasing the input capacitance lowers the characteristic impedance which makes the input resistance move effective at damping the overshoot, but risks damaging the input contacts by the high inrush current.
3. Placing a resistor in series with the input dampens the overshoot, but causes excess power dissipation.

The device only requires a small capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the OUT and GND pad is typically sufficient.

9.2.3 Application Curves

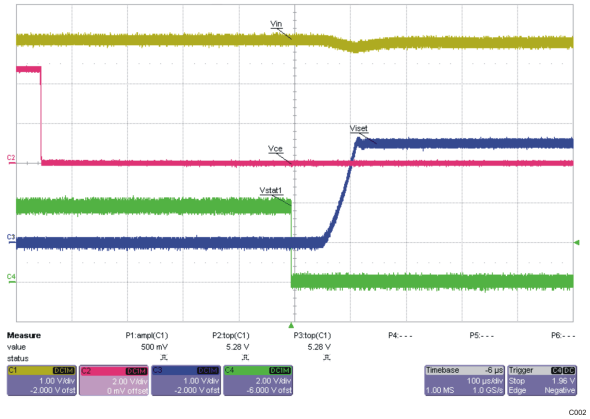
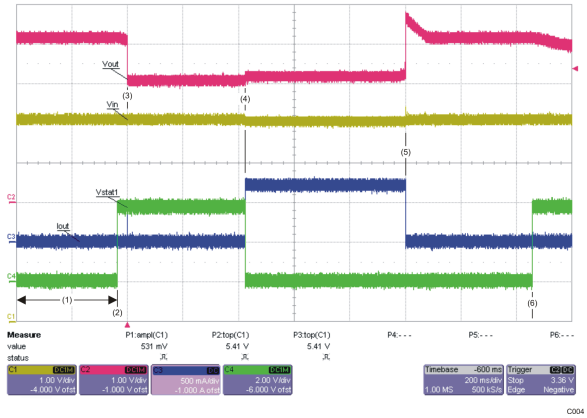


Figure 11. Charge Enable Power-Up Sequence ($\overline{CE}$ = High-to-Low)



No battery – In termination deglitch prior to STAT1 going high. V_{OUT} (V_{BAT}) cycling between *charge* and *done* prior to screen capture

Stat1 goes high – In *done* state

2-V battery is inserted during the *charge done* state.

Charging is initiated – STAT1 goes low and charge current is applied.

Battery is removed – V_{OUT} goes into regulation, I_{OUT} goes to zero, and termination deglitch timer starts running (same as state 1).

Deglitch timer expires – *charge done* is declared.

Figure 12. Battery Hot-Plug and Removal Power Sequence

10 Power Supply Recommendations

The devices are intended to operate withing the ranges shown in Recommended Operating Conditions. Because the input of the device on pin IN is subject to a power source that is external, care muse be taken to not exercise the pin above the Absolute Maximum Rating of the Pin shown in the *Absolute Maximum Ratings* table.

11 Layout

11.1 Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to $V_{(IN)}$ and the output filter capacitors from OUT to V_{SS} should be placed as close as possible to the device, with short trace runs to both signal and V_{SS} pins. The V_{SS} pin should have short trace runs to the GND pin.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small-signal ground path and the power ground path.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The device is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number SLUA271).

11.2 Layout Example

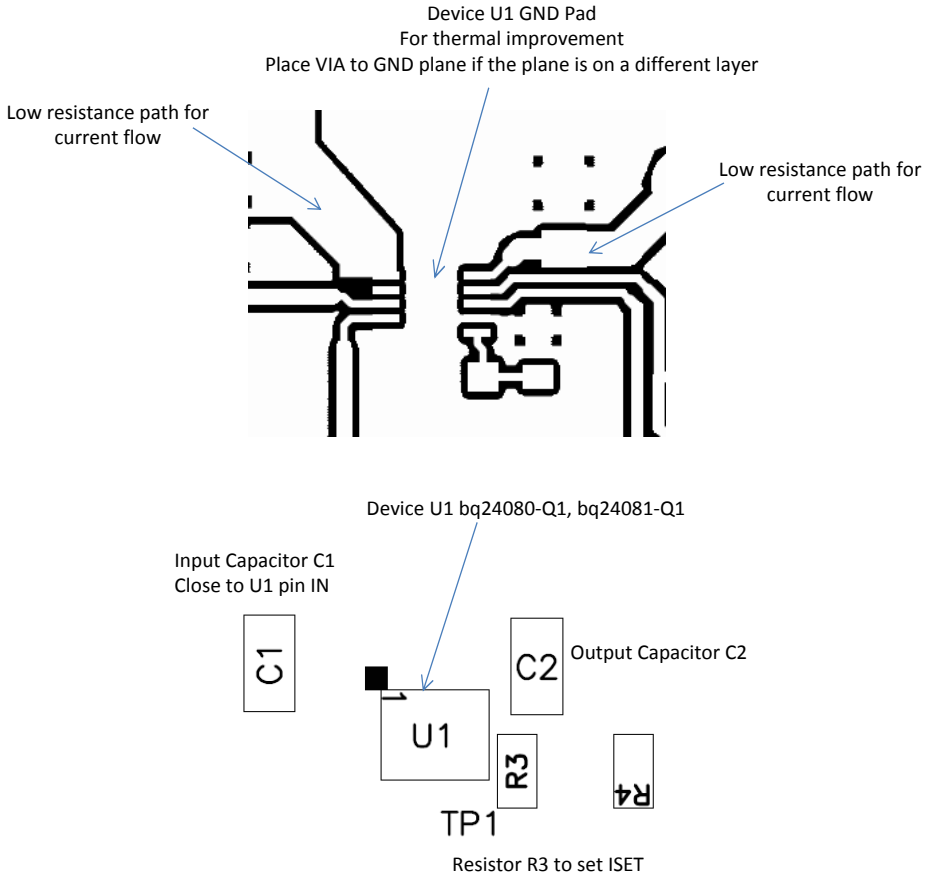


Figure 13. Board Layout

11.3 Thermal Considerations

The bq24080-Q1 and bq24081-Q1 are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed-circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number SLUA271).

The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for $R_{\theta JA}$ is:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \tag{11}$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of $R_{\theta JA}$ include:

- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested
- Use multiple 10–13 mil vias in the PowerPAD™ to copper ground plane.
- Avoid cutting the ground plane with a signal trace near the power IC.
- The PCB must be sized to have adequate surface area for heat dissipation.
- FR4 (figerglass) thickness should be minimized.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal Power FET. It can be calculated from the following equation:

$$P = (V_{(IN)} - V_{(OUT)}) \times I_{O(OUT)} \tag{12}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 6.

12 器件和文档支持

12.1 器件支持

12.2 文档支持

《*QFN/SON PCB 连接*》（文献编号：SLUA271）。

12.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **3.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
bq24080-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24081-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24081QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ZACQ	Samples
BQ24081QDRCTQ1	PREVIEW	VSON	DRC	10	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

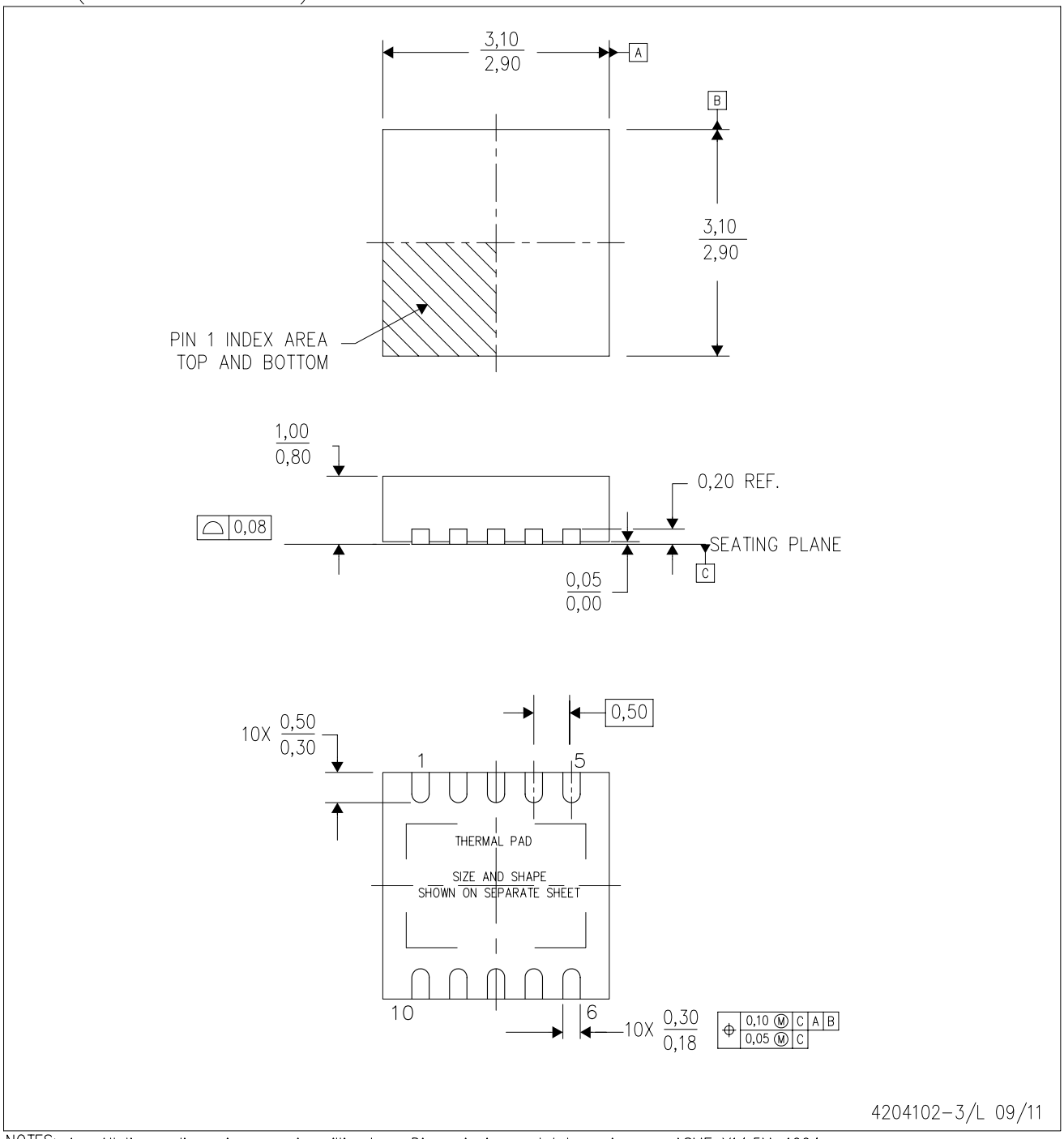
OTHER QUALIFIED VERSIONS OF BQ24081-Q1 :

- Catalog: BQ24081

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

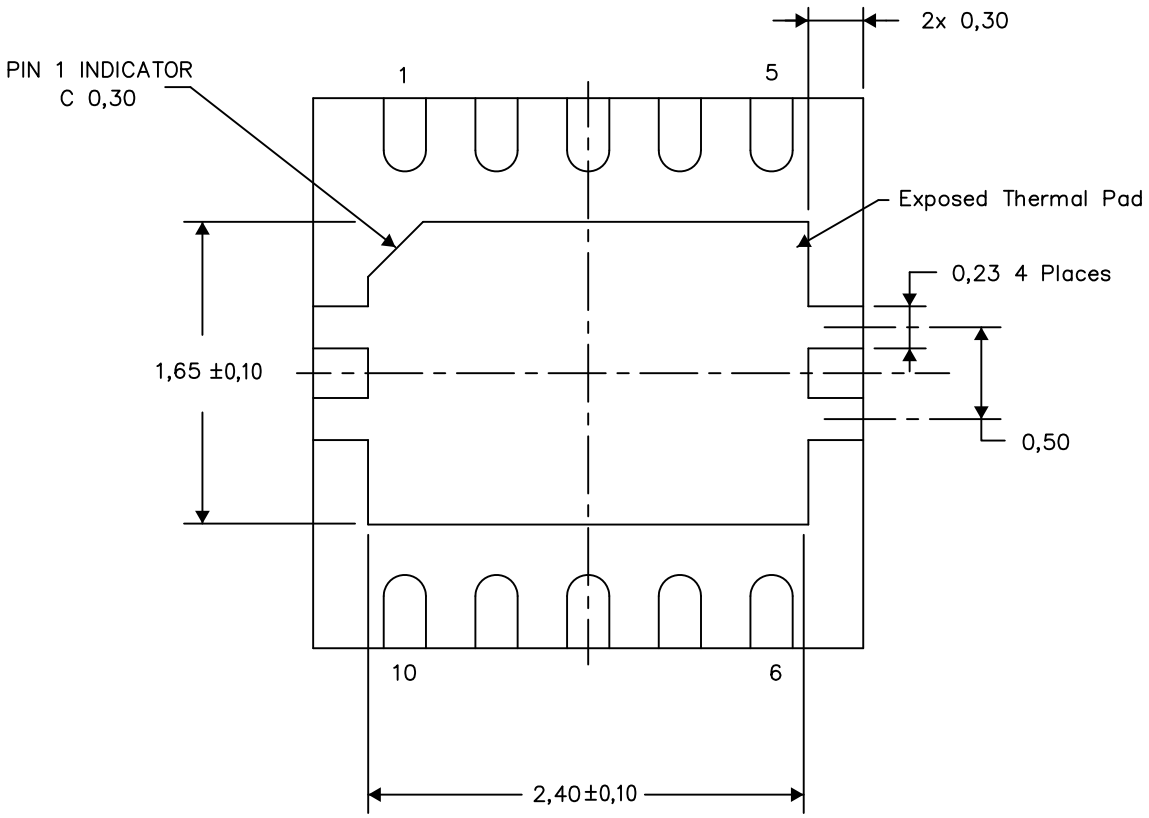
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



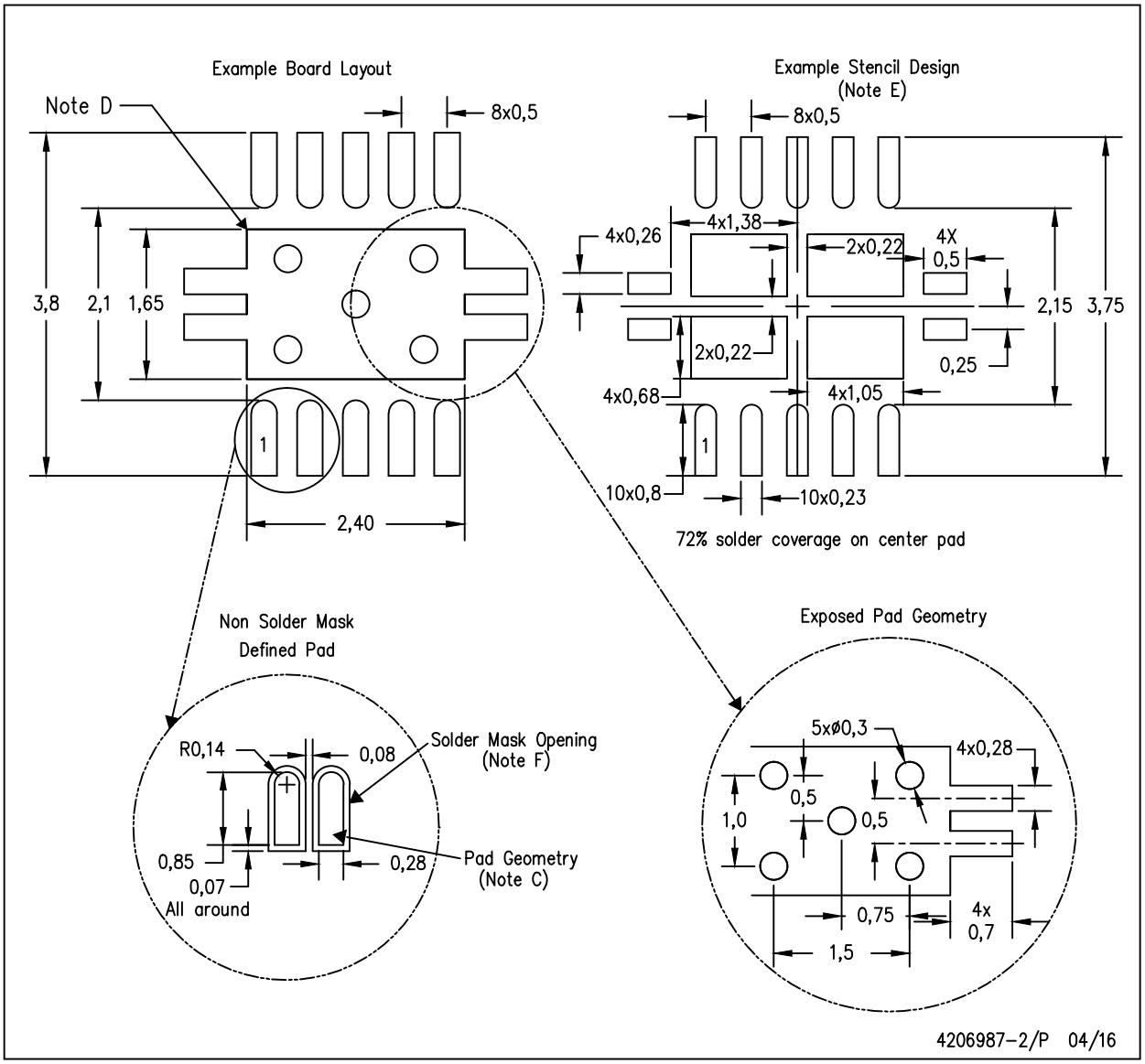
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265