支持电池管理和针对能量采集器应用中主电池的自主电源复用器的超低功耗升压充电器

查询样片: bq25505

特性

- 超低功耗， 具有高效直流/直流升压充电器
  - 冷启动电压：V_{IN} ≥ 330mV
  - 能够在 VIN 低至 100mV 时持续能量采集
  - 325nA 的超低静态电流
  - 输入电压稳压防止高阻抗输入源故障
  - 电池电流 < 5nA 的运输节电模式
- 储能
  - 可将能量存储在可再充电锂离子电池、薄膜电池、超大电容器或传统电容器中
- 电池充电和保护
  - 内部设定欠压电平
  - 用户可编程过压电平
- 电池正常输出标志
  - 可编程阀值和滞后
  - 功率损耗待定的随附报警功能的微控制器
  - 可被用来启用/禁用系统负载
- 可编程最大功率点跟踪 (MPPT)
  - 实现从多种能量采集器中最优能量提取的集成 MPPT
- 针对主（非可再充电）和副（可再充电）储能元件复用的栅极驱动器
  - 基于 VBAT_OK 的自主开关
  - 先开后合防止系统电源轨减弱

应用范围

- 能量采集
- 太阳能充电器
- 热电发电机 (TEG) 能量采集
- 无线传感器网络 (WSN)
- 工业监控
- 环境监测
- 桥梁和结构健康监测 (SHM)
- 智能楼宇控制
- 便携式和可佩戴式健康器件
- 娱乐系统遥控

说明

bq25505 是全新智能化集成能量采集超低功耗管理解决方案新系列中的第一个，这些解决方案十分适合满足超低功耗应用的特殊需求。 本产品专门设计用于高效获取和管理从诸如光伏（太阳能）或热电发生器 (TEG) 等多种不同直流源产生的微瓦 (μW) 至毫瓦 (mW) 级的电能。 bq25505 是一款高效升压充电器，此充电器针对诸如具有严格的电源和工作要求的无线传感器网络 (WSN) 等产品和系统。 bq25505 的设计始于只需要微瓦电力即可开始工作的直流到直流升压转换器/充电器。

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明（继续）

一旦启动，升压充电器能够有效地从诸如 TEG 或单节或双节太阳能电池板的低压输出采集器中提取能量。 升压充电器能够在 VIN 低至 330mV 时启动，并且一旦启动，能够在 V_{IN} 低至 100mV 时继续采集能量。

bq25505 执行一个可编程最大功率点跟踪 (MPPT) 采样网络来优化进入器件的功率传输。 VIN_DC 开环路电压的采样由外部电阻器设定，并且采样电压由一个外部电容器保存。 例如，太阳能电池运行在它们开环路电压最大功率点 (MPP) 的 80%，电阻分压器可被设定为 VIN_DC 电压的 80%，并且此网络将控制 VIN_DC 在采样的基准电压附近运行。 或者，可通过一个微控制器 (MCU) 来提供一个外部基准电压来产生一个更加复杂的 MPPT 算法。

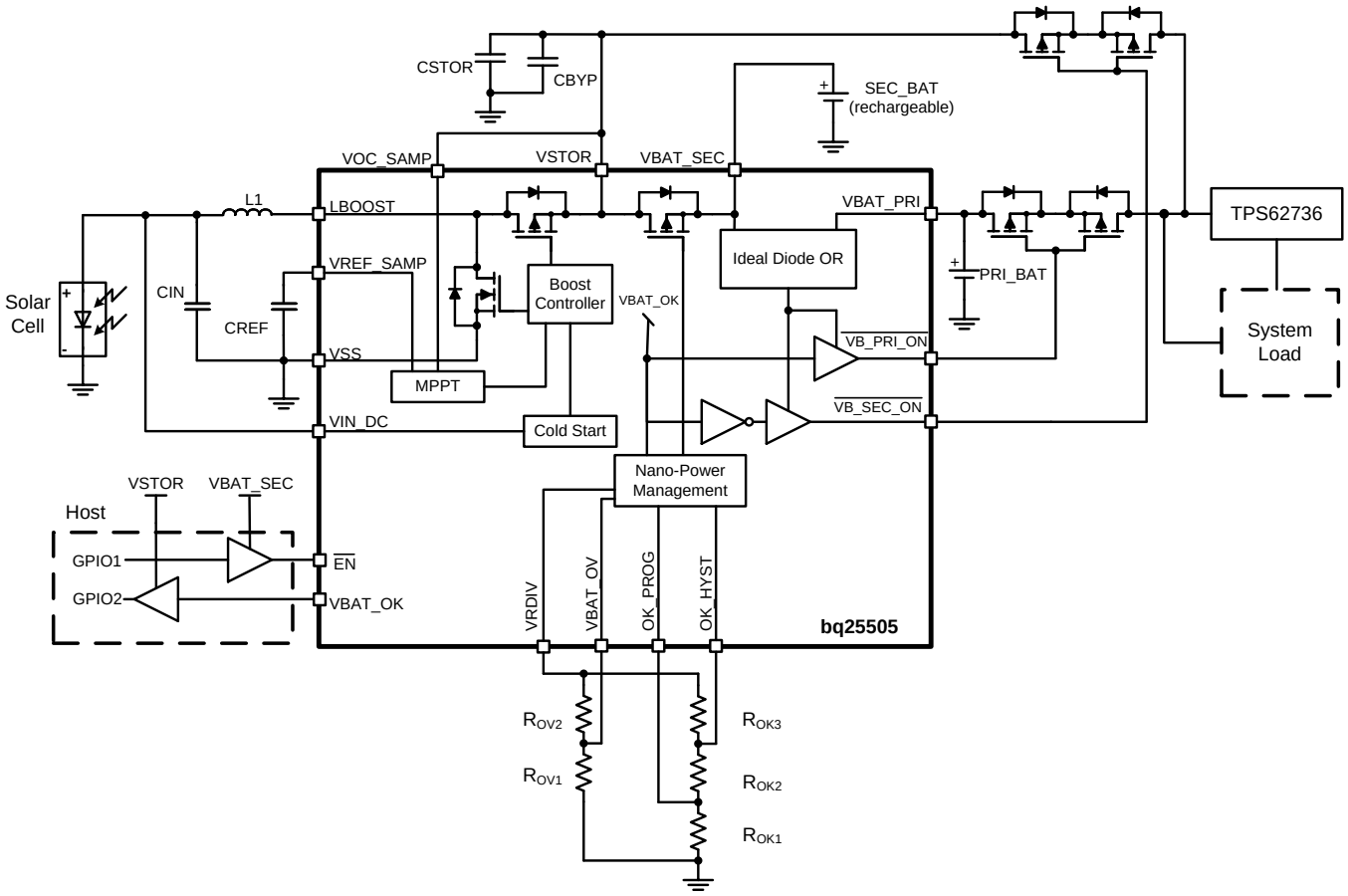
bq25505 的设计具有灵活性以支持多种储能元件。 能量采集器提取能量的能量源往往是不固定的，或者随时间变化的。 通常情况下，系统将需要某些类型的储能元件，例如一个可再充电电池、超大电容器或传统电容器。 储能元件将在系统需要时使特定的恒定功率可用。 储能元件也使得系统能够处理任何无法直接来自输入源的峰值电流。为了防止对储能元件造成损害，参照内部设定欠压 (UV) 和用户可编程过压 (OV) 电平来监视最大和最小电压。

为了帮助用户进一步严格管理他们的能耗预算，当储能电池或电容器上的电压已经下降到低于一个预先设定的临界电平以下时，bq25505 切换电池正常标志来向一个连接的微控制器发出一个信号。 这样应该使负载电流减少，以防止系统进入一个欠压状态。 OV 和电池正常阀值被单独设定。

除了升压充电前端，bq25505 为系统提供一个自主电源复用器栅极驱动。 为了将一个单电源轨提供给系统负载，此栅极驱动器能够实现两个储能元件自主复用。 这个复用器基于 VBAT_OK 阀值，用户可通过电阻器来设定此阀值。 这使得用户能够在系统由能量采集器储能元件供电时设定电平，例如，由可再充电电池或超大电容器或一个主要非可再充电电池（例如，两节 AA 电池）供电时。 这个混合系统架构类型可根据采集器上可用能量来延长一个典型电池供电类系统的运行时间。 如果由于延长的“黑暗时间”而导致没有足够的能量来运行系统，主电池在 8μs 内被自主切换到主系统电源轨以提供不间断运行。

bq25505 的全部功能被封装在一个小尺寸 20 引线 3.5mm x 3.5mm 四方扁平无引线 (QFN) 封装.

典型应用原理图



For Ordering Information, see the Package Option Addendum at the end of the data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, $\overline{\text{VB\_PRI\_ON}}$, $\overline{\text{VB\_SEC\_ON}}$, VBAT_PRI, VBAT_SEC, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VSTOR, LBST(2)	–0.3	5.5	V
Peak Input Power, PIN_PK			510	mW
Operating junction temperature range, T_J		–40	125	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}/ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		bq25505	UNITS
		RGR (20 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	34.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49.0	
θ_{JB}	Junction-to-board thermal resistance	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VIN(DC)	DC input voltage into VIN_DC(1)	0.1		5.1	V
VBAT_SEC, VBAT_PRI	Battery voltage range(2)	2		5.5	V
CIN	Input capacitance	4.7			µF
CSTOR	Storage capacitance	4.7			µF
CBAT	Battery pin capacitance or equivalent battery capacity	100			µF
CREF	Sampled reference storage capacitance	9	10	11	nF
$R_{OC1} + R_{OC2}$	Total resistance for setting for MPPT reference.	18	20	22	MΩ
$R_{OK\ 1} + R_{OK\ 2} + R_{OK3}$	Total resistance for setting the VBAT_OK threshold voltage.	11	13	15	MΩ
$R_{OV1} + R_{OV2}$	Total resistance for setting VBAT_OV threshold voltage.	11	13	15	MΩ
L1	Input inductance	22			µH
T_A	Operating free air ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

(1) Maximum input power ≤ 400 mW. Cold start has been completed
(2) VBAT_OV setting must be higher than VIN_DC

ELECTRICAL CHARACTERISTICS

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VSTOR = 4.2 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, CSTOR= 4.7 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CHARGER						
VIN(DC)	DC input voltage into VIN_DC	Cold-start completed	100		5100	mV
I-CHG(CBC_LIM)	Cycle-by-cycle current limit of charger	0.5V < V_{IN} < 4.0 V; VSTOR = 4.2 V		230	285	mA
PIN	Input power range for normal charging	VBAT_OV > VSTOR > VSTOR_CHGEN	0.005		510	mW
VIN(CS)	Minimum input voltage for cold start circuit to start charging VSTOR	VBAT_SEC < VBAT_UV; VSTOR = 0 V; 0°C < T_A < 85°C		330	400	mV
VSTOR_CHGEN	Voltage on VSTOR when cold start operation ends and normal charger operation commences		1.6	1.73	1.9	V
PIN(CS)	Minimum cold-start input power for VSTOR to reach $VSTOR_{(CHGEN)}$ and allow normal charging to commence	VSTOR < $VSTOR_{(CHGEN)}$		5		µW
$t_{BAT\_HOT\_PLUG}$	Time for which switch between VSTOR and VBAT_SEC closes when battery is hot plugged into VBAT_SEC	Battery resistance = 300 Ω, Battery voltage = 3.3V		50		ms
QUIESCENT and LEAKAGE CURRENTS						
I_Q	$\overline{EN}$ = GND - Full operating mode	VIN_DC = 0V; VSTOR = 2.1V; T_J = 25°C		325	400	nA
		VIN_DC = 0V; VSTOR = 2.1V; –40°C < T_J < 85°C			700	
	$\overline{EN}$ = VBAT_SEC - Ship mode	VBAT_SEC = VBAT_PRI = 2.1 V; T_J = 25°C; VSTOR = VIN_DC = 0 V		1	5	
		VBAT_SEC = VBAT_PRI = 2.1 V; –40°C < T_J < 85°C; VSTOR = VIN_DC = 0 V			20	
I-BATPRI(LEAK)	$\overline{EN}$ = VBAT_SEC - Ship mode	VBAT_PRI = VBAT_SEC = 2.1 V; T_J = 25°C; VIN_DC = 0 V; VSTOR floating		1	5	nA
		VBAT_PRI = VBAT_SEC = 2.1 V; –40°C < T_J < 85°C; VIN_DC = 0 V; VSTOR floating			20	nA
MOSFET RESISTANCES						
RDS(ON)-BAT	ON resistance of switch between VBAT_SEC and VSTOR	VBAT_SEC = 4.2 V		0.95	1.50	Ω
RDS(ON)_CHG	Charger low side switch ON resistance	VBAT_SEC = 4.2 V		0.70	0.90	Ω
	Charger high side switch ON resistance			2.30	3.00	Ω
	Charger low side switch ON resistance	VBAT_SEC = 2.1 V		0.80	1.00	Ω
	Charger high side switch ON resistance			3.70	4.80	Ω
f_{SW}	Maximum charger switching frequency			1.0		MHz
T_{TEMP_SD}	Junction temperature when charging is discontinued	VBAT_OV > VSTOR > 1.8V		125		C

ELECTRICAL CHARACTERISTICS (continued)

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VSTOR = 4.2 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, CSTOR= 4.7 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY MANAGEMENT						
VBAT_OV	Programmable voltage range for overvoltage threshold	VBAT_SEC increasing	2.2		5.5	V
VBAT_OV_HYST	Battery over-voltage hysteresis (internal)	VBAT_SEC decreasing; VBAT_OV = 5.25V		24	45	mV
VDELTA	VBAT_OV - VIN(DC)	Main boost charger on; MPPT not sampling VOC	400			mV
VBAT_UV	Under-voltage threshold	VBAT_SEC decreasing	1.91	1.95	2	V
VBAT_UV_HYST	Battery under-voltage hysteresis (internal)	VBAT_SEC increasing		15	32	mV
VBAT_OK_HYST	Programmable voltage range of digital signal indicating VSTOR (=VBAT_SEC) is OK	VBAT_SEC increasing	VBAT_UV		VBAT_OV	V
VBAT_OK_PROG	Programmable voltage range of digital signal indicating VSTOR (=VBAT_SEC) is OK	VBAT_SEC decreasing	VBAT_UV		VBAT_OK_HYST – 50	mV
VBAT_ACCURACY	Overall Accuracy for threshold values VBAT_OV, VBAT_OK	Selected resistors are 0.1% tolerance	-2		2	%
VBAT_OK(H)	VBAT_OK (High) threshold voltage	Load = 10 µA			VSTOR – 200	mV
VBAT_OK(L)	VBAT_OK (Low) threshold voltage	Load = 10 µA			100	mV
ENABLE THRESHOLDS						
$\overline{EN}$(H)	Voltage for $\overline{EN}$ high setting. Relative to VBAT_SEC.	VBAT_SEC = 4.2V	VBAT_SEC – 0.2			V
$\overline{EN}$(L)	Voltage for $\overline{EN}$ low setting	VBAT_SEC = 4.2V			0.3	V
BIAS and MPPT CONTROL STAGE						
VOC_SAMPLE	Time period between two MPPT samples			16		s
VOC_STLG	Settling time for MPPT sample measurement of VIN_DC open circuit voltage	Device not switching		256		ms
VIN_REG	Regulation of VIN_DC during charging	0.5 V < VIN < 4 V; IIN(DC) = 10 mA			10%	
MPPT_80	Voltage on VOC_SAMP to set MPPT threshold to 0.80 of open circuit voltage of VIN_DC		VSTOR – 0.015			V
MPPT_50	Voltage on VOC_SAMP to set MPPT threshold to 0.50 of open circuit voltage of VIN_DC				15	mV
VBIAS	Internal reference for the programmable voltage thresholds	VSTOR ≥ VSTOR_CHGEN	1.205	1.21	1.217	V
MULTIPLEXOR						
t_{DEAD}	Dead time between $\overline{VB\_SEC\_ON}$ and $\overline{VB\_PRI\_ON}$			5	8 (1)	us

(1) Specified by design.

DEVICE INFORMATION

RGT PACKAGE
(TOP VIEW)

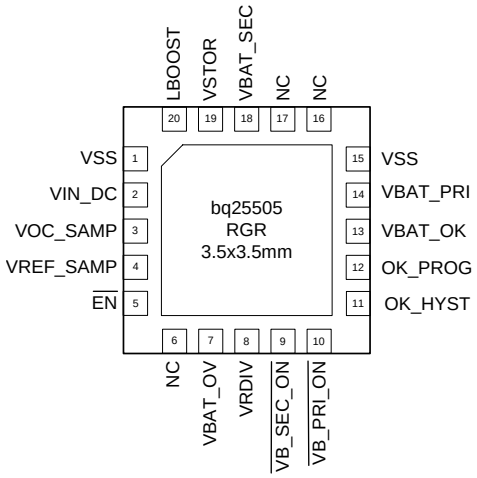


Figure 1. bq25505 3.5mm x 3.5mm QFN-20 Package

PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
1	VSS	Input	General ground connection for the device
2	VIN_DC	Input	DC voltage input from energy harvesters. Connect at least a 4.7 µF capacitor as close as possible between this pin and pin 1.
3	VOC_SAMP	Input	Sampling pin for MPPT network. Connect to VSTOR to sample at 80% of input soure open circuit voltage. Connect to GND for 50% or connect to the mid-point of external resistor divider between VIN_DC and GND.
4	VREF_SAMP	Input	Sample and hold circuit output for the reference set by the MPPT per VOC_SAMP. Connect a 0.01 µF capacitor from this pin to GND.
5	$\overline{\text{EN}}$	Input	Active low digital programming input for enabling/disabling the IC. Connect to GND to enable the IC.
6	NC	Input	Connect to VSS via the IC's PowerPad.
7	VBAT_OV		Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_SEC overvoltage threshold.
8	VRDIV	Output	Connect high side of resistor divider networks to this biasing voltage.
9	$\overline{\text{VB\_SEC\_ON}}$	Output	Active low push-pull driver for the secondary (rechargeable) energy storage PMOS FET.
10	$\overline{\text{VB\_PRI\_ON}}$	Output	Active low push-pull driver for the primary (non-rechargeable) energy storage PMOS FET.
11	OK_HYST	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK hysteresis threshold.
12	OK_PROG	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK threshold.
13	VBAT_OK	Output	Digital output for battery good indicator. Internally referenced to the VSTOR voltage.
14	VBAT_PRI	Input	Primary (non-rechargeable) energy storage element HiZ sense input.
15	VSS	Supply	Signal ground connection for the device.
16	NC	Input	Connect to ground using the IC's PowerPad.
17	NC	Input	Connect to ground using the IC's PowerPad.
18	VBAT_SEC	I/O	Connect a secondary (rechargeable) storage element with at least 100uF of equivalent capacitance to this pin.
19	VSTOR	Output	Connection for the output of the boost charger. Connect at least a 4.7 µF capacitor in parallel with a 0.1 µF capacitor as close as possible to between this pin and pin 1 (VSS).
20	LBOOST	Input	Inductor connection for the boost charger switching node. Connect a 22 µH inductor between this pin and pin 2 (VIN_DC).

TYPICAL APPLICATION CIRCUITS

VBAT_OV = 3.11 V, VBAT_OK = 2.39 V, VBAT_OK_HYST = 2.80 V, MPPT (V_{OC}) = 80%

L1 = 22 µH, CIN = CSTOR = 4.7 µF, CBYP=0.1 µF, CREF = 10 nF

R_{OK1} = 5.62 MΩ, R_{OK2} = 5.49 MΩ, R_{OK3} = 1.87 MΩ, R_{OV1} = 7.5 MΩ, R_{OV2} = 5.36 MΩ

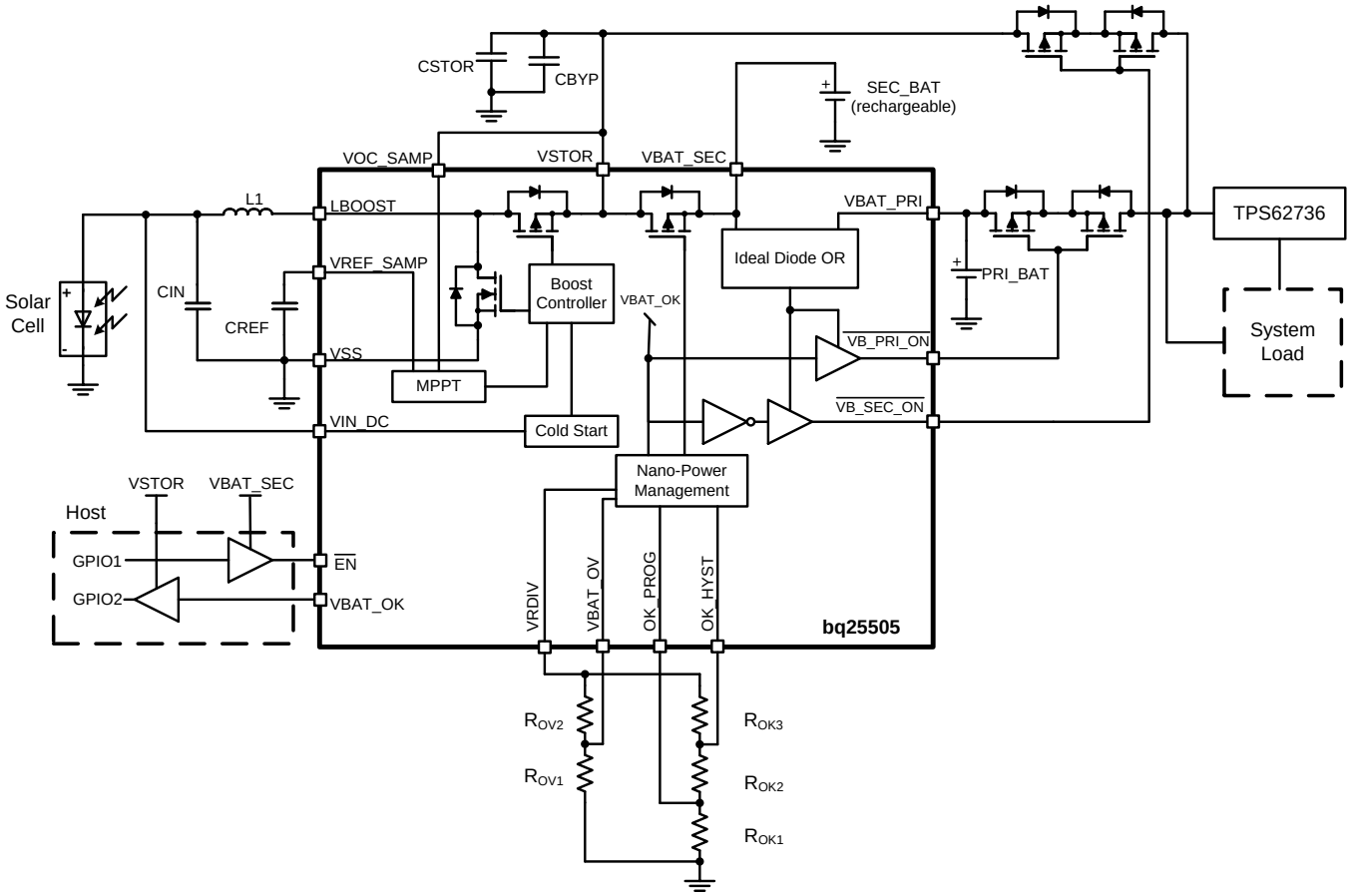


Figure 2. Typical Solar Application Circuit with Primary and Secondary Batteries

VBAT_OV = 4.18V, VBAT_OK = 3.5 V, VBAT_OK_HYST = 3.7 V, MPPT (V_{OC}) = 50%

L1 = 22 µH, CIN = CSTOR = 4.7 µF, CBYP=0.1 µF, CREF = 10 nF

R_{OK1} = 4.22 MΩ, R_{OK2} = 8.06 MΩ, R_{OK3} = 0.698 MΩ, R_{OV1} = 6.04 MΩ, R_{OV2} = 7.87 MΩ

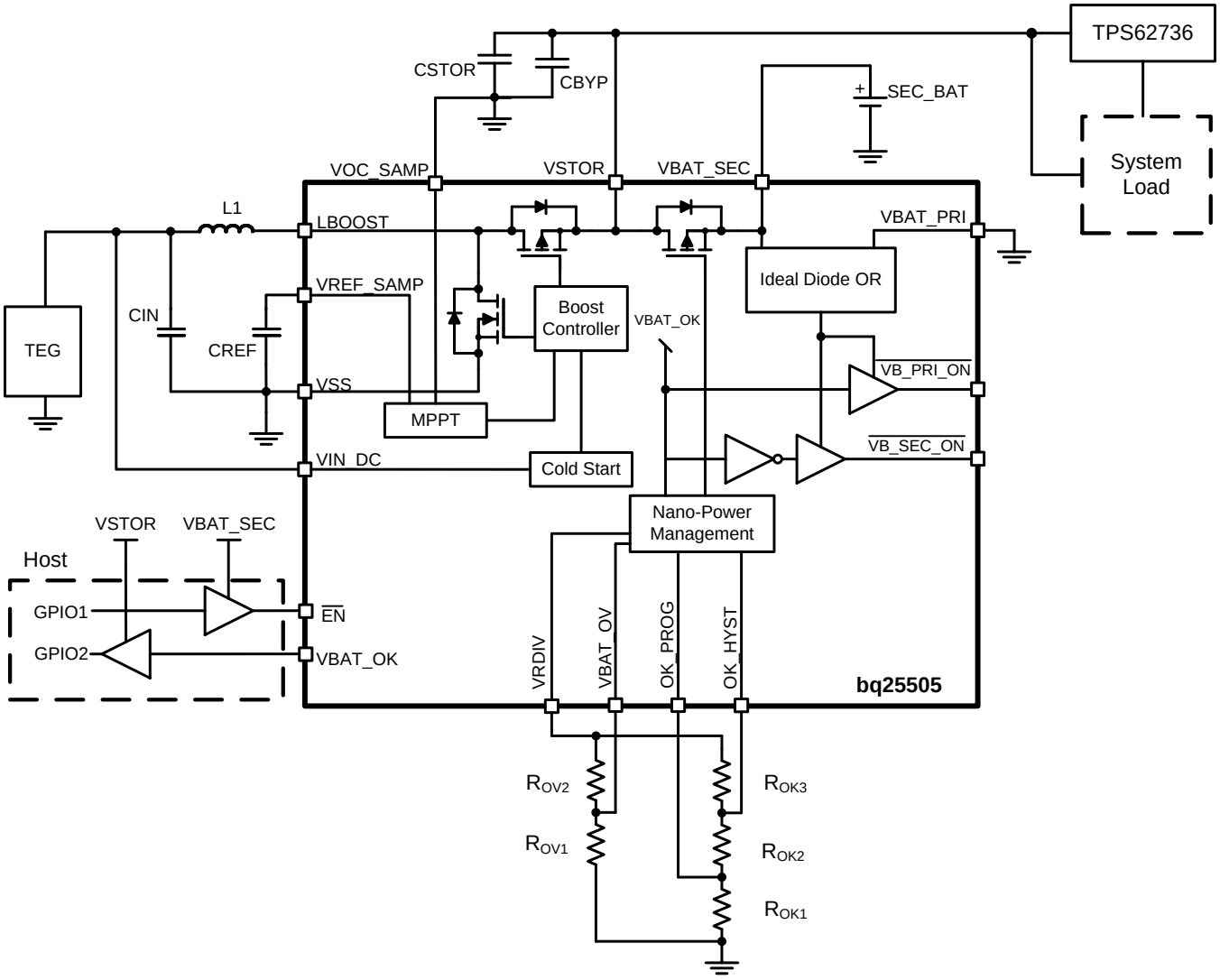


Figure 3. Typical TEG Application Circuit without a Primary Battery

VBAT_OV = 3.31 V, VBAT_OK = 2.82 V, VBAT_OK_HYST = 3.12 V, MPPT (V_{OC}) = 40%

L1 = 22 µH, CIN = CSTOR = 4.7 µF, CBYP=0.1 µF, CREF = 10 nF

R_{OK1} = 4.99 MΩ, R_{OK2} = 6.65 MΩ, R_{OK3} = 1.24 MΩ, R_{OV1} = 6.98 MΩ, R_{OV2} = 5.76 MΩ

R_{OC1} = 8.06 MΩ, R_{OC2} = 12 MΩ

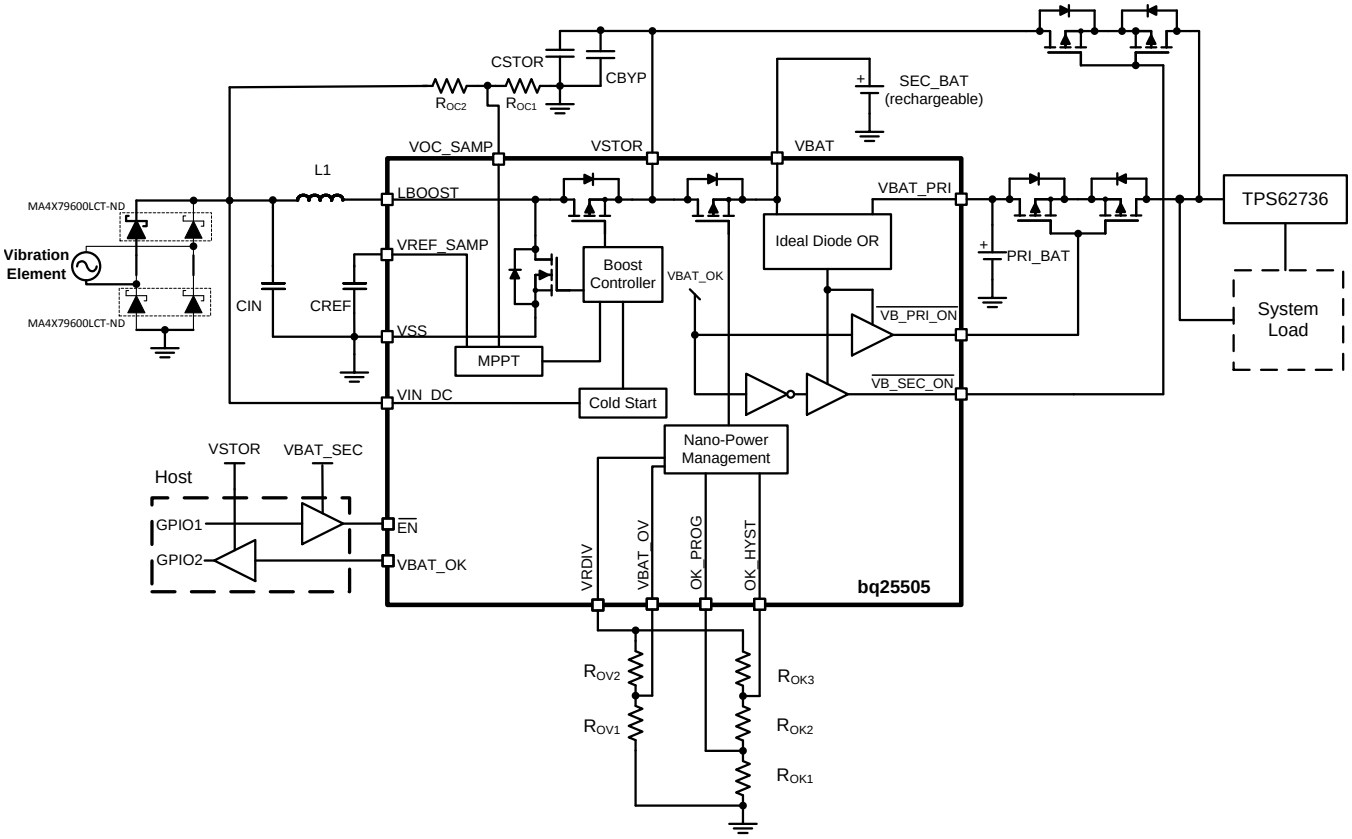


Figure 4. Typical Piezoelectric Application Circuit with Primary and Secondary Batteries

HIGH-LEVEL FUNCTIONAL BLOCK DIAGRAM

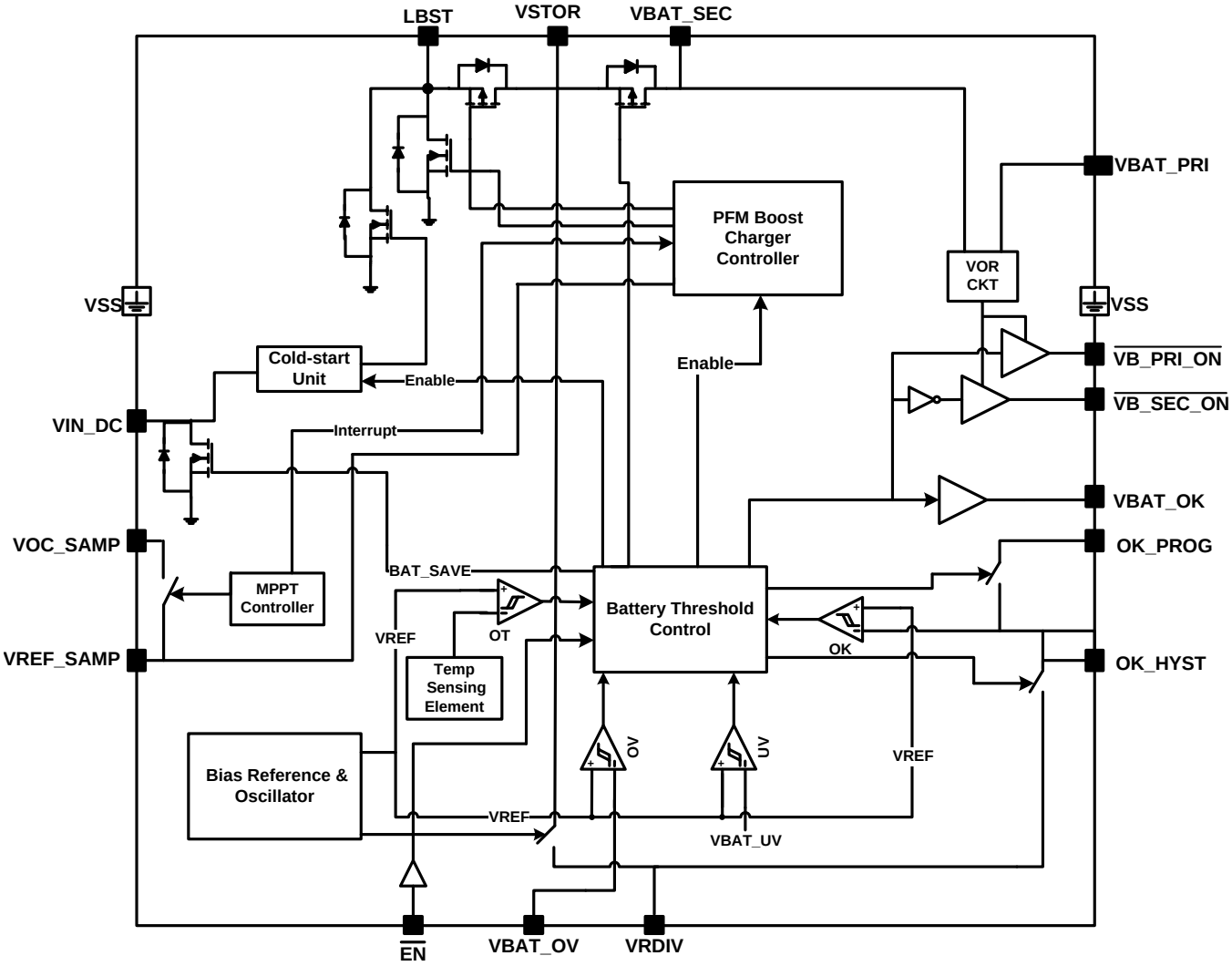


Figure 5. High-Level Functional Diagram

TYPICAL CHARACTERISTICS

Table of Graphs

Unless otherwise noted, graphs were taken using with CIN = 4.7µF, L1 = Coilcraft 22µH LPS4018, CSTOR = 4.7µF, VBAT_OV=4.2V			FIGURE
Charger Efficiency (η)(1)	vs. Input Voltage	IN= 10 µA	Figure 6
		IN= 100 µA	Figure 7
		IIN = 10 mA	Figure 8
	vs. Input Current	VIN = 2.0 V	Figure 9
		VIN = 1.0 V	Figure 10
		VIN = 0.5 V	Figure 11
		VIN = 0.2 V	Figure 12
VBAT_SEC Quiescent Current	vs. VBAT_SEC Voltage	$\overline{EN}$ = VBAT_SEC (Active Mode)	Figure 13
		$\overline{EN}$ = GND (Ship Mode)	Figure 14
VBAT_PRI Leakage Current	vs. VBAT_PRI Voltage	$\overline{EN}$ = VBAT_SEC (Ship Mode)	Figure 15
Startup by Taking EN Low (from Ship mode)	VBAT = 3.4-V charged Li coin cell; VIN_DC = 1.0 V power supply; MPPT=50%; ZIN = 100Ω		Figure 16
MPPT Operation	VBAT = 3.2-V charged Li coin cell; VIN_DC = 2.0 V power supply; ZIN = 100Ω	VOC_SAMP = VSTOR to GND to VSTOR	Figure 17
50mA Load Transient on VSTOR	VBAT = 4.2V charged 0.5 F; VIN_DC = 1.5 V power supply; MPPT=80%; ZIN = 75Ω	R(VSTOR) = open to 84 Ω to open	Figure 18
50mA Load Transient on VSTOR with Sampling		R(VSTOR) = open to 84 Ω to open	Figure 19
Charger Operational Waveform During 50mA Load Transient		R(VSTOR) = 84 Ω	Figure 20
VRDIV Waveform over Two Periods	VSTOR = 4.2V		Figure 21
VRDIV Waveform			Figure 22
VBAT_OK Operation	VSTOR ramped from 0 V to 4.2 V to 0 V with function generator		Figure 23
Multiplexor Output (VOR) as VBAT_SEC Crosses VBAT_OK Threshold	VSTOR ramped from 0 V to 4.2 V to 0 V with function generator; VBAT_PRI = 3.6V power supply	VBAT_SEC = 0.5 F super capacitor; 1kΩ load on VOR	Figure 24
Multiplexor Signals When VBAT_SEC > VBAT_OK Threshold	$\overline{VB\_PRI\_ON}$ goes high; $\overline{VB\_SEC\_ON}$ goes low		Figure 25
Multiplexor Signals When VBAT_SEC < VBAT_OK Threshold	$\overline{VB\_PRI\_ON}$ goes low; $\overline{VB\_SEC\_ON}$ goes low		Figure 26
Charging a Super Cap on VBAT	VIN_DC = sourcemeter with compliance = 1.2 V and ISC = 1.0 mA	VBAT_SEC = 120 mF super capacitor	Figure 27

(1) See SLUA691 for an explanation on how to take these measurements. Because the MPPT feature cannot be disabled on the bq25505, these measurements need to be taken in the middle of the 16 s sampling period.

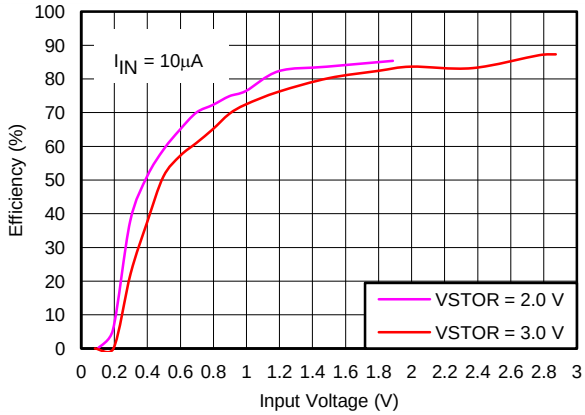


Figure 6. Charger Efficiency vs Input Voltage

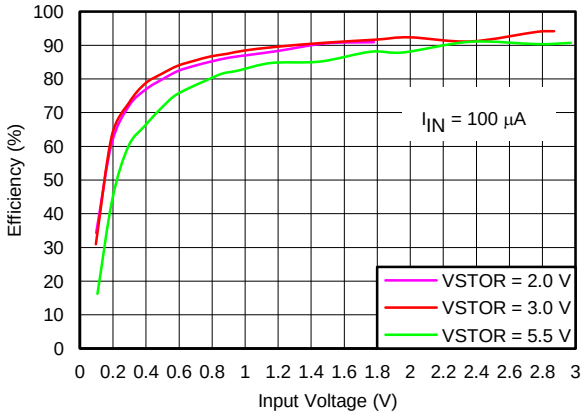


Figure 7. Charger Efficiency vs Input Voltage

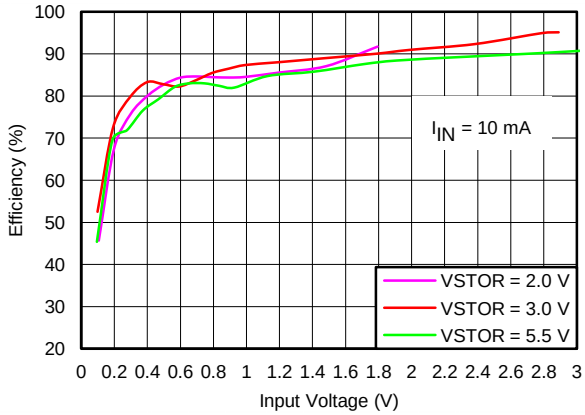


Figure 8. Charger Efficiency vs Input Voltage

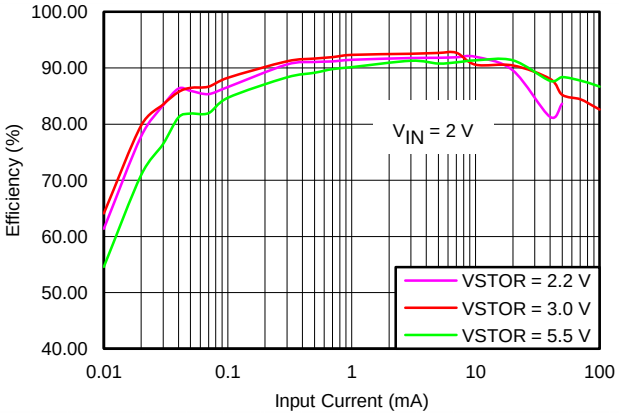


Figure 9. Charger Efficiency vs Input Current

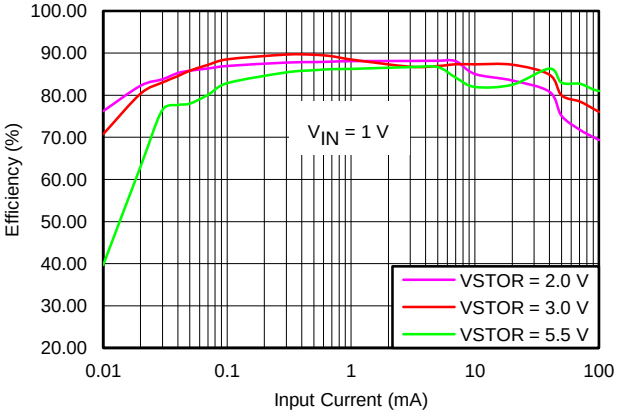


Figure 10. Charger Efficiency vs Input Current

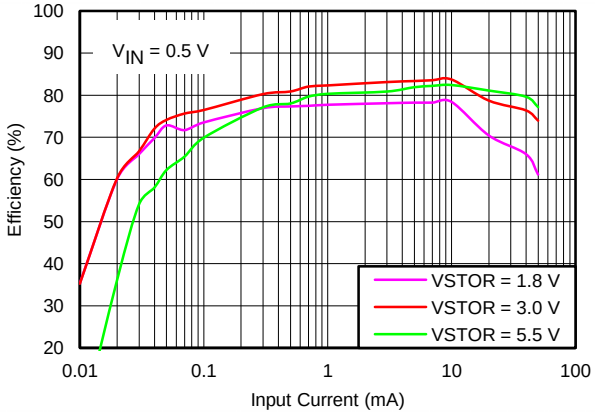


Figure 11. Charger Efficiency vs Input Current

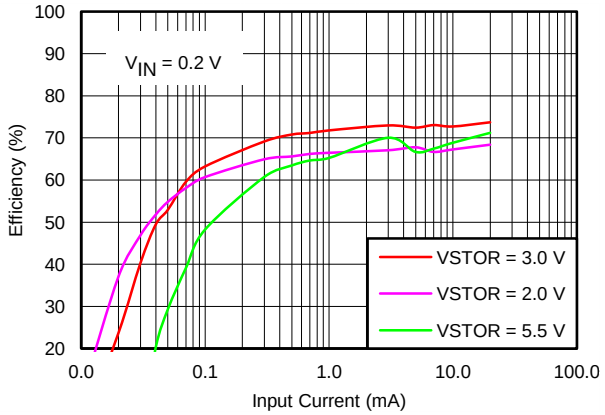


Figure 12. Charger Efficiency vs Input Current

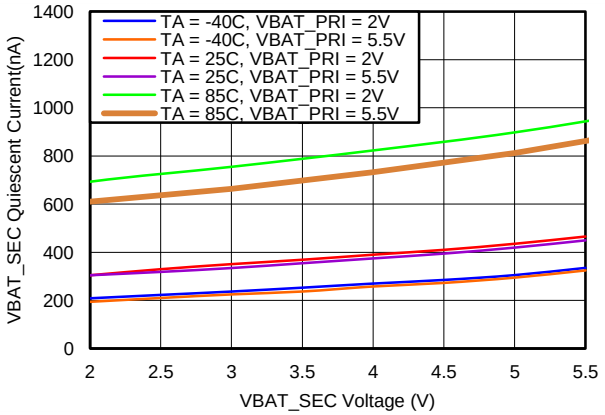


Figure 13. Quiescent Current vs VBAT_SEC Voltage: Active Mode

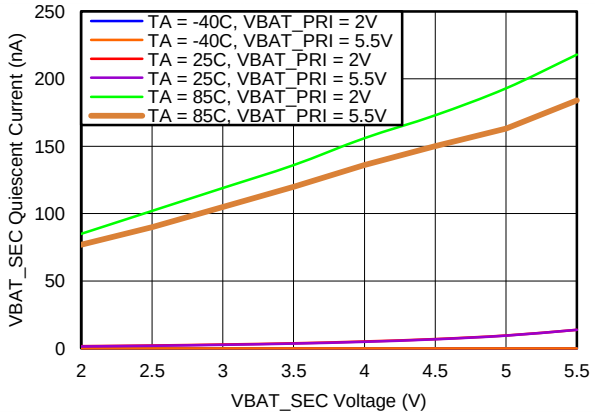


Figure 14. Quiescent Current vs VBAT_SEC Voltage: Ship Mode

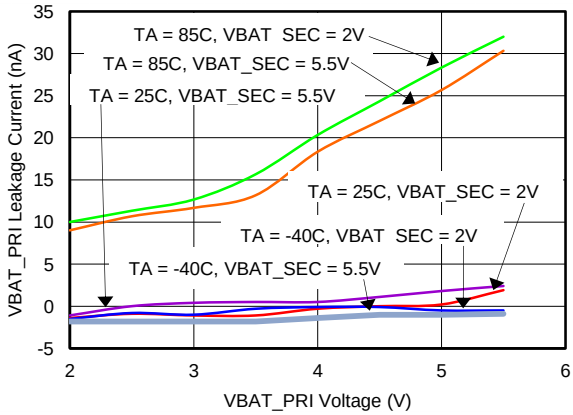


Figure 15. VBAT_PRI Leakage Current vs VBAT_PRI Voltage

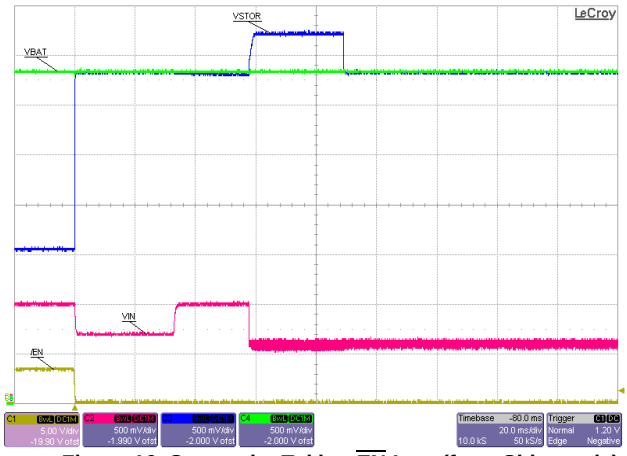


Figure 16. Startup by Taking $\overline{EN}$ Low (from Ship mode)

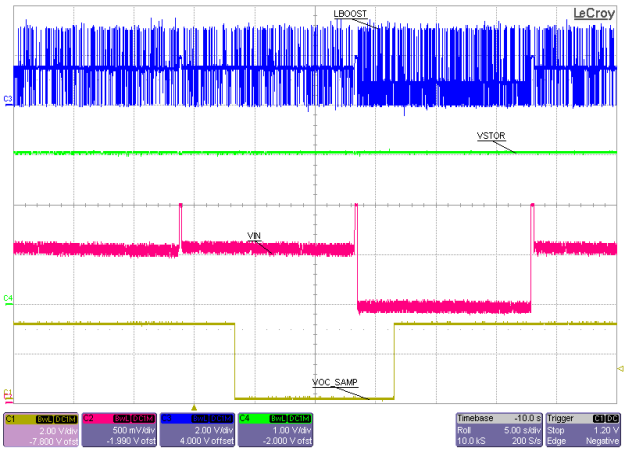


Figure 17. MPPT Operation

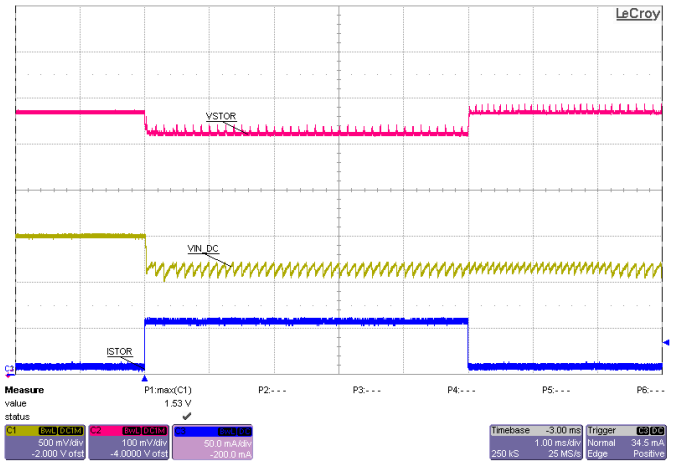


Figure 18. 50 mA Load Transient on VSTOR

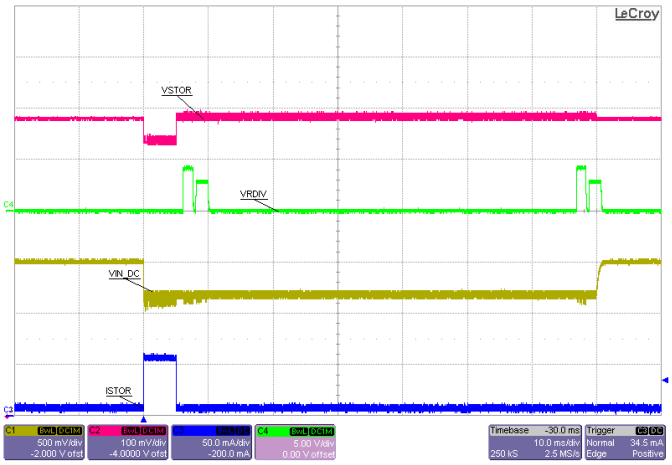


Figure 19. 50 mA Load Transient on VSTOR - Zoom Out

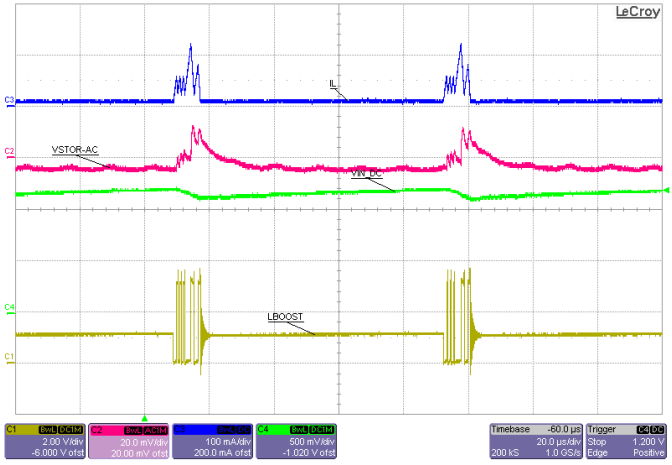


Figure 20. Charger Operational Waveforms During 50 mA Load Transient

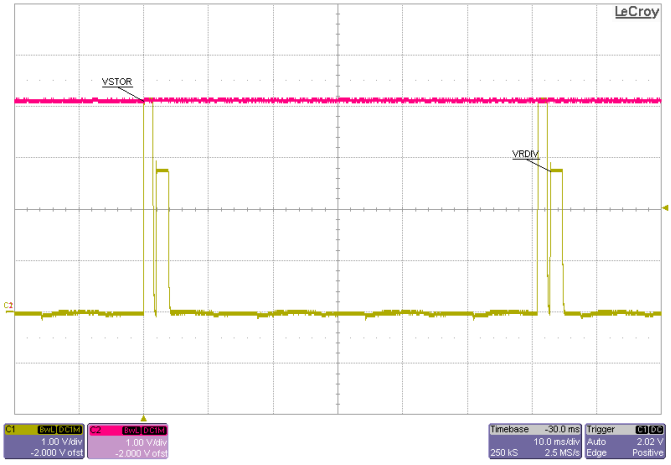


Figure 21. VRDIV Waveform over Two Periods

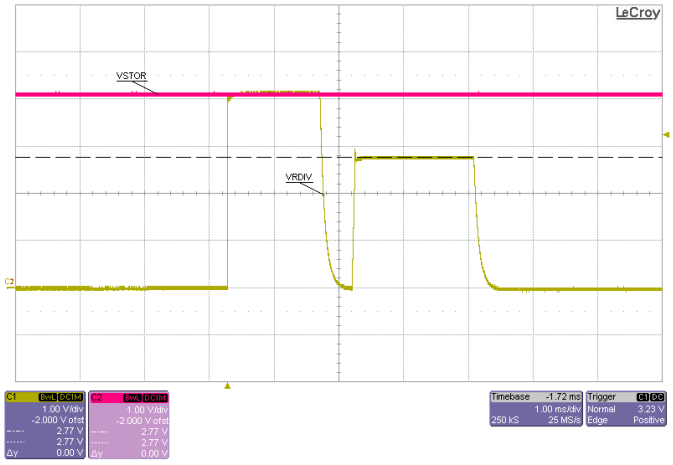


Figure 22. VRDIV Waveform

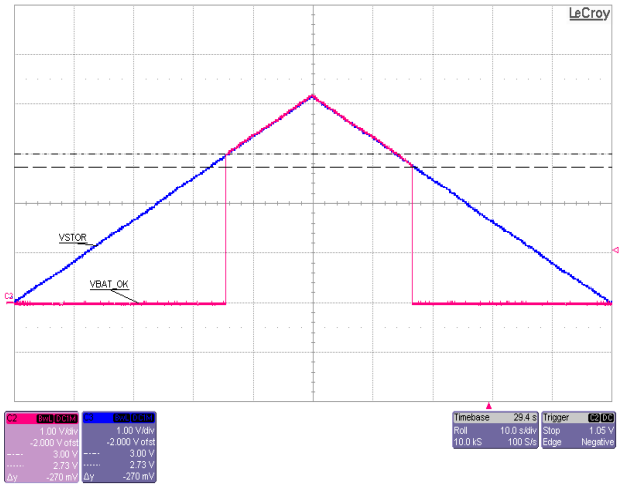


Figure 23. VBAT_OK Operation

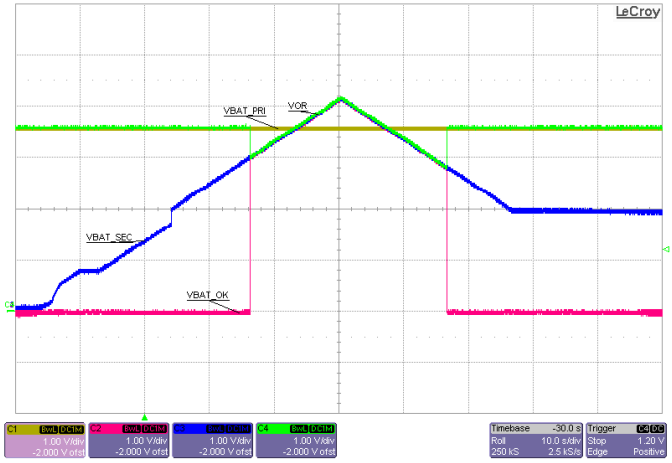


Figure 24. Multiplexor Output (VOR) as VBAT_SEC Crosses VBAT_OK Threshold

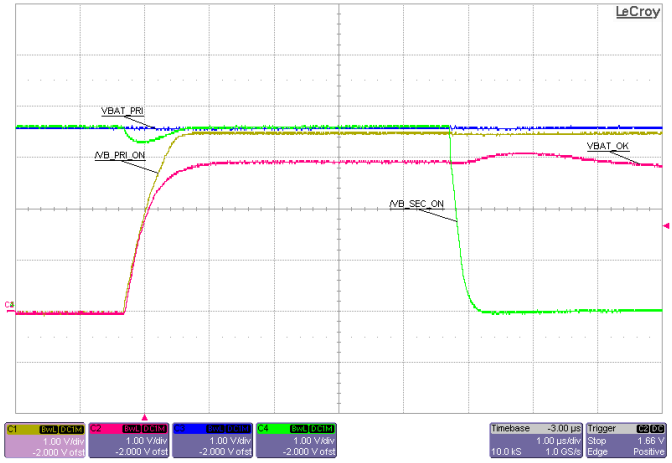


Figure 25. MUX Signals When VBAT_SEC > VBAT_OK Threshold

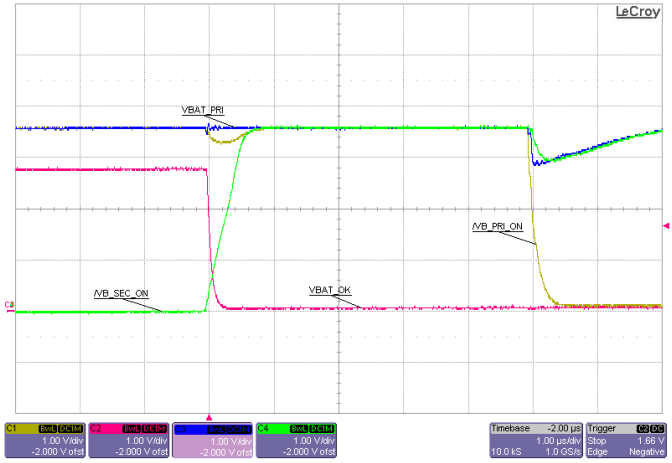


Figure 26. MUX Signals When VBAT_SEC < VBAT_OK threshold

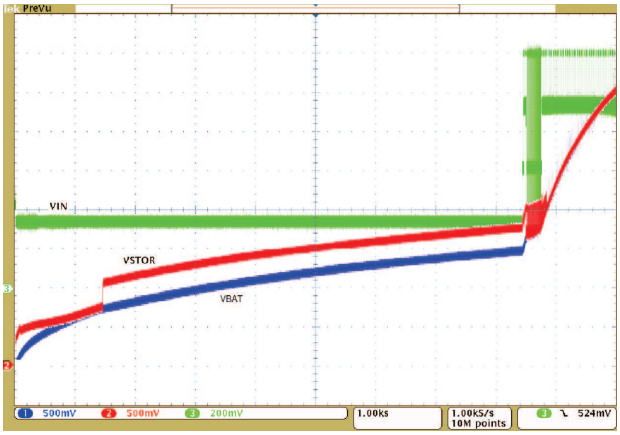


Figure 27. Charging a Super Cap on VBAT_SEC

DETAILED DESCRIPTION

Boost Charger Overview

The bq25505 is based on an ultra low quiescent current, efficient synchronous boost charger. The boost charger is intended to be powered from a high impedance DC source, such as a solar panel, TEG or piezoelectric module; therefore, it regulates its input voltage (VIN_DC) in order to prevent the input source from collapsing. The boost charger monitors its output voltage (VSTOR) and stops switching when VSTOR reaches a resistor programmable threshold level. The boost charger is based on a switching regulator architecture which maximizes efficiency while minimizing start-up and operation power. It uses pulse frequency modulation (PFM) to maintain efficiency, even under light load conditions. In addition, the boost charger implements battery protection features so that either rechargeable batteries or capacitors can be used as energy storage elements at the rechargeable storage element output (VBAT_SEC). Figure 5 is a high-level functional block diagram which highlights most of the major functional blocks inside the bq25505.

Enable Controls

There is one enable pin implemented in bq25505 in order to maximize the flexibility of control for the system. When taken high, the $\overline{EN}$ pin shuts down the IC completely including the boost charger and battery management circuitry. It also turns off the PFET that connects VBAT_SEC to VSTOR. This can be described as ship mode, because it will put the IC in the lowest leakage state and provide a long storage period without discharging the battery on VBAT_SEC. If there is no need to control $\overline{EN}$, it is recommended that this pin be tied to VSS, or system ground.

Startup Operation

The bq25505 has two circuits for boosting the input voltage, a low-power cold-start circuit, drawing power exclusively from VIN_DC when ≥ VIN(CS), and the high efficiency main boost charger, with the bias rails drawing power from VSTOR when ≥ VSTOR_CHGEN and the power stage drawing power from VIN_DC when ≥ VIN(DC) minimum. When $\overline{EN}$ = 0 and VSTOR ≤ VSTOR_CHGEN, there are two options for charging the VSTOR capacitor, CSTOR, to VSTOR_CHGEN for the main boost charger to turn on. The first option, shown in Figure 28, is to allow the cold start circuit to charge VSTOR to VSTOR_CHGEN. Due to the body diode of the PFET connecting VSTOR and VBAT_SEC, the cold start circuit must charge both the capacitor on CSTOR and the storage element connected to VBAT_SEC up to VSTOR_CHGEN. When a rechargeable battery with an open protector is attached, the charge time is typically short due to the minimum charge needed to close the FET. When large, discharged super capacitors are attached, the charge time can be signficant. The second option, shown in Figure 29, is to connect a storage element, charged above VSTOR_CHGEN, to VBAT_SEC. Assuming the voltages on VSTOR and VBAT_SEC are both below 100mV, when a charged storage element is attached (i.e. hot-plugged) to VBAT_SEC, the IC turns on the internal PFET between the VSTOR and VBAT_SEC pins for $t_{BAT\_HOT\_PLUG}$ in order to charge CSTOR to VSTOR_CHGEN. If a system load tied to VSTOR prevents the storage element from charging VSTOR within $t_{BAT\_HOT\_PLUG}$, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal can be used to drive the gate of this system-isolating PFET. Once the VSTOR pin voltage reaches the internal under voltage threshold (VBAT_UV), the internal PFET stays on and the main boost charger begins to charge the storage element if there is sufficient power available at the VIN_DC pin, as explained below. If VSTOR does not reach VBAT_UV within 50ms, then the PFET turns off and the cold-start circuit turns on, also as explained below.

Boost Charger Cold-Start Operation (VSTOR < VSTOR_CHGEN and VIN_DC > VIN(CS))

If the attached storage element does not charge CSTOR above VSTOR_CHGEN, VIN_DC ≥ VIN(CS), the cold-start circuit turns on. The cold-start circuit is essentially an unregulated boost converter with lower efficiency compared to the main boost charger. The energy harvester must supply sufficient power for the IC to exit cold start. See the Energy Harvester Selection applications section for guidance.

When the CSTOR voltage reaches VSTOR_CHGEN, the main boost charger starts up. The VSTOR voltage from the main boost charger is compared against the battery undervoltage threshold (VBAT_UV). When the VBAT_UV threshold is reached, the PMOS switch between VSTOR and VBAT_SEC turns on, which allows the energy storage element attached to VBAT_SEC to charge up. Cold start is not as efficient as the main boost regulator. If sufficient input power is not available, it is possible that the cold start circuit continuously runs and the VSTOR output does not increase above VSTOR_CHGEN for the main boost conveter to start up. The battery management thresholds are explained later is this section. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

Main Boost Charger Operation (VSTOR > VSTOR_CHGEN and VIN_DC > VIN(DC))

The main boost charger charges the storage element attached to VBAT_SEC with the energy available from the high impedance input source. For the first 32 ms (typical) after the main charger is turned on (assuming $\overline{EN}$ is low), the charger is disabled to let the input rise to its open-circuit voltage. This sample period is required to get the reference voltage which will be used for the remainder of the charger operation till the next MPPT sampling cycle. The boost charger employs pulse frequency modulation (PFM) mode of control to regulate the voltage at VIN_DC close to the desired reference voltage. The reference voltage is set by the MPPT control scheme as described in the next section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is dithered internally to pre-determined levels in order to maintain high efficiency of the charger across a wide input current range. The charger transfers up to a maximum of 100 mA average input current (230mA typical peak inductor current). The boost charger is disabled when the voltage on VSTOR reaches the user set VBAT_OV threshold to protect the battery connected at VBAT_SEC from overcharging. In order for the battery to charge to VBAT_OV, the input power must exceed the power needed for the load on VSTOR. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in order to maximize the power extracted from an energy harvester source. The boost converter indirectly modulates the impedance of main boost charger by regulating the charger's input voltage, as sensed by the VIN_DC pin, to the sampled reference voltage, as stored on the VREF_SAMP pin. The MPPT circuit obtains a new reference voltage 16 s (typical) by periodically disabling the charger for 256 ms (typical) and sampling a fraction of the open-circuit voltage. For solar harvesters, the maximum power point is typically 70%-80% and for thermoelectric harvesters, the MPPT is typically 50%. Tying VOC_SAMP to VSTOR internally sets the MPPT regulation point to 80% of VOC. Tying VOC_SAMP to GND internally sets the MPPT regulation point to 50% of VOC. If input source does not have either 80% or 50% of VOC as its MPP point, the exact ratio for MPPT can be optimized to meet the needs of the input source being used by connecting external resistors R_{OC1} and R_{OC2} between VRDIV and GND with mid-point at VOC_SAMP.

The reference voltage is set by the following expression:

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

Storage Element / Battery Management

In this section the battery management functionality of the bq25505 integrated circuit (IC) is presented. The IC has internal circuitry to manage the voltage across the storage element and to optimize the charging of the storage element. For successfully extracting energy from the source, two different threshold voltages must be programmed using external resistors, namely battery good threshold (VBAT_OK) and over voltage (OV) threshold. The two user programmable threshold voltages and the internally set undervoltage threshold determine the IC's region of operation. Figure 28 and Figure 29 show plots of the voltage at the VSTOR pin and the various threshold voltages for two use cases 1) when a depleted battery on VBAT_SEC is attached and the charger enters cold start and 2) when a battery at VBAT_SEC charged above VBAT_UV is attached. For the best operation of the system, the VBAT_OK should be used to determine when a load can be applied or removed. A detailed description of the three voltage thresholds and the procedure for designing the external resistors for setting the three voltage thresholds are described next.

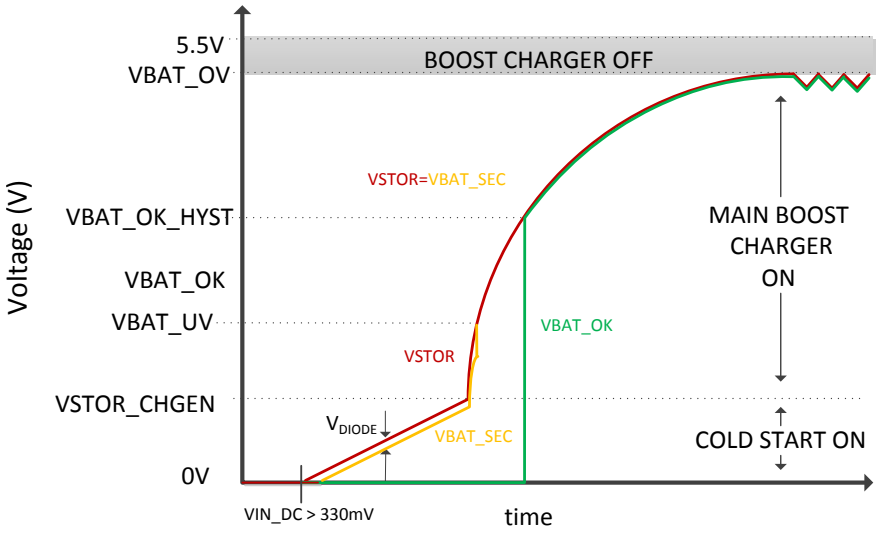


Figure 28. Charger Operation after a Depleted Storage Element is Attached

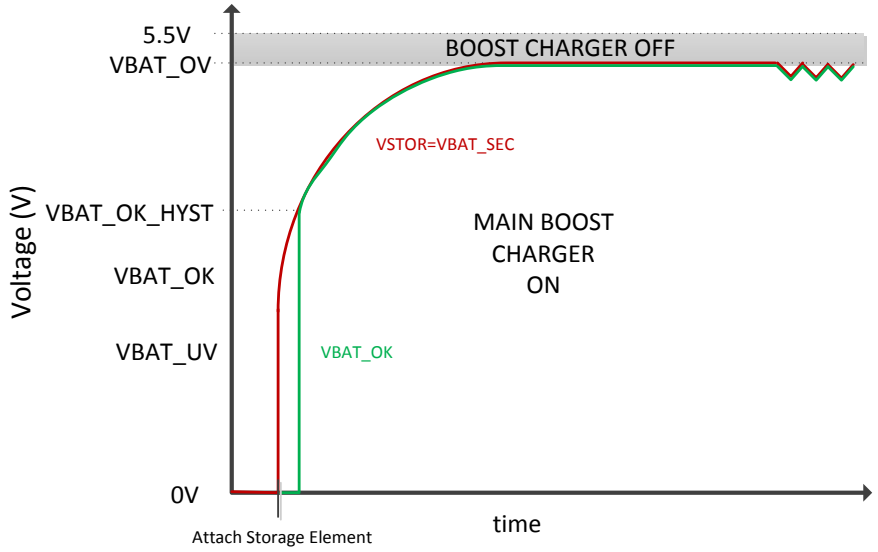


Figure 29. Charger Operation after a Partially Charged Storage Element is Attached

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (e.g., the battery protector PFET is closed) and with the VSTOR node above ground results in the PFET between VSTOR and VBAT_SEC remaining off until an input source is attached. In addition, if a system load attached to VSTOR has fast transients that could pull VSTOR below VBAT_UV, the internal PFET switch will turn off in order to recharge the CSTOR capacitor to VSTOR_CHGEN. See the application section for guidance on sizing the VSTOR and/or VBAT_SEC capacitance to account for transients. If the voltage applied at VIN_DC is greater than VSTOR or VBAT_SEC then current may flow until the voltage at the input is reduced or the voltage at VSTOR and VBAT_SEC rise. This is considered an abnormal condition and the boost charger does not operate.

Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the IC has an internally set undervoltage (VBAT_UV) threshold plus an internal hysteresis voltage (VBAT_UV_HYST). The VBAT_UV threshold voltage when the battery voltage is decreasing is internally set to 1.95V (typical). The undervoltage threshold when battery voltage is increasing is given by VBAT_UV plus VBAT_UV_HYST. For most applications, the system load should be

connected to the VSTOR pin while the storage element should be connected to the VBAT_SEC pin. Once the VSTOR pin voltage goes above the VBAT_UV_HYST threshold, the VSTOR pin and the VBAT_SEC pins are shorted. The switch remains closed until the VSTOR pin voltage falls below VBAT_UV. The VBAT_UV threshold should be considered a fail safe to the system; therefore the system load should be removed or reduced based on the VBAT_OK threshold which should be set above the VBAT_UV threshold.

Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the over-voltage (VBAT_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT_SEC pin when the input has sufficient power. The VBAT_OV threshold when the battery voltage is rising is given by Equation 2:

$$VBAT\_OV = \frac{3}{2} VBIAS \left(1 + \frac{R_{OV2}}{R_{OV1}} \right) \quad (2)$$

The sum of the resistors is recommended to be no higher than 13 MΩ that is, R_{OV1} + R_{OV2} = 13 MΩ. The overvoltage threshold when battery voltage is decreasing is given by OV_HYST. It is internally set to the over voltage threshold minus an internal hysteresis voltage denoted by VBAT_OV_HYST. Once the voltage at the battery exceeds VBAT_OV threshold, the boost charger is disabled. The charger starts again once the battery voltage falls below the VBAT_OV_HYST level. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT_OV and the VBAT_OV_HYST levels. SLUC484 provides help on sizing and selecting the resistors.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is higher than VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

Battery Voltage in Operating Range (VBAT_OK Output)

The IC allows the user to set a programmable voltage independent of the overvoltage and undervoltage settings to indicate whether the VSTOR voltage (and therefore the VBAT_SEC voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by Equation 3:

$$VBAT\_OK\_PROG = VBIAS \left(1 + \frac{R_{OK2}}{R_{OK1}} \right) \quad (3)$$

When the battery voltage is increasing, the threshold is set by Equation 4:

$$VBAT\_OK\_HYST = VBIAS \left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}} \right) \quad (4)$$

The sum of the resistors is recommended to be no higher than approximately i.e., R_{OK1} + R_{OK2} + R_{OK3}= 13 MΩ. The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current to prevent MCU damage until it is fully powered. The VBAT_OK_PROG threshold must be greater than or equal to the UV threshold. For the best operation of the system, the VBAT_OK should be setup to drive an external PFET between VSTOR and the system load in order to determine when the load can be applied or removed to optimize the storage element capacity. SLUC484 provides help on sizing and selecting the resistors.

Push-Pull Multiplexor Drivers

There are two push-pull drivers intended to mulitplex between a primary non-rechargeable connected at VBAT_PRI and secondary storage element connected on VBAT_SEC based on the VBAT_OK signal. When the VBAT_OK signal goes high, indicating that the secondary rechargeable battery at VBAT_SEC is above the VBAT_OK_HYST threshold, the VB_PRI_ON output goes high followed by the VB_SEC_ON signal going low in order to connect VBAT_SEC to the system output (referred to as the VOR node). When VBAT_OK goes low, indicating that the secondary rechargeable battery at VBAT_SEC is below the VBAT_OK threshold, the VB_SEC_ON output goes high followed by the VB_PRI_ON signal going low in order to connect VBAT_PRI to the system. The drivers are designed to support up to 2 nF of gate capacitance and to drive a PMOS FET. The switching characteristics follow a break-before-make model, wherein during a transition, the drivers both go high for a typical dead time of 5 us before one of the signals goes low. The figure below shows the FET gate voltages for the transition from the secondary battery being connected to the system to the primary battery being connected.

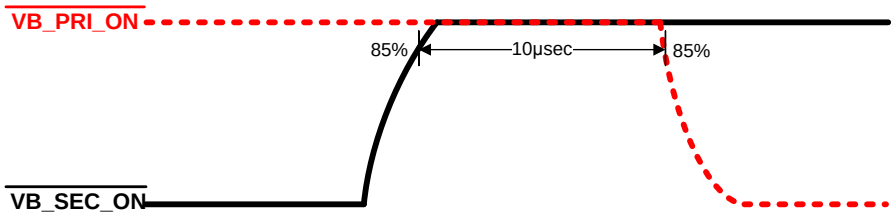


Figure 30. Break-Before-Make Operation of $\overline{\text{VB\_PRI\_ON}}$ and $\overline{\text{VB\_SEC\_ON}}$

Steady State Operation and Cycle by Cycle Behavior

Steady state operation for the boost charger is shown in Figure 20. These plots highlight the inductor current waveform, the VSTOR voltage ripple, and the LBOOST switching nodes. The charger uses hysteretic control and pulse frequency modulation (PFM) switching in order to maintain high efficiency at light load. As long as the VIN_DC voltage is above the MPPT regulation set point (i.e. voltage at VREF_SAMP), the boost charger's low-side power FET turns on and draws current until it reaches its respective peak current limit. These switching bursts continue until VSTOR reaches the VBAT_OV threshold. This cycle-by-cycle minor switching frequency is a function of each converter's inductor value, peak current limit and voltage levels on each side of each inductor. Once the VSTOR capacitor, CSTOR, droops below a minimum value, the hysteretic switching repeats.

Nano-Power Management and Efficiency

The high efficiency of the bq25505 charger is achieved via the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds all references (except for VBAT_UV) in order to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in Figure 21 where the VRDIV node is monitored. Here the VRDIV node provides a connection to the VSTOR voltage (first pulse) and then generates the reference levels for the VBAT_OV and VBAT_OK resistor dividers for a short period of time. The divided down values at each pin are sampled and held for comparison against VBIAS as part of the hysteretic control. Since this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection—hence reducing the overall quiescent current due to the resistors. This process repeats every 64 ms.

The bq25505's boost charger efficiency is shown for various input power levels in Figure 6 through Figure 12. All data points were captured by averaging the overall input current. This must be done due to the periodic biasing scheme implemented via the Nano-Power management circuitry. In order to properly measure the resulting input current when calculating the output to input efficiency, the input current efficiency data was gathered using a source meter set to average over at least 50 samples.

Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The bq25505 uses an integrated temperature sensor to monitor the junction temperature of the device. The temperature threshold for thermal protection is set to 125°C. Once the temperature threshold is exceeded, the boost charger is disabled and charging ceases. Once the temperature of the device drops below this threshold, the boost charger and buck converter resumes operation. To avoid unstable operation near the overtemp threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost charger is disabled. However, if the supply voltage drops to the VBAT_UV setting, then the switch between VBAT_SEC and VSTOR will open and protect the battery even if the device is in thermal shutdown.

APPLICATION INFORMATION

Energy Harvester Selection

The energy harvesting source (e.g., solar panel, TEG, vibration element) must provide a minimum level of power for the IC to operate as designed. The IC's minimum input power required to exit cold start can be estimated as:

$$PIN > [(I\text{-}STR\_ELM\_LEAK_{@1.8V} \times 1.8V) + (1.8V^2 / RSTOR(CS))] / 0.05$$

where $I\text{-}STR\_ELM\_LEAK_{@1.8V}$ is the storage element leakage current at 1.8V and

RSTOR(CS) is the equivalent resitive load on VSTOR during cold start and 0.05 is an estimate of the worst case efficiency of the cold start circuit.

Once the IC is out of cold start and the system load has been activated (e.g., using the VBAT_OK signal), the energy harvesting element must provide the main boost charger with at least enough power to meet the average system load. Assuming RSTOR(AVG) represents the average resistive load on VSTOR, the simplified equation below gives an estimate of the IC's minimum input power needed during system operation:

$$PIN \times \eta_{EST} > PLOAD = (VBAT\_OV^2 / RSTOR(AVG) + VBAT\_OV * I\text{-}STR\_ELM\_LEAK_{@VBAT\_OV})$$

where η_{EST} can be derived from the datasheet efficiency curves for the given input voltage and current and VBAT_OV. The simplified equation above assumes that, while the harvester is still providing power, the system goes into low power or sleep mode long enough to charge the storage element so that it can power the system when the harvester eventually is down. Refer to SLUC463 for a design example that sizes the energy harvester.

Storage Element Selection

In order for the charge management circuitry to protect the storage element from over-charging or discharging, the storage element must be connected to VBAT pin and the system load tied to the VSTOR pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100uF equivalent capacitance is required to filter the pulse currents of the PFM switching charger. The equivalent capacitance of a battery can be computed as computed as:

$$C_{EQ} = 2 \times mAHr_{BAT(CHRGD)} \times 3600\ s/Hr / V_{BAT(CHRGD)}$$

In order for the storage element to be able to charge VSTOR capacitor (CSTOR) within the $t_{VB\_HOT\_PLUG}$ (50 ms typical) window at hot-plug; therefore preventing the IC from entering cold start, the time constant created by the storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than $t_{VB\_HOT\_PLUG}$. For example, a battery's resistance can be computed as:

$R_{BAT} = V_{BAT} / I_{BAT(CONTINUOUS)}$ from the battery specifications.

The storage element must be sized large enough to provide all of the system load during periods when the harvester is no longer providing power. The harvester is expected to provide at least enough power to fully charge the storage element while the system is in low power or sleep mode. Assuming no load on VSTOR (i.e., the system is in low power or sleep mode), the following equation estimates charge time from voltage VBAT1 to VBAT2 for given input power is:

$$PIN \times \eta_{EST} \times t_{CHRG} = 1/2 \times CEQ \times (VBAT2^2 - VBAT1^2)$$

Refer to SLUC463 for a design example that sizes the storage element.

Note that if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7uF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. See below for guidance on sizing capacitors.

Inductor Selection

The boost charger needs an appropriately sized inductor for proper operation. The inductor's saturation current should be at least 25% higher than the expected peak inductor currents recommended below if system load transients on VSTOR are expected. Since this device uses hysteretic control, the boost charger is considered naturally stable systems (single order transfer function).

For the boost charger to operate properly, an inductor of appropriate value must be connected between LBOOST, pin 20, and VIN_DC, pin 2. The boost charger internal control circuitry is designed to control the switching behavior with a nominal inductance of 22 µH ± 20%. The inductor must have a peak current capability of > 300 mA with a low series resistance (DCR) to maintain high efficiency.

A list of inductors recommended for this device is shown in Table 1.

Table 1.

Inductance (µH)	Dimensions (mm)	Part Number	Manufacturer
22	4.0x4.0x1.7	LPS4018-223M	Coilcraft
22	3.8x3.8x1.65	744031220	Wuerth

Capacitor Selection

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

VREF_SAMP Capacitance

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, it is recommended that the capacitor be an X7R or COG low leakage capacitor.

VIN_DC Capacitance

Energy from the energy harvester input source is initially stored on a capacitor, CIN, connected to VIN_DC, pin 2, and VSS, pin 1. For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but a minimum value of 4.7 µF is recommended.

VSTOR Capacitance

Operation of the bq25505 requires two capacitors to be connected between VSTOR, pin 19, and VSS, pin 1. A high frequency bypass capacitor of at 0.01 µF should be placed as close as possible between VSTOR and VSS. In addition, a low ESR capacitor of at least 4.7 µF should be connected in parallel.

Additional Capacitance on VSTOR or VBAT_SEC

If there are large, fast system load transients and/or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT_UV threshold in response to the transient. This causes the bq25505 to turn off the PFET switch between VSTOR and VBAT_SEC and turn on the boost charger. The CSTOR capacitors may further discharge below the VSTOR_CHGEN threshold and cause the bq25505 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increasing the CSTOR capacitance or adding additional capacitance in parallel with the storage element is recommended. For example, if boost charger is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 µs duration infrequently occurs, then, solving I = C x dv/dt for CSTOR gives:

$$\text{CSTOR} \geq 500\ \text{mA} \times 50\ \mu\text{s}/(4.2\ \text{V} - 1.8\ \text{V}) = 10.5\ \mu\text{F} \quad (5)$$

Note that increasing CSTOR is the recommended solution but will cause the boost charger to operate in the less efficient cold start mode for a longer period at startup compared to using CSTOR = 4.7 µF. If longer cold start run times are not acceptable, then place the additional capacitance in parallel with the storage element.

For a recommended list of standard components, see the EVM User's guide (SLUUAA8).

LAYOUT CONSIDERATIONS

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1 uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost charger inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. It is best to use vias and bottom traces for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (e.g. from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPad should not be used as a power ground return path.

The remaining pins are either NC pins, that should be connected to the PowerPad as shown below, or digital signals with minimal layout restrictions. See the EVM user's guide for an example layout (SLUUAA8).

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. In addition, the sample and hold circuit output capacitor on VREF_SAMP must hold the voltage for 16 s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 Mohm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

THERMAL CONSIDERATIONS

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

REVISION HISTORY

Changes from Original (August 2013) to Revision A **Page**

- Changed 从产品预览改为生产数据 1

Changes from Revision A (September 2013) to Revision B **Page**

- 将特性从：能够在输入源低至 120mV 时持续能量采集改为：能够在输入源低至 100mV 时持续能量采集 1
- 将说明中的文本从：能够在 V_{IN} = 120mV 时继续能量采集。 改为：能够在 V_{IN} = 100mV 时继续采集能量。 2
- Changed Peak Input Power in the Absolute Maximum Ratings table From: MAX = 400 mW To: MAX = 510 mW 4
- Changed VIN(DC) in the Recommended Operating Conditions table From: MIN = 0.12 V MAX = 4 V To: MIN = 0.1 V MAX = 5.1 V 4
- Changed VINDC in the Electrical Characteristics table From: MIN = 120 MAX = 4000 mV To: MIN = 100 mV MAX = 5100 mV 5
- Changed PIN in the Electrical Characteristics table From: MAX = 400 mW To: MAX = 510 mW 5
- Added VDELTA, VBAT_OV - VIN(DC to the ELECTRICAL CHARACTERISTICS table 6
- Changed "Refer to SLUC41 for a design example" To: "Refer to SLUC463 for a design example" in the Energy Harvester Selection section 23
- Changed "Refer to SLUC41 for a design example" To: "Refer to SLUC463 for a design example" in the Storage Element Selection section 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25505RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ505	Samples
BQ25505RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ505	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

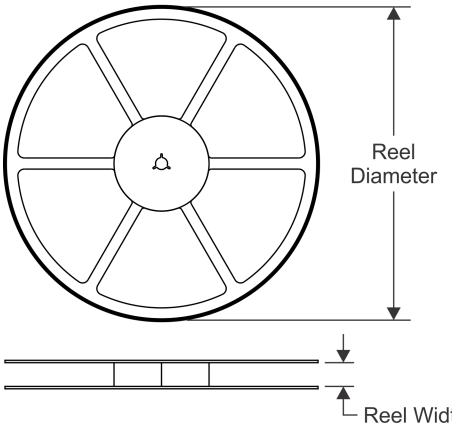
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

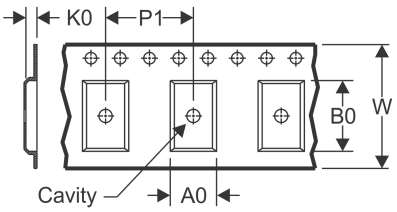
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

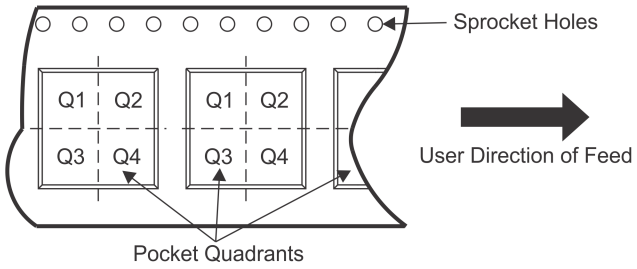


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

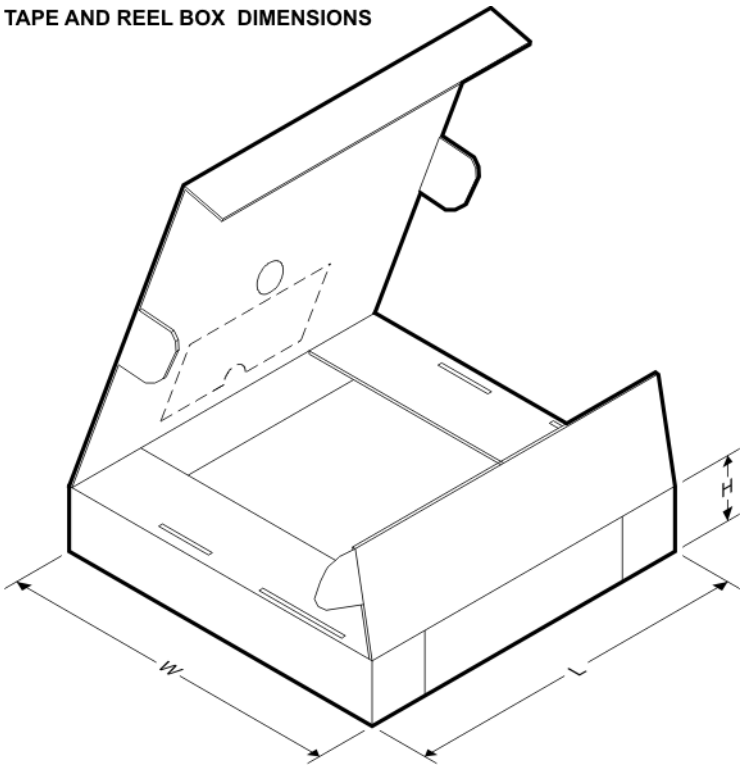
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25505RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ25505RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

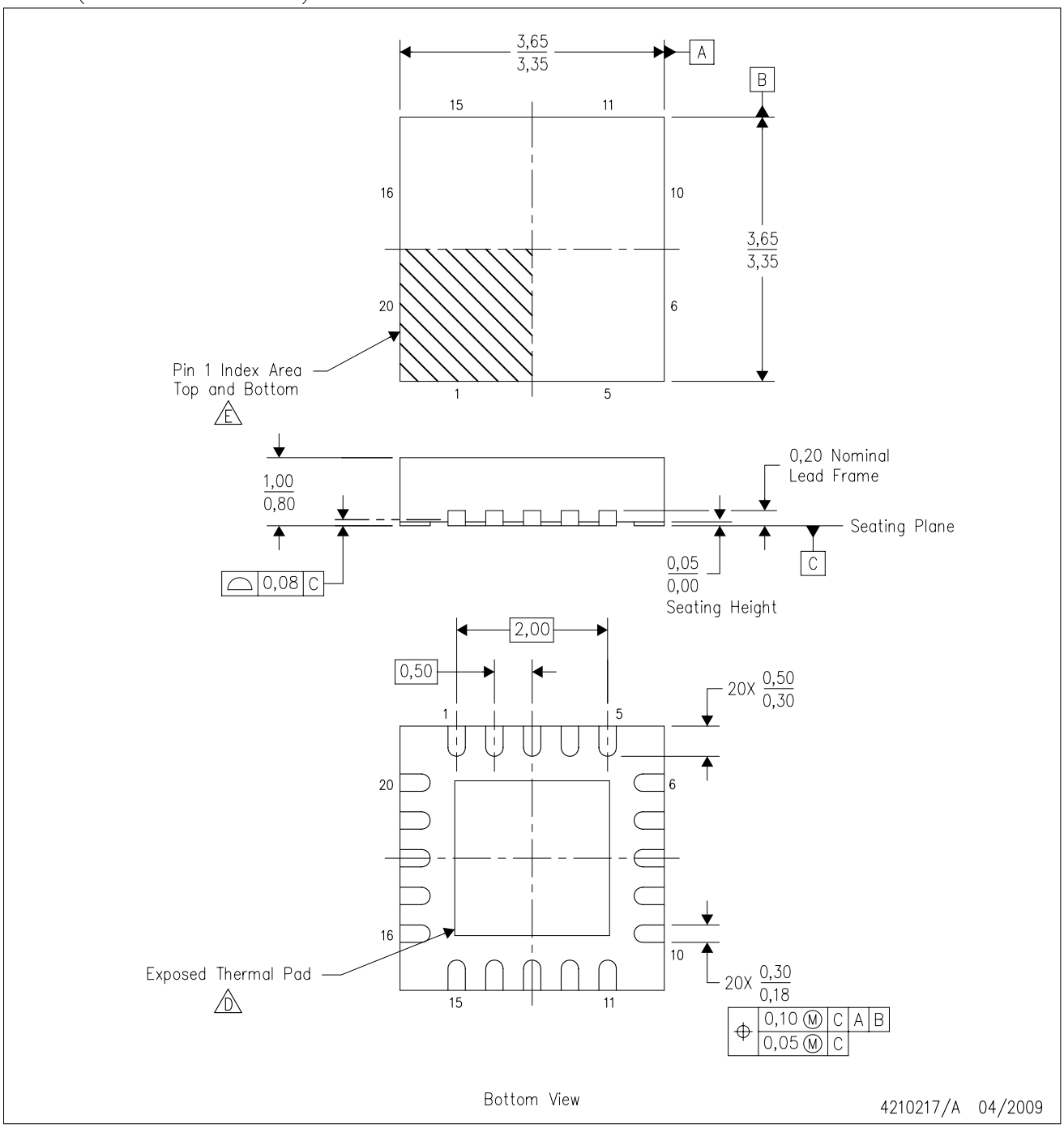
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25505RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
BQ25505RGRT	VQFN	RGR	20	250	210.0	185.0	35.0

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

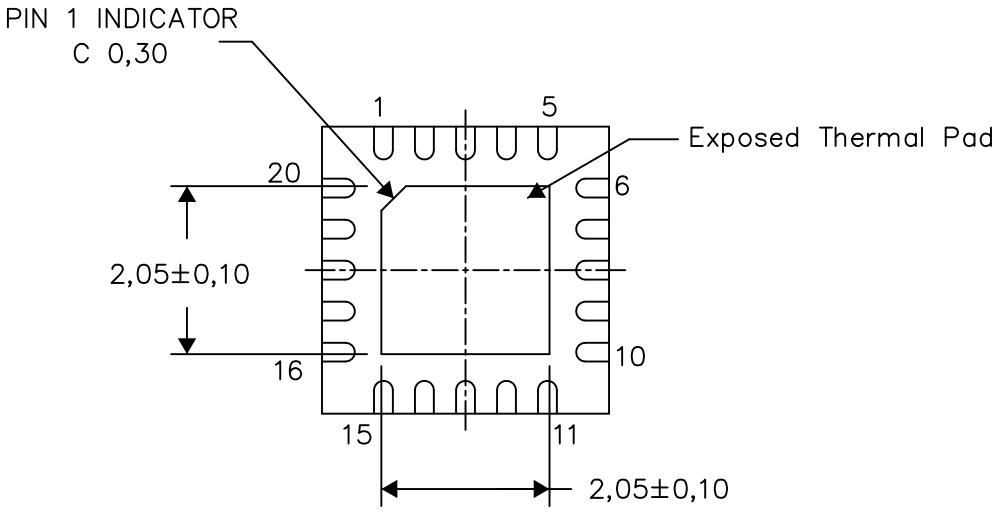
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



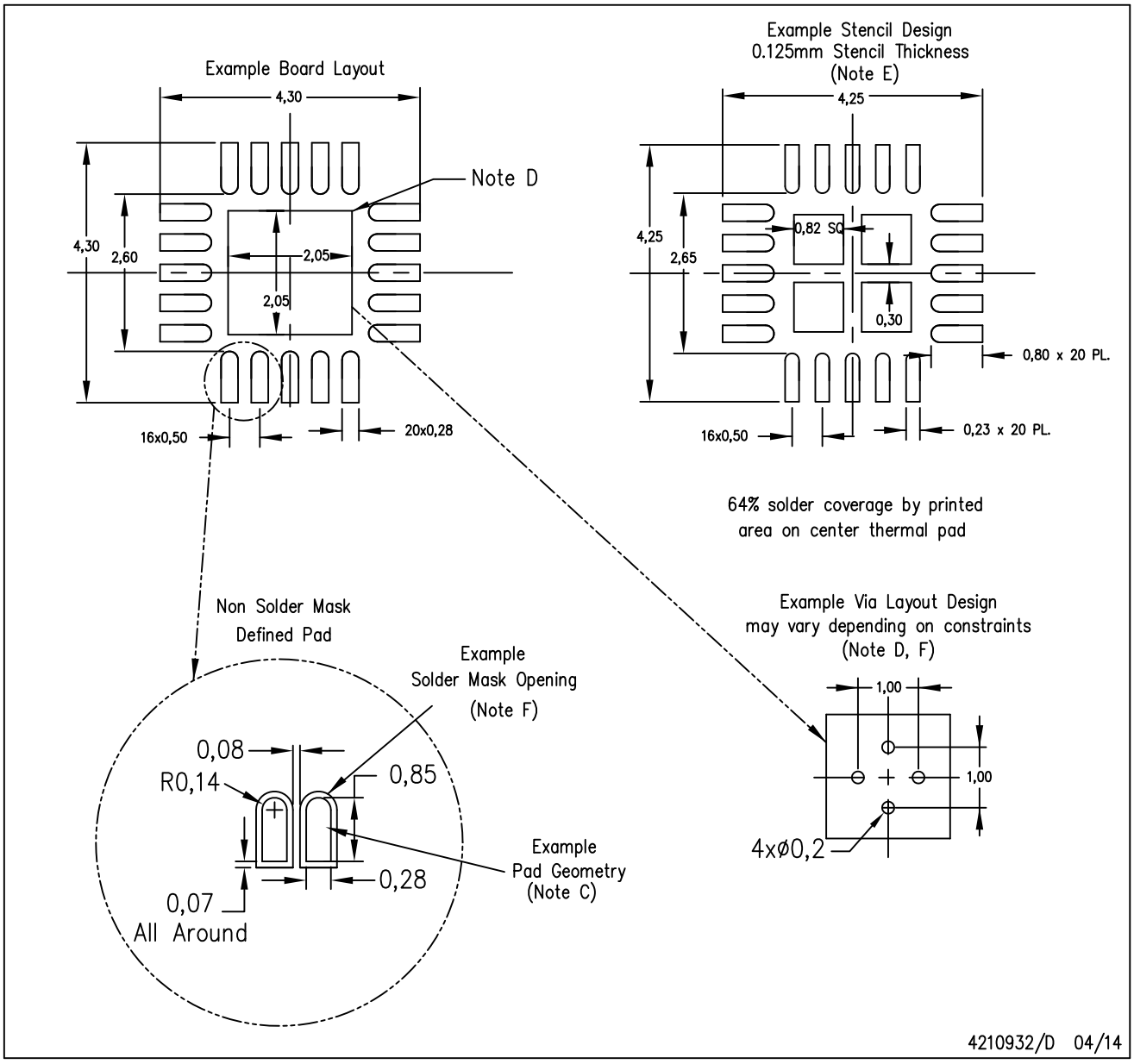
Bottom View

Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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