OPA2333-HT 1.8-V Micropower CMOS Operational Amplifier Zero-Drift Series

1 Features

- Low Offset Voltage: 26 µV (Maximum)
- 0.01-Hz to 10-Hz Noise: 1.5 μV_{PP}
- Quiescent Current: 50 µA
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Supports Extreme Temperature Applications
- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme (–55°C to 210°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments' high temperature products use highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

NOTE: Custom temperature ranges available

2 Applications

- Down-Hole Drilling
- High Temperature Environments

3 Description

The OPA2333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage and near-zero drift over time and temperature(1). These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 150 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) may be used. They are optimized for low-voltage single-supply operation.

The OPA2333 offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

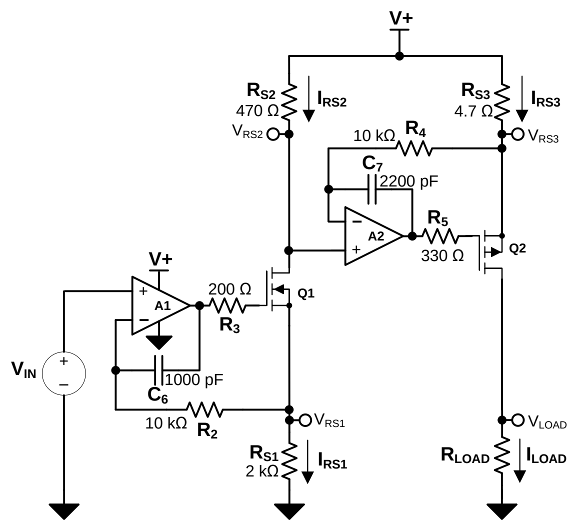
Device Information(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2333-HT	SOIC (8)	4.90 mm × 3.91 mm
	CFP (8)	6.90 mm × 5.65 mm
	CFP (8)	7.035 mm × 5.75 mm
	CDIP SB (8)	18.55 mm × 7.49 mm

(1) See *Electrical Characteristics* for performance degradation over temperature.

(2) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (November 2013) to Revision I — **Page**

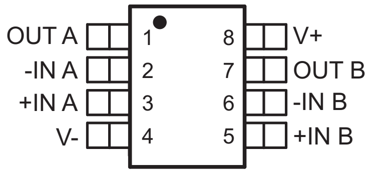
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed *Ordering Information* table 1
- Moved temperature range from *Electrical Characteristics* table to the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables 5

Changes from Revision G (September 2012) to Revision H — **Page**

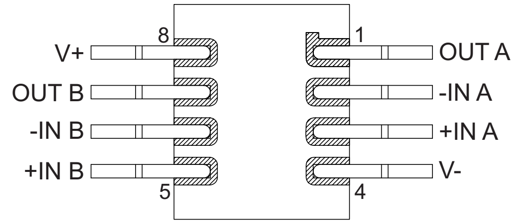
- Changed Operating Life Derating Chart 8

5 Pin Configuration and Functions

D, JD, or HKJ Package
8-Pin SOIC, CDIP SB, or CFP
Top View



HKQ Package
8-Pin CFP
Top View



HKQ as formed or HKL mounted dead bug

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Analog output channel A
2	–IN A	I	Inverting analog input channel A
3	+IN A	I	Noninverting analog input channel A
5	+IN B	I	Noninverting analog input channel B
6	–IN B	I	Inverting analog input channel B
4	V–	—	Negative (lowest) power supply
7	OUT B	O	Analog output channel B
8	V+	—	Positive (highest) power supply

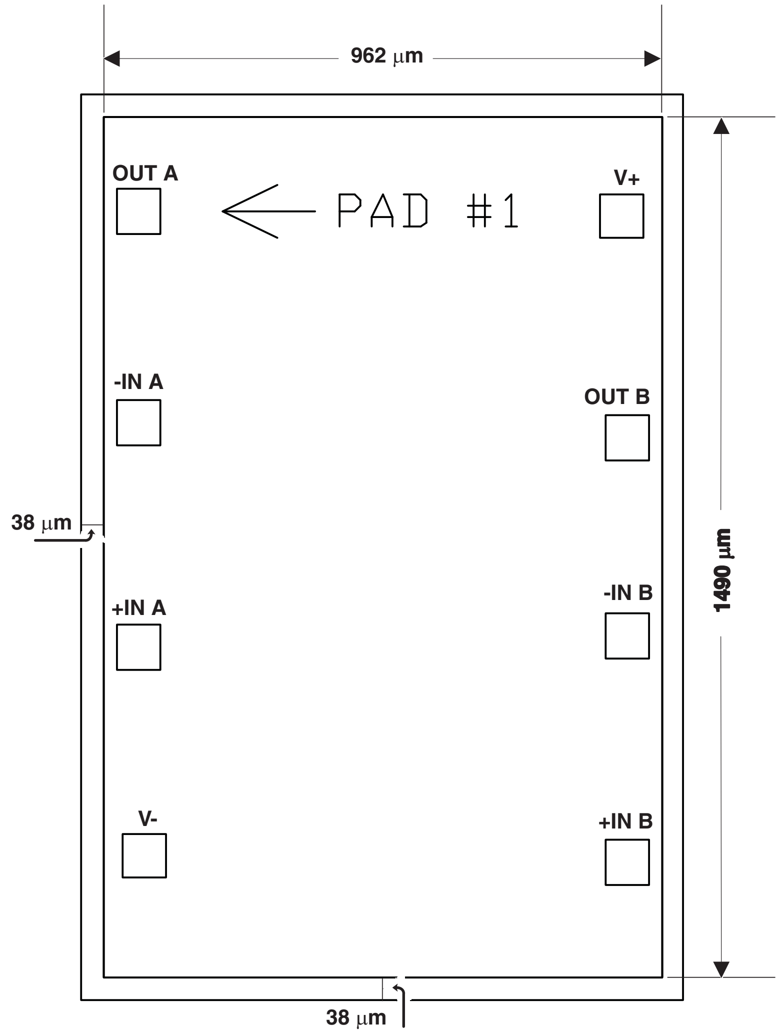


Table 1. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

Table 2. Bond Pad Coordinates

DESCRIPTION	PAD NUMBER	A	B	C	D
OUT A	1	21.20	1288.50	97.20	1364.50
–IN A	2	21.20	923.65	97.20	999.65
+IN A	3	21.20	533.05	97.20	609.05
V–	4	31.30	172.20	107.30	248.20
+IN B	5	864.80	162.25	940.80	238.25
–IN B	6	864.80	552.65	940.80	628.65
OUT B	7	864.80	897.10	940.80	973.10
V+	8	854.70	1280.45	930.70	1356.45

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			7	V
Signal input terminals, voltage(2)		–0.3	(V+) + 0.3	V
Output short circuit(3)		Continuous		
Operating temperature	JD, HKJ, HKQ packages	–55	210	°C
	D package	–55	175	
Junction temperature	JD, HKJ, HKQ packages		210	°C
	D package		175	
Storage temperature, T_{stg}		–65	210	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		1.8 (±0.9)	5 (±2.5)	5.5 (±2.75)	V
Operating temperature	JD, HKJ, HKQ packages	–55		210	°C
	D package	–55		175	

6.4 Thermal Information

THERMAL METRIC(1)			OPA2333-HT				UNIT
			JD (CDIP SB)	HKJ (CFP)	HKQ (CFP)	D (SOIC)	
			8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	High-K board(3), no airflow	—	—	—	117.5	°C/W
		No airflow	—	—	—	—	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		53.8	57.7		62.0	°C/W
		to ceramic side of case	—	—	15.2	—	
		to top of case lid (metal side of case)	—	—	—	—	
$R_{\theta JB}$	Junction-to-board thermal resistance	High-K board without underfill	76.0	61.0	151.6	57.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		—	—	—	19.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter		—	—	—	57.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		26.7	15.2	56.9	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The intent of $R_{\theta JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment.
This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(3) JED51-7, high effective thermal conductivity test board for leaded surface mount packages

6.5 Electrical Characteristics

V_S = 1.8 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V	T_A = 25°C		2	10	µV
			T_A = –55°C to 125°C			22	
			T_A = –55°C to 175°C (1)			26	
			T_A = –55°C to 210°C (2)			26	µV
dV_{OS}/d_T	Input Offset Voltage Temperature Drift	V_S = 5 V	T_A = –55°C to 125°C		0.02		µV/°C
			T_A = –55°C to 175°C (1)		0.05		
			T_A = –55°C to 210°C (2)		0.05		
PSRR	Input Offset Voltage vs Power Supply	V_S = 1.8 V to 5.5 V	T_A = –55°C to 125°C		1	6	µV/V
			T_A = –55°C to 175°C (1)		1.2	8	
			T_A = –55°C to 210°C (2)		1.7	11	
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±70	±200	pA
		T_A = –55°C to 125°C			±150		
		T_A = –55°C to 175°C			±1250		
		T_A = –55°C to 210°C			±5300		
I_{OS}	Input offset current	T_A = –55°C to 125°C			±140	±400	pA
		T_A = –55°C to 175°C			±700		
		T_A = –55°C to 210°C			±10600		
NOISE							
	Input Noise Voltage	f = 0.01 Hz to 1 Hz	T_A = –55°C to 125°C		0.3		$µV_{PP}$
			T_A = –55°C to 175°C (1)		1		
			T_A = –55°C to 210°C (2)		1		
		f = 0.1 Hz to 10 Hz	T_A = –55°C to 125°C		1.1		$µV_{PP}$
			T_A = –55°C to 175°C (1)		1.5		
			T_A = –55°C to 210°C (2)		1.5		
i_n	Input Noise Current Density	f = 10 Hz	T_A = 25°C		100		fA/√Hz
INPUT VOLTAGE RANGE (3)							
V_{CM}	Common mode voltage range	T_A = –55°C to 125°C		(V–) – 0.1		(V+) + 0.1	V
		T_A = –55°C to 175°C		(V–) – 0.25		(V+) + 0.25	
		T_A = –55°C to 210°C		(V–) – 0.25		(V+) + 0.25	
CMRR	Common-Mode Rejection Ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	T_A = –55°C to 125°C	102	130		dB
			T_A = –55°C to 175°C		101		
			T_A = –55°C to 210°C		91		
INPUT CAPACITANCE							
	Differential	T_A = –55°C to 125°C			2		pF
		T_A = –55°C to 175°C			4.25		
		T_A = –55°C to 210°C			4.25		
	Common mode	T_A = –55°C to 125°C			4		pF
		T_A = –55°C to 175°C			12.25		
		T_A = –55°C to 210°C			12.25		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ	T_A = –55°C to 125°C	104	130		dB
			T_A = –55°C to 175°C (1)	93	110		
			T_A = –55°C to 210°C (2)	85	93		

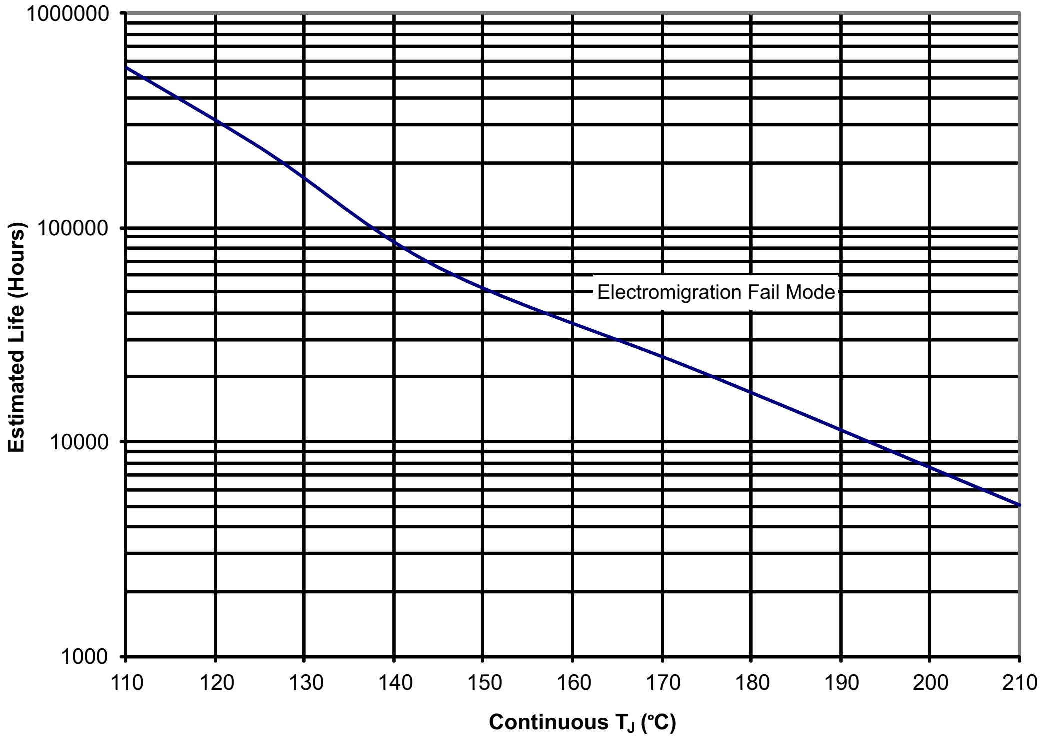
(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) The OPA2333-HT is not intended to be used as a comparator due to its limited differential input range capability.

Electrical Characteristics (continued)

V_S = 1.8 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF	T_A = –55°C to 125°C		350		kHz
			T_A = –55°C to 175°C		350		
			T_A = –55°C to 210°C		350		
SR	Slew rate	G = 1	T_A = –55°C to 125°C		0.16		V/μs
			T_A = –55°C to 175°C		0.25		
			T_A = –55°C to 210°C		0.25		
OUTPUT							
	Voltage output swing from rail	R_L = 10 kΩ	T_A = 25°C		30	50	mV
			T_A = –55°C to 125°C			85	
			T_A = –55°C to 175°C (1)			110	
			T_A = –55°C to 210°C (2)			150	
ISC	Short-circuit current	T_A = 25°C			±5		mA
	Open-loop output impedance (4)	f = 350 kHz, I_O = 0			2		kΩ
POWER SUPPLY							
V_S	Specified voltage range	T_A = –55°C to 210°C (2)		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0	T_A = 25°C		17	25	μA
			T_A = –55°C to 125°C			30	
			T_A = –55°C to 175°C (1)		35	40	
			T_A = –55°C to 210°C (2)		50	80	
	Turnon time	V_S = 5 V	T_A = 25°C		100		μs

(4) See *Typical Characteristics*.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) This device is qualified for 1000 hours of continuous operation at maximum rated temperature.

Figure 1. OPA2333SKGD1 and OPA2333HD Operating Life Derating Chart

6.6 Typical Characteristics

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted).

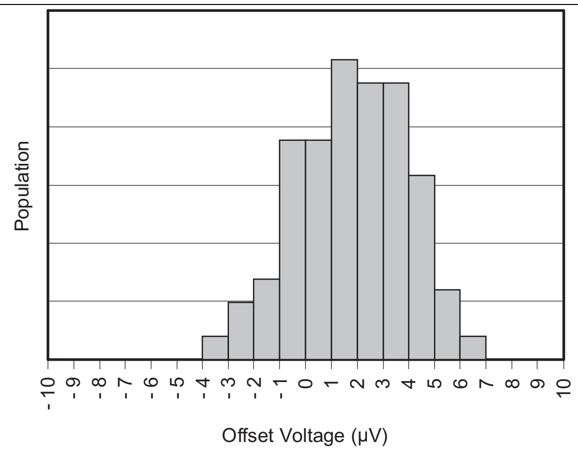


Figure 2. Offset Voltage Production Distribution

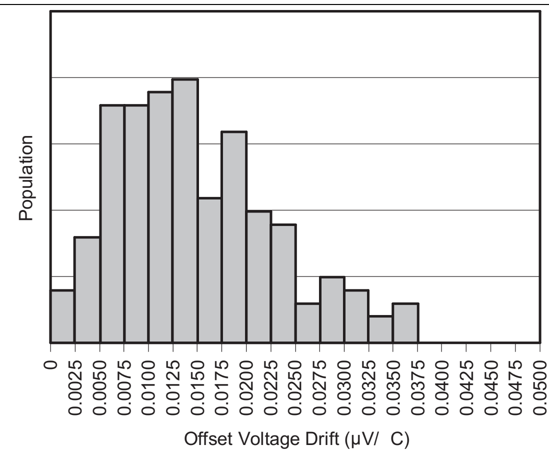


Figure 3. Offset Voltage Drift Production Distribution

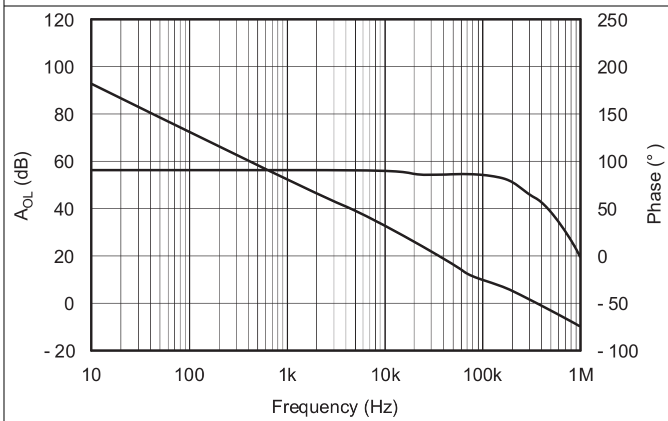


Figure 4. Open−Loop Gain vs Frequency

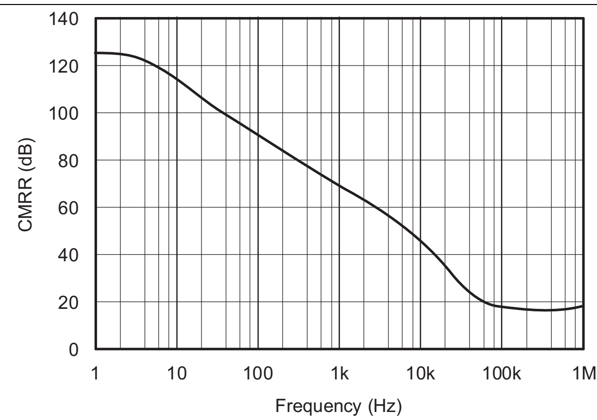


Figure 5. CMMR vs Frequency

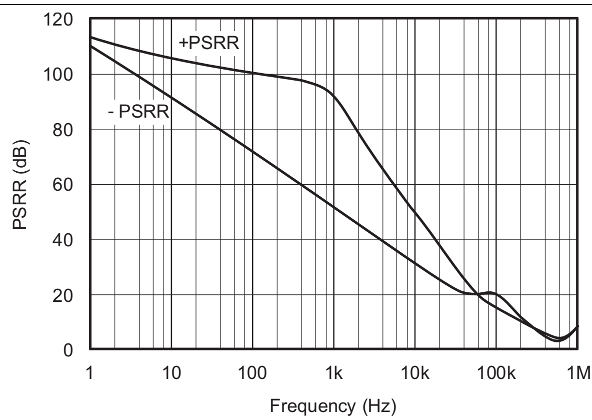


Figure 6. PSRR vs Frequency

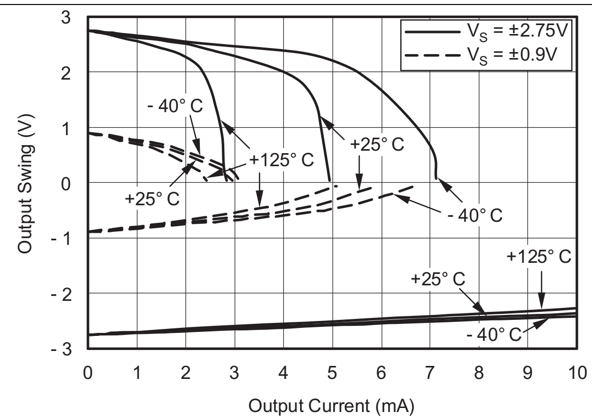


Figure 7. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

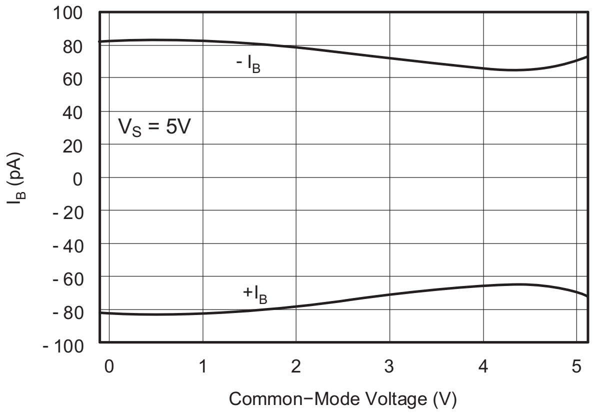


Figure 8. Input Bias Current vs Common−Mode Voltage

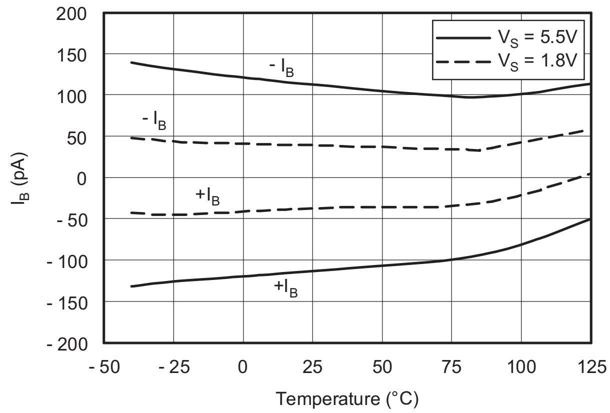


Figure 9. Input Bias Current vs Temperature

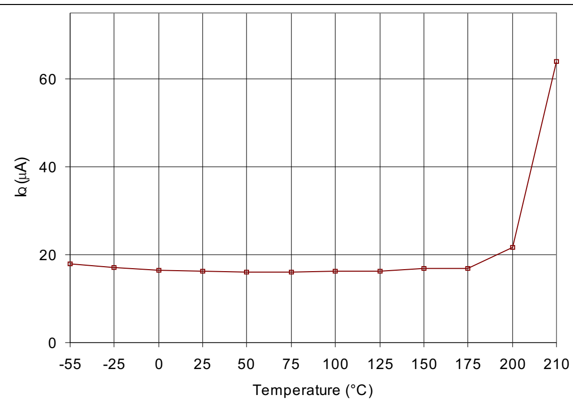


Figure 10. Quiescent Current vs Temperature

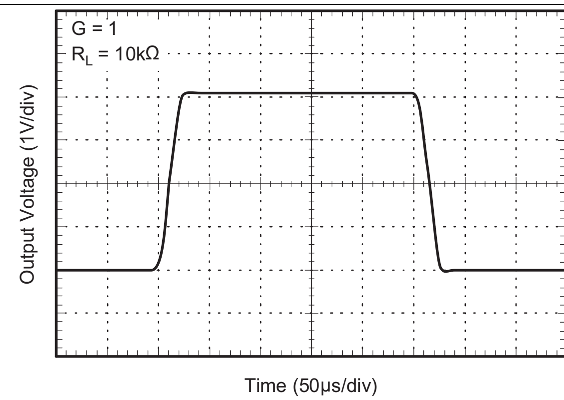


Figure 11. Large−Signal Step Response

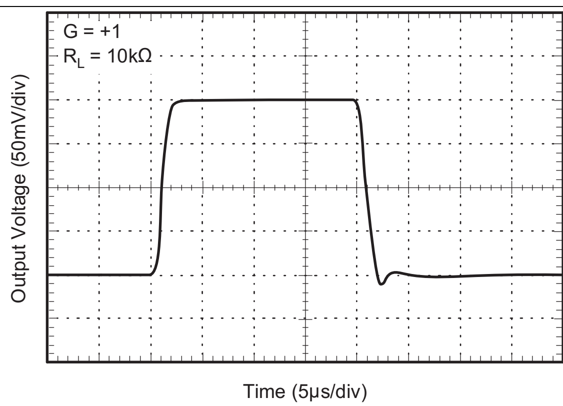


Figure 12. Small−Signal Step Response

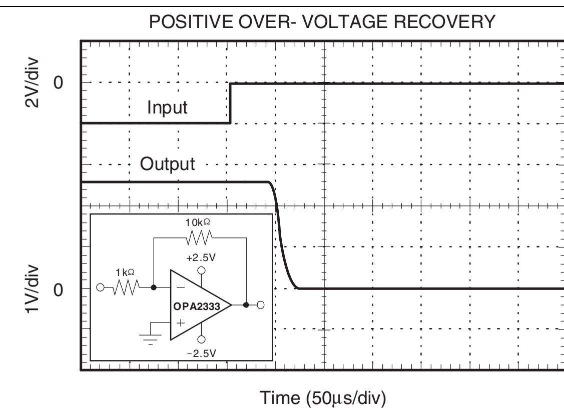


Figure 13. Positive Overvoltage Recovery

Typical Characteristics (continued)

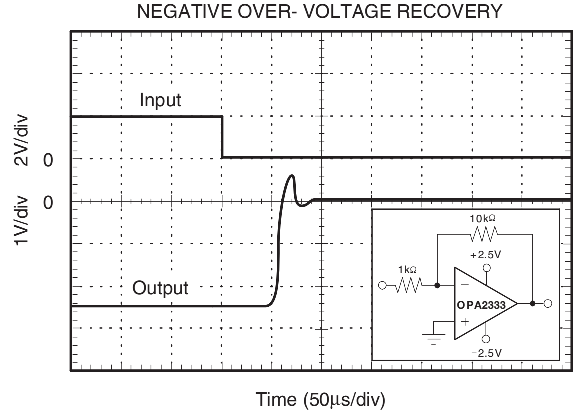


Figure 14. Negative Overvoltage Recovery

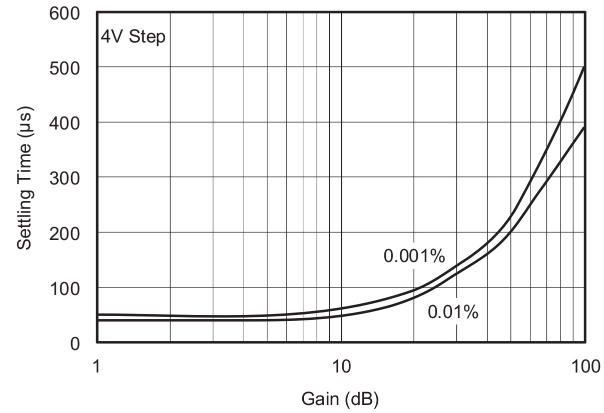


Figure 15. Settling Time vs Closed−Loop Gain

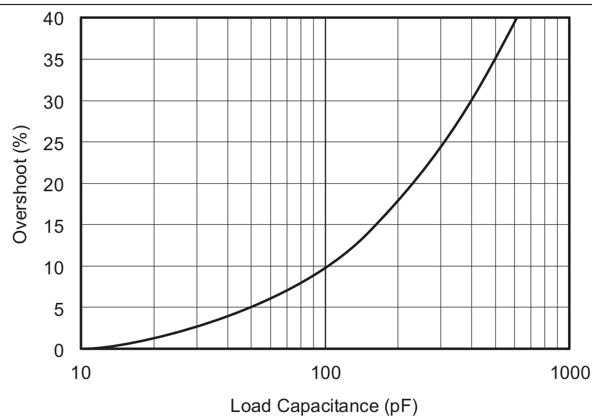


Figure 16. Small−Signal Overshoot vs Load Capacitance

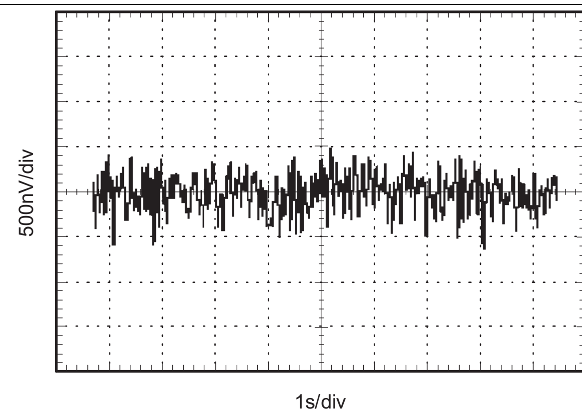


Figure 17. 0.1-Hz to 10-Hz Noise

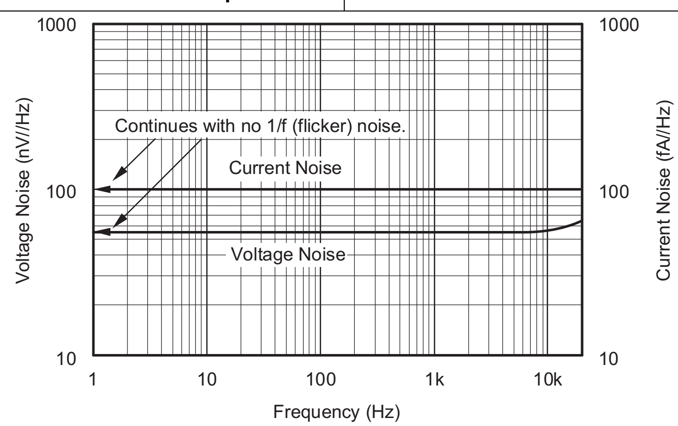


Figure 18. Current and Voltage Noise Spectral Density vs Frequency

7 Detailed Description

7.1 Overview

The OPA2333 is a Zero-Drift, low-power, rail-to-rail input and output dual operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The Zero-Drift architecture provides low offset voltage and near zero offset voltage drift.

7.2 Functional Block Diagrams

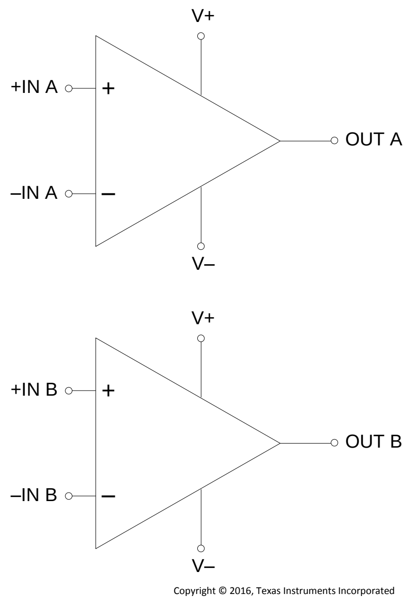


Figure 19. Functional Block Diagram for A and B Amps

7.3 Feature Description

The OPA2333 is unity-gain stable and free from unexpected output phase reversal. It uses a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include: [5]

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield operational amplifier and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on materials used.

7.3.1 Operating Voltage

The OPA2333 operational amplifier operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in *Typical Characteristics*.

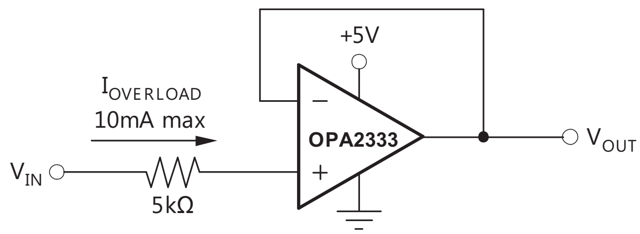
(5) At T_A = 25°C (unless otherwise noted).

Feature Description (continued)

7.3.2 Input Voltage

The OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA2333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor (see Figure 20).



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Current-limiting resistor required if input voltage exceeds supply rails by ≥ 0.5 V

Figure 20. Input Current Protection

7.3.3 Internal Offset Correction

The OPA2333 operational amplifier uses an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 Achieving Output Swing to the Operational Amplifier Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good single-supply operational amplifier may swing close to single-supply ground, but will not reach ground. The output of the OPA2333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the operational amplifier negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 21).

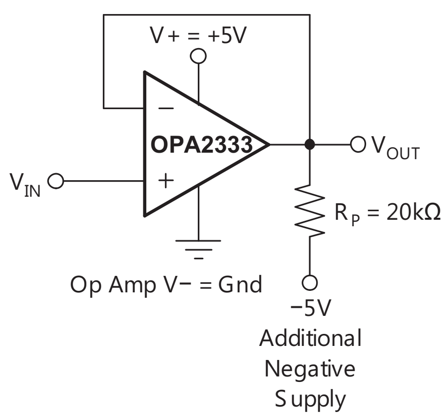

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Figure 21. V_{OUT} Range to Ground

Feature Description (continued)

The OPA2333 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA2333 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ.

NOTE

This configuration will increase the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

7.4 Device Functional Modes

The OPA2333 device has a single functional mode. The device is powered on as long as the power supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2333 family is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 22 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2333 facilitate excellent dc accuracy for the circuit.

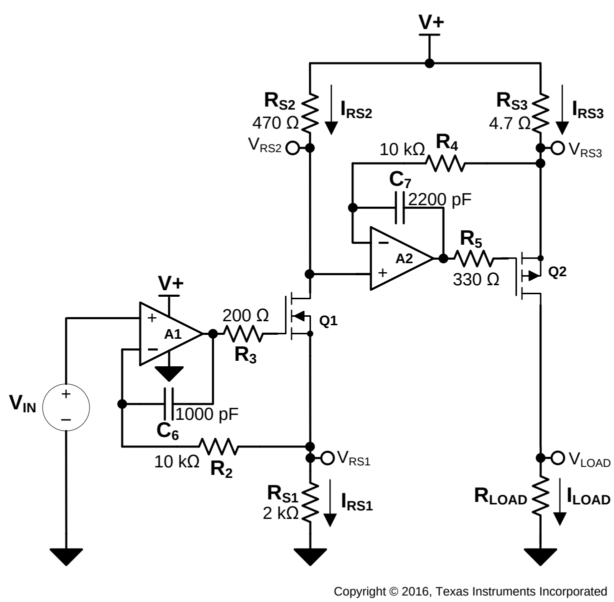


Figure 22. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5-V DC
- Input: 0-V to 2-V DC
- Output: 0-mA to 10-mA DC

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the DC characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333 CMOS operational amplifier is a high-precision, 5-µV offset, 0.05-µV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise DC control. The rail-to-rail output stage of the OPA2333 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

See TIPD102 for a detailed error analysis, design procedure, and additional measured results.

8.2.1.3 Application Curve

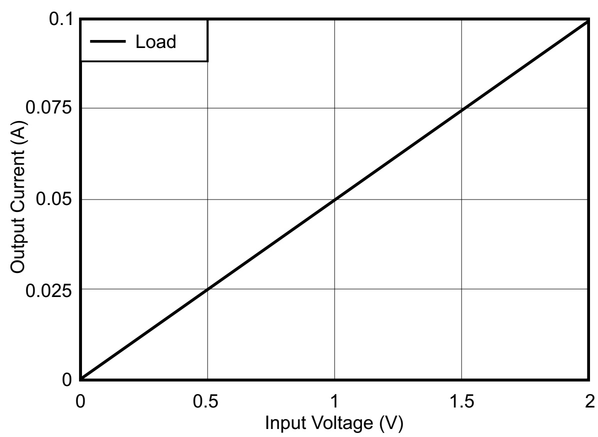


Figure 23. Measured Transfer Function for High-Side V-I Converter

Typical Applications (continued)

8.2.2 Precision, Low-Level Voltage-to-Current (V-I) Converter

The circuit shown in Figure 24 is a precision, low-level voltage-to-current (V-I) converter. The converter translates in input voltage of 0 V to 5 V and output current of 0 µA to 5 µA. Figure 25 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2333 facilitate excellent dc accuracy for the circuit. Figure 26 shows the calibrated error for the entire range of the circuit.

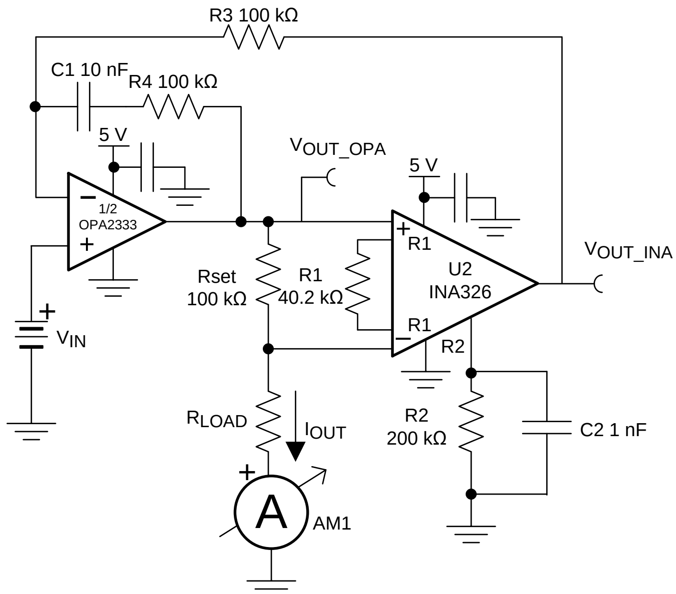


Figure 24. Low-Level, Precision V-I Converter

8.2.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5-V DC
- Input: 0-V to 5-V DC
- Output: 0-µA to 5-µA DC

8.2.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, R_{SET}, and the instrumentation amplifier (INA) gain. During operation, the input voltage divided by the INA gain appears across the set resistor in Equation 1:

$$V_{SET} = V_{IN}/G_{INA} \tag{1}$$

The current through R_{SET} must flow through the load, so I_{OUT} is V_{SET} / R_{SET}. I_{OUT} remains a well-regulated current as long as the total voltage across R_{SET} and R_{LOAD} does not violate the output limits of the operational amplifier or the input common-mode limits of the INA. The voltage across the set resistor (V_{SET}) is the input voltage divided by the INA gain (that is, V_{SET} = 1 V / 10 = 0.1 V). The current is determined by V_{SET} and R_{SET} shown in Equation 2:

$$I_{OUT} = V_{SET} / R_{SET} = 0.1\ \text{V} / 100\ \text{k}\Omega = 1\ \mu\text{A} \tag{2}$$

See TIPD107 for a detailed error analysis, design procedure, and additional measured results.

Typical Applications (continued)

8.2.2.3 Application Curves

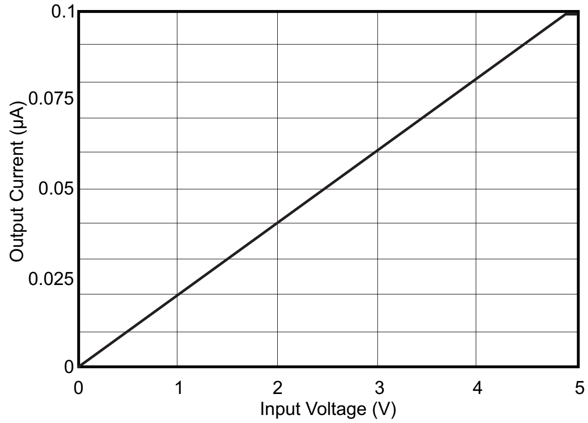


Figure 25. Measured Transfer Function for Low-Level Precision V-I

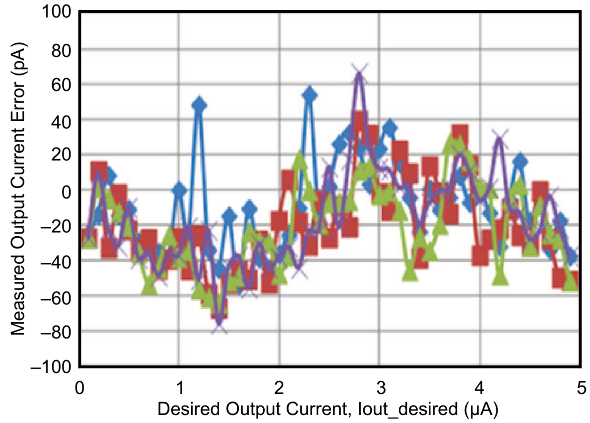


Figure 26. Calibrated Output Error for Low-Level V-I

8.2.3 Composite Amplifier

The circuit shown in Figure 27 is a composite amplifier used to drive the reference on the ADS8881. The OPA2333 provides excellent dc accuracy, and the THS4281 allows the output of the circuit to respond quickly to the transient current requirements of a typical SAR data converter reference input. The ADS8881 system was optimized for THD and achieved a measured performance of –110 dB. The linearity of the ADC is shown Figure 28.

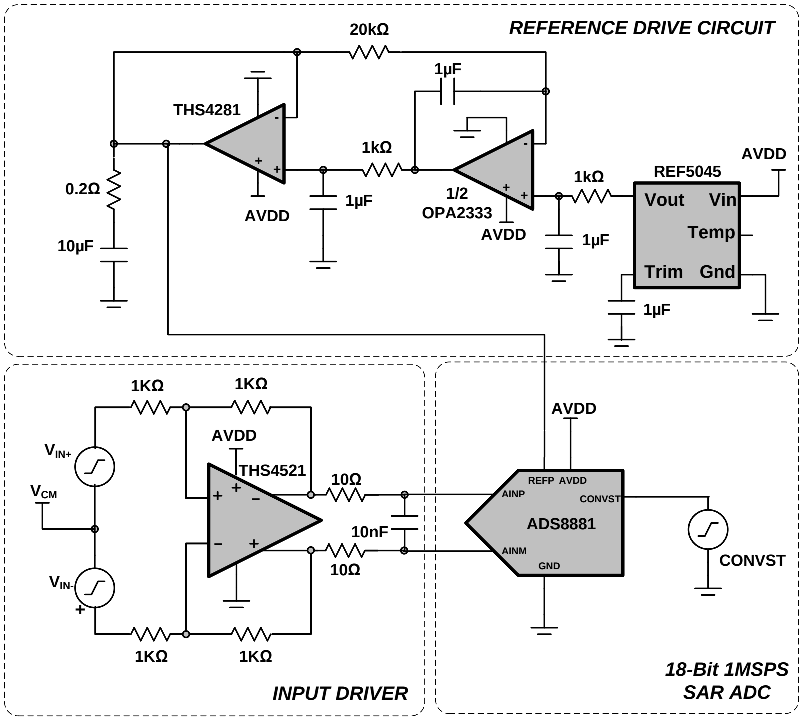


Figure 27. Composite Amplifier Reference Driver Circuit

Typical Applications (continued)

8.2.3.1 Design Requirements

The design requirements for this block design are:

- System Supply Voltage: 5-V DC
- ADC Supply Voltage: 3.3-V DC
- ADC Sampling Rate: 1 MSPS
- ADC Reference Voltage (VREF): 4.5-V DC
- ADC Input Signal: A differential input signal with amplitude of V_{pk} = 4.315 V (–0.4 dBFS to avoid clipping) and frequency, f_{IN} = 10 kHz are applied to each differential input of the ADC

8.2.3.2 Detailed Design Procedure

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver design. The circuit comprises the critical analog circuit blocks, the input driver, anti-aliasing filter, and the reference driver. Each analog circuit block should be carefully designed based on the ADC performance specifications in order to maximize the distortion and noise performance of the data acquisition system while consuming low power. The diagram includes the most important specifications for each individual analog block. This design systematically approaches the design of each analog circuit block to achieve a 16-bit, low-noise and low-distortion data acquisition system for a 10-kHz sinusoidal input signal. The first step in the design requires an understanding of the requirement of extremely low distortion input driver amplifier. This understanding helps in the decision of an appropriate input driver configuration and selection of an input amplifier to meet the system requirements. The next important step is the design of the anti-aliasing RC-filter to attenuate ADC kick-back noise while maintaining the amplifier stability. The final design challenge is to design a high-precision reference driver circuit, which would provide the required value VREF with low offset, drift, and noise contributions.

In designing a very low distortion data acquisition block, it is important to understand the sources of nonlinearity. Both the ADC and the input driver introduce nonlinearity in a data acquisition block. To achieve the lowest distortion, the input driver for a high-performance SAR ADC must have a distortion that is negligible against the ADC distortion. This parameter requires the input driver distortion to be 10 dB lower than the ADC THD. This stringent requirement ensures that overall THD of the system is not degraded by more than –0.5 dB.

$$THD_{AMP} < THD_{ADC} - 10\ dB \quad (3)$$

It is therefore important to choose an amplifier that meets the above criteria to avoid the system THD from being limited by the input driver. The amplifier nonlinearity in a feedback system depends on the available loop gain. See TIPD115 for a detailed error analysis, design procedure, and additional measured results.

8.2.3.3 Application Curve

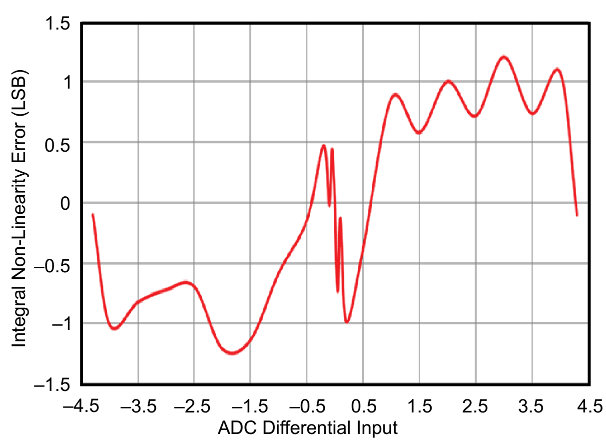


Figure 28. Linearity of the ADC8881 System

8.3 System Examples

8.3.1 Temperature Measurement Application

Figure 29 shows a temperature measurement application.

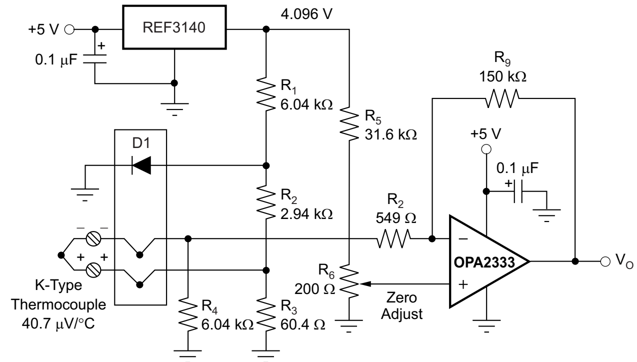


Figure 29. Temperature Measurementf

8.3.2 Single Operational Amplifier Bridge Amplifier Application

Figure 30 shows the basic configuration for a bridge amplifier.

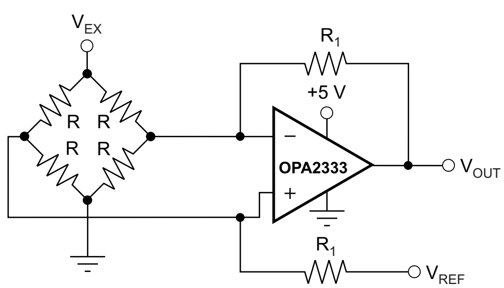
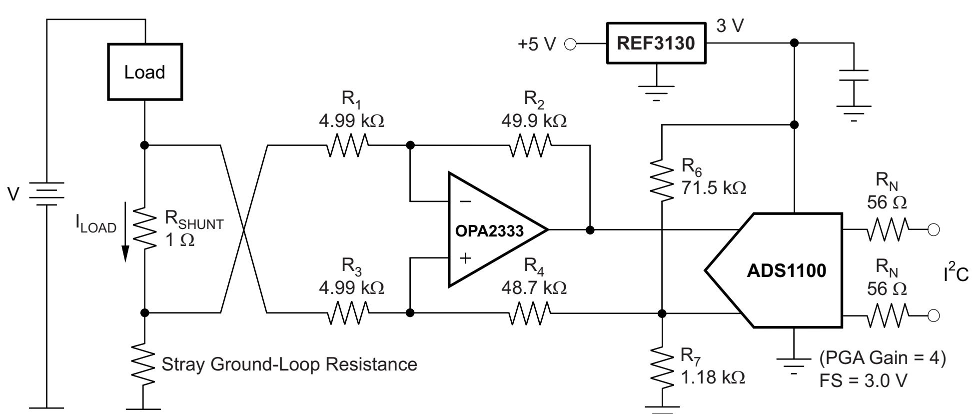


Figure 30. Single Operational Amplifier Bridge Amplifier

8.3.3 Low-Side Current Monitor Application

A low-side current shunt monitor is shown in Figure 31. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

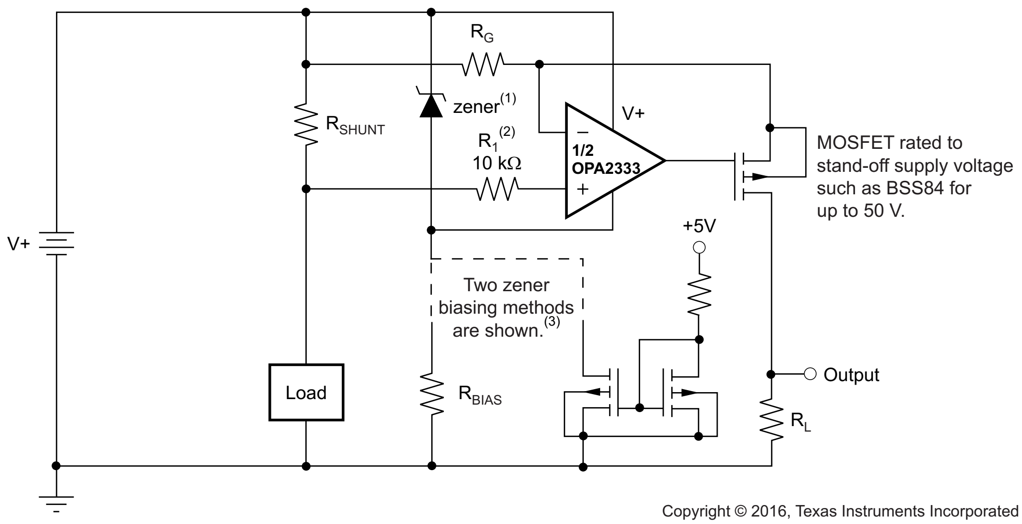


NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 31. Low-Side Current Monitor

8.3.4 Other Applications

Additional application ideas are shown in Figure 32 through Figure 35.



(1) Zener rated for operational amplifier supply capability (that is, 5.1 V for OPA2333).
(2) Current-limiting resistor.
(3) Choose zener biasing resistor or dual N-MOSFETs (FDG6301N, NTJD4001N, or Si1034).

Figure 32. High-Side Current Monitor

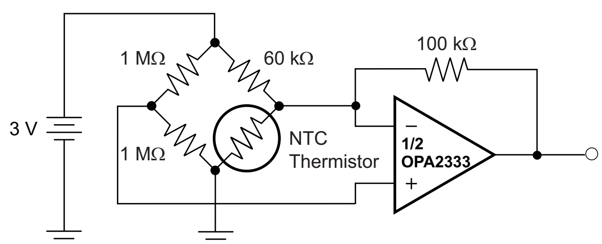


Figure 33. Thermistor Measurement

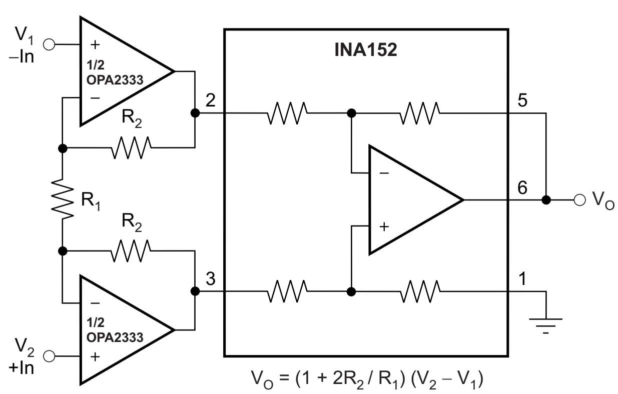
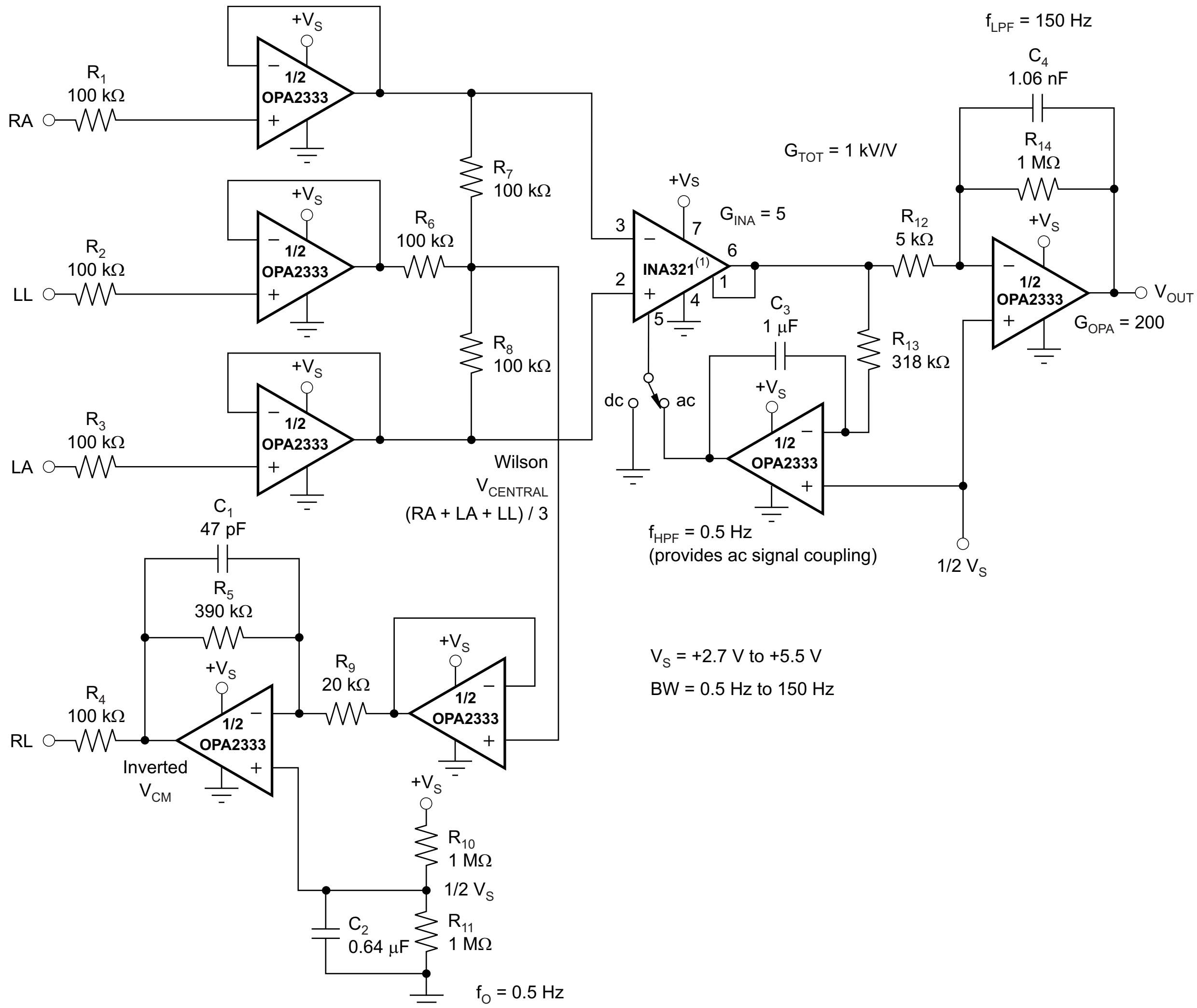


Figure 34. Precision Instrumentation Amplifier



(1) Other instrumentation amplifiers can be used, such as the INA326, which has lower noise, but higher quiescent current.

Figure 35. Single-Supply, Very Low Power, ECG Circuit

9 Power Supply Recommendations

The OPA2333 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Recommended Operating Conditions* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

10.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA2333 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

10.1.2 DFN Layout Guidelines

Solder the exposed leadframe die pad on the DFN package to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example

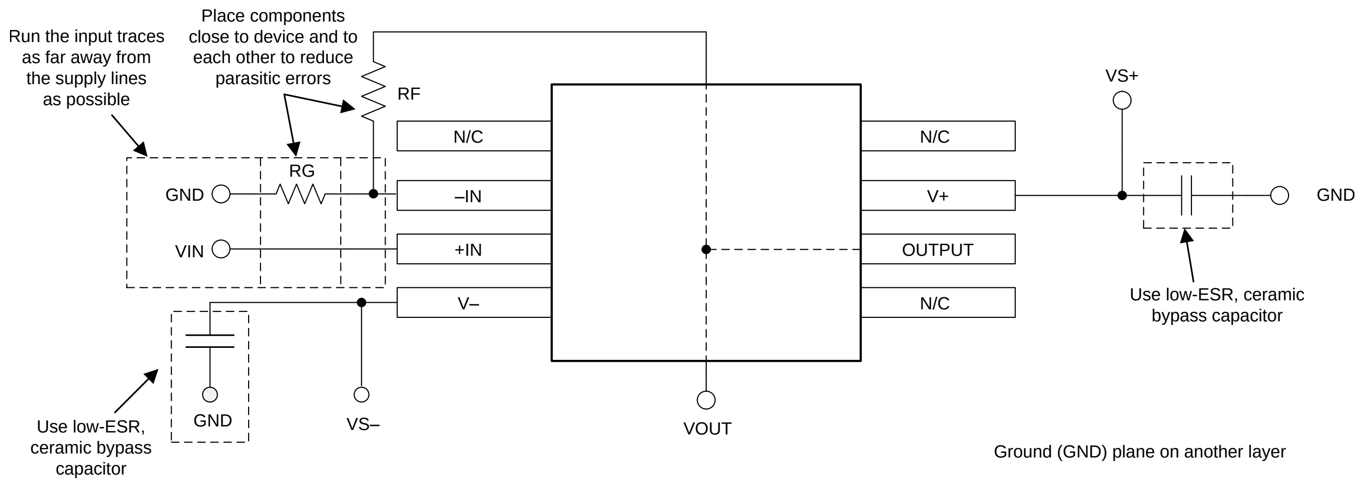


Figure 36. OPA2333-HT Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support on this product, see the following:

- *High-Side V-I Converter, 0 V to 2 V to 0 mA to 100 mA, 1% Full-Scale Error,* TIPD102
- *Low-Level V-to-I Converter Reference Design, 0-V to 5-V Input to 0-µA to 5-µA Output,* TIPD107
- *18-Bit, 1-MSPS, Serial Interface, microPower, Truly-Differential Input, SAR ADC,* ADS8881
- *Very Low-Power, High-Speed, Rail-To-Rail Input/Output, Voltage Feedback Operational Amplifier,* THS4281
- *Data Acquisition Optimized for Lowest Distortion, Lowest Noise, 18-bit, 1-MSPS Reference Design,* TIPD115
- *Self-Calibrating, 16-Bit Analog-to-Digital Converter,* ADS1100
- *20-ppm/Degrees C Max, 100-µA, SOT23-3 Series Voltage Reference,* REF3130
- *Precision, Low Drift, CMOS Instrumentation Amplifier, INA326,* INA326

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2333HD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-55 to 175	O2333H	Samples
OPA2333SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	OPA2333S HKJ	Samples
OPA2333SHKQ	ACTIVE	CFP	HKQ	8	1	TBD	AU	N / A for Pkg Type	-55 to 210	OPA2333S HKQ	Samples
OPA2333SJD	ACTIVE	CDIP SB	JD	8	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 210	OPA2333SJD	Samples
OPA2333SKGD1	ACTIVE	XCEPT	KGD	0	100	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2333-HT :

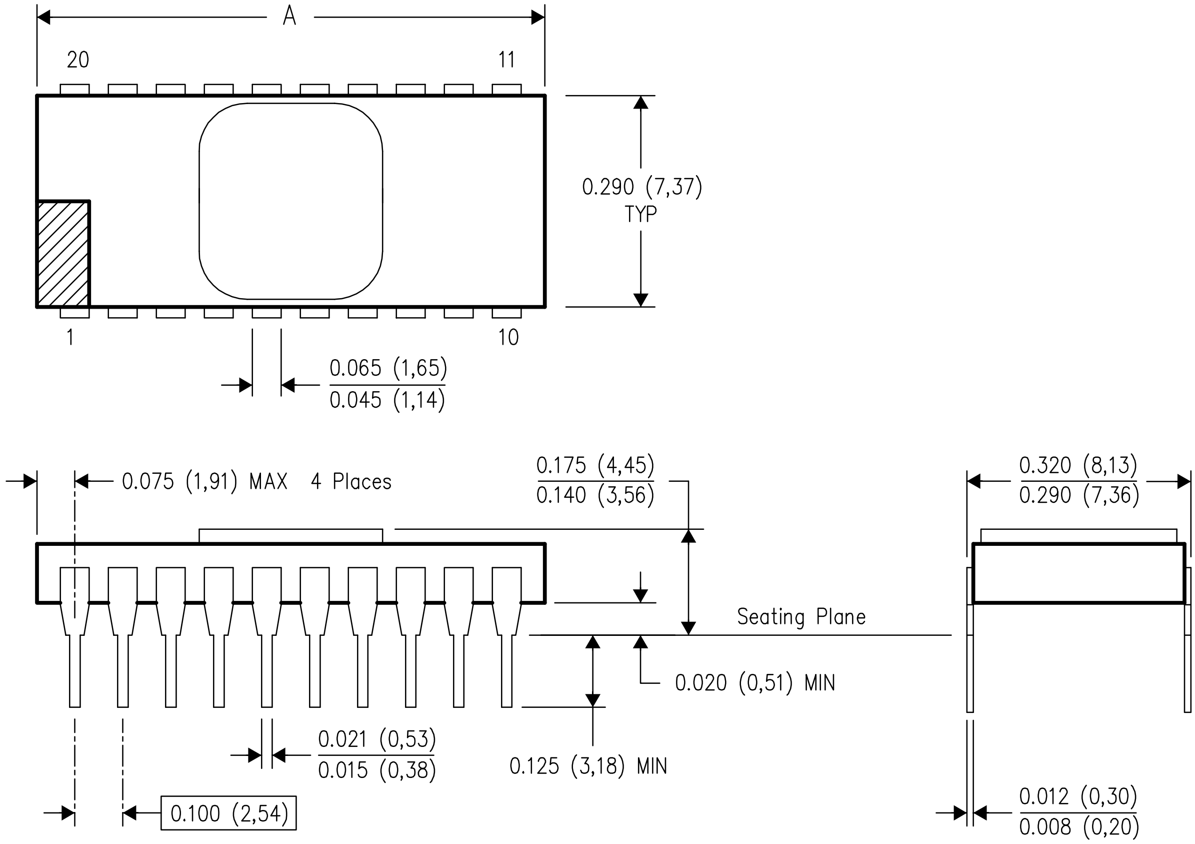
- Catalog: OPA2333
- Automotive: OPA2333-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN

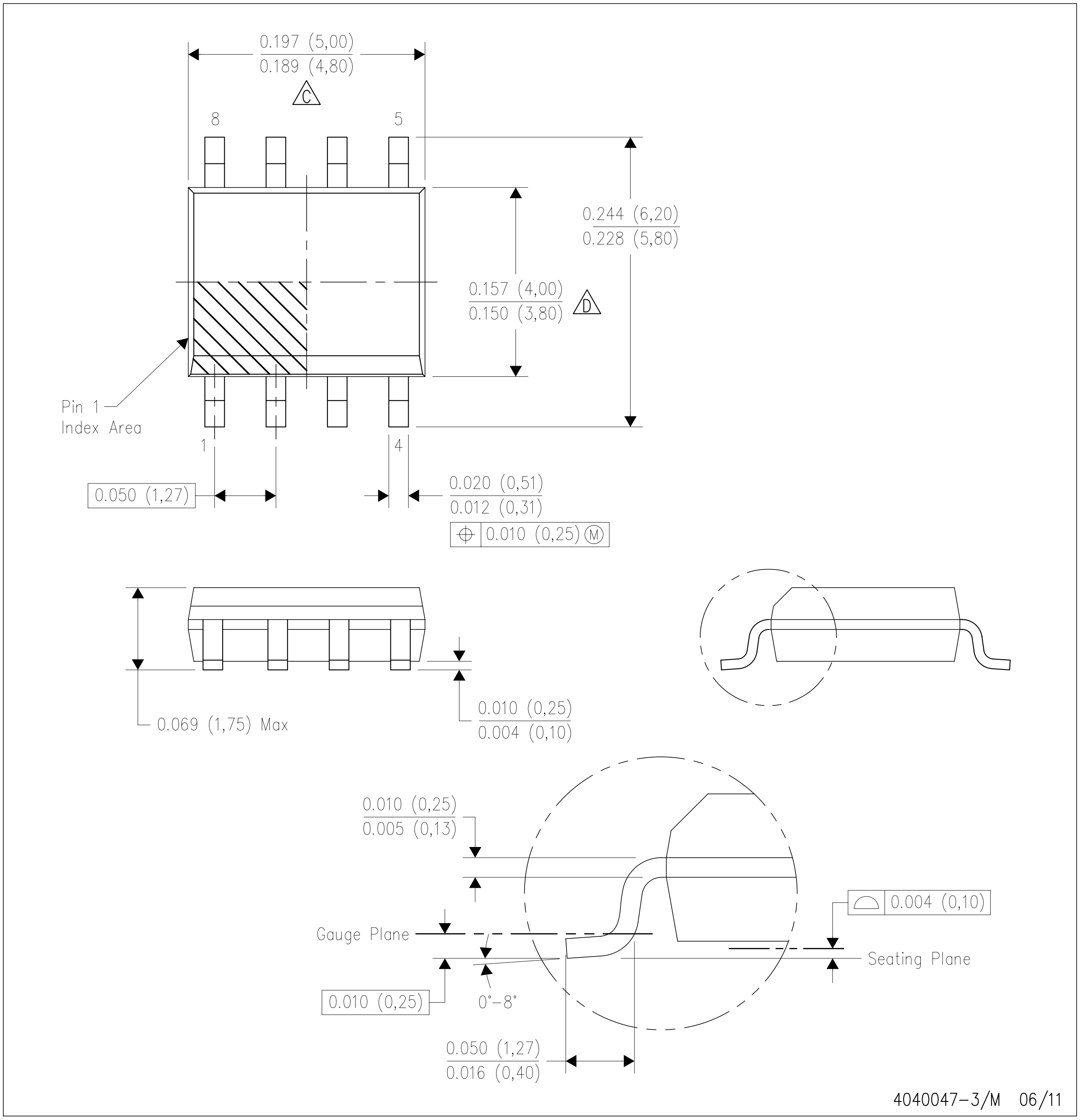


DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

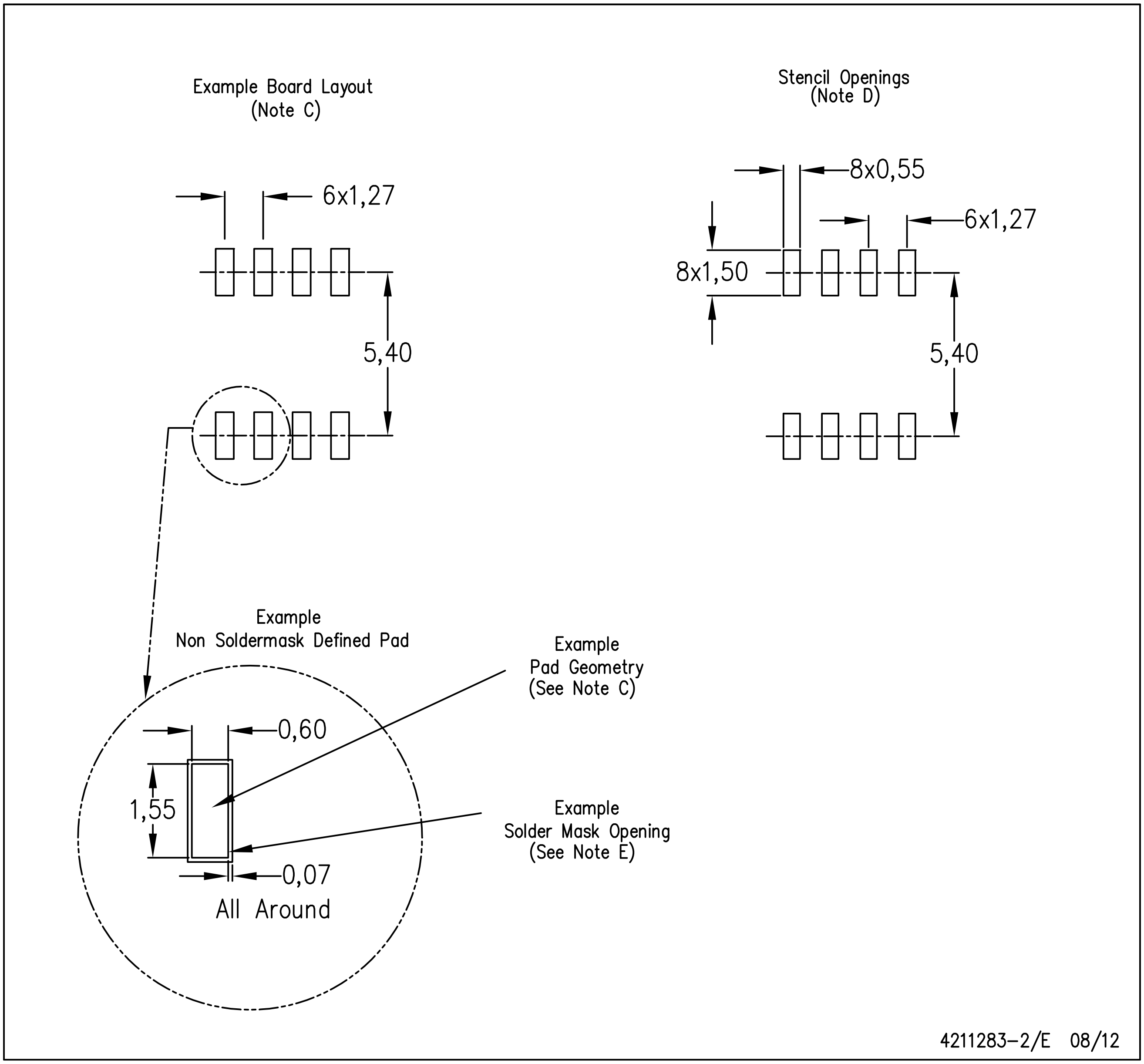
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



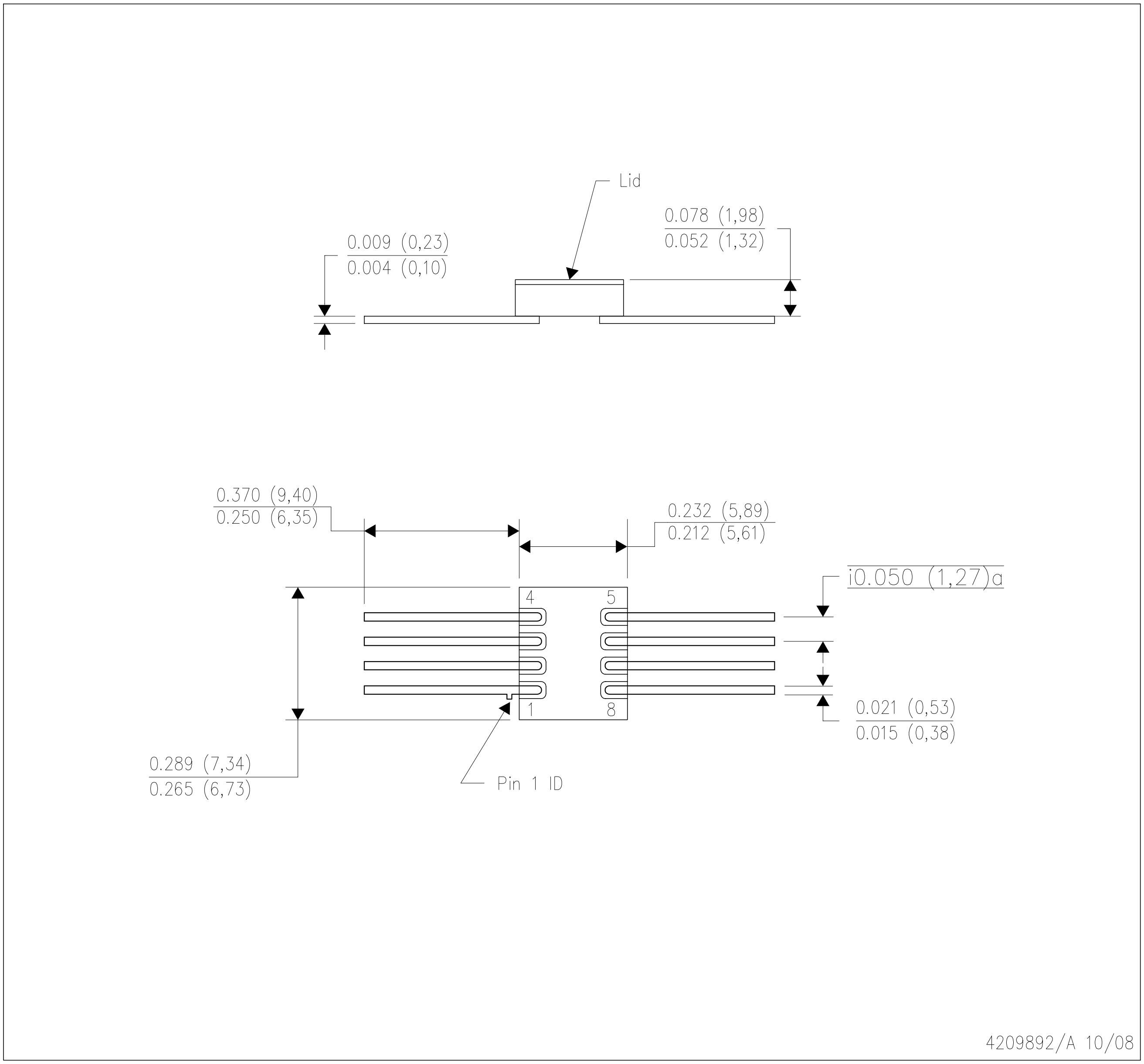
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



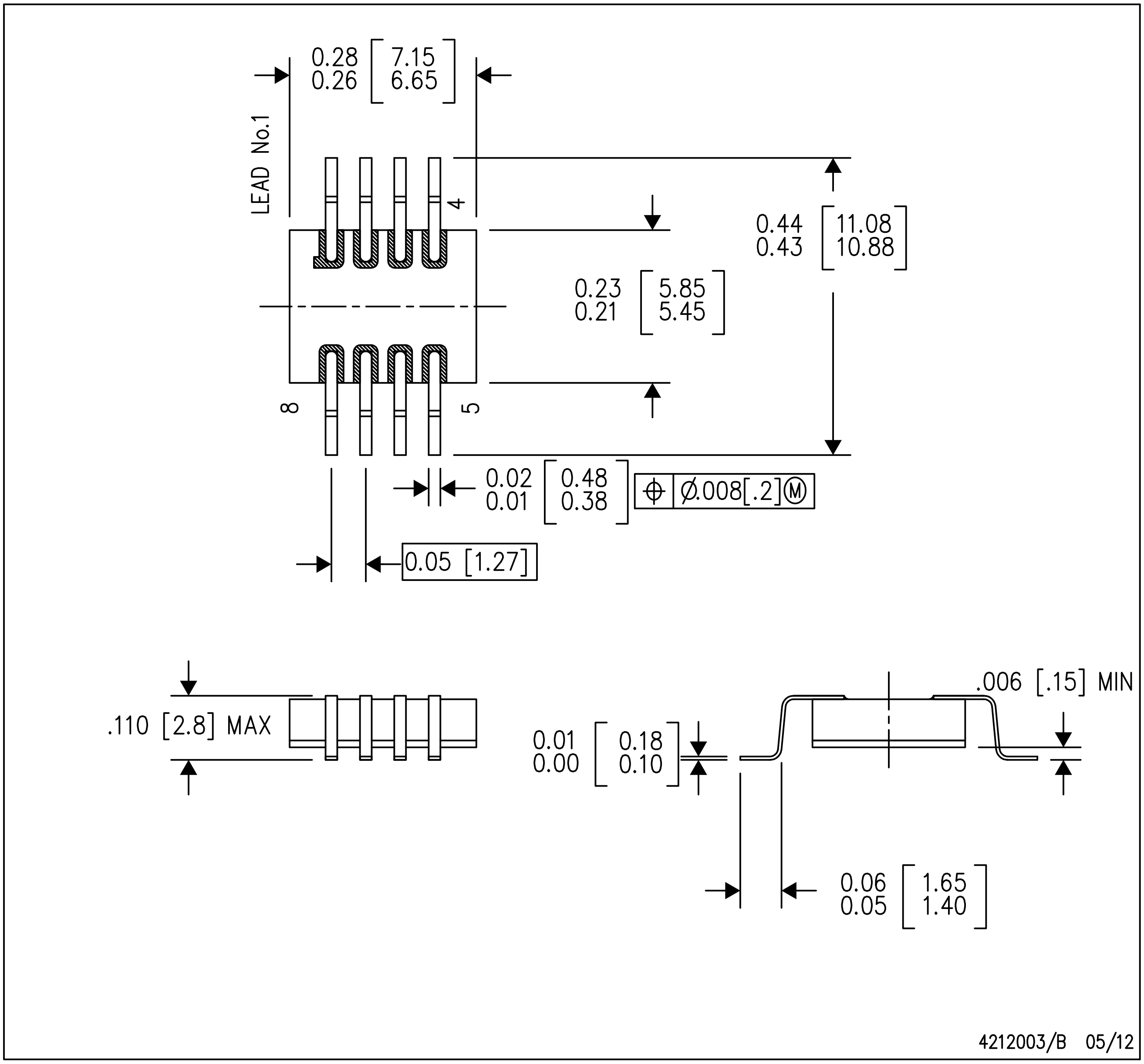
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

HKJ (R—CDFP—F8) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

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