2.3V 至 20V，750mA 低压降电压稳压器

查询样片: TPS7A4501-SP

特性

- 符合 **QMLV**，**SMD 5962-12224**
- 针对快速瞬态响应进行了优化
- 输出电流：**750mA**
- 高输出电压精度：在 **25°C** 时为 **1%**（典型值）
- 压降电压：**300mV**
- 低噪声：**Vout = 5V** 时为 **50μV_{RMS}**（**10Hz** 至 **100kHz**）
- 高纹波抑制：**1KHz** 时为 **68dB**
- **1mA** 静态电流
- 无需保护二极管
- 压降中的受控静态电流
- **2.3V** 到 **20V** 的宽输入电压 **(Vin)**
- **1.21V** 至 **20V** 的可调节输出范围
- 关断时静态电流小于 **1μA**
- 与陶瓷输出电容器一起工作时保持稳定
- 反向电池保护
- 反向电流保护

应用范围

- **TPS7A4501-SP:** 抗辐射应用
- 射频 **(RF)** 组件压控稳压器 **(VCO)**，接收器，模数转换器 **(ADC)**，放大器
- 时钟分配
- 洁净模拟电源需求
- **TPS7A4501-SP** 在军用温度范围（**-55°C** 至 **125°C**）内可用
- 可提供工程评估 **(/EM)** 样品 (1)

(1) 这些部件只用于工程评估。 它们的加工工艺为非兼容流程（例如，无预烧过程等）并且只在 25°C 的温度额定值下测试。 这些部件不适合于品质检定、生产、辐射测试或飞行使用。 不担保在整个军用额定温度范围（ -55°C 至 125°C ）内或使用寿命内的器件性能。

说明

TPS7A4501 是一款针对快速瞬态响应而进行优化的低压降 (LDO) 稳压器。 此器件在压降为 300mV 时可提供 750mA 的输出电流。 运行静态电流为 1mA，在关断时下降到少于 1μA。 静态电流受到很好的控制；与很多其他稳压器一同工作时一样，它在压降时不上升。 除了快速瞬态响应，TPS7A4501 稳压器具有极低的输出噪声，这使得它非常适合于灵敏 RF 电源应用。

输出电压范围为 1.21V 至 20V。 TPS7A4501 在使用低至 10μF 的输出电容器时保持稳定。 与其它稳压器一同使用时的常见情况一样，在无需额外等效串联电阻 (ESR) 的前提下可使用小型陶瓷电容器。 内部保护电路包括反向电池保护、电流限制、热限制和反向电流保护。 此器件可被用作一个基准电压为 1.21V 的可调器件。 TPS7A4501 稳压器采用 10 引脚 GDFP (U) 封装。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Floating	TiW/AlCu2	1627 nm

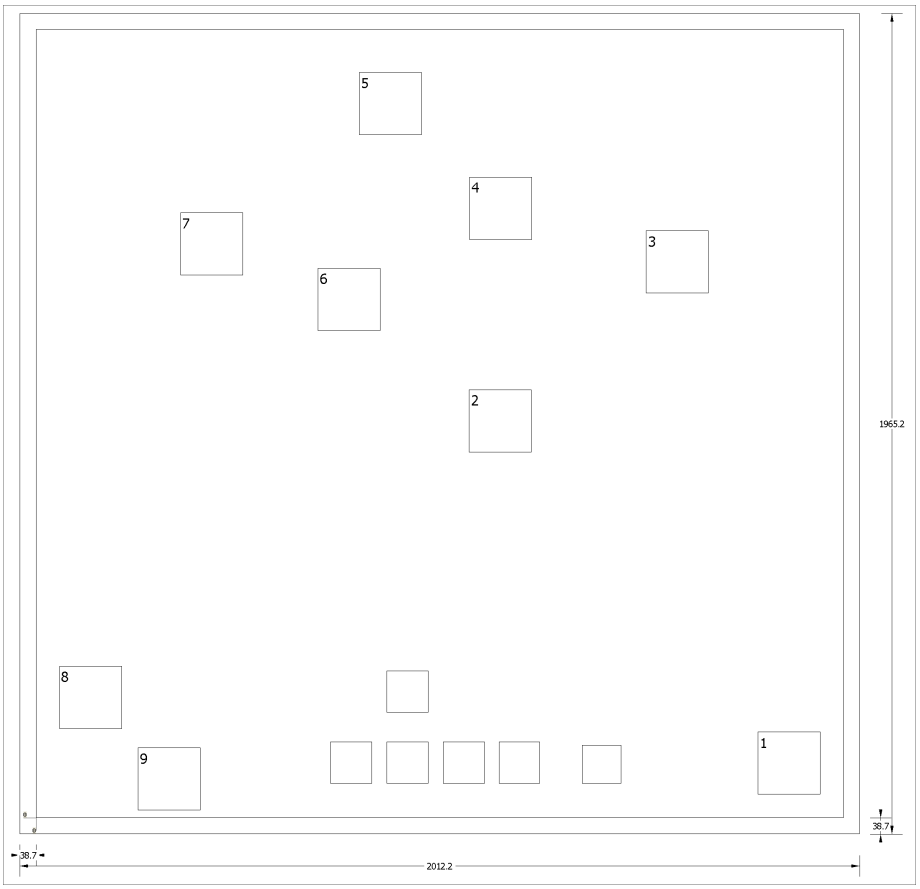


Table 1. Bond Pad Coordinates in Microns(1)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
$\overline{\text{SHDN}}$	1	1729.25	55.5	1879.25	205.5
IN	2	1037.25	875	1187.25	1025
IN	3	1460.75	1255.5	1610.75	1405.5
IN	4	1037.75	1384.5	1187.75	1534.5
OUT	5	774.25	1634.75	924.25	1784.75
OUT	6	675.25	1166	825.25	1316
OUT	7	345.5	1299.25	495.5	1449.25
SENSE/ADJ	8	55.5	213	205.5	363
GND	9	244	17.5	394	167.5

(1) Substrate is not to be connected.

ABSOLUTE MAXIMUM RATINGS(1)

over operating junction temperature range (unless otherwise noted)

Input voltage range, V_{IN}	IN	–22 V to 22 V
	OUT	–22 V to 22 V
	Input-to-output differential(2)	–22 V to 22 V
	ADJ	–7 V to 7 V
	$\overline{SHDN}$	–22 V to 22 V
Maximum lead temperature (10-s soldering time), T_{lead}		260°C
Maximum operating junction temperature, T_J		150°C
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 22 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT can not exceed ±22 V.

RECOMMENDED OPERATING CONDITIONS

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	-55		125	°C

THERMAL INFORMATION

THERMAL METRIC		TPS7A4501-SP U 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	86.6	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(2)	10.3	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)	35.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)	31.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)	53.5	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

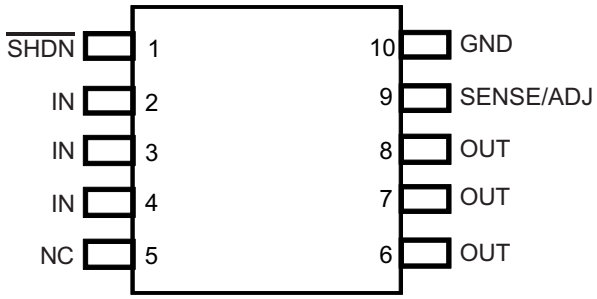
Over operating junction temperature range T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP(1)	MAX	UNIT
V_{IN}	Minimum input voltage(2) (3)	I_{LOAD} = 500 mA	25°C		1.9	2.3	V
		I_{LOAD} = 750 mA	Full range		2.1	2.5	
V_{ADJ}	ADJ pin voltage(2) (4)	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.196	1.21	1.224	V
		V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 750 mA	Full range	1.174	1.21	1.246	
	Line regulation(2)	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		1.5	4.5	mV
	Load regulation(2)	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 750 mA	25°C		2	8	mV
			Full range			18	
V_{DO}	Dropout voltage(5) (6) V_{OUT} = 2.4 V	I_{LOAD} = 1 mA	25°C		0.02	0.05	V
			Full range			0.07	
		I_{LOAD} = 100 mA	25°C		0.085	0.10	
			Full range			0.13	
		I_{LOAD} = 500 mA	25°C		0.17	0.21	
			Full range			0.27	
		I_{LOAD} = 750 mA	25°C		0.20	0.27	
			Full range			0.33	
I_{GND}	GND pin current(6) (7) V_{IN} = 2.5 V	I_{LOAD} = 0 mA	Full range		1	1.5	mA
		I_{LOAD} = 1 mA	Full range		1.1	1.6	
		I_{LOAD} = 100 mA	Full range		3.3	7	
		I_{LOAD} = 500 mA	Full range		15	30	
		I_{LOAD} = 750 mA	Full range		28	45	
e_N	Output voltage noise	C_{OUT} = 22 µF, I_{LOAD} = 750 mA, V_{IN} = 7 V, V_{OUT}= 5 V, B_W = 10 Hz to 100 kHz	25°C		50		μV_{RMS}
I_{ADJ}	ADJ pin bias current(2) (8)		25°C		3	7	µA
	Shutdown threshold	V_{OUT} = OFF to ON	Full range		0.9	2	V
		V_{OUT} = ON to OFF	Full range	0.15	0.75		
$I_{\overline{SHDN}}$	$\overline{SHDN}$ pin current	$V_{\overline{SHDN}}$ = 0 V	25°C		0.01	1	µA
		$V_{\overline{SHDN}}$ = 20 V	25°C		3	20	
	Quiescent current in shutdown	V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V	25°C		0.01	1	µA
	Ripple rejection(9)	$V_{IN} – V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A	25°C	60	68		dB
I_{LIMIT}	Current limit(9)	V_{IN} = 7 V, V_{OUT} = 0 V	25°C	1.7	1.9		A
		V_{IN} = 2.5 V	Full range	1.6	1.9		
I_{IL}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V	Full range			300	µA
I_{RO}	Reverse output current(10)	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	25°C		300	500	µA

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) The TPS7A4501 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
(3) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(4) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} – V_{DROPOUT}$.
(6) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-µA DC load on the output.
(7) GND pin current is tested with V_{IN} = 2.5 V and a current source load. The GND pin current decreases at higher input voltages.
(8) ADJ pin bias current flows into the ADJ pin.
(9) Specification is guaranteed by characterization for KGD and is not tested in production.
(10) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

DEVICE INFORMATION

U PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	$\overline{\text{SHDN}}$	Shutdown. $\overline{\text{SHDN}}$ is used to put the TPS7A4501 regulator into a low-power shutdown state. The output is off when $\overline{\text{SHDN}}$ is pulled low. $\overline{\text{SHDN}}$can be driven by 5-V logic, 3-V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and $\overline{\text{SHDN}}$ current, typically 3 µA. If unused, $\overline{\text{SHDN}}$ must be connected to V_{IN}. The device is in the low-power shutdown state if $\overline{\text{SHDN}}$ is not connected.
2, 3, 4	IN	Input. Power is supplied to the device through IN. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 µF to 10 µF is sufficient. The TPS7A4501 regulator is designed to withstand reverse voltages on IN with respect to ground and on OUT. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
5	NC	This pin is not connected to any internal circuitry. It can be left floating or tied to VIN or GND.
6, 7, 8	OUT	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
9	ADJ	Adjust. This is the input to the error amplifier. ADJ is internally clamped to ±7 V. It has a bias current of 3 µA that flows into the pin. ADJ voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
10	GND	Ground.

TYPICAL CHARACTERISTICS

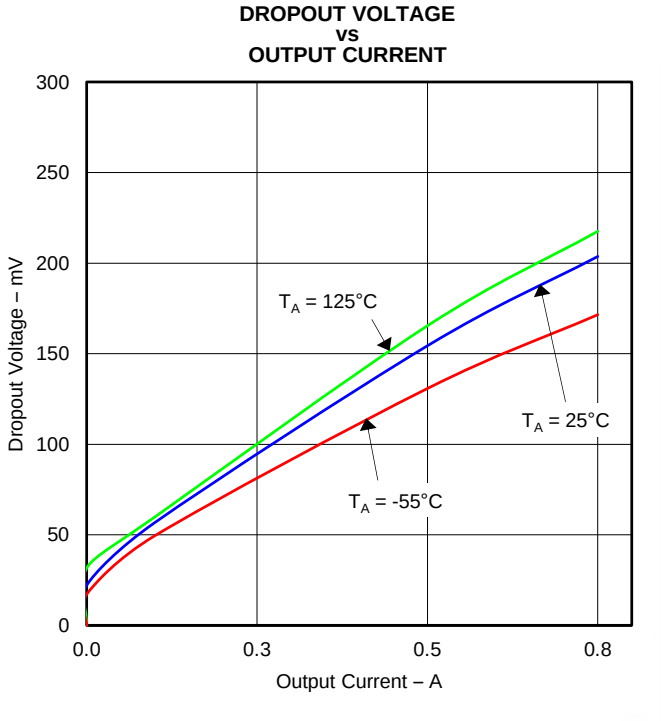


Figure 1.

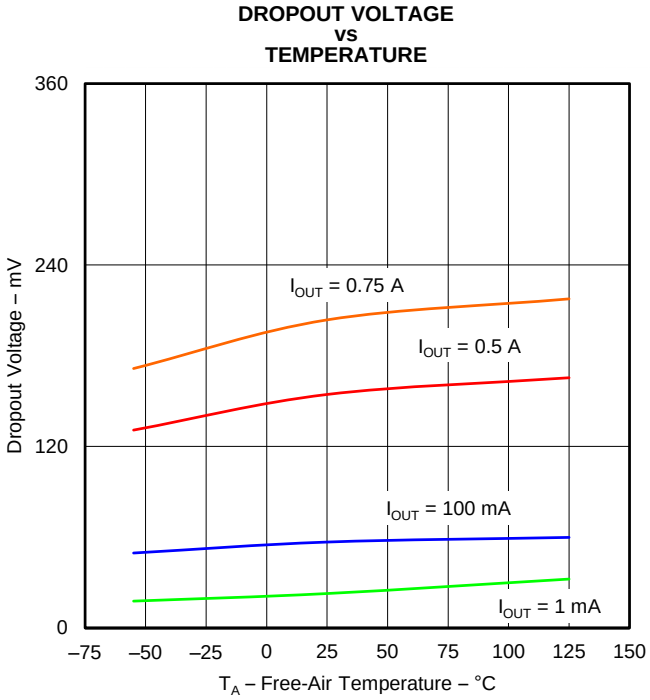


Figure 2.

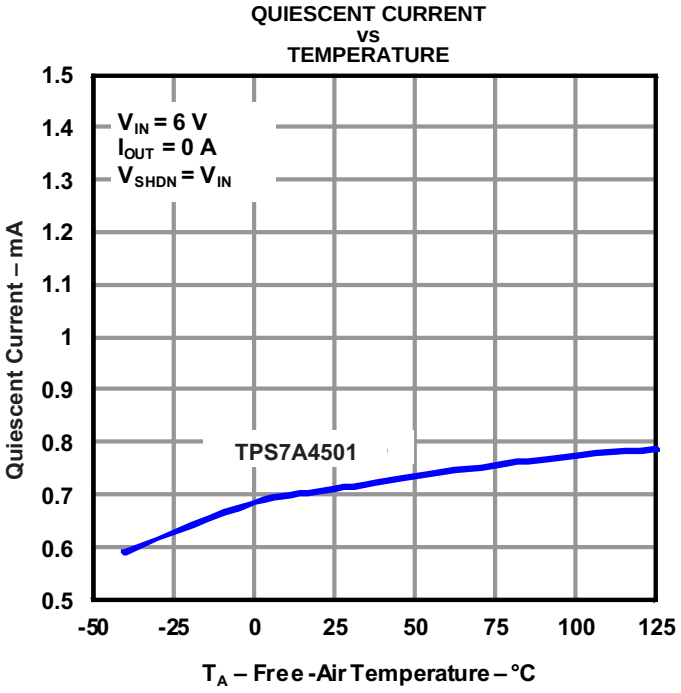


Figure 3.

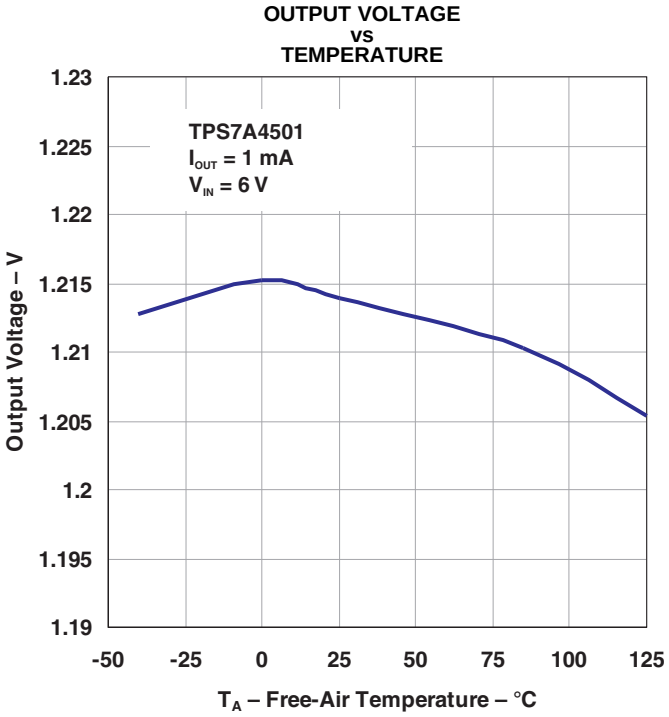


Figure 4.

TYPICAL CHARACTERISTICS (continued)

QUIESCENT CURRENT vs INPUT VOLTAGE

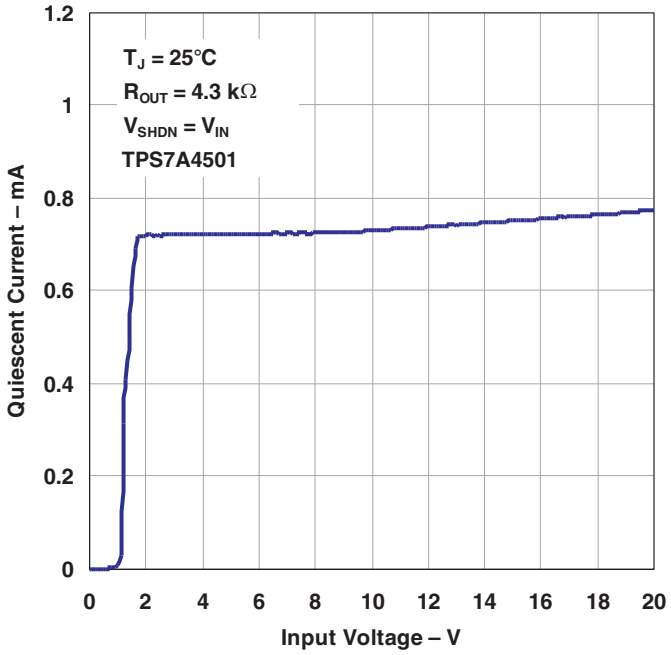


Figure 5.

GROUND CURRENT vs INPUT VOLTAGE

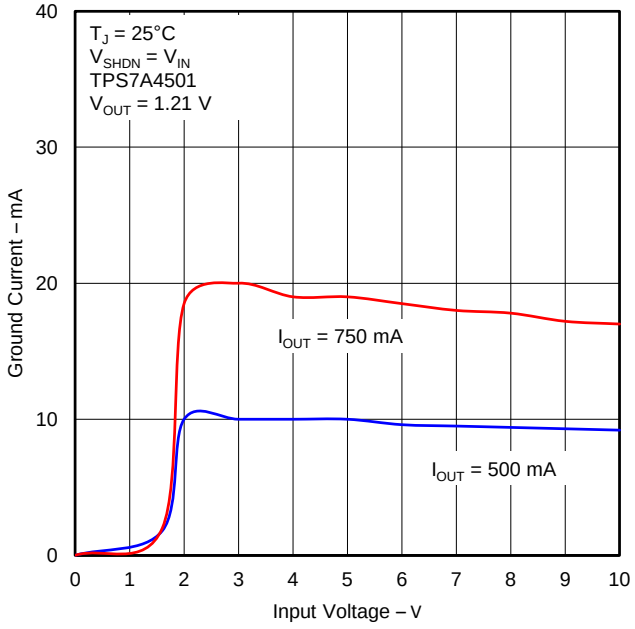


Figure 6.

GROUND CURRENT vs INPUT VOLTAGE

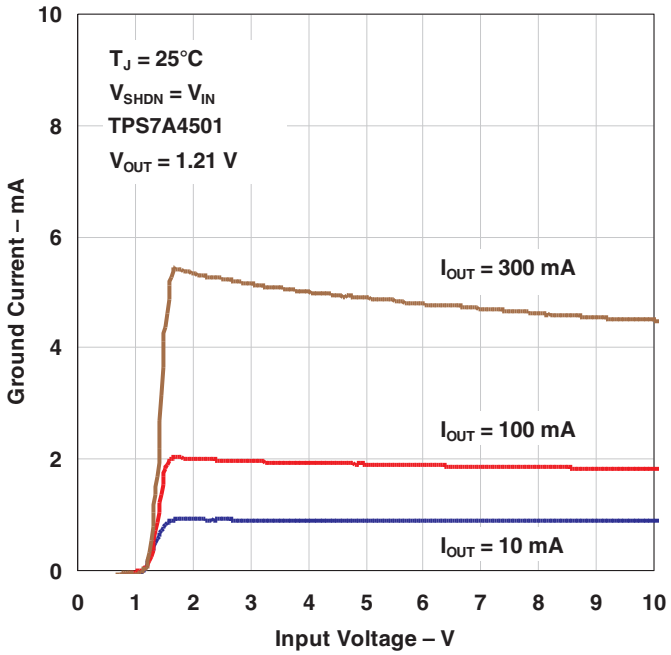


Figure 7.

GROUND CURRENT vs OUTPUT CURRENT

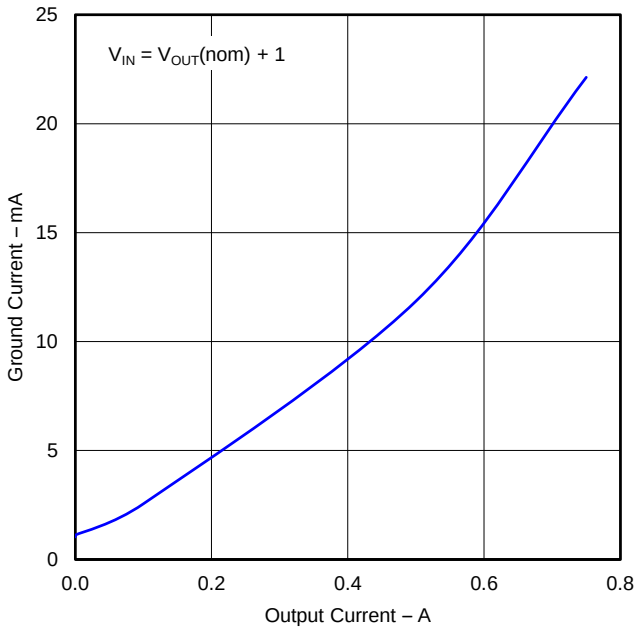


Figure 8.

TYPICAL CHARACTERISTICS (continued)

$\overline{SHDN}$ INPUT CURRENT vs TEMPERATURE

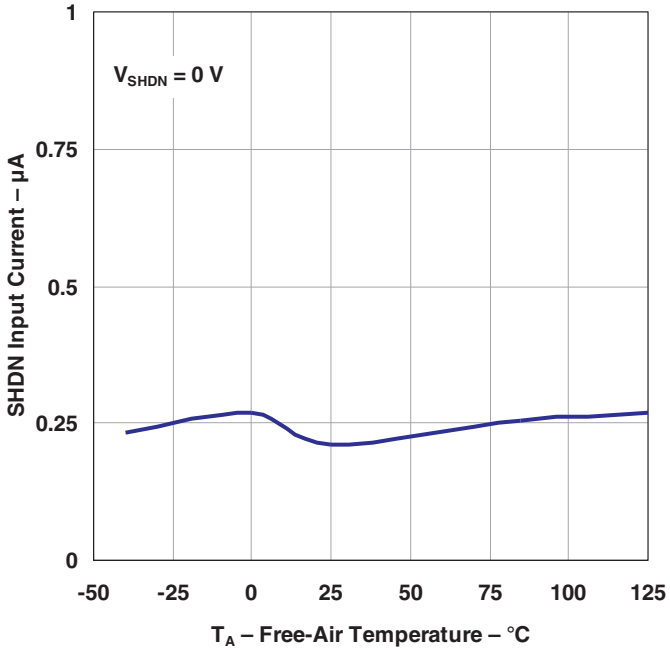


Figure 9.

$\overline{SHDN}$ INPUT CURRENT vs $\overline{SHDN}$ INPUT VOLTAGE

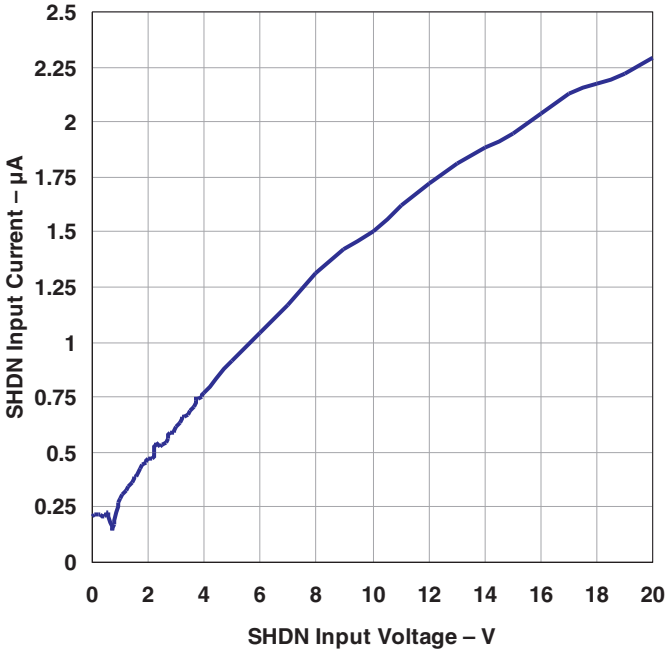


Figure 10.

$\overline{SHDN}$ THRESHOLD (OFF TO ON) vs TEMPERATURE

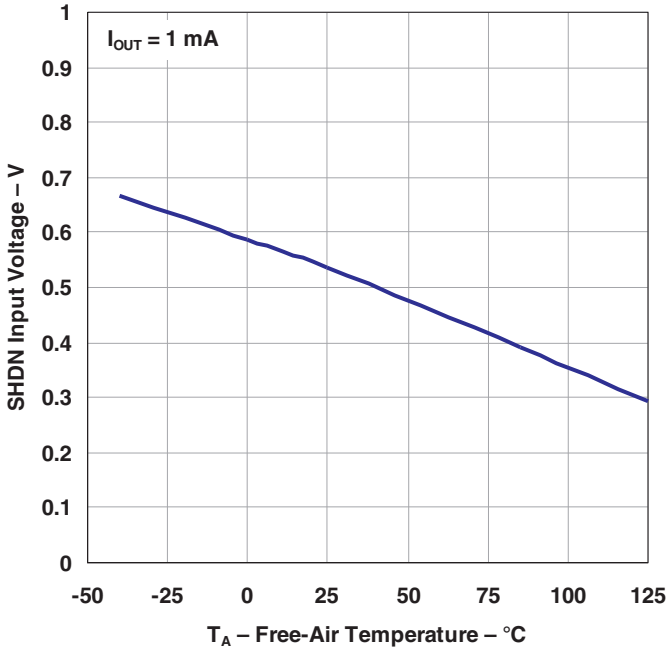


Figure 11.

$\overline{SHDN}$ THRESHOLD (ON TO OFF) vs TEMPERATURE

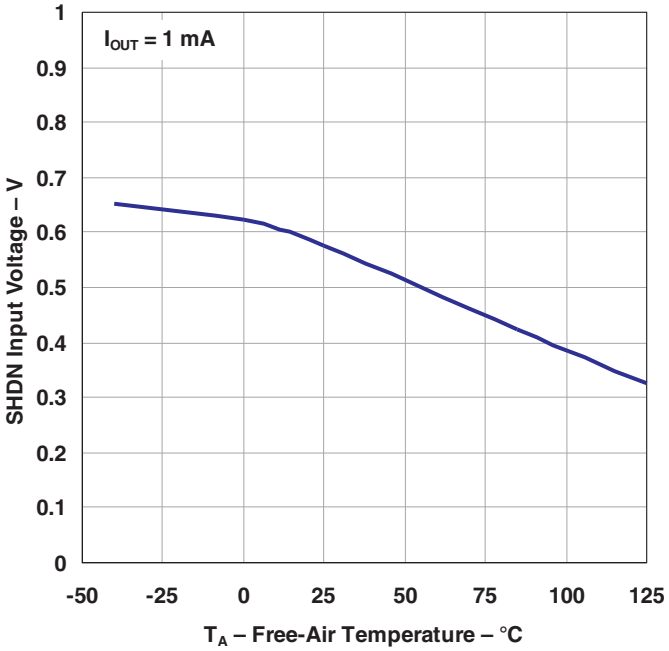


Figure 12.

TYPICAL CHARACTERISTICS (continued)

ADJ BIAS CURRENT
vs
TEMPERATURE

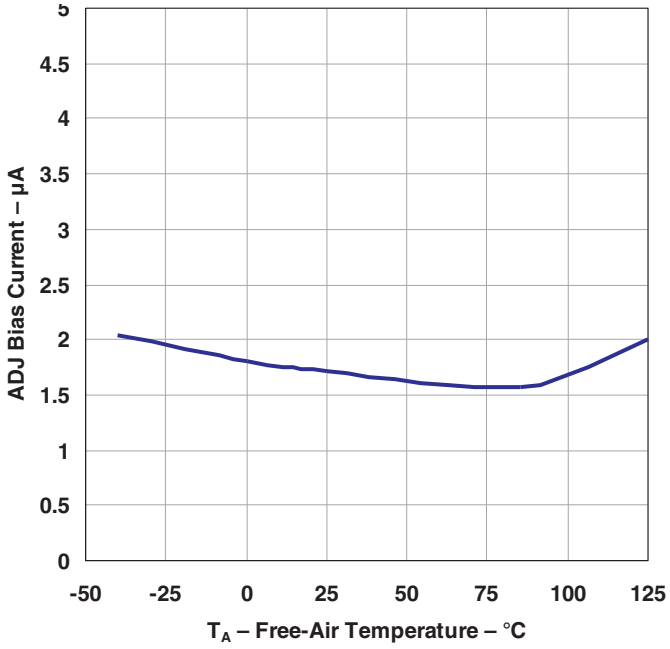


Figure 13.

CURRENT LIMIT
vs
INPUT/OUTPUT DIFFERENTIAL VOLTAGE

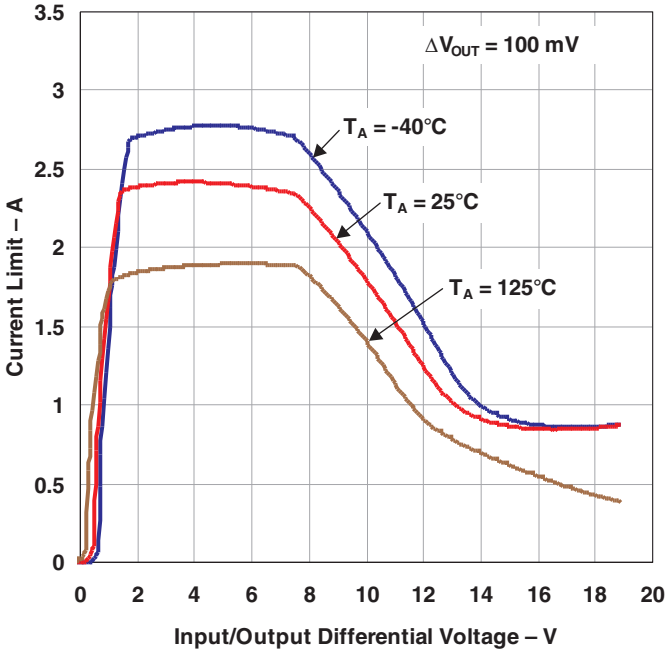


Figure 14.

CURRENT LIMIT
vs
TEMPERATURE

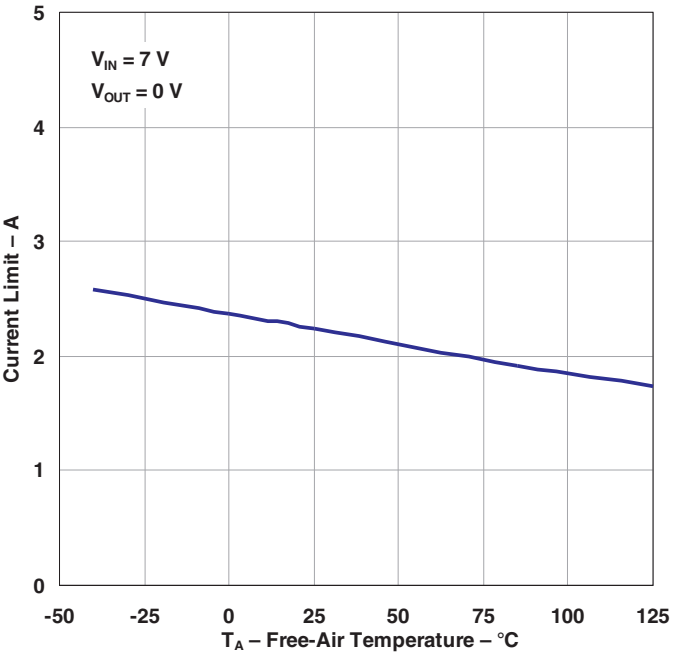


Figure 15.

REVERSE OUTPUT CURRENT
vs
OUTPUT VOLTAGE

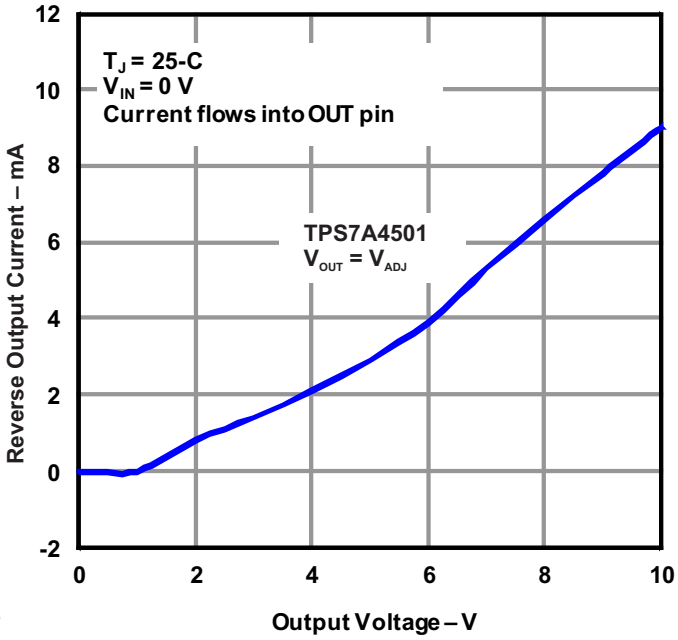


Figure 16.

TYPICAL CHARACTERISTICS (continued)

REVERSE OUTPUT CURRENT
vs
TEMPERATURE

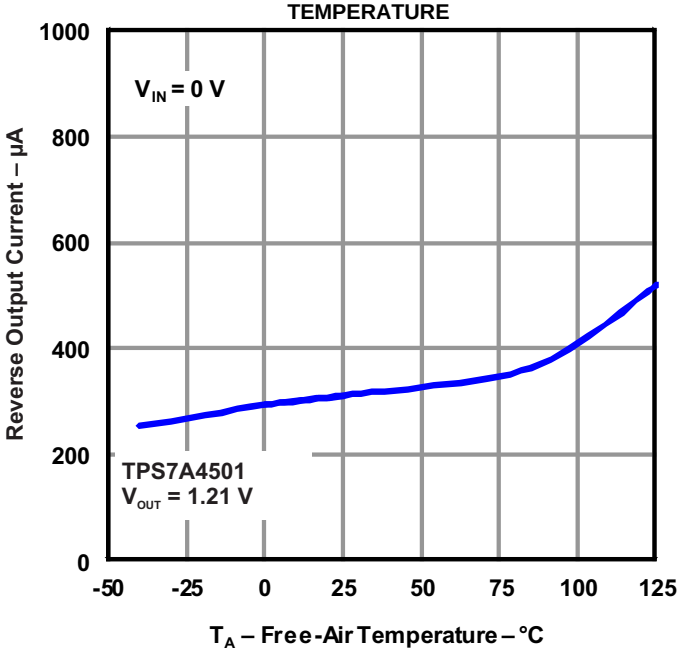


Figure 17.

RIPPLE REJECTION
vs
FREQUENCY

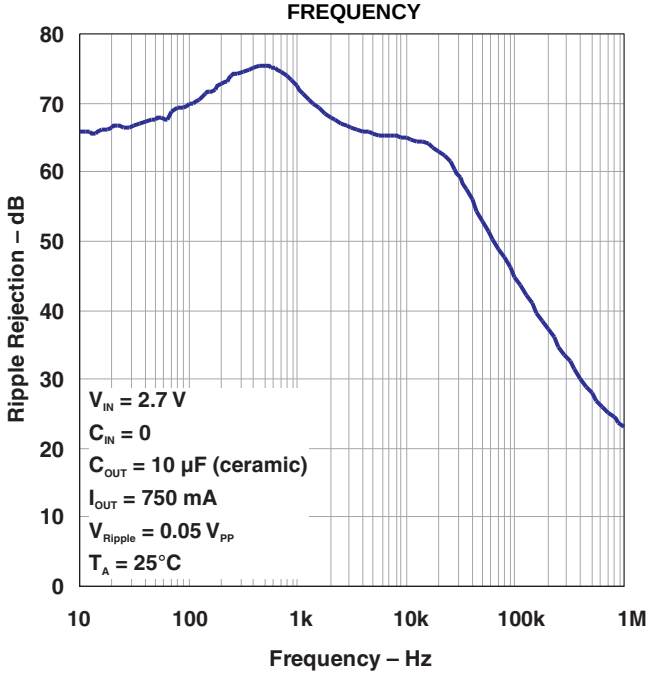


Figure 18.

LOAD REGULATION
vs
TEMPERATURE

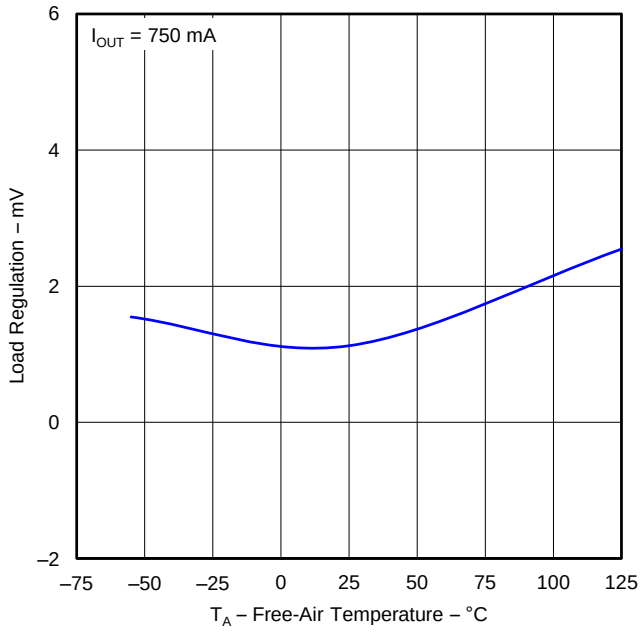


Figure 19.

LOAD TRANSIENT RESPONSE

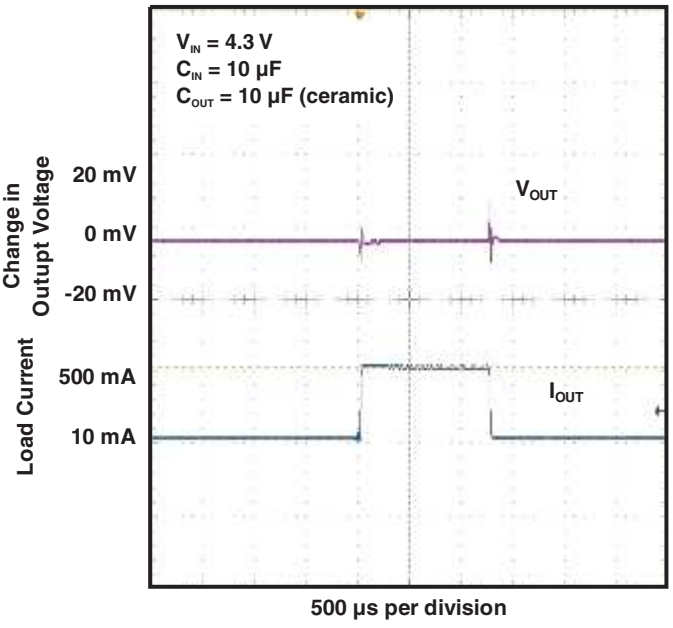


Figure 20.

APPLICATION INFORMATION

The TPS7A4501 is a 750-mA low-dropout regulator optimized for fast transient response. The device is capable of supplying 750 mA at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1 µA in shutdown. In addition to the low quiescent current, the TPS7A4501 regulator incorporates several protection features that makes it ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS7A4501 acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as (20 V - VIN) and still allow the device to start and operate.

Typical Applications

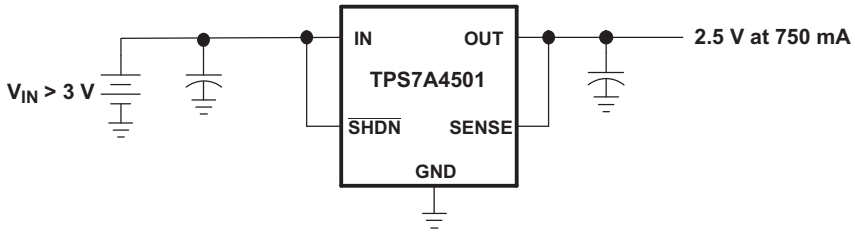


Figure 22. 3.3 V to 2.5 V Regulator

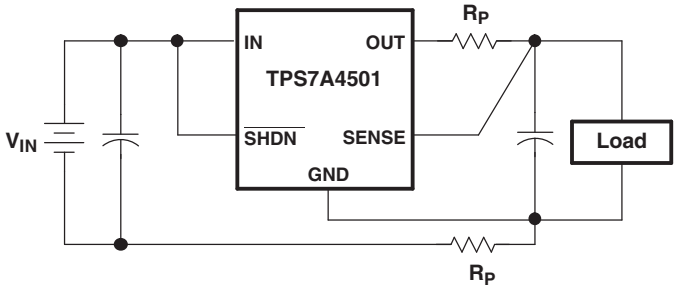
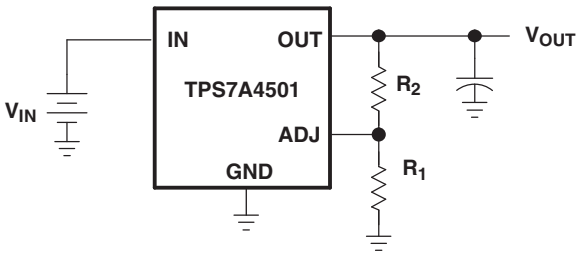


Figure 23. Kelvin Sense Connection

Adjustable Operation

The adjustable TPS7A4501 has an output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in Figure 24. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula shown in Figure 24. The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.



$V_{OUT} = 1.21\ V\left(1 + \frac{R2}{R1}\right) + (I_{ADJ})(R2)$
$V_{ADJ} = 1.21$ V
$I_{ADJ} = 3$ µA at 25°C
Output range = 1.21 V to 20 V

Figure 24. Adjustable Operation

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT}/1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –3 mV (typ) at V_{OUT} = 1.21 V. At V_{OUT} = 5 V, load regulation is:

(5 V/1.21 V)(–3 mV) = –12.4 mV

Compensation

TPS7A4501 is internally compensated, however, a lead network using C_3 can be implemented to boost the phase margin as well as reduce output noise.

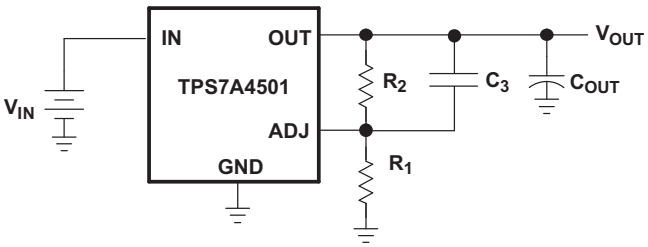


Figure 25. Compensation

R_1 bottom resistor, R_2 top resistor form the output voltage divider network. C_3 across R_2 adds a lead network.

For R_1 = 3.2 kΩ and R_2 = 10 kΩ V_{OUT} is set at 5 V and C_3 = 470 pF.

Zero and pole can be calculated as shown below.

$$f_{z2} = \frac{1}{2 \bullet \pi \bullet R_2 \bullet C_3} \quad (1)$$

f_{z2} = 33.863 kHz

$$R_{1p} = \frac{R_1 \bullet R_2}{R_1 + R_2} \quad (2)$$

R_{1p} = 2.424 kΩ

$$f_{p2} = \frac{1}{2 \bullet \pi \bullet R_{1p} \bullet C_3} \quad (3)$$

f_{p2} = 139.684 kHz

Output Capacitance and Transient Response

The TPS7A4501 regulator is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS7A4501, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectric used for harsh environment is X7R. Ceramic capacitors loose capacitance when DC bias is applied across the capacitor. This capacitance loss is due to the polarization of the ceramic material. The capacitance loss is not permanent: after a large DC bias has been applied, reducing the DC bias will reduce the degree of polarization and capacitance will increase. DC bias effects vary dramatically with voltage rating, case size, capacitor value, and capacitor manufacturer. Since a capacitor could lose more than 50% of its capacitance with DC bias voltages near the voltage rating of the capacitor, it is important to consider DC bias when selecting a ceramic capacitor for an application.

Ceramic capacitors dielectric also change over the temperature range. For example X7R, first two letters X denotes lower temperature range -55°C whereas 7 denotes higher temperature range 125°C and R denotes capacitance variation over the temperature range (±15%). For harsh environment applications minimum dielectric thickness must be 1mil for 100V DC rated capacitor and 0.8mil for 50V DC rated capacitors.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

Tantalum capacitors can provide higher capacitance per unit volume. Tantalum capacitors can be either manganese dioxide (MNO2) based capacitors where cathode is MN02 or polymer. MN02 based tantalum capacitors will exhibit high ESR as compared to polymer based tantalum capacitors. MN02 based tantalum capacitors require in excess of 60% voltage derating. Thus a 10V rated capacitor can only be used for 3.3V application. Whereas polymer based capacitors only require 10% voltage derating. Paralleling ceramic and tantalum capacitors will provide optimum balance between capacitance and ESR.

Table 2 highlights some of the capacitors used in the device.

Overload Recovery

Like many IC power regulators, the TPS7A4501 has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS7A4501.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The TPS7A4501 regulator has been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 50 uV/$\sqrt{Hz}$ over this frequency bandwidth for the TPS7A4501. For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS7A4501. Power-supply ripple rejection must also be considered; the TPS7A4501 regulator does not have unlimited power-supply rejection and passes a small portion of the input noise through to the output.

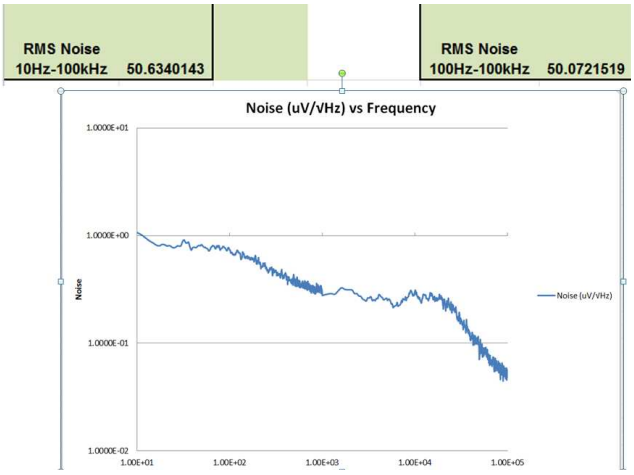


Figure 26. Output Noise Plot, V_{IN} = 7 V, V_{OUT} = 5 V at 750 mA , C_{OUT} = 22 µF Tantalum Capacitor

Table 2. TPS7A4501-SP Capacitors

Capacitor Part Number	Capacitor Details Type Vendor (Capacitor, Voltage, ESR)	Type	Vendor
T493X226M025AH6x20	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT}(V_{IN} – V_{OUT})$
2. GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$.

The GND pin current can be found using the GND Pin Current graphs in *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed above.

Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum case temperature of 50°C, what is the maximum junction temperature?

The power dissipated by the device is equal to:

$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT}) + I_{GND}(V_{IN(MAX)})$

where,

$I_{OUT(MAX)}$ = 500 mA

$V_{IN(MAX)}$ = 6 V

I_{GND} at (I_{OUT} = 500 mA, V_{IN} = 6 V) = 10 mA

So,

P = 500 mA × (6 V – 3.3 V) + 10 mA × 6 V = 1.41 W

Using a U package, the thermal resistance is about 10.3°C/W. So the junction temperature rise above case is approximately equal to:

1.41 W × 10.3°C/W = 14.5°C

The TPS7A4501 regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The maximum junction temperature is then be equal to the maximum junction-temperature rise above case plus the maximum case temperature or:

T_{JMAX} = 50°C + 14.5°C = 64.5°C

Protection Features

The TPS7A4501 regulator incorporates several protection features which makes it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 μA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS7A4501 can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the SHDN pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7-V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13-V difference between OUT and ADJ divided by the 5-mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TPS7A4501 is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 μA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the SHDN pin has no effect on the reverse output current when the output is pulled above the input.

修订历史记录

Changes from Original (December 2013) to Revision A	Page
• Changed 产品状态从产品预览改为生产数据	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1222402V9A	ACTIVE	XCEPT	KGD	0	100	TBD	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962-1222402VHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	1222402VHA 7A4501-SP	Samples
5962R1222403V9A	ACTIVE	XCEPT	KGD	0	50	TBD	Call TI	Call TI	-25 to 125		Samples
5962R1222403VXC	ACTIVE	CFP	HKU	10	1	TBD	Call TI	Call TI	-55 to 125	R1222403VXC 7A4501-RHA	Samples
TPS7A4501HKU/EM	ACTIVE	CFP	HKU	10	1	TBD	AU	N / A for Pkg Type	25 Only	7A4501HKU/EM EVAL ONLY	Samples
TPS7A4501U/EM	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	25 Only	7A4501U/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

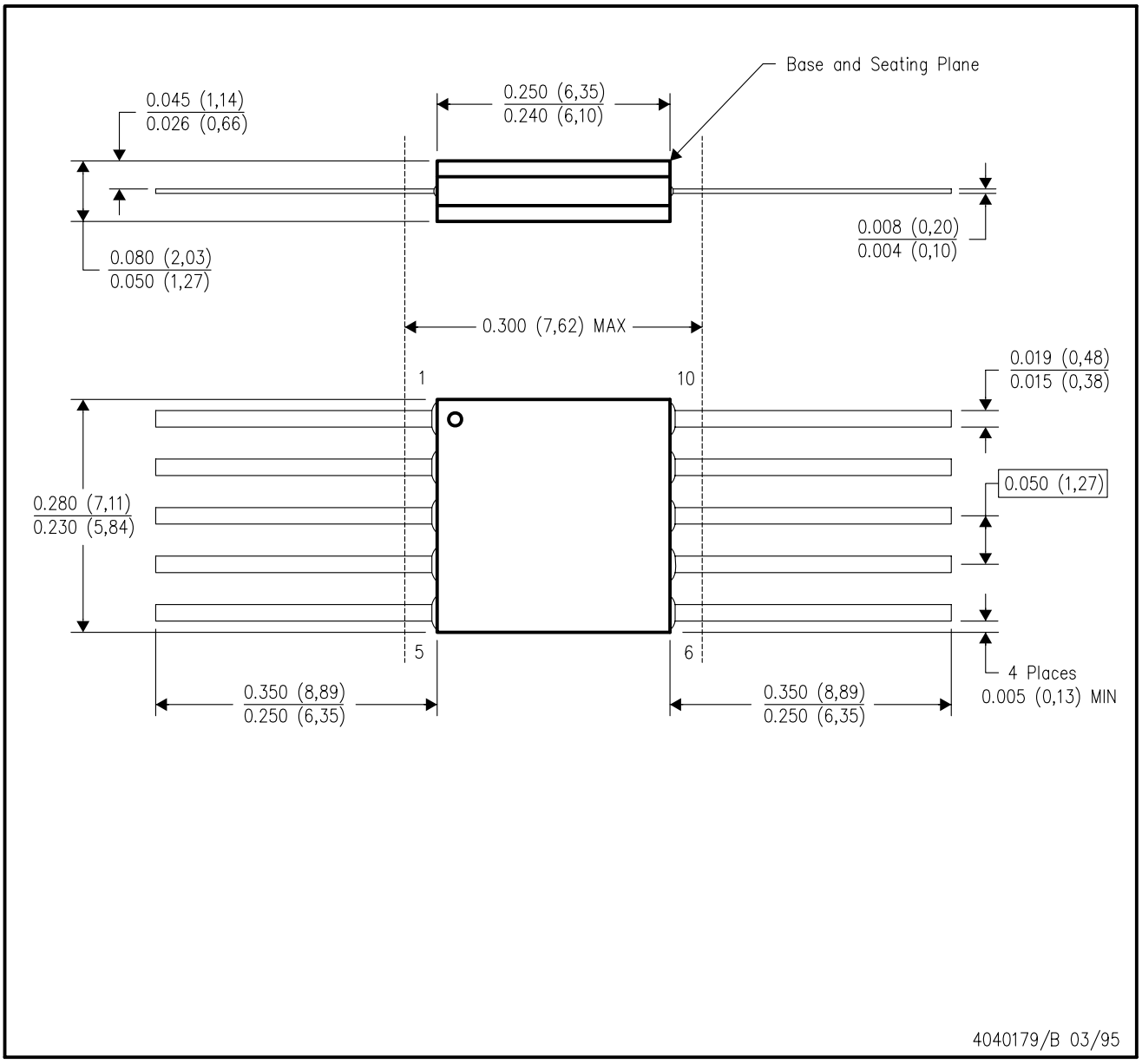
OTHER QUALIFIED VERSIONS OF TPS7A4501-SP :

- Catalog: TPS7A4501
- Military: TPS7A4501M

NOTE: Qualified Version Definitions:

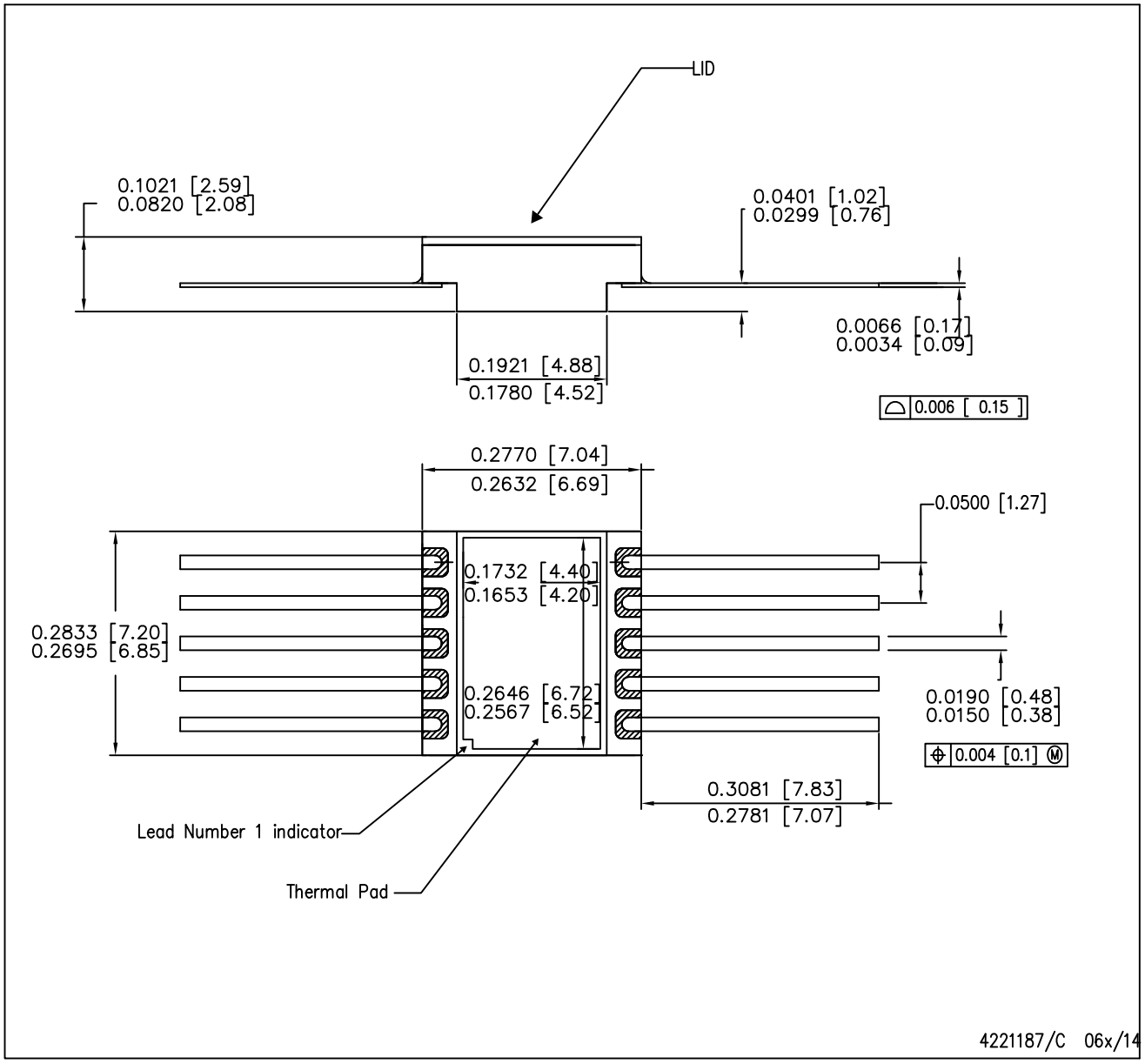
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

HKU (R–CDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This drawing does not comply with Mil Std 1835. Do not use this package for compliant product.
D. The terminals will be gold plated.

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TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

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