REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline F. Make changes to 1.2.4, 1.3, and FIGURE 1. - ro	97-10-20	R. MONNIN
B	Make change to power dissipation as specified under 1.3. - ro	97-11-18	R. MONNIN
C	Add device type 02. Add case outline X. Changes to θ_{JA} and θ_{JC} for case F. Add radiation hardened requirements. Add vendor CAGE 65342. - rrp	00-05-25	R. MONNIN
D	Make change to the offset voltage, V_{OS}, test in table I. Update boilerplate. –rrp	01-03-01	R. MONNIN
E	Add device type 03. Editorial changes throughout. –rrp	01-06-11	R. MONNIN
F	Add radiation hardened version of device type 01. Make changes to 1.2.2, 1.5, I_{CC}, and I_{CCZ} tests in table I. –rrp	01-09-06	R. MONNIN
G	Add case outline Z. Changes to 1.2.4, 1.3, and figure 1. –rrp	02-04-11	R. MONNIN
H	Make change to note 1/ in table I for device type 01. –rrp	02-04-30	R. MONNIN
J	Make change to the neutron irradiation and SEL latch-up tests in paragraph 1.5. Removed dose rate induced latchup testing and dose rate burnout paragraphs in section 4. Modified paragraph 4.4.4.3. –rrp	02-08-12	R. MONNIN
K	Add device type 01 to the SEL latchup test in 1.5. –rrp	03-05-08	R. MONNIN
L	Add power-off leakage test, I_{OFF}, in table I. –rrp	03-07-28	R. MONNIN
M	Make changes to neutron irradiation and SEL latch-up features in paragraph 1.5. –rrp	08-06-02	R. HEBER
N	Add room temperature anneal note to device type 01 in paragraph 1.5. –rrp	09-01-06	R. HEBER
P	Add microcircuit die appendix A and paragraph 3.1.1. - ro	09-03-12	R. HEBER

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	P	P	P																
SHEET	15	16	17																

REV STATUS	REV	P	P	P	P	P	P	P	P	P	P	P	P	P	P
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
SANDRA ROONEY

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
SANDRA ROONEY

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
96-05-03

REVISION LEVEL
P

MICROCIRCUIT, LINEAR, LVDS QUAD CMOS DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95833**

SHEET 1 OF 17

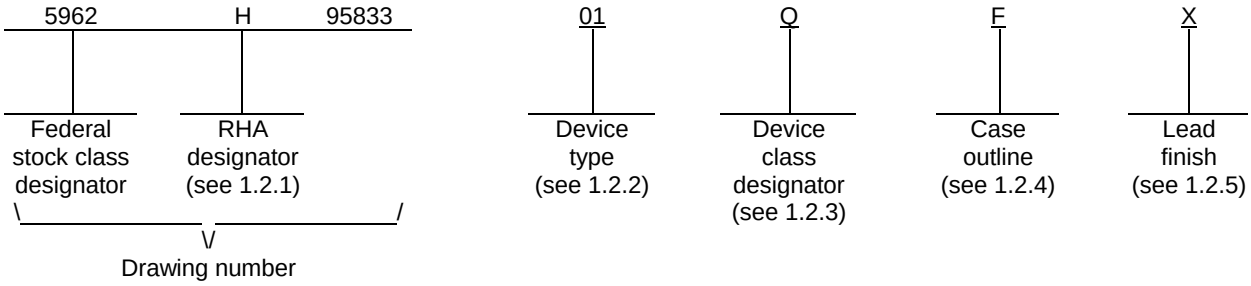
DSCC FORM 2233
APR 97

5962-E188-09

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	DS90C031	Radiation hardened, LVDS quad cmos differential line driver
02	UT54LVDS031	Radiation hardened, LVDS quad cmos differential line driver
03	UT54LVDSC031	Radiation hardened, LVDS quad cmos differential line driver with cold spare on LVDS bus

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
X	CDFP4-F16	16	Flat pack
Z	GDFP1-G16	16	Flat pack with gull wing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.3 V to +6 V
Input voltage (V_{IN})	-0.3 V to (V_{CC} + 0.3 V)
Enable input voltage (EN, EN*)	-0.3 V to (V_{CC} + 0.3 V)
Output voltage (D_{OUT+}, D_{OUT-})	-0.3 V to (V_{CC} + 0.3 V)
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D):	
Cases F and Z	1450 mW 2/
Case 2	1900 mW 2/
Case X	1250 mW 2/
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+150°C 3/
Thermal resistance, junction-to-case (θ_{JC}):	
Cases F and Z	14°C/W
Case 2	18°C/W
Case X	10°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Cases F and Z	145°C/W
Case 2	78°C/W
Case X	120°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V to 5.5 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features

Total dose (effective dose rate = 0.16 rad(Si)/s):	
Device type 01	≥ 100 Krad (Si) 4/
Total dose (dose rate = 50 – 300 rad(Si)/s):	
Device type 02	≥ 1 Mrad (Si)
Device type 03	≥ 300 Krad (Si)
Neutron irradiation:	
Device types 02 and 03	5/
Single event latch-up (SEL):	
Device types 01, 02, and 03	≥100 MeV-cm^2/mg 6/ 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ At T_A > +25°C, the derating factor for cases F and Z is 9.7 mW/°C, 12.8 mW/°C for case 2, and 0.04 mW/°C for case X.

3/ For device types 02 and 03, the maximum junction temperature may be increased to +175°C during burn-in and life test.

4/ Device type 01 is irradiated at dose rate = 50 - 300 rads(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 0.16 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

5/ Neutron irradiation is not tested but guaranteed up to 1 x 10^{13} neutrons/cm^2. Contact manufacturer for requirements beyond this level.

6/ Limits are based on characterization, but not production tested unless specified by the customer through the purchase order or contract.

7/ Device type 01, applicable to class V only.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. For device type 01, the radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. For device types 02 and 03, the radiation exposure circuit shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage high	V_{OH}	R_L = 100 Ω	1,2,3	All		1.6	V
Output voltage low	V_{OL}	R_L = 100 Ω	1,2,3	All	0.9		V
Input voltage high	V_{IH}		1,2,3	All	2.0	V_{CC}	V
Input voltage low	V_{IL}		1,2,3	All	GND	0.8	V
Input current	I_{IN}	V_{IN} = V_{CC}, GND, 2.5 V or 0.4 V	1,2,3	01	-10	10	µA
		V_{IN} = V_{CC}, GND 3/		02	-10	10	
		V_{IN} = 5.5 V, V_{CC} = GND, LVDS outputs		03	-10	10	
Differential output voltage	V_{OD1}	R_L = 100 Ω	1,2,3	01	250	450	mV
				02, 03	250	400	
Offset voltage	V_{OS}	R_L = 100 Ω	1,2,3	All	1.125	1.375	V
Change in magnitude of V_{OD1} for complementary output states	DV_{OD1}	R_L = 100 Ω	1,2,3	01		35	mV
				02, 03		10	
Change in magnitude of V_{OS} for complementary output states	DV_{OS}	R_L = 100 Ω	1,2,3	All		25	mV
Input clamp voltage	V_I	I_{IN} = -18 mA	1,2,3	01		-1.5	V
		I_{IN} = -18 mA 4/		02, 03		-1.5	
Power-off leakage	I_{OFF}	V_{OUT} = 0 V or 2.4 V, V_{CC} = 0 V or open	1,2,3	01	-10	10	µA
Output short circuit current	I_{OS}	V_{OUT} = 0 V	1,2,3	01		-5.0	mA
		V_{OUT} = 0 V 4/		02, 03		-5.0	
Output tri-state current	I_O	EN = 0.8 V, EN* = 2.0 V, V_{OUT} = 0 V or V_{CC} 3/	1,2,3	All	-10	10	µA
Drivers enabled supply current	I_{CC}	D_{IN} = high or low	1,2,3	01		25	mA
		M,D,P,L,R	1			30	
		D_{IN} = V_{CC} or V_{SS} 3/	1,2,3	02, 03		25	
Drivers disabled supply current	I_{CCZ}	D_{IN} = high or low, EN = GND, EN* = V_{CC}	1,2,3	01		10	mA
		M,D,P,L,R	1			30	
		D_{IN} = V_{CC} or V_{SS}, EN = GND, EN* = V_{CC} 3/	1,2,3	02, 03		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test	FT	See 4.4.1c	7,8	All			
Differential propagation delay, high to low	t_{PHLD}		9,10,11	All	0.5	5.0	ns
Differential propagation delay, low to high	t_{PLHD}		9,10,11	All	0.5	5.0	ns
Differential skew	t_{SKD}		9,10,11	01		3	ns
		4/		02, 03		3	
Channel to channel 5/ skew	t_{SK1}		9,10,11	01		3	ns
		4/		02, 03		3	
Chip to chip skew 6/	t_{SK2}		9,10,11	01		4.5	ns
		4/		02, 03		4.5	
Disable time, high to Z	t_{PHZ}		9,10,11	01		20	ns
		4/		02, 03		10	
Disable time, low to Z	t_{PLZ}		9,10,11	01		20	ns
		4/		02, 03		10	
Enable time, Z to high	t_{PZH}		9,10,11	01		20	ns
		4/		02, 03		10	
Enable time, Z to low	t_{PZL}		9,10,11	01		20	ns
		4/		02, 03		10	

1/ Device type 01 supplied to this drawing is tested at all levels M, D, P, L, R of irradiation. Device type 02 supplied to this drawing meets all levels M, D, P, L, R, F, G, H of irradiation. However, this device is only tested at the "H" level. Device type 03 supplied to this drawing meets all levels M, D, P, L, R, F of irradiation. However, this device is only tested at the "F" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ For device type 01, $V_{CC} = 4.5$ V, 5.0 V, and 5.5 V, $R_L = 100\ \Omega$ between outputs, $C_L = 20$ pF each output to GND, unless otherwise specified. For device types 02 and 03, $V_{CC} = 4.5$ V and 5.5 V.

3/ Device types 02 and 03, tested at $V_{CC} = 5.5$ V only.

4/ These parameters may not be tested, but shall be guaranteed to the limits specified in table I herein.

5/ Channel to channel skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

6/ Chip to chip skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Device types	01		02, 03
Case outlines	F and Z	2	X
Terminal number	Terminal symbol		
1	INPUT A	NC	INPUT A
2	OUTPUT A+	INPUT A	OUTPUT A+
3	OUTPUT A-	OUTPUT A+	OUTPUT A-
4	ENABLE	OUTPUT A-	ENABLE
5	OUTPUT B-	ENABLE	OUTPUT B-
6	OUTPUT B+	NC	OUTPUT B+
7	INPUT B	OUTPUT B-	INPUT B
8	GND	OUTPUT B+	GND
9	INPUT C	INPUT B	INPUT C
10	OUTPUT C+	GND	OUTPUT C+
11	OUTPUT C-	NC	OUTPUT C-
12	$\overline{\text{ENABLE}}$	INPUT C	$\overline{\text{ENABLE}}$
13	OUTPUT D-	OUTPUT C+	OUTPUT D-
14	OUTPUT D+	OUTPUT C-	OUTPUT D+
15	INPUT D	$\overline{\text{ENABLE}}$	INPUT D
16	V_{CC}	NC	V_{CC}
17	---	OUTPUT D-	---
18	---	OUTPUT D+	---
19	---	INPUT D	---
20	---	V_{CC}	---

FIGURE 1. Terminal connections.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 1/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9, 10,11	1,2,3,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.

TABLE III. Irradiation test connections.

Test	1/	V_{DD} = 5.5 V	Ground
Radiation exposure	2,3,5,6,10, 11,13,14	4,9,15,16	1,7,8,12

1/ A 100 Ω resistor is connected between pins 2 and 3, 5 and 6, 10 and 11, and 13 and 14. One resistor is attached to each pair.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall include verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. Neutron testing is not required for this technology. Devices are guaranteed to meet the post irradiation end point electrical parameter limits as defined in table I after exposure of 1×10^{13} neutrons/cm^2 minimum.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

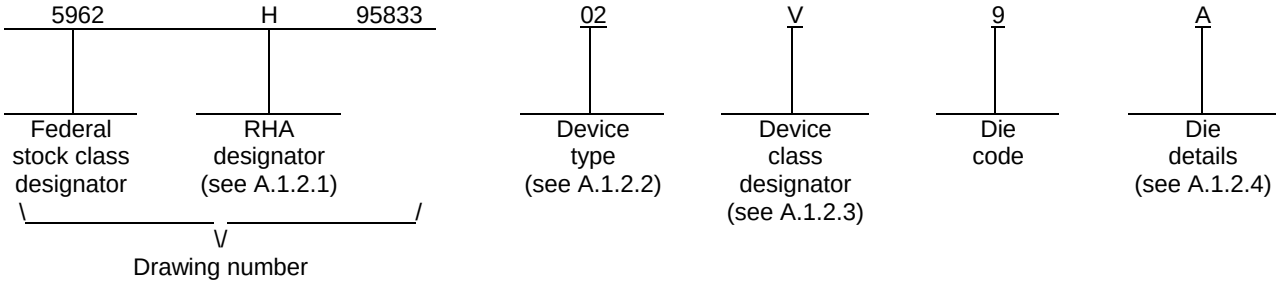
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
02	UT54LVDS031	Radiation hardened, LVDS quad cmos differential line driver
03	UT54LVDSC031	Radiation hardened, LVDS quad cmos differential line driver with cold spare on LVDS bus

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
02, 03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02, 03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
02, 03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
02, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

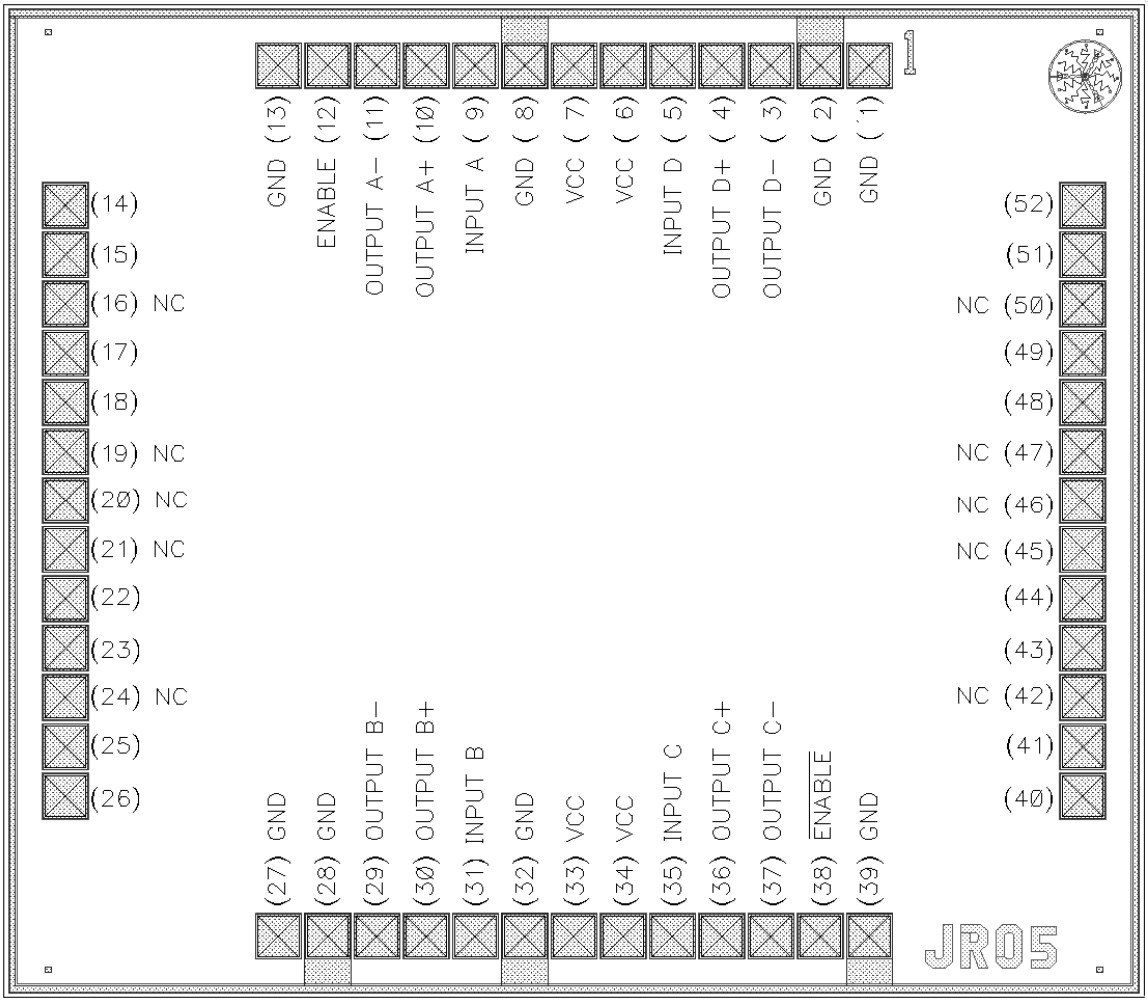
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.



NOTE: Numbers identify die pad position and do not reflect terminal numbers.

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions.

Die physical dimensions.
Die size: 85.0 mils x 74.0 mils
Die thickness: 17.5 mils ±1.0 mils

Interface materials.
Top metallization: Si Al Cu 6.2 kÅ – 7.6 kÅ
Backside metallization: None

Glassivation.
Type: SiO_2 / SiN_4
Thickness: 9 kÅ – 11 kÅ

Substrate: Epitaxial layer on single crystal silicon

Assembly related information.
Substrate potential: Tied to GND.
Bond all GND and V_{CC} die pads.
Special assembly instructions: Contact manufacturer for bonding information on die pads 14 – 15, 17 – 18, 22 – 23, 25 – 26, 40 – 41, 43 – 44, 48 – 49, and 51 – 52.

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-03-12

Approved sources of supply for SMD 5962-95833 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9583301QFA	27014 3/	DS90C031W-QML
5962-9583301Q2A	27014	DS90C31E-QML
5962-9583301VFA	27014	DS90C031W-QMLV
5962R9583301VFA	27014	DS90C031WRQMLV
5962-9583301QZA	4/	DS90C031WG-QML
5962-9583301VZA	4/	DS90C031WG-QMLV
5962R9583301VZA	27014	DS90C031WGRQMLV
5962H9583302QXA	65342	UT54LVDS031UCA
5962H9583302QXC	65342	UT54LVDS031UCC
5962H9583302VXA	65342	UT54LVDS031UCA
5962H9583302VXC	65342	UT54LVDS031UCC
5962H9583302V9A	65342	UT54LVDS031-VDIE
5962H9583302Q9A	65342	UT54LVDS031-QDIE
5962F9583303QXA	65342	UT54LVDSC031UCA
5962F9583303QXC	65342	UT54LVDSC031UCC
5962F9583303VXA	65342	UT54LVDSC031UCA
5962F9583303VXC	65342	UT54LVDSC031UCC
5962F9583303V9A	65342	UT54LVDSC031-VDIE
5962F9583303Q9A	65342	UT54LVDSC031-QDIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Item has an end-of-life date of 12/1/2009.
4/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd Colorado Springs, CO 80907-3486