DS90C031QML LVDS Quad CMOS Differential Line Driver

Check for Samples: DS90C031QML

FEATURES

- **Radiation guaranteed 100 krad(Si)**
- **High impedance LVDS outputs with power-off**
- **±350 mV differential signaling**
- **Low power dissipation**
- **Low differential skew**
- **Low propagation delay**
- **Pin compatible with DS26C31**
- **Compatible with IEEE 1596.3 SCI LVDS standard**
- **Compatible with proposed TIA LVDS standard**
- **Fail safe logic for floating inputs**

DESCRIPTION

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, thus dropping the device to a low idle power state of 11 mW typical.

In addition, the DS90C031 provides power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present. The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.
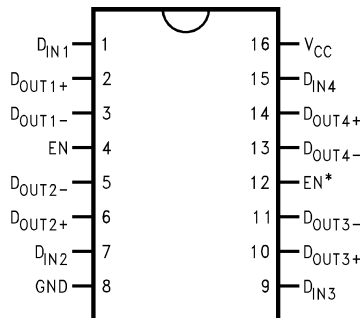
Connection Diagram

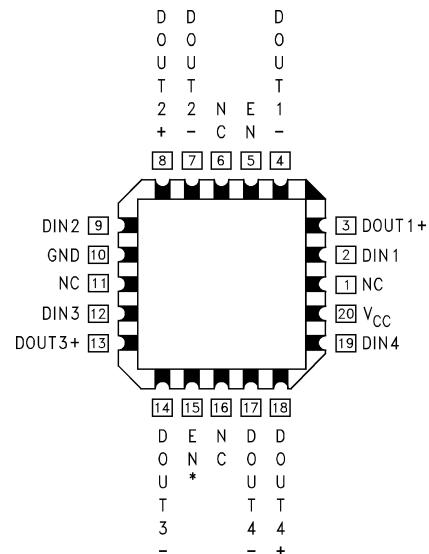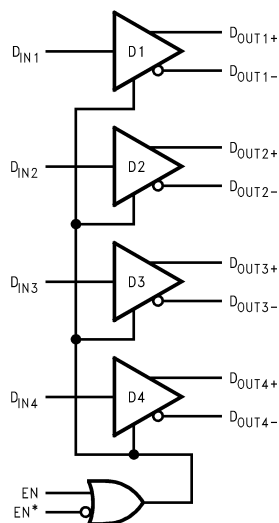**Figure 1. Dual-In-Line**
See Package Number NAD0016A & NAC0016A

Figure 2. LCCC Package
See Pacakage Number NAJ0020A

Functional Block Diagram

Truth Table

Enables		Input	Outputs	
EN	EN*	D_I	D_{O+}	D_{O-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Product Folder Links: *DS90C031QML*

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_I)	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{O+}, D_{O-})	−0.3V to + 5.8V
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature Range, Soldering (4 seconds)	+260°C
Maximum Package Power Dissipation at +25°C [2]	
20 Pin LCCC Package	1900 mW
16 Pin CLGA (NAD)	1450 mW
16 Pin CLGA (NAC)	1450 mW
Thermal Resistance	
θ_{JA}	
20 Pin LCCC Package	78°C/W
16 Pin CLGA (NAD)	145°C/W
16 Pin CLGA (NAC)	145°C/W
θ_{JC}	
20 Pin LCCC Package	18°C/W
16 Pin CLGA (NAD)	14°C/W
16 Pin CLGA (NAC)	14°C/W
ESD Rating [3]	3.5KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Derate LCCC at 12.8mW/°C above +25°C. Derate CLGA at 6.9mW/°C above +25°C.
(3) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)	−55	+25	+125	°C

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DC Parameters [1]

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{OD1}	Differential Ouput Voltage	$R_L = 100\Omega$		250	450	mV	1, 2, 3
DV_{OD1}	Change in Magnitude of Vod1 for complementary output States	$R_L = 100\Omega$			35	mV	1, 2, 3
V_{OS}	Offset Voltage	$R_L = 100\Omega$		1.125	1.375	V	1, 2, 3
DV_{OS}	Change in Magnitude of Vos for Complementary Output States	$R_L = 100\Omega$			25	mV	1, 2, 3
V_{OH}	Output Voltage High	$R_L = 100\Omega$			1.6	V	1, 2, 3
V_{OL}	Output Voltage Low	$R_L = 100\Omega$		0.9		V	1, 2, 3
V_{IH}	Input Voltage High		[2]	2.0	V_{CC}	V	1, 2, 3
V_{IL}	Input Voltage Low		[2]	Gnd	0.8	V	1, 2, 3
I_I	Input Current	$V_I = V_{CC}$, Gnd, 2.5, or 0.4V			±10	µA	1, 2, 3
V_{CI}	Input Clamp Voltage	$I_{CI} = -18mA$			-1.5	V	1, 2, 3
I_{OS}	Output Short Circuit Current	$V_O = 0V$			-5.0	mA	1, 2, 3
I_{Off}	Power-off Leakage	$V_O = 0V$ or 2.4V, $V_{CC} = 0V$ or Open			±10	µA	1, 2, 3
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V $V_O = 0V$ or V_{CC}			±10	µA	1, 2, 3
I_{CC}	Drivers Enabled Supply Current	D_I = Hi or Low			25	mA	1, 2, 3
I_{CCZ}	Drivers Disabled Supply Current	D_I = Hi or Low, En = Gnd, En* = V_{CC}			10	mA	1, 2, 3

(1) Pre and Post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the "Post Radiation Limits" table. Radiation end point limits for the noted parameters are guaranteed only for the conditions, as specified.
(2) Tested during V_{OH} / V_{OL} tests.

AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = 4.5V / 5.0V / 5.5V, R_L = 100Ω (between outputs), C_L = 20pF (each output to Gnd)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHLD}	Differential Propagation Delay High to Low			0.5	5.0	ns	9, 10, 11
t_{PLHD}	Differential Propagation Delay Low to High			0.5	5.0	ns	9, 10, 11
t_{SkD}	Differential Skew |tPHLD-tPLHD|				3.0	ns	9, 10, 11
t_{Sk1}	Channel to Channel Skew		(1)		3.0	ns	9, 10, 11
t_{Sk2}	Chip to Chip Skew		(2)		4.5	ns	9, 10, 11
t_{PHZ}	Disable Time High to Z		(3)		20	ns	9, 10, 11
t_{PLZ}	Disable Time Low To Z		(3)		20	ns	9, 10, 11
t_{PZH}	Enable Time Z to High		(3)		20	ns	9, 10, 11
t_{PZL}	Enable Time Z to Low		(3)		20	ns	9, 10, 11

(1)   Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
(2)   Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
(3)   Parameter guaranteed, not tested 100%

AC/DC Parameters - Post Radiation Limits (1)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Drivers Enabled Supply Current	D_I - Hi or Low, En = Gnd, En* = V_{CC}			30	mA	1
I_{CCZ}	Drivers Disabled Supply Current	D_I - Hi or Low, En = Gnd, En* = V_{CC}			30	mA	1

(1)   Pre and Post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the "Post Radiation Limits" table. Radiation end point limits for the noted parameters are guaranteed only for the conditions, as specified.
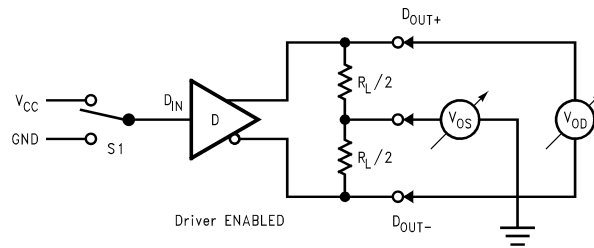
Parameter Measurement Information

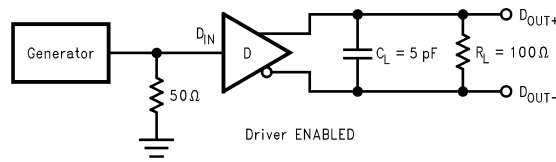**Figure 3. Driver V_{OD} and V_{OS} Test Circuit**

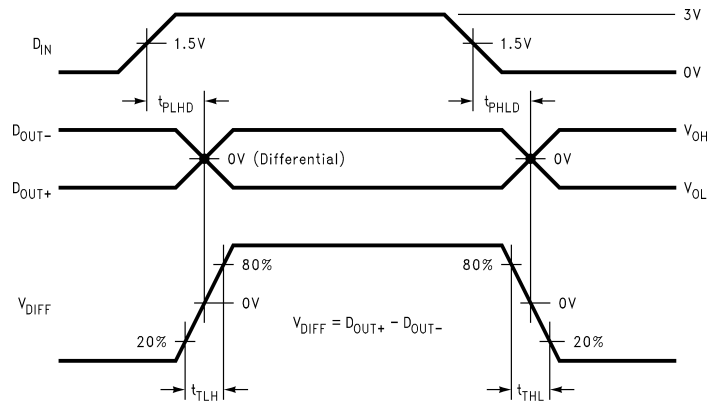**Figure 4. Driver Propagation Delay and Transition Time Test Circuit**

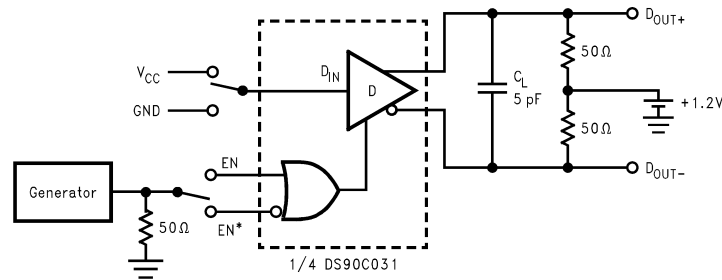**Figure 5. Driver Propagation Delay and Transition Time Waveforms**

Figure 6. Driver TRI-STATE Delay Test Circuit

Product Folder Links: *DS90C031QML*

Parameter Measurement Information (continued)
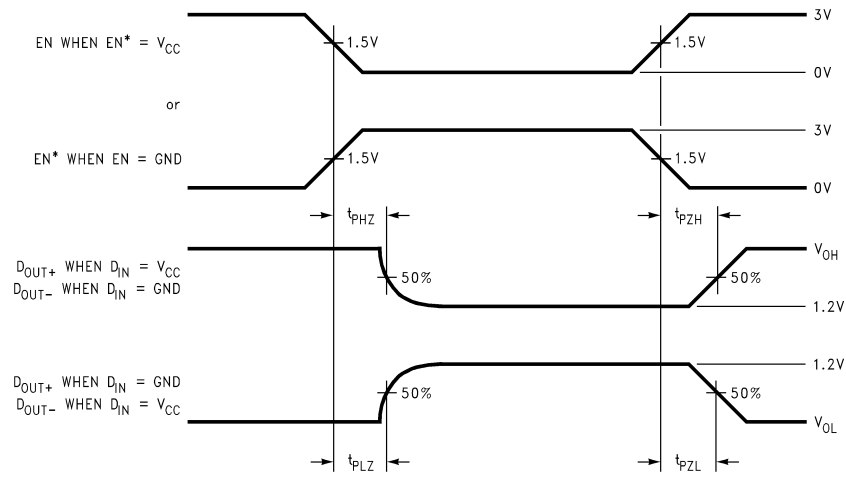
Figure 7. Driver TRI-STATE Delay Waveform

Typical Performance Characteristics
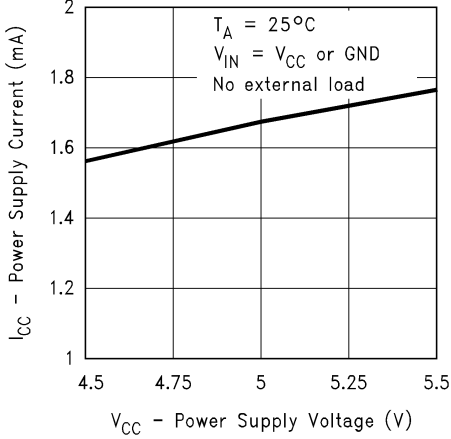
Power Supply Current vs Power Supply Voltage
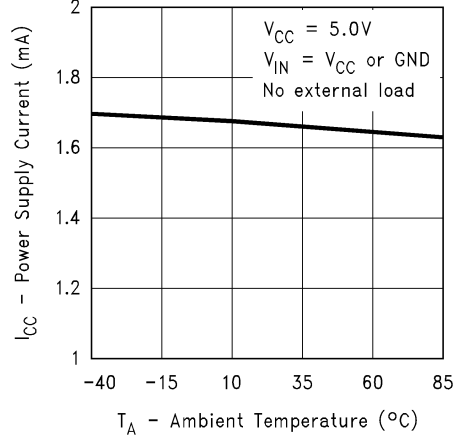
I_{CC} – Power Supply Current (mA)

V_{CC} – Power Supply Voltage (V)

T_A = 25°C
V_{IN} = V_{CC} or GND
No external load

Figure 8.

Power Supply Current vs Temperature

I_{CC} – Power Supply Current (mA)

T_A – Ambient Temperature (°C)

V_{CC} = 5.0V
V_{IN} = V_{CC} or GND
No external load

Figure 9.

Power Supply Current vs Power Supply Voltage

I_{CC} – Power Supply Current (mA)

V_{CC} – Power Supply Voltage (V)

T_A = 25°C
V_{IN} = V_{CC} or GND
Ext. load = 100Ω/dr.
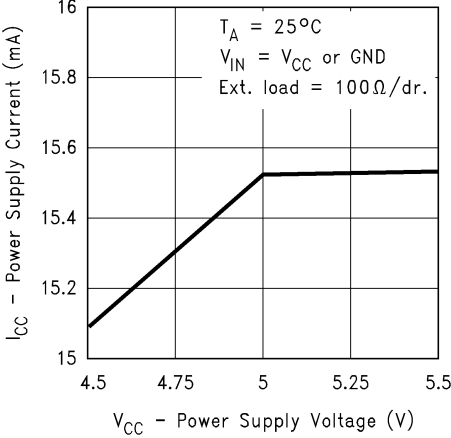
Figure 10.

Power Supply Current vs Temperature

I_{CC} – Power Supply Current (mA)

T_A – Ambient Temperature (°C)

V_{CC} = 5.0V
V_{IN} = V_{CC} or GND
Ext. load = 100Ω/dr.
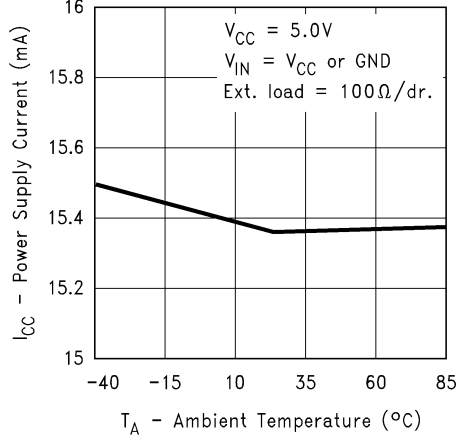
Figure 11.

Output TRI-STATE Current vs Power Supply Voltage

I_{OZ} – Output TRI-STATE Current (μA)

V_{CC} – Power Supply Voltage (V)

T_A = 25°C
V_{IN} = V_{CC} or GND
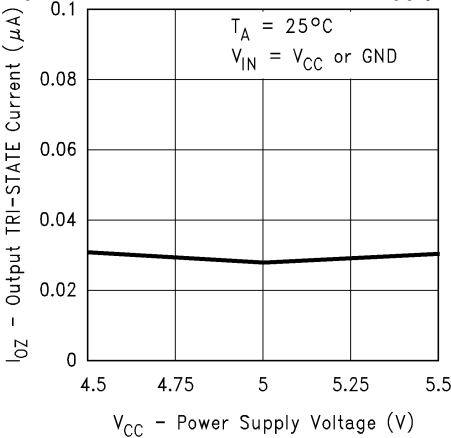
Figure 12.

Output Short Circuit Current vs Power Supply Voltage

I_{OS} – Output Short Circuit Current (mA)

V_{CC} – Power Supply Voltage (V)

T_A = 25°C
V_{IN} = 0V or 5V
V_{OUT} = 0V

Figure 13.

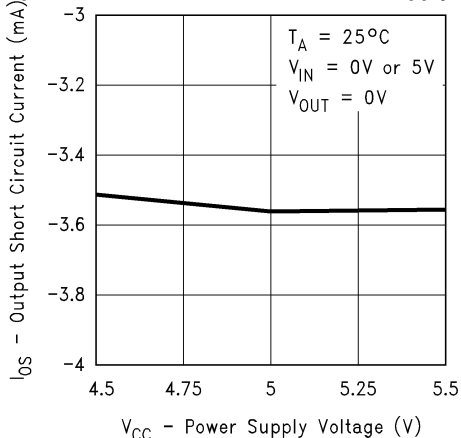Product Folder Links: DS90C031QML

Typical Performance Characteristics (continued)

Differential Output Voltage vs Power Supply Voltage
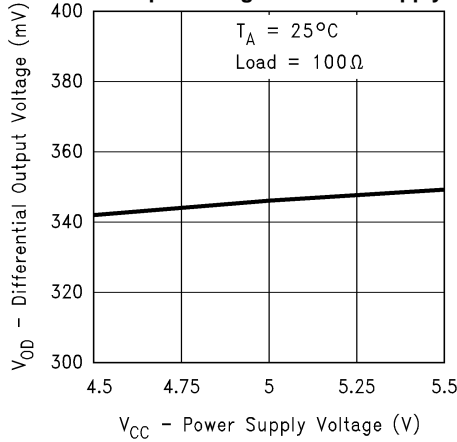

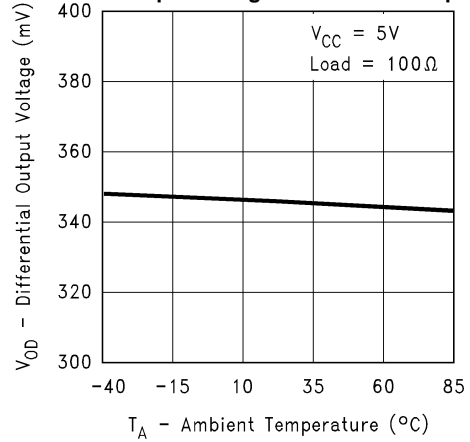**Figure 14.**

Differential Output Voltage vs Ambient Temperature

Figure 15.

Output Voltage High vs Power Supply Voltage
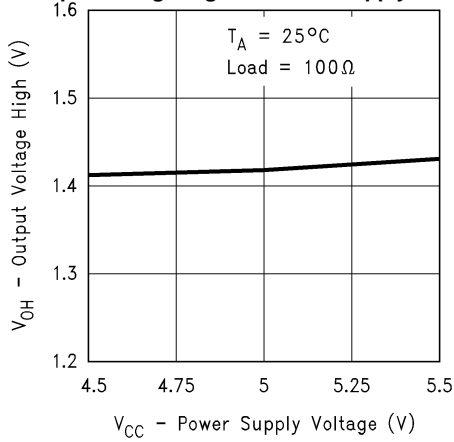

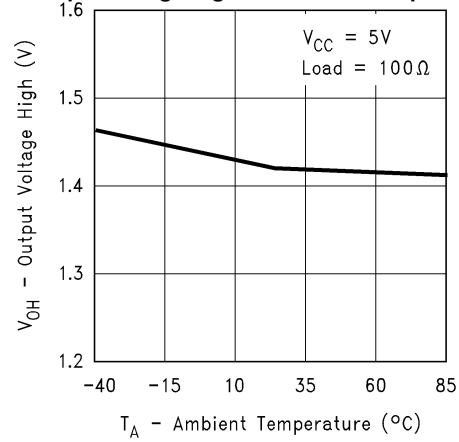**Figure 16.**

Output Voltage High vs Ambient Temperature
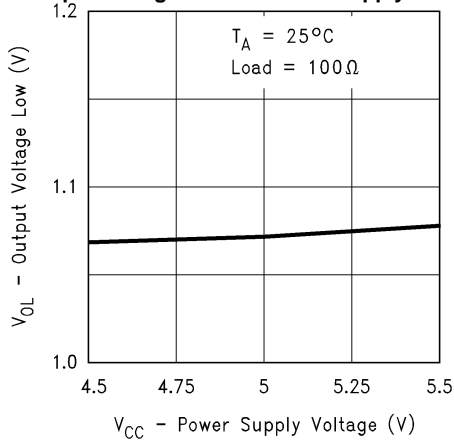

Figure 17.

Output Voltage Low vs Power Supply Voltage

Figure 18.

Output Voltage Low vs Ambient Temperature
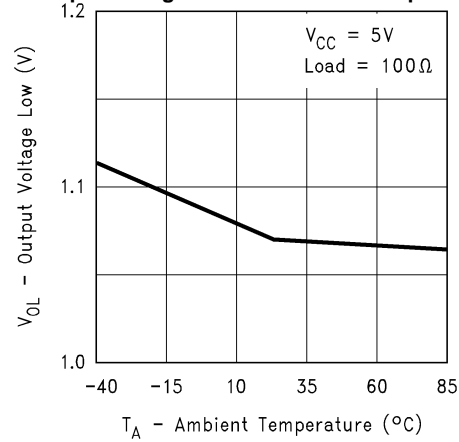
Figure 19.
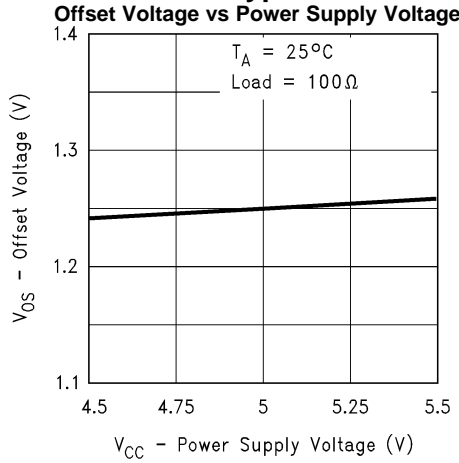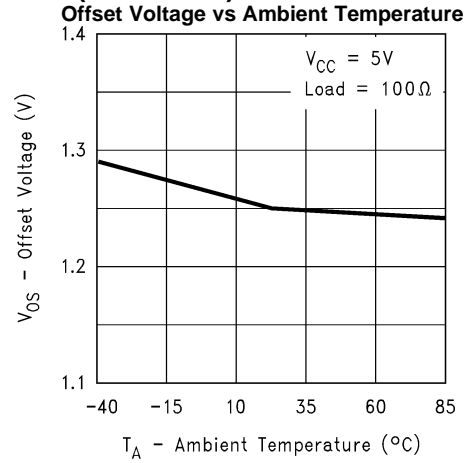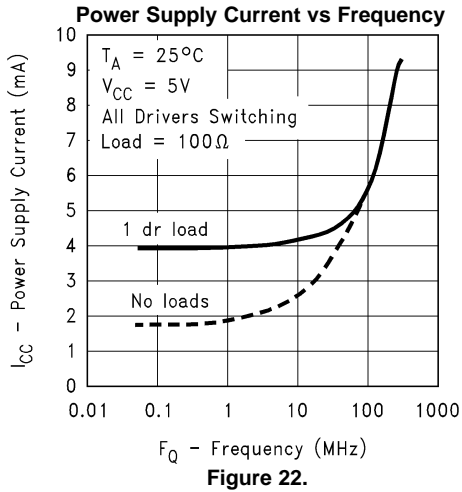
Product Folder Links: *DS90C031QML*

Typical Performance Characteristics (continued)

Offset Voltage vs Power Supply Voltage

Figure 20.

Offset Voltage vs Ambient Temperature

Figure 21.

Power Supply Current vs Frequency

Figure 22.

Power Supply Current vs Frequency

Figure 23.

Differential Output Voltage vs Load Resistor

Figure 24.

Differential Propagation Delay vs Power Supply Voltage

Figure 25.

Product Folder Links: *DS90C031QML*
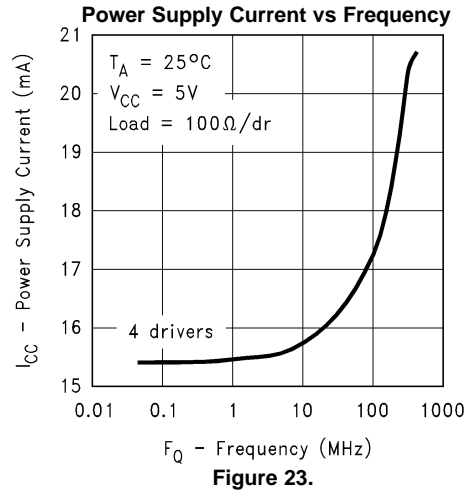
Typical Performance Characteristics (continued)

Differential Propagation Delay vs Ambient Temperature

Figure 26.

Differential Skew vs Power Supply Voltage

Figure 27.

Differential Skew vs Ambient Temperature

Figure 28.

Differential Transition Time vs Power Supply Voltage

Figure 29.

Differential Transition Time vs Ambient Temperature

Figure 30.

TYPICAL APPLICATION

Figure 31. Point-to-Point Application

APPLICATIONS INFORMATION

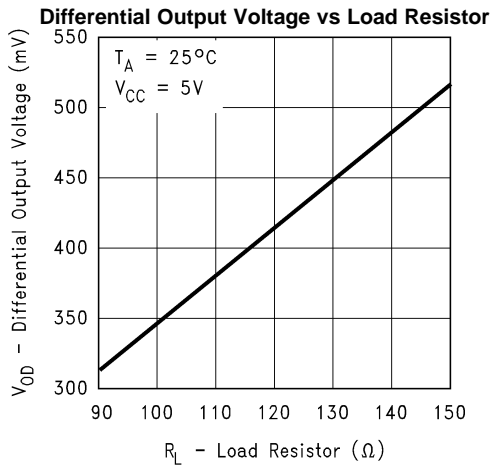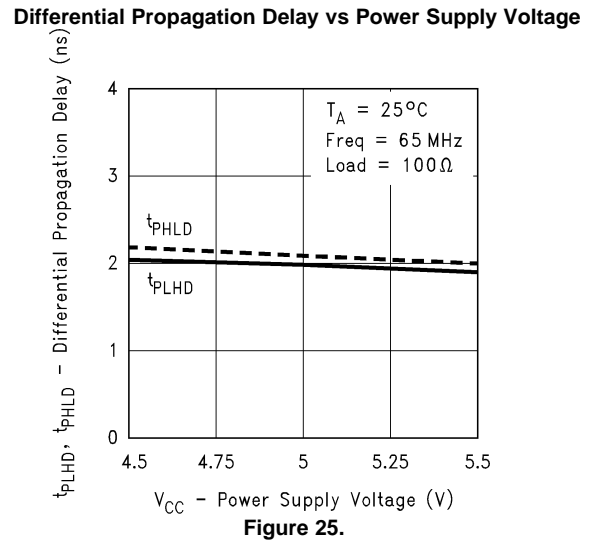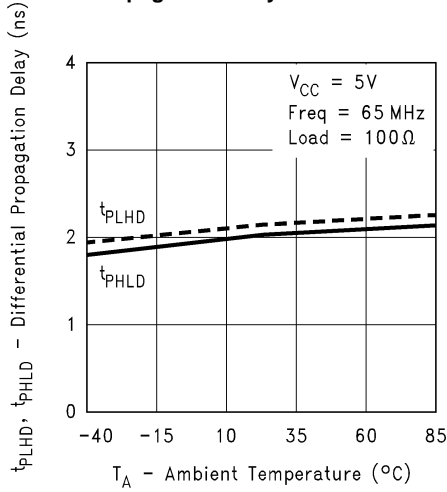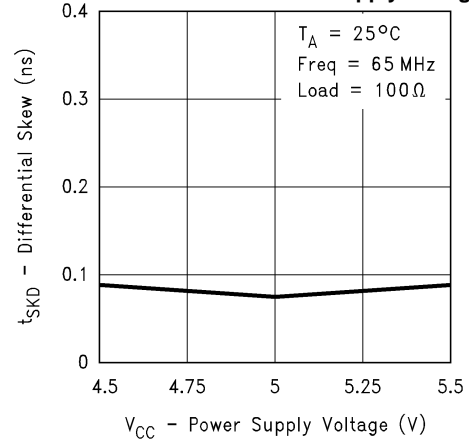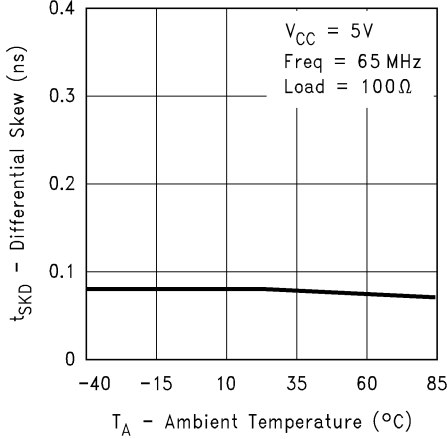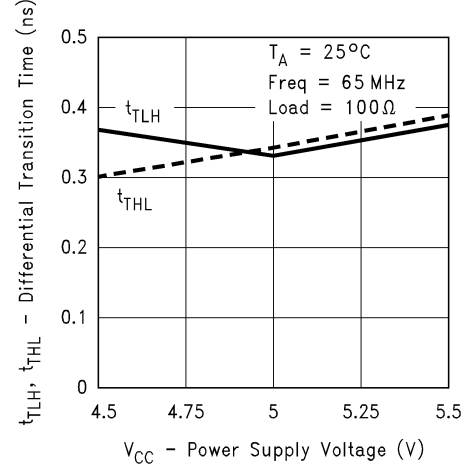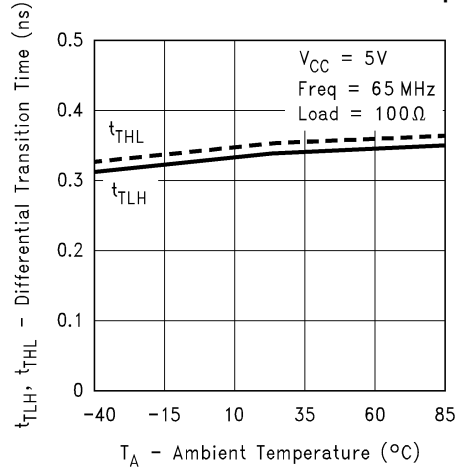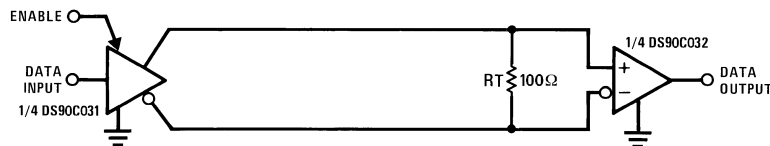LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 31. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C031differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 31. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV − 100 mV = 240 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 32. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required. The LVDS outputs are high impedance under power-off condition. This allows for multiple or redundant drivers to be used in certain applications.

The footprint of the DS90C031 is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.
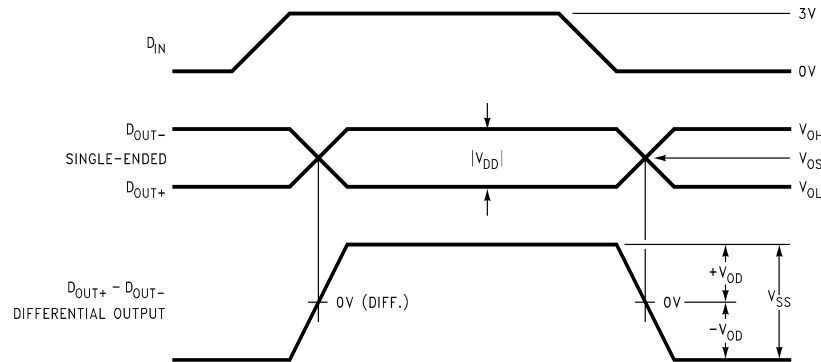
Figure 32. Driver Output Levels

Pin Descriptions

Pin No. (SOIC)	Name	Description
1, 7, 9, 15	D_I	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{O+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	$D_{O–}$	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	Gnd	Ground pin

Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883G, Test Method 1019.7, Condition A and the "Extended room temperature anneal test" described in section 3.11 for application environment dose rates less than 0.16 rad(Si)/s. Wafer level TID data is available with lot shipments.

Single Event Latch-Up

One time single event latch-up (SEL) testing was preformed showing SEL immunity to 103 MeV-cm^2/mg. A test report is available upon request.

Single Event Upset

Single event upset (SEU) data are available upon request.

REVISION HISTORY

Released	Revision	Section	Changes
03/01/06	New	New Release, Corporate format	1 MDS data sheet converted into Corp. data sheet format. MNDS90C031-X-RH Rev 2A1 will be archived.
10/12/2010	A	Features, Ordering Table, Absolute Maximum Ratings, Applications Information	Added reference to Radiation and Fail safe. Removed reference to EOL NSID, Output Voltage changed limit from −0.3V to (V_{CC} + 0.3V) to −0.3V to +5.8V, Added paragraph to Applications Information section and New Radiation Environment section. Revision A will be Archived.
03/04/2013	B	All	Changed layout of National Data Sheet to TI format.

Product Folder Links: *DS90C031QML*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9583301Q2A	ACTIVE	LCCC	NAJ	20	50	TBD	Call TI	Call TI	-55 to 125	DS90C031E -QML Q 5962-95833 01Q2A ACO 01Q2A >T	Samples
5962-9583301VFA	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 125	DS90C031W- QMLV Q 5962-95833 01VFA ACO 01VFA >T	Samples
5962R9583301VFA	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 125	DS90C031WR QMLV Q 5962R95833 01VFA ACO 01VFA >T	Samples
5962R9583301VZA	ACTIVE	CFP	NAC	16	42	TBD	Call TI	Call TI	-55 to 125	DS90C031WGR QMLV Q 5962R95833 01VZA ACO 01VZA >T	Samples
DS90C031 MDR	ACTIVE	DIESALE	Y	0	28	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
DS90C031E-QML	ACTIVE	LCCC	NAJ	20	50	TBD	Call TI	Call TI	-55 to 125	DS90C031E -QML Q 5962-95833 01Q2A ACO 01Q2A >T	Samples
DS90C031W-QMLV	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 125	DS90C031W- QMLV Q 5962-95833 01VFA ACO 01VFA >T	Samples
DS90C031WGRQMLV	ACTIVE	CFP	NAC	16	42	TBD	Call TI	Call TI	-55 to 125	DS90C031WGR QMLV Q 5962R95833 01VZA ACO 01VZA >T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C031WRQMLV	ACTIVE	CFP	NAD	16	19	TBD	Call TI	Call TI	-55 to 125	DS90C031WR QMLV Q 5962R95833 01VFA ACO 01VFA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DS90C031QML, DS90C031QML-SP :

● Military: DS90C031QML

● Space: DS90C031QML-SP

NOTE: Qualified Version Definitions:

● Military - QML certified for Military and Defense Applications

● Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NAD0016A

.074 +.006 −.024

.045
.026

.39 MAX

.000 MIN TYP

16   9

8X
.32±.01

.3 MAX
GLASS

.250 +.025 −.005

PIN #1 ID
NOTE 3

8X
.32±.01

1   8

.006±.002 TYP
NOTE 2

.010±.002

16X .017±.002
NOTE 2

14X .050±.005

DIMENSIONS ARE IN INCHES

W16A (Rev T)

NAC0016A

.010±.002
[0.25±0.05]

LEAD 1 ID
NOTE 3

SUPPLIER OPTION
NOTE 3

.00 MIN TYP
[0.0]

.018 MAX TYP
[0.46]

1   16

.390 MAX
[9.91]

14X .050±.002
[1.27±0.05]

16X .017±.002
[0.43±0.05]

8   9

.250 +.020 -.005
[6.35 +0.50 -0.12]

.410±.010
[10.41±0.25]

.070 +.010 -.020
[1.78 +0.25 -0.50]

.008±.004 TYP
[0.2±0.1]

SEE DETAIL A

.004 [0.1]

SEATING PLANE

.006±.002 TYP
[0.15±0.05]

R.015±.002
[0.38±0.05]

0° - 4°

.040±.003
[1.02±0.07]

**MIL-PRF-38535
CONFIGURATION CONTROL**

DETAIL A
TYPICAL

WG16A (RevG)

NAJ0020A

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

IMPORTANT NOTICE

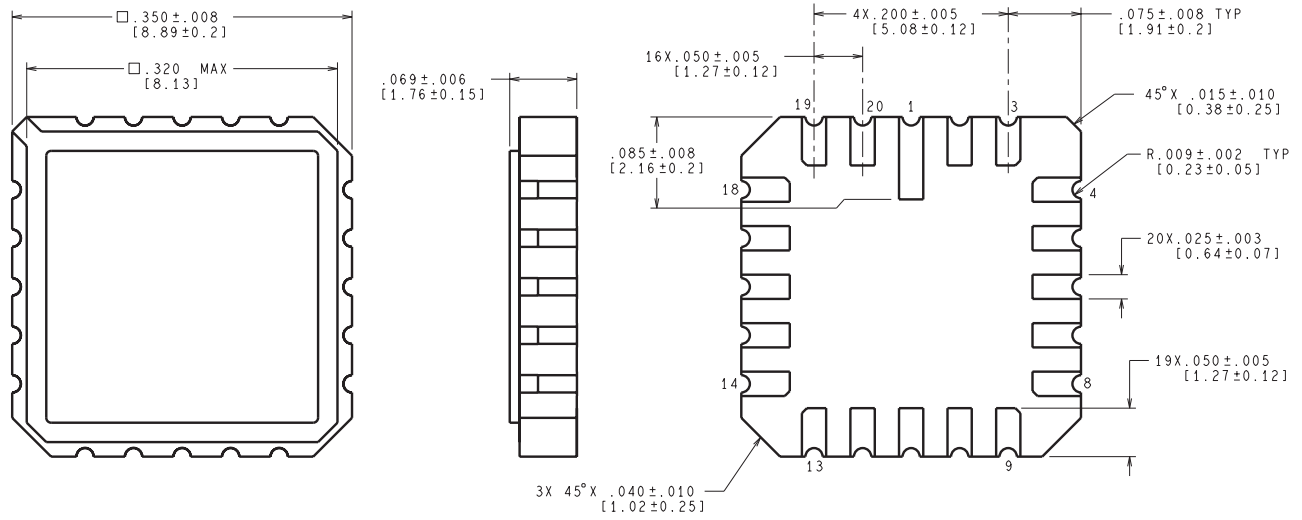Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

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