

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
G	Convert to SMD format. Add vendor CAGE 01295. Add device types 03 and 04.	87-07-28	M. A. Frye
H	Convert to one part-one part number format. Technical changes to 1.3, 4.2, and tables I and II. Add device type 05. Add vendor CAGE 18324 and 27014. Add figures 2 and 3.	91-07-05	M. A. Frye
J	Changes in accordance with N.O.R. 5962-R061-92.	91-11-22	M. L. Poelking
K	Redrawn with changes. Add device type 06.	95-10-31	M. A. Frye
L	Changes in accordance with N.O.R. 5962-R089-96.	96-03-28	M. A. Frye
M	Redrawn with changes to table I for device type 05. - drw	97-10-14	R. Monnin
N	Add radiation hardened information. - drw	99-05-25	R. Monnin
P	Make changes to 3.1, 3.5.1, and 6.6.3. - ro	00-02-15	R. Monnin
R	Add radiation hardness assurance level R devices. - ro	00-08-08	R. Monnin
T	Add case outline Z. - ro	01-05-03	R. Monnin
U	Make a change to 6.6.3 and footnote 3/ as specified under the BULLETIN SHEET. - ro	07-07-17	R. Heber
V	Add device type 07. Editorial changes throughout. - drw	10-03-03	Charles F. Saffle

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

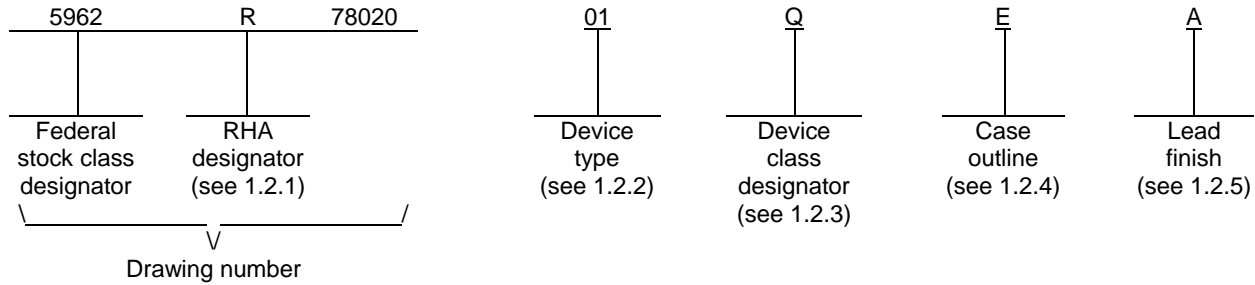
REV																				
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REV STATUS OF SHEETS	REV			V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Monica L. Poelking	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsc.dla.mil</p> <p align="center">MICROCIRCUIT, LINEAR, QUAD DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON</p>																	
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Charles E. Besore																		
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 79-01-26																		
REVISION LEVEL V	SIZE A	CAGE CODE 14933	78020																
SHEET		1 OF 17																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	26LS32	Quad, differential line receiver <u>1/</u>
02	26LS33	Quad, differential line receiver <u>2/</u>
03	26LS32A	Quad, differential line receiver <u>1/</u>
04	26LS33A	Quad, differential line receiver <u>2/</u>
05	26F32	Quad, differential line receiver <u>1/</u>
06	26LS32	Quad, differential line receiver <u>1/</u>
07	26LS33A	Quad, differential line receiver <u>2/</u>

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
Z	GDFP1-G16	16	Flat pack with gullwing leads
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

- 1/ Input voltage range (differential or common mode) ± 7 V. Input sensitivity 200 mV.
- 2/ Input voltage range (differential or common mode) ± 15 V. Input sensitivity 500 mV.

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1.3 Absolute maximum ratings. 3/

Power supply voltage (V_{CC})	7.0 V dc	
Common mode range	± 25 V dc	
Differential input voltage	± 25 V dc	
Enable voltage	7.0 V dc	
Output sink current	50 mA	
Storage temperature range	-65°C to +150°C	
Power dissipation (P_D)	500 mW 4/	
Lead temperature (soldering, 10 seconds)	+300°C	
Junction temperature (T_J)	+150°C	
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835	
Thermal resistance, junction-to-ambient (θ_{JA}):	Device types	Device type
	<u>01-04, 06, 07</u>	<u>05</u>
Case outline E	100°C/W	100°C/W
Case outlines F and Z	140°C/W	142°C/W
Case outline 2	130°C/W	87°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Input hysteresis (V_{HYST})	50 mV typical
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rads (Si)/s) 100 Krads(Si) 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ Must withstand the added P_D due to short circuit test, e.g., I_{OS} .

5/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 53 (see MIL-PRF-38535, appendix A).

3.11 PIN supersession information. The PIN supersession information shall be as specified in the appendix.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential input voltage sensitivity	V _{TH}	V _{OUT} = V _{OL} or V _{OH} , -7 V ≤ V _{CM} ≤ +7 V	1, 2, 3	01,03, 05,06	-0.2	+0.2	V
		M,D,P,L,R	1	05	-0.2	+0.2	
		V _{OUT} = V _{OL} or V _{OH} , -15 V ≤ V _{CM} ≤ +15 V	1, 2, 3	02,04, 07	-0.5	+0.5	
Input resistance <u>3/</u>	R _{IN}	-15 V ≤ V _{CM} ≤ +15 V (one input ac ground)	4, 5, 6	01,02 06	6.0		kΩ
				03,04, 07	12.0		
				05	14.0		
Input current (under test)	I _{IN}	V _{IN} = +15 V, (other input -15 V ≤ V _{IN} ≤ 15 V)	1, 2, 3	01,02, 05,06		2.3	mA
			M,D,P,L,R	1	05		
		V _{IN} = -15 V, (other input -15 V ≤ V _{IN} ≤ 15 V)	1, 2, 3	01,02, 05,06		-2.8	
			M,D,P,L,R	1	05		
		V _{IN} = +15 V, (other input -10 V ≤ V _{IN} ≤ 15 V)	1, 2, 3	03,04		2.3	
			07			1.2	
		V _{IN} = -15 V, (other input -15 V ≤ V _{IN} ≤ 10 V)	1, 2, 3	03,04		-2.8	
			07			-1.7	
Output high voltage (3006)	V _{OH}	V _{CC} = 4.5 V, ΔV _{IN} = 1.0 V, V _{ENABLE} = 0.8 V, I _{OH} = -440 μA	1, 2, 3	All	2.5		V
			M,D,P,L,R	1	05	2.5	
Output low voltage (3007)	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{ENABLE} = 0.8 V, ΔV _{IN} = -1.0 V	1, 2, 3	All		0.4	V
			M,D,P,L,R	1	05		
		V _{CC} = 4.5 V, I _{OL} = 8.0 mA, V _{ENABLE} = 0.8 V, ΔV _{IN} = -1.0 V	1, 2, 3	All		0.45	
			M,D,P,L,R	1	05		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Enable low voltage	V _{IL}	V _{CC} = 5.5 V <u>4/</u>	1, 2, 3	All		0.8	V	
Enable high voltage	V _{IH}	V _{CC} = 4.5 V <u>4/</u>	1, 2, 3	All	2.0		V	
Enable clamp voltage (3022)	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA <u>4/</u> V _{CC} = 5.5 V	1, 2, 3	All		-1.5	V	
Off-state (high impedance) output output current (3021)	I _O	V _{CC} = 5.5 V, V _O = 2.4 V	1, 2, 3	All		20	μA	
			M,D,P,L,R	1	05	20		
		V _{CC} = 5.5 V, V _O = 0.4 V	1, 2, 3	All		-20		
			M,D,P,L,R	1	05	-20		
Enable low current (3009)	I _{IL}	V _{IN} = 0.4 V, V _{CC} = 5.5 V <u>5/</u>	1, 2, 3	All		-0.36	mA	
Enable high current sensitivity (3010)	I _{IH}	V _{IN} = 2.7 V, V _{CC} = 5.5 V <u>5/</u>	1, 2, 3	All		20	μA	
Output short circuit current (3011)	I _{OS}	V _O = 0 V, V _{CC} = 5.5 V, <u>6/</u> ΔV _{IN} = 1.0 V	1, 2, 3	All	-15	-85	mA	
Supply current (3005)	I _{CC}	V _{CC} = 5.5 V, data inputs = GND, outputs disabled	1, 2, 3	01-04, 06,07		70	mA	
				05		50		
			M,D,P,L,R	1	05	50		
Enable input high current	I _I	V _{IN} = 5.5 V, V _{CC} = 5.5 V <u>5/</u>	1, 2, 3	01-04, 06,07		100	μA	
				05	-10	50		
Propagation delay, input to output (3003)	t _{PLH}	V _{CC} = 5.0 V, C _L = 15 pF, see figure 2	9	01,02		25	ns	
			10, 11			38		
			9	03,04,		35		
			10, 11		07	53		
				05	9			23
					10, 11			31

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit				
					Min	Max					
Propagation delay, input to output (3003)	t _{PLH}	V _{CC} = 5.0 V, C _L = 15 pF, see figure 2	9	05		22	ns				
			10, 11	<u>7/</u>		30					
			9, 11	06		30					
			10			120					
	t _{PHL}		9	01,02		25					
			10, 11			38					
			9	03,04,		35					
			10, 11	07		53					
			C _L = 50 pF	9	05			23			
				10, 11				31			
				9	05			22			
				10, 11	<u>7/</u>			30			
			9, 11	06		30					
			10			120					
			Output disable time, ENABLE to output (3003)	t _{PLZ}	V _{CC} = 5.0 V, C _L = 5 pF, see figure 2	9		01,02		30	ns
						10, 11				45	
9	03,04,					40					
10, 11	07					60					
C _L = 50 pF	9	05					30				
	10, 11						42				
9	05					18					
10, 11	<u>7/</u>					30					
9	06					34					
10						64					
11						27					

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit				
					Min	Max					
Output disable time, ENABLE to output (3003)	t _{PHZ}	V _{CC} = 5.0 V, C _L = 5 pF, see figure 2	9	01,02		22	ns				
			10, 11			33					
			9	03,04, 07		30					
			10, 11			45					
			C _L = 50 pF		9	05			55		
					10, 11				62		
					9	05			20		
					10, 11			<u>7/</u>		27	
					9, 11	06			32		
					10				35		
			Output enable time, ENABLE to output (3003)	t _{PZL}	V _{CC} = 5.0 V, C _L = 15 pF, see figure 2	9		01,02		22	ns
						10, 11				33	
9	03,04, 07					25					
10, 11						38					
C _L = 50 pF		9				05		20			
		10, 11						29			
		9				05		18			
		10, 11					<u>7/</u>		27		
		9				06		34			
		10						65			
		11						27			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Output enable time, ENABLE to output (3003)	t _{PZH}	V _{CC} = 5.0 V, C _L = 15 pF, see figure 2	9	01,02		22	ns	
			10, 11			33		
			9	03,04, 07		25		
			10, 11			38		
			C _L = 50 pF	9	05			18
				10, 11				29
				9	05			16
				10, 11		<u>7/</u>		
				9,11	06			35
				10				65

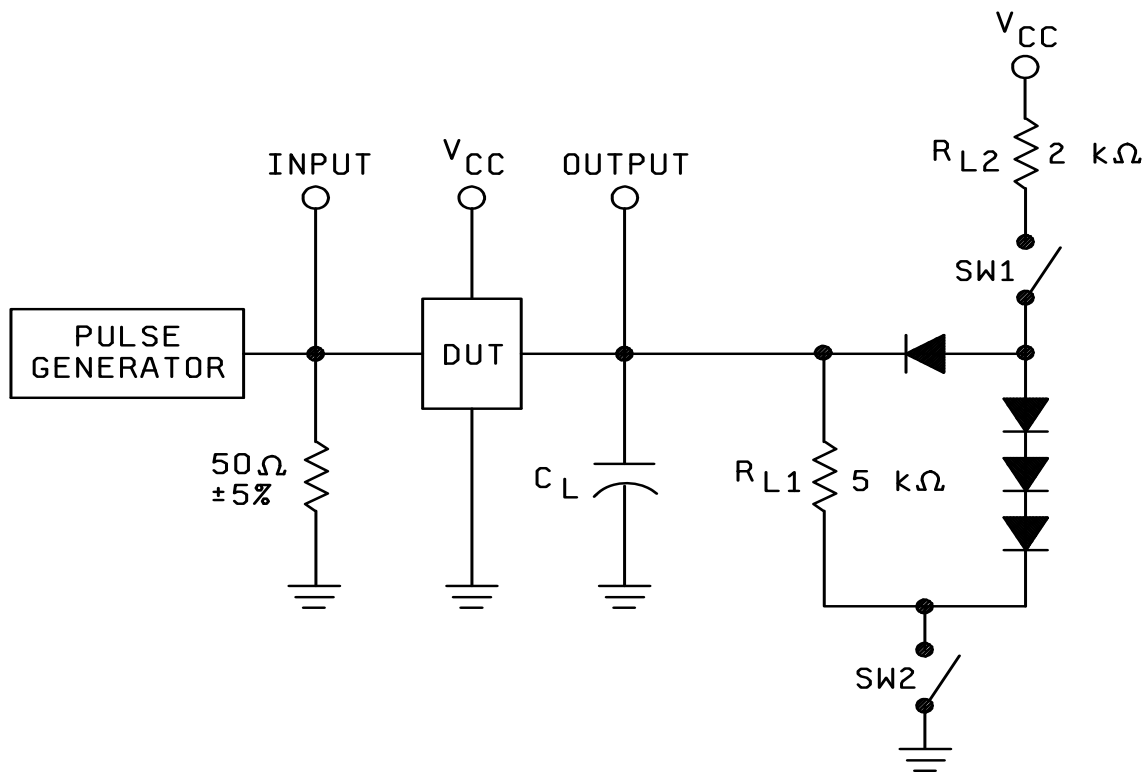
- 1/ Devices supplied to this drawing will meet all levels M, D, P, L, R of irradiation. However, this device is only tested at the 'R' level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 2/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
- 3/ Guaranteed by design.
- 4/ The V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for the V_{OL} and V_{OH} tests.
- 5/ These limits are not tested. The limits specified for the input low current represent the numerical range in which this parameter will pass: -0.36 to +0.10.
- 6/ Not more than output should be shorted at one time and the duration of the short circuit condition should not exceed one second.
- 7/ This parameter is guaranteed by correlation to the testing at C_L = 50 pF.

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Case outlines	2	E, F, Z
Device types	All	
Terminal number	Terminal symbol	
1	NC	INPUT A-
2	INPUT A-	INPUT A+
3	INPUT A+	OUTPUT A
4	OUTPUT A	ENABLE
5	ENABLE	OUTPUT C
6	NC	INPUT C+
7	OUTPUT C	INPUT C-
8	INPUT C+	GND
9	INPUT C-	INPUT D-
10	GND	INPUT D+
11	NC	OUTPUT D
12	INPUT D-	$\overline{\text{ENABLE}}$
13	INPUT D+	OUTPUT B
14	OUTPUT D	INPUT B+
15	$\overline{\text{ENABLE}}$	INPUT B-
16	NC	V _{CC}
17	OUTPUT B	---
18	INPUT B+	---
19	INPUT B-	---
20	V _{CC}	---

FIGURE 1. Terminal connections.

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Switch matrix		
Parameter	SW1	SW2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

NOTES:

1. Pulse generator, rate ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns.
2. All diodes, 1N916 or 1N3064

FIGURE 2. Test circuit and switching waveforms.

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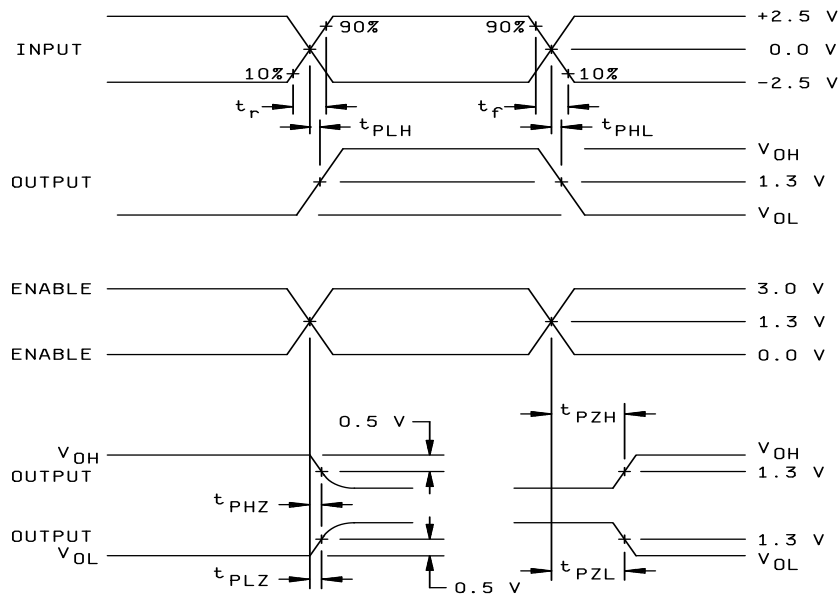
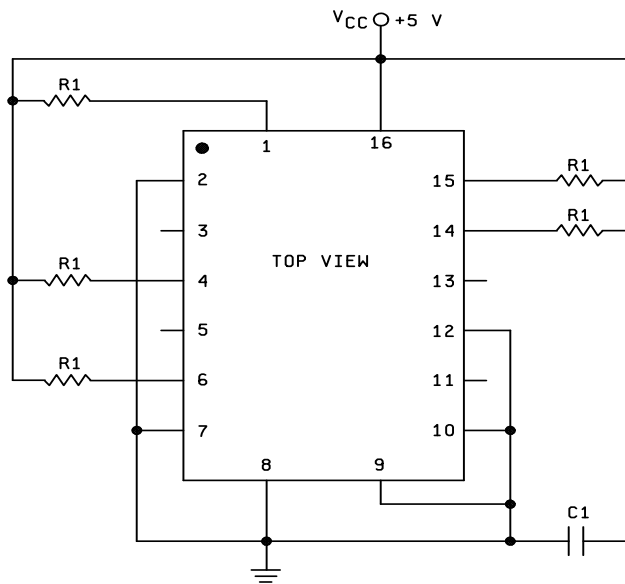


FIGURE 2. Test circuit and switching waveforms – continued.



$C_1 = 0.1 \mu\text{F}$
 $R_1 = 1 \text{ k}\Omega, 1/4 \text{ W}$

FIGURE 3. Radiation exposure circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, <u>3/</u> 9, 10, 11	1, 2, 3, 4, 5, 6, 9,10,11	1, 2, 3, 4, 5, 6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and delta limits. Delta limits shall be in accordance with table IIB and shall be computed with reference to the previous interim electrical parameters.

3/ Subgroups 4, 5, 6, 10, and 11, if not tested, shall be guaranteed to the specified limits in table I.

TABLE IIB. Delta limits at +25°C.

Parameter <u>1/</u>	Device type	Limit
V _{OH}	All	≤ 250 mV
V _{OL}	All	≤ 45 mV
I _{IN}	All	≤ 0.28 mA

1/ These parameters shall be read and recorded at T_A = +25°C before and after each burn-in and shall not change by more than the limits indicated. The delta rejects shall be included in the PDA calculation.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.6.3 Caution to designers. Device type 01 (26LS32) previously supplied by vendor 27014 (National Semiconductor) through June 1984, was manufactured without a failsafe input/output design (output is always high when inputs are open). All other vendors supplying device type 01 have the failsafe input/output design.

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APPENDIX

10. SCOPE

10.1 Scope. This appendix contains the PIN supersession information to support the one part - one part number system. For new system designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing system designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN supersession data shall be as specified in 30.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SUPERSESSION DATA

<u>New PIN</u>	<u>Old PIN</u>
5962-7802001MEX	7802001EX
5962-7802001MFX	7802001FX
5962-7802001M2X	78020012X
5962-7802002MEX	7802002EX
5962-7802002MFX	7802002FX
5962-7802002M2X	78020022X
5962-7802003MEX	7802003EX
5962-7802003MFX	7802003FX
5962-7802003M2X	78020032X
5962-7802004MEX	7802004EX
5962-7802004MFX	7802004FX
5962-7802004M2X	78020042X

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Approved sources of supply for SMD 78020 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-7802001MEA <u>3</u> /	0C7V7	QP26LS32/BEA
	3V146	26LS32/BEA
5962-7802001MFA <u>3</u> /	0C7V7	QP26LS32/BFA
	3V146	26LS32/BFA
5962-7802001M2A <u>3</u> /	0C7V7	QP26LS32/B2A
	3V146	26LS32B2A
5962-7802002MEA	0C7V7	QP26LS33/BEA
	3V146	26LS33/BEA
5962-7802002MFA	0C7V7	QP26LS33/BFA
	3V146	26LS33/BFA
5962-7802002M2A	0C7V7	QP26LS33/B2A
	3V146	26LS33/B2A
5962-7802003MEA	01295	AM26LS32AMJB
5962-7802003MFA	01295	AM26LS32AMWB
5962-7802003M2A	01295	AM26LS32AMFKB
5962-7802004MEA	01295	AM26LS33AMJB
5962-7802004MFA	01295	AM26LS33AMWB
5962-7802004M2A	01295	AM26LS33AMFKB
5962-7802005MEA	<u>4</u> /	DS26F32MJ/883
5962-7802005MFA	27014	DS26F32MW/883
5962-7802005MZA	<u>4</u> /	DS26F32MWG/883
5962-7802005M2A	27014	DS26F32ME/883

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Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-7802005VEA	<u>4</u> /	DS26F32MJ-QMLV
5962-7802005VFA	<u>4</u> /	DS26F32MW-QMLV
5962-7802005VZA	<u>4</u> /	DS26F32MWG-QMLV
5962-7802006QEA	27014	DS26LS32MJ/883
5962-7802006QFA	<u>4</u> /	DS26LS32MW/883
5962-7802006Q2A	<u>4</u> /	DS26LS32ME/883
5962F7802005Q2A	<u>4</u> /	DS26F32MEF-QML
5962F7802005QEA	<u>4</u> /	DS26F32MJF-QML
5962F7802005QFA	<u>4</u> /	DS26F32MWF-QML
5962F7802005VEA	<u>4</u> /	DS26F32MJFQMLV
5962F7802005VFA	<u>4</u> /	DS26F32MWFQMLV
5962R7802005Q2A	<u>4</u> /	DS26F32MER-QML
5962R7802005QEA	<u>4</u> /	DS26F32MJR-QML
5962R7802005QFA	<u>4</u> /	DS26F32MWR-QML
5962R7802005VEA	27014	DS26F32MJRQMLV
5962R7802005VFA	27014	DS26F32MWRQMLV
5962R7802005VZA	<u>4</u> /	DS26F32MWGRQMLV
5962-7802007VEA	01295	AM26LS33A-SP

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ **Caution.** The device type 01 previously supplied by vendor 27014 (National Semiconductor) through June 1984, was manufactured without a failsafe input/output design (output always high when inputs are open). All other vendors supplying device type 01 have the failsafe input/output design.
- 4/ Not available from an approved source of supply.

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DATE: 10-03-03

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.