

漂移电压基准

 查询样品: [REF3325-DIE](#)

特性

- 低电源电流
- 高输出电流
- 低温度漂移
- 高初始精度

应用范围

- 便携式设备
- 数据采集系统
- 医疗设备
- 测试设备

说明

REF3325 是一款低功耗、高精度、低压降电压基准。小尺寸和低功耗使 REF3325 成为多种便携式和电池供电类应用的理想选择。

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	PACKAGE QUANTITY
REF3325	TD	Bare die in waffle pack	REF3325ATDD1	400
			REF3325ATDD2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Processing is per the Texas Instruments commercial production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Floating	TiW/AlCu (0.5%)	1100 nm

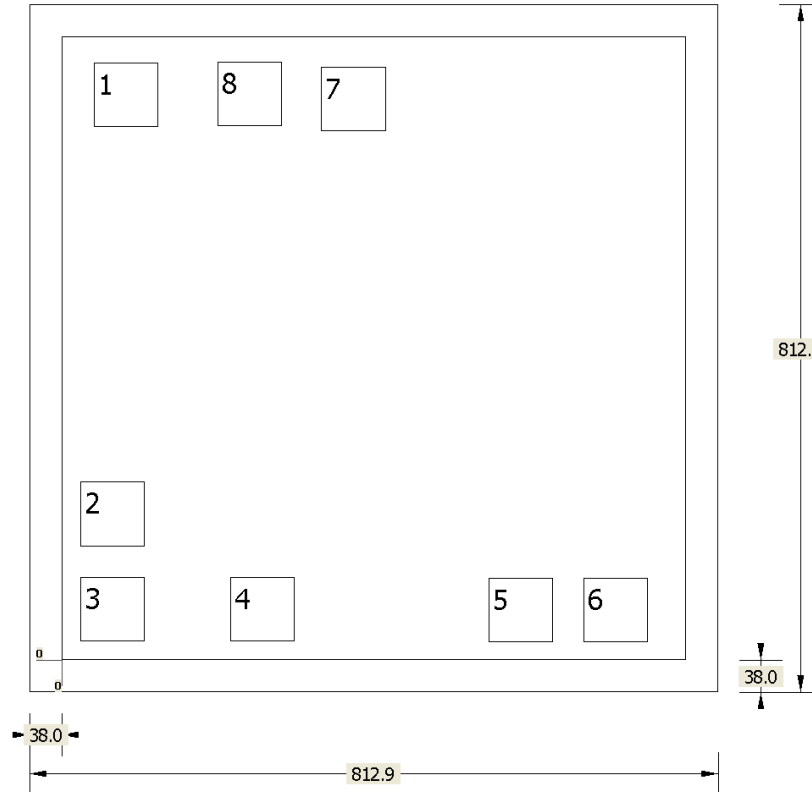


Table 1. Bond Pad Coordinates in Microns⁽¹⁾

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
IN	1	38	629.6	114	705.6
N/C	2	22	134.5	98.15	210.65
N/C	3	22	22.1	98.15	98.25
N/C	4	199.25	22.1	275.4	98.25
OUT	5	504.15	21.3	580.15	97.3
OUT	6	616.35	21.3	692.35	97.3
GND	7	306.4	625.1	382.55	701.25
GND	8	183.8	630.65	259.95	706.8

(1) Substrate N/C.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
REF3325ATDD1	ACTIVE			0	400	TBD	Call TI	N / A for Pkg Type	0 to 70		Samples
REF3325ATDD2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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