

电流模式脉宽调制 (PWM) 控制器

 查询样品: [UC1843-DIE](#)

特性

- 针对离线和直流至直流 (DC-DC) 转换器进行了优化
- 低启动电流
- 自动前馈补偿
- 逐脉冲电流限制
- 增强型负载响应特性
- 带有滞后功能的欠压闭锁
- 双脉冲抑制
- 高电流推挽式输出
- 低 R_o 误差放大器

说明

UC1843-DIE 使用最少的外部部件数量为离线或直流至直流定频电流模式控制系统配置的执行提供必要的特性。内部执行的电路包括欠压闭锁特性启动电流，确保锁存运行的逻辑电路，一个提供电流限制控制的 PWM 比较器，还有一个被设计用来灌入或吸收高峰值电流的推挽式输出级。当处于关闭状态时，适合驱动 N-通道金属氧化物半导体场效应晶体管 (MOSFET) 的输出级为低电平。

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
UC1843	TD	Bare die in waffle pack ⁽²⁾	UC1843TD1	154
			UC1843TD2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Processing is per the Texas Instruments commercial production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



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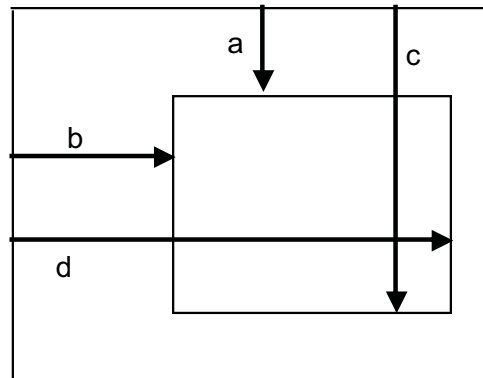


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	AlCu2%	2000 nm



Origin

Table 1. BOND PAD COORDINATES (in Mils)

DESCRIPTION	PAD NUMBER	a	b	c	d
COMP	1	78.70	63.40	82.90	67.60
V _{FB}	2	70.60	63.40	74.80	67.60
I _{SENSE}	3	39.40	63.40	43.60	67.60
R _T /C _T	4	18.60	61.20	22.60	65.60
GROUND	5	17.80	11.70	22.00	15.90
GROUND	6	17.40	3.90	21.80	8.10
OUTPUT	7	32.60	6.40	36.80	10.60
V _{CC}	8	47.50	6.40	51.70	10.60
V _{CC}	9	54.60	6.40	58.80	10.60
V _{REF}	10	68.70	6.40	72.90	10.60
NC	TESTPAD	87.10	6.30	90.80	10.30
NC	TESTPAD	87.10	12.60	90.80	16.60
NC	TESTPAD	87.10	18.00	90.80	22.00
NC	TESTPAD	87.10	24.30	90.80	28.30
NC	TESTPAD	87.10	30.60	90.80	34.60

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1843TD1	ACTIVE			0	154	TBD	Call TI	N / A for Pkg Type	25 to 25		Samples
UC1843TD2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1843-DIE :

- Space: [UC1843-SP](#)

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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