

LM118QML Operational Amplifier

Check for Samples: [LM118QML](#)

FEATURES

- 15 MHz Small Signal Bandwidth
- Ensured 50V/μs Slew Rate
- Maximum Bias Current of 250 nA
- Operates from Supplies of ±5V to ±20V
- Internal Frequency Compensation
- Input and Output Overload Protected
- Pin Compatible with General Purpose Op Amps

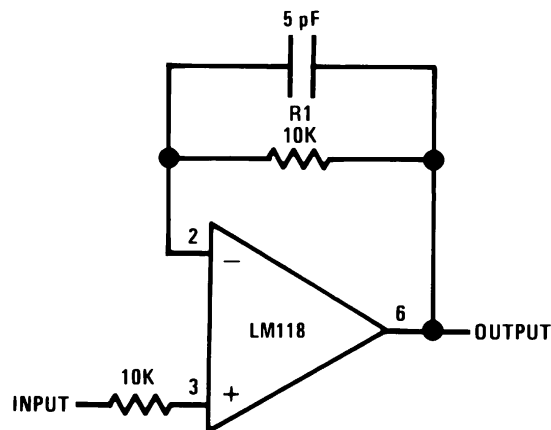
DESCRIPTION

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed forward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of this op amp makes it useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This device is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Fast Voltage Follower


Do not hard-wire as voltage follower ($R1 \geq 5 \text{ k}\Omega$)

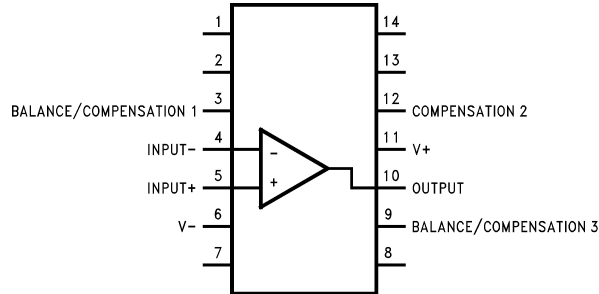

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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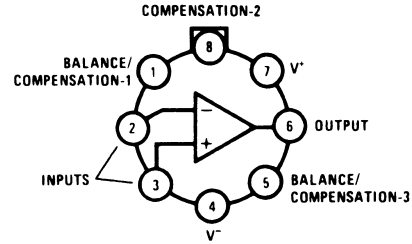


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

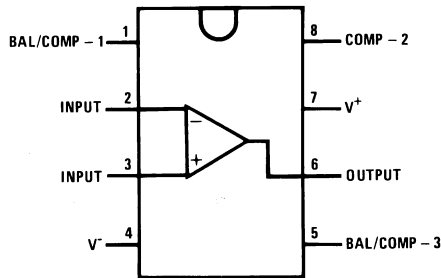
Connection Diagram



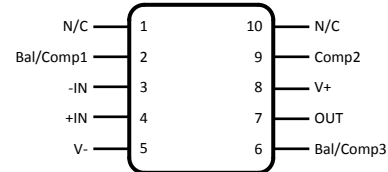
**Figure 1. CDIP Package
Top View
See Package Number J0014A**



**Figure 2. TO-99
Top View
See Package Number LMC**



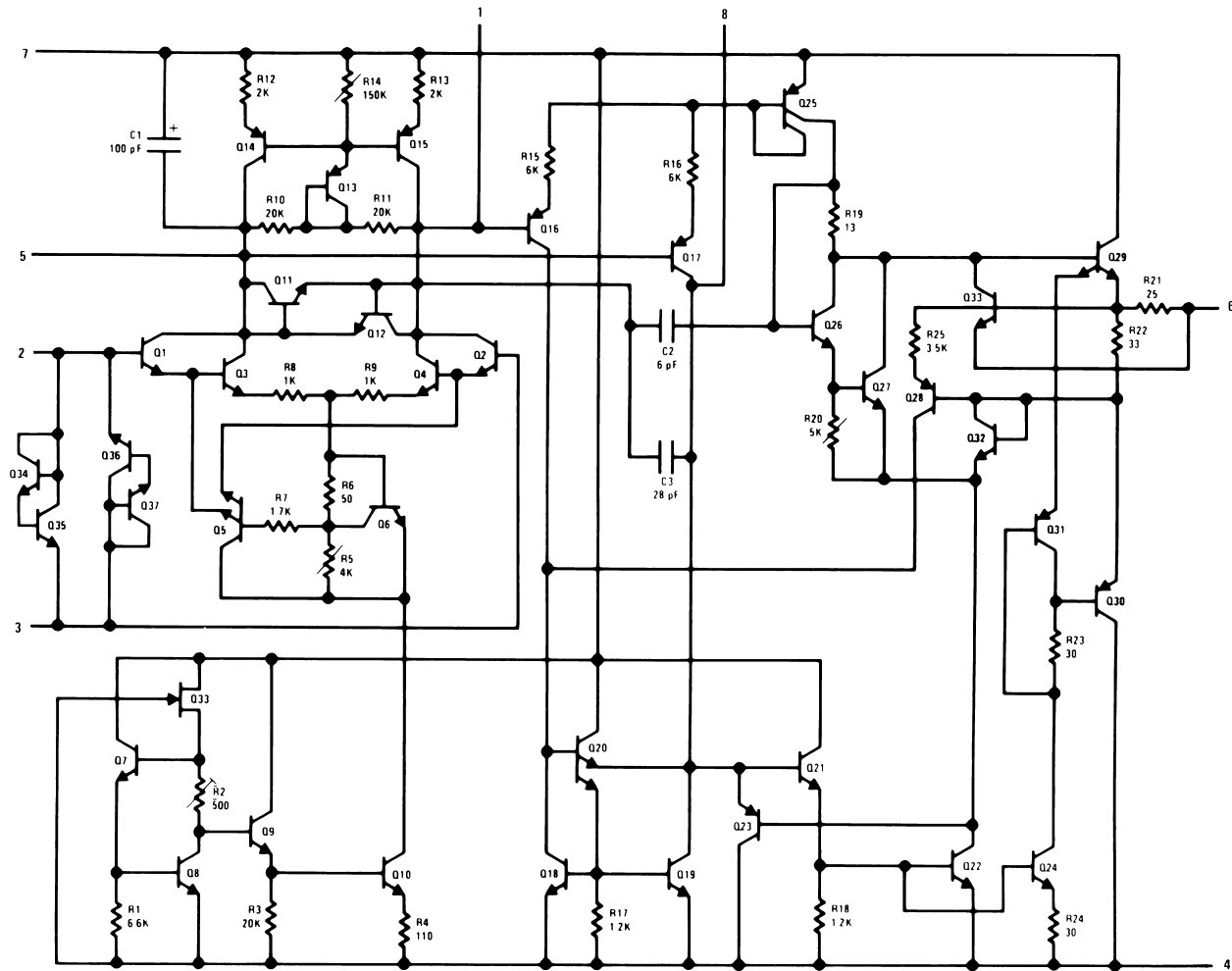
**Figure 3. CDIP Package
Top View
See Package Number NAB0008A**



Pin connections shown on schematic diagram and typical applications are for TO package.

**Figure 4. CLGA Package
Top View
See NS Package Number NAC0010A**

Schematic Diagram



Absolute Maximum Ratings⁽¹⁾

Supply Voltage		±20V	
Power Dissipation ⁽²⁾	8 LD TO-99	750mW	
	8LD CDIP	1000mW	
	14LD CDIP	1250mW	
	10LD CLGA	600mW	
Differential Input Current ⁽³⁾		±10 mA	
Input Voltage ⁽⁴⁾		±15V	
Output Short-Circuit Duration		Continuous	
Operating Temperature Range		-55°C ≤ T _A ≤ +125°C	
Thermal Resistance	θ _{JA}	8 LD TO-99 (Still Air @ 0.5W)	160°C/W
		8 LD TO-99 (500LF / Min Air flow @ 0.5W)	86°C/W
		8LD CDIP (Still Air @ 0.5W)	120°C/W
		8LD CDIP (500LF / Min Air flow @ 0.5W)	66°C/W
		14LD CDIP (Still Air @ 0.5W)	87°C/W
		14LD CDIP (500LF / Min Air flow @ 0.5W)	51°C/W
		10LD CLGA (Still Air @ 0.5W)	198°C/W
		10LD CLGA (500LF / Min Air flow @ 0.5W)	124°C/W
	θ _{JC}	8 LD TO-99	48°C/W
		8LD CDIP	17°C/W
		14LD CDIP	17°C/W
		10LD CLGA	22°C/W
Storage Temperature Range		-65°C ≤ T _A ≤ +150°C	
Lead Temperature (Soldering, 10 seconds)		300°C	
ESD Tolerance ⁽⁵⁾		2000V	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (3) The inputs are shunted with back-to-back diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
- (4) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- (5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005; Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM118/883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.

 DC $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$V_{CM} = \pm 11.5V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
		$V_{CC} = \pm 20V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
		$V_{CC} = \pm 20V$, $V_{CM} = \pm 15V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
I_{IO}	Input Offset Current	$V_{CM} = \pm 11.5V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
		$V_{CC} = \pm 20V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
		$V_{CC} = \pm 5V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
I_{IB}	Input Bias Current	$V_{CM} = \pm 11.5V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
		$V_{CC} = \pm 20V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
		$V_{CC} = \pm 5V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC} = 20V$ to $5V$, $R_S = 50\Omega$		70		dB	1, 2, 3
		$-V_{CC} = -20V$ to $-5V$, $R_S = 50\Omega$		70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	$V_{CC} = \pm 15V$, $V_{CM} = \pm 11.5V$, $R_S = 50\Omega$		80		dB	1, 2, 3
$+I_{OS}$	Short Circuit Current	$t < 25mS$		-65	-5.0	mA	1, 2, 3

LM118/883 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified.

DC $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$-I_{OS}$	Short Circuit Current	$t < 25mS$		5.0	65	mA	1, 2
				5.0	80	mA	3
I_{CC}	Power Supply Current	$V_{CC} = \pm 20V$			8.0	mA	1
					7.0	mA	2
					11	mA	3
$V_{IO\ adj.}$	Input Offset Voltage Adjust	$V_{CC} = \pm 20V$		4.0	-4.0	mV	1
R_I	Input Resistance		See ⁽¹⁾	1.0		M Ω	1
V_I	Input Voltage Range	$V_{CC} = \pm 15V$	See ⁽²⁾	-11.5	+11.5	V	1, 2, 3
A_{VS}	Large Signal Voltage Gain	$R_L = 2K\Omega$, $V_O = 0$ to $-10V$	See ⁽³⁾	50		V/mV	4
			See ⁽³⁾	25		V/mV	5, 6
		$R_L = 2K\Omega$, $V_O = 0$ to $+10V$	See ⁽³⁾	50		V/mV	4
			See ⁽³⁾	25		V/mV	5, 6
V_O	Output Voltage Swing	$R_L = 2K\Omega$		+12	-12	V	4, 5, 6

(1) Specified by design not tested

(2) Specified by CMRR

(3) Datalog in K = V/mV

LM118/883 Electrical Characteristics AC Parameters

The following conditions apply parameters, unless otherwise specified.

AC $V_{CC} = \pm 15V$, $V_{CM} = 0V$, $R_S = 0\Omega$, $R_L = 2K\Omega$, $C_L = 33pF$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
S_R	Slew Rate	$V_{CC} = \pm 20V$, $V_I = -5V$ to $+5V$, $A_V=1$		50		V/ μ S	7
		$V_{CC} = \pm 20V$, $V_I = +5V$ to $-5V$, $A_V=1$		50		V/ μ S	7

Typical Performance Characteristics

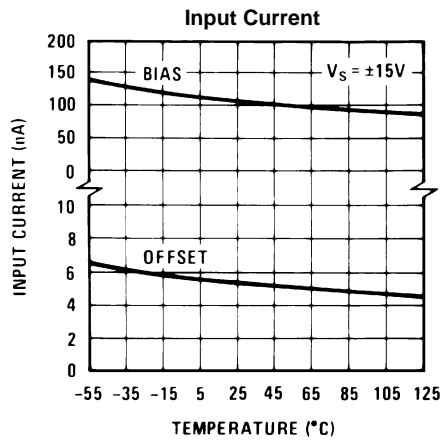


Figure 5.

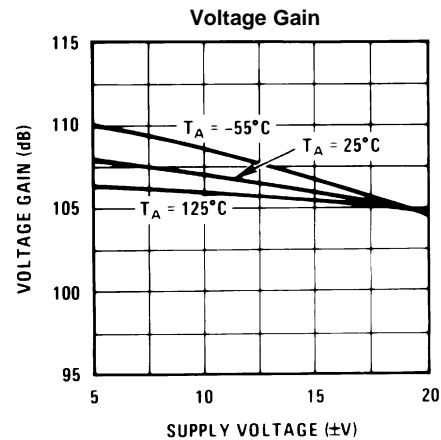


Figure 6.

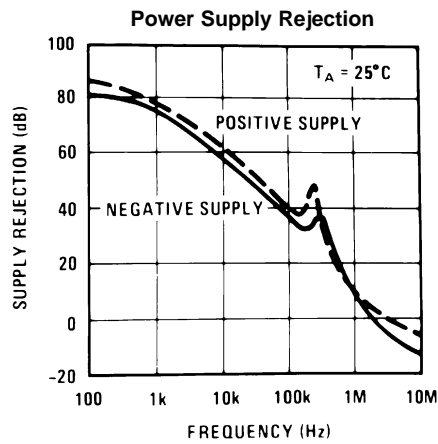


Figure 7.

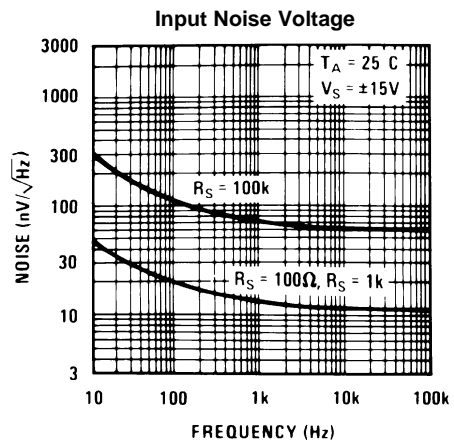


Figure 8.

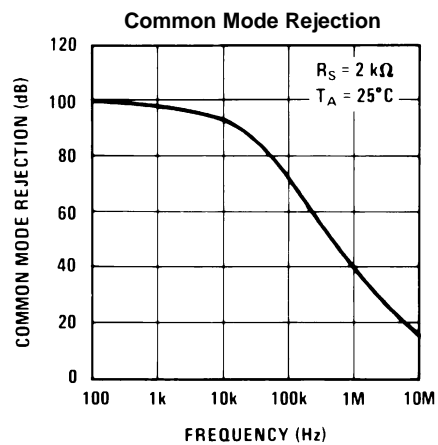


Figure 9.

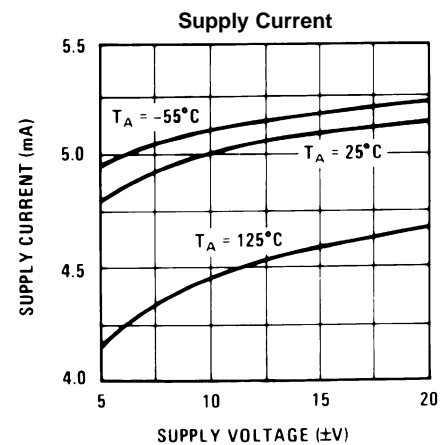


Figure 10.

Typical Performance Characteristics (continued)

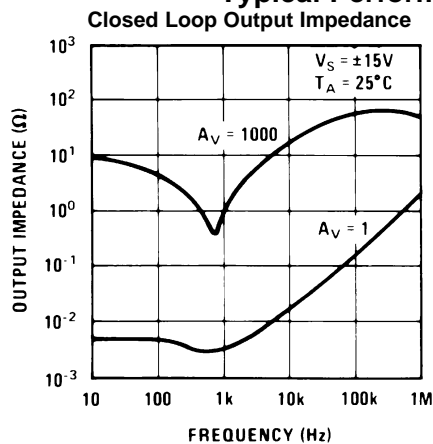


Figure 11.

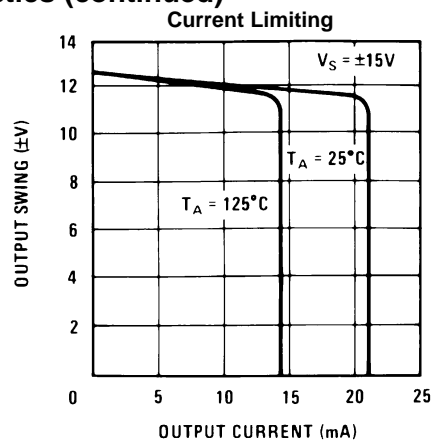


Figure 12.

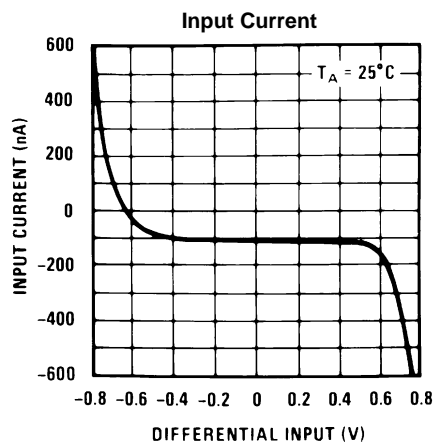


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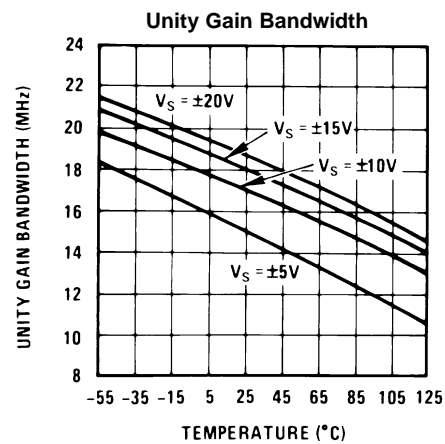


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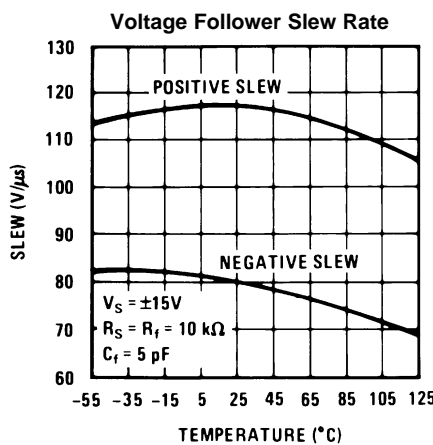


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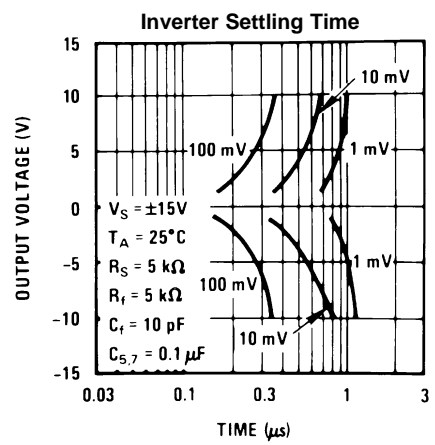
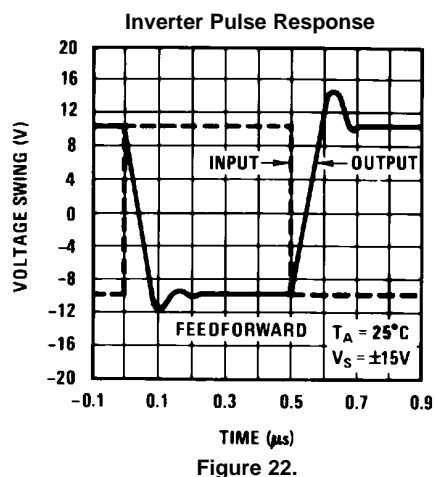
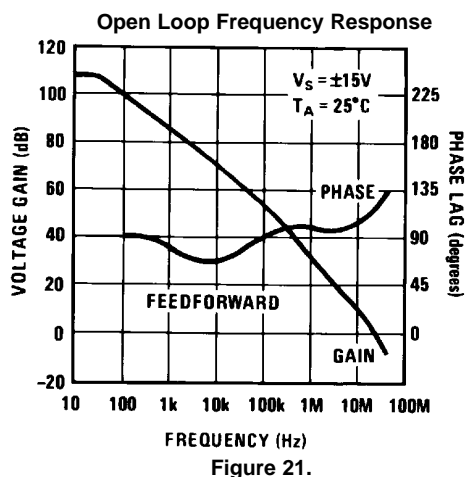
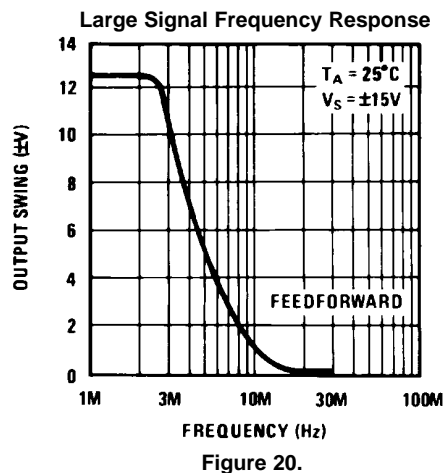
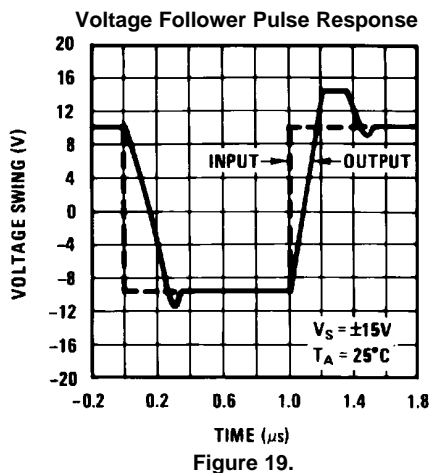
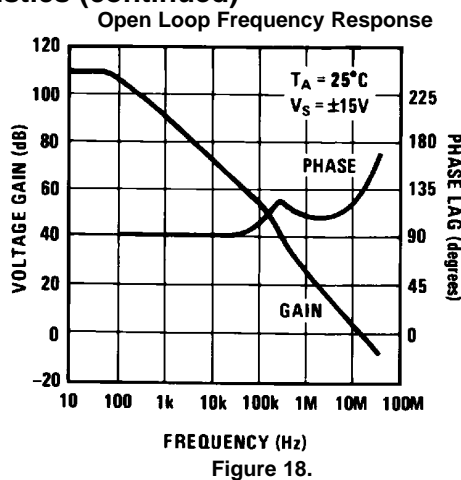
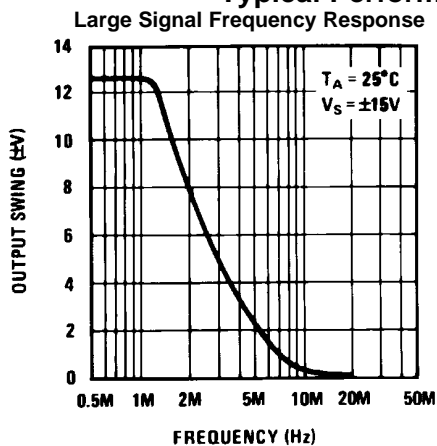


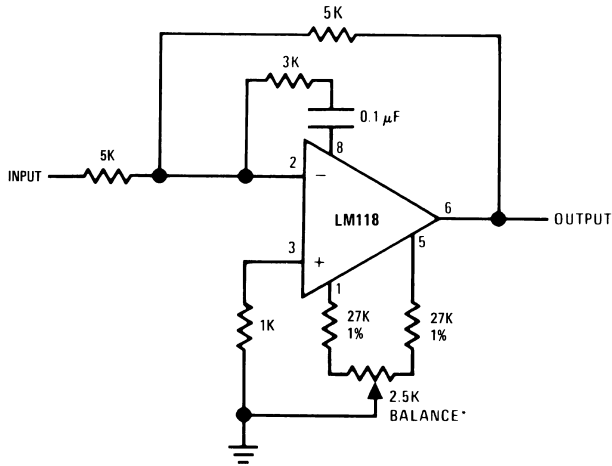
Figure 16.

Typical Performance Characteristics (continued)



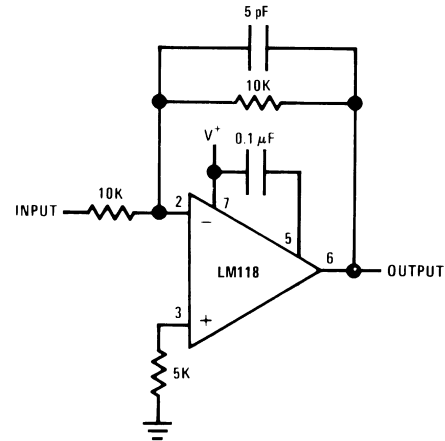
AUXILIARY CIRCUITS

Feedforward Compensation for Greater Inverting Slew Rate



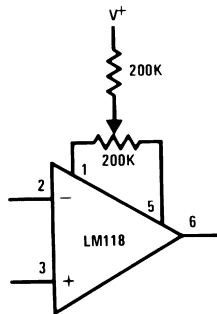
Slew rate typically 150V/μs.

Compensation for Minimum Settling Time

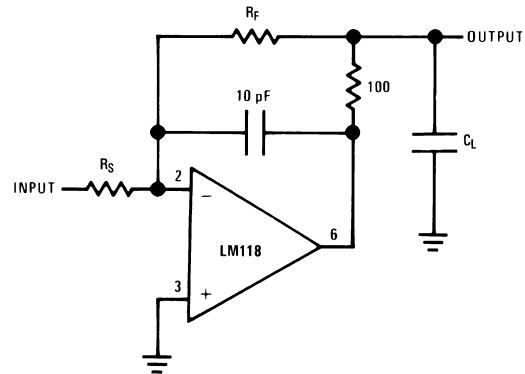


Slew and settling time to 0.1% for a 10V step change is 800 ns.

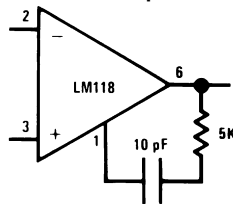
Offset Balancing



Isolating Large Capacitive Loads

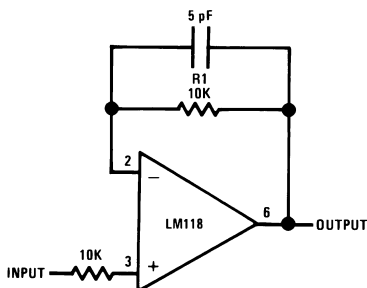


Overcompensation



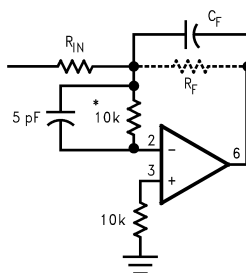
Typical Applications

Fast Voltage Follower



Do not hard-wire as voltage follower ($R_1 \geq 5 \text{ k}\Omega$)

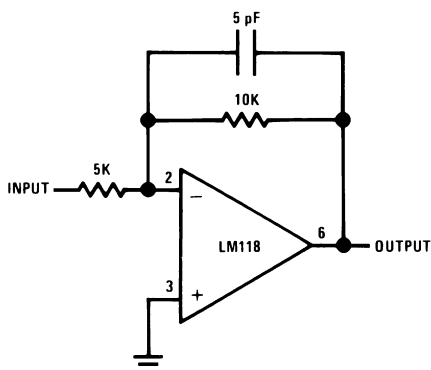
Integrator or Slow Inverter



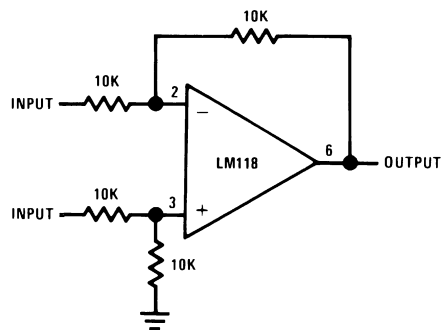
$C_F = \text{Large}$ ($C_F \geq 50 \text{ pF}$)

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

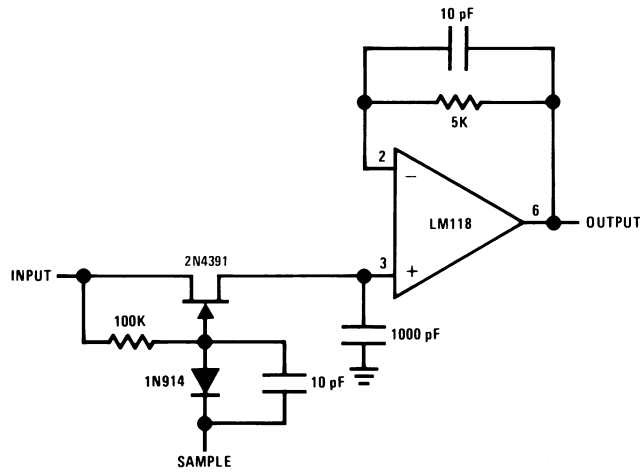
Fast Summing Amplifier



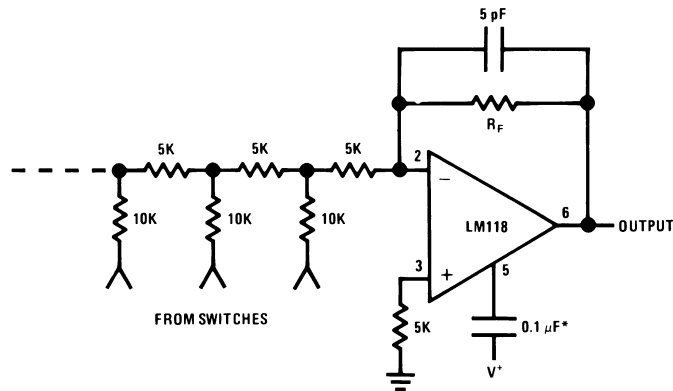
Differential Amplifier



Fast Sample and Hold

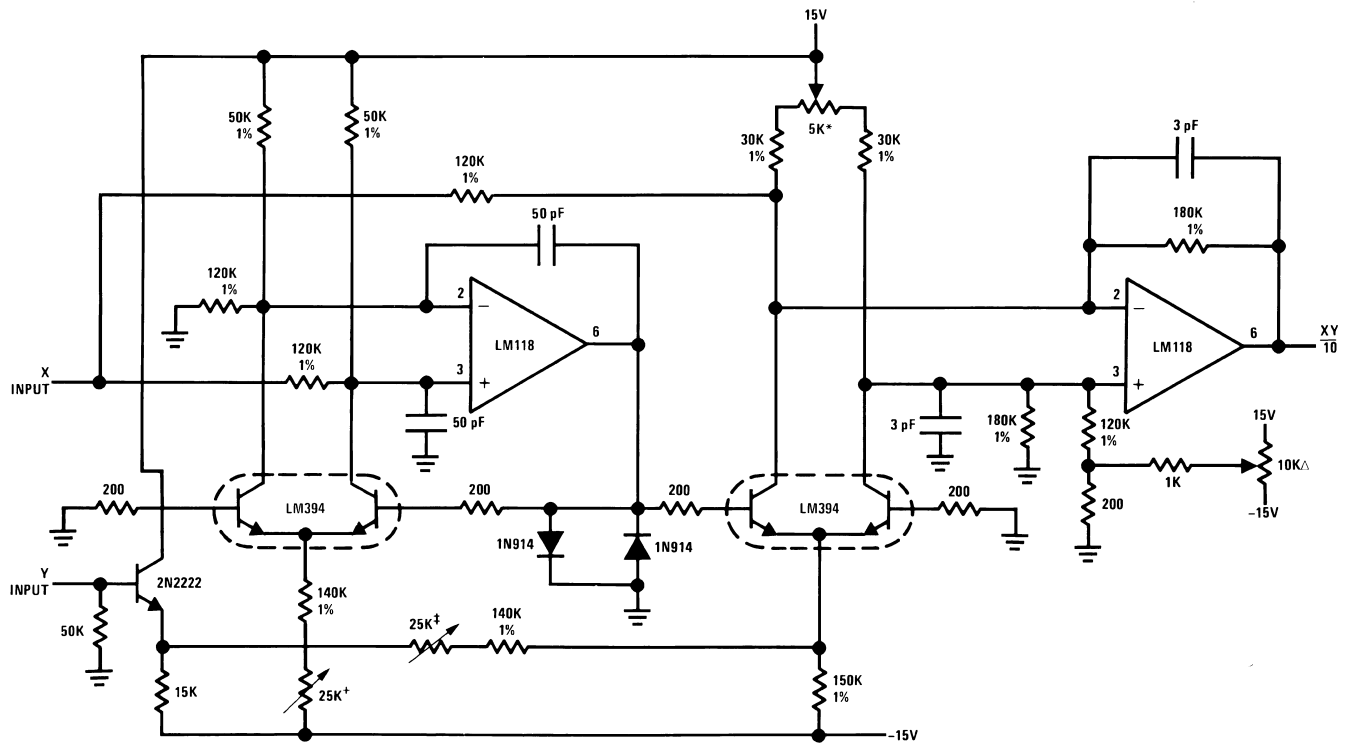


D/A Converter Using Ladder Network



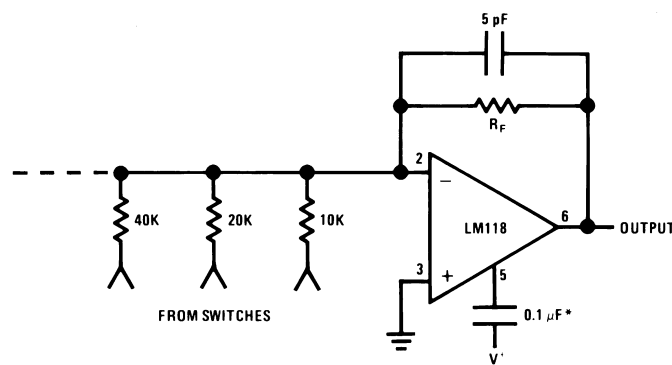
*Optional—Reduces settling time.

Four Quadrant Multiplier



ΔOutput zero.
 *"Y" zero
 + "X" zero
 ‡Full scale adjust.

D/A Converter Using Binary Weighted Network



*Optional—Reduces settling time.

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet, MNL118-X Rev 0A0 was converted into the Corp. datasheet format. MDS datasheet will be archived.
03/20/2013	A	All Sections		Changed Layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM118 MD8	ACTIVE	DIESALE	Y	0	182	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM118 MW8	ACTIVE	WAFERSALE	YS	0	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM118H/883	ACTIVE	TO-99	LMC	8	20	TBD	Call TI	Call TI	-55 to 125	LM118H/883 Q ACO LM118H/883 Q >T	Samples
LM118J-8/883	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Call TI	-55 to 125	LM118J-8 /883 Q ACO /883 Q >T	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

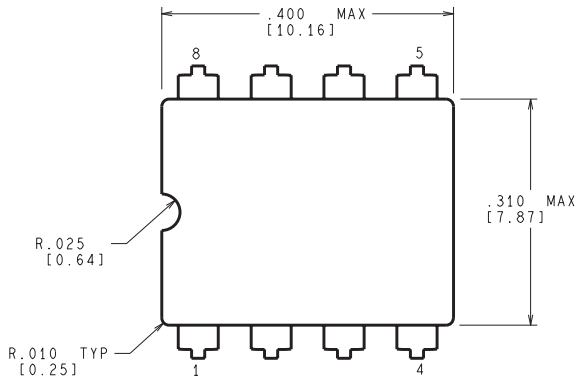
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

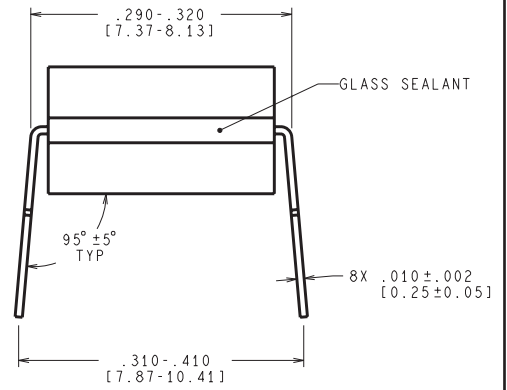
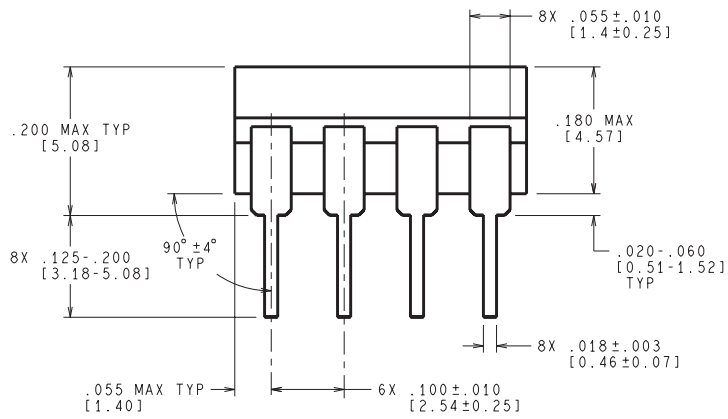
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VALUES IN [] ARE MILLIMETERS



J08A (Rev M)

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