TPA3251D2 175W 立体声/350W 单声道 PurePath™ 超高清模拟输入 D 类放大器

1 特性

- 差分模拟输入
- 总谐波失真+噪声 (THD+N) 为 10% 时的总输出功率
  - 175W/4Ω，桥接负载 (BTL) 立体声配置
  - 220W/3Ω，桥接负载 (BTL) 立体声配置
  - 350W/2Ω，并行桥接负载 (PBTL) 单声道配置
- THD+N 为 1% 时的总输出功率
  - 140W/4Ω，BTL 立体声配置
  - 175W/3Ω，BTL 立体声配置
  - 285W/2Ω，PBTL 单声道配置
- 采用高级集成反馈设计，具有高速栅极驱动器错误校正功能（PurePath™ 超高清）
  - 高达 100kHz 的单宽带，用于高清 (HD) 源的高频成分
  - 超低 THD+N：1W/4Ω 时为 0.005%；削波时 <0.01%
  - 60dB 电源抑制比 (PSRR)（BTL，无输入信号）
  - <60μV（A 加权）输出噪声
  - >111dB（A 加权）信噪比 (SNR)
- 多种可能配置：
  - 立体声、单声道、2.1 和 4xSE
- 启动和停止时无喀哒声和噼啪声
- 90% 高效 D 类操作 (4Ω)
- 12V 至 36V 宽电源电压工作范围
- 具有错误报告功能的自保护设计（包括欠压、过压、削波和短路保护）
- 采用推荐的系统设计时，符合电磁干扰 (EMI) 标准

2 应用

- 蓝光碟磁盘™ /DVD 接收器
- 高端 HTiB 系统
- AV 接收机
- 高端条形音箱
- 微型 Combo 系统
- 有源扬声器和低音炮

3 说明

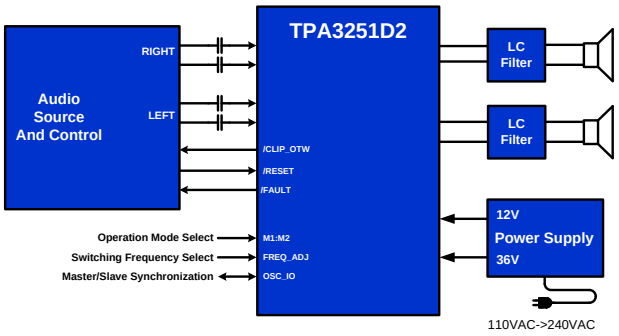
TPA3251D2 是一款高性能 D 类功率放大器，它具有 D 类效率并且能够带来真正的高端音质。 该器件特有高级集成反馈设计和专有高速栅极驱动器错误校正功能（PurePath™ 超高清）。 该技术可使器件在整个音频频带内保持超低失真，同时展现完美音质。 该器件最多可驱动 2 个 175W/4Ω 负载和 2 个 220W/3Ω 负载，并且特有一个 2 VRMS 模拟输入接口，支持与高性能 DAC（例如，TI 的 PCM5242）的无缝连接。 除了出色的音频性能外，TPA3251D2 还兼具高功率效率和超低功率级空闲损耗（1W 以下）两大优点。这可以利用 60mΩ MOSFET 以及优化型栅极驱动器方案来实现，该方案相比传统的分立实现方案可显著降低空闲损耗。

器件信息(1)

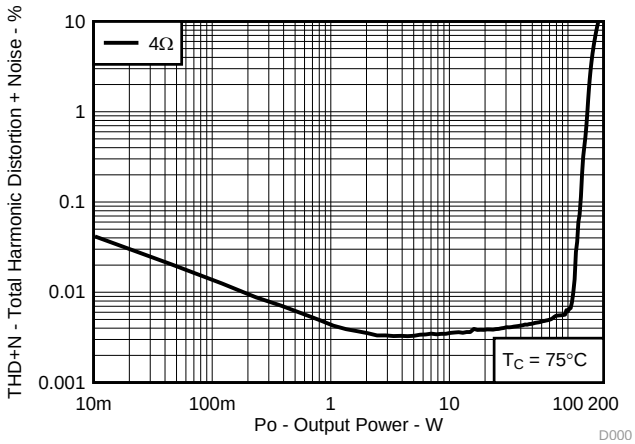
器件型号	封装	封装尺寸（标称值）
TPA3251D2	HTSSOP (44)	6.10mm x 14.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



总谐波失真



目录

4 修订历史记录

Changes from Revision B (June 2015) to Revision C **Page**

- 已从单页“产品预览”更改为完整数据表 ... 1

Changes from Revision A (June 2015) to Revision B **Page**

- 已将*特性*列表项“*80dB 电源抑制比 (PSRR)（BTL，无输入信号）*”更改为“*60dB 电源抑制比 (PSRR)（BTL，无输入信号）*” ... 1
- 已将*特性*列表项“*>112dB（A 加权）信噪比 (SNR)*”更改为“*>111dB（A 加权）信噪比 (SNR)*” ... 1

Changes from Original (May 2015) to Revision A **Page**

- 已更改*特性*列表中的*THD+N 为 1% 时的总输出功率* ... 1
- 已更改*特性*列表项“*高级集成反馈设计...*” ... 1
- 已将*特性*列表项“*<65μV（A 加权）输出噪声*”更改为“*<60μV（A 加权）输出噪声*” ... 1
- 已更改*特性*列表中的“*多种可能配置：*” ... 1
- 已更改*说明* ... 1
- 已添加*简化电路原理图* ... 1

5 Device Comparison Table

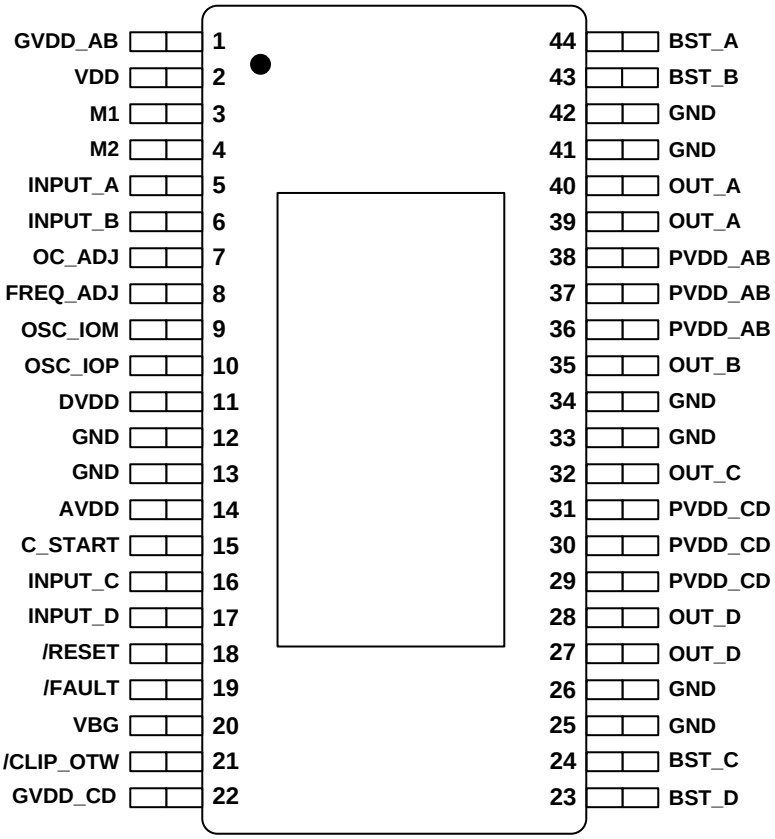
DEVICE NAME	DESCRIPTION
TAS5630B	300-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier
TAS5613A	150-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier
TAS5611A	125-W Stereo Class-D PurePath™ HD Analog Input Audio Power Amplifier

6 Pin Configuration and Functions

The TPA3251D2 is available in a thermally enhanced TSSOP package.

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

DDV Package
HTSSOP 44-Pin
(Top View)



Pin Functions

NAME	NO.	I/O	DESCRIPTION
AVDD	14	P	Internal voltage regulator, analog section
BST_A	44	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_A required.
BST_B	43	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_B required.
BST_C	24	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_C required.
BST_D	23	P	HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_D required.
$\overline{\text{CLIP\_OTW}}$	21	O	Clipping warning and Over-temperature warning; open drain; active low
C_START	15	O	Startup ramp, requires a charging capacitor to GND
DVDD	11	P	Internal voltage regulator, digital section
$\overline{\text{FAULT}}$	19	O	Shutdown signal, open drain; active low
FREQ_ADJ	8	O	Oscillator freqency programming pin
GND	12, 13, 25, 26, 33, 34, 41, 42	P	Ground
GVDD_AB	1	P	Gate-drive voltage supply; AB-side, requires 0.1 µF capacitor to GND
GVDD_CD	22	P	Gate-drive voltage supply; CD-side, requires 0.1 µF capacitor to GND
INPUT_A	5	I	Input signal for half bridge A
INPUT_B	6	I	Input signal for half bridge B
INPUT_C	16	I	Input signal for half bridge C
INPUT_D	17	I	Input signal for half bridge D
M1	3	I	Mode selection 1 (LSB)
M2	4	I	Mode selection 2 (MSB)
OC_ADJ	7	I/O	Over-Current threshold programming pin
OSC_IOM	9	I/O	Oscillator synchronization interface
OSC_IOP	10	O	Oscillator synchronization interface
OUT_A	39, 40	O	Output, half bridge A
OUT_B	35	O	Output, half bridge B
OUT_C	32	O	Output, half bridge C
OUT_D	27, 28	O	Output, half bridge D
PVDD_AB	36, 37, 38	P	PVDD supply for half-bridge A and B
PVDD_CD	29, 30, 31	P	PVDD supply for half-bridge C and D
$\overline{\text{RESET}}$	18	I	Device reset Input; active low
VDD	2	P	Power supply for internal voltage regulator requires a 10-µF capacitor with a 0.1-µF capacitor to GND for decoupling.
VBG	20	P	Internal voltage reference requires a 0.1-µF capacitor to GND for decoupling.
PowerPad™		P	Ground, connect to grounded heat sink

Table 1. Mode Selection Pins

MODE PINS		INPUT MODE	OUTPUT CONFIGURATION	DESCRIPTION
M2	M1			
0	0	2N + 1	2 × BTL	Stereo BTL output configuration
0	1	2N/1N + 1	1 x BTL + 2 x SE	2.1 BTL + SE mode
1	0	2N + 1	1 x PBTL	Parallelled BTL configuration. Connect INPUT_C and INPUT_D to GND.
1	1	1N +1	4 x SE	Single ended output configuration

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	BST_X to GVDD_X(2)	–0.3	50	V
	VDD to GND	–0.3	13.2	V
	GVDD_X to GND(2)	–0.3	13.2	V
	PVDD_X to GND(2)	–0.3	50	V
	DVDD to GND	–0.3	4.2	V
	AVDD to GND	–0.3	8.5	V
	VBG to GND	-0.3	4.2	V
Interface pins	OUT_X to GND(2)	–0.3	50	V
	BST_X to GND(2)	–0.3	62.5	V
	OC_ADJ, M1, M2, OSC_IOP, OSC_IOM, FREQ_ADJ, C_START, to GND	–0.3	4.2	V
	$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$, $\overline{\text{CLIP}}$ to GND	–0.3	4.2	V
	INPUT_X to GND	–0.3	7	V
	Continuous sink current, $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$, $\overline{\text{CLIP}}$, $\overline{\text{RESET}}$ to GND		9	mA
T_J	Operating junction temperature range	0	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	12	36	38	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter inductance within recommended value range	2.7	4		Ω
R_L(SE)			1.5	3		
R_L(PBTL)			1.6	2		
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	5			μH
L_{OUT}(SE)			5			
L_{OUT}(PBTL)			5			
F_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	575	600	625	kHz
		AM1	475	500	525	
		AM2	430	450	470	
$R_{(FREQ\_ADJ)}$	PWM frame rate programming resistor	Nominal; Master mode	9.9	10	10.1	kΩ
		AM1; Master mode	19.8	20	20.2	
		AM2; Master mode	29.7	30	30.3	
C_{PVDD}	PVDD close decoupling capacitors			1.0		μF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22		30	kΩ
$R_{OC(LATCHED)}$	Over-current programming resistor	Resistor tolerance = 5%	47		64	kΩ
$V_{(FREQ\_ADJ)}$	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
T_J	Junction temperature		0		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPA3251D2 DDV 44-PINS HTSSOP		UNIT
		JEDEC STANDARD 4 LAYER PCB	FIXED 85°C HEATSINK TEMPERATURE(2)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	2.5(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.36	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	n/a	
ψ_{JT}	Junction-to-top characterization parameter	0.19	0.5	
ψ_{JB}	Junction-to-board characterization parameter	24.2	n/a	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal data are obtained with 85°C heat sink temperature using thermal compound with 0.7W/mK thermal conductivity and 2mil thickness. In this model heat sink temperature is considered to be the ambient temperature and only path for dissipation is to the heatsink.

7.5 Electrical Characteristics

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator, only used as reference node	VDD = 12 V	3	3.3	3.6	V
AVDD	Voltage regulator, only used as reference node	VDD = 12 V		7.8		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		40		mA
		Idle, reset mode		13		
I_{GVDD_X}	Gate-supply current per full-bridge	50% duty cycle		25		mA
		Reset mode		3		
I_{PVDD_X}	PVDD idle current per full bridge	50% duty cycle with recommended output filter		12.5		mA
		Reset mode, No switching		1		mA
ANALOG INPUTS						
R_{IN}	Input resistance			24		kΩ
V_{IN}	Maximum input voltage swing				7	V
I_{IN}	Maximum input current				1	mA
G	Inverting voltage Gain	V_{OUT}/V_{IN}		20		dB
OSCILLATOR						
$f_{OSC(IO+)}$	Nominal, Master Mode	F_{PWM} × 6	3.45	3.6	3.75	MHz
	AM1, Master Mode		2.85	3	3.15	
	AM2, Master Mode		2.58	2.7	2.82	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, Includes metallization resistance, GVDD = 12 V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	mΩ
I/O PROTECTION						
$V_{uvp,VDD,GVDD}$	Undervoltage protection limit, GVDD_x and VDD			9.5		V
$V_{uvp,VDD,\ GVDD,hyst}$ (1)				0.6		V
OTW	Overtemperature warning, $\overline{\text{CLIP\_OTW}}$ (1)		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{\text{CLIP\_OTW}}$ to be inactive after OTW event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
OTE-$OTW_{(differential)}$ (1)	OTE-OTW differential			30		°C
OTE_{hyst} (1)	A reset needs to occur for $\overline{\text{FAULT}}$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 600 kHz		1.7		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22 kΩ		14		A
$I_{OC(LATCHED)}$	Overcurrent limit protection	Resistor – programmable, peak current in 1Ω load, R_{OCP} = 47kΩ		14		A
I_{DCspkr}	DC Speaker Protection Current Threshold	BTL current imbalance threshold		1.5		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent.		150		ns
I_{PD}	Output pulldown current of each half	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA

(1) Specified by design.

Electrical Characteristics (continued)

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	M1, M2, OSC_IOP, OSC_IOM, RESET	1.9			V
V_{IL}	Low level input voltage				0.8	V
I_{lkg}	Input leakage current				100	µA
OTW/SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{CLIP\_OTW}}$ to DVDD, $\overline{\text{FAULT}}$ to DVDD		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
Device fanout	$\overline{\text{CLIP\_OTW}}$, $\overline{\text{FAULT}}$	No external pullup		30		devices

7.6 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		220		W
		R_L = 4 Ω, 10% THD+N		175		
		R_L = 3 Ω, 1% THD+N		175		
		R_L = 4 Ω, 1% THD+N		140		
THD+N	Total harmonic distortion + noise	1 W		0.005%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		60		µV
$\lvert V_{OS} \rvert$	Output offset voltage	Inputs AC coupled to GND		20	60	mV
SNR	Signal-to-noise ratio(1)			111		dB
DNR	Dynamic range			115		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

7.7 Audio Characteristics (SE)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 µH, C_{DEM} = 1 µF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		84		W
		R_L = 3 Ω, 10% THD+N		60		
		R_L = 4 Ω, 10% THD+N		47		
		R_L = 2 Ω, 1% THD+N		67		
		R_L = 3 Ω, 1% THD+N		48		
		R_L = 4 Ω, 1% THD+N		37		
THD+N	Total harmonic distortion + noise	1 W		0.015%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		115		µV
SNR	Signal to noise ratio(1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted		101		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		0.5		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

7.8 Audio Characteristics (PBTL)

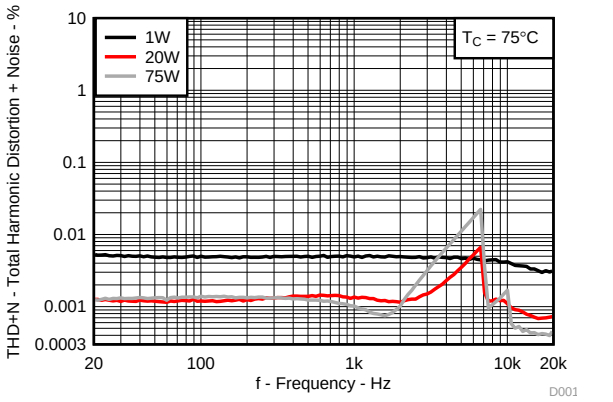
PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		355		W
		R_L = 3 Ω, 10% THD+N		250		
		R_L = 4 Ω, 10% THD+N		195		
		R_L = 2 Ω, 1% THD+N		285		
		R_L = 3 Ω, 1% THD+N		200		
		R_L = 4 Ω, 1% THD+N		155		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		62		µV
SNR	Signal to noise ratio(1)	A-weighted		111		dB
DNR	Dynamic range	A-weighted		111		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

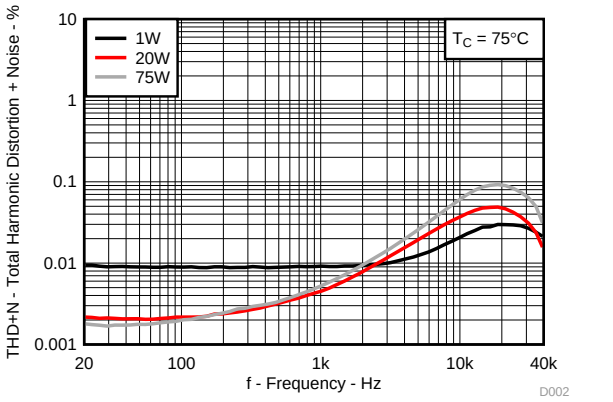
7.9 Typical Characteristics, BTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



R_L = 4 Ω P = 1W, 20W, 75W T_C = 75°C

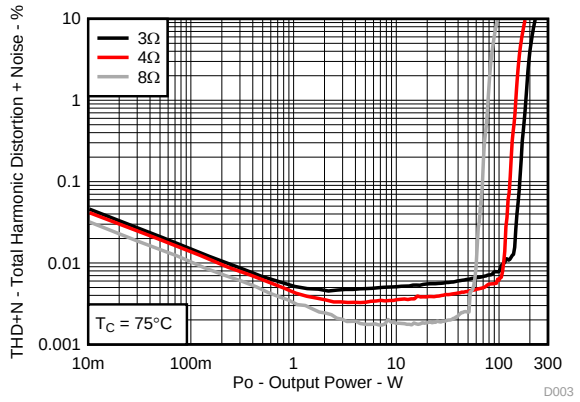
Figure 1. Total Harmonic Distortion+Noise vs Frequency



R_L = 4 Ω P = 1W, 20W, 75W T_C = 75°C

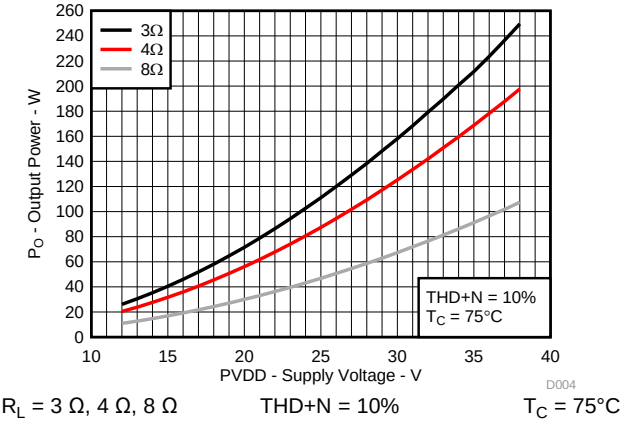
AUX-0025 filter, 80 kHz analyzer BW

Figure 2. Total Harmonic Distortion+Noise vs Frequency



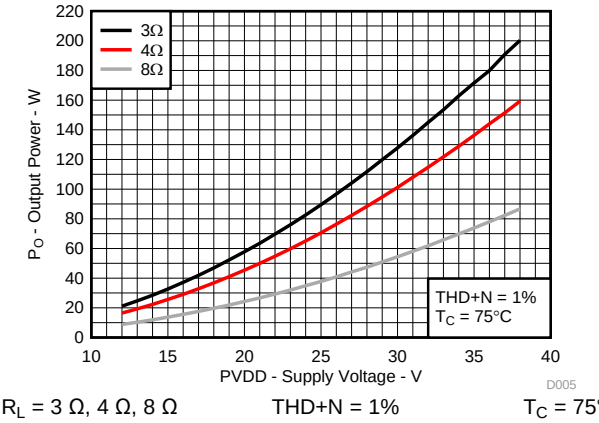
R_L = 3 Ω, 4 Ω, 8 Ω T_C = 75°C

Figure 3. Total Harmonic Distortion + Noise vs Output Power



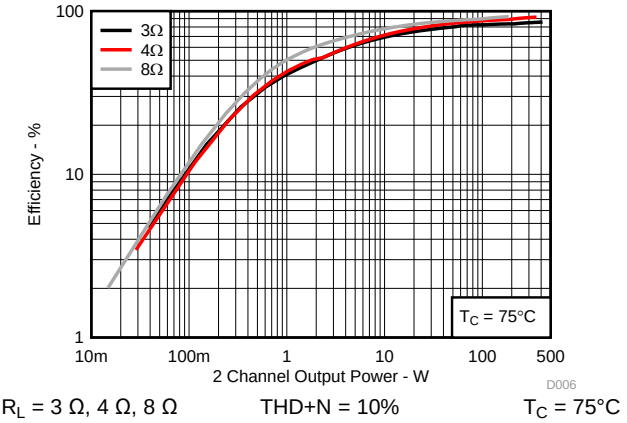
R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 4. Output Power vs Supply Voltage



R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 1% T_C = 75°C

Figure 5. Output Power vs Supply Voltage

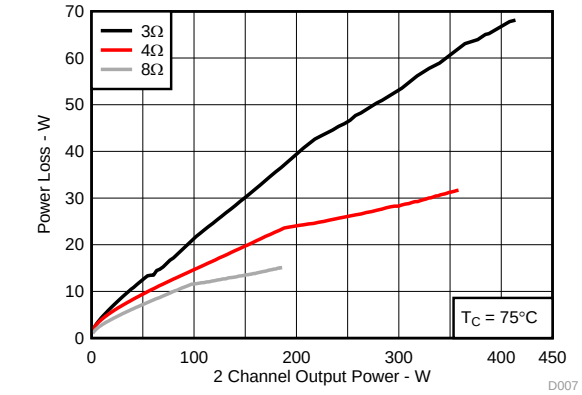


R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 6. System Efficiency vs Output Power

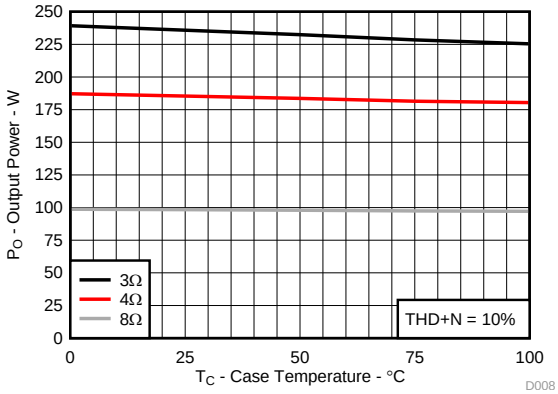
Typical Characteristics, BTL Configuration (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



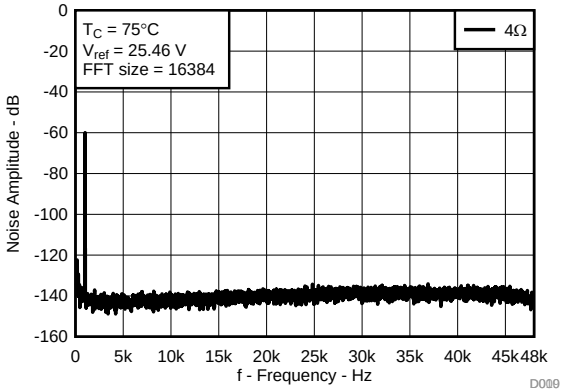
R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 7. System Power Loss vs Output Power



R_L = 3 Ω, 4 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 8. Output Power vs Case Temperature

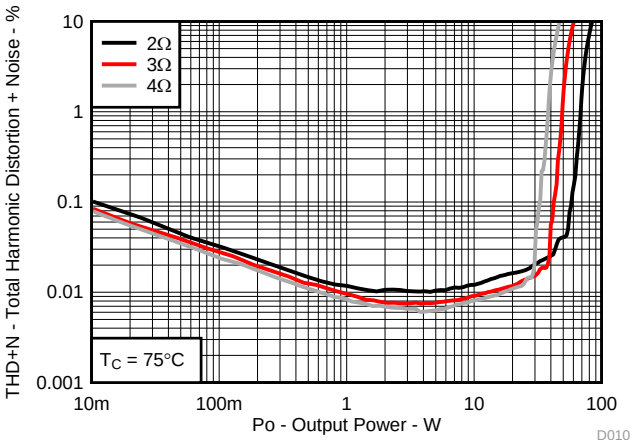


4 Ω, V_{REF} = 25.46 V (1% Output power) FFT = 16384
AUX-0025 filter, 80 kHz analyzer BW T_C = 75°C

Figure 9. Noise Amplitude vs Frequency

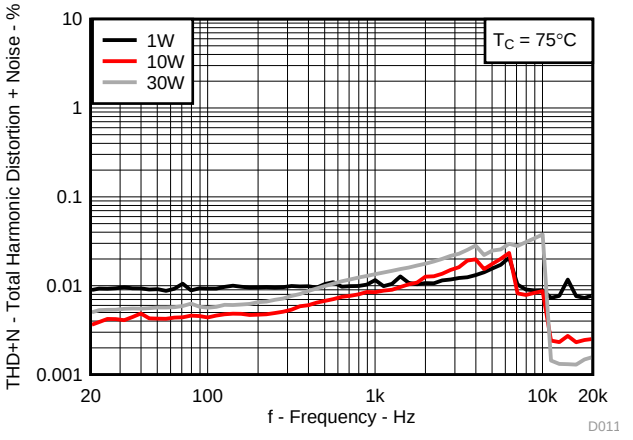
7.10 Typical Characteristics, SE Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 3 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 µH, C_{DEM} = 680 nF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.



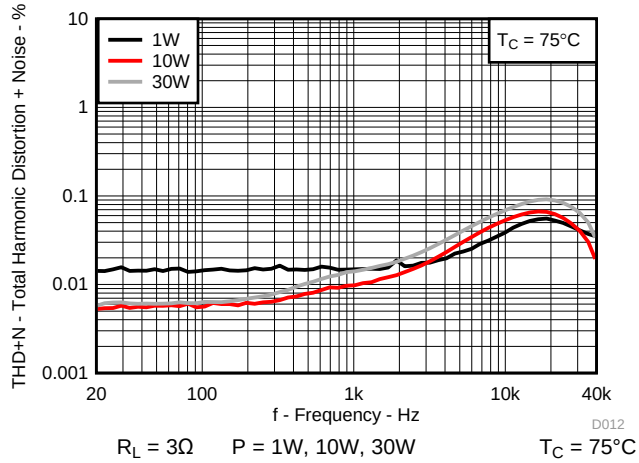
R_L = 2Ω, 3Ω, 4Ω T_C = 75°C

Figure 10. Total Harmonic Distortion+Noise vs Output Power



R_L = 3Ω P = 1W, 10W, 30W T_C = 75°C

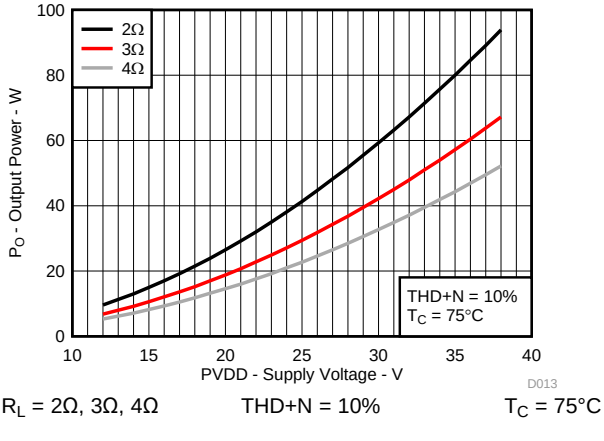
Figure 11. Total Harmonic Distortion+Noise vs Frequency



R_L = 3Ω P = 1W, 10W, 30W T_C = 75°C

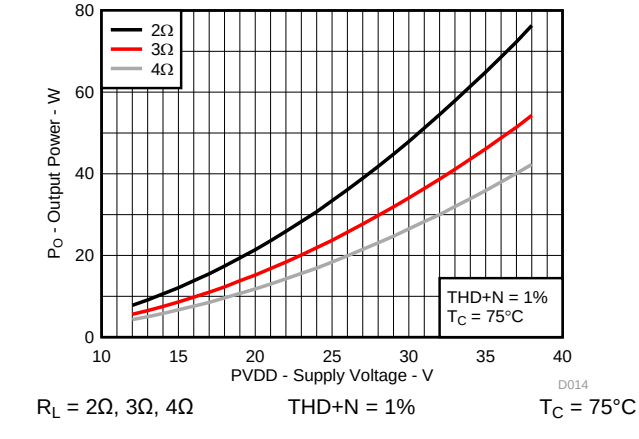
AUX-0025 filter, 80 kHz analyzer BW

Figure 12. Total Harmonic Distortion+Noise vs Frequency



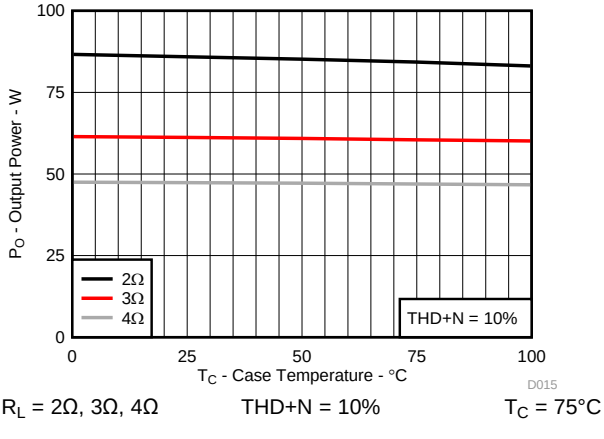
R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 13. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 1% T_C = 75°C

Figure 14. Output Power vs Supply Voltage

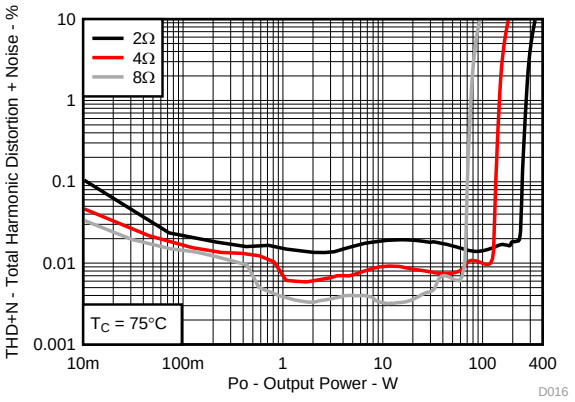


R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 15. Output Power vs Case Temperature

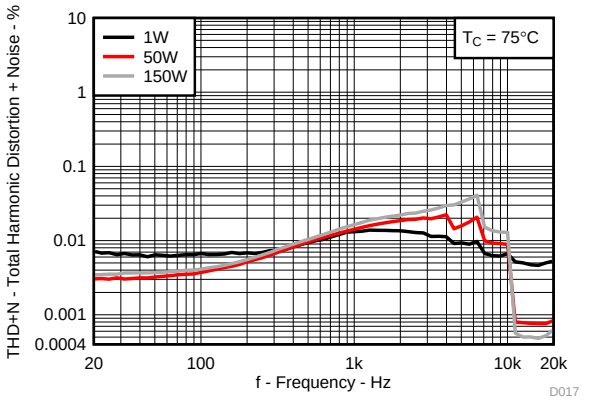
7.11 Typical Characteristics, PBTL Configuration

All Measurements taken at audio frequency = 1kHz, PVDD_X = 36V, GVDD_X = 12V, R_L = 2Ω, f_S = 600 kHz, R_{OC} = 22kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10µH, C_{DEM} = 1 µF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.



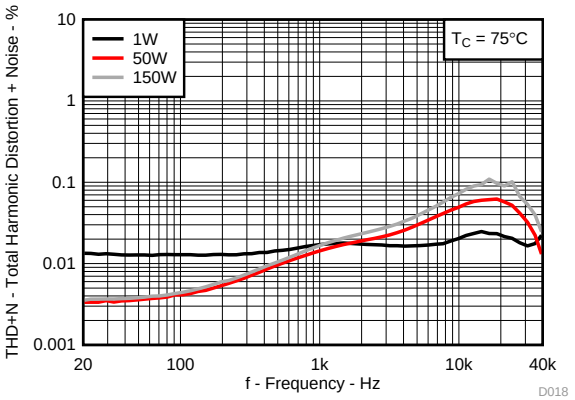
R_L = 2Ω, 4Ω, 8Ω T_C = 75°C

Figure 16. Total Harmonic Distortion+Noise vs Output Power



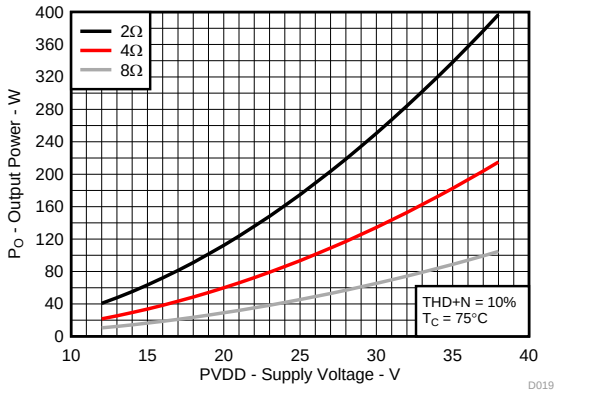
R_L = 2Ω P = 1W, 50W, 1.50W T_C = 75°C

Figure 17. Total Harmonic Distortion+Noise vs Frequency



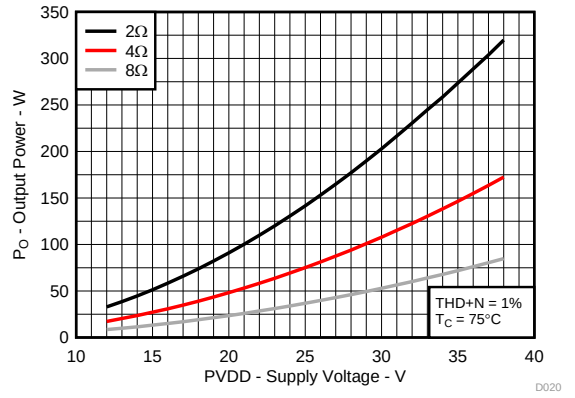
R_L = 2Ω P = 1W, 50W, 150W T_C = 75°C
AUX-0025 filter, 80 kHz analyzer BW

Figure 18. Total Harmonic Distortion+Noise vs Frequency



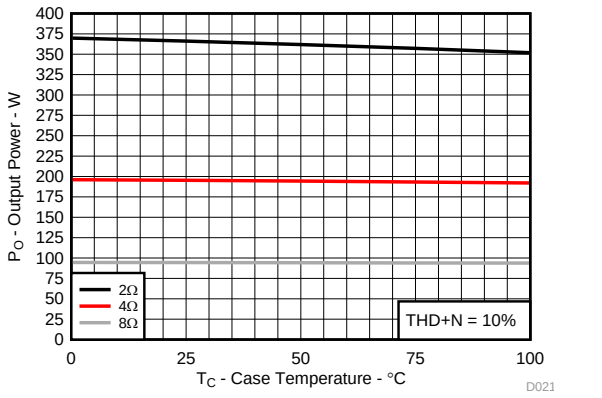
R_L = 2Ω, 4Ω, 8Ω THD+N = 10% T_C = 75°C

Figure 19. Output Power vs Supply Voltage



R_L = 2Ω, 4Ω, 8Ω THD+N = 1% T_C = 75°C

Figure 20. Output Power vs Supply Voltage



R_L = 2Ω, 4Ω, 8Ω THD+N = 10% T_C = 75°C

Figure 21. Output Power vs Case Temperature

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Recommended Operating Conditions*, *Typical Characteristics, BTL Configuration*, *Typical Characteristics, SE Configuration* and *Typical Characteristics, PBTL Configuration* sections.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. AES-17 + AUX-0025 pre-analyzer filters are recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

To facilitate system design, the TPA3251D2 needs only a 12-V supply in addition to the (typical) 36-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry, AVDD and DVDD. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

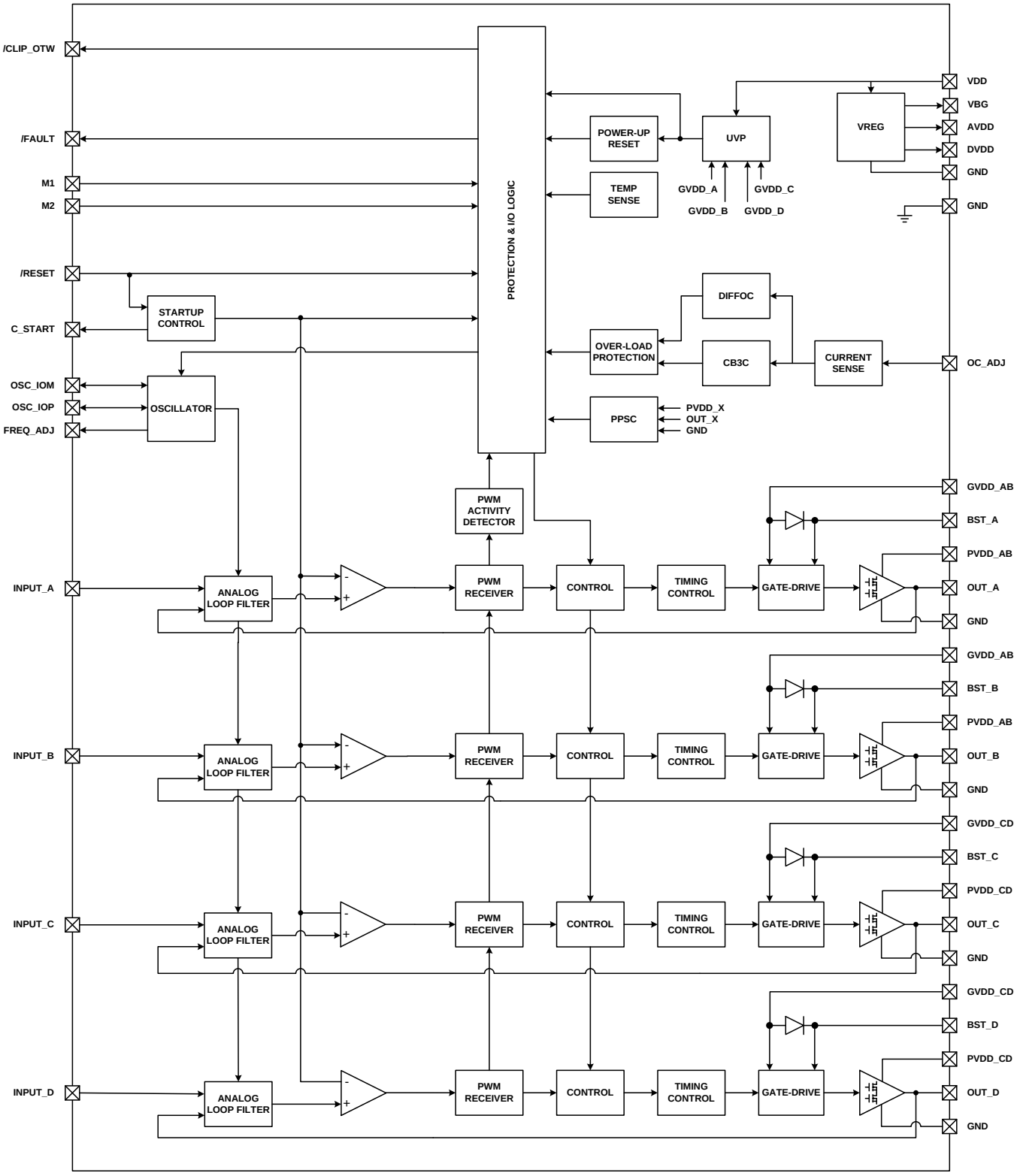
The audio signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X). Power-stage supply pins (PVDD_X) and gate drive supply pins (GVDD_X) are separate for each full bridge. Although supplied from the same 12-V source, separating to GVDD_AB, GVDD_CD, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. It is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1-µF ceramic capacitor placed as close as possible to the supply pins. It is recommended to follow the PCB layout of the TPA3251D2 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 36-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artefacts. Moreover, the TPA3251D2 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

9.2 Functional Block Diagrams



FunctionalBlockDiagram.vsd

Functional Block Diagrams (continued)

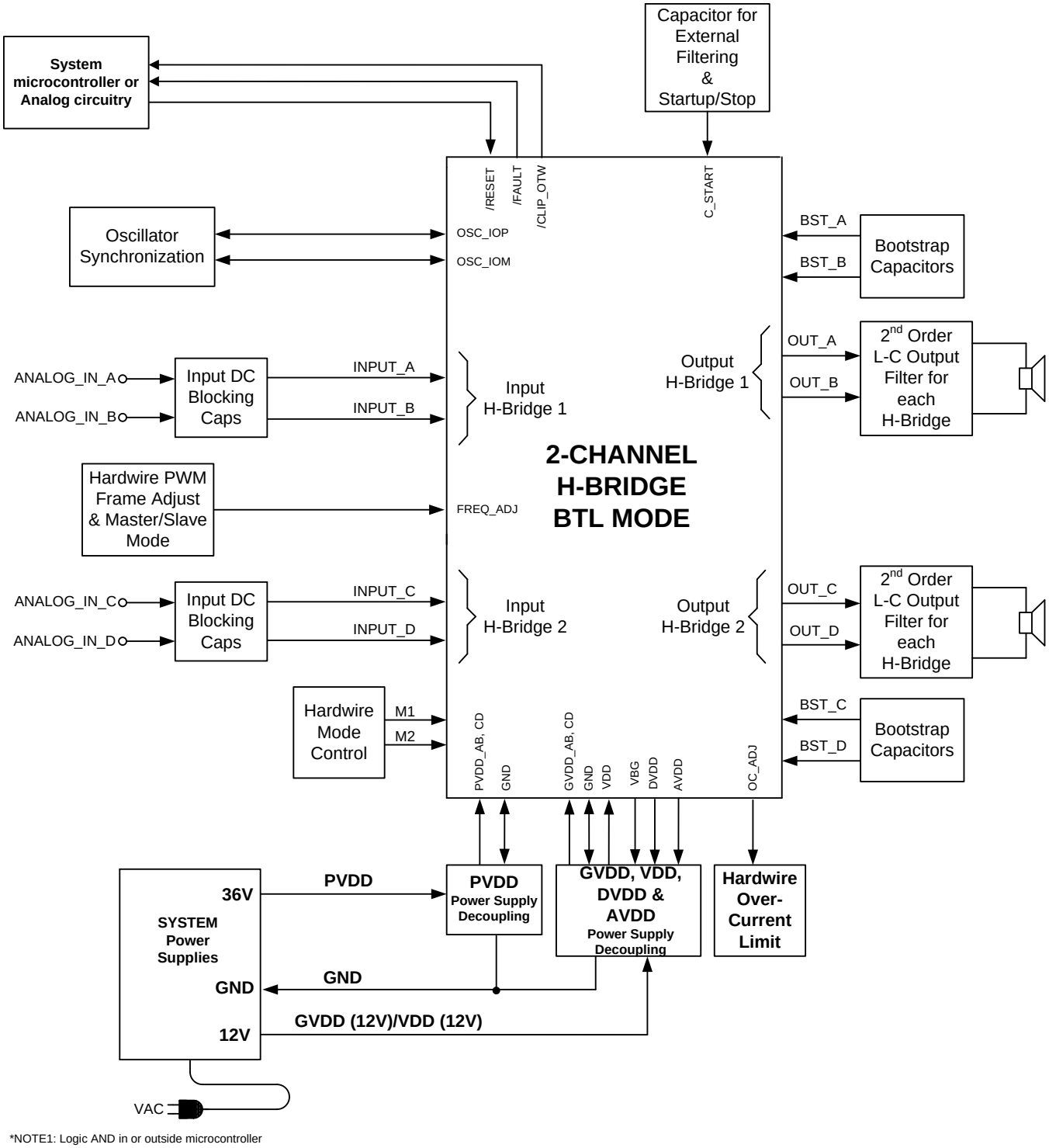


Figure 22. System Block Diagram

9.3 Feature Description

9.3.1 Error Reporting

The $\overline{\text{FAULT}}$, and $\overline{\text{CLIP\_OTW}}$, pins are active-low, open-drain outputs. The function is for protection-mode signaling to a system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Also, $\overline{\text{CLIP\_OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 2).

Table 2. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{CLIP\_OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP) Junction temperature higher than 125°C (overtemperature warning)
0	0	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 125°C (overtemperature warning)
0	1	Overload (OLP) or undervoltage (UVP). Junction temperature lower than 125°C
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{CLIP\_OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by, that is, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{CLIP\_OTW}}$ outputs.

9.4 Device Protection System

The TPA3251D2 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TPA3251D2 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will function on errors, as shown in Table 3.

Table 3. Device Protection

BTL	MODE	PBTL	MODE	SE	MODE
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
A	A+B	A	A+B+C+D	A	A+B
B		B		B	
C	C+D	C		C	C+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert $\overline{\text{FAULT}}$).

9.4.1 Overload and Short Circuit Current Protection

TPA3251D2 has fast reacting current sensors with a programmable trip threshold (OC threshold) on all high-side and low-side FETs. To prevent output current to increase beyond the programmed threshold, TPA3251D2 has the option of either limiting the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) or to perform an immediate shutdown of the output in case of excess output current (Latching Shutdown). CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a drop of real speaker's load impedance, and allows the output current to be limited to a maximum programmed

level. If the maximum output current persists, i.e. the power stage being overloaded with too low load impedance, the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi- Z) state until a RESET cycle is initiated. CB3C works individually for each half bridge output. If an over current event is triggered, CB3C performs a state flip of the half bridge output that is cleared upon beginning of next PWM frame.

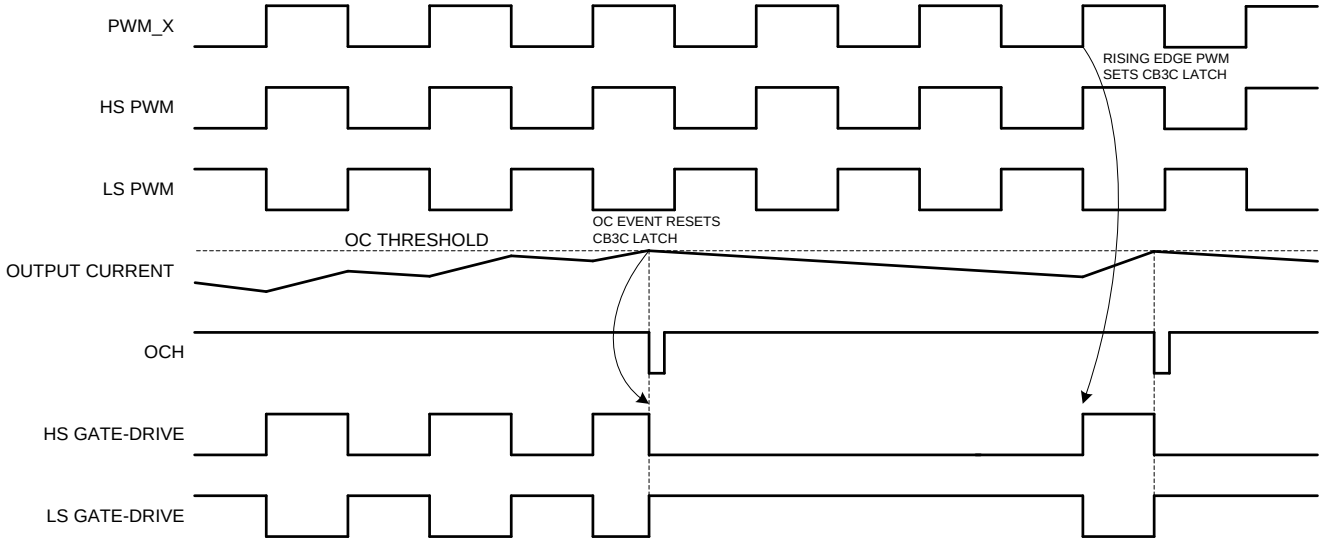


Figure 23. CB3C Timing Example

During CB3C an over load counter increments for each over current event and decrease for each non-over current PWM cycle. This allows full amplitude transients into a low speaker impedance without a shutdown protection action. In the event of a short circuit condition, the over current protection limits the output current by the CB3C operation and eventually shut down the affected output if the overload counter reaches its maximum value. If a latched OC operation is required such that the device shuts down the affected output immediately upon first detected over current event, this protection mode should be selected. The over current threshold and mode (CB3C or Latched OC) is programmed by the OC_ADJ resistor value. The OC_ADJ resistor needs to be within its intentional value range for either CB3C operation or Latched OC operation.

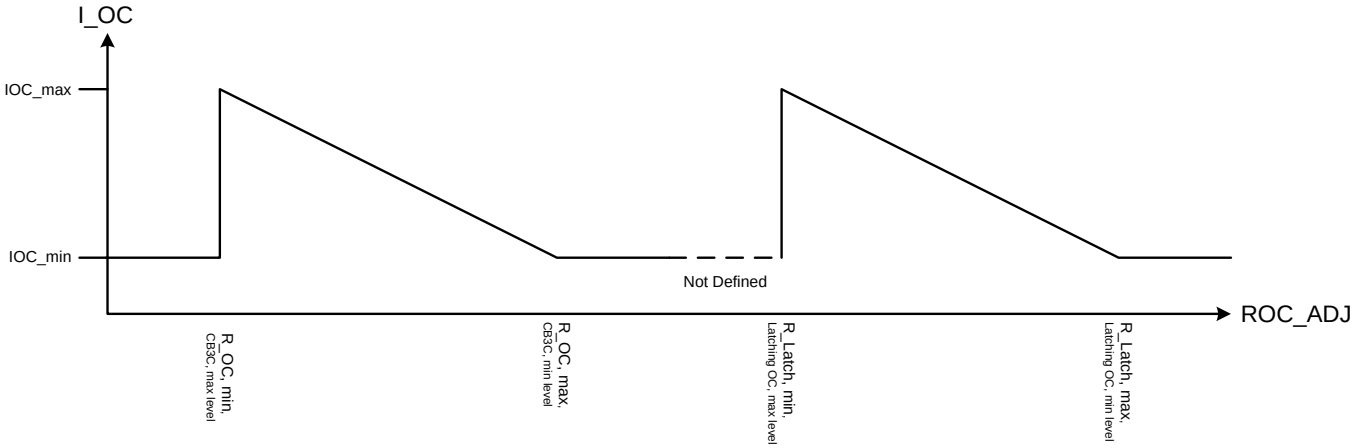


Figure 24. OC Threshold versus OC_ADJ Resistor Value Example

OC_ADJ values outside specified value range for either CB3C or latched OC operation will result in minimum OC threshold.

Table 4. Device Protection

OC_ADJ Resistor Value	Protection Mode	OC Threshold
22kΩ	CB3C	16.3A
24kΩ	CB3C	15.1A
27kΩ	CB3C	13.5A
30kΩ	CB3C	12.3A
47kΩ	Latched OC	16.3A
51kΩ	Latched OC	15.1A
56kΩ	Latched OC	13.5A
64kΩ	Latched OC	12.3A

9.4.2 DC Speaker Protection

The output DC protection scheme protects a connected speaker from excess DC current caused by a speaker wire accidentally shorted to chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL output, and in the event of the unbalance exceeding a programmed threshold, the overload counter increments until its maximum value and the affected output channel is shut down. DC Speaker Protection is disabled in PBTL and SE mode operation.

9.4.3 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15ms/µF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low, and the device will not react to changes applied to the RESET pin. If no shorts are present the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert a resistive load to GND_X or PVDD_X.

9.4.4 Overtemperature Protection OTW and OTE

TPA3251D2 has a two-level temperature-protection system that asserts an active-low warning signal (CLIP_OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

9.4.5 Undervoltage Protection (UVP) and Power-on Reset (POR)

The UVP and POR circuits of the TPA3251D2 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

9.4.6 Fault Handling

If a fault situation occurs while in operation, the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and will assert FAULT low. A global fault is a latching fault and clearing FAULT and restart operation requires resetting the device by toggling RESET. Toggling RESET should never be allowed with excessive system temperature, so it is advised to monitor RESET by a system microcontroller and only allow releasing RESET (RESET high) if the OTW signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channel(s). Note that asserting RESET low forces the FAULT signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system micro controller and responding to an over temperature warning signal by, that is, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

Table 5. Error Reporting

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Increase affected supply voltage	HI-Z
VDD UVP						
AVDD UVP						
POR (DVDD UVP)	Power On Reset	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Allow DVDD to rise	HI-Z
BST_X UVP	Voltage Fault	Channel (Half Bridge)	None	Self Clearing	Allow BST cap to recharge (lowside ON, VDD 12V)	HighSide off
OTW	Thermal Warning	Global	$\overline{\text{OTW}}$ pin	Self Clearing	Cool below OTW threshold	Normal operation
OTE	Thermal Shutdown	Global	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
OLP (CB3C>1.7ms)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
Latched OC (47kΩ<ROC_ADJ<68 kΩ)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
CB3C (22kΩ<ROC_ADJ<30 kΩ)	OC Limiting	Channel	None	Self Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs/3
Stuck at Fault(1)	No OSC_IO activity in Slave Mode	Global	None	Self Clearing	Resume OSC_IO activity	HI-Z

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

9.4.7 Device Reset

Asserting $\overline{\text{RESET}}$ low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active both in SE mode and BTL mode with $\overline{\text{RESET}}$ low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs.

Asserting reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

TPA3251D2 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

10.2 Typical Applications

10.2.1 Stereo BTL Application

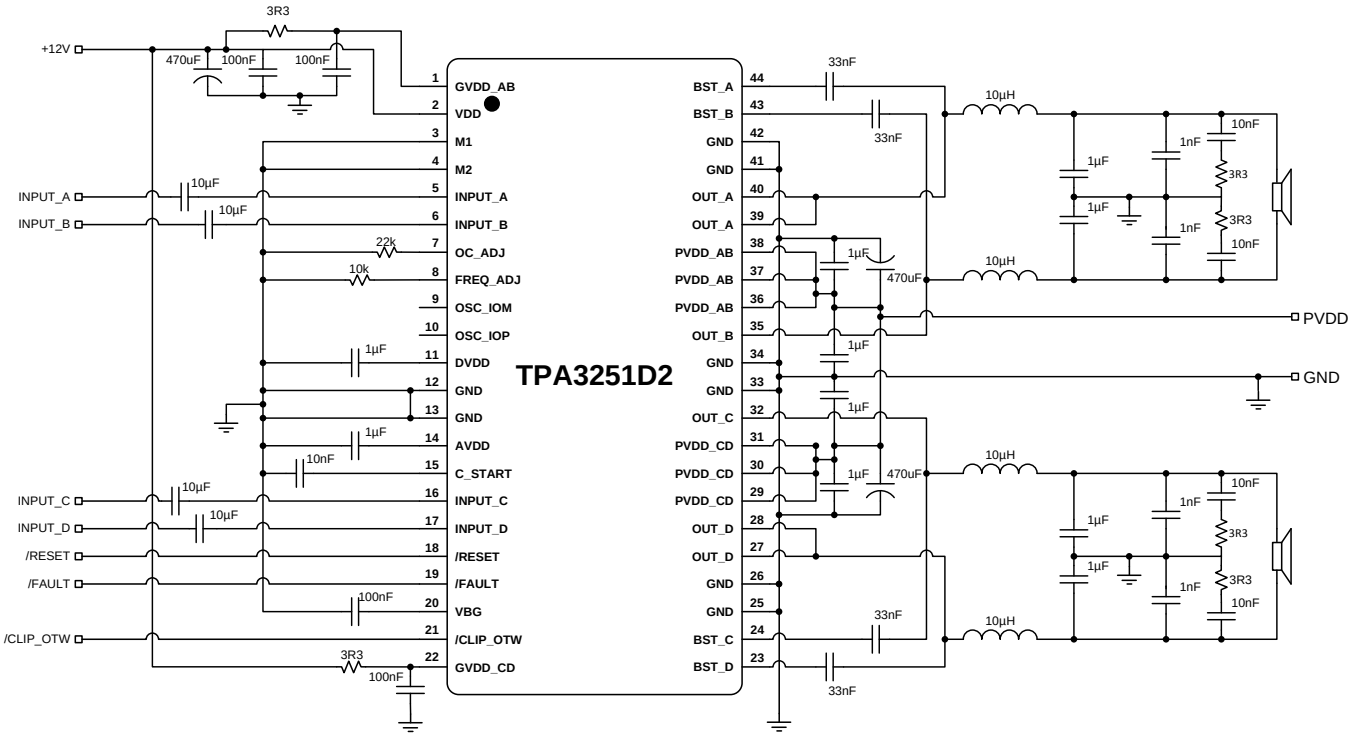


Figure 25. Typical Differential Input BTL Application

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters in Table 6.

Table 6. Design Requirements, BTL Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 12 V	12 V
High Power Supply	12 - 36 V
Mode Selection	M2 = L
	M1 = L
Analog Inputs	INPUT_A = ±3.9 V (peak, max)
	INPUT_B = ± 3.9V (peak, max)
	INPUT_C = ±3.9 V (peak, max)
	INPUT_D = ±3.9 V (peak, max)
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	3-8 Ω

10.2.1.2 Detailed Design Procedures

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply nominally operating at a low rail adjusting to a higher supply rail.

The device is inverting the audio signal from input to output.

The DVDD and AVDD pins are not recommended to be used as a voltage sources for external circuitry.

10.2.1.2.1 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 1µF that is placed on the power supply to each full-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50 V is required for use with a 36V power supply.

10.2.1.2.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 50 V supports most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.2.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper is recommended for use with the TPA3251D2. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

10.2.1.2.4 Oscillator

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

To reduce interference problems while using radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower value switching frequencies together results in the fewest cases of interference throughout the AM band. The oscillator frequency can be selected by the value of the FREQ_ADJ resistor connected to GND in master mode according to the description in the Recommended Operating Conditions table.

For slave mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to DVDD. This configures the OSC_I/O pins as inputs to be slaved from an external differential clock. In a master/slave system inter channel delay is automatically setup between the switching of the audio channels, which can be illustrated by no idle channels switching at the same time. This will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply to optimize audio performance and to get better operating conditions for the power supply. The inter channel delay will be setup for a slave device depending on the polarity of the OSC_I/O connection such that a slave mode 1 is selected by connecting the master device OSC_I/O to the slave 1 device OSC_I/O with same polarity (+ to + and - to -), and slave mode 2 is selected with the inverse polarity (+ to - and - to +).

10.2.2 Application Curves

Relevant performance plots for TPA3251D2 in BTL configuration are shown in *Typical Characteristics, BTL Configuration*

Table 7. Relevant Performance Plots, BTL Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Frequency	Figure 1
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 2
Total Harmonic Distortion + Noise vs Output Power	Figure 3
Output Power vs Supply Voltage, 10% THD+N	Figure 4
Output Power vs Supply Voltage, 10% THD+N	Figure 6
System Efficiency vs Output Power	Figure 6
System Power Loss vs Output Power	Figure 7
Output Power vs Case Temperature	Figure 8
Noise Amplitude vs Frequency	Figure 9

10.2.3 Typical Application, Single Ended (1N) SE

TPA3251D2 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

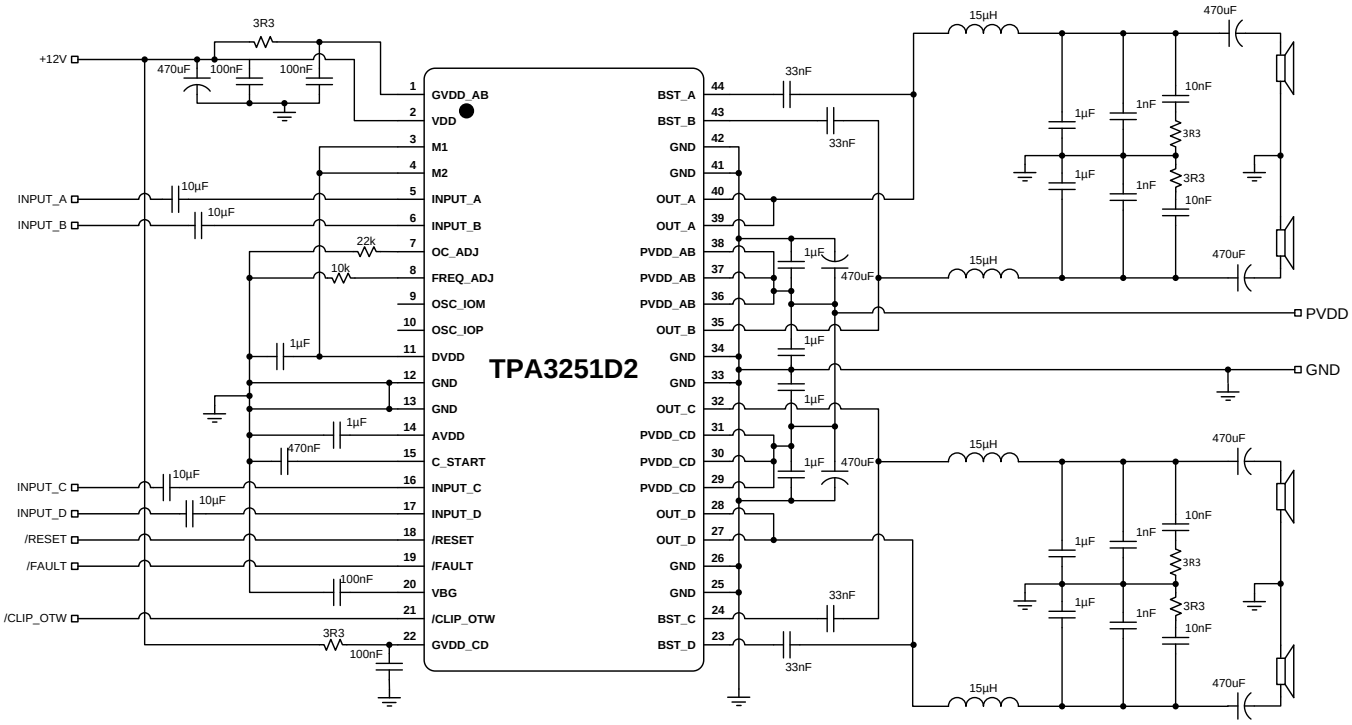


Figure 26. Typical Single Ended (1N) SE Application

10.2.3.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

Table 8. Design Requirements, SE Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 1 2V	12 V
High Power Supply	12 - 36 V
Mode Selection	M2 = H
	M1 = H
Analog Inputs	INPUT_A = ±3.9 V (peak, max)
	INPUT_B = ±3.9 V (peak, max)
	INPUT_C = ±3.9 V (peak, max)
	INPUT_D = ±3.9 V (peak, max)
Output Filters	Inductor-Capacitor Low Pass FIlter (15 µH + 680 nF)
Speaker Impedance	2 - 8 Ω

10.2.3.2 Detailed Design Procedures

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

10.2.3.3 Application Curves

Relevant performance plots for TPA3251D2 in PBTL configuration are shown in *Typical Characteristics, SE Configuration*

Table 9. Relevant Performance Plots, SE Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Output Power	Figure 10
Total Harmonic Distortion+Noise vs Frequency	Figure 11
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 12
Output Power vs Supply Voltage, 10% THD+N	Figure 13
Output Power vs Supply Voltage, 1% THD+N	Figure 14
Output Power vs Case Temperature	Figure 15

10.2.4 Typical Application, Differential (2N) PBTL

TPA3251D2 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

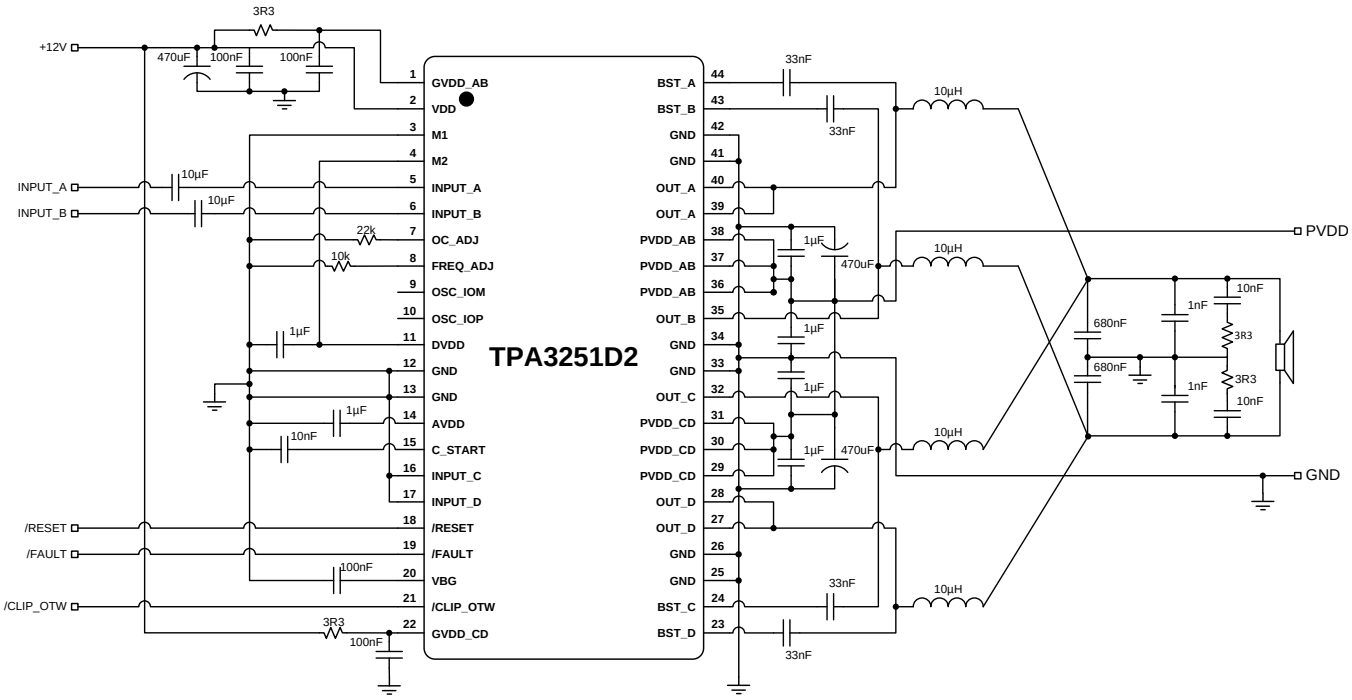


Figure 27. Typical Differential (2N) PBTL Application

10.2.4.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

Table 10. Design Requirements, PBTL Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 12 V	12 V
High Power Supply	12 - 36 V
Mode Selection	M2 = H
	M1 = L
Analog Inputs	INPUT_A = ±3.9V (peak, max)
	INPUT_B = ±3.9V (peak, max)
	INPUT_C = Grounded
	INPUT_D = Grounded
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	2 - 4 Ω

10.2.4.2 Detailed Design Procedures

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

10.2.4.3 Application Curves

Relevant performance plots for TPA3251D2 in PBTL configuration are shown in *Typical Characteristics, PBTL Configuration*

Table 11. Relevant Performance Plots, PBTL Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Output Power	Figure 16
Total Harmonic Distortion+Noise vs Frequency	Figure 17
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 18
Output Power vs Supply Voltage, 10% THD+N	Figure 19
Output Power vs Supply Voltage, 1% THD+N	Figure 20
Output Power vs Case Temperature	Figure 21

11 Power Supply Recommendations

11.1 Power Supplies

The TPA3251D2 device requires two external power supplies for proper operation. A high-voltage supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one mid-voltage power supply for GVDD_X and VDD is required to power the gate-drive and other internal digital and analog portions of the device. The allowable voltage range for both the PVDD and the GVDD_X/VDD supplies are listed in the *Recommended Operating Conditions* table. Ensure both the PVDD and the GVDD_X/VDD supplies can deliver more current than listed in the *Electrical Characteristics* table.

11.1.1 VDD Supply

The VDD supply required from the system is used to power several portions of the device. It provides power to internal regulators DVDD and AVDD that are used to power digital and analog sections of the device, respectively. Proper connection, routing, and decoupling techniques are highlighted in the TPA3251D2 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3251D2 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3251D2 device. Some portions of the device also require a separate power supply which is a lower voltage than the VDD supply. To simplify the power supply requirements for the system, the TPA3251D2 device includes integrated low-dropout (LDO) linear regulators to create these supplies. These linear regulators are internally connected to the VDD supply and their outputs are presented on AVDD and DVDD pins, providing a connection point for an external bypass capacitors. It is important to note that the linear regulators integrated in the device have only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on these pins could cause the voltage to sag and increase noise injection, which negatively affects the performance and operation of the device.

11.1.2 GVDD_X Supply

The GVDD_X supply required from the system is used to power the gate-drives for the output H-bridges. Proper connection, routing, and decoupling techniques are highlighted in the TPA3251D2 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3251D2 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3251D2 device.

Power Supplies (continued)

11.1.3 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TPA3251D2 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TPA3251D2 device EVM User's Guide SLVUAG8. The lack of proper decoupling, like that shown in the EVM User's Guide, can results in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults.

11.2 Powering Up

The TPA3251D2 does not require a power-up sequence, but it is recommended to hold $\overline{\text{RESET}}$ low minimum 400ms after PVDD supply voltage is turned ON. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

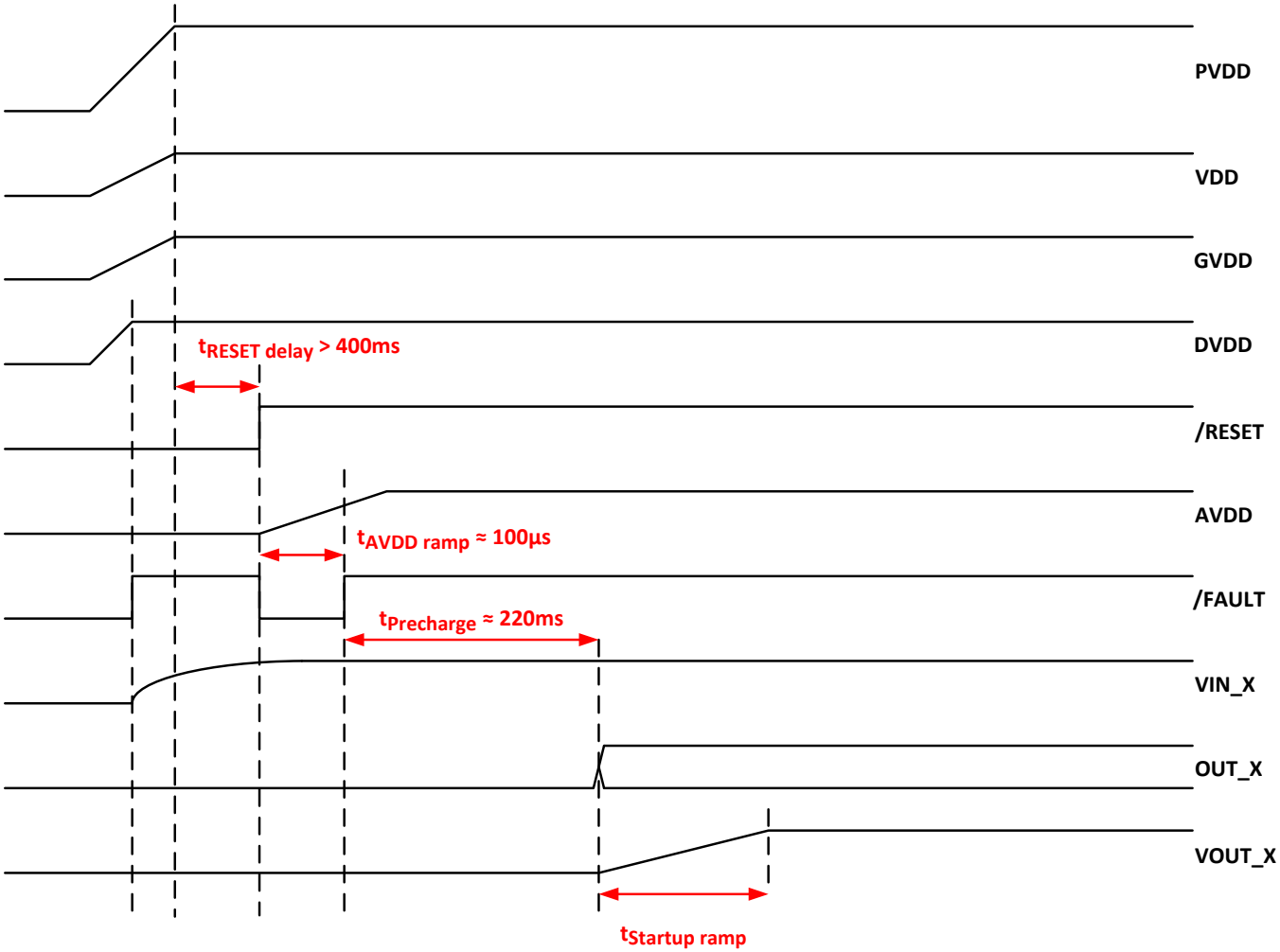


Figure 28. Startup Timing

Powering Up (continued)

When $\overline{\text{RESET}}$ is released to turn on TPA3251D2, $\overline{\text{FAULT}}$ signal will turn low and AVDD voltage regulator will be enabled. $\overline{\text{FAULT}}$ will stay low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). After a precharge time to stabilize the DC voltage across the input AC coupling capacitors, before the ramp up sequence starts.

11.3 Powering Down

The TPA3251D2 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks by initiating a controlled ramp down sequence of the output voltage.

12 Layout

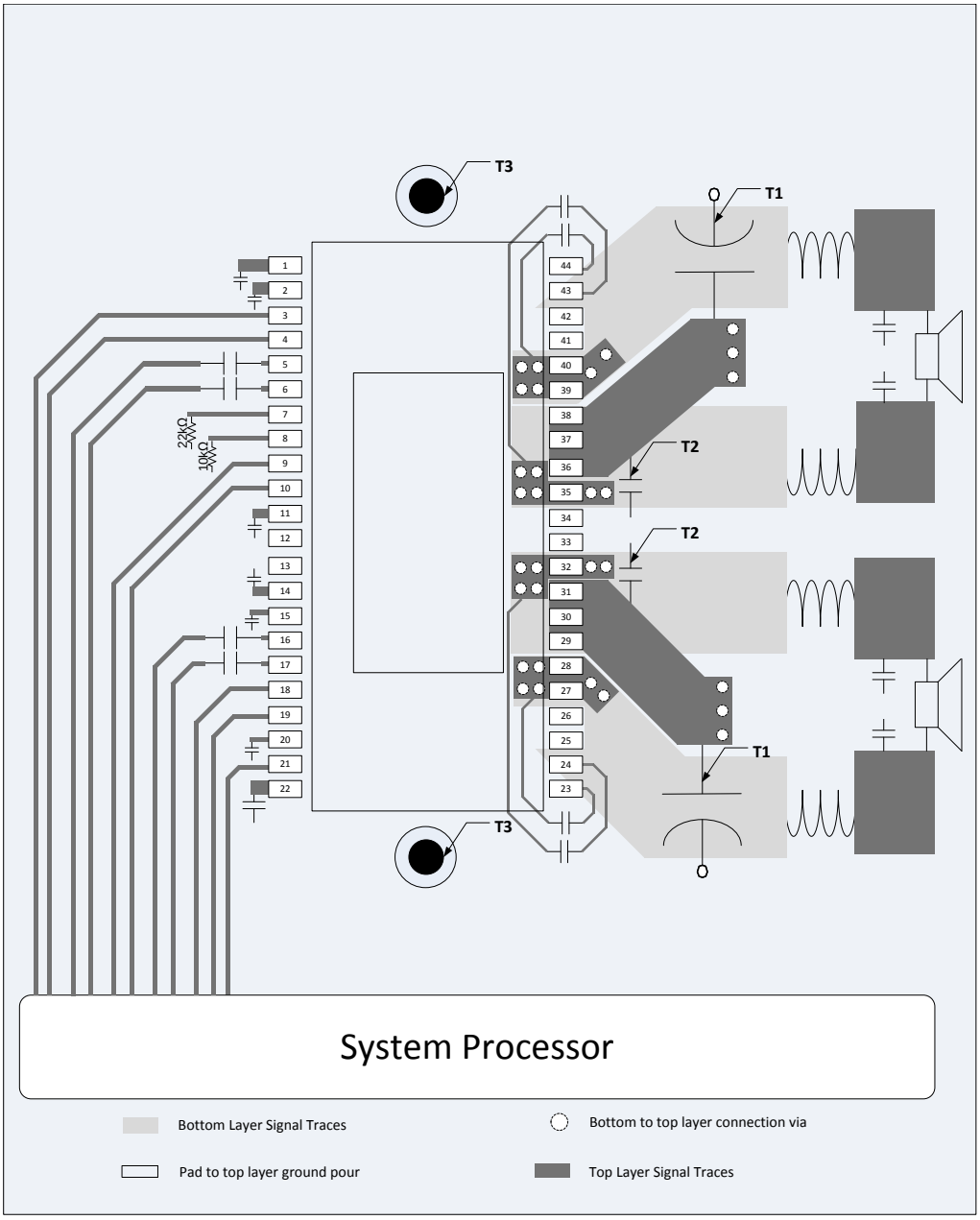
12.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible.
- A local ground area underneath the device is important to keep solid to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TPA3251D2 device, unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads.
- Avoid placing other heat producing components or structures near the TPA3251D2 device.
- Avoid cutting off the flow of heat from the TPA3251D2 device to the surrounding ground areas with traces or via strings, especially on output side of device.

Netlist for this printed circuit board is generated from the schematic in Figure 29.

12.2 Layout Examples

12.2.1 BTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

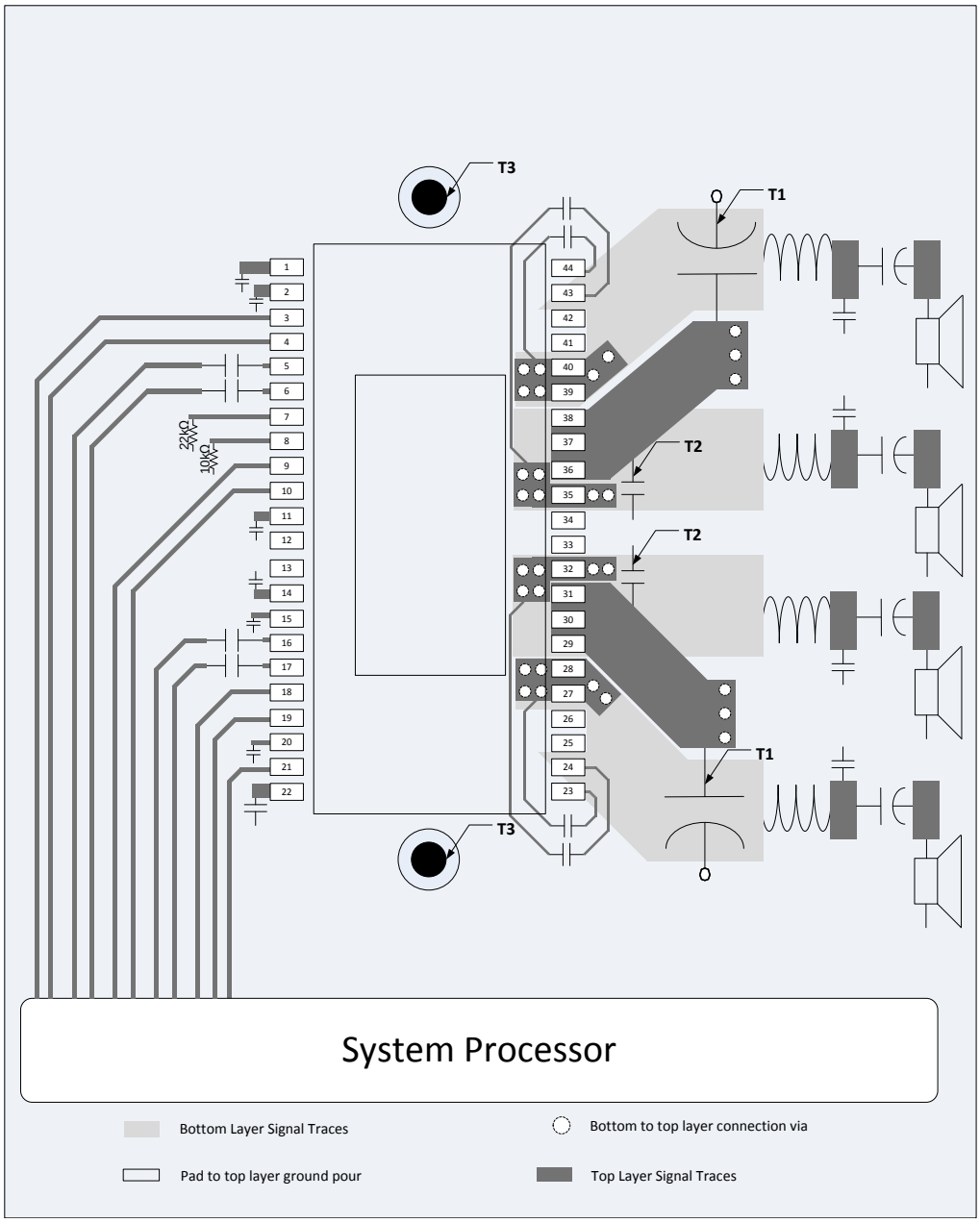
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

Figure 29. BTL Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.2 SE Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

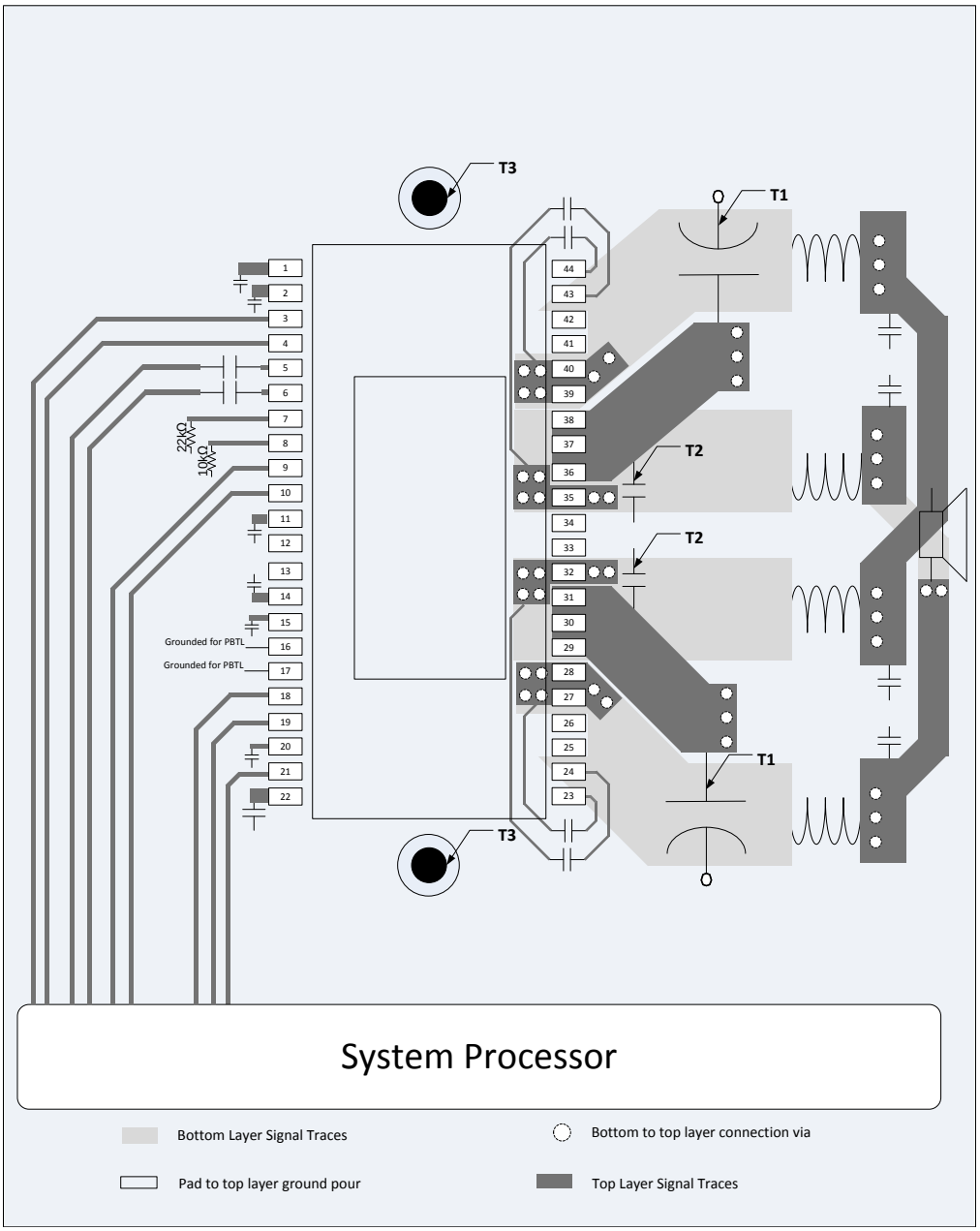
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

Figure 30. SE Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.3 PBTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **ote T3**: Heat sink needs to have a good connection to PCB ground.

Figure 31. PBTL Application Printed Circuit Board - Composite

13 器件和文档支持

13.1 文档支持

《TPA3251D2EVM 用户指南》，SLVUAG8

13.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商标

PurePath, E2E are trademarks of Texas Instruments.
蓝光碟磁盘 is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3251D2DDV	ACTIVE	HTSSOP	DDV	44	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	3251	Samples
TPA3251D2DDVR	ACTIVE	HTSSOP	DDV	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	3251	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

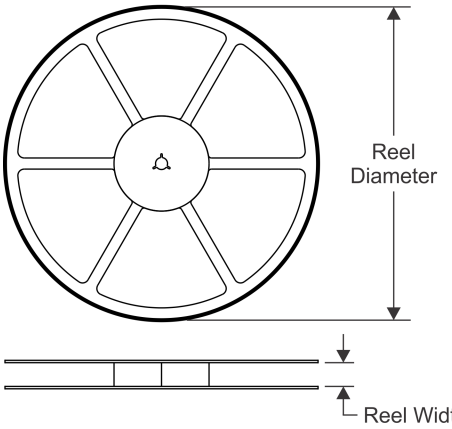
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

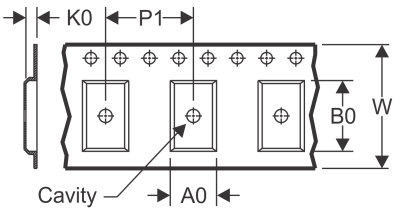
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

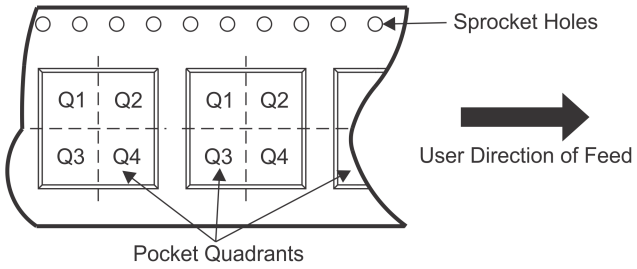


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

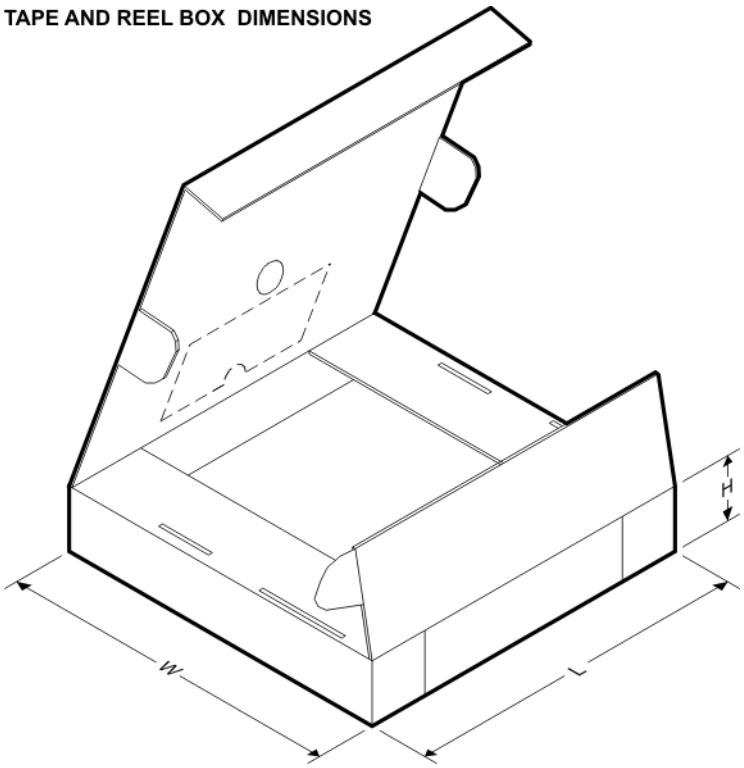
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3251D2DDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

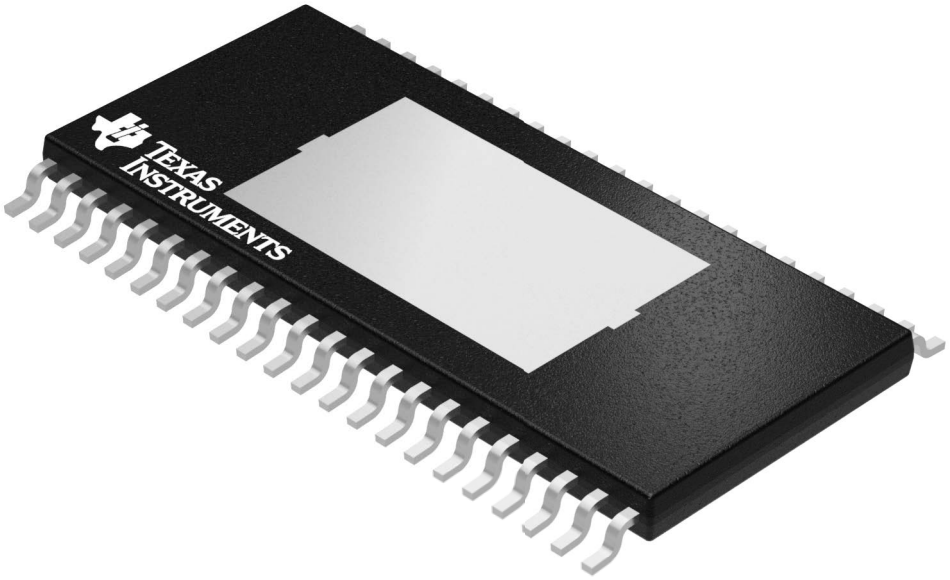


*All dimensions are nominal

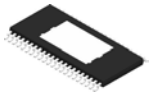
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3251D2DDVR	HTSSOP	DDV	44	2000	367.0	367.0	45.0

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

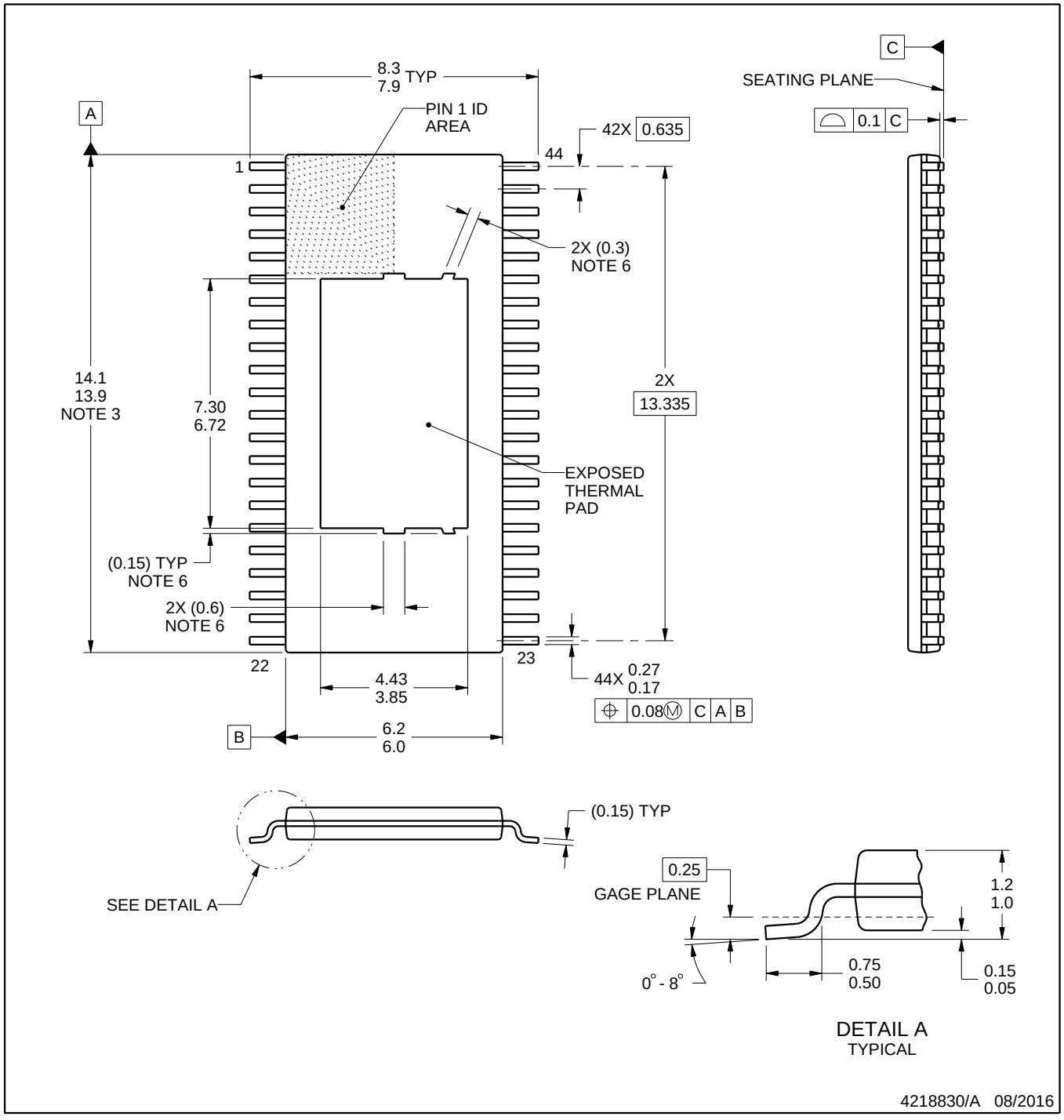


PACKAGE OUTLINE

DDV0044D

PowerPAD™ TSSOP - 1.2 mm max height

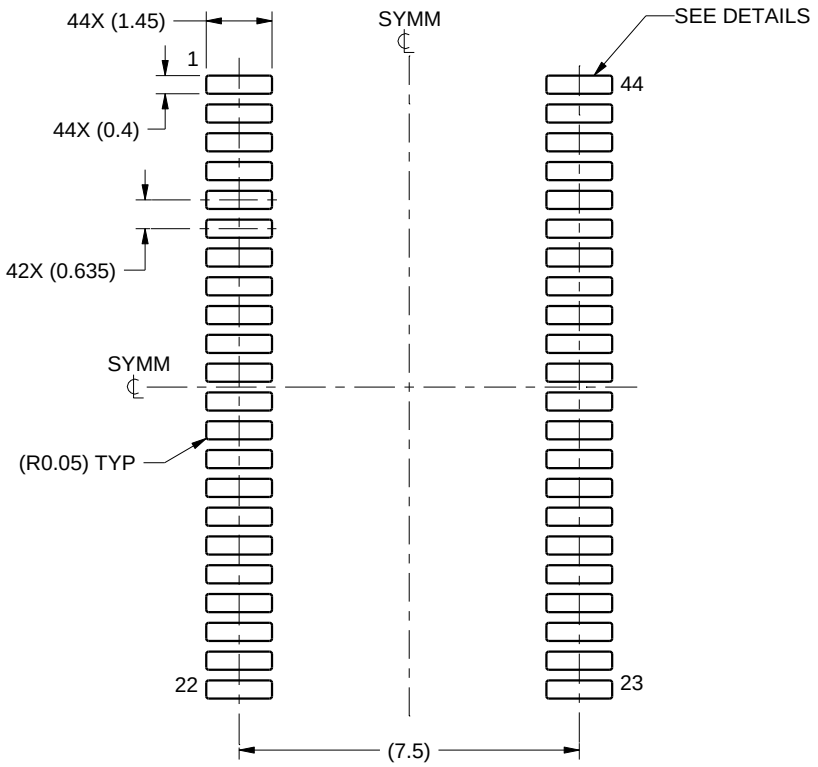
PLASTIC SMALL OUTLINE



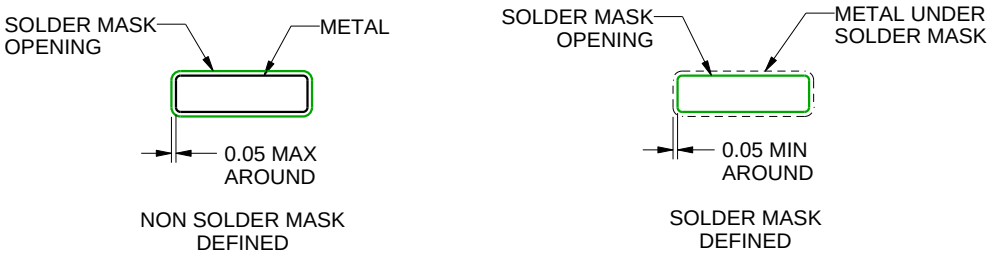
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

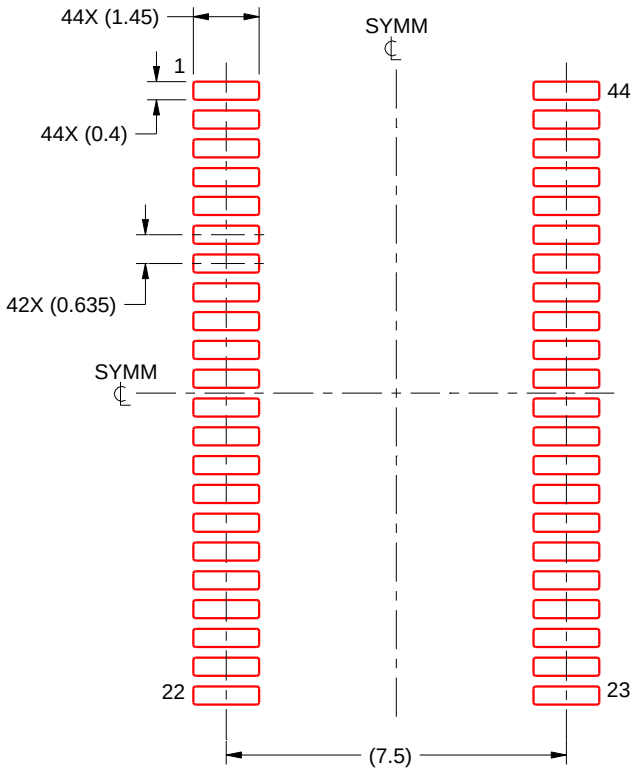


SOLDER MASK DETAILS
NOT TO SCALE

4218830/A 08/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

4218830/A 08/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265