

# TMS320C5545 定点数字信号处理器

## 1 器件概述

### 1.1 特性

- 核心：
  - 高性能、低功耗 TMS320C55x 定点数字信号处理器
    - 16.67ns、10ns 指令周期时间
    - 60MHz、100MHz 时钟速率
    - 每个周期执行一条或两条指令
    - 两个乘积累积 (MAC) 单元 (每秒高达 2 亿次乘积累加运算 [MMACS])
    - 两个算术和逻辑单元 (ALU)
    - 三个内部数据和操作数读取总线以及两个内部数据和操作数写入总线
    - 与 C55x 器件软件兼容
  - 320KB 零等待状态片上 RAM，包括：
    - 64KB 双访问 RAM (DARAM)，8 块 4K × 16 位
    - 256KB 单访问 RAM (SARAM)，32 块 4K × 16 位
  - 128KB 零等待状态片上 ROM (4 块 16K × 16 位)
  - 紧密耦合的快速傅立叶变换 (FFT) 硬件加速器
- 外设：
  - 直接内存访问 (DMA) 控制器
    - 四个 DMA，每个 DMA 有 4 个通道 (共 16 条通道)
  - 三个 32 位通用 (GP) 定时器
    - 一个可选用为看门狗或 GP
  - 两个嵌入式多媒体卡 (eMMC) 和安全数字 (SD) 接口
  - 通用异步收发器 (UART)
  - 具有三芯片选择的串行端口接口 (SPI)
  - 主控和受控内部集成电路 (I<sup>2</sup>C 总线)
- 四个用于数据传输的内部集成电路 (IC) 声音 (I2S 总线)
- 带有集成型 2.0 高速物理层 (PHY) 的器件 USB 端口，支持：
  - USB 2.0 全速和高速器件
- 具有异步接口的 LCD 桥
- 10 位 3 输入逐次逼近 (SAR) 模数转换器 (ADC)
- IEEE 1149.1 (JTAG) 边界扫描兼容
- 多达 32 个通用 I/O (GPIO) 引脚 (与其他器件功能复用)
  - 最多可同时配置 20 个 GPIO 引脚
- 电源：
  - 四个内核隔离电源域：模拟、RTC、CPU 和外设以及 USB
  - 三个 I/O 隔离电源域：RTC I/O、USB 物理层 (PHY) 和 DV<sub>DDIO</sub>
  - 提供三个集成低压降稳压器 (LDO) (DSP\_LDO、ANA\_LDO 和 USB\_LDO) 分别为以下隔离域供电：DSP 内核、模拟和 USB 内核
  - 1.05V 内核 (60MHz)，1.8V、2.5V、2.75V 或 3.3V I/O
  - 1.3V 内核 (100MHz)，1.8V、2.5V、2.75V 或 3.3V I/O
- 时钟：
  - 通过支持 11.2896MHz、12.000MHz 和 12.288MHz 时钟频率的 CLKIN 引脚提供外部时钟源
  - 具有 32.768kHz 晶振输入、独立时钟域和独立电源的实时时钟 (RTC)
  - 低功耗软件可编程锁相环 (PLL) 时钟发生器
- 引导加载程序：
  - 片上 ROM 引导加载程序 (RBL)，可从 SPI EEPROM、SPI 串行闪存或 I<sup>2</sup>C EEPROM eMMC、SD、SDHC、UART 和 USB 启动
- 封装：
  - 118 端子无铅塑料 BGA (球栅阵列) 封装 (后缀 ZQW)



## 1.2 应用

- 无线音频器件（例如：头戴式耳机、麦克风、免提电话）
- 回声消除耳机
- 便携式医疗设备
- 语音应用
- 工业控制
- 指纹识别
- 软件定义无线电

## 1.3 说明

这些器件是 TI C5000™ 定点数字信号处理器 (DSP) 产品系列的成员之一，适用于低功耗应用。选择。

定点 DSP 基于 TMS320C55x DSP 系列 CPU 处理器内核。C55x DSP 架构通过提升的并行性和节能性能实现高性能和低功耗。CPU 支持一个内部总线结构，此结构包含一条程序总线，一条 32 位读取总线和两条 16 位数据读取总线，两条数据写入总线和专门用于外设和 DMA 操作的附加总线。这些总线可实现在一个单周期内执行高达四次 16 位数据读取和两次 16 位数据写入的功能。此器件还包含四个 DMA 控制器，每个控制器具有 4 条通道，可在无需 CPU 干预的情况下提供 16 条独立通道的数据传送。每个 DMA 控制器在每周可执行一个 32 位数据传输，此数据传输与 CPU 的运行并行并且不受 CPU 运行的影响。

C55x CPU 提供两个乘积累积 (MAC) 单元，每个单元在一个单周期内能够进行 17 位 × 17 位乘法以及 32 位加法。一个中央 40 位算术和逻辑单元 (ALU) 由一个附加 16 位 ALU 提供支持。ALU 的使用受指令集控制，从而提供优化并行运行和功耗的能力。C55x CPU 内的地址单元 (AU) 和数据单元 (DU) 对这些资源进行管理。

C55x CPU 支持一个可变字节宽度指令集以改进代码密度。指令单元 (IU) 执行内部或外部存储器中的 32 位程序取指令并且进行针对程序单元 (PU) 的指令排队。PU 对指令进行解码，将任务指向地址单元和数据单元资源，并管理受到完全保护的管线。跳转预测功能避免了条件指令执行时的管线冲刷。

GPIO 功能与 10 位 SAR ADC 一起为状态、中断以及用于 LCD 显示屏、键盘和媒体接口的位 I/O 提供足够的引脚。通过以下器件对串行媒体提供支持：两个安全数字 (SD) 外设、四个内部 IC 声音 (I2S 总线) 模块、一个具有多达三芯片选择的串行端口接口 (SPI)、一个内部集成电路 (I<sup>2</sup>C) 主控和受控接口和一个通用异步收发器 (UART) 接口。

其他外设包括：一条仅支持器件模式的高速通用串行总线 (USB2.0)、一个实时时钟 (RTC)、三个通用 (GP) 定时器（其中一个可配置为看门狗定时器）和一个模拟锁相环 (APLL) 时钟发生器。

此外，该器件还包括紧密耦合 FFT 硬件加速器。紧密耦合 FFT 硬件加速器支持 8 至 1024 点 (2 的幂) 实值和复值 FFT。

器件中还包括以下三个集成 LDO，用于为器件的各个部分供电。

ANA\_LDO 为 DSP PLL ( $V_{DDA\_PLL}$ )、SAR 和电源管理电路 ( $V_{DDA\_ANA}$ ) 提供 1.3V 电压。

DSP\_LDO 为 DSP 内核 ( $CV_{DD}$ )（一旦检测到工作频率范围，便可由软件实时进行选择）提供 1.3V 或 1.05V 电压。

USB\_LDO 为 USB 内核数字电路 ( $USB\_V_{DD1P3}$ ) 和物理层电路 ( $USB\_V_{DDA1P3}$ ) 提供 1.3 V 电压。

这些器件由业界备受赞誉的 eXpressDSP™、Code Composer Studio™ 集成开发环境 (IDE)、DSP/BIOS™、德州仪器 (TI) 的算法标准和业界最大的第三方网络提供支持。Code Composer Studio IDE 提供的代码生成工具包括一个 C 语言编译器和连接器、RTDX™、XDS100、XDS510™、XDS560™ 仿真器件驱动程序和评估模块。这些器件也受 C55x DSP 库以及芯片支持库的支持，此库特有 50 多个基础软件内核（FIR 滤波器、IIR 滤波器、FFT 和多种数学函数）和芯片支持库。

### 器件信息<sup>(1)</sup>

| 产品型号         | 封装                         | 封装尺寸            |
|--------------|----------------------------|-----------------|
| TMS320C5545A | MicroStar JUNIOR BGA™(118) | 7.00mm x 7.00mm |

(1) 更多信息请参见 Section 8，机械封装和可订购产品信息。

### 1.4 功能方框图

图 1-1 显示了器件的功能方框图。

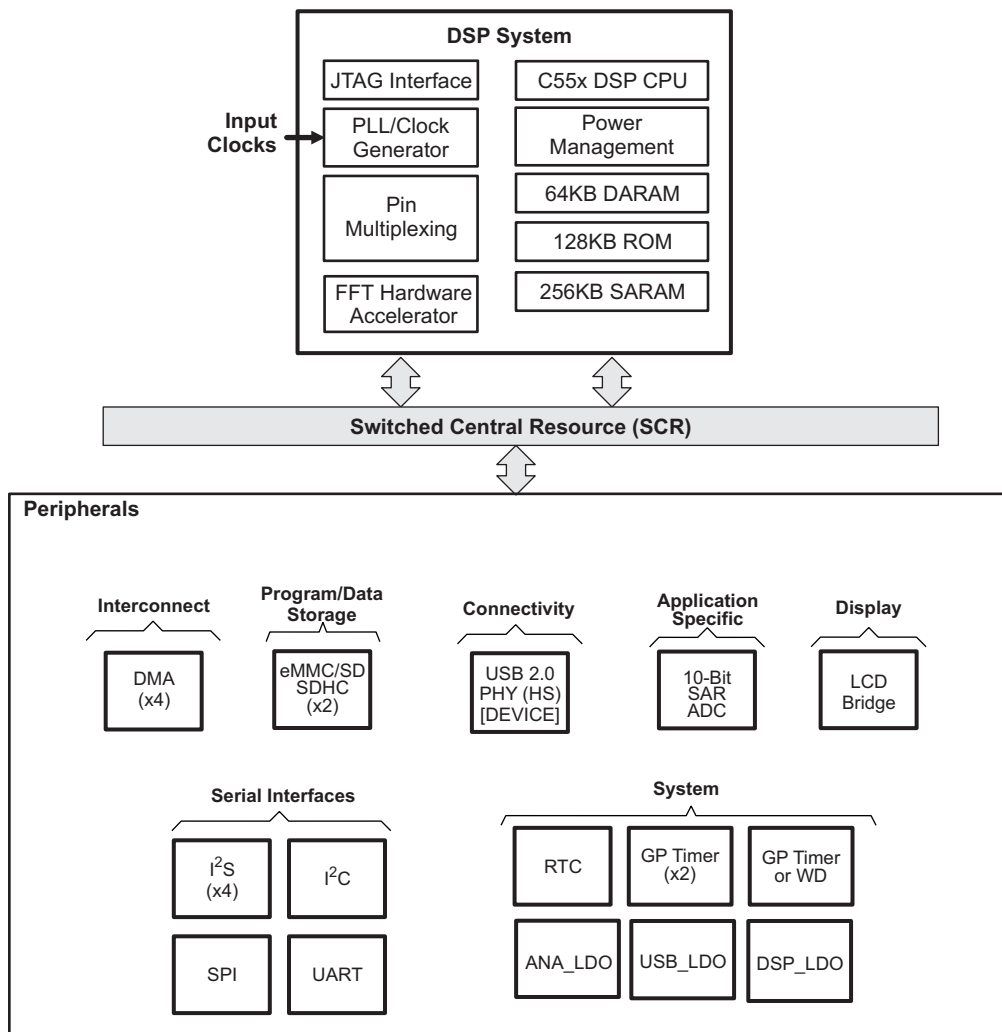


图 1-1. 功能方框图

## 内容

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## 2 修订历史记录

| Changes from Revision B (May 2015) to Revision C   | Page                |
|--|---------------------|
| • 删除了 120MHz 信息 .....  | <a href="#">1</a>   |
| • 已将 特性 由“10 位 4 输入逐次 ...”更新/更改为“10 位 3 输入逐次 ...” .....  | <a href="#">1</a>   |
| • Updated/Changed LDO1 DESCRIPTION in <a href="#">Table 4-14</a> .....                                       | <a href="#">28</a>  |
| • Updated/Changed LDO1 MIN NOM and MAX info in <a href="#">Section 5.3</a> .....                             | <a href="#">35</a>  |
| • Added <a href="#">Section 5.4, Power Consumption Summary</a> .....   | <a href="#">35</a>  |
| • Removed Core supply power rows from <a href="#">Section 5.5</a> .....                                      | <a href="#">37</a>  |
| • Updated/Changed BG_PD BIT column in <a href="#">Table 5-4</a> from "1-Don'tCare-0-0-0" to "1-0-0-0" .....  | <a href="#">41</a>  |
| • Updated/Changed SILICON REVISION from "Revision 2.2" to "Revision 2.4" in <a href="#">Figure 7-1</a> ..... | <a href="#">122</a> |

## 3 Device Comparison

### 3.1 Device Characteristics

Table 3-1 shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count. For more detailed information on the actual device part number and maximum device operating frequency, see Section 7.1, *Device and Development-Support Tool Nomenclature*.

**Table 3-1. Characteristics of the Processor**

| HARDWARE FEATURES   |  | TMS320C5545A   |          |
|---|--|--|----------|
| Peripherals<br>Not all peripheral pins are available at the same time (for more detail, see Section 6). | DMA  | Four DMA controllers each with four channels, for a total of 16 channels   |          |
|   | Timers                                     | Two 32-bit General-Purpose (GP) Timers<br>1 additional timer configurable as a 32-Bit GP Timer or a watchdog   |          |
|   | UART                                       | 1 (with RTS and CTS flow control)  |          |
|   | SPI  | 1 (with 3 chip selects)  |          |
|   | I <sup>2</sup> C                           | 1 (master or slave)  |          |
|   | I2S  | 4 (2-channel, full-duplex communication)   |          |
|   | USB 2.0 (device only)                      | High- and full-speed device  |          |
|   | SD   | 2 SD, 256-byte read and write buffer, maximum 50-MHz clock and signaling for DMA transfers   |          |
|   | LCD bridge                                 | 1 (8-bit or 16-bit asynchronous parallel bus)  |          |
|   | ADC (Successive Approximation [SAR])       | 1 (10-bit, 3-input, 16- $\mu$ s conversion time)   |          |
|   | RTC  | 1 (crystal input, separate clock domain, and power supply)   |          |
|   | FFT hardware accelerator                   | 1 (Supports 8- to 1024-point, 16-bit real and complex FFT)   |          |
|   | GPIO port                                  | 32 pins and 3 special-purpose outputs for use with SAR<br>Configure up to 20 pins simultaneously   |          |
| On-Chip Memory  | Size (bytes)                               | 320KB of RAM, 128KB of ROM   |          |
|   | Organization                               | <ul style="list-style-type: none"> <li>• 64KB of on-chip dual-access RAM (DARAM)</li> <li>• 256KB of on-chip single-access RAM (SARAM)</li> <li>• 128 KB of on-chip single-access ROM (SAROM)</li> </ul> |          |
| JTAG BSDL_ID  | JTAGID register<br>(Value is: 0x1B8F E02F) | See Figure 5-38.   |          |
| CPU Frequency   | MHz  | 1.05-V Core  | 60 MHz   |
|   |  | 1.3-V Core   | 100 MHz  |
| Cycle Time  | ns   | 1.05-V Core  | 16.67 ns |
|   |  | 1.3-V Core   | 10 ns    |
| Voltage   | Core (V)                                   | 1.05 V to 60 MHz   |          |
|   |  | 1.3 V to 100 MHz   |          |
|   | I/O (V)                                    | 1.8 V, 2.5 V, 2.75 V, 3.3 V  |          |
| LDOs  | DSP_LDO                                    | 1.3 V or 1.05 V, 250 mA maximum current for DSP CPU (CV <sub>DD</sub> )  |          |
|   | ANA_LDO                                    | 1.3 V, 4 mA maximum current to supply power to PLL (V <sub>DDA_PLL</sub> ), SAR, and power-management circuits (V <sub>DDA_ANA</sub> )   |          |
|   | USB_LDO                                    | 1.3 V, 25 mA maximum current to supply power to USB core digital (USB_V <sub>DD1P3</sub> ) and PHY circuits (USB_V <sub>DDA1P3</sub> )   |          |
| PLL Options   | Software Programmable Multiplier           | x4 to x4099 multiplier   |          |
| BGA Package   | 7 mm x 7 mm                                | 118-pin BGA (ZQW)  |          |

**Table 3-1. Characteristics of the Processor (continued)**

| HARDWARE FEATURES             |   | TMS320C5545A |
|-------------------------------|---|--------------|
| Product Status <sup>(1)</sup> | Product Preview (PP),<br>Advance Information (AI),<br>or Production Data (PD) | PD           |

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

### 3.2 Related Products

For information about other devices in this family of products or related products, see the following links.

**Digital Signal Processor** DSPs bring computing performance, real-time processing, and power efficiency to diverse applications ranging from sensors to servers. Our product range spans high-performance real-time needs, to power-efficient processors with industry-leading lowest active power needs. Choose one of our scalable solutions below.

**C5000™ Ultra Low Power DSP** The C5000 ultra-low-power DSP platform includes a broad portfolio of the industry's lowest power 16-bit DSPs with performance up to 300MHz (600 MIPS). Ideal for portable devices in audio, voice and vision, and other applications requiring analytics with ultra-low power.

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagram

Extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using software-programmable register settings. For more information on pin muxing, see [Section 6.7, Multiplexed Pin Configurations](#).

Figure 4-1 shows the bottom view of the package pin assignments.

|   | 1   | 2   | 3  | 4                             | 5   | 6           | 7           | 8          | 9          | 10       | 11       | 12          |   |
|---|---|---|--|-------------------------------|---|-------------|-------------|------------|------------|----------|----------|-------------|---|
| M | LCD_D[13]/<br>UART_CTS/<br>GP[29]/<br>I2S3_FS | DVDDIO  | SD0_D2/<br>GP[4]                               | SD1_D2/<br>GP[10]             | RSV17                                       | USB_DM      | USB_VDDPLL  | USB_VDD1P3 | USB_VSSOSC | USB_LDOO | DSP_LDOO | DSP_LDOO_EN | M |
| L | LCD_D[14]/<br>UART_RXD/<br>GP[30]/<br>I2S3_RX | LCD_D[15]/<br>UART_TXD/<br>GP[31]/<br>I2S3_DX | SD1_D0/<br>I2S1_DX/<br>GP[8]                   | SD1_CMD/<br>I2S1_FS/<br>GP[7] | USB_VDD1P3                                  | USB_DP      | USB_VDDA3P3 | USB_VSSPLL | USB_MXI    | LDO1     | LDO1     | RSV0        | L |
| K | LCD_D[9]/<br>I2S2_FS/<br>GP[19]/<br>SPI_CS0   | LCD_D[11]/<br>I2S2_DX/<br>GP[27]/<br>SPI_TX   |  | VSS                           | USB_VBUS                                    | USB_VDDA1P3 | USB_R1      | USB_VDDOSC | USB_MXO    |          | RSV3     | VSSA_ANA    | K |
| J | LCD_D[7]/<br>GP[17]                           | SD0_CMD/<br>I2S0_FS/<br>GP[1]                 | LCD_D[12]/<br>UART_RTS/<br>GP[28]/<br>I2S3_CLK |                               |   |             |             |            | CVDD       | RSV5     | BG_CAP   | GPAIN3      | J |
| H | LCD_D[8]/<br>I2S2_CLK/<br>GP[18]/<br>SPI_CLK  | DVDDIO  | SD1_D1/<br>I2S1_RX/<br>GP[9]                   |                               | SD1_CLK/<br>I2S1_CLK/<br>GP[6]              | USB_VSS1P3  | USB_VSSA3P3 | USB_VSSREF |            | RSV4     | ANA_LDOO | VSSA_ANA    | H |
| G | LCD_D[5]/<br>GP[15]                           | SD0_D1/<br>I2S0_RX/<br>GP[3]                  | SD0_D3/<br>GP[5]                               |                               | SD1_D3/<br>GP[11]                           | VSS         | CVDD        | VSS        |            | LDO1     | VDDA_ANA | VSSRTC      | G |
| F | LCD_D[4]/<br>GP[14]                           | TRST  | VSS  |                               | LCD_D[10]/<br>I2S2_RX/<br>GP[20]/<br>SPI_RX |             | VSS         | GPAIN1     |            | GPAIN2   | RTC_XI   | DVDDRTC     | F |
| E | LCD_D[3]/<br>GP[13]                           | LCD_D[2]/<br>GP[12]                           | LCD_D[6]/<br>GP[16]                            |                               | SD0_CLK/<br>I2S0_CLK/<br>GP[0]              | CVDD        |             | VSSA_PLL   |            | VDDA_PLL | RTC_XO   | CLKIN       | E |
| D | TDO   | DVDDIO  | TMS  |                               | SD0_D0/<br>I2S0_DX/<br>GP[2]                |             |             |            |            | CVDDRTC  | SDA      | CLK_SEL     | D |
| C | TCK   | LCD_D[1]/<br>SPI_TX                           |  | VSS                           |   | CVDD        | VSS         |            | VSS        |          | INT1     | CLKOUT      | C |
| B | EMU1  | LCD_RW_<br>WRB/<br>SPI_CS2                    | EMU0   | TDI                           | CVDD  | VSS         | VSS         | CVDD       | VSS        | DVDDIO   | SCL      | INT0        | B |
| A | LCD_EN_<br>RDB/<br>SPI_CLK                    | LCD_CS0_EO/<br>SPI_CS0                        | LCD_RS/<br>SPI_CS3                             | LCD_D[0]/<br>SPI_RX           | VSS   | VSS         | VSS         | VSS        | CVDD       | VSS      | RESET    | VSS         | A |

Figure 4-1. Pin Diagram (Bottom View)



## 4.2 Terminal Functions

For proper device operation, external pullup and pulldown resistors may be required on some pins. [Section 6.8.1, Pullup and Pulldown Resistors](#), discusses situations where external pullup and pulldown resistors are required.

### 4.2.1 Oscillator and PLL Terminal Functions

[Table 4-1](#) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see [Section 6, Device Configuration](#).

**Table 4-1. Oscillator and PLL Terminal Functions**

| SIGNAL               |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)  | DESCRIPTION   |
|----------------------|-----|-----------------|---|---|
| NAME                 | NO. |                 |   |   |
| CLKOUT               | C12 | O/Z             | –<br>DV <sub>DDIO</sub><br>BH                                     | <p>DSP clock output signal. For debug purposes only, the CLKOUT pin can be used to tap different clocks within the system clock generator. The SRC bits in the CLKOUT Control Source Register (CCSSR) can be used to specify the source of the CLKOUT pin. Additionally, the slew rate of the CLKOUT pin can be controlled by the Output Slew Rate Control Register (OSRCR) [1C16h].</p> <p>The CLKOUT pin is enabled and disabled through the CLKOFF bit in the CPU ST3_55 register. When disabled, the CLKOUT pin is placed in high-impedance (Hi-Z). At reset the CLKOUT pin is enabled until the beginning of the boot sequence, when the on-chip bootloader sets CLKOFF = 1 and the CLKOUT pin is disabled (Hi-Z). For more information on the ST3_55 register, see the <i>TMS320C55x 3.0 CPU Reference Guide (SWPU073)</i>.</p> <p><b>Note:</b> This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin.</p> |
| CLKIN                | E12 | I               | –<br>DV <sub>DDIO</sub><br>BH                                     | <p>Input clock. This signal is used to input an external clock when the 32-kHz on-chip oscillator is not used as the DSP clock (pin CLK_SEL = 1). For boot purposes, the CLKIN frequency is assumed to be either 11.2896, 12, or 12.288 MHz.</p> <p>The CLK_SEL pin (D12) selects between the 32-kHz crystal clock or CLKIN.</p> <p>When the CLK_SEL pin is low, this pin must be tied to ground (V<sub>SS</sub>). When CLK_SEL is high, this pin must be driven by an external clock source.</p> <p>If CLK_SEL is high, this pin is used as the reference clock for the clock generator. During bootup, the bootloader bypasses the PLL and assumes the CLKIN frequency is one of the following frequencies: 11.2896, 12, or 12.288 MHz. In addition, the bootloader sets the SPI clock rate at 500 kHz and the I2C clock rate at 400 kHz.</p>   |
| CLK_SEL              | D12 | I               | –<br>DV <sub>DDIO</sub><br>BH                                     | <p>Clock input select. This pin selects between the 32-kHz crystal clock or CLKIN.</p> <p>0 = 32-kHz on-chip oscillator drives the RTC timer and the system clock generator while CLKIN is ignored.</p> <p>1 = CLKIN drives the system clock generator and the 32-kHz on-chip oscillator drives only the RTC timer.</p> <p>This pin is not allowed to change during device operation; it must be tied high or low at the board.</p>   |
| V <sub>DDA_PLL</sub> | E10 | PWR             | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | <p>1.3-V analog PLL power supply for the system clock generator (PLLOUT ≤ 100 MHz).</p> <p>This signal can be powered from the ANA_LDOO pin.</p>  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see [Section 6.8.1, Pullup and Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-1. Oscillator and PLL Terminal Functions (continued)**

| SIGNAL               |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)  | DESCRIPTION                                      |
|----------------------|-----|-----------------|---|--|
| NAME                 | NO. |                 |   |  |
| V <sub>SSA_PLL</sub> | E8  | GND             | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Analog PLL ground for the system clock generator |

#### 4.2.2 RTC Terminal Functions

[Table 4-2](#) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see [Section 6, Device Configuration](#).

**Table 4-2. Real-Time Clock Terminal Functions**

| SIGNAL |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)                        | DESCRIPTION   |
|--------|-----|-----------------|---|---|
| NAME   | NO. |                 |   |   |
| RTC_XO | E11 | I/O/Z           | –<br>CV <sub>DDRTC</sub><br>DV <sub>DDRTC</sub> | <p>Real-time clock oscillator output. This pin operates at the RTC core voltage, CV<sub>DDRTC</sub>, and supports a 32.768-kHz crystal.</p> <p>If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV<sub>DDRTC</sub> and RTC_XO to ground (V<sub>SS</sub>). A voltage must still be applied to CV<sub>DDRTC</sub> by an external power source (see <a href="#">Section 5.3, Recommended Operating Conditions</a>). None of the on-chip LDOs can be used to power CV<sub>DDRTC</sub>.</p> <p><b>Note:</b> When RTC oscillator is disabled, the RTC registers (I/O address range 1900h to 197Fh) are not accessible.</p> |
| RTC_XI | F11 | I               | –<br>CV <sub>DDRTC</sub><br>DV <sub>DDRTC</sub> | <p>Real-time clock oscillator input.</p> <p>If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV<sub>DDRTC</sub> and RTC_XO to ground (V<sub>SS</sub>). A voltage must still be applied to CV<sub>DDRTC</sub> by an external power source (see <a href="#">Section 5.3, Recommended Operating Conditions</a>). None of the on-chip LDOs can be used to power CV<sub>DDRTC</sub>.</p> <p><b>Note:</b> When RTC oscillator is disabled, the RTC registers (I/O address range 1900h to 197Fh) are not accessible.</p>  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see [Section 6.8.1, Pullup and Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

### 4.2.3 RESET, Interrupts, and JTAG Terminal Functions

Table 4-3 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-3. RESET, Interrupts, and JTAG Terminal Functions**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION  |
|--|-----|-----------------|---------------------------------|--|
| NAME   | NO. |                 |                                 |  |
| <b>RESET</b>   |     |                 |                                 |  |
| $\overline{\text{RESET}}$  | A11 | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>Device reset. <math>\overline{\text{RESET}}</math> causes the DSP to terminate execution and loads the program counter with the contents of the reset vector. When <math>\overline{\text{RESET}}</math> is brought to a high level, the reset vector in ROM at FFFF0h forces the program execution to branch to the location of the on-chip ROM bootloader.</p> <p><math>\overline{\text{RESET}}</math> affects the various registers and status bits.</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register but will be forced ON when <math>\overline{\text{RESET}}</math> is asserted.</p>   |
| <b>JTAG</b>  |     |                 |                                 |  |
| For more detailed information on emulation header design guidelines, see the <i>XDS560 Emulator</i> Technical Reference (SPRU589). |     |                 |                                 |  |
| TMS  | D3  | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>IEEE standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.</p> <p>If the emulation header is located more than 6 inches from the device, TMS must be buffered. In this case, the input buffer for TMS needs a pullup resistor connected to DV<sub>DDIO</sub> to hold the signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (SPRU589).</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.</p>  |
| TDO  | D1  | O/Z             | –<br>DV <sub>DDIO</sub><br>BH   | <p>IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance (Hi-Z) state except when the scanning of data is in progress.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (SPRU589).</p> <p>If the emulation header is located more than 6 inches from the device, TDO must be buffered.</p> <p><b>Note:</b> This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. TDO pin will be in Hi-Z whenever not doing emulation and boundary scan, so an external pullup is highly recommended.</p> |
| TDI  | B4  | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>IEEE standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.</p> <p>If the emulation header is located more than 6 inches from the device, TDI must be buffered. In this case, the input buffer for TDI needs a pullup resistor connected to DV<sub>DDIO</sub> to hold this signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested.</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.</p>  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-3. RESET, Interrupts, and JTAG Terminal Functions (continued)**

| SIGNAL                     |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION   |
|----------------------------|-----|-----------------|---------------------------------|---|
| NAME                       | NO. |                 |                                 |   |
| TCK                        | C1  | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.</p> <p>If the emulation header is located more than 6 inches from the device, TCK must be buffered.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (<a href="#">SPRU589</a>).</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.</p>  |
| $\overline{\text{TRST}}$   | F2  | I               | IPD<br>DV <sub>DDIO</sub><br>BH | <p>IEEE standard 1149.1 reset signal for test and emulation logic. <math>\overline{\text{TRST}}</math>, when high, allows the IEEE standard 1149.1 scan and emulation logic to take control of the operations of the device. If <math>\overline{\text{TRST}}</math> is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. The device will not operate properly if this reset pin is never asserted low.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (<a href="#">SPRU589</a>).</p> <p>TI recommends using an external pull-down resistor in addition to the IPD, especially if there is a long trace to an emulation header.</p>  |
| EMU1                       | B1  | I/O/Z           | IPU<br>DV <sub>DDIO</sub><br>BH | <p>Emulator 1 pin. EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic.</p> <p>An external pullup to DV<sub>DDIO</sub> is required to provide a signal rise time of less than 10 <math>\mu\text{sec}</math>. A 4.7-k<math>\Omega</math> resistor is suggested for most applications.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (<a href="#">SPRU589</a>).</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.</p>  |
| EMU0                       | B3  | I/O/Z           | IPU<br>DV <sub>DDIO</sub><br>BH | <p>Emulator 0 pin. When <math>\overline{\text{TRST}}</math> is driven low and then high, the state of the EMU0 pin is latched and used to connect the JTAG pins (TCK, TMS, TDI, TDO) to either the IEEE 1149.1 Boundary-Scan TAP (when the latched value of EMU0 = 0) or to the DSP Emulation TAP (when the latched value of EMU0 = 1). Once <math>\overline{\text{TRST}}</math> is high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic.</p> <p>An external pullup to DV<sub>DDIO</sub> is required to provide a signal rise time of less than 10 <math>\mu\text{sec}</math>. A 4.7-k<math>\Omega</math> resistor is suggested for most applications.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (<a href="#">SPRU589</a>).</p> <p>The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.</p> |
| <b>EXTERNAL INTERRUPTS</b> |     |                 |                                 |   |
| $\overline{\text{INT1}}$   | C11 | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>External interrupt inputs (<math>\overline{\text{INT1}}</math> and <math>\overline{\text{INT0}}</math>). These pins are maskable through their specific Interrupt Mask Register (IMR1, IMR0) and the interrupt mode bit. The pins can be polled and reset by their specific Interrupt Flag Register (IFR1, IFR0).</p>  |
| $\overline{\text{INT0}}$   | B12 | I               | IPU<br>DV <sub>DDIO</sub><br>BH | <p>The IPU resistor on these pins can be enabled or disabled through the PDINHIBR2 register.</p>  |

#### 4.2.4 I2C Terminal Functions

Table 4-4 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see [Section 6, Device Configuration](#).

**Table 4-4. Inter-Integrated Circuit (I2C) Terminal Functions**

| SIGNAL     |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup> | DESCRIPTION  |
|------------|-----|-----------------|--------------------------|--|
| NAME       | NO. |                 |                          |  |
| <b>I2C</b> |     |                 |                          |  |
| SCL        | B11 | I/O/Z           | DV <sub>DDIO</sub><br>BH | This pin is the I2C clock output. Per the I2C standard, an external pullup is required on this pin.              |
| SDA        | D11 | I/O/Z           | DV <sub>DDIO</sub><br>BH | This pin is the I2C bidirectional data signal. Per the I2C standard, an external pullup is required on this pin. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see [Section 6.8.1, Pullup and Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

## 4.2.5 I2S0 to I2S3 Terminal Functions

Table 4-5 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-5. Inter-IC Sound (I2S0 to I2S3) Terminal Functions**

| SIGNAL                         |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION  |
|--------------------------------|-----|-----------------|---------------------------------|--|
| NAME                           | NO. |                 |                                 |  |
| <b>INTERFACE 0 (I2S0)</b>      |     |                 |                                 |  |
| SD0_D0/<br>I2S0_DX/<br>GP[2]   | D5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For I2S, it is I2S0 transmit data output I2S0_DX.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.               |
| SD0_CLK/<br>I2S0_CLK/<br>GP[0] | E5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For I2S, it is I2S0 clock input/output I2S0_CLK.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.                |
| SD0_D1/<br>I2S0_RX/<br>GP[3]   | G2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For I2S, it is I2S0 receive data input I2S0_RX.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.                 |
| SD0_CMD/<br>I2S0_FS/<br>GP[1]  | J2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For I2S, it is I2S0 frame synchronization input/output I2S0_FS.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| <b>INTERFACE 1 (I2S1)</b>      |     |                 |                                 |  |
| SD1_D0/<br>I2S1_DX/<br>GP[8]   | L3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For I2S, it is I2S1 transmit data output I2S1_DX.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.               |
| SD1_CLK/<br>I2S1_CLK/<br>GP[6] | H5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For I2S, it is I2S1 clock input/output I2S1_CLK.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.                |
| SD1_D1/<br>I2S1_RX/<br>GP[9]   | H3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For I2S, it is I2S1 receive data input I2S1_RX.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.                 |
| SD1_CMD/<br>I2S1_FS/<br>GP[7]  | L4  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S2, and GPIO.<br>For I2S, it is I2S1 frame synchronization input/output I2S1_FS.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-5. Inter-IC Sound (I2S0 to I2S3) Terminal Functions (continued)**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|--|-----|-----------------|---------------------------------|--|
| NAME   | NO. |                 |                                 |  |
| <b>INTERFACE 2 (I2S2)</b>                      |     |                 |                                 |  |
| LCD_D[11]/<br>I2S2_DX/<br>GP[27]/<br>SPI_TX    | K2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI.<br>For I2S, it is I2S2 transmit data output I2S2_DX.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.                |
| LCD_D[8]/<br>I2S2_CLK/<br>GP[18]/<br>SPI_CLK   | H1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI.<br>For I2S, it is I2S2 clock input/output I2S2_CLK.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.                 |
| LCD_D[10]/<br>I2S2_RX/<br>GP[20]/<br>SPI_RX    | F5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI.<br>For I2S, it is I2S2 receive data input I2S2_RX.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.                  |
| LCD_D[9]/<br>I2S2_FS/<br>GP[19]/<br>SPI_CS0    | K1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, I2S2 and GPIO.<br>For I2S, it is I2S2 frame synchronization input/output I2S2_FS.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.        |
| <b>INTERFACE 3 (I2S3)</b>                      |     |                 |                                 |  |
| LCD_D[15]/<br>UART_TXD/<br>GP[31]/<br>I2S3_DX  | L2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.<br>For I2S, it is I2S3 transmit data output I2S3_DX.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.               |
| LCD_D[12]/<br>UART_RTS/<br>GP[28]/<br>I2S3_CLK | J3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.<br>For I2S, it is I2S3 clock input/output I2S3_CLK.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.                |
| LCD_D[14]/<br>UART_RXD/<br>GP[30]/<br>I2S3_RX  | L1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.<br>For I2S, it is I2S3 receive data input I2S3_RX.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.                 |
| LCD_D[13]/<br>UART_CTS/<br>GP[29]/<br>I2S3_FS  | M1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.<br>For I2S, it is I2S3 frame synchronization input/output I2S3_FS.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |



## 4.2.6 SPI Terminal Functions

Table 4-6 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-6. Serial Peripheral Interface (SPI) Terminal Functions**

| SIGNAL                                       |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION   |
|--|-----|-----------------|---------------------------------|---|
| NAME   | NO. |                 |                                 |   |
| <b>SERIAL PORT INTERFACE (SPI)</b>           |     |                 |                                 |   |
| LCD_CS0_E0/<br>SPI_CS0                       | A2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI chip select SPI_CS0.  |
| LCD_D[9]/<br>I2S2_FS/<br>GP[19]/<br>SPI_CS0  | K1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI chip select SPI_CS0.<br><br>The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_RW_WRB/<br>SPI_CS2                       | B2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI chip select SPI_CS2.  |
| LCD_RS/<br>SPI_CS3                           | A3  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI chip select SPI_CS3.  |
| LCD_EN_RDB/<br>SPI_CLK                       | A1  | O/Z             | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is clock output SPI_CLK.<br><br><b>Note:</b> This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. |
| LCD_D[8]/<br>I2S2_CLK/<br>GP[18]/<br>SPI_CLK | H1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is clock output SPI_CLK.<br><br>The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.   |
| LCD_D[11]/<br>SPI_TX                         | C2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI transmit data output.   |
| LCD_D[11]/<br>I2S2_DX/<br>GP[27]/<br>SPI_TX  | K2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI, this pin is SPI transmit data output.<br><br>The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.   |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal



**Table 4-6. Serial Peripheral Interface (SPI) Terminal Functions (continued)**

| SIGNAL                                      |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|---|-----|-----------------|---------------------------------|--|
| NAME  | NO. |                 |                                 |  |
| LCD_D[0]/<br>SPI_RX                         | A4  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI this pin is SPI receive data input.   |
| LCD_D[10]/<br>I2S2_RX/<br>GP[20]/<br>SPI_RX | F5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>Mux control through the PPMODE bits in the EBSR.<br>For SPI this pin is SPI receive data input.<br><br>The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |

### 4.2.7 UART Terminal Functions

Table 4-7 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-7. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|--|-----|-----------------|---------------------------------|--|
| NAME   | NO. |                 |                                 |  |
| <b>UART</b>                                    |     |                 |                                 |  |
| LCD_D[14]/<br>UART_RXD/<br>GP[30]/<br>I2S3_RX  | L1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>When used by UART, it is the receive data input UART_RXD.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[15]/<br>UART_TXD/<br>GP[31]/<br>I2S3_DX  | L2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>In UART mode, it is the transmit data output UART_TXD.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.    |
| LCD_D[13]/<br>UART_CTS/<br>GP[29]/<br>I2S3_FS  | M1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>In UART mode, it is the clear to send input UART_CTS.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.     |
| LCD_D[12]/<br>UART_RTS/<br>GP[28]/<br>I2S3_CLK | J3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>In UART mode, it is the ready to send output UART_RTS.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.    |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

## 4.2.8 USB 2.0 Terminal Functions

Table 4-8 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-8. Universal Serial Bus (USB) 2.0 Terminal Functions**

| SIGNAL         |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)                                 | DESCRIPTION  |
|----------------|-----|-----------------|--|--|
| NAME           | NO. |                 |  |  |
| <b>USB 2.0</b> |     |                 |  |  |
| USB_MXI        | L9  | I               | USB_VDDOSC   | 12-MHz crystal oscillator input<br>When the USB peripheral <i>is not</i> used, USB_MXI must be connected to ground (V <sub>SS</sub> ).<br>When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V <sub>IH</sub> requirement (see Section 5.3, <i>Recommended Operating Conditions</i> ). The USB_MXO remains unconnected and the USB_VSSOSC signal is connected to board ground (V <sub>SS</sub> ). |
| USB_MXO        | K9  | O/Z             | USB_VDDOSC   | 12-MHz crystal oscillator output<br>When the USB peripheral <i>is not</i> used, USB_MXO must be left unconnected.<br>When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V <sub>IH</sub> requirement (see Section 5.3, <i>Recommended Operating Conditions</i> ). The USB_MXO remains unconnected and the USB_VSSOSC signal is connected to board ground (V <sub>SS</sub> ).                      |
| USB_VDDOSC     | K8  | S               | See Section 5.3, <i>Recommended Operating Conditions</i> | 3.3-V power supply for USB oscillator.<br>When the USB peripheral <i>is not</i> used, USB_VDDOSC must be connected to ground (V <sub>SS</sub> ).   |
| USB_VSSOSC     | M9  | S               | See Section 5.3, <i>Recommended Operating Conditions</i> | Ground for USB oscillator<br>When the USB peripheral <i>is not</i> used, USB_VSSOSC must be connected to ground (V <sub>SS</sub> ).<br>When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V <sub>IH</sub> requirement (see Section 5.3, <i>Recommended Operating Conditions</i> ). The USB_MXO remains unconnected and the USB_VSSOSC signal is connected to board ground (V <sub>SS</sub> ).    |
| USB_VBUS       | K5  | A I/O           | See Section 5.3, <i>Recommended Operating Conditions</i> | USB power detect. 5-V input that signifies that VBUS is connected.<br>This signal must be powered on in the order listed in Section 5.6.5.1, <i>Power-Supply Sequencing</i> .<br>When the USB peripheral <i>is not</i> used, the USB_VBUS signal must be connected to ground (V <sub>SS</sub> ).   |
| USB_DP         | L6  | A I/O           | USB_VDDA3P3  | USB bidirectional Data Differential signal pair [positive and negative]<br>When the USB peripheral <i>is not</i> used, the USB_DP and USB_DM signals should both be tied to ground (V <sub>SS</sub> ).   |
| USB_DM         | M6  | A I/O           | USB_VDDA3P3  |  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-8. Universal Serial Bus (USB) 2.0 Terminal Functions (continued)**

| SIGNAL      |           | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)  | DESCRIPTION   |
|-------------|-----------|-----------------|---|---|
| NAME        | NO.       |                 |   |   |
| USB_R1      | K7        | A I/O           | USB_VDDA3P3   | External resistor connect. Reference current output. This must be connected through a 10-kΩ ±1% resistor to USB_VSSREF and placed as close to the device as possible.<br><br>When the USB peripheral is not used, the USB_R1 signal must be connected through a 10-kΩ resistor to ground (V <sub>SS</sub> ).                |
| USB_VSSREF  | H8        | GND             | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Ground for reference current. This must be connected through a 10-kΩ ±1% resistor to USB_R1.<br><br>When the USB peripheral is not used, the USB_VSSREF signal must be connected directly to ground (V <sub>SS</sub> ).   |
| USB_VDDA3P3 | L7        | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Analog 3.3-V power supply for USB PHY<br><br>This signal must be powered on in the order listed in <a href="#">Section 5.6.5.1, Power-Supply Sequencing</a> .<br><br>When the USB peripheral is not used, the USB_VDDA3P3 signal must be connected to ground (V <sub>SS</sub> ).  |
| USB_VSSA3P3 | H7        | GND             | See <a href="#">Section 5.3, ROC</a>                              | Analog ground for USB PHY   |
| USB_VDDA1P3 | K6        | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Analog 1.3-V power supply for USB PHY (For high-speed sensitive analog circuits)<br><br>This signal must be powered on in the order listed in <a href="#">Section 5.6.5.1, Power-Supply Sequencing</a> .<br><br>When the USB peripheral is not used, the USB_VDDA1P3 signal must be connected to ground (V <sub>SS</sub> ). |
| USB_VDD1P3  | L5,<br>M8 | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | 1.3-V digital core power supply for USB PHY.<br><br>This signal must be powered on in the order listed in <a href="#">Section 5.6.5.1, Power-Supply Sequencing</a> .<br><br>When the USB peripheral is not used, the USB_VDD1P3 signal must be connected to ground (V <sub>SS</sub> ).                                      |
| USB_VSS1P3  | H6        | GND             | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Digital core ground for USB PHY. Analog ground for USB PHY (For high-speed sensitive analog circuits)   |
| USB_VDDPLL  | M7        | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | 3.3-V USB analog PLL power supply<br><br>When the USB peripheral <b>is not</b> used, the USB_VDDPLL signal must be connected to ground (V <sub>SS</sub> ).  |
| USB_VSSPLL  | L8        | GND             | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | USB analog PLL ground   |

## 4.2.9 LCD Terminal Functions

Table 4-9 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-9. LCD Bridge Terminal Functions**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION  |
|--|-----|-----------------|---------------------------------|--|
| NAME   | NO. |                 |                                 |  |
| LCD_EN_RDB/<br>SPI_CLK                         | A1  | O/Z             | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, this pin is either LCD bridge read and write enable (MPU68 mode) or read strobe (MPU80 mode).<br>Mux control through the PPMODE bits in the EBSR.<br><b>Note:</b> This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. |
| LCD_CS0_E0/<br>SPI_CS0                         | A2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, this pin is either LCD bridge chip select 0 (MPU68 and MPU80 modes) or enable 0 (HD44780 mode).<br>Mux control through the PPMODE bits in the EBSR.   |
| LCD_RW_WRB/<br>SPI_CS2                         | B2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, this pin is either LCD bridge read and write select (HD44780 and MPU68 modes) or write strobe (MPU80 mode).<br>Mux control through the PPMODE bits in the EBSR.   |
| LCD_RS/<br>SPI_CS3                             | A3  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, this pin is the LCD bridge address setup.<br>Mux control through the PPMODE bits in the EBSR.   |
| LCD_D[15]/<br>UART_TXD/<br>GP[31]/<br>I2S3_DX  | L2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For LCD bridge, it is LCD data pin 15.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[14]/<br>UART_RXD/<br>GP[30]/<br>I2S3_RX  | L1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For LCD bridge, it is LCD data pin 14.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[13]/<br>UART_CTS/<br>GP[29]/<br>I2S3_FS  | M1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For LCD bridge, it is LCD data pin 13.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[12]/<br>UART_RTS/<br>GP[28]/<br>I2S3_CLK | J3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, and GPIO.<br>For LCD bridge, it is LCD data pin 12.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-9. LCD Bridge Terminal Functions (continued)**

| SIGNAL                                      |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION  |
|---|-----|-----------------|---------------------------------|--|
| NAME  | NO. |                 |                                 |  |
| LCD_D[11]/<br>I2S2_DX/<br>GP[27]/<br>SPI_TX | K2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>For LCD bridge, it is LCD data pin 11.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[10]/<br>I2S2_RX/<br>GP[20]/<br>SPI_RX | F5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>For LCD bridge, it is LCD data pin 10.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[9]/<br>I2S2_FS/<br>GP[19]/<br>SPI_CS0 | K1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>For LCD bridge, it is LCD data pin 9.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[8]/<br>I2S2_CLK<br>GP[18]/<br>SPI_CLK | H1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>For LCD bridge, it is LCD data pin 8.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[7]/<br>GP[17]                         | J1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 7.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[6]/<br>GP[16]                         | E3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 6.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[5]/<br>GP[15]                         | G1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 5.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[4]/<br>GP[14]                         | F1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 4.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[3]/<br>GP[13]                         | E1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 3.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[2]/<br>GP[12]                         | E2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For LCD bridge, it is LCD data pin 2.<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.              |
| LCD_D[1]/<br>SPI_TX                         | C2  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, it is LCD data pin 1.<br>Mux control through the PPMODE bits in the EBSR.   |
| LCD_D[0]/<br>SPI_RX                         | A4  | I/O/Z           | DV <sub>DDIO</sub><br>BH        | This pin is multiplexed between LCD bridge and SPI.<br>For LCD bridge, it is LCD data pin 0.<br>Mux control through the PPMODE bits in the EBSR.   |

## 4.2.10 SD 1–0 Terminal Functions

### 4.2.10.1 SD1 Terminal Functions

Table 4-10 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-10. SD1 Terminal Functions**

| SIGNAL                         |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|--------------------------------|-----|-----------------|---------------------------------|--|
| NAME                           | NO. |                 |                                 |  |
| <b>SD</b>                      |     |                 |                                 |  |
| SD1_CLK/<br>I2S1_CLK/<br>GP[6] | H5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For SD, this is the SD1 data clock output SD1_CLK.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.  |
| SD1_CMD/<br>I2S1_FS/<br>GP[7]  | L4  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For SD, this is the SD1 command I/O output SD1_CMD.<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD1_D3/<br>GP[11]              | G5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | The SD1_D3 and SD1_D2 pins are multiplexed between SD1 and GPIO.<br>The SD1_D1 and SD1_D0 pins are multiplexed between SD1, I2S1, and GPIO.<br>In SD mode, all these pins are the SD1 nibble wide bidirectional data bus.                                |
| SD1_D2/<br>GP[10]              | M4  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH |  |
| SD1_D1/<br>I2S1_RX/<br>GP[9]   | H3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | Mux control through the SP1MODE bits in the EBSR.<br>The IPD resistor on these pins can be enabled or disabled through the PDINHIBR1 register.   |
| SD1_D0/<br>I2S1_DX/<br>GP[8]   | L3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH |  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder  
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.  
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.  
(4) Specifies the operating I/O supply voltage for each signal



#### 4.2.10.2 SD0 Terminal Functions

Table 4-11 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-11. SD0 Terminal Functions**

| SIGNAL                         |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|--------------------------------|-----|-----------------|---------------------------------|--|
| NAME                           | NO. |                 |                                 |  |
| <b>SD</b>                      |     |                 |                                 |  |
| SD0_CLK/<br>I2S0_CLK/<br>GP[0] | E5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For SD, this is the SD0 data clock output SD0_CLK.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.  |
| SD0_CMD/<br>I2S0_FS/<br>GP[1]  | J2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For SD, this is the SD0 command I/O output SD0_CMD.<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD0_D3/<br>GP[5]               | G3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | The SD0_D3 and SD0_D2 pins are multiplexed between SD0 and GPIO.<br>The SD0_D1 and SD0_D0 pins are multiplexed between SD0, I2S0, and GPIO.<br>In SD mode, these pins are the SD0 nibble wide bidirectional data bus.                                    |
| SD0_D2/<br>GP[4]               | M3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH |  |
| SD0_D1/<br>I2S0_RX/<br>GP[3]   | G2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | Mux control through the SP0MODE bits in the EBSR.<br>The IPD resistor on these pins can be enabled or disabled through the PDINHIBR1 register.   |
| SD0_D0/<br>I2S0_DX/<br>GP[2]   | D5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH |  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

#### 4.2.11 SAR ADC Terminal Functions

Table 4-12 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-12. 10-Bit SAR ADC Terminal Functions**

| SIGNAL         |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup> | DESCRIPTION  |
|----------------|-----|-----------------|--------------------------|--|
| NAME           | NO. |                 |                          |  |
| <b>SAR ADC</b> |     |                 |                          |  |
| GPAIN1         | F8  | I/O             | V <sub>DDA_ANA</sub>     | <p>GPAIN1: General-Purpose Output and Analog Input pin 1. This pin is connected to ADC Channel 3. GPAIN1 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN1 can accommodate input voltages from 0 V to V<sub>DDA_ANA</sub>.</p> <p><b>Note:</b> If the ANA_LDO is used to supply power to V<sub>DDA_ANA</sub>, this pin must <b>not</b> be used as a general-purpose output (driving high) because the maximum current capability (see the I<sub>SD</sub> parameter in Section 5.5, <i>Electrical Characteristics</i>) of the ANA_LDO can be exceeded. Doing so may result in the on-chip power-on reset (POR) resetting the chip.</p> |
| GPAIN2         | F10 | I/O             | V <sub>DDA_ANA</sub>     | <p>GPAIN2: General-Purpose Output and Analog Input pin 2. This pin is connected to ADC Channel 4. GPAIN2 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN2 can accommodate input voltages from 0 V to V<sub>DDA_ANA</sub>.</p> <p><b>Note:</b> If the ANA_LDO is used to supply power to V<sub>DDA_ANA</sub>, this pin must <b>not</b> be used as a general-purpose output (driving high) because the maximum current capability (see the I<sub>SD</sub> parameter in Section 5.5, <i>Electrical Characteristics</i>) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.</p>                  |
| GPAIN3         | J12 | I/O             | V <sub>DDA_ANA</sub>     | <p>GPAIN3: General-Purpose Output and Analog Input pin 3. This pin is connected to ADC Channel 5. GPAIN3 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN3 can accommodate input voltages from 0 V to V<sub>DDA_ANA</sub>.</p> <p><b>Note:</b> If the ANA_LDO is used to supply power to V<sub>DDA_ANA</sub>, this pin must <b>not</b> be used as a general-purpose output (driving high) because the maximum current capability (see the I<sub>SD</sub> parameter in Section 5.5, <i>Electrical Characteristics</i>) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.</p>                  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal



## 4.2.12 GPIO Terminal Functions

Table 4-13 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions**

| SIGNAL                              |     | TYPE<br>(1) (2) | OTHER <sup>(3) (4)</sup>        | DESCRIPTION  |
|-------------------------------------|-----|-----------------|---------------------------------|--|
| NAME                                | NO. |                 |                                 |  |
| <b>GENERAL-PURPOSE INPUT/OUTPUT</b> |     |                 |                                 |  |
| SD0_CLK/<br>I2S0_CLK/<br>GP[0]      | E5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For GPIO, it is general-purpose input/output pin 0 (GP[0]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD0_CMD/<br>I2S0_FS/<br>GP[1]       | J2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For GPIO, it is general-purpose input/output pin 1 (GP[1]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD0_D0/<br>I2S0_DX/<br>GP[2]        | D5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For GPIO, it is general-purpose input/output pin 2 (GP[2]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD0_D1/<br>I2S0_RX/<br>GP[3]        | G2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0, I2S0, and GPIO.<br>For GPIO, it is general-purpose input/output pin 3 (GP[3]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |
| SD0_D2/<br>GP[4]                    | M3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0 and GPIO.<br>For GPIO, it is general-purpose input/output pin 4 (GP[4]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.        |
| SD0_D3/<br>GP[5]                    | G3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD0 and GPIO.<br>For GPIO, it is general-purpose input/output pin 5 (GP[5]).<br>Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.        |
| SD1_CLK/<br>I2S1_CLK/<br>GP[6]      | H5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For GPIO, it is general-purpose input/output pin 6 (GP[6]).<br>Mux control through the SP1MODE bits in the EBSR.   |
| SD1_CMD/<br>I2S1_FS/<br>GP[7]       | L4  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For GPIO, it is general-purpose input/output pin 7 (GP[7]).<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions (continued)**

| SIGNAL                                       |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION   |
|--|-----|-----------------|---------------------------------|---|
| NAME   | NO. |                 |                                 |   |
| SD1_D0/<br>I2S1_DX/<br>GP[8]                 | L3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For GPIO, it is general-purpose input/output pin 8 (GP[8]).<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.  |
| SD1_D1/<br>I2S1_RX/<br>GP[9]                 | H3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1, I2S1, and GPIO.<br>For GPIO, it is general-purpose input/output pin 9 (GP[9]).<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.  |
| SD1_D2/<br>GP[10]                            | M4  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1 and GPIO.<br>For GPIO, it is general-purpose input/output pin 10 (GP[10]).<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.       |
| SD1_D3/<br>GP[11]                            | G5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between SD1 and GPIO.<br>For GPIO, it is general-purpose input/output pin 11 (GP[11]).<br>Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.       |
| LCD_D[2]/<br>GP[12]                          | E2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 12 (GP[12]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[3]/<br>GP[13]                          | E1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 13 (GP[13]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[4]/<br>GP[14]                          | F1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 14 (GP[14]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[5]/<br>GP[15]                          | G1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 15 (GP[15]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[6]/<br>GP[16]                          | E3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 16 (GP[16]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[7]/<br>GP[17]                          | J1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 17 (GP[17]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[8]/<br>I2S2_CLK/<br>GP[18]/<br>SPI_CLK | H1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge and GPIO.<br>For GPIO, it is general-purpose input/output pin 18 (GP[18]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |

**Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions (continued)**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)        | DESCRIPTION  |
|--|-----|-----------------|---------------------------------|--|
| NAME   | NO. |                 |                                 |  |
| LCD_D[9]/<br>I2S2_FS/<br>GP[19]/<br>SPI_CS0    | K1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, and GPIO.<br>For GPIO, it is general-purpose input/output pin 19 (GP[19]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.       |
| LCD_D[10]/<br>I2S2_RX/<br>GP[20]/<br>SPI_RX    | F5  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO and SPI.<br>For GPIO, it is general-purpose input/output pin 20 (GP[20]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.   |
| LCD_D[11]/<br>I2S2_DX/<br>GP[27]/<br>SPI_TX    | K2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI.<br>For GPIO, it is general-purpose input/output pin 27 (GP[27]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.  |
| LCD_D[12]/<br>UART_RTS/<br>GP[28]/<br>I2S3_CLK | J3  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For GPIO, it is general-purpose input/output pin 28 (GP[28]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[13]/<br>UART_CTS/<br>GP[29]/<br>I2S3_FS  | M1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For GPIO, it is general-purpose input/output pin 29 (GP[29]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[14]/<br>UART_RXD/<br>GP[30]/<br>I2S3_RX  | L1  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For GPIO, it is general-purpose input/output pin 30 (GP[30]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |
| LCD_D[15]/<br>UART_TXD/<br>GP[31]/<br>I2S3_DX  | L2  | I/O/Z           | IPD<br>DV <sub>DDIO</sub><br>BH | This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3.<br>For GPIO, it is general-purpose input/output pin 31 (GP[31]).<br>Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register. |

### 4.2.13 Regulators and Power Management Terminal Functions

Table 4-14 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-14. Regulators and Power Management Terminal Functions**

| SIGNAL                           |                     | TYPE<br>(1) (2) | OTHER<br>(3) (4) | DESCRIPTION  |
|----------------------------------|---------------------|-----------------|------------------|--|
| NAME                             | NO.                 |                 |                  |  |
| <b>REGULATORS</b>                |                     |                 |                  |  |
| DSP_LDOO                         | M11                 | S               |                  | <p>DSP_LDO output. When enabled, this output provides a regulated 1.3- or 1.05-V output and up to 250 mA of current (see the <math>I_{SD}</math> parameter in Section 5.5, <i>Electrical Characteristics</i>). The DSP_LDO is intended to supply current to the digital core circuits only (<math>CV_{DD}</math>) and not external devices. For proper device operation, the external decoupling capacitor of this pin must be <math>5\mu\text{F} \sim 10\mu\text{F}</math>. For more detailed information, see Section 5.6.5.4, <i>Power-Supply Decoupling</i>.</p> <p>When disabled, this pin is in the high-impedance (Hi-Z) state.</p> <p>When DSP_LDO comes out of reset, it is enabled to 1.3 V for the bootloader to operate.</p>   |
| LDOI                             | L10,<br>L11,<br>G10 | S               |                  | <p>LDO inputs. For proper device operation, LDOI must always be powered. The LDOI pins must be connected to the same power supply source with a voltage range as specified for LDOI in Section 5.3, <i>Recommended Operating Conditions</i>. These pins supply power to the internal LDOs, the bandgap reference generator circuits, and serve as the I/O supply for some input pins.</p>  |
| $\overline{\text{DSP\_LDO\_EN}}$ | M12                 | I               |                  | <p>DSP_LDO enable input. This signal is not intended to be dynamically switched.</p> <p>0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V, according to the DSP_LDO_V bit in the LDOCNTL register (see Figure 5-2). At power-on-reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the RESET pin.</p> <p>1 = DSP_LDO is disabled and the DSP_LDOO pin is in a high-impedance (Hi-Z) state. The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The RESET pin (A11) will act as the sole reset source for the device. If an external power supply is used to provide power to <math>CV_{DD}</math>, then DSP_LDO_EN must be tied to LDOI, DSP_LDOO must be left unconnected, and the <math>\overline{\text{RESET}}</math> pin must be asserted appropriately for device initialization after power up.</p> <p><b>Note:</b> To pull up this pin, connect it to the same supply as the LDOI pins.</p> |
| USB_LDOO                         | M10                 | S               |                  | <p>USB_LDO output. This output provides a regulated 1.3 V output and up to 25 mA of current (see the <math>I_{SD}</math> parameter in Section 5.5, <i>Electrical Characteristics</i>). For proper device operation, this pin must be connected to a <math>1\mu\text{F} \sim 2\mu\text{F}</math> decoupling capacitor to <math>V_{SS}</math>. For more detailed information, see Section 5.6.5.4, <i>Power-Supply Decoupling</i>. This LDO is intended to supply power to the USB_ <math>V_{DD1P3}</math>, USB_ <math>V_{DDA1P3}</math> pins and not external devices.</p>  |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

**Table 4-14. Regulators and Power Management Terminal Functions (continued)**

| SIGNAL   |     | TYPE<br>(1) (2) | OTHER<br>(3) (4) | DESCRIPTION  |
|----------|-----|-----------------|------------------|--|
| NAME     | NO. |                 |                  |  |
| ANA_LDOO | H11 | S               |                  | ANA_LDO output. This output provides a regulated 1.3 V output and up to 4 mA of current (see the I <sub>SD</sub> parameter in <a href="#">Section 5.5, Electrical Characteristics</a> ).<br><br>For proper device operation, this pin must be connected to an ~ 1.0 μF decoupling capacitor to V <sub>SS</sub> . For more detailed information, see <a href="#">Section 5.6.5.4, Power-Supply Decoupling</a> . This LDO is intended to supply power to the V <sub>DDA_ANA</sub> and V <sub>DDA_PLL</sub> pins and <b>not</b> external devices. |
| BG_CAP   | J11 | A I/O           |                  | Bandgap reference filter signal.<br><br>For proper device operation, this pin should be bypassed with a 0.1-μF capacitor to analog ground (V <sub>SSA_ANA</sub> ).<br><br>BG_CAP provides a settling time of 200 ms that must elapse before executing bootloader code. The settling time is used by Timer0. The BG_CAP external capacitor provides filtering for stable reference voltages and currents generated by the bandgap circuit. The bandgap produces the references for use by the System PLL, SAR, and POR circuits.                |

#### 4.2.14 Reserved and No Connects Terminal Functions

[Table 4-15](#) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see [Section 6, Device Configuration](#).

**Table 4-15. Reserved and No Connects Terminal Functions**

| SIGNAL          |     | TYPE<br>(1) (2) | OTHER<br>(3) (4) | DESCRIPTION  |
|-----------------|-----|-----------------|------------------|--|
| NAME            | NO. |                 |                  |  |
| <b>RESERVED</b> |     |                 |                  |  |
| RSV0            | L12 | I               | –                | Reserved. For proper device operation, this pin must be tied directly to V <sub>SS</sub> . |
| RSV3            | K11 | I               | –                | Reserved. For proper device operation, this pin must be tied directly to V <sub>SS</sub> . |
| RSV4            | H10 | I               | –                | Reserved. For proper device operation, this pin must be tied directly to V <sub>SS</sub> . |
| RSV5            | J10 | I               | –                | Reserved. For proper device operation, this pin must be tied directly to V <sub>SS</sub> . |
| RSV17           | M5  | I               | –                | Reserved. For proper device operation, this pin must be unconnected.                       |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see [Section 6.8.1, Pullup and Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

### 4.2.15 Supply Voltage Terminal Functions

Table 4-16 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-16. Supply Voltage Terminal Functions**

| SIGNAL                   |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)                                 | DESCRIPTION   |
|--------------------------|-----|-----------------|--|---|
| NAME                     | NO. |                 |  |   |
| <b>SUPPLY VOLTAGES</b>   |     |                 |  |   |
| CV <sub>DD</sub>         | A9  | PWR             |  | 1.05-V Digital Core supply voltage (60 MHz)<br>1.3-V Digital Core supply voltage (100 MHz)  |
|                          | B5  |                 |  |   |
|                          | B8  |                 |  |   |
|                          | C6  |                 |  |   |
|                          | E6  |                 |  |   |
|                          | G7  |                 |  |   |
| DV <sub>DDIO</sub>       | B10 | PWR             |  | 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for non-RTC I/Os<br>The DV <sub>DDIO</sub> signal must always be powered for proper operation.  |
|                          | D2  |                 |  |   |
|                          | H2  |                 |  |   |
|                          | M2  |                 |  |   |
| CV <sub>DDRTC</sub>      | D10 | PWR             |  | 1.05-V through 1.3-V RTC digital core and RTC oscillator power supply<br><b>Note:</b> The CV <sub>DDRTC</sub> must be powered though RTC is not used.<br><b>Note:</b> The CV <sub>DDRTC</sub> cannot be powered by any of the on-chip LDOs and must be externally powered.  |
| DV <sub>DDRTC</sub>      | F12 | PWR             |  | 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for RTC_XO and RTC_XI pins  |
| V <sub>D</sub> DA_PLL    | E10 | PWR             | See Section 5.3, <i>Recommended Operating Conditions</i> | 1.3-V Analog PLL power supply for the system clock generator (PLLOUT ≤ 100 MHz)<br>This signal can be powered from the ANA_LDOO pin.  |
| USB_V <sub>DD</sub> PLL  | M7  | S               | See Section 5.3, <i>Recommended Operating Conditions</i> | 3.3-V USB Analog PLL power supply<br>When the USB peripheral is not used, the USB_V <sub>DD</sub> PLL signal must be connected to ground (V <sub>SS</sub> ).  |
| USB_V <sub>DD</sub> 1P3  | L5  | S               | See Section 5.3, <i>Recommended Operating Conditions</i> | 1.3-V digital core power supply for USB PHY.<br>This signal must be powered on in the order listed in Section 5.6.5.1, <i>Power-Supply Sequencing</i> .<br>When the USB peripheral is not used, the USB_V <sub>DD</sub> 1P3 signal must be connected to ground (V <sub>SS</sub> ).                                      |
| USB_V <sub>D</sub> DA1P3 | K6  | S               | See Section 5.3, <i>Recommended Operating Conditions</i> | Analog 1.3-V power supply for USB PHY (For high-speed sensitive analog circuits)<br>This signal must be powered on in the order listed in Section 5.6.5.1, <i>Power-Supply Sequencing</i> .<br>When the USB peripheral is not used, the USB_V <sub>D</sub> DA1P3 signal must be connected to ground (V <sub>SS</sub> ). |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder  
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.  
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.  
(4) Specifies the operating I/O supply voltage for each signal

**Table 4-16. Supply Voltage Terminal Functions (continued)**

| SIGNAL               |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)  | DESCRIPTION  |
|----------------------|-----|-----------------|---|--|
| NAME                 | NO. |                 |   |  |
| USB_VDDA3P3          | L7  | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | Analog 3.3 V power supply for USB PHY<br>This signal must be powered on in the order listed in <a href="#">Section 5.6.5.1, Power-Supply Sequencing</a> .<br>When the USB peripheral is not used, the USB_VDDA3P3 signal must be connected to ground (V <sub>SS</sub> ). |
| USB_VDDOSC           | K8  | S               | See <a href="#">Section 5.3, Recommended Operating Conditions</a> | 3.3-V power supply for USB oscillator<br>When the USB peripheral is not used, the USB_VDDOSC signal must be connected to ground (V <sub>SS</sub> ).  |
| V <sub>DDA_ANA</sub> | G11 | PWR             |   | 1.3-V supply for power management and 10-bit SAR ADC<br>This signal can be powered from the ANA_LDOO pin.  |



#### 4.2.16 Ground Terminal Functions

Table 4-17 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

**Table 4-17. Ground Terminal Functions**

| SIGNAL                 |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)                                 | DESCRIPTION  |
|------------------------|-----|-----------------|--|--|
| NAME                   | NO. |                 |  |  |
| V <sub>SS</sub>        | A5  | GND             |  | Ground pins  |
|                        | A6  |                 |  |  |
|                        | A7  |                 |  |  |
|                        | A8  |                 |  |  |
|                        | A10 |                 |  |  |
|                        | A12 |                 |  |  |
|                        | B6  |                 |  |  |
|                        | B7  |                 |  |  |
|                        | B9  |                 |  |  |
|                        | C4  |                 |  |  |
|                        | C7  |                 |  |  |
|                        | C9  |                 |  |  |
|                        | F3  |                 |  |  |
|                        | F7  |                 |  |  |
| G6                     |     |                 |  |  |
| G8                     |     |                 |  |  |
| K4                     |     |                 |  |  |
| V <sub>SSRTC</sub>     | G12 | GND             | See Section 5.3, <i>Recommended Operating Conditions</i> | Ground for RTC oscillator. When using a 32.768-kHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-6 and Figure 5-7). When not using RTC and the crystal is not populated on the board, this pin is connected to the board ground. |
| V <sub>SSA_PLL</sub>   | E8  | GND             | See Section 5.3, <i>Recommended Operating Conditions</i> | Analog PLL ground for the system clock generator   |
| USB_V <sub>SSPLL</sub> | L8  | GND             | See Section 5.3, <i>Recommended Operating Conditions</i> | USB analog PLL ground  |
| USB_V <sub>SS1P3</sub> | H6  | GND             | See Section 5.3, <i>Recommended Operating Conditions</i> | Digital core ground for USB PHY. Analog ground for USB PHY (for high speed sensitive analog circuits).   |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal



**Table 4-17. Ground Terminal Functions (continued)**

| SIGNAL      |     | TYPE<br>(1) (2) | OTHER <sup>(3)</sup> (4)  | DESCRIPTION  |
|-------------|-----|-----------------|---|--|
| NAME        | NO. |                 |   |  |
| USB_VSSA3P3 | H7  | GND             | See<br><a href="#">Section 5.3</a> ,<br><i>Recommended<br/>Operating<br/>Conditions</i> | Analog ground for USB PHY  |
| USB_VSSOSC  | M9  | S               | See<br><a href="#">Section 5.3</a> ,<br><i>Recommended<br/>Operating<br/>Conditions</i> | Ground for USB oscillator  |
| USB_VSSREF  | H8  | GND             | See<br><a href="#">Section 5.3</a> ,<br><i>Recommended<br/>Operating<br/>Conditions</i> | Ground for reference current. This signal must be connected through a 10-kΩ ±1% resistor to USB_R1.<br>When the USB peripheral is not used, the USB_VSSREF signal must be connected directly to ground (V <sub>SS</sub> ). |
| VSSA_ANA    | H12 | 0               |   | Ground pins for power management (POR and Bandgap circuits) and 10-bit SAR ADC   |
|             | K12 |                 |   |  |

## 5 Specifications

For the device maximum operating frequency, see [Section 7.1, Device and Development-Support Tool Nomenclature](#).

### 5.1 Absolute Maximum Ratings <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|  |   | VALUE       | UNIT |
|--|---|-------------|------|
| Supply voltage                             | Digital Core (CV <sub>DD</sub> , CV <sub>DDRTC</sub> , USB_V <sub>DD1P3</sub> ) <sup>(2)</sup>  | –0.5 to 1.7 | V    |
|  | I/O, 1.8 V, 2.5 V, 2.75 V, 3.3 V (DV <sub>DDIO</sub> , DV <sub>DDRTC</sub> ) 3.3 V USB supplies USB PHY (USB_V <sub>DDOSC</sub> , USB_V <sub>DDPLL</sub> , USB_V <sub>DDA3P3</sub> ) <sup>(2)</sup> | –0.5 to 4.2 |      |
|  | LDO1  | –0.5 to 4.2 |      |
|  | Analog, 1.3 V (V <sub>DDA_PLL</sub> , USB_V <sub>DDA1P3</sub> , V <sub>DDA_ANA</sub> ) <sup>(2)</sup>   | –0.5 to 1.7 |      |
| Input and Output voltage ranges:           | V <sub>I</sub> I/O, all pins with DV <sub>DDIO</sub> or USB_V <sub>DDOSC</sub> or USB_V <sub>DDPLL</sub> or USB_V <sub>DDA3P3</sub> as supply source  | –0.5 to 4.2 | V    |
|  | V <sub>O</sub> I/O, all pins with DV <sub>DDIO</sub> or USB_V <sub>DDOSC</sub> or USB_V <sub>DDPLL</sub> or USB_V <sub>DDA3P3</sub> as supply source  | –0.5 to 4.2 |      |
|  | RTC_XI and RTC_XO   | –0.5 to 1.7 |      |
|  | V <sub>I</sub> and V <sub>O</sub> , GPAIN[3:1]  | –0.5 to 1.7 |      |
|  | V <sub>O</sub> , BG_CAP   | –0.5 to 1.7 |      |
|  | USB_V <sub>BUS</sub> Input  | –0.5 to 5.5 |      |
|  | ANA_LDO0, DSP_LDO0, and USB_LDO0  | –0.5 to 1.7 |      |
| Operating case temperature, T <sub>c</sub> | Commercial temperature (default)  | –10 to 70   | °C   |
| Storage temperature, T <sub>stg</sub>      |   | –65 to 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V<sub>SS</sub>.

### 5.2 ESD Ratings

|                    |                         | VALUE  | UNIT |
|--------------------|-------------------------|--|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000-V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250-V may actually have higher performance.

### 5.3 Recommended Operating Conditions

|                                |   |  |                        | MIN                         | NOM                        | MAX  | UNIT |      |      |
|--------------------------------|---|--|------------------------|-----------------------------|----------------------------|------|------|------|------|
| Core Supplies                  | CV <sub>DD</sub>                        | Supply voltage, Digital Core   | 60 MHz                 | 0.998                       | 1.05                       | 1.15 | V    |      |      |
|                                |   |  | 100 MHz                | 1.24                        | 1.3                        | 1.43 |      |      |      |
|                                | CV <sub>DDRTC</sub>                     | Supply voltage, RTC and RTC OSC  | 32.768 kHz             | 0.998                       |                            | 1.43 |      |      |      |
|                                | USB_V <sub>DD1P3</sub>                  | Supply voltage, Digital USB  |                        | 1.24                        | 1.3                        | 1.43 |      |      |      |
|                                | USB_V <sub>DDA1P3</sub>                 | Supply voltage, 1.3-V Analog USB   |                        | 1.24                        | 1.3                        | 1.43 |      |      |      |
|                                | V <sub>DDA_ANA</sub>                    | Supply voltage, 1.3-V SAR and Power Management   |                        | 1.24                        | 1.3                        | 1.43 |      |      |      |
|                                | V <sub>DDA_PLL</sub>                    | Supply voltage, System PLL   |                        | 1.24                        | 1.3                        | 1.43 |      |      |      |
| I/O Supplies                   | USB_V <sub>DDPLL</sub>                  | Supply voltage, 3.3-V USB PLL  |                        | 2.97                        | 3.3                        | 3.63 | V    |      |      |
|                                |   |  | DV <sub>DDIO</sub>     | Supply voltage, I/O, 3.3-V  |                            | 2.97 |      | 3.3  | 3.63 |
|                                |   |  | DV <sub>DDRTC</sub>    | Supply voltage, I/O, 2.75-V |                            | 2.48 |      | 2.75 | 3.02 |
|                                |   |  |                        | Supply voltage, I/O, 2.5-V  |                            | 2.25 |      | 2.5  | 2.75 |
|                                |   | Supply voltage, I/O, 1.8-V   |                        | 1.65                        | 1.8                        | 1.98 |      |      |      |
|                                | USB_V <sub>DDOSC</sub>                  | Supply voltage, I/O, 3.3-V USB OSC   |                        | 2.97                        | 3.3                        | 3.63 |      |      |      |
|                                | USB_V <sub>DDA3P3</sub>                 | Supply voltage, I/O, 3.3-V Analog USB PHY  |                        | 2.97                        | 3.3                        | 3.63 |      |      |      |
| GND                            | LDO1                                    | Supply voltage, Analog Power Management and LDO Inputs   |                        | 1.75                        | 1.8                        | 1.85 | V    |      |      |
|                                | V <sub>SS</sub>                         | Supply ground, Digital I/O   |                        |                             |                            |      |      |      |      |
|                                | V <sub>SSRTC</sub>                      | Supply ground, RTC   |                        |                             |                            |      |      |      |      |
|                                | USB_V <sub>SSOSC</sub>                  | Supply ground, USB OSC   |                        |                             |                            |      |      |      |      |
|                                | USB_V <sub>SSPLL</sub>                  | Supply ground, USB PLL   |                        |                             |                            |      |      |      |      |
|                                | USB_V <sub>SSA3P3</sub>                 | Supply ground, 3.3-V Analog USB PHY  |                        | 0                           | 0                          | 0    |      |      |      |
|                                | USB_V <sub>SSREF</sub>                  | Supply ground, USB Reference Current   |                        |                             |                            |      |      |      |      |
|                                | V <sub>SSA_PLL</sub>                    | Supply ground, System PLL  |                        |                             |                            |      |      |      |      |
|                                | USB_V <sub>SS1P3</sub>                  | Supply ground, 1.3-V Digital USB PHY   |                        |                             |                            |      |      |      |      |
| V <sub>SSA_ANA</sub>           | Supply ground, SAR and Power Management |  |                        |                             |                            |      |      |      |      |
| V <sub>IH</sub> <sup>(1)</sup> |   | High-level input voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3:1] pins) <sup>(2)</sup> | 0.7 × DV <sub>DD</sub> |                             | DV <sub>DD</sub> + 0.3     | V    |      |      |      |
| V <sub>IL</sub> <sup>(1)</sup> |   | Low-level input voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3:1] pins) <sup>(2)</sup>  | −0.3                   |                             | 0.3 × DV <sub>DD</sub>     | V    |      |      |      |
| V <sub>IN</sub>                |   | Input voltage, GPAIN[3:1] pins   | −0.3                   |                             | V <sub>DDA_ANA</sub> + 0.3 | V    |      |      |      |
| T <sub>c</sub>                 |   | Operating case temperature   | Default (Commercial)   | −10                         |                            | 70   | °C   |      |      |
| F <sub>SYSCLK</sub>            |   | DSP Operating Frequency (SYSCLK)   | 1.05-V                 | 0                           |                            | 60   | MHz  |      |      |
|                                |   |  | 1.3-V                  | 0                           |                            | 100  |      |      |      |

(1) DV<sub>DD</sub> refers to the pin I/O supply voltage. To determine the I/O supply voltage for each pin, see [Section 4.2, Terminal Functions](#).

(2) The I<sup>2</sup>C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the DV<sub>DDIO</sub> is powered down. Due to the fact that different voltage devices can be connected to I<sup>2</sup>C bus and that the I<sup>2</sup>C inputs are LVCMOS, the level of logic 0 (low) and logic 1 (high) are not fixed and depend on DV<sub>DDIO</sub>.

### 5.4 Power Consumption Summary

#### NOTE

Power consumption on this device depends on several operating parameters such as operating voltage, operating frequency, and temperature. Power consumption also varies by end applications that determine the overall processor, CPU, and peripheral activity. For more specific power consumption details, see *Power Estimation and Power Consumption Summary for TMS320C5504/05/14/15/32/33/34/35/45 (SPRABN0)*. This document includes a spreadsheet for estimating power based on parameters that closely resemble the end application to generate a realistic estimate of power consumption on this device based on use-case and operating conditions.

## 5.5 Electrical Characteristics

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER   |   | TEST CONDITIONS <sup>(1)</sup>   | MIN                        | TYP                     | MAX                        | UNIT |
|---|---|--|----------------------------|-------------------------|----------------------------|------|
| V <sub>OH</sub>                                     | Full speed: USB_DN and USB_DP <sup>(2)</sup>  |  | 2.8                        | USB_V <sub>DDA3P3</sub> |                            | V    |
|   | High speed: USB_DN and USB_DP <sup>(2)</sup>  |  | 360                        |                         | 440                        | mV   |
|   | High-level output voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3:1] pins)        | IO = I <sub>OH</sub>   | 0.8 × DV <sub>DD</sub>     |                         |                            | V    |
|   | High-level output voltage, GPAIN[3:1] pins  | IO = I <sub>OH</sub>   | 0.8 × V <sub>DDA_ANA</sub> |                         |                            |      |
| V <sub>OL</sub>                                     | Full speed: USB_DN and USB_DP <sup>(2)</sup>  |  | 0.0                        |                         | 0.3                        | V    |
|   | High speed: USB_DN and USB_DP <sup>(2)</sup>  |  | -10                        |                         | 10                         | mV   |
|   | Low-level output voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except I2C and GPAIN[3:1] pins) | IO = I <sub>OL</sub>   |                            |                         | 0.2 × DV <sub>DD</sub>     | V    |
|   | Low-level output voltage, I2C pins <sup>(3)</sup>                                       | V <sub>DD</sub> > 2 V, I <sub>OL</sub> = 3 mA  | 0                          |                         | 0.4                        | V    |
|   | Low-level output voltage, GPAIN[3:1] pins   | IO = I <sub>OL</sub>   |                            |                         | 0.2 × V <sub>DDA_ANA</sub> |      |
| V <sub>HYS</sub>                                    | Input hysteresis <sup>(4)</sup>   | DV <sub>DD</sub> = 3.3-V   |                            | 162                     |                            | mV   |
|   |   | DV <sub>DD</sub> = 2.5-V   |                            | 141                     |                            |      |
|   |   | DV <sub>DD</sub> = 1.8-V   |                            | 122                     |                            |      |
| V <sub>LDO</sub>                                    | USB_LDOO voltage  |  | 1.24                       | 1.3                     | 1.43                       | V    |
|   | ANA_LDOO voltage  |  | 1.24                       | 1.3                     | 1.43                       |      |
|   | DSP_LDOO voltage  | DSP_LDO_V bit in the LDOCNTL register = 1  | 1.24                       | 1.3                     | 1.43                       |      |
|   |   | DSP_LDO_V bit in the LDOCNTL register = 0  | 0.998                      | 1.05                    | 1.15                       |      |
| I <sub>SD</sub>                                     | DSP_LDO shutdown current <sup>(5)</sup>   | LDOI = V <sub>MIN</sub>  | 250                        |                         |                            | mA   |
|   | ANA_LDO shutdown current <sup>(5)</sup>   | LDOI = V <sub>MIN</sub>  | 4                          |                         |                            |      |
|   | USB_LDO shutdown current <sup>(5)</sup>   | LDOI = V <sub>MIN</sub>  | 25                         |                         |                            |      |
| I <sub>ILPU</sub> <sup>(6)(7)</sup>                 | Input current [DC] (except I2C and GPAIN[3:1] pins)                                     | Input only pin, internal pulldown or pullup disabled   | -5                         |                         | 5                          | μA   |
|   |   | DV <sub>DD</sub> = 3.3 V with internal pullup enabled <sup>(8)</sup>                               |                            | -59 to -161             |                            |      |
|   |   | DV <sub>DD</sub> = 2.5 V with internal pullup enabled <sup>(8)</sup>                               |                            | -31 to -93              |                            |      |
|   |   | DV <sub>DD</sub> = 1.8 V with internal pullup enabled <sup>(8)</sup>                               |                            | -14 to -44              |                            |      |
| I <sub>IHPD</sub> <sup>(6)(7)</sup>                 | Input current [DC] (except I2C and GPAIN[3:1] pins)                                     | Input only pin, internal pulldown or pullup disabled   | -5                         |                         | 5                          | μA   |
|   |   | DV <sub>DD</sub> = 3.3 V with internal pulldown enabled <sup>(8)</sup>                             |                            | 52 to 158               |                            |      |
|   |   | DV <sub>DD</sub> = 2.5 V with internal pulldown enabled <sup>(8)</sup>                             |                            | 27 to 83                |                            |      |
|   |   | DV <sub>DD</sub> = 1.8 V with internal pulldown enabled <sup>(8)</sup>                             |                            | 11 to 35                |                            |      |
| I <sub>IH</sub> /<br>I <sub>IL</sub> <sup>(7)</sup> | Input current [DC], ALL pins  | V <sub>I</sub> = V <sub>SS</sub> to DV <sub>DD</sub> with internal pullups and pulldowns disabled. | -5                         |                         | 5                          |      |

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.

(2) The USB I/Os adhere to the universal bus specification revision 2.0 (USB 2.0 specifications).

(3) V<sub>DD</sub> is the voltage to which the I2C bus pullup resistors are connected.

(4) Applies to all input pins except I2C pins, GPAIN[3:1], RTC\_XI, and USB\_MX1.

(5) I<sub>SD</sub> is the amount of current the LDO is ensured to deliver before shutting down to protect itself.

(6) I<sub>I</sub> applies to input-only pins and bidirectional pins. For input-only pins, I<sub>I</sub> indicates the input leakage current. For bidirectional pins, I<sub>I</sub> indicates the input leakage current and off-state (Hi-Z) output leakage current.

(7) When CV<sub>DD</sub> power is ON, the pin bus-holders are disabled. For more detailed information, see [Section 5.6.5.2, Digital I/O Behavior When Core Power \(CV<sub>DD</sub>\) is Down](#).

(8) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

## Electrical Characteristics (continued)

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER   |  | TEST CONDITIONS <sup>(1)</sup>   |   | MIN   | TYP | MAX  | UNIT          |
|---|--|--|---|-------|-----|------|---------------|
| $I_{OH}^{(7)}$  | High-level output current [DC]                             | All Pins (except USB, CLKOUT, and GPAIN[3:1] pins)   |   | -4    |     |      | mA            |
|   |  | CLKOUT pin   | $DV_{DD} = 3.3\text{ V}$  | -6    |     |      |               |
|   |  |  | $DV_{DD} = 1.8\text{ V}$  | -4    |     |      |               |
|   |  | GPAIN[3:1] pins  | $DV_{DD} = V_{DDA\_ANA} = 1.3\text{ V}$ , external regulator <sup>(9)</sup> | -4    |     |      | $\mu\text{A}$ |
| $DV_{DD} = V_{DDA\_ANA} = 1.3\text{ V}$ , internal regulator <sup>(9)</sup> | -100   |  |   |       |     |      |               |
| $I_{OL}^{(7)}$  | Low-level output current [DC]                              | All pins (except USB, CLKOUT, and GPAIN[3:1])  |   |       |     | 4    | mA            |
|   |  | CLKOUT pin   | $DV_{DD} = 3.3\text{ V}$  |       |     | 6    |               |
|   |  |  | $DV_{DD} = 1.8\text{ V}$  |       |     | 4    |               |
| $I_{OZ}^{(10)}$   | I/O off-state output current                               | All pins (except USB and GPAIN[3:1])   |   | -10   |     | 10   | $\mu\text{A}$ |
|   |  | GPAIN [3:1] pins   |   | -10   |     | 10   |               |
| $I_{OLBH}^{(11)}$   | Bus-holder pull low current when $CV_{DD}$ is powered off  | Supply voltage, I/O, 3.3-V   |   |       |     | 2.2  | mA            |
|   |  | Supply voltage, I/O, 2.75-V  |   |       |     | 1.6  |               |
|   |  | Supply voltage, I/O, 2.5-V   |   |       |     | 1.4  |               |
|   |  | Supply voltage, I/O, 1.8-V   |   |       |     | 0.72 |               |
| $I_{OHBH}^{(11)}$   | Bus-holder pull high current when $CV_{DD}$ is powered off | Supply voltage, I/O, 3.3-V   |   | -1.3  |     |      | mA            |
|   |  | Supply voltage, I/O, 2.75-V  |   | -0.97 |     |      |               |
|   |  | Supply voltage, I/O, 2.5-V   |   | -0.83 |     |      |               |
|   |  | Supply voltage, I/O, 1.8-V   |   | -0.46 |     |      |               |
| $I$   | Analog PLL ( $V_{DDA\_PLL}$ ) supply current               | $V_{DDA\_PLL} = 1.3\text{ V}$<br>Room temp (25°C), Phase detector = 170 kHz, VCO = 100 MHz |   |       | 0.7 |      | $\text{mA}$   |
| $I$   | SAR Analog ( $V_{DDA\_ANA}$ ) supply current               | $V_{DDA\_ANA} = 1.3\text{ V}$ , SAR clock = 2 MHz, Temp (70 °C)                            |   |       |     | 1    | $\text{mA}$   |
| $C_I$   | Input capacitance  |  |   |       |     | 4    | $\text{pF}$   |
| $C_O$   | Output capacitance   |  |   |       |     | 4    | $\text{pF}$   |

(9) When the ANA\_LDO supplies  $V_{DDA\_ANA}$ , it is not recommended to use the GPAIN[3:1] signals for general-purpose outputs (driving high). The  $I_{SD}$  parameter of the ANA\_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through  $V_{DDA\_PLL}$  and the SAR through  $V_{DDA\_ANA}$ .

(10)  $I_{OZ}$  applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

(11) This parameter specifies the maximum strength of the bus-holder and is needed to calculate the minimum strength of external pullups and pulldowns.

**Table 5-1. Thermal Resistance Characteristics (PBGA Package) [ZQW]**

| NAME                                | DESCRIPTION             | VELOCITY (m/s) <sup>(1)</sup> | 1S0P  | 2S2P  |
|-------------------------------------|-------------------------|-------------------------------|-------|-------|
| $\Theta_{JA}$ (°C/W) <sup>(2)</sup> | Junction-to-free air    | 0                             | 74.21 | 39.53 |
|                                     |                         | 1                             | 58.98 | 34.82 |
|                                     |                         | 2                             | 51.54 | 32.75 |
|                                     |                         | 3                             | 45.27 | 30.66 |
| $\Psi_{JT}$ (°C/W)                  | Junction-to-package top | 0                             | 0.33  | 0.15  |
|                                     |                         | 1                             | 0.59  | 0.38  |
|                                     |                         | 2                             | 1.04  | 0.68  |
|                                     |                         | 3                             | 1.90  | 1.30  |

(1) m/s = meters per second

(2) These measurements were conducted in a JEDEC-defined 1S0P/2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages*.

**Table 5-1. Thermal Resistance Characteristics (PBGA Package) [ZQW] (continued)**

| NAME                 | DESCRIPTION       | VELOCITY<br>(m/s) <sup>(1)</sup> | 1S0P  | 2S2P  |
|----------------------|-------------------|----------------------------------|-------|-------|
| $\Psi_{JB}$ (°C/W)   | Junction-to-board | 0                                | 15.28 | 16.28 |
|                      |                   | 1                                | 14.99 | 16.01 |
|                      |                   | 2                                | 14.45 | 15.69 |
|                      |                   | 3                                | 13.72 | 15.08 |
| $\Theta_{JC}$ (°C/W) | Junction-to-case  |                                  | 11.12 | N/A   |
| $\Theta_{JB}$ (°C/W) | Junction-to-board |                                  | 14.99 | 16.21 |

## 5.6 Timing and Switching Characteristics

### 5.6.1 Power Considerations

The device provides several means of managing power consumption.

To minimize power consumption, the device divides its circuits into eight main isolated supply domains:

- LDO1 (LDOs and bandgap power supply)
- Analog POR, SAR, and PLL ( $V_{DDA\_ANA}$  and  $V_{DDA\_PLL}$ )
- RTC Core ( $CV_{DDRTC}$ )

#### NOTE

$CV_{DDRTC}$  must always be powered by an external power source and none of the on-chip LDOs can be used to power  $CV_{DDRTC}$ .

- Digital Core ( $CV_{DD}$ )
- USB Core ( $USB\_V_{DD1P3}$  and  $USB\_V_{DDA1P3}$ )
- USB PHY and USB PLL ( $USB\_V_{DDOSC}$ ,  $USB\_V_{DDA3P3}$ , and  $USB\_V_{DDPLL}$ )
- RTC I/O ( $DV_{DDRTC}$ )
- Rest of the I/O ( $DV_{DDIO}$ )

#### 5.6.1.1 LDO Configuration

The device includes low-dropout regulators (LDOs) that regulate the power supplies of the analog PLL and SAR ADC and power management (ANA\_LDO), digital core (DSP\_LDO), and USB core (USB\_LDO).

A combination of pin configuration and register settings control these LDOs. For more detailed information see the following sections.

##### 5.6.1.1.1 LDO Inputs

The LDOI pins (G10, L10, L11) provide power to the internal ANA\_LDO, DSP\_LDO, USB\_LDO, the bandgap reference generator, and some I/O input pins, and range as specified for LDOI in [Section 5.3, Recommended Operating Conditions](#). The bandgap provides accurate voltage and current references to the POR, LDOs, PLL, and SAR. Even if the LDO outputs are unused, power must always be applied to the LDOI pins .

##### 5.6.1.1.2 LDO Outputs

The ANA\_LDOO pin (H11) is the output of the internal ANA\_LDO and can provide regulated 1.3 V power of up to 4 mA. On the board, the ANA\_LDOO pin is intended to be connected to the  $V_{DDA\_ANA}$  and  $V_{DDA\_PLL}$  pins to provide a regulated 1.3 V to the 10-bit SAR ADC, Power Management Circuits, and System PLL. TI recommends powering  $V_{DDA\_ANA}$  and  $V_{DDA\_PLL}$  by this LDO output to take advantage of the device's power management techniques or by an external power supply. The ANA\_LDO cannot be disabled individually (see [Section 5.6.1.1.3, LDO Control](#)).

The DSP\_LDOO pin (M11) is the output of the internal DSP\_LDO and provides software-selectable regulated 1.3 V or regulated 1.05 V power of up to 250 mA. On the board, TI intends the DSP\_LDOO pin to connect to the CV<sub>DD</sub> pins. In this configuration, the  $\overline{\text{DSP\_LDO\_EN}}$  pin must be tied to the board V<sub>SS</sub>, enabling the DSP\_LDO. Optionally, the CV<sub>DD</sub> pins may be powered by an external power supply; the  $\overline{\text{DSP\_LDO\_EN}}$  pin must be tied (high) to LDO1, disabling DSP\_LDO. The  $\overline{\text{DSP\_LDO\_EN}}$  also affects how reset is generated to the chip (for more details, see the  $\overline{\text{DSP\_LDO\_EN}}$  pin description in [Table 4-14](#)). When the DSP\_LDO is disabled, its output pin is in a high-impedance state.

---

**NOTE**

$\overline{\text{DSP\_LDO\_EN}}$  is not intended to be changed dynamically.

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When DSP\_LDO comes out of reset, it is enabled to 1.3 V for the bootloader to operate.

The USB\_LDOO pin (M10) is the output of the internal USB\_LDO and provides regulated 1.3 V, software-switchable (on and off) power of up to 25 mA. On the board, TI intends the USB\_LDOO pin to connect to the USB\_V<sub>DD1P3</sub> and USB\_V<sub>DDA1P3</sub> pins to provide power to portions of the USB. Optionally, the USB\_V<sub>DD1P3</sub> and USB\_V<sub>DDA1P3</sub> may be powered by an external power supply and the USB\_LDO can be left disabled. When the USB\_LDO is disabled, its output pin is in a high-impedance state.

### 5.6.1.1.3 LDO Control

All LDOs can be simultaneously disabled through software by writing to either the BG\_PD bit or the LDO\_PD bit in the RTCPMGT register (see [Figure 5-1](#)). When the LDOs are disabled through this mechanism, the only way to re-enable them is by an RTC alarm interrupt or by cycling power to the CV<sub>DDRTC</sub> pin.

**ANA\_LDO:** The ANA\_LDO is only disabled by the BG\_PD and the LDO\_PD mechanism described above. If not, ANA\_LDO is always enabled.

**DSP\_LDO:** The DSP\_LDO can be statically disabled by the  $\overline{\text{DSP\_LDO\_EN}}$  pin as described in [Section 5.6.1.1.2, LDO Outputs](#). The DSP\_LDO can be also dynamically disabled through the BG\_PD and the LDO\_PD mechanism described above. The DSP\_LDO can change its output voltage dynamically by software through the DSP\_LDO\_V bit in the LDOCNTL register (see [Figure 5-2](#)). The DSP\_LDO output voltage is set to 1.3 V at reset.

**USB\_LDO:** The USB\_LDO can be independently and dynamically enabled or disabled by software through the USB\_LDO\_EN bit in the LDOCNTL register (see [Figure 5-2](#)). The USB\_LDO is disabled at reset.

The RTCPMGT register is shown in [Figure 5-1](#) and described in [Table 5-2](#). The LDOCNTL register is shown in [Figure 5-2](#) and described in [Table 5-3](#).

[Table 5-4](#) shows the ON and OFF control of each LDO and its register control bit configurations.

**Figure 5-1. RTC Power Management Register (RTCPMGT) [1930h]**

|          |          |          |          |       |        |          |   |
|----------|----------|----------|----------|-------|--------|----------|---|
| 15       | Reserved |          |          |       |        |          | 8 |
| R-0      |          |          |          |       |        |          |   |
| 7        | 5        | 4        | 3        | 2     | 1      | 0        |   |
| Reserved |          | Reserved | Reserved | BG_PD | LDO_PD | Reserved |   |
|          |          | R-0      | R-0      | R/W-0 | R/W-0  | R-0      |   |

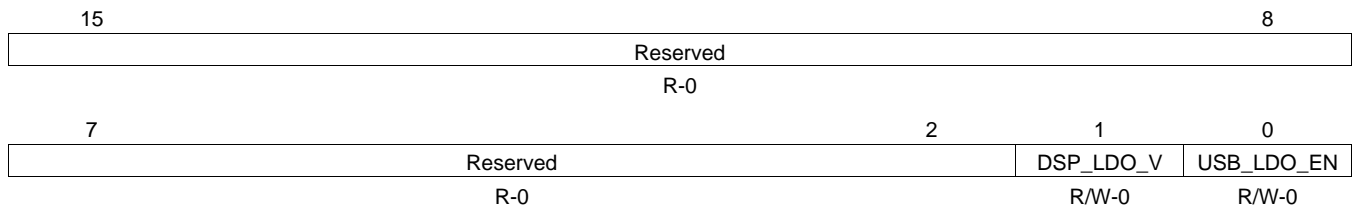
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 5-2. RTCPMGT Register Bit Descriptions**

| BIT  | NAME     | DESCRIPTION  |
|------|----------|--|
| 15:5 | RESERVED | Reserved. Read-only, writes have no effect.  |
| 4    | RESERVED | Reserved. For proper operation, default value cannot be changed.   |
| 3    | RESERVED | Reserved. For proper operation, default value cannot be changed.   |
| 2    | BG_PD    | <p>Bandgap, on-chip LDOs, and the analog POR power down bit</p> <p>This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO), the analog POR, and bandgap reference. TI intends using BG_PD and LDO_PD only when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and unused then the BG_PD and LDO_PD power down mechanisms should not be used because POR gets powered down and the POWERGOOD signal is not generated properly.</p> <p>After this bit is asserted, the on-chip LDOs, analog POR, and the Bandgap reference can be reenabled by the RTC alarm interrupt. The bandgap circuit will take about 100 msec to charge the external 0.1-<math>\mu</math>F capacitor through the internal 326-k<math>\Omega</math> resistor.</p> <p>0 = On-chip LDOs, analog POR, and bandgap reference are enabled.<br/>1 = On-chip LDOs, analog POR, and bandgap reference are disabled (shutdown).</p> |
| 1    | LDO_PD   | <p>On-chip LDOs and analog POR power down bit</p> <p>This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO). TI intends using the analog POR. BG_PD and LDO_PD only when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power down mechanisms should not be used because POR gets powered down and the POWERGOOD signal is not generated properly.</p> <p>After this bit is asserted, the on-chip LDOs and analog POR can be re-enabled by the RTC alarm interrupt. This bit keeps the bandgap reference turned on to allow a faster wake-up time with the expense power consumption of the bandgap reference.</p> <p>0 = On-chip LDOs and analog POR are enabled.<br/>1 = On-chip LDOs and analog POR are disabled (shutdown).</p>  |
| 0    | RESERVED | Reserved. For proper operation, default value cannot be changed.   |



**Figure 5-2. LDO Control Register (LDOCNTL) [7004h]**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 5-3. LDOCNTL Register Bit Descriptions**

| BIT  | NAME       | DESCRIPTION  |
|------|------------|--|
| 15:2 | Reserved   | Reserved. read-only, writes have no effect   |
| 1    | DSP_LDO_V  | DSP_LDO voltage select bit<br>0 = DSP_LDOO is regulated to 1.3 V.<br>1 = DSP_LDOO is regulated to 1.05 V   |
| 0    | USB_LDO_EN | USB_LDO enable bit<br>0 = USB_LDO output is disabled. USB_LDOO pin is placed in high-impedance (Hi-Z) state.<br>1 = USB_LDO output is enabled. USB_LDOO is regulated to 1.3 V. |

**Table 5-4. LDO Controls Matrix**

| RTCPMGT REGISTER<br>(1930h) |            | LDOCNTL REGISTER<br>(7004h) | $\overline{\text{DSP\_LDO\_EN}}$<br>(PIN M12) | ANA_LDO | DSP_LDO | USB_LDO |
|-----------------------------|------------|-----------------------------|---|---------|---------|---------|
| BG_PD BIT                   | LDO_PD BIT | USB_LDO_EN BIT              |   |         |         |         |
| 1                           | Don't Care | Don't Care                  | Don't Care                                    | OFF     | OFF     | OFF     |
| 0                           | 1          | Don't Care                  | Don't Care                                    | OFF     | OFF     | OFF     |
| 0                           | 0          | 0                           | Low   | ON      | ON      | OFF     |
| 0                           | 0          | 0                           | High  | ON      | OFF     | OFF     |
| 0                           | 0          | 1                           | Low   | ON      | ON      | ON      |

## 5.6.2 Clock Considerations

Used by the CPU and most of the DSP peripherals, the system clock is controlled by the system clock generator. The system clock generator features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input reference clock from the CLKIN pin or the output clock of the 32.768-kHz real-time clock (RTC) oscillator. The selection of the input reference clock is based on the state of the CLK\_SEL pin. The CLK\_SEL pin is required to be statically tied high or low and cannot change dynamically after reset.

The DSP requires a reference clock for USB applications. The USB reference clock is generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB\_MXI and USB\_MXO pins.

The USB reference clock is not required if the USB peripheral is unused. To completely disable the USB oscillator, connect the USB\_MXI pin to ground ( $V_{SS}$ ) and leave the USB\_MXO pin unconnected. The USB oscillator power pins (USB\_V<sub>DDOSC</sub> and USB\_V<sub>SSOSC</sub>) should also be connected to ground.

The RTC oscillator generates a clock when a 32.768-kHz crystal is connected to the RTC\_XI and RTC\_XO pins. The 32.768-kHz crystal can be disabled if CLKIN is used as the clock source for the DSP. When the RTC oscillator is disabled, the RTC peripheral will not operate and the RTC registers (I/O address range 1900h to 197Fh) will not be accessible. To disable the RTC oscillator, connect the RTC\_XI pin to CV<sub>DDRTC</sub> and the RTC\_XO pin to ground.

For more information on crystal specifications for the RTC oscillator and the USB oscillator, see [Section 5.6.6, External Clock Input From RTC\\_XI, CLKIN, and USB\\_MXI Pins](#).

### 5.6.2.1 Clock Configurations After Device Reset

After reset, the on-chip bootloader programs the system clock generator based on the input clock selected through the CLK\_SEL pin.

If CLK\_SEL = 0, the bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375).

If CLK\_SEL = 1, the bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin. In this case, the CLKIN frequency is expected to be 11.2896 MHz, 12.000 MHz, or 12.288 MHz. While the bootloader tries to boot from the USB, the clock generator will be programmed to output approximately 36 MHz.

#### 5.6.2.1.1 Device Clock Frequency

After the boot process is complete, reprogram the system clock generator to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating or not). Adhere to the clock requirements when programming the system clock generator. For more information, see [Section 5.6.7, Clock PLLs](#).

---

#### NOTE

The on-chip bootloader allows for DSP registers to be configured during the boot process. Do not use this feature to change the output frequency of the system clock generator during the boot process. The bootloader also uses Timer0 to calculate the settling time of BG\_CAP until executing bootloader code. The bootloader register modification feature must not modify the Timer0 registers.

---

### 5.6.2.1.2 Peripheral Clock State

The clock and reset state of each of peripheral is controlled through a set of system registers. The peripheral clock gating control registers (PCGCR1 and PCGCR2) enable and disable peripheral clocks. The peripheral software reset counter register (PSRCR) and the peripheral reset control register (PRCR) assert and deassert peripheral reset signals.

At hardware reset, all of the peripheral clocks are off to conserve power. After hardware reset, the DSP boots through the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. In this process, the bootloader reads each peripheral searching for a valid boot image file. At that time, the individual peripheral clocks will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. When the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR will be idled except for the CPU domain.

### 5.6.2.1.3 USB Oscillator Control

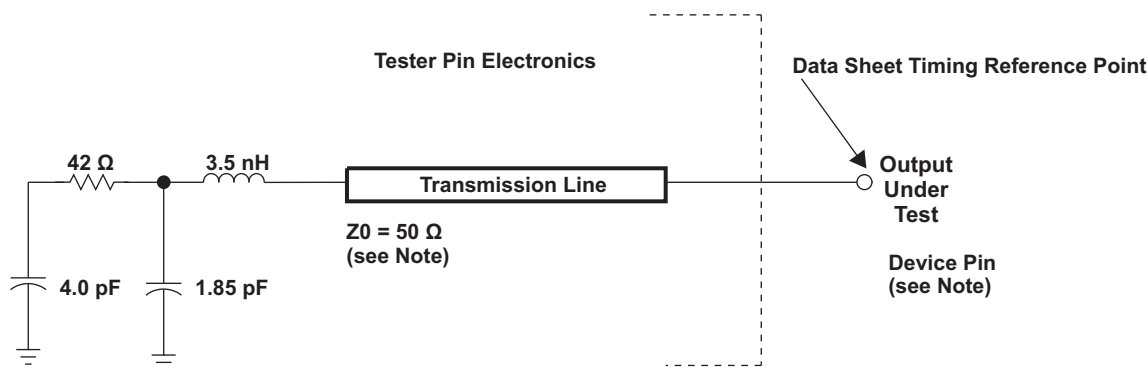
The USB system control register (USBSCR) controls the USB oscillator. To enable the oscillator, the USBOSCDIS and USBOSCBIASDIS bits must be cleared to 0. Wait until the USB oscillator stabilizes before proceeding with the USB configuration. The USB oscillator stabilization time is typically 100  $\mu$ s, with a 10 ms maximum.

#### NOTE

The start-up time is dependent on the ESR and capacitive load on the crystal.

### 5.6.3 Parameter Information

Figure 5-3 shows the test load circuit for AC timing measurements.



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

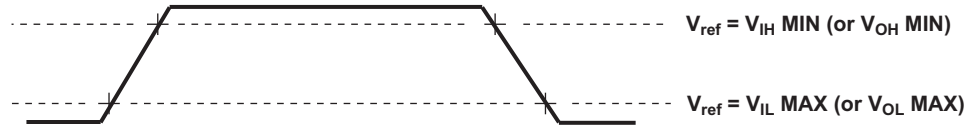
**Figure 5-3. 3.3-V Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

### 5.6.3.1 1.8-V, 2.5-V, 2.75-V, and 3.3-V Signal Transition Levels

All rise and fall transition timing parameters are referenced to  $V_{IL\ MAX}$  and  $V_{IH\ MIN}$  for input clocks,  $V_{OL\ MAX}$  and  $V_{OH\ MIN}$  for output clocks.

Figure 5-4 shows the rise and fall transition time of the voltage reference levels.



**Figure 5-4. Rise and Fall Transition Time Voltage Reference Levels**

### 5.6.3.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

### 5.6.3.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do not include delays by board routing. As a good practice, always take delays into account. Increase or decrease delays to adjust timing values. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see *Using IBIS Models for Timing Analysis* (SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

### 5.6.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.

## 5.6.5 Power Supplies

The device includes four core voltage-level supplies ( $CV_{DD}$ ,  $CV_{DDRTC}$ ,  $USB\_V_{DD1P3}$ ,  $USB\_V_{DDA1P3}$ ), and four I/O supplies ( $DV_{DDIO}$ ,  $DV_{DDRTC}$ ,  $USB\_V_{DDOSC}$ , and  $USB\_V_{DDA3P3}$ ), as well as four analog supplies (LDO1,  $V_{DDA\_PLL}$ ,  $V_{DDA\_ANA}$ , and  $USB\_V_{DDPLL}$ ). Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start and Enable features. For more information regarding TI's power management products and suggested devices to power TI DSPs, see [www.ti.com/processorpower](http://www.ti.com/processorpower).

### 5.6.5.1 Power-Supply Sequencing

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#### NOTE

The external reset signal on the  $\overline{RESET}$  pin must be held low until all of the external power supplies reach their operating voltage conditions.

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The device includes four core voltage-level supplies ( $CV_{DD}$ ,  $CV_{DDRTC}$ ,  $USB\_V_{DD1P3}$ ,  $USB\_V_{DDA1P3}$ ), and four I/O supplies ( $DV_{DDIO}$ ,  $DV_{DDRTC}$ ,  $USB\_V_{DDOSC}$ , and  $USB\_V_{DDA3P3}$ ).

If the DSP\_LDO is disabled ( $\overline{DSP\_LDO\_EN} = \text{high}$ ) and an external regulator supplies power to the CPU Core ( $CV_{DD}$ ), the external reset signal ( $\overline{RESET}$ ) must be held asserted until all of the supply voltages reach their valid operating ranges.

The I/O design allows either the core supplies ( $CV_{DD}$ ,  $CV_{DDRTC}$ ,  $USB\_V_{DD1P3}$ ,  $USB\_V_{DDA1P3}$ ) or the I/O supplies ( $DV_{DDIO}$ ,  $DV_{DDRTC}$ ,  $USB\_V_{DDOSC}$ , and  $USB\_V_{DDA3P3}$ ) to be powered up for an indefinite period of time while the other supply is not powered if the following constraints are met:

1. All maximum ratings and recommended operating conditions are satisfied.
2. All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature are satisfied. These apply to power transitions as well as normal operation.
3. Bus contention while core supplies are powered must be limited to 100 hours over the projected lifetime of the device.
4. Bus contention while core supplies are powered down does not violate the absolute maximum ratings.

If the USB subsystem is used, the subsystem must be powered up in the following sequence:

1.  $USB\_V_{DDA1P3}$  and  $USB\_V_{DD1P3}$
2.  $USB\_V_{DDA3P3}$
3.  $USB\_V_{BUS}$

If the USB subsystem is unused, the following can be powered off:

- USB Core
  - $USB\_V_{DD1P3}$
  - $USB\_V_{DDA1P3}$
- USB PHY and I/O level supplies
  - $USB\_V_{DDOSC}$
  - $USB\_V_{DDA3P3}$
  - $USB\_V_{DDPLL}$

A supply bus is powered up when the voltage is within the TI-recommended operating range. The supply bus is powered down when the voltage is below that range, either stable or while in transition.

### 5.6.5.2 Digital I/O Behavior When Core Power ( $CV_{DD}$ ) is Down

With some exceptions, all digital I/O pins on the device have special features to allow powering down of the digital core domain ( $CV_{DD}$ ) without causing I/O contentions or floating inputs at the pins (see [Figure 5-5](#)). The device asserts the internal signal called HHV high when power has been removed from the digital core domain ( $CV_{DD}$ ). Asserting the internal HHV signal causes the following conditions to occur in any order:

- All output pin strong drivers to go to the high-impedance (Hi-Z) state
- Weak bus-holders to be enabled to hold the pin at a valid high or low
- The internal pullups or pulldowns (IPUs and IPDs) on the I/O pins will be disabled

The exception pins that do not have this special feature are:

- Pins driven by the  $CV_{DDRTC}$  Power Domain [This power domain is Always On; therefore, the pins driven by  $CV_{DDRTC}$  do not need these special features]:
  - RTC\_XI and RTC\_XO
- USB Pins:
  - USB\_DP, USB\_DM, USB\_R1, USB\_VBUS, USB\_MXI, and USB\_MXO

#### NOTE

The USB oscillator consumes power when core voltage is removed. For more information, see *TMS320C5545A Fixed-Point DSP Silicon Errata (SPRZ404)*.

- Pins for the Analog Block:
  - GPAIN[3:1],  $\overline{DSP\_LDO\_EN}$  and BG\_CAP

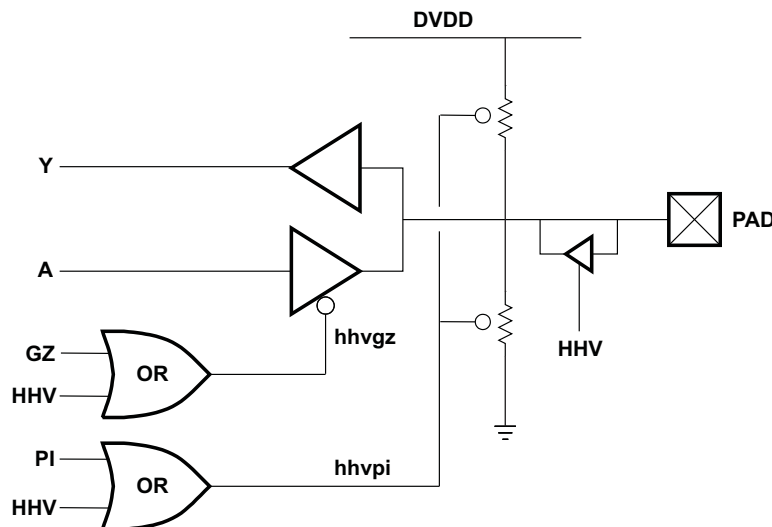


Figure 5-5. Bus-Holder I/O Circuit

#### NOTE

[Figure 5-5](#) shows both a pullup and pulldown but pins have only one, not both.

PI = Pullup and pulldown Inhibit

GZ = Output enable (active low)

HHV = Described in [Section 5.6.5.2](#)

### 5.6.5.3 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. When designing for high-performance applications using the device, the PC board should include separate power planes for core, I/O,  $V_{DDA\_ANA}$  and  $V_{DDA\_PLL}$  (which can share the same PCB power plane), and ground; all bypassed with high-quality low-ESL and ESR capacitors.

### 5.6.5.4 Power-Supply Decoupling

To properly decouple the supply planes from system noise, place capacitors (caps) as close as possible to the device. These caps should be no more than 1.25 cm maximum distance from the device power pins to be effective. Physically smaller caps, like 0402, are better but must be evaluated from a yield and manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors; physically smaller capacitors must be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 10  $\mu\text{F}$ ) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime must be considered.

The recommended decoupling capacitance for the DSP core supplies should be 1  $\mu\text{F}$  in parallel with 0.01- $\mu\text{F}$  capacitor per supply pin.

### 5.6.5.5 LDO Input Decoupling

The LDO inputs should follow the same decoupling guidelines as other power-supply pins.

### 5.6.5.6 LDO Output Decoupling

The LDO circuits implement a voltage feedback control system which TI has designed to optimize gain and stability tradeoffs. Design assumptions exist for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors must be used when the on-chip LDOs are enabled:

- ANA\_LDOO – 1  $\mu\text{F}$
- DSP\_LDOO – 5  $\mu\text{F}$  to 10  $\mu\text{F}$
- USB\_LDOO – 1  $\mu\text{F}$  to 2  $\mu\text{F}$



### 5.6.6 External Clock Input From RTC\_XI, CLKIN, and USB\_MXI Pins

The device DSP includes two options to provide an external clock input to the system clock generator:

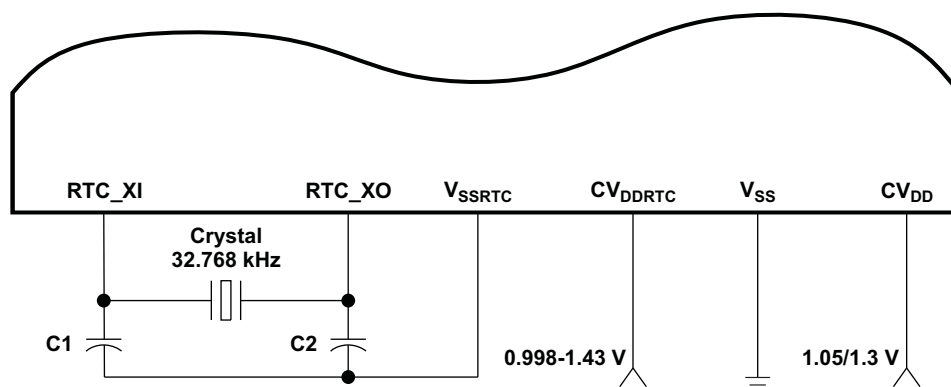
- Use the on-chip RTC oscillator with an external 32.768-kHz crystal connected to the RTC\_XI and RTC\_XO pins.
- Use an external 11.2896-, 12.0-, or 12.288-MHz LVCMOS clock input fed into the CLKIN pin that operates at the same voltage as the DV<sub>DDIO</sub> supply (1.8-, 2.5-, 2.75-, or 3.3-V).

The CLK\_SEL pin determines which input is used as the clock source for the system clock generator. For more details, see [Section 6.5.1, Device and Peripheral Configurations at Device Reset](#). The crystal for the RTC oscillator is not required if CLKIN is used as the system reference clock but the RTC must still be powered by an external power source. None of the on-chip LDOs can power CV<sub>DDRTC</sub>. The RTC registers starting at I/O address 1900h will be inaccessible without an RTC clock. [Section 5.6.6.1, Real-Time Clock \(RTC\) On-Chip Oscillator With External Crystal](#) provides more details on using the RTC on-chip oscillator with an external crystal. [Section 5.6.6.2, CLKIN Pin With LVCMOS-Compatible Clock Input](#) provides details on using an external LVCMOS-compatible clock input fed into the CLKIN pin.

The USB requires a reference clock generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB\_MXI and USB\_MXO pins. The USB reference clock is not required if the USB peripheral is unused. [Section 5.6.6.3, USB On-Chip Oscillator With External Crystal](#) provides details on using the USB on-chip oscillator with an external crystal.

#### 5.6.6.1 Real-Time Clock (RTC) On-Chip Oscillator With External Crystal

The on-chip oscillator requires an external 32.768-kHz crystal connected across the RTC\_XI and RTC\_XO pins, along with two load capacitors, as shown in [Figure 5-6](#). The external crystal load capacitors must be connected only to the RTC oscillator ground pin (V<sub>SSRTC</sub>). Do not connect to board ground (V<sub>SS</sub>). Position the V<sub>SS</sub> lead on the board between RTC\_XI and RTC\_XO as a shield to reduce direct capacitance between RTC\_XI and RTC\_XO leads on the board. The CV<sub>DDRTC</sub> pin can be connected to the same power supply as CV<sub>DD</sub>, or may be connected to a different supply that meets the recommended operating conditions (see [Section 5.3, Recommended Operating Conditions](#)), if desired. However, the CV<sub>DDRTC</sub> pin must not be supplied by any on-chip LDOs.



**Figure 5-6. 32.768-kHz RTC Oscillator**

The crystal should be in fundamental-mode function, and parallel resonant, with a maximum effective series resistance (ESR) specified in [Table 5-5](#). The load capacitors, C1 and C2, are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitors values are usually approximately twice the value of the load capacitance (CL) of the crystal, specified in the crystal manufacturer's data sheet and should be chosen to satisfy the equation.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

All discrete components used to implement the oscillator circuit must be placed as close as possible to the associated oscillator pins (RTC\_XI and RTC\_XO) and to the  $V_{SSRTC}$  pin.

**Table 5-5. Input Requirements for Crystal on the 32.768-kHz RTC Oscillator**

| PARAMETER  | MIN | NOM    | MAX | UNIT       |
|--|-----|--------|-----|------------|
| Start-up time (from power up until oscillating at stable frequency of 32.768-kHz) <sup>(1)</sup> | 0.2 |        | 2   | sec        |
| Oscillation frequency  |     | 32.768 |     | kHz        |
| ESR  |     |        | 100 | k $\Omega$ |
| Maximum shunt capacitance  |     |        | 1.6 | pF         |
| Maximum crystal drive  |     |        | 1.0 | $\mu$ W    |

(1) The start-up time is highly dependent on the ESR and the capacitive load of the crystal.

### 5.6.6.2 CLKIN Pin With LVCMOS-Compatible Clock Input (Optional)

#### NOTE

If CLKIN is not used, the pin must be tied low.

A LVCMOS-compatible clock input of a frequency less than 24 MHz can be fed into the CLKIN pin for use by the DSP system clock generator. The external connections are shown in [Figure 5-7](#) and [Figure 5-8](#). The bootloader assumes that the CLKIN pin is connected to the LVCMOS-compatible clock source with a frequency of 11.2896-, 12.0-, or 12.288-MHz. These frequencies were selected to support boot mode peripheral speeds of 500 kHz for SPI and 400 kHz for I2C and UART. These clock frequencies are achieved by dividing the CLKIN value by 25 for SPI and by 32 for I2C and UART. If a faster external clock is input, then these boot modes will run at faster clock speeds. If the system design uses faster peripherals or these boot modes are not used, CLKIN values higher than 12.288 MHz can be used.

#### NOTE

The CLKIN pin operates at the same voltage as the  $DV_{DDIO}$  supply (1.8-, 2.5-, 2.75-, or 3.3-V).

In this configuration the RTC oscillator can be optionally disabled by connecting RTC\_XI to  $CV_{DDRTC}$  and RTC\_XO to ground ( $V_{SS}$ ). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible.

#### NOTE

The RTC core must still be powered by an external power source even if the RTC oscillator is disabled. None of the on-chip LDOs can power  $CV_{DDRTC}$ .

For more details on the RTC on-chip oscillator, see [Section 5.6.6.1, Real-Time Clock \(RTC\) On-Chip Oscillator With External Crystal](#).

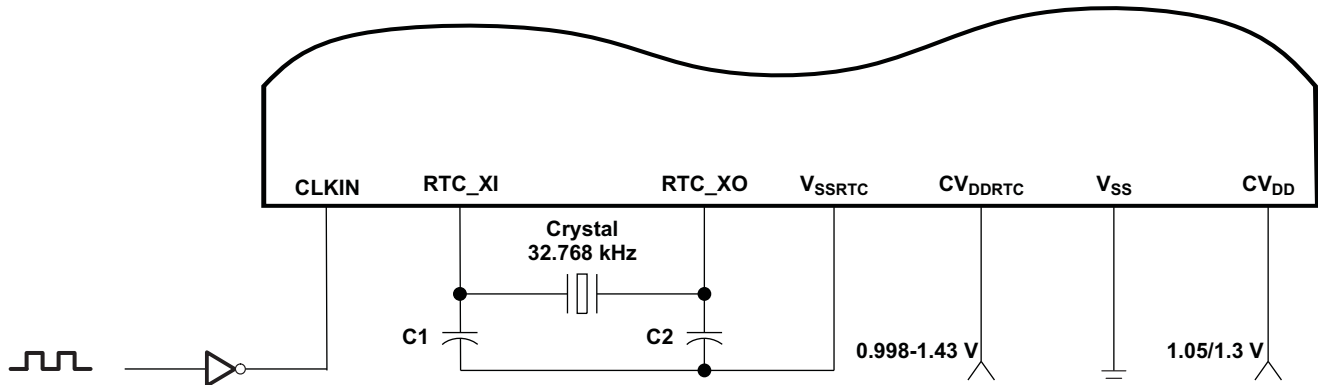


Figure 5-7. LVC MOS-Compatible Clock Input With RTC Oscillator Enabled

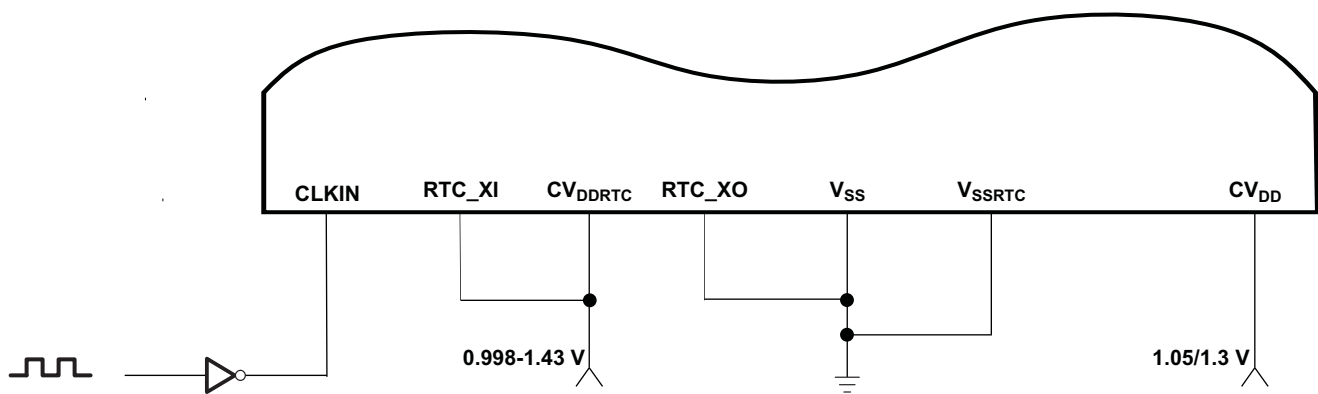


Figure 5-8. LVC MOS-Compatible Clock Input With RTC Oscillator Disabled

### 5.6.6.3 USB On-Chip Oscillator With External Crystal (Optional)

When using the USB, the USB on-chip oscillator requires an external 12-MHz crystal connected across the USB\_MXI and USB\_MXO pins, along with two load capacitors, as shown in [Figure 5-9](#). The external crystal load capacitors must be connected only to the USB oscillator ground pin (USB\_VSSOSC). Do not connect to board ground (V<sub>SS</sub>). The USB\_VDDOSC pin can be connected to the same power supply as USB\_VDDA3P3.

The USB on-chip oscillator can be permanently disabled, through tie-offs, if the USB peripheral is unused. To permanently disable the USB oscillator, connect the USB\_MXI pin to ground (V<sub>SS</sub>) and leave the USB\_MXO pin unconnected. The USB oscillator power pins (USB\_VDDOSC and USB\_VSSOSC) should also be connected to ground, as shown in [Figure 5-10](#).

When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB\_MXI pin and the amplitude of the oscillator clock signal must meet the V<sub>IH</sub> requirement (see [Section 5.3, Recommended Operating Conditions](#)). The USB\_MXO remains unconnected and the USB\_VSSOSC signal is connected to board ground (V<sub>SS</sub>).

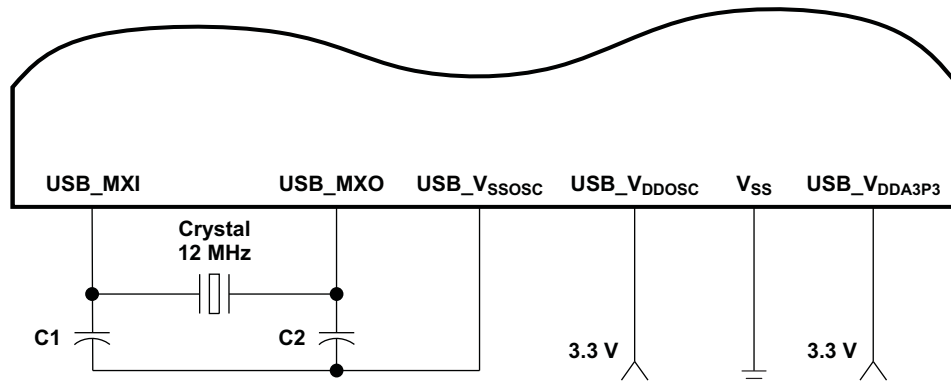


Figure 5-9. 12-MHz USB Oscillator

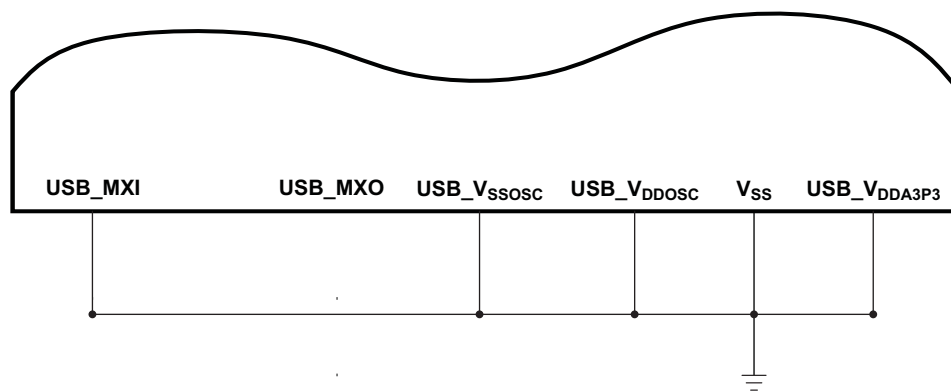


Figure 5-10. Connections when USB Oscillator is Permanently Disabled

The crystal should be in fundamental-mode operation and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5-6. The load capacitors, C1 and C2 are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitor value is usually approximately twice the value of the load capacitance (CL) of the crystal, specified in the crystal manufacturer's data sheet and should be chosen such that the equation below is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (USB\_MXI and USB\_MXO) and to the USB\_VSSOSC pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)} \tag{1}$$

Table 5-6. Input Requirements for Crystal on the 12-MHz USB Oscillator

| PARAMETER  | MIN | NOM   | MAX  | UNIT |
|--|-----|-------|------|------|
| Start-up time (from power up until oscillating at stable frequency of 12 MHz) <sup>(1)</sup> |     | 0.100 | 10   | ms   |
| Oscillation frequency  |     | 12    |      | MHz  |
| ESR  |     |       | 100  | Ω    |
| Frequency stability <sup>(2)</sup>   |     |       | ±100 | ppm  |
| Maximum shunt capacitance  |     |       | 5    | pF   |
| Maximum crystal drive  |     |       | 330  | μW   |

(1) The start-up time is highly dependent on the ESR and the capacitive load of the crystal.

(2) If the USB is used, a 12-MHz, ±100-ppm crystal is recommended.

### 5.6.7 Clock PLLs

The DSP uses a software-programmable PLL to generate frequencies required by the CPU, DMA, and peripherals. The reference clock for the PLL is taken from either the CLKIN pin or the RTC on-chip oscillator (specified through the CLK\_SEL pin).

#### 5.6.7.1 PLL Device-Specific Information

Table 5-7 lists the PLL clock frequency ranges.

**Table 5-7. PLL Clock Frequency Ranges**

| CLOCK SIGNAL NAME    | CV <sub>DD</sub> = 1.05 V<br>V <sub>D<sub>DA</sub>_PLL</sub> = 1.3 V |                         | CV <sub>DD</sub> = 1.3 V<br>V <sub>D<sub>DA</sub>_PLL</sub> = 1.3 V |                         | UNIT |
|----------------------|--|-------------------------|---|-------------------------|------|
|                      | MIN  | MAX                     | MIN   | MAX                     |      |
| CLKIN <sup>(1)</sup> |  | 11.2896<br>12<br>12.288 |   | 11.2896<br>12<br>12.288 | MHz  |
| RTC Clock            |  | 32.768                  |   | 32.768                  | kHz  |
| PLLIN                | 32.768   | 170                     | 32.768  | 170                     | kHz  |
| PLLOUT               | 60   | 100                     | 60  | 100                     | MHz  |
| SYSCLK               | 0.032768   | 60                      | 0.032768  | 100                     | MHz  |
| PLL_LOCKTIME         |  | 4                       |   | 4                       | ms   |

(1) These CLKIN values are used when the CLK\_SEL pin = 1.

Follow the lock time requirements for the PLL. The PLL lock time is the amount of time needed for the PLL to complete its phase-locking sequence.

#### 5.6.7.2 Clock PLL Considerations With External Clock Sources

If the CLKIN pin provides the reference clock to the PLL, a single clean power supply should power both the device and the external clock oscillator circuit to minimize the clock jitter. Observe the minimum CLKIN rise and fall times. For the input clock timing requirements, see [Section 5.6.7.3, Clock PLL Electrical Data and Timing \(Input and Output Clocks\)](#).

Rise and fall times, duty cycles (high and low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see [Section 5.5, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature](#), and [Section 5.6.7.3, Clock PLL Electrical Data and Timing \(Input and Output Clocks\)](#)).

5.6.7.3 Clock PLL Electrical Data and Timing (Input and Output Clocks)

Table 5-8 and Table 5-9 list the timing and switching requirements for CLKIN and CLKOUT, respectively.

Table 5-8. Timing Requirements for CLKIN<sup>(1)</sup> <sup>(2)</sup> (see Figure 5-11)

| NO. |  | CV <sub>DD</sub> = 1.05 V        |                                    |     | CV <sub>DD</sub> = 1.3 V           |     |     | UNIT |
|-----|--|----------------------------------|------------------------------------|-----|------------------------------------|-----|-----|------|
|     |  | MIN                              | NOM                                | MAX | MIN                                | NOM | MAX |      |
| 1   | t <sub>c(CLKIN)</sub> Cycle time, external clock driven on CLKIN |                                  | 88.577,<br>83.333,<br>or<br>81.380 |     | 88.577,<br>83.333,<br>or<br>81.380 |     | ns  |      |
| 2   | t <sub>w(CLKINH)</sub> Pulse width, CLKIN high                   | 0.466 ×<br>t <sub>c(CLKIN)</sub> |                                    |     | 0.466 ×<br>t <sub>c(CLKIN)</sub>   |     | ns  |      |
| 3   | t <sub>w(CLKINL)</sub> Pulse width, CLKIN low                    | 0.466 ×<br>t <sub>c(CLKIN)</sub> |                                    |     | 0.466 ×<br>t <sub>c(CLKIN)</sub>   |     | ns  |      |
| 4   | t <sub>t(CLKIN)</sub> Transition time, CLKIN                     |                                  |                                    | 4   |                                    | 4   | ns  |      |

- (1) The CLKIN frequency and PLL multiply factor must be chosen so that the resulting clock frequency is within the specific range for CPU operating frequency.
- (2) The reference points for the rise and fall transitions are measured at V<sub>IL</sub> MAX and V<sub>IH</sub> MIN.

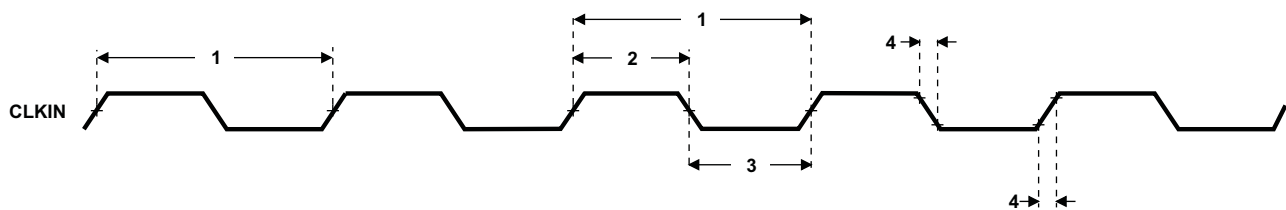


Figure 5-11. CLKIN Timing

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for CLKOUT<sup>(1)</sup> <sup>(2)</sup> (see Figure 5-12)

| NO. | PARAMETER   | CV <sub>DD</sub> = 1.05 V<br>V <sub>DDA_PLL</sub> = 1.3 V |       | CV <sub>DD</sub> = 1.3 V<br>V <sub>DDA_PLL</sub> = 1.3 V |     | UNIT |
|-----|---|---|-------|--|-----|------|
|     |   | MIN   | MAX   | MIN  | MAX |      |
| 1   | t <sub>c(CLKOUT)</sub> Cycle time, CLKOUT                             | P   | 16.67 | P  | 10  | ns   |
| 2   | t <sub>w(CLKOUTH)</sub> Pulse duration, CLKOUT high                   | 0.466 ×<br>t <sub>c(CLKOUT)</sub>                         |       | 0.466 ×<br>t <sub>c(CLKOUT)</sub>                        |     | ns   |
| 3   | t <sub>w(CLKOUTL)</sub> Pulse duration, CLKOUT low                    | 0.466 ×<br>t <sub>c(CLKOUT)</sub>                         |       | 0.466 ×<br>t <sub>c(CLKOUT)</sub>                        |     | ns   |
| 4   | t <sub>t(CLKOUTR)</sub> Transition time (rise), CLKOUT <sup>(3)</sup> |   | 5     |  | 5   | ns   |
| 5   | t <sub>t(CLKOUTF)</sub> Transition time (fall), CLKOUT <sup>(3)</sup> |   | 5     |  | 5   | ns   |

- (1) The reference points for the rise and fall transitions are measured at V<sub>OL</sub> MAX and V<sub>OH</sub> MIN.
- (2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.
- (3) Transition time is measured with the slew rate set to FAST and DV<sub>DDIO</sub> = 1.65 V. (For more detailed information, see the Section 6.6.6, Output Slew Rate Control Register (OSRCR) [1C16h].).

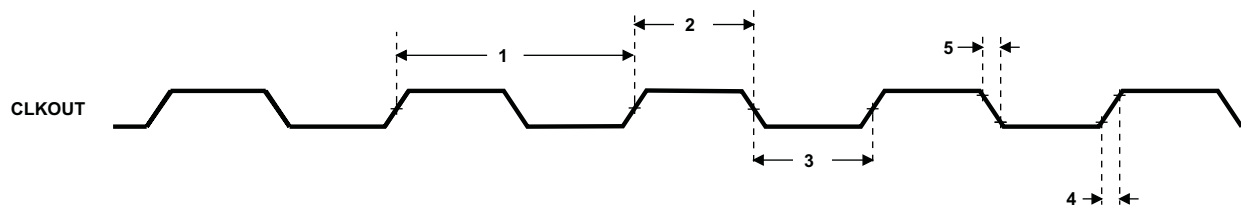


Figure 5-12. CLKOUT Timing

### 5.6.8 Direct Memory Access (DMA) Controller

The DMA controller moves data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

The DSP includes a total of four DMA controllers. Aside from the DSP resources they can access, all four DMA controllers are identical.

The DMA controller has the following features:

- Operation that is independent of the CPU.
- Four channels, which allow the DMA controller to keep track of the context of four independent block transfers.
- Event synchronization. DMA transfers in each channel can be made dependent on the occurrence of selected events.
- An interrupt for each channel. Each channel can send an interrupt to the CPU on completion of the programmed transfer.
- Ping-Pong mode allows the DMA controller to keep track of double-buffering context without CPU intervention.
- A dedicated clock idle domain. The four device DMA controllers can be put into a low-power state by independently turning off their input clocks.

#### 5.6.8.1 DMA Channel Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMA<sub>n</sub> channel event source registers (DMA<sub>n</sub>CESR1 and DMA<sub>n</sub>CESR2).



## 5.6.9 Reset

The device has two main types of reset: hardware reset and software reset.

Hardware reset is responsible for initializing all key states of the device. The hardware reset occurs whenever the  $\overline{\text{RESET}}$  pin is asserted or when the internal power-on-reset (POR) circuit deasserts an internal signal called POWERGOOD. The device's internal POR is a voltage comparator that monitors the DSP\_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP\_LDO is enabled externally by the  $\overline{\text{DSP\_LDO\_EN}}$  pin. POWERGOOD is asserted when the DSP\_LDOO voltage is above a minimum threshold voltage provided by the bandgap. When the DSP\_LDO is disabled ( $\overline{\text{DSP\_LDO\_EN}}$  is high), the internal voltage comparator becomes inactive, and the POWERGOOD signal logic level is immediately set high. The  $\overline{\text{RESET}}$  pin and the POWERGOOD signal are internally combined with a logical AND gate to produce an (active low) hardware reset (see , *Power-On Reset Timing Requirements* and , *Reset Timing Requirements*).

There are two types of software reset: the CPU's software reset instruction and the software control of the peripheral reset signals. For more information on the CPU's software reset instruction, see the *TMS320C55x CPU 3.0 CPU Reference Guide (SWPU073)*. In all the device documentation, all references to reset refer to hardware reset. Any references to software reset will explicitly state software reset.

The device RTC has one additional type of reset, a power-on-reset (POR) for the registers in the RTC core. This POR monitors the voltage of  $\text{CV}_{\text{DDRTC}}$  and resets the RTC registers when power is first applied to the RTC core.

### 5.6.9.1 Power-On Reset (POR) Circuits

The device includes two power-on reset (POR) circuits, one for the RTC (RTC POR) and another for the rest of the chip (MAIN POR).

#### 5.6.9.1.1 RTC Power-On Reset (POR)

The RTC POR ensures that the flip-flops in the  $\text{CV}_{\text{DDRTC}}$  power domain have an initial state upon power-up. In particular, the RTCNOPWR register is reset by this POR and is used to indicate that the RTC time registers must be initialized with the current time and date when power is first applied.

#### 5.6.9.1.2 Main Power-On Reset (POR)

The device includes an analog power-on reset (POR) circuit that keeps the DSP in reset until specific voltages have reached predetermined levels. When the DSP\_LDO is enabled externally by the  $\overline{\text{DSP\_LDO\_EN}}$  pin, the output of the POR circuit, POWERGOOD, is held low until the following conditions are satisfied:

- LDO1 is powered
- The bandgap is active for at least approximately 8 ms
- $\text{VDD\_ANA}$  is powered for at least approximately 4 ms
- DSP\_LDOO is above approximately 950 mV

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#### NOTE

The POR comparator has hysteresis, so the threshold voltage becomes approximately 850 mV after POWERGOOD signal is set high.

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When these conditions are met, the internal POWERGOOD signal is set high. The POWERGOOD signal is internally combined with the  $\overline{\text{RESET}}$  pin signal, through an AND-gate, to produce the DSP subsystem's global reset. This global reset is the hardware reset for the whole chip, except the RTC. When the global reset is deasserted (high), the boot sequence starts. For more detailed information on the boot sequence, see [Section 6.4, Boot Sequence](#).

When the DSP\_LDO is disabled ( $\overline{\text{DSP\_LDO\_EN}}$  pin = 1), the voltage monitoring on the DSP\_LDO pin is deactivated and the POWERGOOD signal is immediately set high. The  $\overline{\text{RESET}}$  pin will be the sole source of hardware reset.

### 5.6.9.1.3 Reset Pin ( $\overline{\text{RESET}}$ )

The device can receive an external reset signal on the  $\overline{\text{RESET}}$  pin. As specified in [Section 5.6.9.1.2, Main Power-On Reset](#), the  $\overline{\text{RESET}}$  pin is combined with the internal POWERGOOD signal, generated by the MAIN POR through an AND-gate. The output of the AND gate provides the hardware reset to the chip. The  $\overline{\text{RESET}}$  pin may be tied high and the MAIN POR can provide the hardware reset in case DSP\_LDO is enabled ( $\overline{\text{DSP\_LDO\_EN}} = 0$ ), but an external hardware reset must be provided through the  $\overline{\text{RESET}}$  pin when the DSP\_LDO is disabled ( $\overline{\text{DSP\_LDO\_EN}} = 1$ ).

When the hardware reset is applied, the system clock generator is enabled and the DSP starts the boot sequence. For more information on the boot sequence, see [Section 6.4, Boot Sequence](#).

### 5.6.9.2 Pin Behavior at Reset

Pins are controlled by the respective peripheral selected in the external bus selection register (EBSR) register. During power-on reset and reset, the behavior of the output pins changes. These changes are categorized as follows:

- **High Group:** LCD\_RS/SPI\_CS3
- **Low Group:** LCD\_EN\_RDB/ SPI\_CLK, SD0\_CLK/I2S0\_CLK/GP[0], SD1\_CLK/I2S1\_CLK/GP[6]
- **Z Group:** EMU[1:0], SCL, SDA, LCD\_D[0]/SPI\_RX, LCD\_D[1]/ SPI\_TX, LCD\_D[10]/ I2S2\_RX/GP[20]/SPI\_RX, LCD\_D[11]/I2S2\_DX/GP[27]/SPI\_TX, LCD\_D[12]/UART\_RTS/GP[28]/I2S3\_CLK, LCD\_D[13]/ UART\_CTS/GP[29]/I2S3\_FS, LCD\_D[14]/UART\_RXD/GP[30]/I2S3\_RX, LCD\_D[15]/UART\_TXD/GP[31]/I2S3\_DX, LCD\_D[2]/ GP[12], LCD\_D[3]/ GP[13], LCD\_D[4]/ GP[14], LCD\_D[5]/ GP[15], LCD\_D[6]/ GP[16], LCD\_D[7]/ GP[17], LCD\_D[8]/ I2S2\_CLK/GP[18]/SPI\_CLK, LCD\_D[9] I2S2\_FS/GP[19]/SPI\_CS0, SD0\_CMD/I2S0\_FS/GP[1], SD0\_D0/I2S0\_DX/GP[2], SD0\_D1/I2S0\_RX/GP[3], SD0\_D2/GP[4], SD0\_D3/GP[5], SD1\_CMD/I2S1\_FS/GP[7], SD1\_D0/I2S1\_DX/GP[8], SD1\_D1/I2S1\_RX/GP[9], SD1\_D2/GP[10], SD1\_D3/GP[11], TDO
- **CLKOUT Group:** CLKOUT
- **SYNCH 0→1 Group:** LCD\_CS0\_E0/SPI\_CS0, LCD\_RW\_WRB/SPI\_CS2

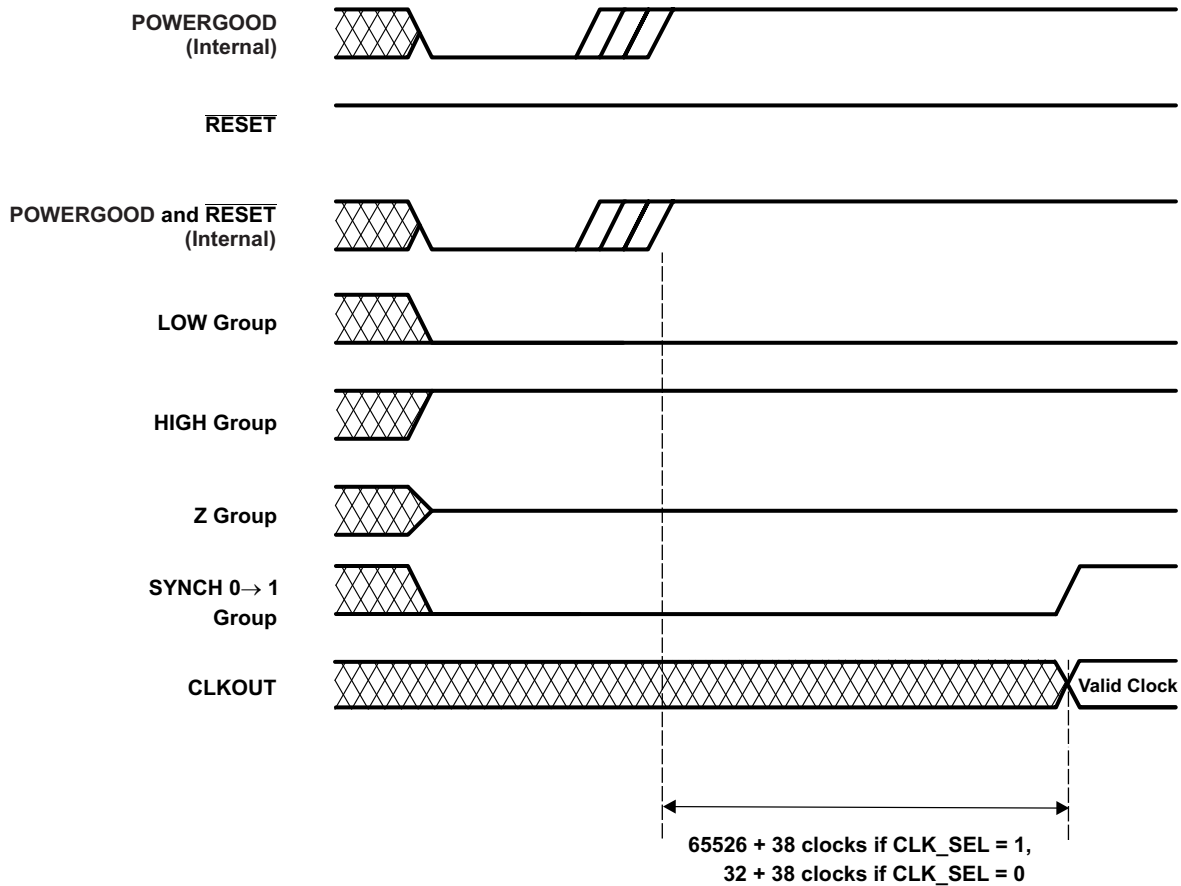
### 5.6.9.3 Reset Electrical Data and Timing

Table 5-10 lists the timing requirements for resets.

**Table 5-10. Timing Requirements for Reset<sup>(1)</sup>** (see Figure 5-13 and Figure 5-14)

| NO. |  | CV <sub>DD</sub> = 1.05 V |     | CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|--|---------------------------|-----|--------------------------|-----|------|
|     |  | MIN                       | MAX | MIN                      | MAX |      |
| 1   | t <sub>w(RSTL)</sub> Pulse duration, $\overline{\text{RESET}}$ low | 3P                        |     | 3P                       |     | ns   |

(1) P = 1/SYSCLK clock frequency in ns. For example, if SYSCLK = 12 MHz, use P = 83.3 ns. In IDLE3 mode the system clock generator is bypassed and the SYSCLK frequency is equal to either CLKIN or the RTC clock frequency depending on CLK\_SEL.



**Figure 5-13. Power-On Reset Timing Requirements**

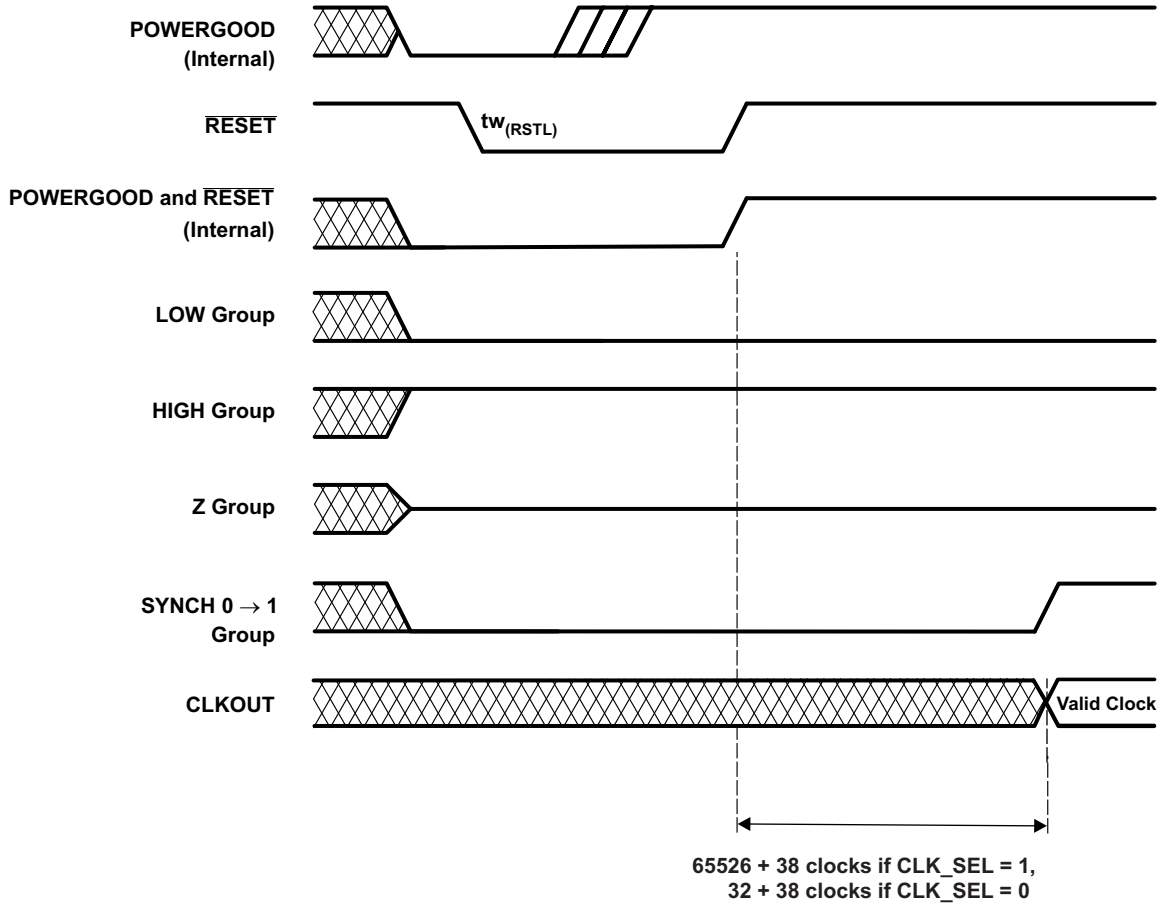


Figure 5-14. Reset Timing Requirements

### 5.6.10 Interrupts

The device has interrupts to service its peripherals. The interrupts can be selectively enabled or disabled.

#### 5.6.10.1 Interrupts Electrical Data and Timing

Table 5-11 lists the timing requirements for interrupts.

Table 5-11. Timing Requirements for Interrupts<sup>(1)</sup> (see Figure 5-15)

| NO. |                      |   | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|----------------------|---|---|-----|------|
|     |                      |   | MIN   | MAX |      |
| 1   | t <sub>w(INTH)</sub> | Pulse duration, interrupt high CPU active | 2P  |     | ns   |
| 2   | t <sub>w(INTL)</sub> | Pulse duration, interrupt low CPU active  | 2P  |     | ns   |

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns. For example, when the CPU core is clocked at 120 MHz, use P = 8.3 ns.

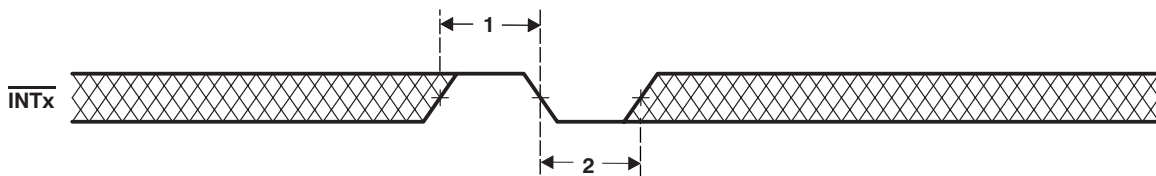


Figure 5-15. External Interrupt Timings

### 5.6.11 Secure Digital (SD)

The device includes two SD controllers that are compliant with Secure Digital Part 1 Physical Layer Specification V2.0 and Secure Digital Input Output (SDIO) V2.0 and eMMC V4.3 specifications. The SD card controller supports these industry standards and assumes the reader also supports these standards.

Each SD controller in the device has the following features:

- Embedded multimedia card and secure digital (eMMC, SD, HCSD, and HSSD) protocol support
- Programmable clock frequency
- 512-bit read and write FIFO to lower system overhead
- Slave DMA transfer capability

The SD card controller transfers data between the CPU and DMA controller on one side and the SD card on the other side. The CPU and DMA controller can read and write the data in the card by accessing the registers in the SD controller.

The SD controller on this device does not support the SPI mode of operation.

### 5.6.11.1 SD Peripheral Register Descriptions

Table 5-12 and Table 5-13 shows the SD registers. The SD0 registers start at address 3A00h and the SD1 registers start at address 3B00h.

**Table 5-12. SD0 Registers**

| HEX ADDRESS RANGE | ACRONYM   | REGISTER NAME                        |
|-------------------|-----------|--------------------------------------|
| 3A00h             | SDCTL     | SD Control Register                  |
| 3A04h             | SDCLK     | SD Memory Clock Control Register     |
| 3A08h             | SDST0     | SD Status Register 0                 |
| 3A0Ch             | SDST1     | SD Status Register 1                 |
| 3A10h             | SDIM      | SD Interrupt Mask Register           |
| 3A14h             | SDTOR     | SD Response Time-Out Register        |
| 3A18h             | SDTOD     | SD Data Read Time-Out Register       |
| 3A1Ch             | SDBLEN    | SD Block Length Register             |
| 3A20h             | SDNBLK    | SD Number of Blocks Register         |
| 3A24h             | SDNBLC    | SD Number of Blocks Counter Register |
| 3A28h             | SDDRR1    | SD Data Receive 1 Register           |
| 3A29h             | SDDRR2    | SD Data Receive 2 Register           |
| 3A2Ch             | SDDXR1    | SD Data Transmit 1 Register          |
| 3A2Dh             | SDDXR2    | SD Data Transmit 2 Register          |
| 3A30h             | SDCMD     | SD Command Register                  |
| 3A34h             | SDARGHL   | SD Argument Register                 |
| 3A38h             | SDRSP0    | SD Response Register 0               |
| 3A39h             | SDRSP1    | SD Response Register 1               |
| 3A3Ch             | SDRSP2    | SD Response Register 2               |
| 3A3Dh             | SDRSP3    | SD Response Register 3               |
| 3A40h             | SDRSP4    | SD Response Register 4               |
| 3A41h             | SDRSP5    | SD Response Register 5               |
| 3A44h             | SDRSP6    | SD Response Register 6               |
| 3A45h             | SDRSP7    | SD Response Register 7               |
| 3A48h             | SDDRSP    | SD Data Response Register            |
| 3A50h             | SDCIDX    | SD Command Index Register            |
| 3A64h to 3A70h    | –         | Reserved                             |
| 3A74h             | SDFIFOCTL | SD FIFO Control Register             |

**Table 5-13. SD1 Registers**

| HEX ADDRESS RANGE | ACRONYM   | REGISTER NAME                        |
|-------------------|-----------|--------------------------------------|
| 3B00h             | SDCTL     | SD Control Register                  |
| 3B04h             | SDCLK     | SD Memory Clock Control Register     |
| 3B08h             | SDST0     | SD Status Register 0                 |
| 3B0Ch             | SDST1     | SD Status Register 1                 |
| 3B10h             | SDIM      | SD Interrupt Mask Register           |
| 3B14h             | SDTOR     | SD Response Time-Out Register        |
| 3B18h             | SDTOD     | SD Data Read Time-Out Register       |
| 3B1Ch             | SDBLEN    | SD Block Length Register             |
| 3B20h             | SDNBLK    | SD Number of Blocks Register         |
| 3B24h             | SDNBLC    | SD Number of Blocks Counter Register |
| 3B28h             | SDDRR1    | SD Data Receive 1 Register           |
| 3B29h             | SDDRR2    | SD Data Receive 2 Register           |
| 3B2Ch             | SDDXR1    | SD Data Transmit 1 Register          |
| 3B2Dh             | SDDXR2    | SD Data Transmit 2 Register          |
| 3B30h             | SDCMD     | SD Command Register                  |
| 3B34h             | SDARGHL   | SD Argument Register                 |
| 3B38h             | SDRSP0    | SD Response Register 0               |
| 3B39h             | SDRSP1    | SD Response Register 1               |
| 3B3Ch             | SDRSP2    | SD Response Register 2               |
| 3B3Dh             | SDRSP3    | SD Response Register 3               |
| 3B40h             | SDRSP4    | SD Response Register 4               |
| 3B41h             | SDRSP5    | SD Response Register 5               |
| 3B44h             | SDRSP6    | SD Response Register 6               |
| 3B45h             | SDRSP7    | SD Response Register 7               |
| 3B48h             | SDDRSP    | SD Data Response Register            |
| 3B50h             | SDCIDX    | SD Command Index Register            |
| 3B74h             | SDFIFOCTL | SD FIFO Control Register             |



### 5.6.11.2 SD Electrical Data and Timing

Table 5-14 and Table 5-15 list the timing and switching requirements for SD, respectively.

**Table 5-14. Timing Requirements for SD (see Figure 5-16, Figure 5-17, Figure 5-18, and Figure 5-19)**

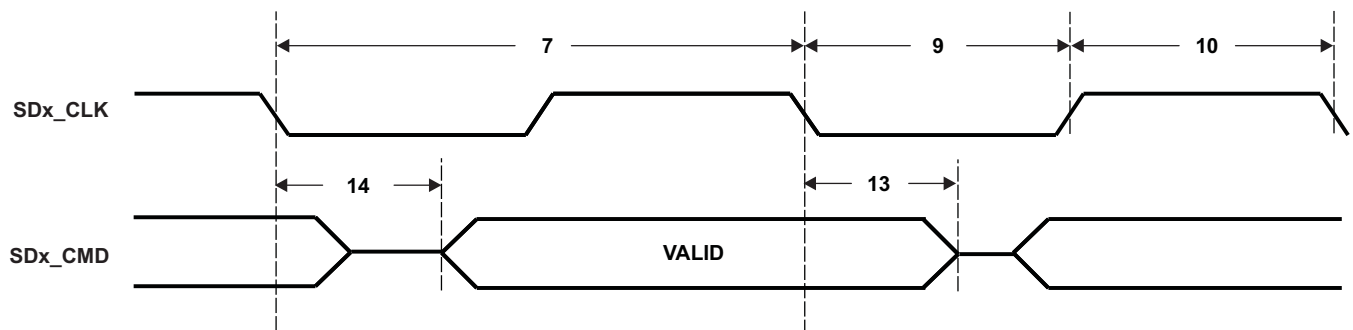
| NO. |                             | CV <sub>DD</sub> = 1.3 V                                 |     | CV <sub>DD</sub> = 1.05 V |     | UNIT |
|-----|-----------------------------|--|-----|---------------------------|-----|------|
|     |                             | FAST MODE  |     | STD MODE                  |     |      |
|     |                             | MIN  | MAX | MIN                       | MAX |      |
| 1   | t <sub>su</sub> (CMDV-CLKH) | Setup time, SDx_CMD data input valid before SDx_CLK high |     | 3                         | 3   | ns   |
| 2   | t <sub>h</sub> (CLKH-CMDV)  | Hold time, SDx_CMD data input valid after SDx_CLK high   |     | 3                         | 3   | ns   |
| 3   | t <sub>su</sub> (DATV-CLKH) | Setup time, SD_Dx data input valid before SDx_CLK high   |     | 3                         | 3   | ns   |
| 4   | t <sub>h</sub> (CLKH-DATV)  | Hold time, SD_Dx data input valid after SDx_CLK high     |     | 3                         | 3   | ns   |

**Table 5-15. Switching Characteristics Over Recommended Operating Conditions for SD Output<sup>(1)</sup> (see Figure 5-16, Figure 5-17, Figure 5-18, and Figure 5-19)**

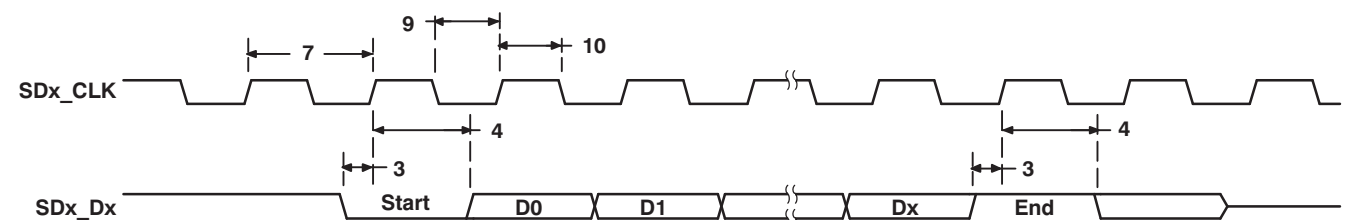
| NO. | PARAMETER                     | CV <sub>DD</sub> = 1.3 V                              |                   | CV <sub>DD</sub> = 1.05 V |                   | UNIT |
|-----|-------------------------------|---|-------------------|---------------------------|-------------------|------|
|     |                               | FAST MODE   |                   | STD MODE                  |                   |      |
|     |                               | MIN   | MAX               | MIN                       | MAX               |      |
| 7   | f <sub>(CLK)</sub>            | 0   | 50 <sup>(2)</sup> | 0                         | 25 <sup>(2)</sup> | MHz  |
| 8   | f <sub>(CLK_ID)</sub>         | 0   | 400               | 0                         | 400               | kHz  |
| 9   | t <sub>w</sub> (CLKL)         | Pulse width, SDx_CLK low                              |                   | 7                         | 10                | ns   |
| 10  | t <sub>w</sub> (CLKH)         | Pulse width, SDx_CLK high                             |                   | 7                         | 10                | ns   |
| 11  | t <sub>r</sub> (CLK)          | Rise time, SDx_CLK                                    |                   | 3                         | 3                 | ns   |
| 12  | t <sub>f</sub> (CLK)          | Fall time, SDx_CLK                                    |                   | 3                         | 3                 | ns   |
| 13  | t <sub>d</sub> (MDCLKL-CMDIV) | Delay time, SDx_CLK low to SD_CMD data output invalid |                   | -4                        | -4.1              | ns   |
| 14  | t <sub>d</sub> (MDCLKL-CMDV)  | Delay time, SDx_CLK low to SD_CMD data output valid   |                   | 4                         | 5.1               | ns   |
| 15  | t <sub>d</sub> (MDCLKL-DATIV) | Delay time, SDx_CLK low to SD_Dx data output invalid  |                   | -4                        | -4.1              | ns   |
| 16  | t <sub>d</sub> (MDCLKL-DATV)  | Delay time, SDx_CLK low to SD_Dx data output valid    |                   | 4                         | 5.1               | ns   |

(1) For SD, the parametric values are measured at DV<sub>DDIO</sub> = 3.3 V and 2.75 V.

(2) Use this value or SYS\_CLK/2 whichever is smaller.



**Figure 5-16. SD Host Command Write Timing**



**Figure 5-17. SD Card Response Timing**

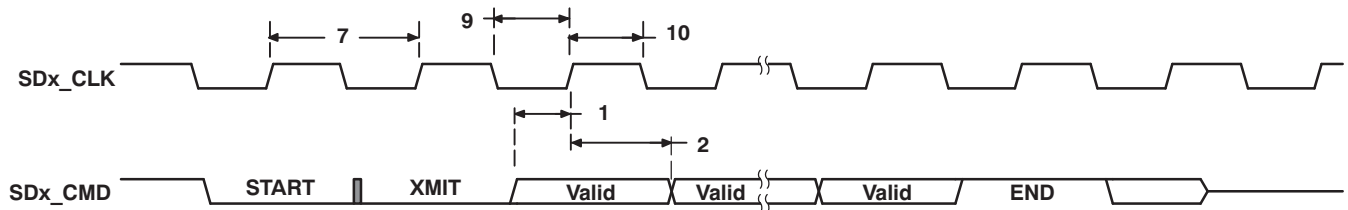


Figure 5-18. SD Host Write Timing

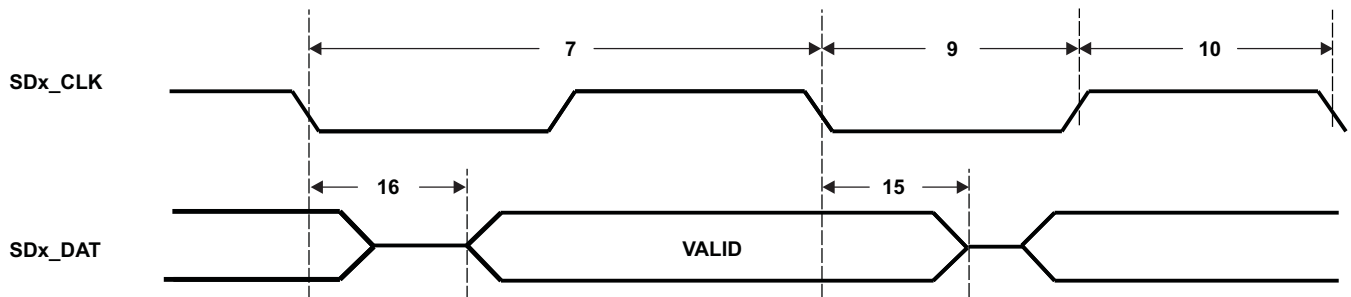


Figure 5-19. SD Data Write Timing

### 5.6.12 Real-Time Clock (RTC)

The device includes an RTC with its own separated power supply and isolation circuits. All RTC registers are preserved (except for RTC Control and RTC Update Registers) and the counter continues to operate when the device is powered off.

The RTC also has the capability to wake up the device from idle states through alarms and periodic interrupts.

---

#### NOTE

The RTC Core ( $CV_{DDRTC}$ ) must be properly powered by an external power source even though RTC is not used. None of the on-chip LDOs can power  $CV_{DDRTC}$ .

---

The device RTC provides the following features:

- 100-year calendar up to year 2099.
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Millisecond time correction
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 24-hour clock mode
- Second, minute, hour, day, or week alarm interrupt
- Periodic interrupt: every millisecond, second, minute, hour, or day
- Alarm interrupt: precise time of day
- Single interrupt to the DSP CPU
- 32.768-kHz crystal oscillator with frequency calibration

Control of the RTC is maintained through a set of I/O memory mapped registers (see [Table 5-16](#)). Any write to these registers will be synchronized to the RTC 32.768-kHz clock; the CPU must run at least 3X faster than the RTC. Writes to these registers will not be apparent until the next two 32.768-kHz clock cycles later. If the RTC oscillator is disabled, no RTC register can be written to.

The RTC has its own power-on-reset (POR) circuit that resets the registers in the RTC core domain when power is first applied to the  $CV_{DDRTC}$  power pin. The RTC flops are not reset by the device's  $\overline{\text{RESET}}$  pin nor the digital core's POR (powergood signal).

The scratch registers in the RTC can take advantage of this unique reset domain to keep track of when the DSP boots and whether the RTC time registers have already been initialized to the current clock time or whether the software must go into a routine to prompt the user to set the time and date.

### 5.6.12.1 RTC Peripheral Register Descriptions

Table 5-16 shows the RTC registers.

**Table 5-16. RTC Registers**

| HEX ADDRESS RANGE | ACRONYM   | REGISTER NAME                  |
|-------------------|-----------|--------------------------------|
| 1900h             | RTCINTEN  | RTC Interrupt Enable Register  |
| 1901h             | RTCUPDATE | RTC Update Register            |
| 1904h             | RTCMIL    | Milliseconds Register          |
| 1905h             | RTCMILA   | Milliseconds Alarm Register    |
| 1908h             | RTCSEC    | Seconds Register               |
| 1909h             | RTCSECA   | Seconds Alarm Register         |
| 190Ch             | RTCMIN    | Minutes Register               |
| 190Dh             | RTCMINA   | Minutes Alarm Register         |
| 1910h             | RTCHOUR   | Hours Register                 |
| 1911h             | RTCHOURA  | Hours Alarm Register           |
| 1914h             | RTCDAY    | Days Register                  |
| 1915h             | RTCDAYA   | Days Alarm Register            |
| 1918h             | RTCMONTH  | Months Register                |
| 1919h             | RTCMONTHA | Months Alarm Register          |
| 191Ch             | RTCYEAR   | Years Register                 |
| 191Dh             | RTCYEARA  | Years Alarm Register           |
| 1920h             | RTCINTFL  | RTC Interrupt Flag Register    |
| 1921h             | RTCNOPWR  | RTC Lost Power Status Register |
| 1924h             | RTCINTREG | RTC Interrupt Register         |
| 1928h             | RTCDRIFT  | RTC Compensation Register      |
| 192Ch             | RTCOSC    | RTC Oscillator Register        |
| 1930h             | RTCPMGT   | RTC Power Management Register  |
| 1960h             | RTCSCR1   | RTC LSW Scratch Register 1     |
| 1961h             | RTCSCR2   | RTC MSW Scratch Register 2     |
| 1964h             | RTCSCR3   | RTC LSW Scratch Register 3     |
| 1965h             | RTCSCR4   | RTC MSW Scratch Register 4     |

#### 5.6.12.1.1 RTC Electrical Data and Timing

For more detailed information on RTC electrical timings, see the [Section 5.6.9.3, Reset Electrical Data and Timing](#).

### 5.6.13 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between the device and other devices compliant with Philips Semiconductors Inter-IC bus (I<sup>2</sup>C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit and receive 2 to 8-bit data to and from the DSP through the I2C module. The I2C port does not support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Data Transfer Rate from 10 kbps to 400 kbps (Philips Fast-Mode Rate)
- Noise Filter to Remove Noise 50 ns or Less
- 7- and 10-Bit Device Addressing Modes
- Master (Transmit and Receive) and Slave (Transmit and Receive) Functionality
- One Read DMA Event and One Write DMA Event That the DMA Controller Can Use
- One Interrupt That the CPU Can Use
- Slew-Rate Limited Open-Drain Output Buffers

The I2C module clock must be in the range from 6.7 MHz to 13.3 MHz. With the I2C module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The I2C module clock is derived from the DSP clock divided by a programmable prescaler.

#### 5.6.13.1 I2C Peripheral Register Descriptions

Table 5-17 shows the I2C registers.

**Table 5-17. I2C Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME                            |
|-------------------|---------|--|
| 1A00h             | ICOAR   | I2C Own Address Register                 |
| 1A04h             | ICIMR   | I2C Interrupt Mask Register              |
| 1A08h             | ICSTR   | I2C Interrupt Status Register            |
| 1A0Ch             | ICCLKL  | I2C Clock Low-Time Divider Register      |
| 1A10h             | ICCLKH  | I2C Clock High-Time Divider Register     |
| 1A14h             | ICCNT   | I2C Data Count Register                  |
| 1A18h             | ICDRR   | I2C Data Receive Register                |
| 1A1Ch             | ICSAR   | I2C Slave Address Register               |
| 1A20h             | ICDXR   | I2C Data Transmit Register               |
| 1A24h             | ICMDR   | I2C Mode Register                        |
| 1A28h             | ICIVR   | I2C Interrupt Vector Register            |
| 1A2Ch             | ICEMDR  | I2C Extended Mode Register               |
| 1A30h             | ICPSC   | I2C Prescaler Register                   |
| 1A34h             | ICPID1  | I2C Peripheral Identification Register 1 |
| 1A38h             | ICPID2  | I2C Peripheral Identification Register 2 |

5.6.13.2 I2C Electrical Data and Timing

Table 5-18 and Table 5-19 list the timing and switching requirements for I2C, respectively.

Table 5-18. Timing Requirements for I2C Timings<sup>(1)</sup> (see Figure 5-20)

| NO. |                               |   | CV <sub>DD</sub> = 1.05 V, CV <sub>DD</sub> = 1.3 V |      |                                       |                    | UNIT |
|-----|-------------------------------|---|---|------|---------------------------------------|--------------------|------|
|     |                               |   | STANDARD MODE                                       |      | FAST MODE                             |                    |      |
|     |                               |   | MIN   | MAX  | MIN                                   | MAX                |      |
| 1   | t <sub>c(SCL)</sub>           | Cycle time, SCL   | 10  |      | 2.5                                   |                    | μs   |
| 2   | t <sub>su(SCLH-SDAL)</sub>    | Setup time, SCL high before SDA low (for a repeated START condition)          | 4.7   |      | 0.6                                   |                    | μs   |
| 3   | t <sub>h(SCLL-SDAL)</sub>     | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4   |      | 0.6                                   |                    | μs   |
| 4   | t <sub>w(SCLL)</sub>          | Pulse duration, SCL low   | 4.7   |      | 1.3                                   |                    | μs   |
| 5   | t <sub>w(SCLH)</sub>          | Pulse duration, SCL high  | 4   |      | 0.6                                   |                    | μs   |
| 6   | t <sub>su(SDAV-SCLH)</sub>    | Setup time, SDA valid before SCL high   | 250   |      | 100 <sup>(2)</sup>                    |                    | ns   |
| 7   | t <sub>h(SDA-SCLL)</sub>      | Hold time, SDA valid after SCL low  | 0 <sup>(3)</sup>                                    |      | 0 <sup>(3)</sup>                      | 0.9 <sup>(4)</sup> | μs   |
| 8   | t <sub>w(SDAH)</sub>          | Pulse duration, SDA high between STOP and START conditions                    | 4.7   |      | 1.3                                   |                    | μs   |
| 9   | t <sub>r(SDA)</sub>           | Rise time, SDA <sup>(5)</sup>   |   | 1000 | 20 + 0.1C <sub>b</sub> <sup>(6)</sup> | 300                | ns   |
| 10  | t <sub>r(SCL)</sub>           | Rise time, SCL <sup>(5)</sup>   |   | 1000 | 20 + 0.1C <sub>b</sub> <sup>(6)</sup> | 300                | ns   |
| 11  | t <sub>f(SDA)</sub>           | Fall time, SDA <sup>(5)</sup>   |   | 300  | 20 + 0.1C <sub>b</sub> <sup>(6)</sup> | 300                | ns   |
| 12  | t <sub>f(SCL)</sub>           | Fall time, SCL <sup>(5)</sup>   |   | 300  | 20 + 0.1C <sub>b</sub> <sup>(6)</sup> | 300                | ns   |
| 13  | t <sub>su(SCLH-SDAH)</sub>    | Setup time, SCL high before SDA high (for STOP condition)                     | 4   |      | 0.6                                   |                    | μs   |
| 14  | t <sub>w(SP)</sub>            | Pulse duration, spike (must be suppressed)                                    |   |      | 0                                     | 50                 | ns   |
| 15  | C <sub>b</sub> <sup>(6)</sup> | Capacitive load for each bus line   |   | 400  |                                       | 400                | pF   |

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Also these pins are not 3.6 V-tolerant (their V<sub>IH</sub> cannot go above DV<sub>DDIO</sub> + 0.3 V).
- (2) A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>su(SDA-SCLH)</sub> ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r</sub> max + t<sub>su(SDA-SCLH)</sub> = 1000 + 250 = 1250 ns (according to the Standard-mode I<sup>2</sup>C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IHmin</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum t<sub>h(SDA-SCLL)</sub> only has to be met if the device does not stretch the low period [t<sub>w(SCLL)</sub>] of the SCL signal.
- (5) The rise and fall times are measured at 30% and 70% of DV<sub>DDIO</sub>. The fall time is only slightly influenced by the external bus load (C<sub>b</sub>) and external pullup resistor. The rise time (t<sub>r</sub>) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.
- (6) C<sub>b</sub> = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

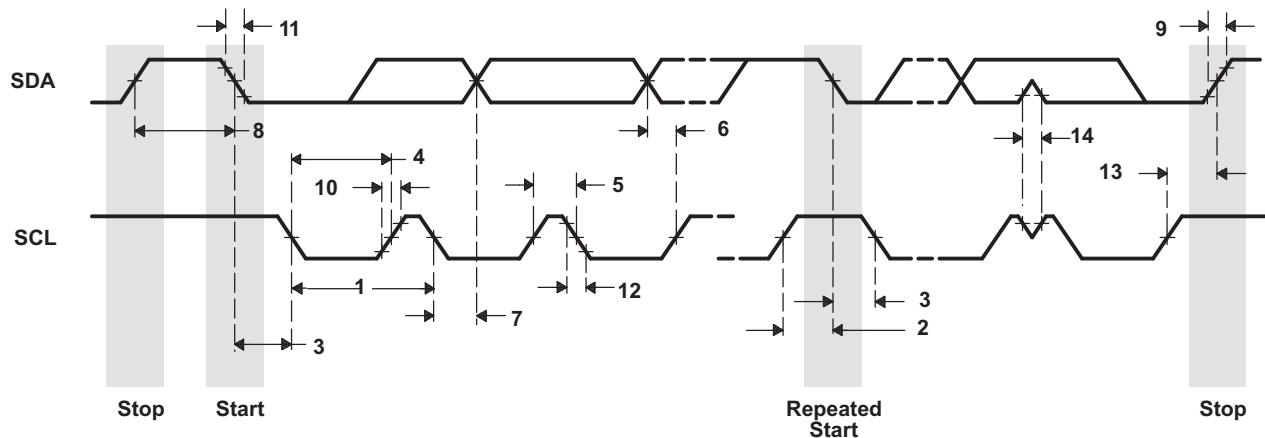


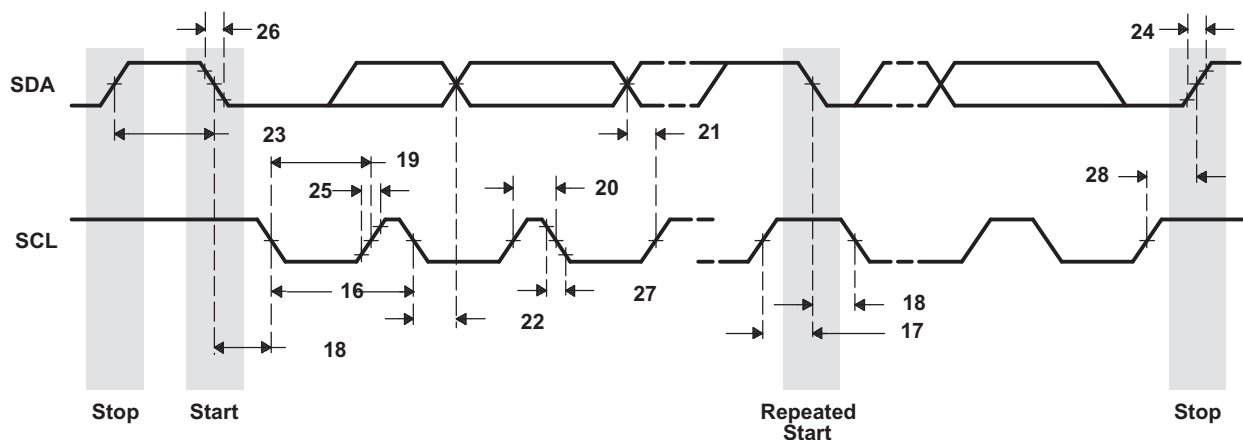
Figure 5-20. I2C Receive Timings

**Table 5-19. Switching Characteristics for I2C Timings<sup>(1)</sup> (see Figure 5-21)**

| NO. | PARAMETER  | $CV_{DD} = 1.05\text{ V}, CV_{DD} = 1.3\text{ V}$ |      |                              |     | UNIT          |
|-----|--|---|------|------------------------------|-----|---------------|
|     |  | STANDARD MODE                                     |      | FAST MODE                    |     |               |
|     |  | MIN   | MAX  | MIN                          | MAX |               |
| 16  | $t_{c(SCL)}$ Cycle time, SCL   | 10  |      | 2.5                          |     | $\mu\text{s}$ |
| 17  | $t_{d(SCLH-SDAL)}$ Delay time, SCL high to SDA low (for a repeated START condition)            | 4.7   |      | 0.6                          |     | $\mu\text{s}$ |
| 18  | $t_{d(SDAL-SCLL)}$ Delay time, SDA low to SCL low (for a START and a repeated START condition) | 4   |      | 0.6                          |     | $\mu\text{s}$ |
| 19  | $t_{w(SCLL)}$ Pulse duration, SCL low  | 4.7   |      | 1.3                          |     | $\mu\text{s}$ |
| 20  | $t_{w(SCLH)}$ Pulse duration, SCL high   | 4   |      | 0.6                          |     | $\mu\text{s}$ |
| 21  | $t_{d(SDAV-SCLH)}$ Delay time, SDA valid to SCL high   | 250   |      | 100                          |     | ns            |
| 22  | $t_{v(SCLL-SDAV)}$ Valid time, SDA valid after SCL low   | 0   |      | 0                            | 0.9 | $\mu\text{s}$ |
| 23  | $t_{w(SDAH)}$ Pulse duration, SDA high between STOP and START conditions                       | 4.7   |      | 1.3                          |     | $\mu\text{s}$ |
| 24  | $t_{r(SDA)}$ Rise time, SDA <sup>(2)</sup>   |   | 1000 | $20 + 0.1C_b$ <sup>(1)</sup> | 300 | ns            |
| 25  | $t_{r(SCL)}$ Rise time, SCL <sup>(2)</sup>   |   | 1000 | $20 + 0.1C_b$ <sup>(1)</sup> | 300 | ns            |
| 26  | $t_{f(SDA)}$ Fall time, SDA <sup>(2)</sup>   |   | 300  | $20 + 0.1C_b$ <sup>(1)</sup> | 300 | ns            |
| 27  | $t_{f(SCL)}$ Fall time, SCL <sup>(2)</sup>   |   | 300  | $20 + 0.1C_b$ <sup>(1)</sup> | 300 | ns            |
| 28  | $t_{d(SCLH-SDAH)}$ Delay time, SCL high to SDA high (for STOP condition)                       | 4   |      | 0.6                          |     | $\mu\text{s}$ |
| 29  | $C_p$ Capacitance for each I2C pin   |   | 10   |                              | 10  | pF            |

(1)  $C_b$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

(2) The rise and fall times are measured at 30% and 70% of  $DV_{DDIO}$ . The fall time is only slightly influenced by the external bus load ( $C_b$ ) and external pullup resistor. The rise time ( $t_r$ ) is determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.


**Figure 5-21. I2C Transmit Timings**



### 5.6.14 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from an external peripheral device and parallel-to-serial conversions on data transmitted to an external peripheral device through a serial bus.

The device has one UART peripheral with the following features:

- Programmable baud rates (frequency prescale values from 1 to 65535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals

#### 5.6.14.1 UART Peripheral Register Descriptions

[Table 5-20](#) shows the UART registers.

**Table 5-20. UART Registers**

| HEX ADDRESS RANGE | ACRONYM     | REGISTER NAME                                 |
|-------------------|-------------|---|
| 1B00h             | RBR         | Receiver Buffer Register (read only)          |
| 1B00h             | THR         | Transmitter Holding Register (write only)     |
| 1B02h             | IER         | Interrupt Enable Register                     |
| 1B04h             | IIR         | Interrupt Identification Register (read only) |
| 1B04h             | FCR         | FIFO Control Register (write only)            |
| 1B06h             | LCR         | Line Control Register                         |
| 1B08h             | MCR         | Modem Control Register                        |
| 1B0Ah             | LSR         | Line Status Register                          |
| 1B0Ch             | MSR         | Modem Status Register                         |
| 1B0Eh             | SCR         | Scratch Register                              |
| 1B10h             | DLL         | Divisor LSB Latch                             |
| 1B12h             | DLH         | Divisor MSB Latch                             |
| 1B18h             | PWREMU_MGMT | Power and Emulation Management Register       |

### 5.6.14.2 UART Electrical Data and Timing [Receive and Transmit]

Table 5-21 and Table 5-22 list the timing and switching requirements of UART, respectively.

**Table 5-21. Timing Requirements for UART Receive<sup>(1)</sup> <sup>(2)</sup> (see Figure 5-22)**

| NO. |                       |  | CV <sub>DD</sub> = 1.05 V |       | CV <sub>DD</sub> = 1.3 V |       | UNIT |
|-----|-----------------------|--|---------------------------|-------|--------------------------|-------|------|
|     |                       |  | MIN                       | MAX   | MIN                      | MAX   |      |
| 4   | t <sub>w(URXDB)</sub> | Pulse duration, receive data bit (UART_RXD) [15/30 pF] | U - 3.5                   | U + 3 | U - 3.5                  | U + 3 | ns   |
| 5   | t <sub>w(URXSB)</sub> | Pulse duration, receive start bit [15/30 pF]           | U - 3.5                   | U + 3 | U - 3.5                  | U + 3 | ns   |

(1) U = UART baud time = 1/programmed baud rate.

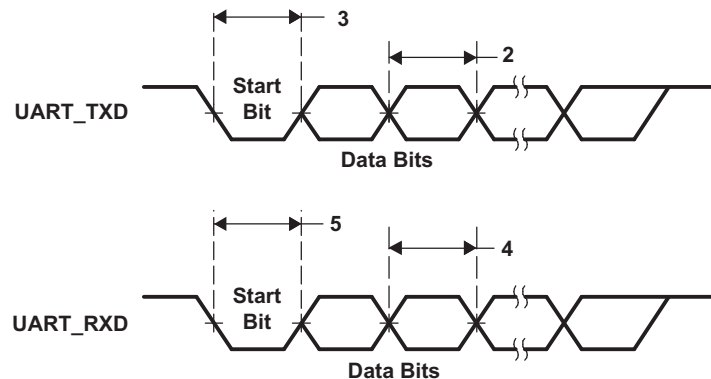
(2) Based on a maximum CPU frequency of 60 MHz.

**Table 5-22. Switching Characteristics Over Recommended Operating Conditions for UART Transmit<sup>(1)</sup> <sup>(2)</sup> (see Figure 5-22)**

| NO. | PARAMETER             | CV <sub>DD</sub> = 1.05 V                               |     | CV <sub>DD</sub> = 1.3 V |       | UNIT |
|-----|-----------------------|---|-----|--------------------------|-------|------|
|     |                       | MIN   | MAX | MIN                      | MAX   |      |
| 1   | f <sub>(baud)</sub>   | Maximum programmable bit rate                           |     | 3.75                     | 6.25  | MHz  |
| 2   | t <sub>w(UTXDB)</sub> | Pulse duration, transmit data bit (UART_TXD) [15/30 pF] |     | U - 3.5                  | U + 4 | ns   |
| 3   | t <sub>w(UTXSB)</sub> | Pulse duration, transmit start bit [15/30 pF]           |     | U - 3.5                  | U + 4 | ns   |

(1) U = UART baud time = 1/programmed baud rate.

(2) Based on a maximum CPU frequency of 60 MHz.



**Figure 5-22. UART Transmit and Receive Timing**

### 5.6.15 Inter-IC Sound (I2S)

The device I2S peripherals allow serial transfer of full-duplex streaming data, usually audio data, between the device and an external I2S peripheral device such as an audio codec.

The device supports four independent dual-channel I2S peripherals, each with the following features:

- Full-duplex (transmit and receive) dual-channel communication
- Double-buffered data registers that allow for continuous data streaming
- I2S/Left-justified and DSP data format with a data delay of 1 or 2 bits
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
- Ability to sign-extend received data samples for easy use in signal processing algorithms
- Programmable polarity for both frame synchronization and bit clocks
- Stereo (in I2S/Left-justified or DSP data formats) or mono (in DSP data format) mode
- Detection of overrun, underrun, and frame-sync error conditions

#### 5.6.15.1 I2S Peripheral Register Descriptions

Table 5-23, Table 5-24, Table 5-25, and Table 5-26 list the I2S0, I2S1, I2S2, and I2S3 registers, respectively.

**Table 5-23. I2S0 Registers**

| HEX ADDRESS RANGE | ACRONYM     | REGISTER NAME                       |
|-------------------|-------------|-------------------------------------|
| 2800h             | I2S0CTRL    | I2S0 Serializer Control Register    |
| 2804h             | I2S0SRATE   | I2S0 Sample Rate Generator Register |
| 2808h             | I2S0TXLT0   | I2S0 Transmit Left Data 0 Register  |
| 2809h             | I2S0TXLT1   | I2S0 Transmit Left Data 1 Register  |
| 280Ch             | I2S0TXRT0   | I2S0 Transmit Right Data 0 Register |
| 280Dh             | I2S0TXRT1   | I2S0 Transmit Right Data 1 Register |
| 2810h             | I2S0INTFL   | I2S0 Interrupt Flag Register        |
| 2814h             | I2S0INTMASK | I2S0 Interrupt Mask Register        |
| 2828h             | I2S0RXLT0   | I2S0 Receive Left Data 0 Register   |
| 2829h             | I2S0RXLT1   | I2S0 Receive Left Data 1 Register   |
| 282Ch             | I2S0RXRT0   | I2S0 Receive Right Data 0 Register  |
| 282Dh             | I2S0RXRT1   | I2S0 Receive Right Data 1 Register  |

**Table 5-24. I2S1 Registers**

| HEX ADDRESS RANGE | ACRONYM     | REGISTER NAME                       |
|-------------------|-------------|-------------------------------------|
| 2900h             | I2S1CTRL    | I2S1 Serializer Control Register    |
| 2904h             | I2S1SRATE   | I2S1 Sample Rate Generator Register |
| 2908h             | I2S1TXLT0   | I2S1 Transmit Left Data 0 Register  |
| 2909h             | I2S1TXLT1   | I2S1 Transmit Left Data 1 Register  |
| 290Ch             | I2S1TXRT0   | I2S1 Transmit Right Data 0 Register |
| 290Dh             | I2S1TXRT1   | I2S1 Transmit Right Data 1 Register |
| 2910h             | I2S1INTFL   | I2S1 Interrupt Flag Register        |
| 2914h             | I2S1INTMASK | I2S1 Interrupt Mask Register        |
| 2928h             | I2S1RXLT0   | I2S1 Receive Left Data 0 Register   |
| 2929h             | I2S1RXLT1   | I2S1 Receive Left Data 1 Register   |
| 292Ch             | I2S1RXRT0   | I2S1 Receive Right Data 0 Register  |
| 292Dh             | I2S1RXRT1   | I2S1 Receive Right Data 1 Register  |

**Table 5-25. I2S2 Registers**

| HEX ADDRESS RANGE | ACRONYM     | REGISTER NAME                       |
|-------------------|-------------|-------------------------------------|
| 2A00h             | I2S2SCTRL   | I2S2 Serializer Control Register    |
| 2A04h             | I2S2SRATE   | I2S2 Sample Rate Generator Register |
| 2A08h             | I2S2TXLT0   | I2S2 Transmit Left Data 0 Register  |
| 2A09h             | I2S2TXLT1   | I2S2 Transmit Left Data 1 Register  |
| 2A0Ch             | I2S2TXRT0   | I2S2 Transmit Right Data 0 Register |
| 2A0Dh             | I2S2TXRT1   | I2S2 Transmit Right Data 1 Register |
| 2A10h             | I2S2INTFL   | I2S2 Interrupt Flag Register        |
| 2A14h             | I2S2INTMASK | I2S2 Interrupt Mask Register        |
| 2A28h             | I2S2RXLT0   | I2S2 Receive Left Data 0 Register   |
| 2A29h             | I2S2RXLT1   | I2S2 Receive Left Data 1 Register   |
| 2A2Ch             | I2S2RXRT0   | I2S2 Receive Right Data 0 Register  |
| 2A2Dh             | I2S2RXRT1   | I2S2 Receive Right Data 1 Register  |

**Table 5-26. I2S3 Registers**

| HEX ADDRESS RANGE | ACRONYM     | REGISTER NAME                       |
|-------------------|-------------|-------------------------------------|
| 2B00h             | I2S3SCTRL   | I2S3 Serializer Control Register    |
| 2B04h             | I2S3SRATE   | I2S3 Sample Rate Generator Register |
| 2B08h             | I2S3TXLT0   | I2S3 Transmit Left Data 0 Register  |
| 2B09h             | I2S3TXLT1   | I2S3 Transmit Left Data 1 Register  |
| 2B0Ch             | I2S3TXRT0   | I2S3 Transmit Right Data 0 Register |
| 2B0Dh             | I2S3TXRT1   | I2S3 Transmit Right Data 1 Register |
| 2B10h             | I2S3INTFL   | I2S3 Interrupt Flag Register        |
| 2B14h             | I2S3INTMASK | I2S3 Interrupt Mask Register        |
| 2B28h             | I2S3RXLT0   | I2S3 Receive Left Data 0 Register   |
| 2B29h             | I2S3RXLT1   | I2S3 Receive Left Data 1 Register   |
| 2B2Ch             | I2S3RXRT0   | I2S3 Receive Right Data 0 Register  |
| 2B2Dh             | I2S3RXRT1   | I2S3 Receive Right Data 1 Register  |

### 5.6.15.2 I2S Electrical Data and Timing

Table 5-27, Table 5-28, Table 5-29, and Table 5-30 list the timing and switching requirements for I2S.

**Table 5-27. Timing Requirements for I2S [I/O = 3.3 V, 2.75 V, and 2.5 V]<sup>(1)</sup> (see Figure 5-23)**

| NO. |                            |   | MASTER                      |     |                             |     | SLAVE                                      |     |  |     | UNIT |
|-----|----------------------------|---|-----------------------------|-----|-----------------------------|-----|--|-----|--|-----|------|
|     |                            |   | CV <sub>DD</sub> = 1.05 V   |     | CV <sub>DD</sub> = 1.3 V    |     | CV <sub>DD</sub> = 1.05 V                  |     | CV <sub>DD</sub> = 1.3 V                   |     |      |
|     |                            |   | MIN                         | MAX | MIN                         | MAX | MIN  | MAX | MIN  | MAX |      |
| 1   | t <sub>c</sub> (CLK)       | Cycle time, I2S_CLK                                       | 40 or 2P <sup>(1)</sup> (2) |     | 40 or 2P <sup>(1)</sup> (2) |     | 40 or 2P <sup>(1)</sup> (2)                |     | 40 or 2P <sup>(1)</sup> (2)                |     | ns   |
| 2   | t <sub>w</sub> (CLKH)      | Pulse duration, I2S_CLK high                              | 20                          |     | 20                          |     | 20   |     | 20   |     | ns   |
| 3   | t <sub>w</sub> (CLKL)      | Pulse duration, I2S_CLK low                               | 20                          |     | 20                          |     | 20   |     | 20   |     | ns   |
| 7   | t <sub>su</sub> (RXV-CLKH) | Setup time, I2S_RX valid before I2S_CLK high (CLKPOL = 0) | 5                           |     | 5                           |     | 5  |     | 5  |     | ns   |
|     | t <sub>su</sub> (RXV-CLKL) | Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)  | 5                           |     | 5                           |     | 5  |     | 5  |     | ns   |
| 8   | t <sub>h</sub> (CLKH-RXV)  | Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)   | 3                           |     | 3                           |     | 3  |     | 3  |     | ns   |
|     | t <sub>h</sub> (CLKL-RXV)  | Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)    | 3                           |     | 3                           |     | 3  |     | 3  |     | ns   |
| 9   | t <sub>su</sub> (FSV-CLKH) | Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0) | –                           |     | –                           |     | 15   |     | 15   |     | ns   |
|     | t <sub>su</sub> (FSV-CLKL) | Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)  | –                           |     | –                           |     | 15   |     | 15   |     | ns   |
| 10  | t <sub>h</sub> (CLKH-FSV)  | Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)   | –                           |     | –                           |     | t <sub>w</sub> (CLKH) + 0.6 <sup>(3)</sup> |     | t <sub>w</sub> (CLKH) + 0.6 <sup>(3)</sup> |     | ns   |
|     | t <sub>h</sub> (CLKL-FSV)  | Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)    | –                           |     | –                           |     | t <sub>w</sub> (CLKL) + 0.6 <sup>(3)</sup> |     | t <sub>w</sub> (CLKL) + 0.6 <sup>(3)</sup> |     | ns   |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use the greater value.

(3) In slave mode, I2S\_FS must be latched on both edges of I2S input clock (I2S\_CLK).

**Table 5-28. Timing Requirements for I2S [I/O = 1.8 V]<sup>(1)</sup> (see Figure 5-23)**

| NO. |                            | MASTER  |     |                             |     | SLAVE                       |     |  |     | UNIT                                       |  |    |
|-----|----------------------------|---|-----|-----------------------------|-----|-----------------------------|-----|--|-----|--|--|----|
|     |                            | CV <sub>DD</sub> = 1.05 V                                 |     | CV <sub>DD</sub> = 1.3 V    |     | CV <sub>DD</sub> = 1.05 V   |     | CV <sub>DD</sub> = 1.3 V                   |     |  |  |    |
|     |                            | MIN   | MAX | MIN                         | MAX | MIN                         | MAX | MIN  | MAX |  |  |    |
| 1   | t <sub>c</sub> (CLK)       | Cycle time, I2S_CLK                                       |     | 50 or 2P <sup>(1)</sup> (2) |     | 40 or 2P <sup>(1)</sup> (2) |     | 50 or 2P <sup>(1)</sup> (2)                |     | 40 or 2P <sup>(1)</sup> (2)                |  | ns |
| 2   | t <sub>w</sub> (CLKH)      | Pulse duration, I2S_CLK high                              |     | 25                          |     | 20                          |     | 25   |     | 20   |  | ns |
| 3   | t <sub>w</sub> (CLKL)      | Pulse duration, I2S_CLK low                               |     | 25                          |     | 20                          |     | 25   |     | 20   |  | ns |
| 7   | t <sub>su</sub> (RXV-CLKH) | Setup time, I2S_RX valid before I2S_CLK high (CLKPOL = 0) |     | 5                           |     | 5                           |     | 5  |     | 5  |  | ns |
|     | t <sub>su</sub> (RXV-CLKL) | Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)  |     | 5                           |     | 5                           |     | 5  |     | 5  |  | ns |
| 8   | t <sub>h</sub> (CLKH-RXV)  | Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)   |     | 3                           |     | 3                           |     | 3  |     | 3  |  | ns |
|     | t <sub>h</sub> (CLKL-RXV)  | Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)    |     | 3                           |     | 3                           |     | 3  |     | 3  |  | ns |
| 9   | t <sub>su</sub> (FSV-CLKH) | Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0) |     | –                           |     | –                           |     | 15   |     | 15   |  | ns |
|     | t <sub>su</sub> (FSV-CLKL) | Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)  |     | –                           |     | –                           |     | 15   |     | 15   |  | ns |
| 10  | t <sub>h</sub> (CLKH-FSV)  | Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)   |     | –                           |     | –                           |     | t <sub>w</sub> (CLKH) + 0.6 <sup>(3)</sup> |     | t <sub>w</sub> (CLKH) + 0.6 <sup>(3)</sup> |  | ns |
|     | t <sub>h</sub> (CLKL-FSV)  | Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)    |     | –                           |     | –                           |     | t <sub>w</sub> (CLKL) + 0.6 <sup>(3)</sup> |     | t <sub>w</sub> (CLKL) + 0.6 <sup>(3)</sup> |  | ns |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use the greater value.

(3) In slave mode, I2S\_FS is required to be latched on both edges of I2S input clock (I2S\_CLK).

**Table 5-29. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 3.3 V, 2.75 V, or 2.5 V] (see Figure 5-23)**

| NO. | PARAMETER                    |  | MASTER                      |     |                             |     | SLAVE                       |     |                             |     | UNIT |
|-----|------------------------------|--|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|------|
|     |                              |  | CV <sub>DD</sub> = 1.05 V   |     | CV <sub>DD</sub> = 1.3 V    |     | CV <sub>DD</sub> = 1.05 V   |     | CV <sub>DD</sub> = 1.3 V    |     |      |
|     |                              |  | MIN                         | MAX | MIN                         | MAX | MIN                         | MAX | MIN                         | MAX |      |
| 1   | t <sub>c</sub> (CLK)         | Cycle time, I2S_CLK  | 40 or 2P <sup>(1) (2)</sup> |     | 40 or 2P <sup>(1) (2)</sup> |     | 40 or 2P <sup>(1) (2)</sup> |     | 40 or 2P <sup>(1) (2)</sup> |     | ns   |
| 2   | t <sub>w</sub> (CLKH)        | Pulse duration, I2S_CLK high (CLKPOL = 0)                    | 20                          |     | 20                          |     | 20                          |     | 20                          |     | ns   |
|     | t <sub>w</sub> (CLKL)        | Pulse duration, I2S_CLK low (CLKPOL = 1)                     | 20                          |     | 20                          |     | 20                          |     | 20                          |     | ns   |
| 3   | t <sub>w</sub> (CLKL)        | Pulse duration, I2S_CLK low (CLKPOL = 0)                     | 20                          |     | 20                          |     | 20                          |     | 20                          |     | ns   |
|     | t <sub>w</sub> (CLKH)        | Pulse duration, I2S_CLK high (CLKPOL = 1)                    | 20                          |     | 20                          |     | 20                          |     | 20                          |     | ns   |
| 4   | t <sub>dmax</sub> (CLKL-DXV) | Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)  | 0                           | 15  | 0                           | 14  | 0                           | 15  | 0                           | 15  | ns   |
|     | t <sub>dmax</sub> (CLKH-DXV) | Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1) | 0                           | 15  | 0                           | 14  | 0                           | 15  | 0                           | 15  | ns   |
| 5   | t <sub>dmax</sub> (CLKL-FSV) | Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)         | -1.1                        | 14  | -1.1                        | 14  | -                           | -   | -                           | -   | ns   |
|     | t <sub>dmax</sub> (CLKH-FSV) | Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)        | -1.1                        | 14  | -1.1                        | 14  | -                           | -   | -                           | -   | ns   |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.  
 (2) Use the greater value.

**Table 5-30. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 1.8 V] (see Figure 5-23)**

| NO. | PARAMETER  | MASTER                         |     |                                |     | SLAVE                          |     |                                |      | UNIT |
|-----|--|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|--------------------------------|------|------|
|     |  | CV <sub>DD</sub> = 1.05 V      |     | CV <sub>DD</sub> = 1.3 V       |     | CV <sub>DD</sub> = 1.05 V      |     | CV <sub>DD</sub> = 1.3 V       |      |      |
|     |  | MIN                            | MAX | MIN                            | MAX | MIN                            | MAX | MIN                            | MAX  |      |
| 1   | t <sub>c(CLK)</sub> Cycle time, I2S_CLK  | 50 or<br>2P <sup>(1) (2)</sup> |     | 40 or<br>2P <sup>(1) (2)</sup> |     | 50 or<br>2P <sup>(1) (2)</sup> |     | 40 or<br>2P <sup>(1) (2)</sup> |      | ns   |
| 2   | t <sub>w(CLKH)</sub> Pulse duration, I2S_CLK high (CLKPOL = 0)                           | 25                             |     | 20                             |     | 25                             |     | 20                             |      | ns   |
|     | t <sub>w(CLKL)</sub> Pulse duration, I2S_CLK low (CLKPOL = 1)                            | 25                             |     | 20                             |     | 25                             |     | 20                             |      | ns   |
| 3   | t <sub>w(CLKL)</sub> Pulse duration, I2S_CLK low (CLKPOL = 0)                            | 25                             |     | 20                             |     | 25                             |     | 20                             |      | ns   |
|     | t <sub>w(CLKH)</sub> Pulse duration, I2S_CLK high (CLKPOL = 1)                           | 25                             |     | 20                             |     | 25                             |     | 20                             |      | ns   |
| 4   | t <sub>dmax(CLKL-DXV)</sub> Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)  | 0                              | 19  | 0                              | 14  | 0                              | 19  | 0                              | 16.5 | ns   |
|     | t <sub>dmax(CLKH-DXV)</sub> Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1) | 0                              | 19  | 0                              | 14  | 0                              | 19  | 0                              | 16.5 | ns   |
| 5   | t <sub>dmax(CLKL-FSV)</sub> Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)         | -1.1                           | 14  | -1.1                           | 14  | -                              | -   | -                              | -    | ns   |
|     | t <sub>dmax(CLKH-FSV)</sub> Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)        | -1.1                           | 14  | -1.1                           | 14  | -                              | -   | -                              | -    | ns   |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use the greater value.



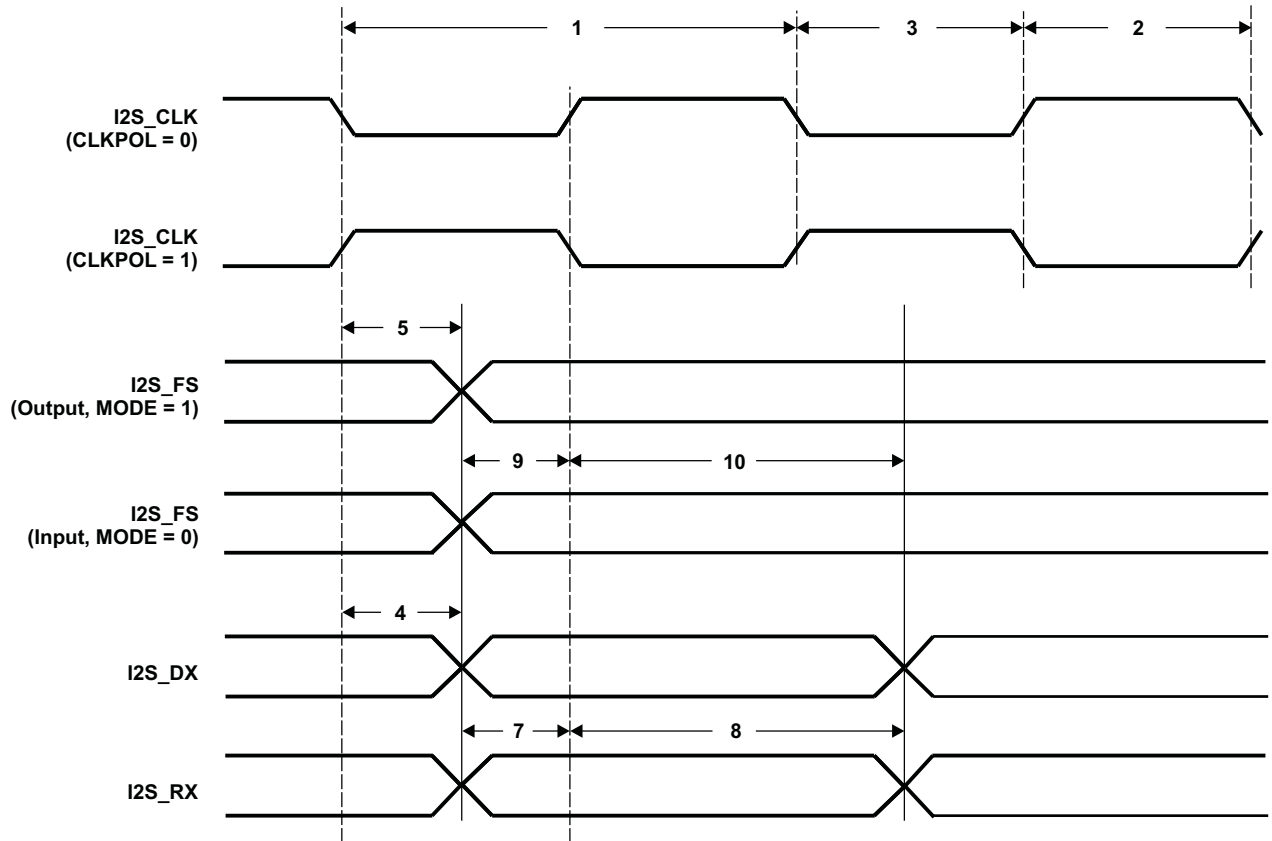


Figure 5-23. I2S Input and Output Timings

### 5.6.16 Liquid Crystal Display Controller (LCDC)

The device includes a LCD interface display driver (LIDD) controller.

The LIDD controller supports the asynchronous LCD interface and has the following features:

- Provides full-timing programmability of control signals and output data

#### NOTE

Raster mode is not supported on this device.

The LCD controller generates the correct external timing. The DMA engine provides a constant flow of data from the frame buffer to the external LCD panel through the LIDD controller. CPU access is provided to read and write registers.

#### 5.6.16.1 LCDC Peripheral Register Descriptions

Table 5-31 lists the LCDC peripheral registers.

**Table 5-31. LCD Controller Registers**

| CPU WORD ADDRESS | ACRONYM           | REGISTER DESCRIPTION                              |
|------------------|-------------------|---|
| 2E00h            | LCDREVMIN         | LCD Minor Revision Register                       |
| 2E01h            | LCDREVMAJ         | LCD Major Revision Register                       |
| 2E04h            | LCDCR             | LCD Control Register                              |
| 2E08h            | LCDSR             | LCD Status Register                               |
| 2E0Ch            | LCDLIDDCR         | LCD LIDD Control Register                         |
| 2E10h            | LCDLIDDCS0CONFIG0 | LCD LIDD CS0 Configuration Register 0             |
| 2E11h            | LCDLIDDCS0CONFIG1 | LCD LIDD CS0 Configuration Register 1             |
| 2E14h            | LCDLIDDCS0ADDR    | LCD LIDD CS0 Address Read and Write Register      |
| 2E18h            | LCDLIDDCS0DATA    | LCD LIDD CS0 Data Read and Write Register         |
| 2E1Ch            | LCDLIDDCS1CONFIG0 | LCD LIDD CS1 Configuration Register 0             |
| 2E1Dh            | LCDLIDDCS1CONFIG1 | LCD LIDD CS1 Configuration Register 1             |
| 2E20h            | LCDLIDDCS1ADDR    | LCD LIDD CS1 Address Read and Write Register      |
| 2E24h            | LCDLIDDCS1DATA    | LCD LIDD CS1 Data Read and Write Register         |
| 2E28h to 2E3Ah   | —                 | Reserved  |
| 2E40h            | LCDDMACR          | LCD DMA Control Register                          |
| 2E44h            | LCDDMAFB0BAR0     | LCD DMA Frame Buffer 0 Base Address Register 0    |
| 2E45h            | LCDDMAFB0BAR1     | LCD DMA Frame Buffer 0 Base Address Register 1    |
| 2E48h            | LCDDMAFB0CAR0     | LCD DMA Frame Buffer 0 Ceiling Address Register 0 |
| 2E49h            | LCDDMAFB0CAR1     | LCD DMA Frame Buffer 0 Ceiling Address Register 1 |
| 2E4Ch            | LCDDMAFB1BAR0     | LCD DMA Frame Buffer 1 Base Address Register 0    |
| 2E4Dh            | LCDDMAFB1BAR1     | LCD DMA Frame Buffer 1 Base Address Register 1    |
| 2E50h            | LCDDMAFB1CAR0     | LCD DMA Frame Buffer 1 Ceiling Address Register 0 |
| 2E51h            | LCDDMAFB1CAR1     | LCD DMA Frame Buffer 1 Ceiling Address Register 1 |

### 5.6.16.2 LCDC Electrical Data and Timing

Table 5-32 and Table 5-33 list the timing and switching requirements for LCDC, respectively.

**Table 5-32. Timing Requirements for LCD LIDD Mode<sup>(1)</sup> (see Figure 5-24, Figure 5-25, Figure 5-26, Figure 5-27, Figure 5-28, Figure 5-29, Figure 5-30, and Figure 5-31)**

| NO. |                            |  | CV <sub>DD</sub> = 1.05 V |     | CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|----------------------------|--|---------------------------|-----|--------------------------|-----|------|
|     |                            |  | MIN                       | MAX | MIN                      | MAX |      |
| 16  | t <sub>su(LCD_D-CLK)</sub> | Setup time, LCD_D[15:0] valid before LCD_CLK rising edge | 27                        |     | 42                       |     | ns   |
| 17  | t <sub>h(CLK-LCD_D)</sub>  | Hold time, LCD_D[15:0] valid after LCD_CLK rising edge   | 0                         |     | 0                        |     | ns   |

(1) Over operating free-air temperature range (unless otherwise noted)

**Table 5-33. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode (see Figure 5-24, Figure 5-25, Figure 5-26, Figure 5-27, Figure 5-28, Figure 5-29, Figure 5-30, and Figure 5-31)**

| NO. | PARAMETER                  |   | CV <sub>DD</sub> = 1.05 V |     | CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|----------------------------|---|---------------------------|-----|--------------------------|-----|------|
|     |                            |   | MIN                       | MAX | MIN                      | MAX |      |
| 4   | t <sub>d(LCD_D_V)</sub>    | Delay time, LCD_CLK rising edge to LCD_D[15:0] valid (write)      |                           | 5   |                          | 7   | ns   |
| 5   | t <sub>d(LCD_D_I)</sub>    | Delay time, LCD_CLK rising edge to LCD_D[15:0] invalid (write)    | -6                        |     | -6                       |     | ns   |
| 6   | t <sub>d(LCD_E_A)</sub>    | Delay time, LCD_CLK rising edge to LCD_CS <sub>x</sub> _Ex low    |                           | 5   |                          | 7   | ns   |
| 7   | t <sub>d(LCD_E_I)</sub>    | Delay time, LCD_CLK rising edge to LCD_CS <sub>x</sub> _Ex high   | -6                        |     | -6                       |     | ns   |
| 8   | t <sub>d(LCD_A_A)</sub>    | Delay time, LCD_CLK rising edge to LCD_RS low                     |                           | 5   |                          | 7   | ns   |
| 9   | t <sub>d(LCD_A_I)</sub>    | Delay time, LCD_CLK rising edge to LCD_RS high                    | -6                        |     | -6                       |     | ns   |
| 10  | t <sub>d(LCD_W_A)</sub>    | Delay time, LCD_CLK rising edge to LCD_RW_WRB low                 |                           | 5   |                          | 7   | ns   |
| 11  | t <sub>d(LCD_W_I)</sub>    | Delay time, LCD_CLK rising edge to LCD_RW_WRB high                | -6                        |     | -6                       |     | ns   |
| 12  | t <sub>d(LCD_STRB_A)</sub> | Delay time, LCD_CLK rising edge to LCD_EN_RDB high                |                           | 5   |                          | 7   | ns   |
| 13  | t <sub>d(LCD_STRB_I)</sub> | Delay time, LCD_CLK rising edge to LCD_EN_RDB low                 | -6                        |     | -6                       |     | ns   |
| 14  | t <sub>d(LCD_D_Z)</sub>    | Delay time, LCD_CLK rising edge to LCD_D[15:0] in 3-state         |                           | 5   |                          | 7   | ns   |
| 15  | t <sub>d(Z_LCD_D)</sub>    | Delay time, LCD_CLK rising edge to LCD_D[15:0] valid from 3-state | -6                        |     | -6                       |     | ns   |

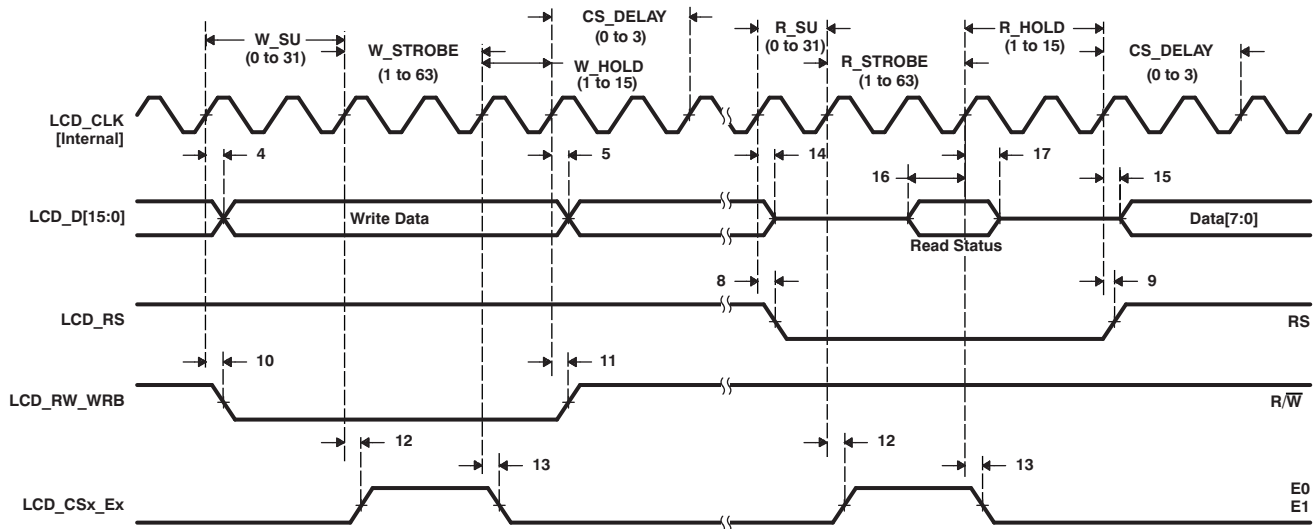


Figure 5-24. Character Display HD44780 Write

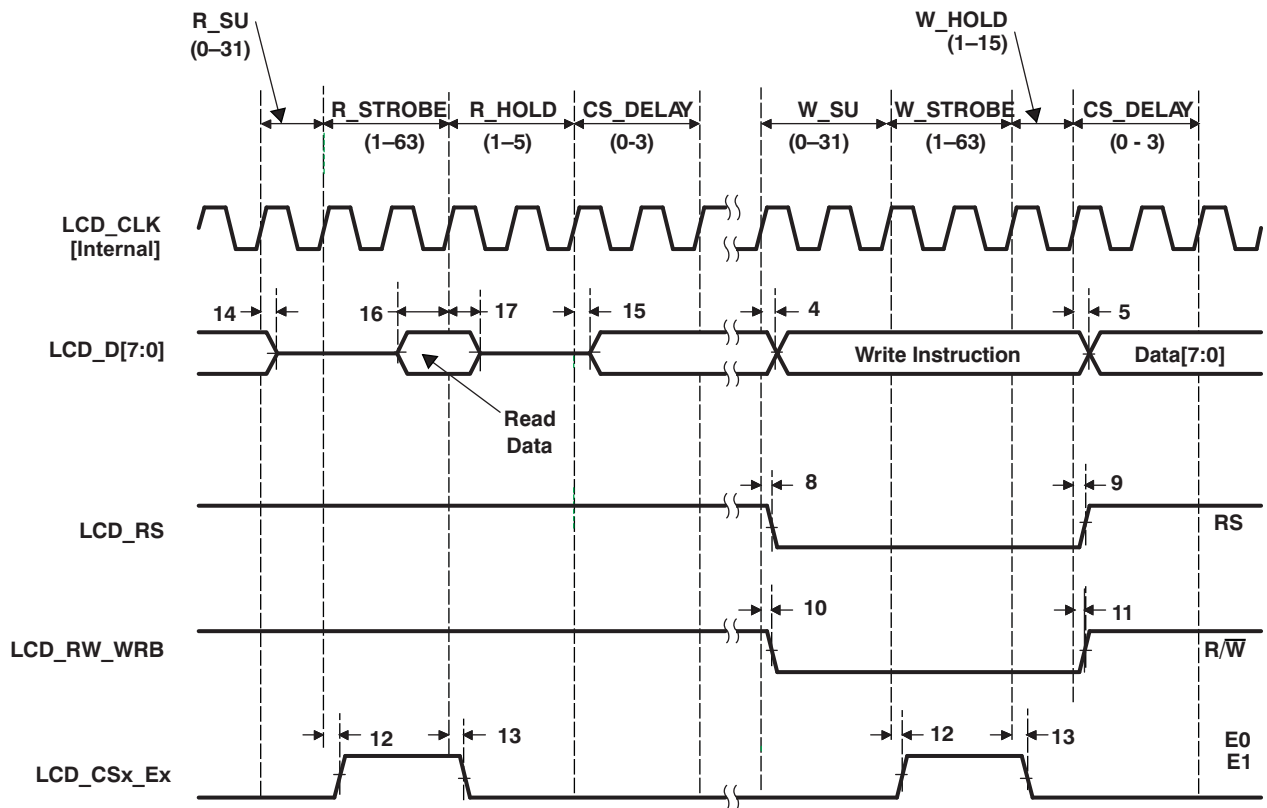


Figure 5-25. Character Display HD44780 Read

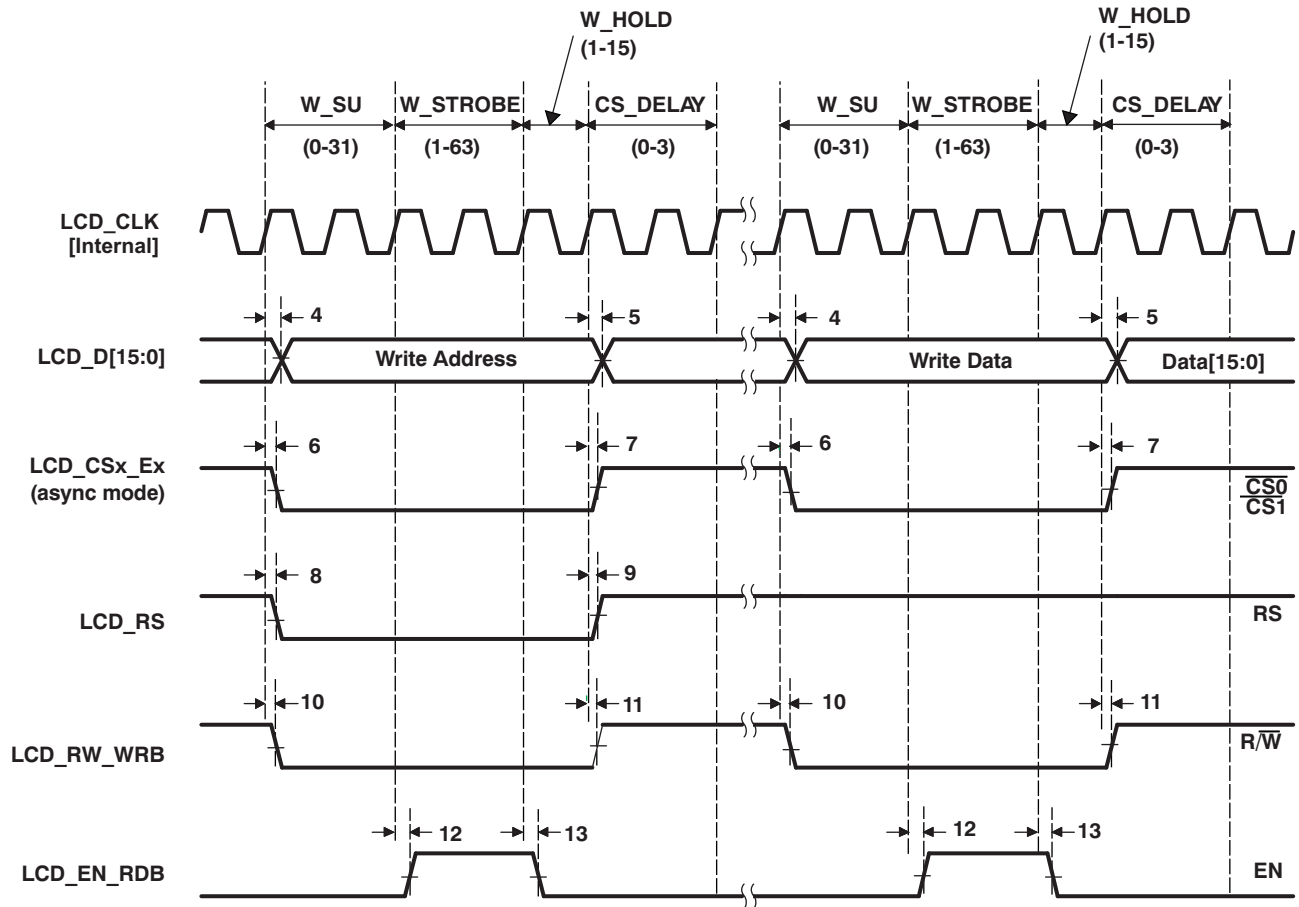


Figure 5-26. Micro-Interface Graphic Display 6800 Write

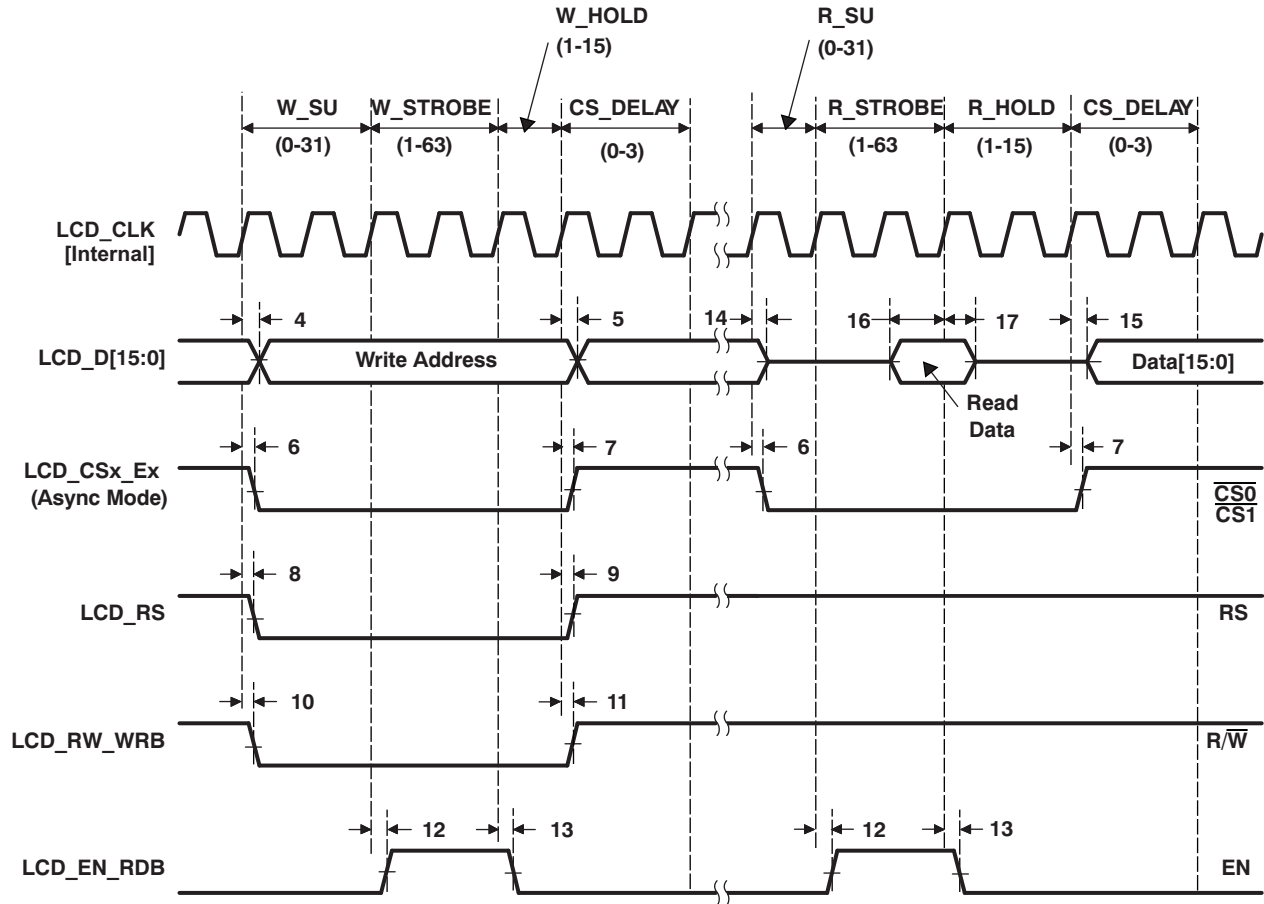


Figure 5-27. Micro-Interface Graphic Display 6800 Read

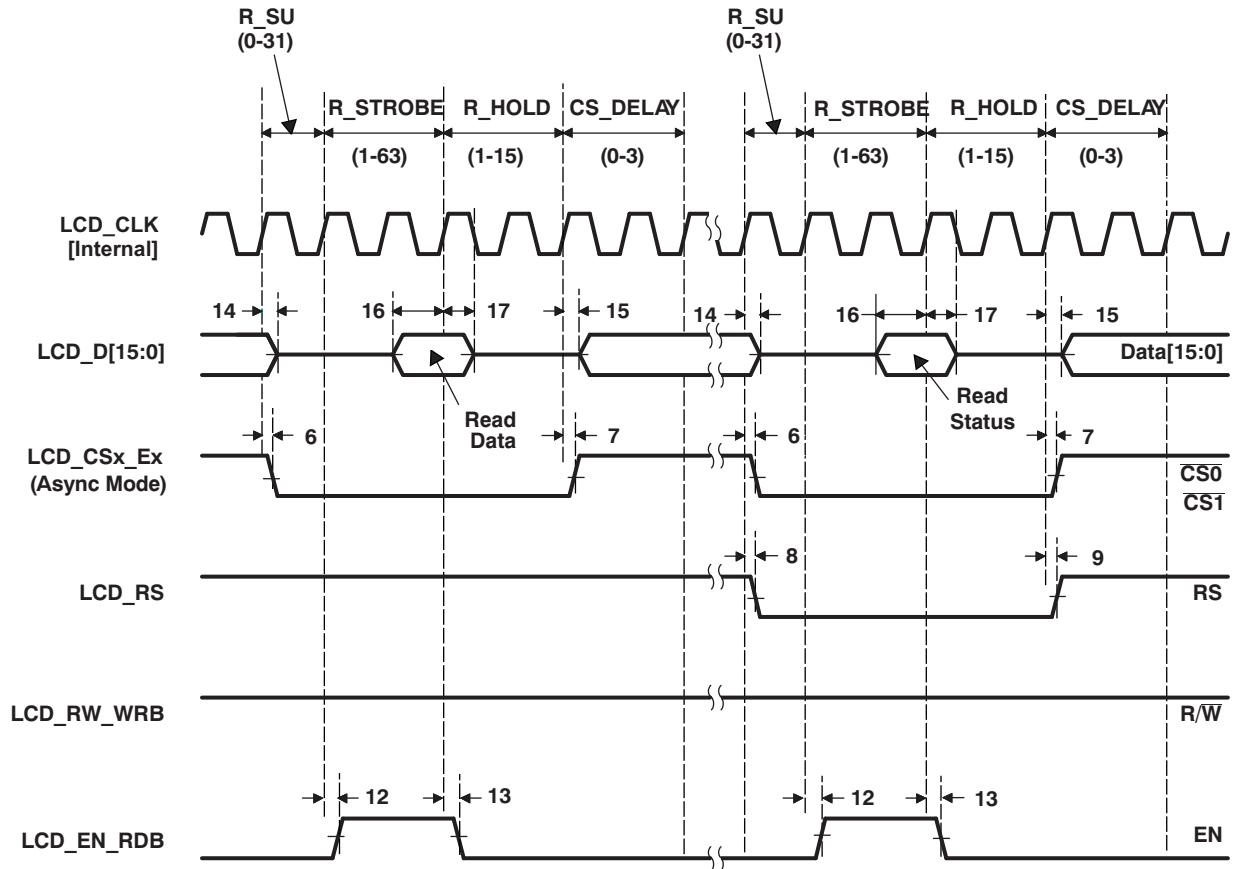


Figure 5-28. Micro-Interface Graphic Display 6800 Status

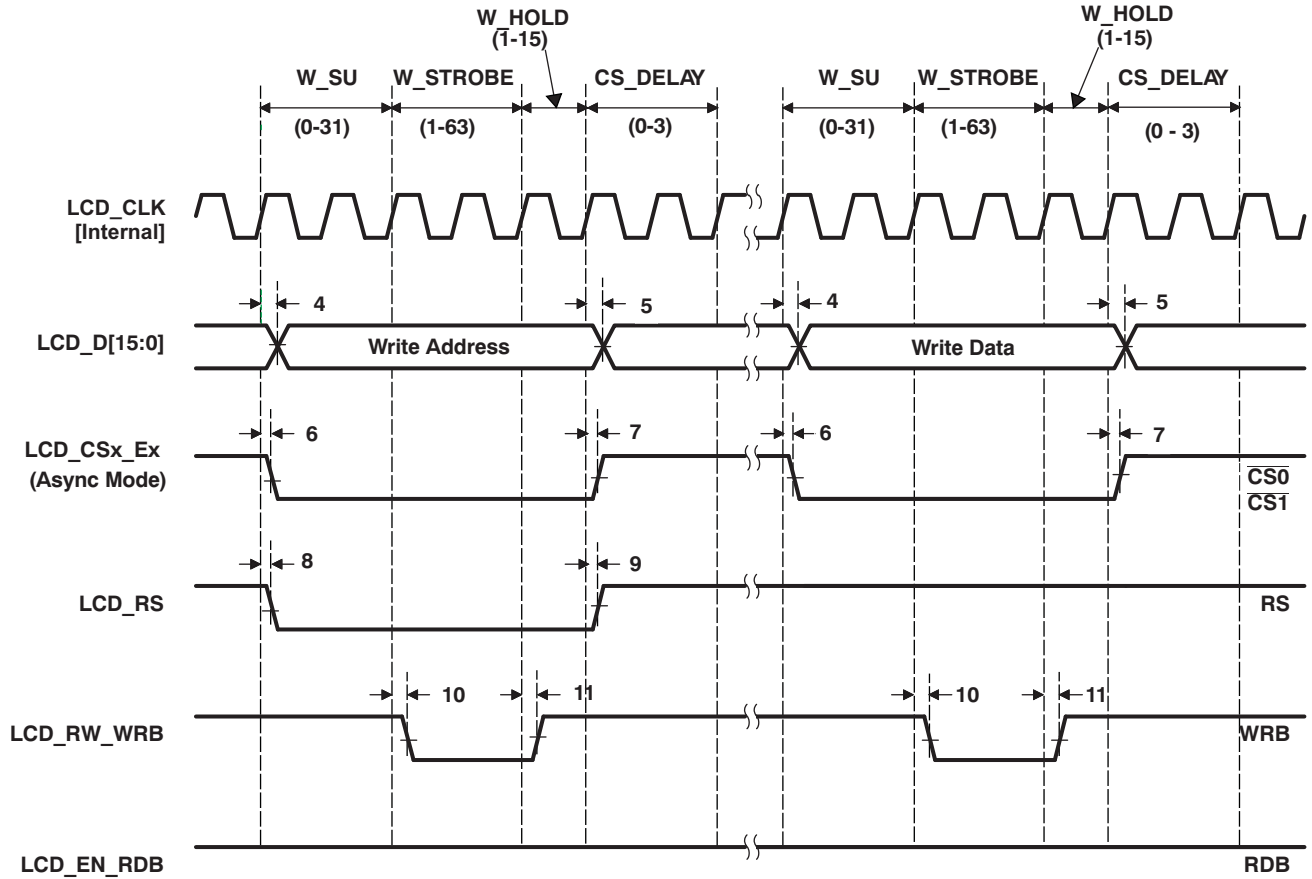


Figure 5-29. Micro-Interface Graphic Display 8080 Write



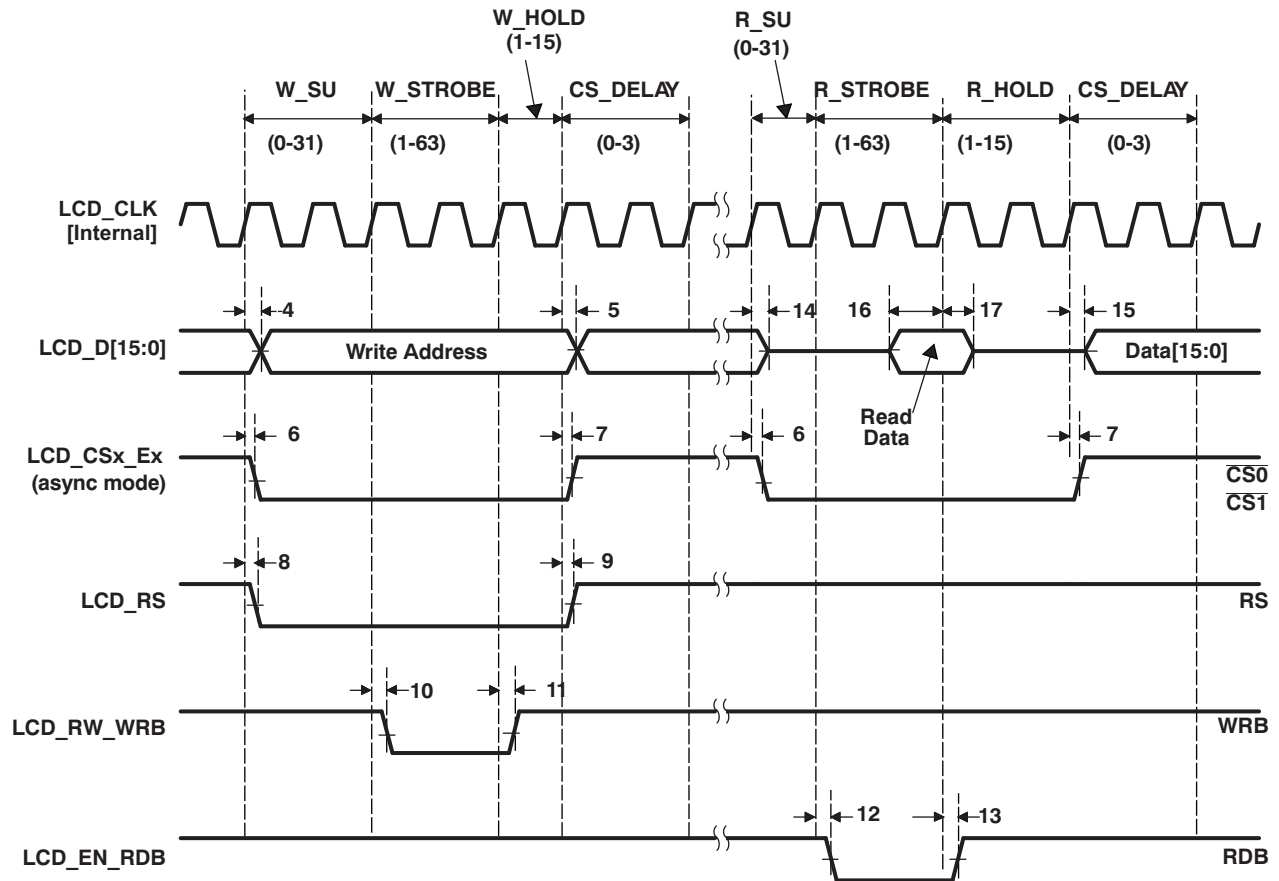


Figure 5-30. Micro-Interface Graphic Display 8080 Read

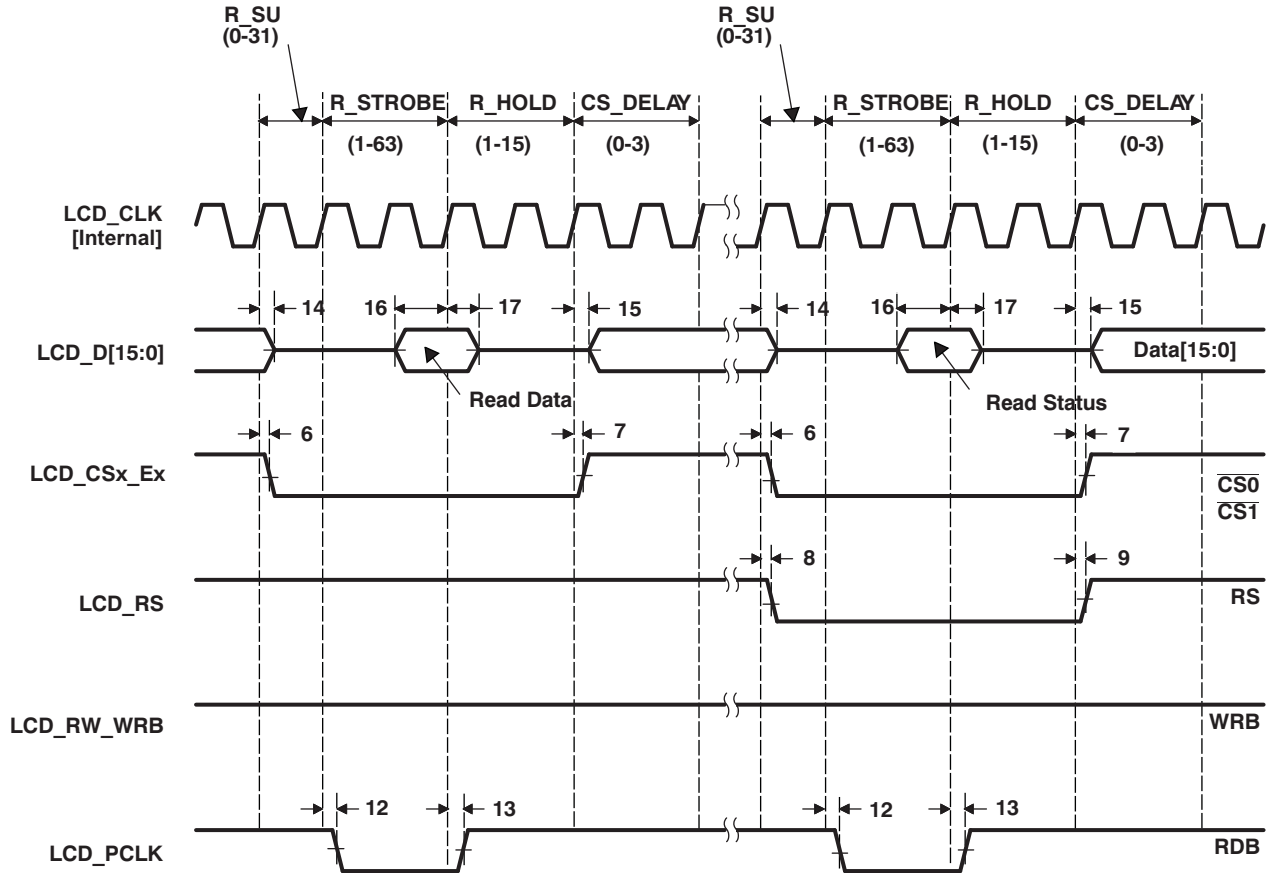


Figure 5-31. Micro-Interface Graphic Display 8080 Status

### 5.6.17 10-Bit SAR ADC

The device includes a 10-bit SAR ADC using a switched capacitor architecture that converts an analog input signal to a digital value at a maximum rate of 62.5-k samples per second (ksps) for the DSP. This SAR module supports six channels connected to three general purpose analog pins (GPAIN[3:1]) which can be used as general purpose outputs.

The device SAR supports the following features:

- Up to 62.5 ksps (2-MHz clock with 32 cycles per conversion)
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable bandgap reference voltages of 1 V or 0.8 V; or external  $V_{ref}$  of  $V_{DDA\_ANA}$
- Software controlled power down
- Individually configurable general-purpose digital outputs

#### 5.6.17.1 SAR ADC Peripheral Register Descriptions

Table 5-34 lists the SAR ADC peripheral registers.

**Table 5-34. SAR Analog Control Registers**

| CPU WORD ADDRESS | ACRONYM    | REGISTER DESCRIPTION                       |
|------------------|------------|--|
| 7012h            | SARCTRL    | SAR A/D Control Register                   |
| 7014h            | SARDATA    | SAR A/D Data Register                      |
| 7016h            | SARCLKCTRL | SAR A/D Clock Control Register             |
| 7018h            | SARPINCTRL | SAR A/D Reference and Pin Control Register |
| 701Ah            | SARGPOCTRL | SAR A/D GPO Control Register               |

#### 5.6.17.2 SAR ADC Electrical Data and Timing

Table 5-35 lists the switching characteristics for ADC.

**Table 5-35. Switching Characteristics Over Recommended Operating Conditions for ADC Characteristics**

| NO. | PARAMETER  | $CV_{DD} = 1.3\text{ V}, CV_{DD} = 1.05\text{ V}$ |           |                 | UNIT       |
|-----|--|---|-----------|-----------------|------------|
|     |  | MIN   | TYP       | MAX             |            |
| 1   | $t_{C(SCLC)}$ Cycle time, ADC internal conversion clock                    |   |           | 2               | MHz        |
| 3   | $t_{d(CONV)}$ Delay time, ADC conversion time                              |   |           | $32t_{C(SCLC)}$ | ns         |
| 4   | $S_{DNL}$ Static differential nonlinearity error (DNL measured for 9 bits) |   | $\pm 0.6$ |                 | LSB        |
| 5   | $S_{INL}$ Static integral nonlinearity error                               |   | $\pm 1$   |                 | LSB        |
| 6   | $Z_{set}$ Zero-scale offset error (INL measured for 9 bits)                |   |           | 2               | LSB        |
| 7   | $F_{set}$ Full-scale offset error  |   |           | 2               | LSB        |
| 8   | Analog input impedance   | 1   |           |                 | M $\Omega$ |
| 9   | Signal-to-noise ratio  |   | 54        |                 | dB         |

### 5.6.18 Serial Port Interface (SPI)

The device serial port interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to three SPI slave devices. The SPI can operate as a master device only, slave mode is not supported.

#### NOTE

The SPI is not supported by the device DMA controller, so DMA cannot be used in transferring data between the SPI and the on-chip RAM.

The DSP and external peripherals use the SPI to communicate. Typical applications include an interface to external I/O or peripheral expansion through devices such as shift registers, display drivers, SPI EEPROMs, and ADCs.

The SPI has the following features:

- Programmable divider for serial data clock generation
- Four pin interface (SPI\_CLK, SPI\_CS<sub>n</sub>, SPI\_RX, and SPI\_TX)
- Programmable data length (1 to 32 bits)
- Three external chip select signals
- Programmable transfer or frame size (1 to 4096 characters)
- Optional interrupt generation on character completion
- Programmable SPI\_CS<sub>n</sub> to SPI\_TX delay from 0 to 3 SPI\_CLK cycles
- Programmable signal polarities
- Programmable active clock edge
- Internal loopback mode for testing

#### 5.6.18.1 SPI Peripheral Register Descriptions

Table 5-36 lists the SPI registers.

**Table 5-36. SPI Module Registers**

| CPU WORD ADDRESS | ACRONYM  | REGISTER NAME                   |
|------------------|----------|---------------------------------|
| 3000h            | SPICDR   | Clock Divider Register          |
| 3001h            | SPICCR   | Clock Control Register          |
| 3002h            | SPIDCR1  | Device Configuration Register 1 |
| 3003h            | SPIDCR2  | Device Configuration Register 2 |
| 3004h            | SPICMD1  | Command Register 1              |
| 3005h            | SPICMD2  | Command Register 2              |
| 3006h            | SPISTAT1 | Status Register 1               |
| 3007h            | SPISTAT2 | Status Register 2               |
| 3008h            | SPIDAT1  | Data Register 1                 |
| 3009h            | SPIDAT2  | Data Register 2                 |

5.6.18.2 SPI Electrical Data and Timing

Table 5-37 and Table 5-38 list the timing and switching requirements for the SPI, respectively.

Table 5-37. Timing Requirements for SPI Inputs (see Figure 5-32, Figure 5-33, Figure 5-34, and Figure 5-35)

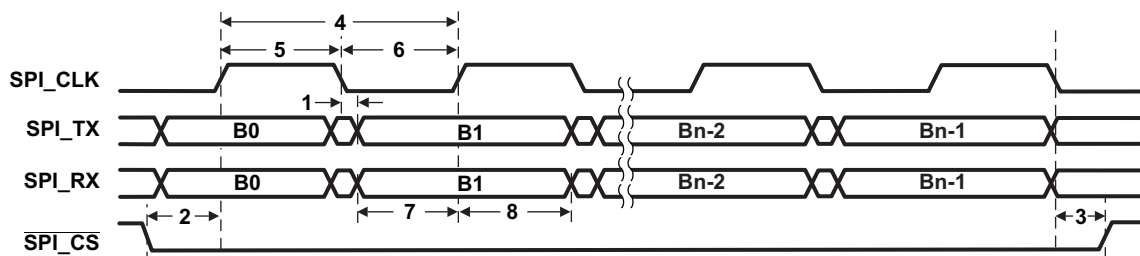
| NO. |                            |  | CV <sub>DD</sub> = 1.05 V     |     | CV <sub>DD</sub> = 1.3 V    |     | UNIT |
|-----|----------------------------|--|-------------------------------|-----|-----------------------------|-----|------|
|     |                            |  | MIN                           | MAX | MIN                         | MAX |      |
| 4   | t <sub>C(SCLK)</sub>       | Cycle time, SPI_CLK                                      | 66.4 or 4P <sup>(1)</sup> (2) |     | 40 or 4P <sup>(1)</sup> (2) |     | ns   |
| 5   | t <sub>w(SCLKH)</sub>      | Pulse duration, SPI_CLK high                             | 30                            |     | 19                          |     | ns   |
| 6   | t <sub>w(SCLKL)</sub>      | Pulse duration, SPI_CLK low                              | 30                            |     | 19                          |     | ns   |
| 7   | t <sub>su(SRXV-SCLK)</sub> | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 0 | 16.1                          |     | 13.9                        |     | ns   |
|     |                            | Setup time, SPI_RX valid before SPI_CLK low, SPI Mode 1  | 16.1                          |     | 13.9                        |     | ns   |
|     |                            | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 2 | 16.1                          |     | 13.9                        |     | ns   |
|     |                            | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 3 | 16.1                          |     | 13.9                        |     | ns   |
| 8   | t <sub>h(SCLK-SRXV)</sub>  | Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 0   | 0                             |     | 0                           |     | ns   |
|     |                            | Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 1    | 0                             |     | 0                           |     | ns   |
|     |                            | Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 2    | 0                             |     | 0                           |     | ns   |
|     |                            | Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 3   | 0                             |     | 0                           |     | ns   |

- (1) P = SYSCLOCK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
- (2) Use whichever value is greater.

Table 5-38. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs (see Figure 5-32, Figure 5-33, Figure 5-34, and Figure 5-35)

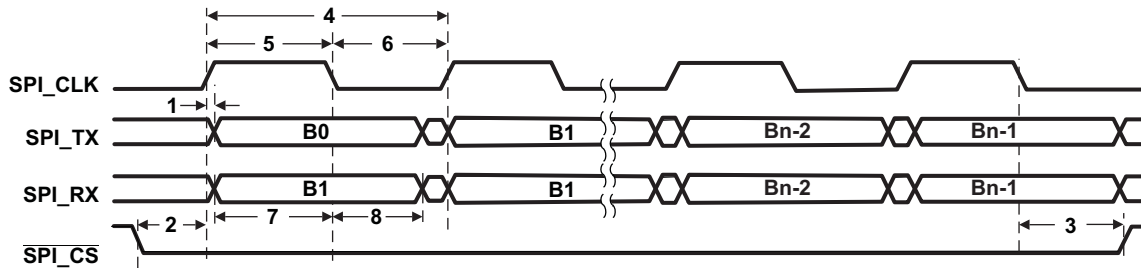
| NO. | PARAMETER                     | CV <sub>DD</sub> = 1.05 V                            |      | CV <sub>DD</sub> = 1.3 V              |      | UNIT |    |
|-----|-------------------------------|--|------|---------------------------------------|------|------|----|
|     |                               | MIN  | MAX  | MIN                                   | MAX  |      |    |
| 1   | t <sub>d(SCLK-STXV)</sub>     | Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 0  | -4.2 | 8.9                                   | -4.9 | 5.3  | ns |
|     |                               | Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 1 | -4.2 | 8.9                                   | -4.9 | 5.3  | ns |
|     |                               | Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 2 | -4.2 | 8.9                                   | -4.9 | 5.3  | ns |
|     |                               | Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 3  | -4.2 | 8.9                                   | -4.9 | 5.3  | ns |
| 2   | t <sub>d(SPICS-SCLK)</sub>    | t <sub>C</sub> - 8 + D <sup>(1)</sup>                |      | t <sub>C</sub> - 8 + D <sup>(1)</sup> |      | ns   |    |
| 3   | t <sub>oh(SCLKI-SPICSI)</sub> | 0.5t <sub>C</sub> - 2.2                              |      | 0.5t <sub>C</sub> - 2.2               |      | ns   |    |

- (1) D is the programmable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.



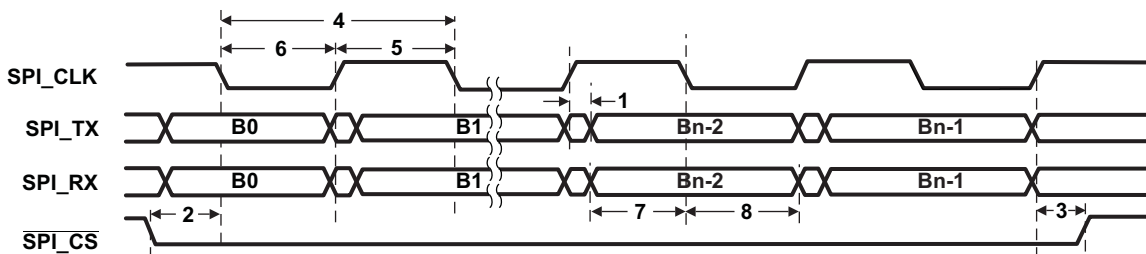
- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI\_CS<sub>n</sub> is configurable, active-low polarity is shown.

Figure 5-32. SPI Mode 0 Transfer (CKP<sub>n</sub> = 0, CKPH<sub>n</sub> = 0)



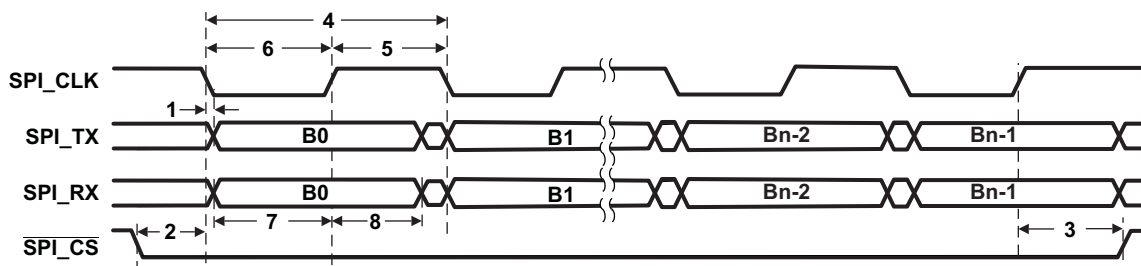
- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI\_CSn is configurable, active-low polarity is shown.

**Figure 5-33. SPI Mode 1 Transfer (CKPn = 0, CKPHn = 1)**



- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI\_CSn is configurable, active-low polarity is shown.

**Figure 5-34. SPI Mode 2 Transfer (CKPn = 1, CKPHn = 0)**



- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI\_CSn is configurable, active-low polarity is shown.

**Figure 5-35. SPI Mode 3 Transfer (CKPn = 1, CKPHn = 1)**

### 5.6.19 Universal Serial Bus (USB) 2.0 Controller

The device USB2.0 peripheral supports the following features:

- USB2.0 peripheral at speeds high-speed (480 Mbps) and full-speed (12 Mbps)
- All transfer modes (control, bulk, interrupt, and isochronous asynchronous mode)
- Four transmit (TX) and four receive (RX) Endpoints in addition to Control Endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB2.0 high-speed PHY
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB 2.0 peripheral on this device, does not support:

- Host mode (only peripheral and device modes are supported)
- On-Chip Charge Pump
- On-the-Go (OTG) mode

### 5.6.19.1 USB 2.0 Peripheral Register Descriptions

Table 5-39 lists of the USB2.0 peripheral registers.

**Table 5-39. Universal Serial Bus (USB) Registers<sup>(1)</sup>**

| CPU WORD ADDRESS | ACRONYM     | REGISTER DESCRIPTION                   |
|------------------|-------------|--|
| 8000h            | REVID1      | Revision Identification Register 1     |
| 8001h            | REVID2      | Revision Identification Register 2     |
| 8004h            | CTRLR       | Control Register                       |
| 8008h            | STATR       | Status Register                        |
| 800Ch            | EMUR        | Emulation Register                     |
| 8010h            | MODER1      | Mode Register 1                        |
| 8011h            | MODER2      | Mode Register 2                        |
| 8014h            | AUTOREQ     | Auto Request Register                  |
| 8018h            | SRPFIXTIME1 | SRP Fix Time Register 1                |
| 8019h            | SRPFIXTIME2 | SRP Fix Time Register 2                |
| 801Ch            | TEARDOWN1   | Teardown Register 1                    |
| 801Dh            | TEARDOWN2   | Teardown Register 2                    |
| 8020h            | INTSRCR1    | USB Interrupt Source Register 1        |
| 8021h            | INTSRCR2    | USB Interrupt Source Register 2        |
| 8024h            | INTSETR1    | USB Interrupt Source Set Register 1    |
| 8025h            | INTSETR2    | USB Interrupt Source Set Register 2    |
| 8028h            | INTCLRR1    | USB Interrupt Source Clear Register 1  |
| 8029h            | INTCLRR2    | USB Interrupt Source Clear Register 2  |
| 802Ch            | INTMSKR1    | USB Interrupt Mask Register 1          |
| 802Dh            | INTMSKR2    | USB Interrupt Mask Register 2          |
| 8030h            | INTMSKSETR1 | USB Interrupt Mask Set Register 1      |
| 8031h            | INTMSKSETR2 | USB Interrupt Mask Set Register 2      |
| 8034h            | INTMSKCLRR1 | USB Interrupt Mask Clear Register 1    |
| 8035h            | INTMSKCLRR2 | USB Interrupt Mask Clear Register 2    |
| 8038h            | INTMASKEDR1 | USB Interrupt Source Masked Register 1 |
| 8039h            | INTMASKEDR2 | USB Interrupt Source Masked Register 2 |
| 803Ch            | EOIR        | USB End of Interrupt Register          |
| 8040h            | INTVECTR1   | USB Interrupt Vector Register 1        |
| 8041h            | INTVECTR2   | USB Interrupt Vector Register 2        |
| 8050h            | GREP1SZR1   | Generic RNDIS EP1Size Register 1       |
| 8051h            | GREP1SZR2   | Generic RNDIS EP1Size Register 2       |
| 8054h            | GREP2SZR1   | Generic RNDIS EP2 Size Register 1      |
| 8055h            | GREP2SZR2   | Generic RNDIS EP2 Size Register 2      |
| 8058h            | GREP3SZR1   | Generic RNDIS EP3 Size Register 1      |
| 8059h            | GREP3SZR2   | Generic RNDIS EP3 Size Register 2      |
| 805Ch            | GREP4SZR1   | Generic RNDIS EP4 Size Register 1      |
| 805Dh            | GREP4SZR2   | Generic RNDIS EP4 Size Register 2      |

(1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to 00b in the USB system control register to enable word accesses to the USB registers .



**Table 5-39. Universal Serial Bus (USB) Registers<sup>(1)</sup> (continued)**

| CPU WORD ADDRESS                      | ACRONYM                                  | REGISTER DESCRIPTION  |
|---------------------------------------|--|---|
| <b>Common USB Registers</b>           |  |   |
| 8401h                                 | FADDR_POWER                              | Function Address Register, Power Management Register  |
| 8402h                                 | INTRTX                                   | Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4  |
| 8405h                                 | INTRRX                                   | Interrupt Register for Receive Endpoints 1 to 4   |
| 8406h                                 | INTRTXE                                  | Interrupt enable register for INTRTX  |
| 8409h                                 | INTRRXE                                  | Interrupt Enable Register for INTRRX  |
| 840Ah                                 | INTRUSB_INTRUSBE                         | Interrupt Register for Common USB Interrupts, Interrupt Enable Register   |
| 840Dh                                 | FRAME                                    | Frame Number Register   |
| 840Eh                                 | INDEX_TESTMODE                           | Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes |
| <b>USB Indexed Registers</b>          |  |   |
| 8411h                                 | TXMAXP_IND                               | Maximum Packet Size for Peripheral and Host Transmit Endpoint. (Index register set to select Endpoints 1-4)       |
| 8412h                                 | PERI_CSR0_IND                            | Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)              |
|                                       | PERI_TXCSR_IND                           | Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)            |
| 8415h                                 | RXMAXP_IND                               | Maximum Packet Size for Peripheral and Host Receive Endpoint. (Index register set to select Endpoints 1-4)        |
| 8416h                                 | PERI_RXCSR_IND                           | Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)             |
| 8419h                                 | COUNT0_IND                               | Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)                            |
|                                       | RXCOUNT_IND                              | Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)                      |
| 841Ah                                 | –  | Reserved  |
| 841Dh                                 | –  | Reserved  |
| 841Eh                                 | CONFIGDATA_INDC<br>(Upper byte of 841Eh) | Returns details of core configuration. (index register set to select Endpoint 0)                                  |
| <b>USB FIFO Registers</b>             |  |   |
| 8421h                                 | FIFO0R1                                  | Transmit and Receive FIFO Register 1 for Endpoint 0   |
| 8422h                                 | FIFO0R2                                  | Transmit and Receive FIFO Register 2 for Endpoint 0   |
| 8425h                                 | FIFO1R1                                  | Transmit and Receive FIFO Register 1 for Endpoint 1   |
| 8426h                                 | FIFO1R2                                  | Transmit and Receive FIFO Register 2 for Endpoint 1   |
| 8429h                                 | FIFO2R1                                  | Transmit and Receive FIFO Register 1 for Endpoint 2   |
| 842Ah                                 | FIFO2R2                                  | Transmit and Receive FIFO Register 2 for Endpoint 2   |
| 842Dh                                 | FIFO3R1                                  | Transmit and Receive FIFO Register 1 for Endpoint 3   |
| 842Eh                                 | FIFO3R2                                  | Transmit and Receive FIFO Register 2 for Endpoint 3   |
| 8431h                                 | FIFO4R1                                  | Transmit and Receive FIFO Register 1 for Endpoint 4   |
| 8432h                                 | FIFO4R2                                  | Transmit and Receive FIFO Register 2 for Endpoint 4   |
| <b>Dynamic FIFO Control Registers</b> |  |   |
| 8461h                                 | DEVCTL                                   | Device Control Register   |
| 8462h                                 | TXFIFOSZ_RXFIFOSZ                        | Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4)              |
| 8465h                                 | TXFIFOADDR                               | Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4)                                       |
| 8466h                                 | RXFIFOADDR                               | Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4)  |
| 846Dh                                 | –  | Reserved  |

Table 5-39. Universal Serial Bus (USB) Registers<sup>(1)</sup> (continued)

| CPU WORD ADDRESS                                  | ACRONYM                             | REGISTER DESCRIPTION   |
|---|-------------------------------------|--|
| <b>Control and Status Register for Endpoint 0</b> |                                     |  |
| 8501h   | –                                   | Reserved   |
| 8502h   | PERI_CSR0                           | Control Status Register for Peripheral Endpoint 0                          |
| 8505h   | –                                   | Reserved   |
| 8506h   | –                                   | Reserved   |
| 8509h   | COUNT0                              | Number of Received Bytes in Endpoint 0 FIFO                                |
| 850Ah   | –                                   | Reserved   |
| 850Dh   | –                                   | Reserved   |
| 850Eh   | CONFIGDATA<br>(Upper byte of 850Eh) | Returns details of core configuration.                                     |
| <b>Control and Status Register for Endpoint 1</b> |                                     |  |
| 8511h   | TXMAXP                              | Maximum Packet Size for Peripheral and Host Transmit Endpoint              |
| 8512h   | PERI_TXCSR                          | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8515h   | RXMAXP                              | Maximum Packet Size for Peripheral and Host Receive Endpoint               |
| 8516h   | PERI_RXCSR                          | Control Status Register for Peripheral Receive Endpoint (peripheral mode)  |
| 8519h   | RXCOUNT                             | Number of Bytes in the Receiving Endpoint's FIFO                           |
| 851Ah   | –                                   | Reserved   |
| 851Dh   | –                                   | Reserved   |
| 851Eh   | –                                   | Reserved   |
| <b>Control and Status Register for Endpoint 2</b> |                                     |  |
| 8521h   | TXMAXP                              | Maximum Packet Size for Peripheral and Host Transmit Endpoint              |
| 8522h   | PERI_TXCSR                          | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8525h   | RXMAXP                              | Maximum Packet Size for Peripheral and Host Receive Endpoint               |
| 8526h   | PERI_RXCSR                          | Control Status Register for Peripheral Receive Endpoint (peripheral mode)  |
| 8529h   | RXCOUNT                             | Number of Bytes in Host Receive endpoint FIFO                              |
| 852Ah   | –                                   | Reserved   |
| 852Dh   | –                                   | Reserved   |
| 852Eh   | –                                   | Reserved   |
| <b>Control and Status Register for Endpoint 3</b> |                                     |  |
| 8531h   | TXMAXP                              | Maximum Packet Size for Peripheral and Host Transmit Endpoint              |
| 8532h   | PERI_TXCSR                          | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8535h   | RXMAXP                              | Maximum Packet Size for Peripheral and Host Receive Endpoint               |
| 8536h   | PERI_RXCSR                          | Control Status Register for Peripheral Receive Endpoint (peripheral mode)  |
| 8539h   | RXCOUNT                             | Number of Bytes in Host Receive endpoint FIFO                              |
| 853Ah   | –                                   | Reserved   |
| 853Dh   | –                                   | Reserved   |
| 853Eh   | –                                   | Reserved   |
| <b>Control and Status Register for Endpoint 4</b> |                                     |  |
| 8541h   | TXMAXP                              | Maximum Packet Size for Peripheral and Host Transmit Endpoint              |
| 8542h   | PERI_TXCSR                          | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8545h   | RXMAXP                              | Maximum Packet Size for Peripheral and Host Receive Endpoint               |
| 8546h   | PERI_RXCSR                          | Control Status Register for Peripheral Receive Endpoint (peripheral mode)  |
| 8549h   | RXCOUNT                             | Number of Bytes in Host Receive endpoint FIFO                              |
| 854Ah   | –                                   | Reserved   |
| 854Dh   | –                                   | Reserved   |
| 854Eh   | –                                   | Reserved   |

**Table 5-39. Universal Serial Bus (USB) Registers<sup>(1)</sup> (continued)**

| CPU WORD ADDRESS                 | ACRONYM         | REGISTER DESCRIPTION                                     |
|----------------------------------|-----------------|--|
| <b>CPPI DMA (CMDA) Registers</b> |                 |  |
| 9000h                            | –               | Reserved   |
| 9001h                            | –               | Reserved   |
| 9004h                            | TDFDQ           | CDMA Teardown Free Descriptor Queue Control Register     |
| 9008h                            | DMAEMU          | CDMA Emulation Control Register                          |
| 9800h                            | TXGCR1[0]       | Transmit Channel 0 Global Configuration Register 1       |
| 9801h                            | TXGCR2[0]       | Transmit Channel 0 Global Configuration Register 2       |
| 9808h                            | RXGCR1[0]       | Receive Channel 0 Global Configuration Register 1        |
| 9809h                            | RXGCR2[0]       | Receive Channel 0 Global Configuration Register 2        |
| 980Ch                            | RXHPCR1A[0]     | Receive Channel 0 Host Packet Configuration Register 1 A |
| 980Dh                            | RXHPCR2A[0]     | Receive Channel 0 Host Packet Configuration Register 2 A |
| 9810h                            | RXHPCR1B[0]     | Receive Channel 0 Host Packet Configuration Register 1 B |
| 9811h                            | RXHPCR2B[0]     | Receive Channel 0 Host Packet Configuration Register 2 B |
| 9820h                            | TXGCR1[1]       | Transmit Channel 1 Global Configuration Register 1       |
| 9821h                            | TXGCR2[1]       | Transmit Channel 1 Global Configuration Register 2       |
| 9828h                            | RXGCR1[1]       | Receive Channel 1 Global Configuration Register 1        |
| 9829h                            | RXGCR2[1]       | Receive Channel 1 Global Configuration Register 2        |
| 982Ch                            | RXHPCR1A[1]     | Receive Channel 1 Host Packet Configuration Register 1 A |
| 982Dh                            | RXHPCR2A[1]     | Receive Channel 1 Host Packet Configuration Register 2 A |
| 9830h                            | RXHPCR1B[1]     | Receive Channel 1 Host Packet Configuration Register 1 B |
| 9831h                            | RXHPCR2B[1]     | Receive Channel 1 Host Packet Configuration Register 2 B |
| 9840h                            | TXGCR1[2]       | Transmit Channel 2 Global Configuration Register 1       |
| 9841h                            | TXGCR2[2]       | Transmit Channel 2 Global Configuration Register 2       |
| 9848h                            | RXGCR1[2]       | Receive Channel 2 Global Configuration Register 1        |
| 9849h                            | RXGCR2[2]       | Receive Channel 2 Global Configuration Register 2        |
| 984Ch                            | RXHPCR1A[2]     | Receive Channel 2 Host Packet Configuration Register 1 A |
| 984Dh                            | RXHPCR2A[2]     | Receive Channel 2 Host Packet Configuration Register 2 A |
| 9850h                            | RXHPCR1B[2]     | Receive Channel 2 Host Packet Configuration Register 1 B |
| 9851h                            | RXHPCR2B[2]     | Receive Channel 2 Host Packet Configuration Register 2 B |
| 9860h                            | TXGCR1[3]       | Transmit Channel 3 Global Configuration Register 1       |
| 9861h                            | TXGCR2[3]       | Transmit Channel 3 Global Configuration Register 2       |
| 9868h                            | RXGCR1[3]       | Receive Channel 3 Global Configuration Register 1        |
| 9869h                            | RXGCR2[3]       | Receive Channel 3 Global Configuration Register 2        |
| 986Ch                            | RXHPCR1A[3]     | Receive Channel 3 Host Packet Configuration Register 1 A |
| 986Dh                            | RXHPCR2A[3]     | Receive Channel 3 Host Packet Configuration Register 2 A |
| 9870h                            | RXHPCR1B[3]     | Receive Channel 3 Host Packet Configuration Register 1 B |
| 9871h                            | RXHPCR2B[3]     | Receive Channel 3 Host Packet Configuration Register 2 B |
| A000h                            | DMA_SCHED_CTRL1 | CDMA Scheduler Control Register 1                        |
| A001h                            | DMA_SCHED_CTRL2 | CDMA Scheduler Control Register 1                        |
| A800h + 4 × N                    | ENTRYLSW[N]     | CDMA Scheduler Table Word N Registers LSW (N = 0 to 63)  |
| A801h + 4 × N                    | ENTRYMSW[N]     | CDMA Scheduler Table Word N Registers MSW (N = 0 to 63)  |

Table 5-39. Universal Serial Bus (USB) Registers<sup>(1)</sup> (continued)

| CPU WORD ADDRESS                      | ACRONYM       | REGISTER DESCRIPTION   |
|---------------------------------------|---------------|--|
| <b>Queue Manager (QMGR) Registers</b> |               |  |
| C000h                                 | –             | Reserved   |
| C001h                                 | –             | Reserved   |
| C008h                                 | DIVERSION1    | Queue Manager Queue Diversion Register 1                             |
| C009h                                 | DIVERSION2    | Queue Manager Queue Diversion Register 2                             |
| C020h                                 | FDBSC0        | Queue Manager Free Descriptor and Buffer Starvation Count Register 0 |
| C021h                                 | FDBSC1        | Queue Manager Free Descriptor and Buffer Starvation Count Register 1 |
| C024h                                 | FDBSC2        | Queue Manager Free Descriptor and Buffer Starvation Count Register 2 |
| C025h                                 | FDBSC3        | Queue Manager Free Descriptor and Buffer Starvation Count Register 3 |
| C028h                                 | FDBSC4        | Queue Manager Free Descriptor and Buffer Starvation Count Register 4 |
| C029h                                 | FDBSC5        | Queue Manager Free Descriptor and Buffer Starvation Count Register 5 |
| C02Ch                                 | FDBSC6        | Queue Manager Free Descriptor and Buffer Starvation Count Register 6 |
| C02Dh                                 | FDBSC7        | Queue Manager Free Descriptor and Buffer Starvation Count Register 7 |
| C080h                                 | LRAM0BASE1    | Queue Manager Linking RAM Region 0 Base Address Register 1           |
| C081h                                 | LRAM0BASE2    | Queue Manager Linking RAM Region 0 Base Address Register 2           |
| C084h                                 | LRAM0SIZE     | Queue Manager Linking RAM Region 0 Size Register                     |
| C085h                                 | –             | Reserved   |
| C088h                                 | LRAM1BASE1    | Queue Manager Linking RAM Region 1 Base Address Register 1           |
| C089h                                 | LRAM1BASE2    | Queue Manager Linking RAM Region 1 Base Address Register 2           |
| C090h                                 | PEND0         | Queue Manager Queue Pending 0  |
| C091h                                 | PEND1         | Queue Manager Queue Pending 1  |
| C094h                                 | PEND2         | Queue Manager Queue Pending 2  |
| C095h                                 | PEND3         | Queue Manager Queue Pending 3  |
| C098h                                 | PEND4         | Queue Manager Queue Pending 4  |
| C099h                                 | PEND5         | Queue Manager Queue Pending 5  |
| D000h + 16 × R                        | QMEMRBASE1[R] | Queue Manager Memory Region R Base Address Register 1 (R = 0 to 15)  |
| D001h + 16 × R                        | QMEMRBASE2[R] | Queue Manager Memory Region R Base Address Register 2 (R = 0 to 15)  |
| D004h + 16 × R                        | QMEMRCTRL1[R] | Queue Manager Memory Region R Control Register (R = 0 to 15)         |
| D005h + 16 × R                        | QMEMRCTRL2[R] | Queue Manager Memory Region R Control Register (R = 0 to 15)         |
| E000h + 16 × N                        | CTRL1A        | Queue Manager Queue N Control Register 1A (N = 0 to 63)              |
| E001h + 16 × N                        | CTRL2A        | Queue Manager Queue N Control Register 2A (N = 0 to 63)              |
| E004h + 16 × N                        | CTRL1B        | Queue Manager Queue N Control Register 1B (N = 0 to 63)              |
| E005h + 16 × N                        | CTRL2B        | Queue Manager Queue N Control Register 2B (N = 0 to 63)              |
| E008h + 16 × N                        | CTRL1C        | Queue Manager Queue N Control Register 1C (N = 0 to 63)              |
| E009h + 16 × N                        | CTRL2C        | Queue Manager Queue N Control Register 2C (N = 0 to 63)              |
| E00Ch + 16 × N                        | CTRL1D        | Queue Manager Queue N Control Register 1D (N = 0 to 63)              |
| E00Dh + 16 × N                        | CTRL2D        | Queue Manager Queue N Control Register 2D (N = 0 to 63)              |
| E800h + 16 × N                        | QSTAT1A       | Queue Manager Queue N Status Register 1A (N = 0 to 63)               |
| E801h + 16 × N                        | QSTAT2A       | Queue Manager Queue N Status Register 2A (N = 0 to 63)               |
| E804h + 16 × N                        | QSTAT1B       | Queue Manager Queue N Status Register 1B (N = 0 to 63)               |
| E805h + 16 × N                        | QSTAT2B       | Queue Manager Queue N Status Register 2B (N = 0 to 63)               |
| E808h + 16 × N                        | QSTAT1C       | Queue Manager Queue N Status Register 1C (N = 0 to 63)               |
| E809h + 16 × N                        | QSTAT2C       | Queue Manager Queue N Status Register 2C (N = 0 to 63)               |

### 5.6.19.2 USB 2.0 Electrical Data and Timing

Table 5-40 lists the switching characteristics USB 2.0.

**Table 5-40. Switching Characteristics Over Recommended Operating Conditions for USB 2.0**  
(see Figure 5-36)

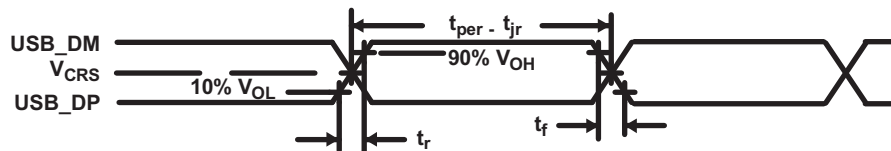
| NO. | PARAMETER   | CV <sub>DD</sub> = 1.05 V, CV <sub>DD</sub> = 1.3 V |      |                                       |      | UNIT |
|-----|---|---|------|---------------------------------------|------|------|
|     |   | FULL SPEED<br>12 Mbps                               |      | HIGH SPEED<br>480 Mbps <sup>(1)</sup> |      |      |
|     |   | MIN   | MAX  | MIN                                   | MAX  |      |
| 1   | t <sub>r(D)</sub> Rise time, USB_DP and USB_DM signals <sup>(2)</sup> | 4   | 20   | 0.5                                   |      | ns   |
| 2   | t <sub>f(D)</sub> Fall time, USB_DP and USB_DM signals <sup>(2)</sup> | 4   | 20   | 0.5                                   |      | ns   |
| 3   | t <sub>rFM</sub> Rise and Fall time, matching <sup>(3)</sup>          | 90  | 111  | –                                     | –    |      |
| 4   | V <sub>CRS</sub> Output signal cross-over voltage <sup>(2)</sup>      | 1.3   | 2    | –                                     | –    | V    |
| 7   | t <sub>w(EOPT)</sub> Pulse duration, EOP transmitter <sup>(4)</sup>   | 160   | 175  | –                                     | –    | ns   |
| 8   | t <sub>w(EOPR)</sub> Pulse duration, EOP receiver <sup>(4)</sup>      | 82  |      | –                                     |      | ns   |
| 9   | t <sub>(DRATE)</sub> Data Rate  |   | 12   |                                       | 480  | Mbps |
| 10  | Z <sub>DRV</sub> Driver Output Resistance                             | 40.5  | 49.5 | 40.5                                  | 49.5 | Ω    |
| 11  | Z <sub>INP</sub> Receiver Input Impedance                             | 100k  |      | –                                     | –    | Ω    |

(1) For more detailed information, see the Universal Serial Bus Specification, Revision 2.0, Chapter 7.

(2) Full speed and high speed C<sub>L</sub> = 50 pF

(3) t<sub>RFM</sub> = (t<sub>r</sub>/t<sub>f</sub>) × 100. [Excluding the first transaction from the IDLE state.]

(4) Must accept as valid EOP.



**Figure 5-36. USB2.0 Integrated Transceiver Interface Timing**

## 5.6.20 General-Purpose Timers

The device has three 32-bit software programmable timers. Each timer can be used as a general-purpose (GP) timer. Timer2 can be configured as either a GP or a Watchdog (WD) or both. General-purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. A watchdog timer is used to reset the CPU in case it gets into an infinite loop. The GP timers are 32-bit timers with a 13-bit prescaler that can divide the CPU clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts. The watchdog timer is a 16-bit counter with a 16-bit prescaler used to provide a recovery mechanism for the device in the event of a fault condition, such as a nonexiting code loop.

The device timers support the following:

- A 32-bit programmable countdown timer
- A 13-bit prescaler divider
- Timer modes:
  - 32-bit general-purpose timer
  - 32-bit watchdog timer (Timer2 only)
- An auto-reload option
- Generating a single interrupt to CPU (The interrupt is individually latched to determine which timer triggered the interrupt.)
- Generating an active low pulse to the hardware reset (watchdog only)
- Using an interrupt for a DMA event

### 5.6.20.1 Timers Peripheral Register Descriptions

Table 5-41, Table 5-42, Table 5-43, and Table 5-44 show the timer and watchdog registers.

**Table 5-41. Watchdog Timer Registers (Timer2 Only)**

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION               |
|------------------|---------|------------------------------------|
| 1880h            | WDKCKLK | Watchdog Kick Lock Register        |
| 1882h            | WDKICK  | Watchdog Kick Register             |
| 1884h            | WDSVLR  | Watchdog Start Value Lock Register |
| 1886h            | WDSVR   | Watchdog Start Value Register      |
| 1888h            | WDENLOK | Watchdog Enable Lock Register      |
| 188Ah            | WDEN    | Watchdog Enable Register           |
| 188Ch            | WDPSLR  | Watchdog Prescale Lock Register    |
| 188Eh            | WDPS    | Watchdog Prescale Register         |

**Table 5-42. General-Purpose Timer 0 Registers**

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION       |
|------------------|---------|----------------------------|
| 1810h            | TCR     | Timer 0 Control Register   |
| 1812h            | TIMPRD1 | Timer 0 Period Register 1  |
| 1813h            | TIMPRD2 | Timer 0 Period Register 2  |
| 1814h            | TIMCNT1 | Timer 0 Counter Register 1 |
| 1815h            | TIMCNT2 | Timer 0 Counter Register 2 |

**Table 5-43. General-Purpose Timer 1 Registers**

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION       |
|------------------|---------|----------------------------|
| 1850h            | TCR     | Timer 1 Control Register   |
| 1852h            | TIMPRD1 | Timer 1 Period Register 1  |
| 1853h            | TIMPRD2 | Timer 1 Period Register 2  |
| 1854h            | TIMCNT1 | Timer 1 Counter Register 1 |
| 1855h            | TIMCNT2 | Timer 1 Counter Register 2 |

**Table 5-44. General-Purpose Timer 2 Registers**

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION       |
|------------------|---------|----------------------------|
| 1890h            | TCR     | Timer 2 Control Register   |
| 1892h            | TIMPRD1 | Timer 2 Period Register 1  |
| 1893h            | TIMPRD2 | Timer 2 Period Register 2  |
| 1894h            | TIMCNT1 | Timer 2 Counter Register 1 |
| 1895h            | TIMCNT2 | Timer 2 Counter Register 2 |

### 5.6.21 General-Purpose Input and Output

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. The GPIO can also send interrupts to the CPU.

The GPIO peripheral supports the following:

- 32 GPIO pins and 3 special-purpose outputs for use with SAR
  - Configure up to 20 GPIO pins simultaneously
- Each GPIO pin has internal pulldowns (IPDs) which can be individually disabled
- Each GPIO pin can be configured to generate edge detected interrupts to the CPU on either the rising or falling edge

The device GPIO pin functions are multiplexed with various other signals. For more detailed information on what signals are multiplexed with the GPIO and how to configure them, see [Section 4.2, Terminal Functions](#) and [Section 6, Device Configuration](#) of this document.

### 5.6.21.1 General-Purpose Input and Output Peripheral Register Descriptions

The external parallel port interface includes a 16-bit general purpose I/O that can be individually programmed as input or output with interrupt capability. Control of the general purpose I/O is maintained through a set of I/O memory-mapped registers listed in [Table 5-45](#).

**Table 5-45. GPIO Registers**

| HEX ADDRESS RANGE | ACRONYM    | REGISTER NAME                                 |
|-------------------|------------|---|
| 1C06h             | IODIR1     | GPIO Direction Register 1                     |
| 1C07h             | IODIR2     | GPIO Direction Register 2                     |
| 1C08h             | IOINDATA1  | GPIO Data In Register 1                       |
| 1C09h             | IOINDATA2  | GPIO Data In Register 2                       |
| 1C0Ah             | IODATAOUT1 | GPIO Data Out Register 1                      |
| 1C0Bh             | IODATAOUT2 | GPIO Data Out Register 2                      |
| 1C0Ch             | IOINTEDG1  | GPIO Interrupt Edge Trigger Enable Register 1 |
| 1C0Dh             | IOINTEDG2  | GPIO Interrupt Edge Trigger Enable Register 2 |
| 1C0Eh             | IOINTEN1   | GPIO Interrupt Enable Register 1              |
| 1C0Fh             | IOINTEN2   | GPIO Interrupt Enable Register 2              |
| 1C10h             | IOINTFLG1  | GPIO Interrupt Flag Register 1                |
| 1C11h             | IOINTFLG2  | GPIO Interrupt Flag Register 2                |



### 5.6.21.2 GPIO Peripheral Input and Output Electrical Data and Timing

Table 5-46 and Table 5-47 lists the timing and switching requirements for GPIO, respectively.

**Table 5-46. Timing Requirements for GPIO Inputs<sup>(1)</sup> (see Figure 5-37)**

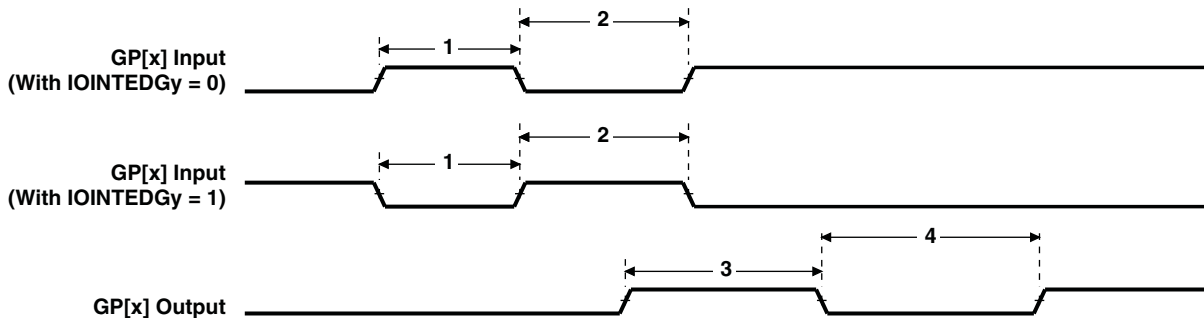
| NO. |                          |  | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|--------------------------|--|---|-----|------|
|     |                          |  | MIN   | MAX |      |
| 1   | t <sub>w(ACTIVE)</sub>   | Pulse duration, GPIO input and external interrupt pulse active   | 2C <sup>(1) (2)</sup>                                 |     | ns   |
| 2   | t <sub>w(INACTIVE)</sub> | Pulse duration, GPIO input and external interrupt pulse inactive | C <sup>(1) (2)</sup>                                  |     | ns   |

- (1) The pulse width given is sufficient to get latched into the GPIO\_IFR register and to generate an interrupt. If you want the device recognize the GPIO changes through software polling of the GPIO Data In (GPIO\_DIN) register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
- (2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

**Table 5-47. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-37)**

| NO. | PARAMETER            | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|----------------------|---|-----|------|
|     |                      | MIN   | MAX |      |
| 3   | t <sub>w(GPOH)</sub> | 3C <sup>(1) (2)</sup>                                 |     | ns   |
| 4   | t <sub>w(GPOL)</sub> | 3C <sup>(1) (2)</sup>                                 |     | ns   |

- (1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
- (2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.



**Figure 5-37. GPIO Port Timing**

### 5.6.21.3 GPIO Peripheral Input Latency Electrical Data and Timing

Table 5-48 lists the timing requirements for GPIO input latency.

**Table 5-48. Timing Requirements for GPIO Input Latency<sup>(1)</sup>**

| NO. |                     |                      | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |     | UNIT |     |
|-----|---------------------|----------------------|---|-----|------|-----|
|     |                     |                      | MIN   | MAX |      |     |
| 1   | t <sub>L(GPI)</sub> | Latency, GP[x] input | Polling GPIO_DIN register                             |     | 5    | cyc |
|     |                     |                      | Polling GPIO_IFR register                             |     | 7    | cyc |
|     |                     |                      | Interrupt detection                                   |     | 8    | cyc |

- (1) The pulse width given is sufficient to generate a CPU interrupt. However, if a user wants to have the device recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow device enough time to access the GPIO register through the internal bus.

## 5.6.22 IEEE 1149.1 JTAG

The JTAG interface is used for boundary-scan testing and emulation of the device.

$\overline{\text{TRST}}$  should only to be deasserted when it is necessary to use a JTAG controller to debug the device or exercise the boundary-scan functionality of the device.

The device includes an internal pulldown (IPD) on the  $\overline{\text{TRST}}$  pin to ensure that  $\overline{\text{TRST}}$  will always be asserted upon power up and the internal emulation logic of the device will always be properly initialized. TI also recommends an external pulldown to ensure proper device operation when an emulation or boundary-scan JTAG controller is not connected to the JTAG pins. JTAG controllers from TI actively drive  $\overline{\text{TRST}}$  high. However, some third-party JTAG controllers may not drive  $\overline{\text{TRST}}$  high but expect the use of a pullup resistor on  $\overline{\text{TRST}}$ . When using this type of JTAG controller, assert  $\overline{\text{TRST}}$  to initialize the device after powerup and externally drive  $\overline{\text{TRST}}$  high before trying any emulation or boundary-scan operations. The device will not operate properly if  $\overline{\text{TRST}}$  is not asserted low during power up.

### 5.6.22.1 JTAG ID (JTAGID) Register Descriptions

The JTAGID register is shown in [Table 5-49](#) and [Figure 5-38](#) and described in [Table 5-50](#).

**Table 5-49. JTAG ID Register**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME                | COMMENTS  |
|-------------------|---------|------------------------------|---|
| N/A               | JTAGID  | JTAG Identification Register | Read-only. Provides 32-bit JTAG ID of the device. |

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. The register hex value for the device is: 0x1B8F E02F. For the actual register bit names and their associated bit field descriptions, see [Figure 5-38](#) and [Table 5-50](#).

| 31-28           | 27-12                 | 11-1                  | 0   |
|-----------------|-----------------------|-----------------------|-----|
| VARIANT (4-Bit) | PART NUMBER (16-Bit)  | MANUFACTURER (11-Bit) | LSB |
| R-0001          | R-1011 1000 1111 1110 | R-0000 0010 111       | R-1 |

LEGEND: R = Read, W = Write, n = value at reset

**Figure 5-38. JTAG ID Register Description — 0x1B8F E02F**

**Table 5-50. JTAG ID Register Selection Bit Descriptions**

| BIT   | NAME         | DESCRIPTION                                      |
|-------|--------------|--|
| 31:28 | VARIANT      | Variant (4-bit) value: 0001.                     |
| 27:12 | PART NUMBER  | Part Number (16-bit) value: 1011 1000 1111 1110. |
| 11:1  | MANUFACTURER | Manufacturer (11-bit) value: 0000 0010 111.      |
| 0     | LSB          | LSB. This bit is read as 1.                      |

**5.6.22.2 JTAG Test\_port Electrical Data and Timing**

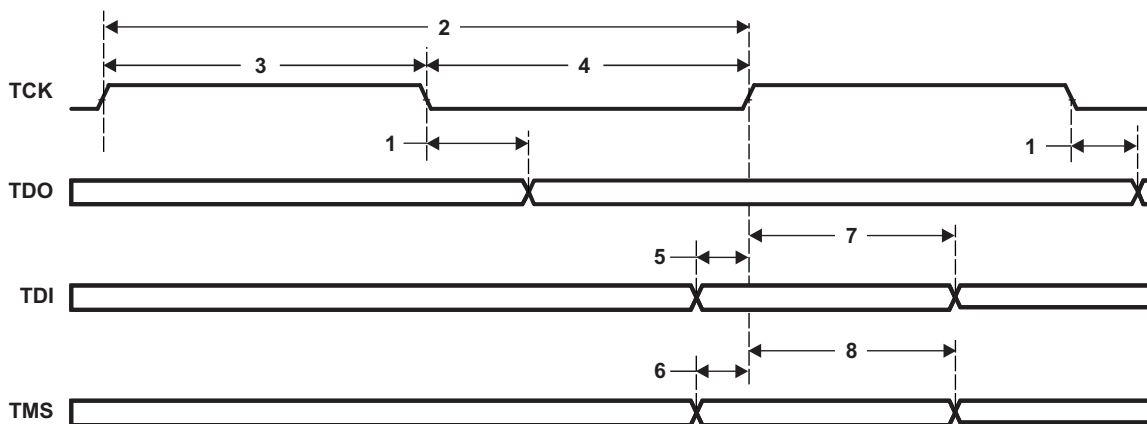
Table 5-51 and Table 5-52 list the timing and switching requirements for JTAG test port.

**Table 5-51. Timing Requirements for JTAG Test Port (see Figure 5-39)**

| NO. | PARAMETER                   | DESCRIPTION                           | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |     | UNIT |
|-----|-----------------------------|---------------------------------------|---|-----|------|
|     |                             |                                       | MIN   | MAX |      |
| 2   | t <sub>c</sub> (TCK)        | Cycle time, TCK                       | 60  |     | ns   |
| 3   | t <sub>w</sub> (TCKH)       | Pulse duration, TCK high              | 24  |     | ns   |
| 4   | t <sub>w</sub> (TCKL)       | Pulse duration, TCK low               | 24  |     | ns   |
| 5   | t <sub>su</sub> (TDIV-TCKH) | Setup time, TDI valid before TCK high | 10  |     | ns   |
| 6   | t <sub>su</sub> (TMSV-TCKH) | Setup time, TMS valid before TCK high | 6   |     | ns   |
| 7   | t <sub>h</sub> (TCKH-TDIV)  | Hold time, TDI valid after TCK high   | 5   |     | ns   |
| 8   | t <sub>h</sub> (TCKH-TDIV)  | Hold time, TMS valid after TCK high   | 4   |     | ns   |

**Table 5-52. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-39)**

| NO. | PARAMETER                  | DESCRIPTION                      | CV <sub>DD</sub> = 1.05 V<br>CV <sub>DD</sub> = 1.3 V |      | UNIT |
|-----|----------------------------|----------------------------------|---|------|------|
|     |                            |                                  | MIN   | MAX  |      |
| 1   | t <sub>d</sub> (TCKL-TDOV) | Delay time, TCK low to TDO valid |   | 30.5 | ns   |



**Figure 5-39. JTAG Test-Port Timing**

## 6 Detailed Description

### 6.1 C55x CPU

The fixed-point digital signal processors (DSPs) are based on the C55x CPU 3.3 generation processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, three data read buses (one 32-bit data read bus and two 16-bit data read buses), two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four data reads and two data writes in a single cycle. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-and-accumulate (MAC) units, each capable of 17-bit × 17-bit multiplication in a single cycle. A central 40-bit arithmetic and logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The instruction unit (IU) performs 32-bit program fetches from internal or external memory, stores them in a 128-byte instruction buffer queue, and queues instructions for the program unit (PU). The PU decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instruction calls.

For more detailed information on the CPU, see the *TMS320C55x CPU 3.0 CPU Reference Guide (SWPU073)*.

#### 6.1.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is in the byte address range 000000h to 00FFFFh and is composed of eight blocks of 4K words each (see [Table 6-1](#)). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). The DARAM can be accessed by the internal program, data, or DMA buses.

**Table 6-1. DARAM Blocks**

| CPU<br>BYTE ADDRESS RANGE | DMA CONTROLLER<br>BYTE ADDRESS RANGE | MEMORY BLOCK           |
|---------------------------|--------------------------------------|------------------------|
| 000000h to 001FFFh        | 0001 0000h to 0001 1FFFh             | DARAM 0 <sup>(1)</sup> |
| 002000h to 003FFFh        | 0001 2000h to 0001 3FFFh             | DARAM 1                |
| 004000h to 005FFFh        | 0001 4000h to 0001 5FFFh             | DARAM 2                |
| 006000h to 007FFFh        | 0001 6000h to 0001 7FFFh             | DARAM 3                |
| 008000h to 009FFFh        | 0001 8000h to 0001 9FFFh             | DARAM 4                |
| 00A000h to 00BFFFh        | 0001 A000h to 0001 BFFFh             | DARAM 5                |
| 00C000h to 00DFFFh        | 0001 C000h to 0001 DFFFh             | DARAM 6                |
| 00E000h to 00FFFFh        | 0001 E000h to 0001 FFFFh             | DARAM 7                |

(1) The first 192 bytes are reserved for memory-mapped registers (MMRs). See [Section 6.2, Memory Map Summary](#).

## 6.1.2 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE0000h to FFFFFFFh. The ROM is composed of four 16K-word blocks, for a total of 128KB of ROM. The ROM address space can be mapped by software to the internal ROM.

The standard device includes a bootloader program resident in the ROM.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range FE0000h to FFFFFFFh is reserved for the on-chip ROM. When software sets the MPNMC bit field of the ST3 status register, the on-chip ROM is disabled and not present in the memory map, and byte address range FE0000h to FFFFFFFh is unmapped. A hardware reset always clears the MPNMC bit, so the ROM at reset cannot be disabled. The software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the program and data buses. Each on-chip ROM block is a one cycle per word access memory.

## 6.1.3 On-Chip Single-Access RAM (SARAM)

### 6.1.3.1 SARAM

The SARAM is located at the byte address range 010000h to 04FFFFFFh and is composed of 32 blocks of 4K words each (see [Table 6-2](#)). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses.

SARAM is also accessed by the USB and LCD DMA buses.

**Table 6-2. SARAM Blocks**

| CPU<br>BYTE ADDRESS RANGE | DMA and USB CONTROLLER<br>BYTE ADDRESS RANGE | MEMORY BLOCK |
|---------------------------|--|--------------|
| 010000h to 011FFFh        | 0009 0000h to 0009 1FFFh                     | SARAM 0      |
| 012000h to 013FFFh        | 0009 2000h to 0009 3FFFh                     | SARAM 1      |
| 014000h to 015FFFh        | 0009 4000h to 0009 5FFFh                     | SARAM 2      |
| 016000h to 017FFFh        | 0009 6000h to 0009 7FFFh                     | SARAM 3      |
| 018000h to 019FFFh        | 0009 8000h to 0009 9FFFh                     | SARAM 4      |
| 01A000h to 01BFFFh        | 0009 A000h to 0009 BFFFh                     | SARAM 5      |
| 01C000h to 01DFFFh        | 0009 C000h to 0009 DFFFh                     | SARAM 6      |
| 01E000h to 01FFFFh        | 0009 E000h to 0009 FFFFh                     | SARAM 7      |
| 020000h to 021FFFh        | 000A 0000h to 000A 1FFFh                     | SARAM 8      |
| 022000h to 023FFFh        | 000A 2000h to 000A 3FFFh                     | SARAM 9      |
| 024000h to 025FFFh        | 000A 4000h to 000A 5FFFh                     | SARAM 10     |
| 026000h to 027FFFh        | 000A 6000h to 000A 7FFFh                     | SARAM 11     |
| 028000h to 029FFFh        | 000A 8000h to 000A 9FFFh                     | SARAM 12     |
| 02A000h to 02BFFFh        | 000A A000h to 000A BFFFh                     | SARAM 13     |
| 02C000h to 02DFFFh        | 000A C000h to 000A DFFFh                     | SARAM 14     |
| 02E000h to 02FFFFh        | 000A E000h to 000A FFFFh                     | SARAM 15     |
| 030000h to 031FFFh        | 000B 0000h to 000B 1FFFh                     | SARAM 16     |
| 032000h to 033FFFh        | 000B 2000h to 000B 3FFFh                     | SARAM 17     |
| 034000h to 035FFFh        | 000B 4000h to 000B 5FFFh                     | SARAM 18     |
| 036000h to 037FFFh        | 000B 6000h to 000B 7FFFh                     | SARAM 19     |
| 038000h to 039FFFh        | 000B 8000h to 000B 9FFFh                     | SARAM 20     |
| 03A000h to 03BFFFh        | 000B A000h to 000B BFFFh                     | SARAM 21     |
| 03C000h to 03DFFFh        | 000B C000h to 000B DFFFh                     | SARAM 22     |
| 03E000h to 03FFFFh        | 000B E000h to 000B FFFFh                     | SARAM 23     |

**Table 6-2. SARAM Blocks (continued)**

| CPU<br>BYTE ADDRESS RANGE | DMA and USB CONTROLLER<br>BYTE ADDRESS RANGE | MEMORY BLOCK            |
|---------------------------|--|-------------------------|
| 040000h to 041FFFh        | 000C 0000h to 000C 1FFFh                     | SARAM 24                |
| 042000h to 043FFFh        | 000C 2000h to 000C 3FFFh                     | SARAM 25                |
| 044000h to 045FFFh        | 000C 4000h to 000C 5FFFh                     | SARAM 26                |
| 046000h to 047FFFh        | 000C 6000h to 000C 7FFFh                     | SARAM 27                |
| 048000h to 049FFFh        | 000C 8000h to 000C 9FFFh                     | SARAM 28                |
| 04A000h to 04BFFFh        | 000C A000h to 000C BFFFh                     | SARAM 29                |
| 04C000h to 04DFFFh        | 000C C000h to 000C DFFFh                     | SARAM 30                |
| 04E000h to 04FFFFh        | 000C E000h to 000C FFFFh                     | SARAM 31 <sup>(1)</sup> |

(1) SARAM31 (byte address range: 0x4E000 to 0x4EFFF) is reserved for the bootloader. After the boot process completes, this memory space can be used.

### 6.1.4 I/O Memory

Each device includes a 64-KB I/O space for the memory-mapped registers of the DSP peripherals and system registers used for idle control, status monitoring, and system configuration. I/O space is separate from program and memory space and is accessed with separate instruction opcodes or through the DMAs.

[Table 6-3](#) lists the memory-mapped registers of each device. Not all addresses in the 64-KB I/O space are used; these addresses must be treated as reserved and not accessed by the CPU or DMA. For the expanded tables of each peripheral, see [Section 5.6, Peripheral Information and Electrical Specifications](#) of this document.

Some DMA controllers have access to the I/O-Space memory-mapped registers of the following peripherals registers: I2C, UART, I2S, SD, USB, and SAR ADC.

Before accessing any peripheral memory-mapped register, ensure the peripheral being accessed is not held in reset through the Peripheral Reset Control Register (PRCR) and its internal clock is enabled through the Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2).

**Table 6-3. Peripheral I/O-Space Control Registers**

| WORD ADDRESS                              | PERIPHERAL   |
|---|--------------|
| 0x0000 to 0x0004                          | Idle Control |
| 0x0005 to 0x000D through 0x0803 to 0x0BFF | Reserved     |
| 0x0C00 to 0x0C7F                          | DMA0         |
| 0x0C80 to 0x0CFF                          | Reserved     |
| 0x0D00 to 0x0D7F                          | DMA1         |
| 0x0D80 to 0x0DFF                          | Reserved     |
| 0x0E00 to 0x0E7F                          | DMA2         |
| 0x0E80 to 0x0EFF                          | Reserved     |
| 0x0F00 to 0x0F7F                          | DMA3         |
| 0x0F80 to 0x17FF                          | Reserved     |
| 0x1800 to 0x181F                          | Timer0       |
| 0x1820 to 0x183F                          | Reserved     |
| 0x1840 to 0x185F                          | Timer1       |
| 0x1860 to 0x187F                          | Reserved     |
| 0x1880 to 0x189F                          | Timer2       |
| 0x1900 to 0x197F                          | RTC          |
| 0x1980 to 0x19FF                          | Reserved     |

**Table 6-3. Peripheral I/O-Space Control Registers (continued)**

| WORD ADDRESS                              | PERIPHERAL                       |
|---|----------------------------------|
| 0x1A00 to 0x1A6C                          | I2C                              |
| 0x1A6D to 0x1AFF                          | Reserved                         |
| 0x1B00 to 0x1B1F                          | UART                             |
| 0x1B80 to 0x1BFF                          | Reserved                         |
| 0x1C00 to 0x1CFF                          | System Control                   |
| 0x1D00 to 0x1FFF through 0x2600 to 0x27FF | Reserved                         |
| 0x2800 to 0x2840                          | I2S0                             |
| 0x2900 to 0x2940                          | I2S1                             |
| 0x2A00 to 0x2A40                          | I2S2                             |
| 0x2B00 to 0x2B40                          | I2S3                             |
| 0x2C41 to 0x2DFF                          | Reserved                         |
| 0x2E00 to 0x2E40                          | LCD                              |
| 0x2E41 to 0x2FFF                          | Reserved                         |
| 0x3000 to 0x300F                          | SPI                              |
| 0x3010 to 0x39FF                          | Reserved                         |
| 0x3A00 to 0x3A7F                          | SD0                              |
| 0x3A80 to 0x3AFF                          | Reserved                         |
| 0x3B00 to 0x3B7F                          | SD1                              |
| 0x3B80 to 0x6FFF                          | Reserved                         |
| 0x7000 to 0x70FF                          | SAR and Analog Control Registers |
| 0x7100 to 0x7FFF                          | Reserved                         |
| 0x8000 to 0xFFFF                          | USB                              |

## 6.2 Memory Map Summary

The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. There are eight blocks of 8KB of dual-access RAM and thirty-two blocks of 8KB of single-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle.

The DSP memory can be accessed by different master modules within the DSP. These master modules include the C55x CPU, the four DMA controllers, LCD, and CDMA of the USB (see [Figure 6-1](#)).

| CPU BYTE ADDRESS <sup>(A)</sup> | DMA/USB/LCD BYTE ADDRESS <sup>(A)</sup> | MEMORY BLOCKS                 | BLOCK SIZE                |
|---------------------------------|---|-------------------------------|---------------------------|
| 000000h                         | 0001 0000h                              | MMR (Reserved) <sup>(B)</sup> |                           |
| 0000C0h                         | 0001 00C0h                              | DARAM <sup>(C)</sup>          | 64K Minus 192 bytes       |
| 010000h                         | 0009 0000h                              | SARAM                         | 256KB                     |
| 050000h                         | 0100 0000h                              | Reserved                      |                           |
| FE0000h                         | 050E 0000h                              | ROM (if MPNMC=0)              | Unmapped (if MPNMC=1)     |
| FFFFFFh                         | 050F FFFFh                              | Reserved (if MPNMC=1)         | 128KB of ROM (if MPNMC=0) |

- A. Address shown represents the first byte address in each block.
- B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
- C. The USB and LCD controllers do not have access to DARAM.

**Figure 6-1. Memory Map Summary**



### 6.3 System Registers

The system registers configure the device and monitor its status. Brief descriptions of the various system registers are provided in [Table 6-4](#).

**Table 6-4. Idle Control, Status, and System Registers**

| CPU WORD ADDRESS | ACRONYM                | REGISTER DESCRIPTION                                   | COMMENTS                                |
|------------------|------------------------|--|---|
| 0001h            | ICR                    | Idle Control Register                                  |   |
| 0002h            | ISTR                   | Idle Status Register                                   |   |
| 1C00h            | EBSR                   | External Bus Selection Register                        | See <a href="#">Section 6.6.1</a> .     |
| 1C02h            | PCGCR1                 | Peripheral Clock Gating Control Register 1             |   |
| 1C03h            | PCGCR2                 | Peripheral Clock Gating Control Register 2             |   |
| 1C04h            | PSRCR                  | Peripheral Software Reset Counter Register             |   |
| 1C05h            | PRCR                   | Peripheral Reset Control Register                      |   |
| 1C14h            | TIAFR                  | Timer Interrupt Aggregation Flag Register              |   |
| 1C16h            | ODSCR                  | Output Drive Strength Control Register                 |   |
| 1C17h            | PDINHIBR1              | Pulldown Inhibit Register 1                            |   |
| 1C18h            | PDINHIBR2              | Pulldown Inhibit Register 2                            |   |
| 1C19h            | PDINHIBR3              | Pulldown Inhibit Register 3                            |   |
| 1C1Ah            | DMA0CESR1              | DMA0 Channel Event Source Register 1                   |   |
| 1C1Bh            | DMA0CESR2              | DMA0 Channel Event Source Register 2                   |   |
| 1C1Ch            | DMA1CESR1              | DMA1 Channel Event Source Register 1                   |   |
| 1C1Dh            | DMA1CESR2              | DMA1 Channel Event Source Register 2                   |   |
| 1C28h            | RAMSLPMDCNTRLR1        | RAM Sleep Mode Control Register 1                      |   |
| 1C2Ah            | RAMSLPMDCNTRLR2        | RAM Sleep Mode Control Register 2                      |   |
| 1C2Bh            | RAMSLPMDCNTRLR3        | RAM Sleep Mode Control Register 3                      |   |
| 1C2Ch            | RAMSLPMDCNTRLR4        | RAM Sleep Mode Control Register 4                      |   |
| 1C2Dh            | RAMSLPMDCNTRLR5        | RAM Sleep Mode Control Register 5                      |   |
| 1C30h            | DMAIFR                 | DMA Interrupt Flag Aggregation Register                |   |
| 1C31h            | DMAIER                 | DMA Interrupt Enable Register                          |   |
| 1C32h            | USBSCR                 | USB System Control Register                            |   |
| 1C36h            | DMA2CESR1              | DMA2 Channel Event Source Register 1                   |   |
| 1C37h            | DMA2CESR2              | DMA2 Channel Event Source Register 2                   |   |
| 1C38h            | DMA3CESR1              | DMA3 Channel Event Source Register 1                   |   |
| 1C39h            | DMA3CESR2              | DMA3 Channel Event Source Register 2                   |   |
| 1C3Ah            | CLKSTOP                | Peripheral Clock Stop Request and Acknowledge Register |   |
| 1C40h            | DIEIDR0 <sup>(1)</sup> | Die ID Register 0                                      |   |
| 1C41h            | DIEIDR1 <sup>(1)</sup> | Die ID Register 1                                      |   |
| 1C42h            | DIEIDR2 <sup>(1)</sup> | Die ID Register 2                                      |   |
| 1C43h            | DIEIDR3 <sup>(1)</sup> | Die ID Register 3                                      |   |
| 1C44h            | DIEIDR4 <sup>(1)</sup> | Die ID Register 4                                      |   |
| 1C45h            | DIEIDR5 <sup>(1)</sup> | Die ID Register 5                                      |   |
| 1C46h            | DIEIDR6 <sup>(1)</sup> | Die ID Register 6                                      |   |
| 1C47h            | DIEIDR7 <sup>(1)</sup> | Die ID Register 7                                      |   |
| 7004h            | LDOCNTL                | LDO Control Register                                   | See <a href="#">Section 5.6.1.1.3</a> . |

(1) This register is reserved.

## 6.4 Boot Sequence

The boot sequence is when the on-chip memory of the device is loaded with program and data sections from an external image file (in flash memory, for example). The boot sequence lets you program some internal registers of the device with predetermined values. The boot sequence is started automatically after each device reset. For more details on device reset, see [Section 5.6.9, Reset](#).

There are several methods by which the memory and register initialization can occur. Each of these methods is referred to as a boot mode. At reset, the device cycles through different boot modes until it finds an image with a valid boot signature. The on-chip bootloader allows the DSP registers to be configured during the boot process, if the optional register configuration section is present in the boot image (see [Figure 6-2](#)). For more information on the boot modes supported, see [Section 6.4.1, Boot Modes](#).

After reset, the CPU gets the reset vector from 0xFFFF00. MP or  $\overline{MC}$  is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.

The device bootloader follows the following steps (see [Figure 6-2](#).)

1. After reset, the CPU gets the reset vector from 0xFFFF00. MP or MC is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals, MPORT, and HWA.
4. If CLK\_SEL = 0, the bootloader powers up the PLL and sets its output frequency to 12.288 MHz (with a 375x multiplier using VP = 749, VS = 0, input divider disabled, output divide-by-8 enabled, and output divider enabled with VO = 0). If CLK\_SEL = 1, the bootloader keeps the PLL bypassed. Enable Timer0 to count the settling time of BG\_CAP
5. Apply manufacturing trim to the bandgap references.
6. Disable CLKOUT.
7. Test for the 16-bit and 24-bit SPI EEPROM boot on SPI\_CS[0] with a 500-kHz clock rate and set to parallel port mode on the EBSR to 5, then set to 6:
  - (a) Check the first 2 bytes read from boot table for a boot signature match using 16-bit address mode.
  - (b) If the boot signature is not valid, read the first 2 bytes again using 24-bit address mode.
  - (c) If the boot signature is not valid from either case (16-bit and 24-bit address modes), go to Step 8.
  - (d) Set Register Configuration, if present in boot image.
  - (e) Attempt SPI Serial Memory boot, go to Step 12.
8. Test for I2C EEPROM boot with a 7-bit slave address 0x50 and 400-kHz clock rate.
  - (a) Check the first 2 bytes read from boot table for a boot signature match.
  - (b) If the boot signature is not valid, go to Step 9.
  - (c) Set Register Configuration, if present in boot image.
  - (d) Attempt I2C EEPROM boot, go to Step 12.
9. Test for eMMC partitions, eMMC, SD0 boot:
  - For an eMMC, SD, or SDHC card, the card must be formatted to FAT16 or FAT32. The boot image file must be renamed bootimg.bin and copied to the foot directory of the formatted card.
  - If an eMMC boot partition is desired (for only eMMC 4.3 and up), then the boot image file must be programmed to one of the two boot partitions (1 or 2) on the eMMC card. PARTITION\_CONFIG in the EXT\_CSD must be set accordingly.
  - If the boot signature is found, attempt eMMC, SD, or SDHC boot and go to Step 12. If boot signature is not found, go to Step 10.
10. Set the PLL output to approximately 36 MHz. If CLK\_SEL = 1, CLKIN multiplied by 3x. If CLK\_SEL = 0, CLKIN is multiplied by 1125x. Re-enable TIMER0 to start counting the settling time of BG\_CAP due to the PLL change.

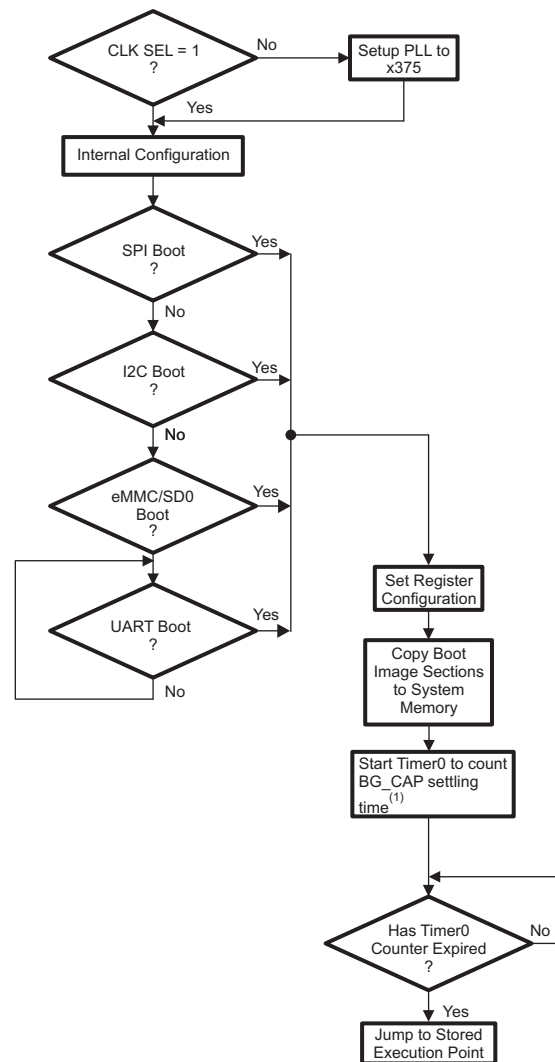
11. Test for UART or USB boot:

- The USB internal LDO will be enabled and the device is configured to accept a boot image on EP1 OUT.
- UART will be set to 57600 baud, 8 bit, 1 stop bit, CTS or RTS auto flow control, and odd parity will be enabled to accept a boot image from the UART transmitter.
- The device will poll UART and USB in turns. If a valid boot signature is detected on either device, a boot image will attempt to download on that device. Go to Step 12. If a valid signature is not detected, return to the start of this step.

12. Copy the boot image sections to system memory.

13. Verify the settling time of BG\_CAP has elapsed before executing application code.

14. Jump to the entry point specified in the boot image.



(1) See settling time of BG\_CAP in Table 4-14.

Figure 6-2. Bootloader Software Architecture

### 6.4.1 Boot Modes

The DSP supports the following boot modes in the following device order: SPI 16-bit EEPROM, SPI 24-bit Flash, I2C EEPROM, and eMMC boot partition, eMMC, SD or SDHC card. The boot mode is determined by checking for a valid boot signature on each supported boot device. The first boot device with a valid boot signature will be used to load and execute the user code. If none of the supported boot devices have a valid boot signature, the bootloader goes into an endless loop checking the UART or USB boot mode and the device must be reset to search for another valid boot image in the supported boot modes.

**Note:** For detailed information on eMMC boot partition, eMMC, SD, or SDHC and UART or USB boot modes, contact your local sales representative.

### 6.4.2 Boot Configuration

After reset, the on-chip bootloader programs the system clock generator based on the input clock selected through the CLK\_SEL pin. If CLK\_SEL = 0, the bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375). If CLK\_SEL = 1, the bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin.

**Note:**

- When CLK\_SEL = 1, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz.
- The on-chip bootloader allows for DSP registers to be configured during the boot process. However, this feature must not be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG\_CAP settling time. The bootloader register modification feature must not modify the PLL or Timer0 registers.

After hardware reset, the DSP boots through the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clocks will be enabled for the query and then disabled when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR will be idled except the CPU domain.

### 6.4.3 DSP Resources Used By the Bootloader

The bootloader uses SARAM block 31 for the storing of temporary data. This block of memory is reserved during the boot process. After the boot process is complete, it can be used by the user application.

## 6.5 Configurations at Reset

Some device configurations are determined at reset. The following subsections give more details.

### 6.5.1 Device and Peripheral Configurations at Device Reset

Table 6-5 summarizes the device boot and configuration pins that are required to be statically tied high, tied low, or remain unconnected during device operation. For proper operation, a device reset must be initiated after changing any of these pin functions.

**Table 6-5. Default Functions Affected by Device Configuration Pins**

| CONFIGURATION PINS               | SIGNAL NO. | IPU and IPD | FUNCTIONAL DESCRIPTION   |
|----------------------------------|------------|-------------|--|
| $\overline{\text{DSP\_LDO\_EN}}$ | M12        | –           | <p>DSP_LDO enable input.</p> <p>This signal is not intended to be dynamically switched.</p> <p>0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V according to the DSP_LDO_V bit in the LDOCNTL register, see Figure 5-2). At power-on reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the RESET pin.</p> <p>1 = DSP_LDO is disabled and the DSP_LDOO pin is in a high-impedance (Hi-Z) state. The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The RESET pin will act as the sole reset source for the device. If an external power supply is used to provide power to <math>\text{CV}_{\text{DD}}</math>, then <math>\overline{\text{DSP\_LDO\_EN}}</math> must be tied to LDOI, DSP_LDOO must be left unconnected, and the RESET pin must be asserted appropriately for device initialization after powerup.</p> <p><b>Note:</b> To pullup this pin, connect it to the same supply as LDOI pins.</p> |
| CLK_SEL                          | D12        | –           | <p>Clock input select.</p> <p>0 = 32-kHz on-chip oscillator drives the RTC timer and the system clock generator. CLKIN is ignored.</p> <p>1 = CLKIN drives the system clock generator and the 32-kHz on-chip oscillator drives only the RTC timer.</p> <p>This pin is not allowed to change during device operation; it must be tied to <math>\text{DV}_{\text{DDIO}}</math> or GND at the board.</p>  |

For proper device operation, external pullup and pulldown resistors may be required on these device configuration pins. For discussion on situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.

This device also has RESERVED pins that must be configured correctly for proper device operation (statically tied high, tied low, or remain unconnected at all times). For more details on these pins, see Table 4-15.

## 6.6 Configurations After Reset

The following sections provide details on configuring the device after reset. Multiplexed pin functions are selected by software after reset. For more details on multiplexed pin function control, see [Section 6.7, Multiplexed Pin Configurations](#).

### 6.6.1 External Bus Selection Register (EBSR)

The External Bus Selection Register (EBSR) determines the mapping of the LCD Controller, I2S2, I2S3, UART, SPI, and GPIO signals to 21 signals of the external parallel port pins. The EBSR also determines the mapping of the I2S or SD ports to serial port 0 pins and serial port pins. The EBSR is at port address 1C00h. Once the bit fields of this register are changed, the routing of the signals occurs on the next CPU clock cycle.

Before modifying the values of the EBSR, you must clock gate all affected peripherals through the PCGCR. After the EBSR has been modified, you must reset the peripherals before using them through the peripheral software reset counter register.

**Figure 6-3. External Bus Selection Register (EBSR) [1C00h]**

|          |          |    |    |         |    |         |   |
|----------|----------|----|----|---------|----|---------|---|
| 15       | 14       | 13 | 12 | 11      | 10 | 9       | 8 |
| Reserved | PPMODE   |    |    | SP1MODE |    | SP0MODE |   |
| R-0      | R/W-000  |    |    | R/W-00  |    | R/W-00  |   |
| 7        | 6        | 5  | 4  | 3       | 2  | 1       | 0 |
| Reserved | Reserved |    |    |         |    |         |   |
| R-0      | R-0      |    |    |         |    |         |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6-6. EBSR Register Bit Descriptions**

| BIT   | NAME     | DESCRIPTION  |
|-------|----------|--|
| 15    | RESERVED | Reserved. Read-only, writes have no effect.  |
| 14:12 | PPMODE   | Parallel port mode control bits. These bits control the pin multiplexing of the LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] pins on the parallel port. For more details, see <a href="#">Table 6-7</a> .         |
|       |          | 000 = Mode 0 (16-bit LCD Controller). All 20 signals of the LCD bridge module are routed to the 20 external signals of the parallel port.  |
|       |          | 001 = Mode 1 (SPI, GPIO, UART, and I2S2). 6 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 20 external signals of the parallel port.                 |
|       |          | 010 = Mode 2 (8-bit LCD Controller and GPIO). 8 bits of pixel data of the LCD controller module and 8 GPIO are routed to the 20 external signals of the parallel port.   |
|       |          | 011 = Mode 3 (8-bit LCD Controller, SPI and I2S3). 8 bits of pixel data of the LCD controller module, 4 signals of the SPI module and 4 signals of the I2S3 module are routed to the 20 external signals of the parallel port.   |
|       |          | 100 = Mode 4 (8-bit LCD Controller, I2S2 and UART). 8 bits of pixel data of the LCD controller module, 4 signals of the I2S2 module and 4 signals of the UART module are routed to the 20 external signals of the parallel port. |
|       |          | 101 = Mode 5 (8-bit LCD Controller, SPI and UART). 8 bits of pixel data of the LCD controller module, 4 signals of the SPI module and 4 signals of the UART module are routed to the 20 external signals of the parallel port.   |
|       |          | 110 = Mode 6 (SPI, I2S2, I2S3, and GPIO). 6 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, and 6 GPIO are routed to the 20 external signals of the parallel port.                        |
|       |          | 111 = Reserved.  |

**Table 6-6. EBSR Register Bit Descriptions (continued)**

| BIT   | NAME     | DESCRIPTION   |
|-------|----------|---|
| 11:10 | SP1MODE  | Serial port 1 mode control bits. The bits control the pin multiplexing of the SD1, I2S1, and GPIO pins on serial port 1.<br>For more details, see <a href="#">Table 6-8</a> .       |
|       |          | 00 = Mode 0 (SD1). All 6 signals of the SD1 module are routed to the 6 external signals of the serial port 1.   |
|       |          | 01 = Mode 1 (I2S1 and GP[11:10]). 4 signals of the I2S1 module and 2 GP[11:10] signals are routed to the 6 external signals of the serial port 1.                                   |
|       |          | 10 = Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1.  |
|       |          | 11 = Reserved.  |
| 9:8   | SP0MODE  | Serial port 0 mode control bits. The bits control the pin multiplexing of the SD0, I2S0, and GPIO pins on serial port 0.<br>For more details, see <a href="#">Section 6.7.1.3</a> . |
|       |          | 00 = Mode 0 (SD0). All 6 signals of the SD0 module are routed to the 6 external signals of the serial port 0.   |
|       |          | 01 = Mode 1 (I2S0 and GP[5:0]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0.                                       |
|       |          | 10 = Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0.  |
|       |          | 11 = Reserved.  |
| 7     | RESERVED | Reserved. Read-only, writes have no effect.   |
| 6     | RESERVED | Reserved. Read-only, writes have no effect.   |
| 5     | RESERVED | Reserved  |
| 4     | RESERVED | Reserved  |
| 3     | RESERVED | Reserved  |
| 2     | RESERVED | Reserved  |
| 1     | RESERVED | Reserved  |
| 0     | RESERVED | Reserved  |

### 6.6.2 LDO Control Register [7004h]

When the DSP\_LDO is enabled by the `DSP_LDO_EN` pin [M12], by default, the DSP\_LDOO voltage is set to 1.3 V. The DSP\_LDOO voltage can be programmed to be either 1.05 V or 1.3 V through the `DSP_LDO_V` bit (bit 1) in the LDO Control Register (LDOCNTL).

At reset, the USB\_LDO is turned off. The USB\_LDO can be enabled through the `USBLDOEN` bit (bit 0) in the LDOCNTL register.

For more detailed information on the LDOs, see [Section 5.6.1.1 LDO Configuration](#).

### 6.6.3 USB System Control Registers (USBSCR) [1C32h]

After reset, by default, the CPU performs 16-bit accesses to the USB register and data space. To perform 8-bit accesses to the USB data space, set the `BYTEMODE` bits to 01b for the high byte or 10b for the low byte in the USB System Control Register (USBSCR).

### 6.6.4 Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2) [1C02h and 1C03h]

After hardware reset, the DSP executes the on-chip bootloader from ROM. As the bootloader executes, it selectively enables the clock of the peripheral being queried for a valid boot. If a valid boot source is not found, the bootloader disables the clock to that peripheral and moves on to the next peripheral in the boot order. After the boot process is complete, all of the peripheral clocks will be off and all domains in the ICR, except for the CPU domain, will be idled (including the MPORT and HWA). The user must enable the clocks to the peripherals and CPU ports that are going to be used. `PCGCR1` and `PCGCR2` are used to enable and disable the peripheral clocks.



### 6.6.5 Pullup and Pulldown Inhibit Registers (PDINHIBR1, 2, and 3) [1C17h, 1C18h, and 1C19h]

Each internal pullup (IPU) and internal pulldown (IPD) resistor on the device DSP, except for the IPD on  $\overline{\text{TRST}}$ , can be individually controlled through the IPU and IPD registers (PDINHIBR1 [1C17h], PDINHIBR2 [1C18h], and PDINHIBR3 [1C19h]). To minimize power consumption, IPU or IPD resistors must be disabled in the presence of an external pullup or pulldown resistor or external driver. [Section 6.8.1, Pullup and Pulldown Resistors](#), describes other situations in which an pullup and pulldown resistors are required.

When  $\text{CV}_{\text{DD}}$  is powered down, pullup and pulldown resistors will be forced disabled and an internal bus-holder will be enabled. For more detailed information, see [Section 5.6.5.2, Digital I/O Behavior When Core Power \( \$\text{CV}\_{\text{DD}}\$ \) is Down](#).

### 6.6.6 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate control on the CLKOUT output pin. The OSRCR is used to set a subset of the device I/O pins, namely the CLKOUT pin, to either fast or slow slew rate. The slew rate feature is implemented by staging or delaying turnon times of the parallel P-channel drive transistors and parallel N-channel drive transistors of the output buffer. In the slow slew rate configuration, the delay is longer but the same number of parallel transistors are used to drive the output high or low. In the slow slew rate configuration, the drive strength is the same. The slower slew rate control can be used for power savings and has the greatest effect at lower  $\text{DV}_{\text{DDIO}}$  voltages.

## 6.7 Multiplexed Pin Configurations

The device DSP uses pin multiplexing to accommodate a larger number of peripheral functions in the smallest possible package, providing the ultimate flexibility for end applications. The EBSR controls all the pin multiplexing functions on the device.

### 6.7.1 Pin Multiplexing Details

This section discusses how to program the EBSR to select the desired peripheral functions and pin muxing. See the individual pin mux sections for pin muxing details for a specific muxed pin. After changing any of the pin mux control registers, it will be necessary to reset the peripherals that are affected.

#### 6.7.1.1 LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing [EBSR.PPMODE Bits]

The LCD controller, SPI, UART, I2S2, I2S3, and GPIO signal muxing is determined by the value of the PPMODE bit fields in the EBSR. For more details on the actual pin functions, see [Table 6-7](#).



**Table 6-7. LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing**

| PDINHIBR3 REGISTER BIT FIELDS <sup>(1)</sup> | PIN NAME                           | EBSR PPMODE BITS       |          |            |            |            |            |          |
|--|------------------------------------|------------------------|----------|------------|------------|------------|------------|----------|
|  |                                    | MODE 0                 | MODE 1   | MODE 2     | MODE 3     | MODE 4     | MODE 5     | MODE 6   |
|  |                                    | 000<br>(Reset default) | 001      | 010        | 011        | 100        | 101        | 110      |
|  | LCD_EN_RDB/SPI_CLK                 | LCD_EN_RDB             | SPI_CLK  | LCD_EN_RDB | LCD_EN_RDB | LCD_EN_RDB | LCD_EN_RDB | SPI_CLK  |
|  | LCD_D[0]/SPI_RX                    | LCD_D[0]               | SPI_RX   | LCD_D[0]   | LCD_D[0]   | LCD_D[0]   | LCD_D[0]   | SPI_RX   |
|  | LCD_D[1]/SPI_TX                    | LCD_D[1]               | SPI_TX   | LCD_D[1]   | LCD_D[1]   | LCD_D[1]   | LCD_D[1]   | SPI_TX   |
| P2PD   | LCD_D[2]/GP[12]                    | LCD_D[2]               | GP[12]   | LCD_D[2]   | LCD_D[2]   | LCD_D[2]   | LCD_D[2]   | GP[12]   |
| P3PD   | LCD_D[3]/GP[13]                    | LCD_D[3]               | GP[13]   | LCD_D[3]   | LCD_D[3]   | LCD_D[3]   | LCD_D[3]   | GP[13]   |
| P4PD   | LCD_D[4]/GP[14]                    | LCD_D[4]               | GP[14]   | LCD_D[4]   | LCD_D[4]   | LCD_D[4]   | LCD_D[4]   | GP[14]   |
| P5PD   | LCD_D[5]/GP[15]                    | LCD_D[5]               | GP[15]   | LCD_D[5]   | LCD_D[5]   | LCD_D[5]   | LCD_D[5]   | GP[15]   |
| P6PD   | LCD_D[6]/GP[16]                    | LCD_D[6]               | GP[16]   | LCD_D[6]   | LCD_D[6]   | LCD_D[6]   | LCD_D[6]   | GP[16]   |
| P7PD   | LCD_D[7]/GP[17]                    | LCD_D[7]               | GP[17]   | LCD_D[7]   | LCD_D[7]   | LCD_D[7]   | LCD_D[7]   | GP[17]   |
| P8PD   | LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK   | LCD_D[8]               | I2S2_CLK | GP[18]     | SPI_CLK    | I2S2_CLK   | SPI_CLK    | I2S2_CLK |
| P9PD   | LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0    | LCD_D[9]               | I2S2_FS  | GP[19]     | SPI_CS0    | I2S2_FS    | SPI_CS0    | I2S2_FS  |
| P10PD  | LCD_D[10]/I2S2_RX/GP[20]/SPI_RX    | LCD_D[10]              | I2S2_RX  | GP[20]     | SPI_RX     | I2S2_RX    | SPI_RX     | I2S2_RX  |
| P11PD  | LCD_D[11]/I2S2_DX/GP[27]/SPI_TX    | LCD_D[11]              | I2S2_DX  | GP[27]     | SPI_TX     | I2S2_DX    | SPI_TX     | I2S2_DX  |
| P12PD  | LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK | LCD_D[12]              | UART_RTS | GP[28]     | I2S3_CLK   | UART_RTS   | UART_RTS   | I2S3_CLK |
| P13PD  | LCD_D[13]/UART_CTS/GP[29]/I2S3_FS  | LCD_D[13]              | UART_CTS | GP[29]     | I2S3_FS    | UART_CTS   | UART_CTS   | I2S3_FS  |
| P14PD  | LCD_D[14]/UART_RXD/GP[30]/I2S3_RX  | LCD_D[14]              | UART_RXD | GP[30]     | I2S3_RX    | UART_RXD   | UART_RXD   | I2S3_RX  |
| P15PD  | LCD_D[15]/UART_TXD/GP[31]/I2S3_DX  | LCD_D[15]              | UART_TXD | GP[31]     | I2S3_DX    | UART_TXD   | UART_TXD   | I2S3_DX  |
|  | LCD_CS0_E0/SPI_CS0                 | LCD_CS0_E0             | SPI_CS0  | LCD_CS0_E0 | LCD_CS0_E0 | LCD_CS0_E0 | LCD_CS0_E0 | SPI_CS0  |
|  | LCD_RW_WRB/SPI_CS2                 | LCD_RW_WRB             | SPI_CS2  | LCD_RW_WRB | LCD_RW_WRB | LCD_RW_WRB | LCD_RW_WRB | SPI_CS2  |
|  | LCD_RS/SPI_CS3                     | LCD_RS                 | SPI_CS3  | LCD_RS     | LCD_RS     | LCD_RS     | LCD_RS     | SPI_CS3  |

(1) The pin names with PDINHIBR3 register bit field references can have the pulldown resistor enabled or disabled through this register.

### 6.7.1.2 SD1, I2S1, and GP[11:6] Pin Multiplexing [EBSR.SP1MODE Bits]

The SD1, I2S1, and GPIO signal muxing is determined by the value of the SP1MODE bit fields in the EBSR. For more details on the actual pin functions, see [Table 6-8](#).

**Table 6-8. SD1, I2S1, and GP[11:6] Pin Multiplexing**

| PDINHIBR1<br>REGISTER<br>BIT FIELDS <sup>(1)</sup> | PIN NAME               | EBSR SP1MODE BITS     |          |        |
|--|------------------------|-----------------------|----------|--------|
|  |                        | MODE 0                | MODE 1   | MODE 2 |
|  |                        | 00<br>(Reset default) | 01       | 10     |
| S10PD  | SD1_CLK/I2S1_CLK/GP[6] | SD1_CLK               | I2S1_CLK | GP[6]  |
| S11PD  | SD1_CMD/I2S1_FS/GP[7]  | SD1_CMD               | I2S1_FS  | GP[7]  |
| S12PD  | SD1_D0/I2S1_DX/GP[8]   | SD1_D0                | I2S1_DX  | GP[8]  |
| S13PD  | SD1_D1/I2S1_RX/GP[9]   | SD1_D1                | I2S1_RX  | GP[9]  |
| S14PD  | SD1_D2/GP[10]          | SD1_D2                | GP[10]   | GP[10] |
| S15PD  | SD1_D3/GP[11]          | SD1_D3                | GP[11]   | GP[11] |

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled through this register.

### 6.7.1.3 SD0, I2S0, and GP[5:0] Pin Multiplexing [EBSR.SP0MODE Bits]

The SD0, I2S0, and GPIO signal muxing is determined by the value of the SP0MODE bit fields in the EBSR. For more details on the actual pin functions, see [Table 6-9](#).

**Table 6-9. SD0, I2S0, and GP[5:0] Pin Multiplexing**

| PDINHIBR1<br>REGISTER<br>BIT FIELDS <sup>(1)</sup> | PIN NAME               | EBSR SP0MODE BITS     |          |        |
|--|------------------------|-----------------------|----------|--------|
|  |                        | MODE 0                | MODE 1   | MODE 2 |
|  |                        | 00<br>(Reset default) | 01       | 10     |
| S00PD  | SD0_CLK/I2S0_CLK/GP[0] | SD0_CLK               | I2S0_CLK | GP[0]  |
| S01PD  | SD0_CMD/I2S0_FS/GP[1]  | SD0_CMD               | I2S0_FS  | GP[1]  |
| S02PD  | SD0_D0/I2S0_DX/GP[2]   | SD0_D0                | I2S0_DX  | GP[2]  |
| S03PD  | SD0_D1/I2S0_RX/GP[3]   | SD0_D1                | I2S0_RX  | GP[3]  |
| S04PD  | SD0_D2/GP[4]           | SD0_D2                | GP[4]    | GP[4]  |
| S05PD  | SD0_D3/GP[5]           | SD0_D3                | GP[5]    | GP[5]  |

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled through this register.

## 6.8 Debugging Considerations

### 6.8.1 Pullup and Pulldown Resistors

Proper board design should ensure that input pins to the device DSP always be at a valid logic level and not floating. This may be achieved through pullup and pulldown resistors. The DSP features IPU and IPD resistors on many pins, including all GPIO pins, to eliminate the need, unless otherwise noted, for external pullup and pulldown resistors.

An external pullup and pulldown resistor may need to be used in the following situations:

- **Configuration Pins:** An external pullup and pulldown resistor is recommended to set the desired value or state (see the configuration pins listed in [Table 6-5](#)). Some configuration pins must be connected directly to ground or to a specific supply voltage.
- **Other Input Pins:** If the IPU and IPD does not match the desired value or state, use an external pullup and pulldown resistor to pull the signal to the opposite rail.

For the configuration pins (listed in [Table 6-5](#)), if they are both routed out and high-impedance state (not driven), TI recommends implementing an external pullup and pulldown resistor. In addition, applying external pullup and pulldown resistors on the configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

When an external pullup or pulldown resistor is used on a pin, the IPU and IPD resistor of the pin must be disabled through the Pullup and Pulldown Inhibit Registers (PDINHIBR1, 2, and 3) [1C17h, 1C18h, and 1C19h, respectively] to minimize power consumption.

Tips for choosing an external pullup and pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Include the leakage currents of all the devices connected to the net, as well as any IPU and IPD resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest  $V_{IL}$  level of all inputs connected to the net. For a pullup resistor, this should be preceding the highest  $V_{IH}$  level of all inputs on the net. A reasonable choice would be to target the  $V_{OL}$  or  $V_{OH}$  levels for the logic family of the limiting device; which, by definition, have margin to the  $V_{IL}$  and  $V_{IH}$  levels.
- Select a pullup and pulldown resistor with the largest possible value that can ensure the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current and any other internal and external pullup and pulldown resistors on the net.
- For bidirectional nets, an additional consideration exists that sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the  $DV_{DDIO}$  rail.

For most systems, a 1-k $\Omega$  resistor can be used to oppose the IPU and IPD while meeting the preceding criteria. Confirm this resistor value is correct for each specific application.

For most systems, a 20-k $\Omega$  resistor can be used to compliment the IPU and IPD on the configuration pins while meeting the above criteria. Confirm this resistor value is correct for each specific application.

For more detailed information on input current ( $I_i$ ), and the low- and high-level input voltages ( $V_{IL}$  and  $V_{IH}$ ) for the device DSP, see [Section 5.5, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature](#).

For the IPU and IPD resistors for all device pins, see the peripheral and system-specific terminal functions table in this document.

## 6.8.2 Bus-Holders

The device has special I/O bus-holder structures to ensure pins are not left floating when  $CV_{DD}$  power is removed while I/O power is applied. When  $CV_{DD}$  is ON, the bus-holders are disabled and the internal pullups or pulldowns, if applicable, function normally. But when  $CV_{DD}$  is OFF and the I/O supply is ON, the bus-holders become enabled and any applicable internal pullups and pulldowns are disabled.

The bus-holders are weak drivers on the pin and, for as long as  $CV_{DD}$  is OFF and I/O power is ON, they hold the last state on the pin. If an external device is strongly driving the device I/O pin to the opposite state then the bus-holder will flip state to match the external driver and DC current will stop.

This bus-holder feature prevents unnecessary power consumption when  $CV_{DD}$  is OFF and I/O supply is ON. For example, current caused by undriven pins (input buffer oscillation) or DC current flowing through pullups or pulldowns.

If external pullup or pulldown resistors are implemented, then care must be taken that those pullup and pulldown resistors can exceed the maximum current of the internal bus-holder and thereby cause the bus-holder to flip state to match the state of the external pullup or pulldown. Otherwise, DC current will flow unnecessarily. When  $CV_{DD}$  power is applied, the bus-holders are disabled (for further details on bus-holders, see [Section 5.6.5.2, Digital I/O Behavior When Core Power \( \$CV\_{DD}\$ \) is Down](#)).

## 6.8.3 CLKOUT Pin

For debug purposes only, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT Control Source Register (CCSSR) can be used to specify the source for the CLKOUT pin.

**Note:** The bootloader disables the CLKOUT pin through CLKOFF bit in the ST3\_55 CPU register.

## 7 Device and Documentation Support

### 7.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, TMS320C5545AZQW10). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

|            |   |
|------------|---|
| <b>TMX</b> | Experimental device that is not necessarily representative of the final device's electrical specifications.                           |
| <b>TMP</b> | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification. |
| <b>TMS</b> | Fully-qualified production device.  |

Support tool development evolutionary flow:

|             |  |
|-------------|--|
| <b>TMDX</b> | Development-support product that has not yet completed Texas Instruments internal qualification testing. |
| <b>TMDS</b> | Fully qualified development-support product.   |

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

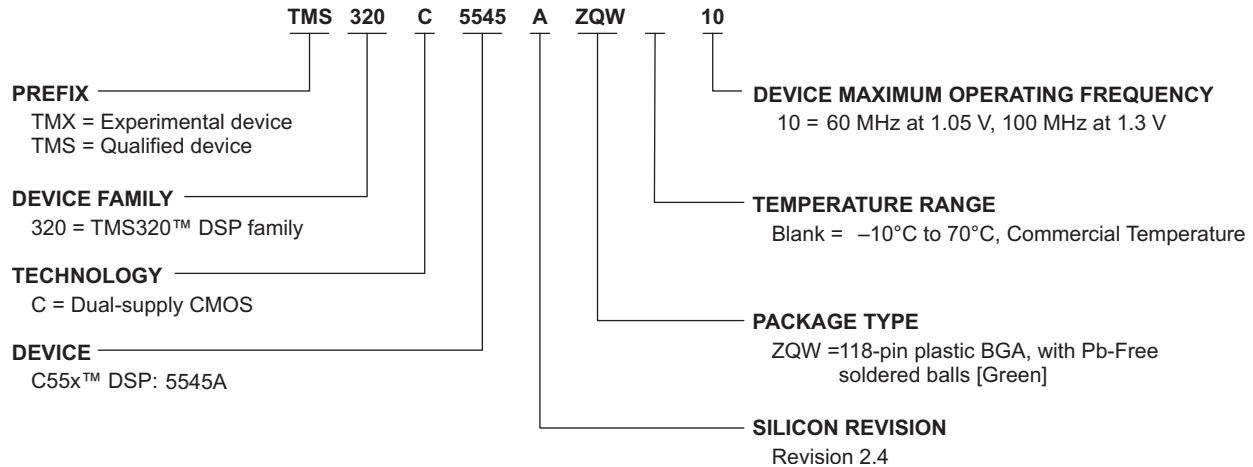
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZQW), and the temperature range (for example, "Blank" is the commercial temperature range).

The following figure provides a legend for reading the complete device name for any DSP platform member.



A. For actual device part numbers (P/Ns) and ordering information, see the TI website (<http://www.ti.com>)

**Figure 7-1. Device Nomenclature**

## 7.2 Tools and Software

TI offers an extensive line of development tools for the TMS320C55x DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320C55x fixed-point DSP-based applications:

### Software Development Tools:

Code Composer Studio Integrated Development Environment (IDE): Associate device as TMS320C5545.

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS Version 5.33 or later), which provides the basic run-time target software needed to support any DSP application.

### Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320C55x DSP platform, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com>. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 7.3 Documentation Support

The current documentation that describes the DSP, related peripherals, and other technical collateral is listed below.

### Errata

**[TMS320C5545A Fixed-Point Digital Signal Processor Silicon Revision 2.4 Silicon Errata](#)** Describes the known exceptions to the functional specifications for this device.

### Application Reports

**[Using the TMS320C5545/35/34/33/32 Bootloader](#)** Describes features of the on-chip ROM for this device, as well as descriptions of how to interface with possible boot devices and generating a boot image to store on an external device.

### **[Power Estimation and Power Consumption Summary for TMS320C5504/05/14/15/32/33/34/35/45](#)**

This application report assists in estimating the power consumption for the TMS320C55xx devices (DSPs), using a power estimation spreadsheet.

**[Migrating From TMS320C5535 to TMS320C5545](#)** This application report provides a summary of the similarities and differences between the TMS320C5535 and TMS320C5545 devices to minimize changes required to migrate from TMS320C5535 to TMS320C5545.

**[Validating High Speed and Full Speed USB on the TMS320C5545 Device](#)** This application report describes the process to validate electrical requirements of high and full speed USB operations on the TMS320C5545 device.

**[C5000 DSP-Based Low-Power System Design](#)** This application report focuses on the Texas Instruments' C5000 DSP family. Low-power related features are highlighted on the architecture level and keynotes are presented for the C5000-based system design.

### User's Guides

**[TMS320C55x DSP v3.x CPU Reference Guide](#)** Describes more detailed information on the C55x CPU.

### Technical Reference Manuals

**[Ultra-Low Power DSP Technical Reference Manual](#)** Collection of documents providing detailed information on the device including system control, FFT implementation, and memory access. Detailed information on the device as well as a functional description of the peripherals supported is also included.

## 7.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范 and 标准且不一定反映 TI 的观点；请见 TI 的[使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 7.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

# 8 Mechanical Packaging and Orderable Information

## 8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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|---------------|--|--------------|--|
| 数字音频          | <a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>                               | 通信与电信        | <a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>             |
| 放大器和线性器件      | <a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>                     | 计算机及周边       | <a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>           |
| 数据转换器         | <a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>             | 消费电子         | <a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a> |
| DLP® 产品       | <a href="http://www.dlp.com">www.dlp.com</a>   | 能源           | <a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>               |
| DSP - 数字信号处理器 | <a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>                                   | 工业应用         | <a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>       |
| 时钟和计时器        | <a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>             | 医疗电子         | <a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>             |
| 接口            | <a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>                       | 安防应用         | <a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>           |
| 逻辑            | <a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>                               | 汽车电子         | <a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>       |
| 电源管理          | <a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>                               | 视频和影像        | <a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>                 |
| 微控制器 (MCU)    | <a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>         |              |  |
| RFID 系统       | <a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>                           |              |  |
| OMAP应用处理器     | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                       |              |  |
| 无线连通性         | <a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a> | 德州仪器在线技术支持社区 | <a href="http://www.deyisupport.com">www.deyisupport.com</a>                 |

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**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type               | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|--------------------|---------------|----------------------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TMS320C5545AZQW06  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -10 to 70    | TMS320C55<br>45AZQW06   |  |
| TMS320C5545AZQW10  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -10 to 70    | TMS320C55<br>45AZQW10   |  |
| TMS320C5545AZQW10R | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 2500        | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -10 to 70    | TMS320C55<br>45AZQW10   |  |
| TMS320C5545AZQW12  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -10 to 70    | TMS320C55<br>45AZQW12   |  |
| TMS320C5545AZQWA06 | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         |   |
| TMS320C5545AZQWA10 | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         |   |
| TMS320C5545AZQWA12 | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQW             | 118  | 250         | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         |   |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

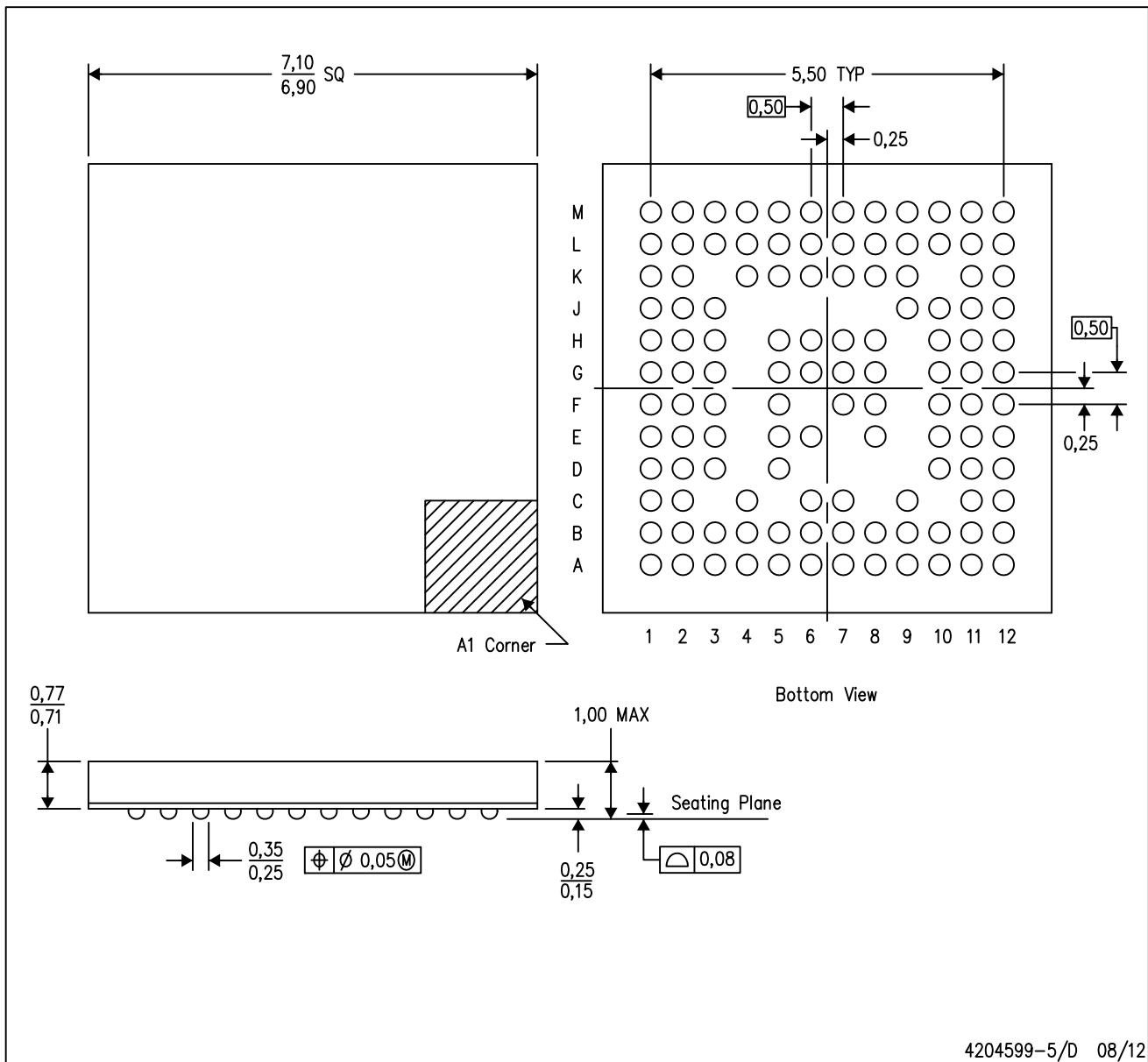
- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZQW (S-PBGA-N118)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225
  - D. This is a Pb-free solder ball design.

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|               | 产品   |              | 应用   |
|---------------|--|--------------|--|
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| 放大器和线性器件      | <a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>                     | 计算机及周边       | <a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>           |
| 数据转换器         | <a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>             | 消费电子         | <a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a> |
| DLP® 产品       | <a href="http://www.dlp.com">www.dlp.com</a>   | 能源           | <a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>               |
| DSP - 数字信号处理器 | <a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>                                   | 工业应用         | <a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>       |
| 时钟和计时器        | <a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>             | 医疗电子         | <a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>             |
| 接口            | <a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>                       | 安防应用         | <a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>           |
| 逻辑            | <a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>                               | 汽车电子         | <a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>       |
| 电源管理          | <a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>                               | 视频和影像        | <a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>                 |
| 微控制器 (MCU)    | <a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>         |              |  |
| RFID 系统       | <a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>                           |              |  |
| OMAP应用处理器     | <a href="http://www.ti.com.cn/omap">www.ti.com.cn/omap</a>                                 |              |  |
| 无线连通性         | <a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a> | 德州仪器在线技术支持社区 | <a href="http://www.deyisupport.com">www.deyisupport.com</a>                 |

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