

# ADS114S0xB Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 16-Bit, Delta-Sigma ADC With PGA and Voltage Reference

## 1 Features

- Low Power Consumption: As Low as 280  $\mu$ A
- Programmable Gain: 1 to 128
- Programmable Data Rates: 2.5 SPS to 4 kSPS
- Simultaneous 50-Hz and 60-Hz Rejection at  $\leq 20$  SPS With Low-Latency Digital Filter
- Analog Multiplexer with 12 (ADS114S08B) or 6 (ADS114S06B) Independently Selectable Inputs
- Dual-Matched Programmable Current Sources for Sensor Excitation: 10  $\mu$ A to 2000  $\mu$ A
- Internal Reference: 2.5 V, 8 ppm/ $^{\circ}$ C (typ) Drift
- Internal Oscillator: 4.096 MHz, 2% Accuracy
- Internal Temperature Sensor
- Self Offset and System Calibration
- Four General-Purpose I/Os
- SPI-Compatible Interface
- Analog Supply: Unipolar (2.7 V to 5.25 V) or Bipolar ( $\pm 2.5$  V)
- Digital Supply: 2.7 V to 3.6 V
- Operating Temperature:  $-40^{\circ}$ C to  $+125^{\circ}$ C
- Pin-Compatible With the [ADS114S0x](#)

## 2 Applications

- Sensor Transducers and Transmitters: Temperature, Pressure, Strain, Flow
- PLC and DCS Analog Input Modules
- Temperature Controllers
- Climate Chambers, Industrial Ovens

## 3 Description

The ADS114S06B and ADS114S08B are precision, 16-bit, delta-sigma ( $\Delta\Sigma$ ), analog-to-digital converters (ADCs) that offer low power consumption and many integrated features to reduce system cost and component count in applications measuring small-signal sensors.

These ADCs feature a digital filter that offers low-latency conversion results and 50-Hz or 60-Hz rejection for noisy industrial environments. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals for resistive bridge or thermocouple applications. Additionally, these devices integrate a low-drift, 2.5-V reference that reduces printed circuit board (PCB) area. Finally, two programmable excitation current sources (IDACs) allow for easy and accurate RTD biasing.

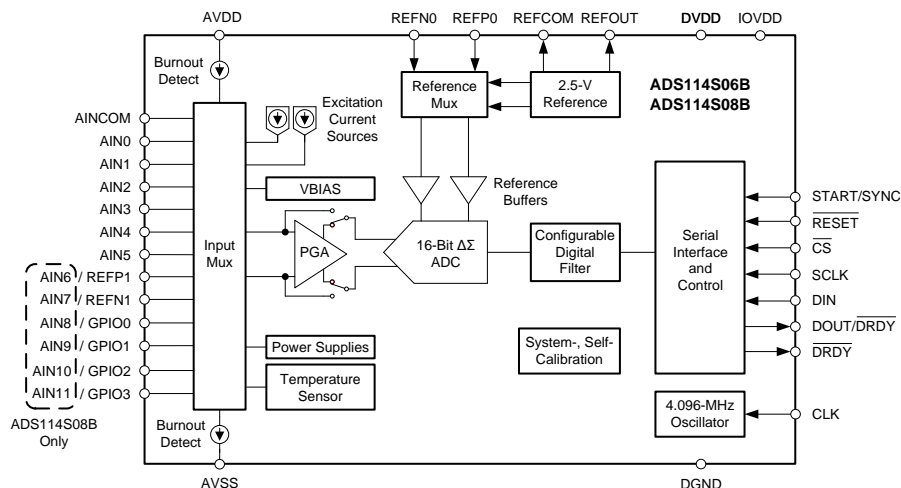
An input multiplexer supports 12 inputs for the ADS114S08B and six inputs for the ADS114S06B that can be connected to the ADC in any combination for design flexibility. In addition, these devices include features such as sensor burn-out detection, voltage bias for thermocouples, system monitoring, and four general-purpose I/Os.

The devices are offered in a leadless VQFN-32 or a TQFP-32 package.

### Device Information

| ORDER NUMBER | PACKAGE (PIN) | BODY SIZE       |
|--------------|---------------|-----------------|
| ADS114S0xB   | TQFP (32)     | 5.0 mm x 5.0 mm |
|              | VQFN (32)     | 5.0 mm x 5.0 mm |

### Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 9.6 Register Map.....  | <b>54</b> |
| <b>2 Applications</b> .....                      | <b>1</b>  | <b>10 Application and Implementation</b> .....                   | <b>67</b> |
| <b>3 Description</b> .....                       | <b>1</b>  | 10.1 Application Information.....                                | <b>67</b> |
| <b>4 Revision History</b> .....                  | <b>2</b>  | 10.2 Typical Application .....                                   | <b>72</b> |
| <b>5 Device Family Comparison Table</b> .....    | <b>3</b>  | 10.3 Do's and Don'ts.....  | <b>77</b> |
| <b>6 Pin Configuration and Functions</b> .....   | <b>3</b>  | <b>11 Power Supply Recommendations</b> .....                     | <b>79</b> |
| <b>7 Specifications</b> .....                    | <b>5</b>  | 11.1 Power Supplies .....  | <b>79</b> |
| 7.1 Absolute Maximum Ratings .....               | <b>5</b>  | 11.2 Power-Supply Sequencing.....                                | <b>79</b> |
| 7.2 ESD Ratings.....                             | <b>5</b>  | 11.3 Power-On Reset.....   | <b>79</b> |
| 7.3 Recommended Operating Conditions.....        | <b>6</b>  | 11.4 Power-Supply Decoupling.....                                | <b>79</b> |
| 7.4 Thermal Information .....                    | <b>6</b>  | <b>12 Layout</b> .....   | <b>80</b> |
| 7.5 Electrical Characteristics.....              | <b>7</b>  | 12.1 Layout Guidelines .....                                     | <b>80</b> |
| 7.6 Timing Characteristics.....                  | <b>10</b> | 12.2 Layout Example .....  | <b>81</b> |
| 7.7 Switching Characteristics .....              | <b>10</b> | <b>13 Device and Documentation Support</b> .....                 | <b>82</b> |
| 7.8 Typical Characteristics.....                 | <b>13</b> | 13.1 Device Support.....   | <b>82</b> |
| <b>8 Parameter Measurement Information</b> ..... | <b>19</b> | 13.2 Documentation Support .....                                 | <b>82</b> |
| 8.1 Noise Performance .....                      | <b>19</b> | 13.3 Related Links .....   | <b>82</b> |
| <b>9 Detailed Description</b> .....              | <b>21</b> | 13.4 Receiving Notification of Documentation Updates             | <b>82</b> |
| 9.1 Overview .....                               | <b>21</b> | 13.5 Community Resources.....                                    | <b>82</b> |
| 9.2 Functional Block Diagram .....               | <b>22</b> | 13.6 Trademarks .....  | <b>82</b> |
| 9.3 Feature Description.....                     | <b>23</b> | 13.7 Electrostatic Discharge Caution.....                        | <b>82</b> |
| 9.4 Device Functional Modes.....                 | <b>42</b> | 13.8 Glossary .....  | <b>83</b> |
| 9.5 Programming.....                             | <b>46</b> | <b>14 Mechanical, Packaging, and Orderable Information</b> ..... | <b>83</b> |

## 4 Revision History

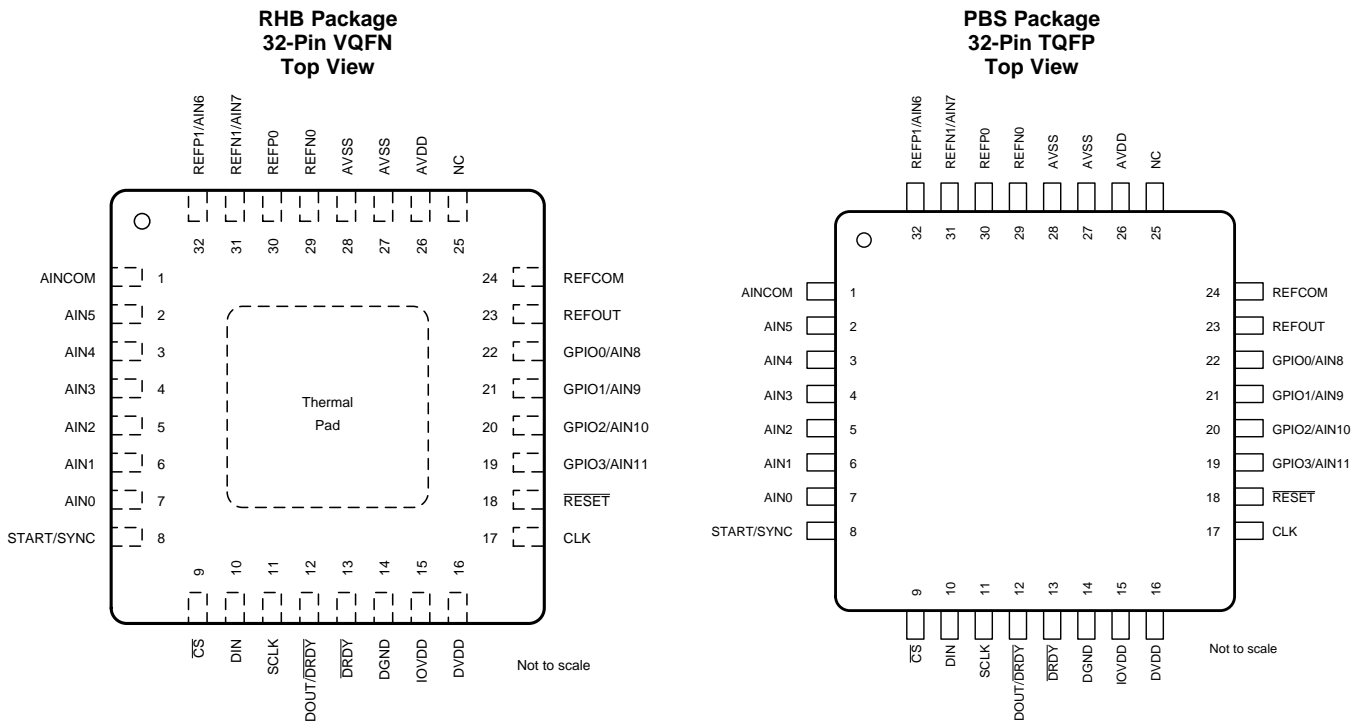
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE        | REVISION | NOTES            |
|-------------|----------|------------------|
| August 2017 | *        | Initial release. |

## 5 Device Family Comparison Table

| PRODUCT    | RESOLUTION (Bits) | NUMBER OF INPUTS |
|------------|-------------------|------------------|
| ADS114S08B | 16                | 12 analog inputs |
| ADS114S06B | 16                | 6 analog inputs  |

## 6 Pin Configuration and Functions



NOTE: The analog input functions (AIN6–AIN11) are not available on pins 19 to 22, 31, and 32 for the ADS114S06B.

### Pin Functions

| PIN |                               | FUNCTION            | DESCRIPTION <sup>(1)</sup>   |
|-----|-------------------------------|---------------------|--|
| NO. | NAME                          |                     |  |
| 1   | AINCOM                        | Analog input        | Common analog input for single-ended measurements  |
| 2   | AIN5                          | Analog input        | Analog input 5   |
| 3   | AIN4                          | Analog input        | Analog input 4   |
| 4   | AIN3                          | Analog input        | Analog input 3   |
| 5   | AIN2                          | Analog input        | Analog input 2   |
| 6   | AIN1                          | Analog input        | Analog input 1   |
| 7   | AIN0                          | Analog input        | Analog input 0   |
| 8   | START/SYNC                    | Digital input       | Start conversion   |
| 9   | $\overline{\text{CS}}$        | Digital input       | Chip select; active low  |
| 10  | DIN                           | Digital input       | Serial data input  |
| 11  | SCLK                          | Digital input       | Serial clock input   |
| 12  | $\overline{\text{DOUT/DRDY}}$ | Digital output      | Serial data output combined with data ready; active low  |
| 13  | $\overline{\text{DRDY}}$      | Digital output      | Data ready; active low   |
| 14  | DGND                          | Digital ground      | Digital ground   |
| 15  | IOVDD                         | Digital supply      | Digital I/O power supply. In case IOVDD is not tied to DVDD, connect a 100-nF (or larger) capacitor to DGND.   |
| 16  | DVDD                          | Digital supply      | Digital core power supply. Connect a 100-nF (or larger) capacitor to DGND.   |
| 17  | CLK                           | Digital input       | External clock input. Connect to DGND to use the internal oscillator.  |
| 18  | $\overline{\text{RESET}}$     | Digital input       | Reset; active low  |
| 19  | GPIO3/AIN11                   | Analog input/output | General-purpose I/O <sup>(2)</sup> ; analog input 11 (ADS114S08B only)   |
| 20  | GPIO2/AIN10                   | Analog input/output | General-purpose I/O <sup>(2)</sup> ; analog input 10 (ADS114S08B only)   |
| 21  | GPIO1/AIN9                    | Analog input/output | General-purpose I/O <sup>(2)</sup> ; analog input 9 (ADS114S08B only)  |
| 22  | GPIO0/AIN8                    | Analog input/output | General-purpose I/O <sup>(2)</sup> ; analog input 8 (ADS114S08B only)  |
| 23  | REFOUT                        | Analog output       | Positive voltage reference output. Connect a 1- $\mu\text{F}$ to 47- $\mu\text{F}$ capacitor to REFCOM if the internal voltage reference is enabled. |
| 24  | REFCOM                        | Analog output       | Negative voltage reference output. Connect to AVSS.  |
| 25  | NC                            | —                   | Leave unconnected or connect to AVSS   |
| 26  | AVDD                          | Analog supply       | Positive analog power supply. Connect a 330-nF (or larger) capacitor to AVSS.  |
| 27  | AVSS                          | Analog supply       | Negative analog power supply   |
| 28  | AVSS                          | Analog supply       | Negative analog power supply   |
| 29  | REFN0                         | Analog input        | Negative external reference input 0  |
| 30  | REFP0                         | Analog input        | Positive external reference input 0  |
| 31  | REFN1/AIN7                    | Analog input        | Negative external reference input 1; analog input 7 (ADS114S08B only)  |
| 32  | REFP1/AIN6                    | Analog input        | Positive external reference input 1; analog input 6 (ADS114S08B only)  |
| Pad | Thermal Pad                   | —                   | RHB package only. Thermal power pad. Connect to AVSS.  |

(1) See the [Unused Inputs and Outputs](#) section for details on how to connect unused pins.

(2) General-purpose inputs and outputs use logic levels based on the analog supply.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

|                       |   | MIN        | MAX         | UNIT |
|-----------------------|---|------------|-------------|------|
| Power-supply voltage  | AVDD to AVSS  | -0.3       | 5.5         | V    |
|                       | AVSS to DGND  | -2.8       | 0.3         |      |
|                       | DVDD to DGND  | -0.3       | 3.9         |      |
|                       | IOVDD to DGND   | -0.3       | 5.5         |      |
| Analog input voltage  | AINx, GPIOx, REFPx, REFNx, REFCOM   | AVSS - 0.3 | AVDD + 0.3  | V    |
| Digital input voltage | $\overline{CS}$ , SCLK, DIN, DOUT/DRDY, $\overline{DRDY}$ , START, $\overline{RESET}$ , CLK | DGND - 0.3 | IOVDD + 0.3 | V    |
| Input current         | Continuous, REFN0, REFOUT   | -100       | 100         | mA   |
|                       | Continuous, all other pins except power-supply pins   | -10        | 10          |      |
| Temperature           | Junction, T <sub>J</sub>  |            | 150         | °C   |
|                       | Storage, T <sub>stg</sub>   | -60        | 150         |      |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|  |                                       | MIN  | NOM   | MAX  | UNIT |
|--|---------------------------------------|--|-------|--|------|
| <b>POWER SUPPLY</b>                                |                                       |  |       |  |      |
| Analog power supply                                | AVDD to AVSS                          | 2.7  |       | 5.25   | V    |
|  | AVSS to DGND                          | -2.625   | 0     | 0.05   |      |
|  | AVDD to DGND                          | 1.5  |       | 5.25   |      |
| Digital core power supply                          | DVDD to DGND                          | 2.7  |       | 3.6  | V    |
| Digital IO power supply                            | IOVDD to DGND                         | DVDD   |       | 5.25   | V    |
| <b>ANALOG INPUTS<sup>(1)</sup></b>                 |                                       |  |       |  |      |
| $V_{(AINx)}$ Absolute input voltage <sup>(2)</sup> | PGA bypassed                          | AVSS – 0.05                                      |       | AVDD + 0.05                                      | V    |
|  | PGA enabled, gain = 1 to 16           | $AVSS + 0.15 +  V_{INMAX}  \cdot (Gain - 1) / 2$ |       | $AVDD - 0.15 -  V_{INMAX}  \cdot (Gain - 1) / 2$ |      |
|  | PGA enabled, gain = 32 to 128         | $AVSS + 0.15 + 15.5 \cdot  V_{INMAX} $           |       | $AVDD - 0.15 - 15.5 \cdot  V_{INMAX} $           |      |
| $V_{IN}$ Differential input voltage                | $V_{IN} = V_{AINP} - V_{AINN}$        | $-V_{REF} / Gain$                                |       | $V_{REF} / Gain$                                 | V    |
| <b>VOLTAGE REFERENCE INPUTS<sup>(3)</sup></b>      |                                       |  |       |  |      |
| $V_{REF}$ Differential reference input voltage     | $V_{REF} = V_{(REFPx)} - V_{(REFNx)}$ | 0.5  |       | AVDD – AVSS                                      | V    |
| $V_{(REFNx)}$ Absolute negative reference voltage  | Negative reference buffer disabled    | AVSS – 0.05                                      |       | $V_{(REFPx)} - 0.5$                              | V    |
|  | Negative reference buffer enabled     | AVSS   |       | $V_{(REFPx)} - 0.5$                              | V    |
| $V_{(REFPx)}$ Absolute positive reference voltage  | Positive reference buffer disabled    | $V_{(REFNx)} + 0.5$                              |       | AVDD + 0.05                                      | V    |
|  | Positive reference buffer enabled     | $V_{(REFNx)} + 0.5$                              |       | AVDD   | V    |
| <b>EXTERNAL CLOCK SOURCE<sup>(4)</sup></b>         |                                       |  |       |  |      |
| $f_{CLK}$ External clock frequency                 |                                       | 2  | 4.096 | 4.5  | MHz  |
| Duty cycle   |                                       | 40%  | 50%   | 60%  |      |
| <b>GENERAL-PURPOSE INPUTS (GPIOs)</b>              |                                       |  |       |  |      |
| Input voltage                                      |                                       | AVSS – 0.05                                      |       | AVDD + 0.05                                      | V    |
| <b>DIGITAL INPUTS (Other than GPIOs)</b>           |                                       |  |       |  |      |
| Input voltage                                      |                                       | DGND   |       | IOVDD  | V    |
| <b>TEMPERATURE RANGE</b>                           |                                       |  |       |  |      |
| $T_A$ Operating ambient temperature                |                                       | -40  |       | 125  | °C   |

- (1)  $A_{INP}$  and  $A_{INN}$  denote the positive and negative inputs of the PGA. Any of the available analog inputs ( $A_{INx}$ ) can be selected as either  $A_{INP}$  or  $A_{INN}$  by the input multiplexer.
- (2)  $V_{INMAX}$  denotes the maximum differential input voltage,  $V_{IN}$ , that is expected in the application.  $|V_{INMAX}|$  can be smaller than  $V_{REF} / Gain$ .
- (3) REFPx and REFNx denote one of the two available external differential reference input pairs.
- (4) An external clock is not required when the internal oscillator is used.

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                                     | ADS114S06B, ADS114S08B |            | UNIT |
|---|------------------------|------------|------|
|   | VQFN (RHB)             | TQFP (PBS) |      |
|   | 32 PINS                | 32 PINS    |      |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance            | 45.2                   | 75.5       | °C/W |
| $R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance    | 28.3                   | 17.1       | °C/W |
| $R_{\theta JB}$ Junction-to-board thermal resistance              | 15.8                   | 28.5       | °C/W |
| $\Psi_{JT}$ Junction-to-top characterization parameter            | 0.4                    | 0.4        | °C/W |
| $\Psi_{JB}$ Junction-to-board characterization parameter          | 15.7                   | 28.3       | °C/W |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | 2.3                    | n/a        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ; all specifications are at  $AVDD = 2.7\text{ V}$  to  $5.25\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , all gains, internal reference, internal oscillator, and all data rates (unless otherwise noted)

| PARAMETER                     |  | TEST CONDITIONS  | MIN   | TYP   | MAX  | UNIT                    |
|-------------------------------|--|--|---|---|------|-------------------------|
| <b>ANALOG INPUTS</b>          |  |  |   |   |      |                         |
| Absolute input current        | PGA bypassed,<br>$AVSS + 0.1\text{ V} \leq V_{(AINx)} \leq AVDD - 0.1\text{ V}$                                      |  |   | $\pm 0.5$   |      | nA                      |
|                               | PGA enabled, gain 1 to 128,<br>$V_{(AINx)MIN} \leq V_{(AINx)} \leq V_{(AINx)MAX}$                                    |  | -10   | $\pm 0.1$   | 10   |                         |
| Differential input current    | PGA bypassed,<br>$V_{CM} = AVDD / 2$ , $-V_{REF} \leq V_{IN} \leq V_{REF}$   |  |   | $\pm 1$   |      | nA/V                    |
|                               | PGA enabled, gain 1 to 128,<br>$V_{CM} = AVDD / 2$ , $-V_{REF} / \text{Gain} \leq V_{IN} \leq V_{REF} / \text{Gain}$ |  |   | $\pm 0.02$  |      | nA                      |
| <b>PGA</b>                    |  |  |   |   |      |                         |
| Gain settings                 |  |  |   | 1, 2, 4, 8, 16,<br>32, 64, 128  |      |                         |
| Startup time                  | Enabling the PGA in conversion mode  |  |   | 190   |      | $\mu\text{s}$           |
| <b>SYSTEM PERFORMANCE</b>     |  |  |   |   |      |                         |
| Resolution (no missing codes) |  |  | 16  |   |      | Bits                    |
| DR                            | Data rate  |  |   | 2.5, 5, 10, 16.6,<br>20, 50, 60, 100,<br>200, 400, 800,<br>1000, 2000, 4000 |      | SPS                     |
| INL                           | Integral nonlinearity (best fit)   | PGA bypassed, $V_{CM} = AVDD / 2$  |   | 1   |      | ppm <sub>FSR</sub>      |
|                               |  | PGA enabled, gain = 1 to 128, $V_{CM} = AVDD / 2$  |   | 2   | 25   |                         |
| $V_{IO}$                      | Input offset voltage   | PGA bypassed   |   | 20  |      | $\mu\text{V}$           |
|                               |  | PGA enabled, gain = 1 to 8   |   | 20 / Gain   |      |                         |
|                               |  | PGA enabled, gain = 16 to 128  |   | 2   |      |                         |
|                               |  | PGA bypassed, after internal offset calibration  |   | On the order of noise <sub>pp</sub> at the set DR and gain                  |      |                         |
|                               |  | PGA enabled, gain = 1 to 128, after internal offset calibration  |   | On the order of noise <sub>pp</sub> at the set DR and gain                  |      |                         |
| Offset drift                  | PGA bypassed   |  |   | 10  |      | nV/ $^{\circ}\text{C}$  |
|                               | PGA enabled, gain = 1 to 128   |  |   | 15  |      |                         |
| Gain error <sup>(1)</sup>     | $T_A = 25^{\circ}\text{C}$ , PGA bypassed  |  |   | 0.01%   | 0.1% |                         |
|                               | $T_A = 25^{\circ}\text{C}$ , PGA enabled, gain = 1 to 128  |  |   | 0.025%  | 0.2% |                         |
| Gain drift <sup>(1)</sup>     | PGA bypassed   |  |   | 0.5   |      | ppm/ $^{\circ}\text{C}$ |
|                               | PGA enabled, gain = 1 to 128   |  |   | 1   |      |                         |
| Noise (input-referred)        |  |  | See the <a href="#">Noise Performance</a> section |   |      |                         |
| NMRR                          | Normal-mode rejection ratio <sup>(2)</sup>   | $f_{IN} = 50\text{ Hz}$ or $60\text{ Hz}$ ( $\pm 1\text{ Hz}$ ), DR = 20 SPS   | 75  | 95  |      | dB                      |
|                               |  | $f_{IN} = 50\text{ Hz}$ or $60\text{ Hz}$ ( $\pm 1\text{ Hz}$ ), DR = 20 SPS,<br>external $f_{CLK} = 4.096\text{ MHz}$ | 95  |   |      |                         |
| CMRR                          | Common-mode rejection ratio  | At dc  |   | 120   |      | dB                      |
|                               |  | $f_{CM} = 50\text{ Hz}$ or $60\text{ Hz}$ ( $\pm 1\text{ Hz}$ ),<br>DR = 2.5 SPS, 5 SPS, 10 SPS, 20 SPS                |   | 125   |      |                         |
| PSRR                          | Power-supply rejection ratio   | AVDD at dc   |   | 105   |      | dB                      |
|                               |  | AVDD at 50 Hz or 60 Hz   |   | 115   |      |                         |
|                               |  | DVDD at dc   |   | 115   |      |                         |

(1) Excluding error of voltage reference.

(2) See the [50-Hz and 60-Hz Line Cycle Rejection](#) section for more information.

## Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ; all specifications are at  $AVDD = 2.7\text{ V}$  to  $5.25\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , all gains, internal reference, internal oscillator, and all data rates (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS  | MIN    | TYP  | MAX          | UNIT                    |
|---|--|--------|--|--------------|-------------------------|
| <b>VOLTAGE REFERENCE INPUTS</b>           |  |        |  |              |                         |
| Absolute input current                    | Reference buffers disabled, external $V_{REF} = 2.5\text{ V}$ , REFP1/REFN1 inputs                       |        | 4  |              | $\mu\text{A/V}$         |
|   | Reference buffers enabled, external $V_{REF} = 2.5\text{ V}$ , REFP1/REFN1 inputs                        |        | 5  |              | nA                      |
| <b>INTERNAL VOLTAGE REFERENCE</b>         |  |        |  |              |                         |
| $V_{REF}$ Output voltage                  |  |        | 2.5  |              | V                       |
| Accuracy                                  | $T_A = 25^{\circ}\text{C}$   | -0.2%  | $\pm 0.01\%$                                 | 0.2%         |                         |
| Temperature drift                         |  |        | 8  | 40           | ppm/ $^{\circ}\text{C}$ |
| Output current                            | $AVDD = 2.7\text{ V}$ to $3.3\text{ V}$ , sink and source  | -5     |  | 5            | mA                      |
|   | $AVDD = 3.3\text{ V}$ to $5.25\text{ V}$ , sink and source   | -10    |  | 10           |                         |
| Short-circuit current limit               | Sink and source  |        | 70   | 100          | mA                      |
| PSRR Power-supply rejection ratio         | $AVDD$ at dc   |        | 85   |              | dB                      |
| Load regulation                           | $AVDD = 2.7\text{ V}$ to $3.3\text{ V}$ , load current = $-5\text{ mA}$ to $5\text{ mA}$                 |        | 8  |              | $\mu\text{V/mA}$        |
|   | $AVDD = 3.3\text{ V}$ to $5.25\text{ V}$ , load current = $-10\text{ mA}$ to $10\text{ mA}$              |        | 8  |              |                         |
| Startup time                              | 1- $\mu\text{F}$ capacitor on REFOUT, 0.001% settling  |        | 5.9  |              | ms                      |
| Capacitive load stability                 | Capacitor on REFOUT  | 1      |  | 47           | $\mu\text{F}$           |
| Reference noise                           | $f = 0.1\text{ Hz}$ to $10\text{ Hz}$ , 1- $\mu\text{F}$ capacitor on REFOUT                             |        | 9  |              | $\mu\text{V}_{PP}$      |
| <b>INTERNAL OSCILLATOR</b>                |  |        |  |              |                         |
| $f_{CLK}$ Frequency                       |  |        | 4.096  |              | MHz                     |
| Accuracy                                  |  | -2%    |  | 2%           |                         |
| <b>EXCITATION CURRENT SOURCES (IDACS)</b> |  |        |  |              |                         |
| Current settings                          |  |        | 10, 50, 100, 250, 500, 750, 1000, 1500, 2000 |              | $\mu\text{A}$           |
| Compliance voltage <sup>(3)</sup>         | 10 $\mu\text{A}$ to 750 $\mu\text{A}$ , 0.1% deviation   | $AVSS$ |  | $AVDD - 0.4$ | V                       |
|   | 1 mA to 2 mA, 0.1% deviation   | $AVSS$ |  | $AVDD - 0.6$ |                         |
| Accuracy (each IDAC)                      | $T_A = 25^{\circ}\text{C}$ , 10 $\mu\text{A}$ to 2 mA  | -6%    | $\pm 1\%$                                    | 6%           |                         |
| Current mismatch between IDACs            | $T_A = 25^{\circ}\text{C}$ , 10 $\mu\text{A}$ to 2 mA  |        | 0.2%   |              |                         |
| Temperature drift (each IDAC)             | 10 $\mu\text{A}$ to 2 mA   |        | 100  |              | ppm/ $^{\circ}\text{C}$ |
| Temperature drift matching between IDACs  | 10 $\mu\text{A}$ to 2 mA   |        | 10   |              | ppm/ $^{\circ}\text{C}$ |
| Startup time                              | With internal reference already settled. From end of WREG command to current flowing out of pin.         |        | 22   |              | $\mu\text{s}$           |
| <b>BIAS VOLTAGE</b>                       |  |        |  |              |                         |
| $V_{BIAS}$ Output voltage                 |  |        | $(AVDD + AVSS) / 2$                          |              | V                       |
| Output impedance                          |  |        | 350  |              | $\Omega$                |
| Startup time                              | Combined capacitive load on all selected analog inputs $C_{LOAD} = 1\text{ }\mu\text{F}$ , 0.1% settling |        | 2.8  |              | ms                      |
| <b>BURNOUT CURRENT SOURCES (BOCS)</b>     |  |        |  |              |                         |
| Current settings                          |  |        | 0.2, 1, 10                                   |              | $\mu\text{A}$           |
| Accuracy                                  | 0.2 $\mu\text{A}$ , sinking or sourcing  |        | $\pm 8\%$                                    |              |                         |
|   | 1 $\mu\text{A}$ , sinking or sourcing  |        | $\pm 4\%$                                    |              |                         |
|   | 10 $\mu\text{A}$ , sinking or sourcing   |        | $\pm 2\%$                                    |              |                         |
| <b>SUPPLY VOLTAGE MONITORS</b>            |  |        |  |              |                         |
| Accuracy                                  | $(AVDD - AVSS) / 4$ monitor  |        | $\pm 1\%$                                    |              |                         |
|   | $DVDD / 4$ monitor   |        | $\pm 1\%$                                    |              |                         |

(3) The IDAC current does not change by more than 0.1% from the nominal value when staying within the specified compliance voltage.



## Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ; all specifications are at  $\text{AVDD} = 2.7\text{ V}$  to  $5.25\text{ V}$ ,  $\text{AVSS} = 0\text{ V}$ ,  $\text{DVDD} = \text{IOVDD} = 3.3\text{ V}$ , all gains, internal reference, internal oscillator, and all data rates (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | MIN   | TYP                | MAX                  | UNIT                           |
|---|---|---|--------------------|----------------------|--------------------------------|
| <b>TEMPERATURE SENSOR</b>   |   |   |                    |                      |                                |
| Output voltage  | $T_A = 25^{\circ}\text{C}$                                    |   | 129                |                      | mV                             |
| Temperature coefficient   |   |   | 403                |                      | $\mu\text{V}/^{\circ}\text{C}$ |
| <b>GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)</b>  |   |   |                    |                      |                                |
| $V_{IL}$  | Logic input level, low  | $\text{AVSS} - 0.05$  |                    | $0.3\text{ AVDD}$    | V                              |
| $V_{IH}$  | Logic input level, high                                       | $0.7\text{ AVDD}$   |                    | $\text{AVDD} + 0.05$ | V                              |
| $V_{OL}$  | Logic output level, low                                       | $I_{OL} = 1\text{ mA}$  | $\text{AVSS}$      | $0.2\text{ AVDD}$    | V                              |
| $V_{OH}$  | Logic output level, high                                      | $I_{OH} = 1\text{ mA}$  | $0.8\text{ AVDD}$  | $\text{AVDD}$        | V                              |
| <b>DIGITAL INPUT/OUTPUTS</b>  |   |   |                    |                      |                                |
| $V_{IL}$  | Logic input level, low  | DGND  |                    | $0.3\text{ IOVDD}$   | V                              |
| $V_{IH}$  | Logic input level, high                                       | $0.7\text{ IOVDD}$  |                    | $\text{IOVDD}$       | V                              |
| $V_{OL}$  | Logic output level, low                                       | $I_{OL} = 1\text{ mA}$  | DGND               | $0.2\text{ IOVDD}$   | V                              |
| $V_{OH}$  | Logic output level, high                                      | $I_{OH} = 1\text{ mA}$  | $0.8\text{ IOVDD}$ | $\text{IOVDD}$       | V                              |
| Input current   | $\text{DGND} \leq V_{\text{Digital Input}} \leq \text{IOVDD}$ | -1  |                    | 1                    | $\mu\text{A}$                  |
| <b>ANALOG SUPPLY CURRENT (AVDD = 3.3 V, External Reference, Internal Reference Disabled, Reference Buffers Disabled, IDACs Disabled, VBIAS Disabled, Internal Oscillator, All Data Rates, <math>V_{IN} = 0\text{ V}</math>)</b>       |   |   |                    |                      |                                |
| $I_{\text{AVDD}}$   | Analog supply current   | Power-down mode   |                    | 0.1                  | $\mu\text{A}$                  |
|   |   | Standby mode, PGA bypassed                                    |                    | 70                   |                                |
|   |   | Conversion mode, PGA bypassed                                 |                    | 85                   |                                |
|   |   | Conversion mode, PGA enabled, gain = 1, 2                     |                    | 120                  |                                |
|   |   | Conversion mode, PGA enabled, gain = 4, 8                     |                    | 140                  |                                |
|   |   | Conversion mode, PGA enabled, gain = 16, 32                   |                    | 165                  |                                |
|   |   | Conversion mode, PGA enabled, gain = 64                       |                    | 200                  |                                |
|   |   | Conversion mode, PGA enabled, gain = 128                      |                    | 250                  |                                |
| <b>ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 3.3 V)</b>  |   |   |                    |                      |                                |
| $I_{\text{AVDD}}$   | Analog supply current   | Internal 2.5-V reference, no external load                    |                    | 185                  | $\mu\text{A}$                  |
|   |   | Positive reference buffer                                     |                    | 35                   |                                |
|   |   | Negative reference buffer                                     |                    | 25                   |                                |
|   |   | VBIAS buffer, no external load                                |                    | 10                   |                                |
|   |   | IDAC overhead, 10 $\mu\text{A}$ to 250 $\mu\text{A}$          |                    | 20                   |                                |
|   |   | IDAC overhead, 500 $\mu\text{A}$ to 750 $\mu\text{A}$         |                    | 30                   |                                |
|   |   | IDAC overhead, 1 mA   |                    | 40                   |                                |
|   |   | IDAC overhead, 1.5 mA   |                    | 50                   |                                |
|   |   | IDAC overhead, 2 mA   |                    | 65                   |                                |
| <b>DIGITAL SUPPLY CURRENT (DVDD = IOVDD = 3.3 V, All Data Rates, SPI Not Active)</b>  |   |   |                    |                      |                                |
| $I_{\text{DVDD}} + I_{\text{IOVDD}}$  | Digital supply current  | Power-down mode, internal oscillator                          |                    | 0.1                  | $\mu\text{A}$                  |
|   |   | Standby mode, internal oscillator                             |                    | 185                  |                                |
|   |   | Conversion mode, internal oscillator                          |                    | 225                  |                                |
|   |   | Conversion mode, external $f_{\text{CLK}} = 4.096\text{ MHz}$ |                    | 195                  |                                |
| <b>POWER DISSIPATION (AVDD = DVDD = IOVDD = 3.3 V, Internal Reference Enabled, Reference Buffers Disabled, IDACs Disabled, VBIAS Disabled, Internal Oscillator, All Data Rates, <math>V_{IN} = 0\text{ V}</math>, SPI Not Active)</b> |   |   |                    |                      |                                |
| $P_D$   | Power dissipation   | Conversion mode, PGA enabled, gain = 1                        |                    | 1.75                 | mW                             |

## 7.6 Timing Characteristics

over operating ambient temperature range, DVDD = 2.7 V to 3.6 V, IOVDD = DVDD to 5.25 V, and DOUT/DRDY load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

|                         |   | MIN  | MAX | UNIT <sup>(1)</sup> |
|-------------------------|---|------|-----|---------------------|
| <b>SERIAL INTERFACE</b> |   |      |     |                     |
| t <sub>d(CSSC)</sub>    | Delay time, first SCLK rising edge after $\overline{CS}$ falling edge   | 20   |     | ns                  |
| t <sub>d(SCCS)</sub>    | Delay time, $\overline{CS}$ rising edge after final SCLK falling edge   | 20   |     | ns                  |
| t <sub>w(CSH)</sub>     | Pulse duration, $\overline{CS}$ high  | 30   |     | ns                  |
| t <sub>c(SC)</sub>      | SCLK period   | 100  |     | ns                  |
| t <sub>w(SCH)</sub>     | Pulse duration, SCLK high   | 40   |     | ns                  |
| t <sub>w(SCL)</sub>     | Pulse duration, SCLK low  | 40   |     | ns                  |
| t <sub>su(DI)</sub>     | Setup time, DIN valid before SCLK falling edge  | 15   |     | ns                  |
| t <sub>h(DI)</sub>      | Hold time, DIN valid after SCLK falling edge  | 20   |     | ns                  |
| t <sub>d(CMD)</sub>     | Delay time, between bytes or commands   | 0    |     | ns                  |
| <b>RESET PIN</b>        |   |      |     |                     |
| t <sub>w(RSL)</sub>     | Pulse duration, $\overline{RESET}$ low  | 4    |     | t <sub>CLK</sub>    |
| t <sub>d(RSSC)</sub>    | Delay time, first SCLK rising edge after $\overline{RESET}$ rising edge (or 7th SCLK falling edge of RESET command)   | 4096 |     | t <sub>CLK</sub>    |
| <b>START/SYNC PIN</b>   |   |      |     |                     |
| t <sub>w(STH)</sub>     | Pulse duration, START/SYNC high   | 4    |     | t <sub>CLK</sub>    |
| t <sub>w(STL)</sub>     | Pulse duration, START/SYNC low  | 4    |     | t <sub>CLK</sub>    |
| t <sub>su(STDR)</sub>   | Setup time, START/SYNC falling edge (or 7th SCLK falling edge of STOP command) before $\overline{DRDY}$ falling edge to stop further conversions (continuous conversion mode) | 32   |     | t <sub>CLK</sub>    |

(1) t<sub>CLK</sub> = 1 / f<sub>CLK</sub>.

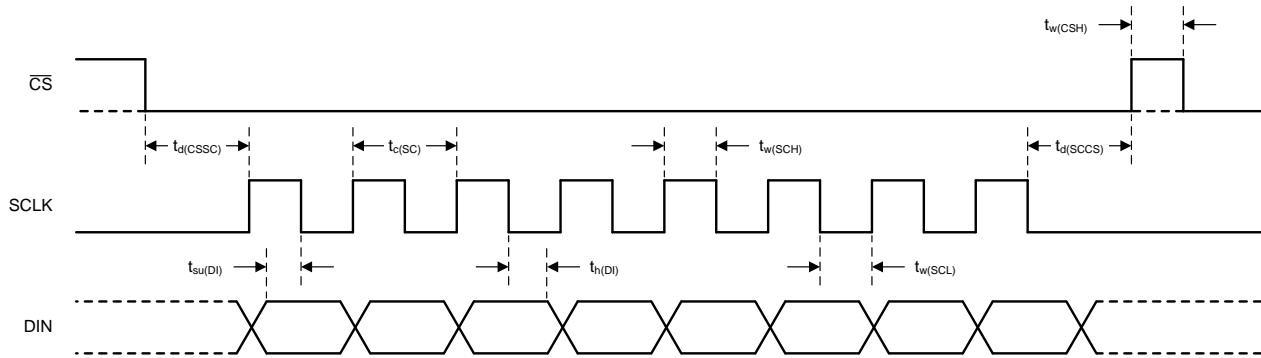
## 7.7 Switching Characteristics

over operating ambient temperature range, DVDD = 2.7 V to 3.6 V, IOVDD = DVDD to 5.25 V, and DOUT/DRDY load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

| PARAMETER             | TEST CONDITIONS   | MIN             | TYP | MAX | UNIT <sup>(1)</sup> |
|-----------------------|---|-----------------|-----|-----|---------------------|
| t <sub>p(CSDO)</sub>  | Propagation delay time, $\overline{CS}$ falling edge to DOUT driven   | 0               |     | 25  | ns                  |
| t <sub>p(SCDO)</sub>  | Propagation delay time, SCLK rising edge to valid new DOUT  | 3               |     | 30  | ns                  |
| t <sub>p(CSDOZ)</sub> | Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance  | 0               |     | 25  | ns                  |
| t <sub>p(STDR)</sub>  | Propagation delay time, START/SYNC rising edge (or first SCLK rising edge of any command or data read) to $\overline{DRDY}$ rising edge |                 |     | 2   | t <sub>CLK</sub>    |
| t <sub>w(DRH)</sub>   | Pulse duration, $\overline{DRDY}$ high  | 24              |     |     | t <sub>CLK</sub>    |
| t <sub>p(GPIO)</sub>  | Propagation delay time, last SCLK falling edge of WREG command to GPIOx output valid  | 3               |     | 100 | ns                  |
|                       | SPI timeout per 8 bits <sup>(2)</sup>   | 2 <sup>15</sup> |     |     | t <sub>CLK</sub>    |

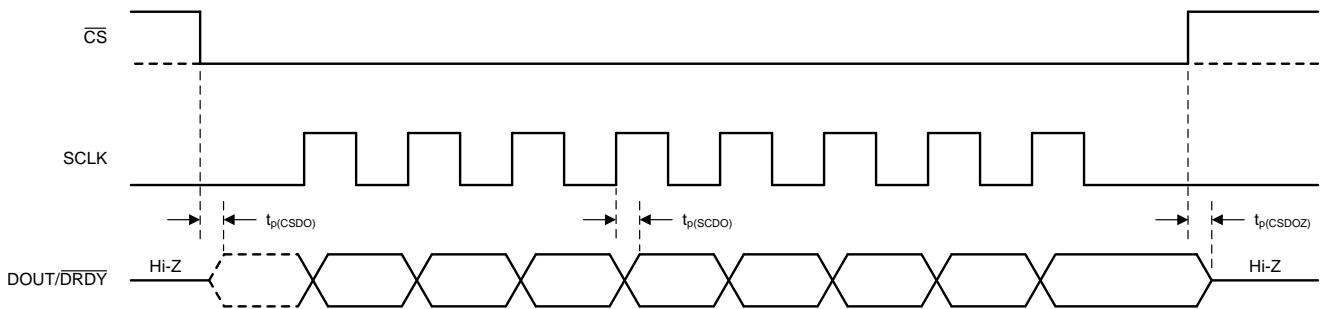
(1) t<sub>CLK</sub> = 1 / f<sub>CLK</sub>

(2) The SPI interface resets when an entire byte is not sent within the specified timeout time.



NOTE: Single-byte communication is shown. Actual communication can be multiple bytes.

Figure 1. Serial Interface Timing Requirements



NOTE: Single-byte communication is shown. Actual communication can be multiple bytes.

Figure 2. Serial Interface Switching Characteristics

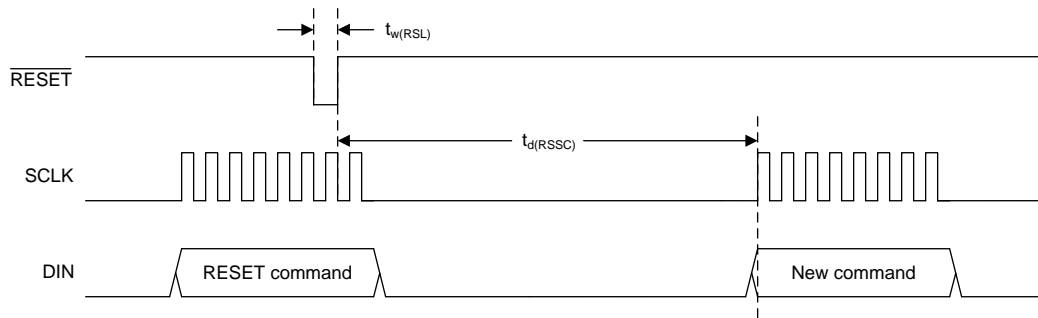


Figure 3.  $\overline{RESET}$  Pin and RESET Command Timing Requirements

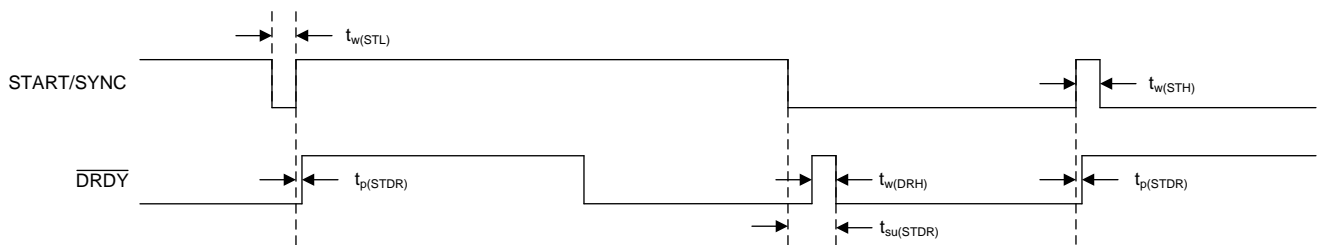
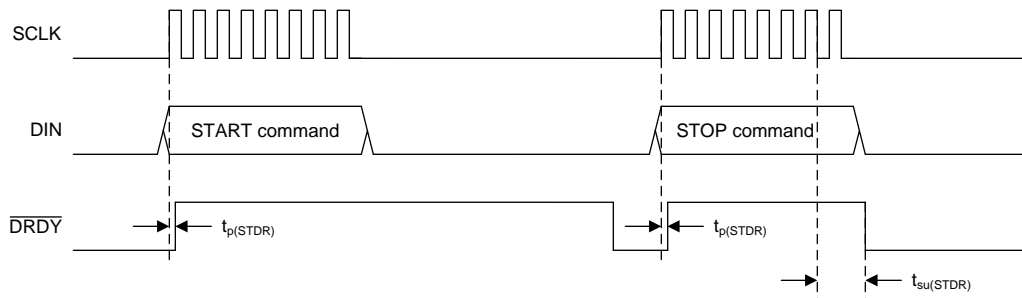
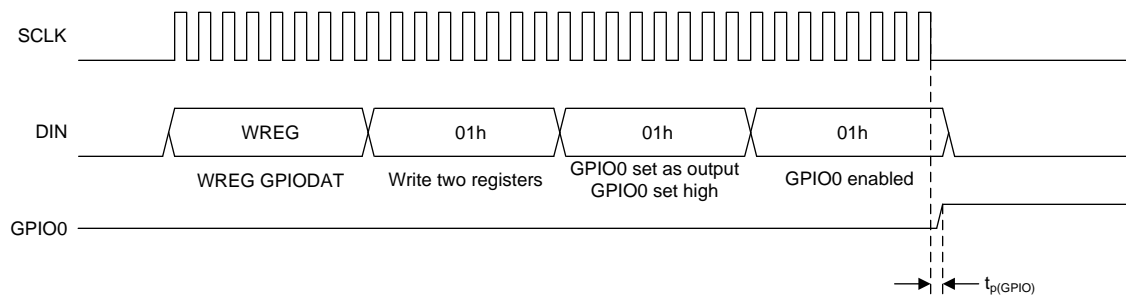


Figure 4. START/SYNC Pin Timing Requirements



**Figure 5. START Command Timing Requirements**



**Figure 6. GPIO Switching Characteristics**

## 7.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

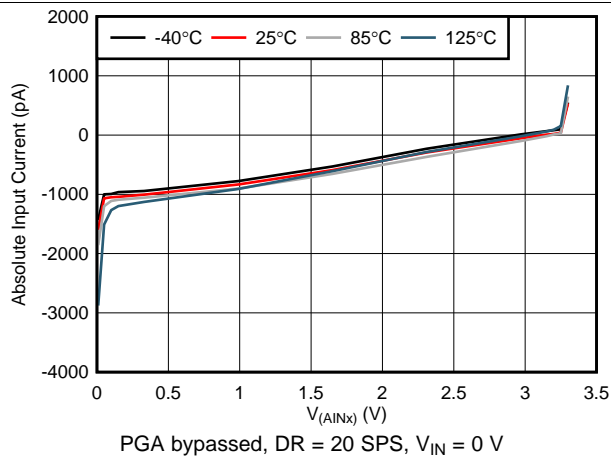


Figure 7. Absolute Input Current vs Absolute Input Voltage

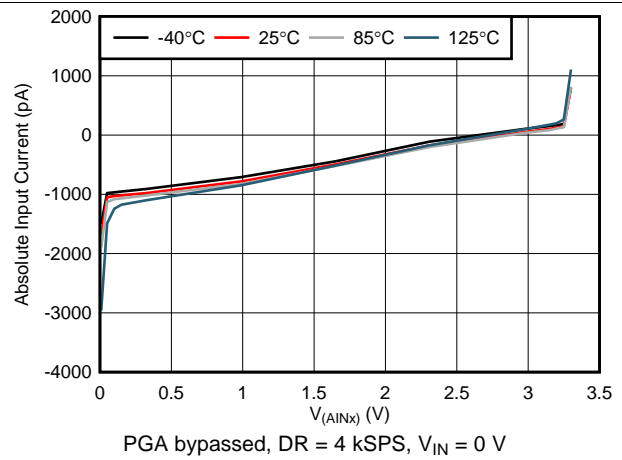


Figure 8. Absolute Input Current vs Absolute Input Voltage

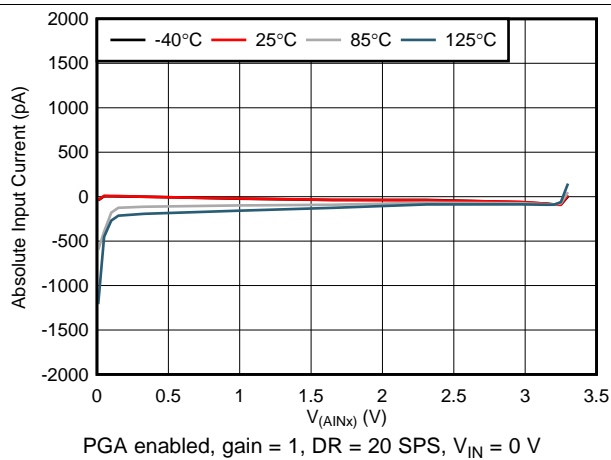


Figure 9. Absolute Input Current vs Absolute Input Voltage

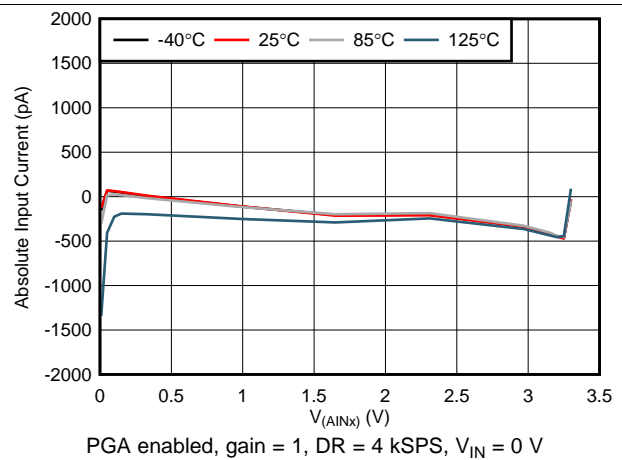


Figure 10. Absolute Input Current vs Absolute Input Voltage

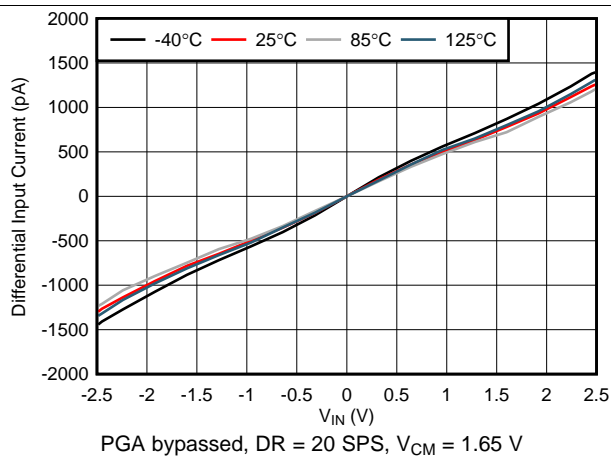


Figure 11. Differential Input Current vs Differential Input Voltage

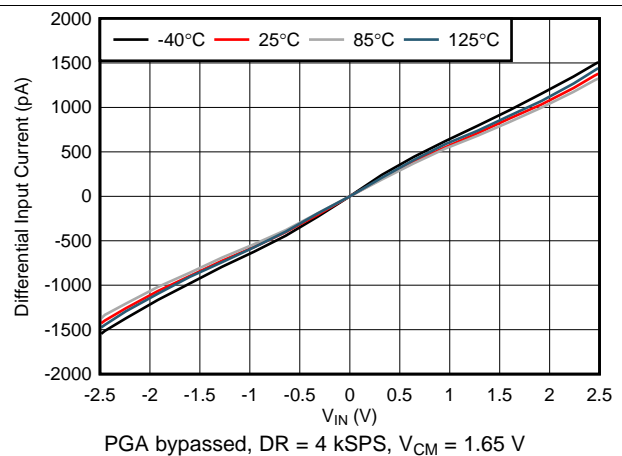
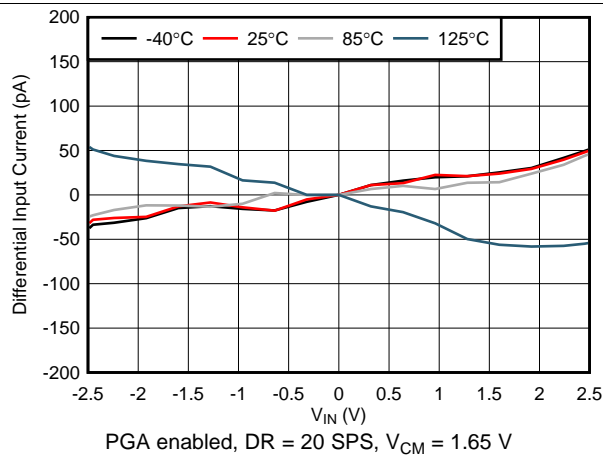


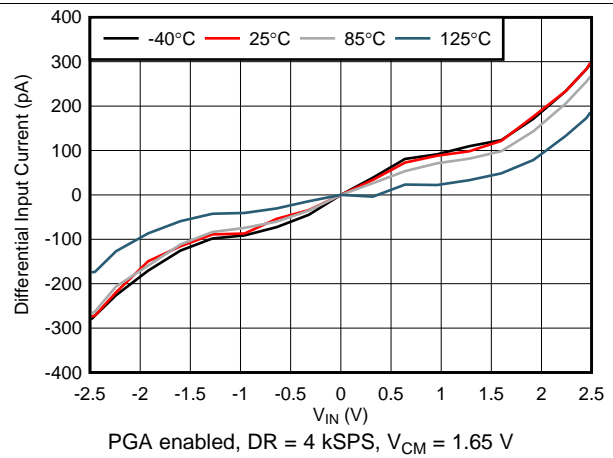
Figure 12. Differential Input Current vs Differential Input Voltage

### Typical Characteristics (continued)

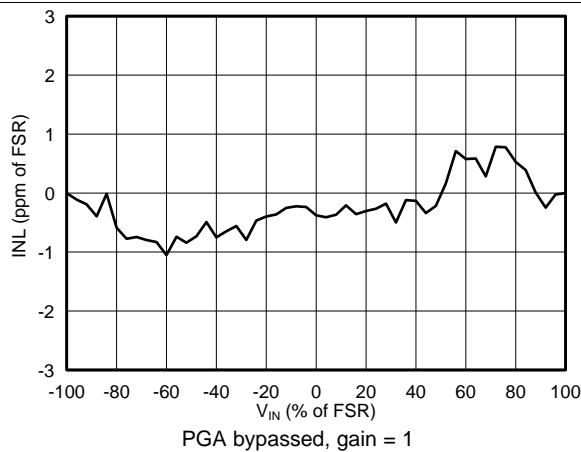
at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)



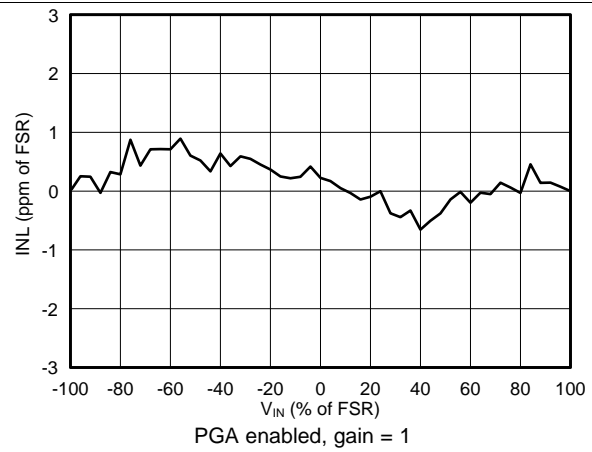
**Figure 13. Differential Input Current vs Differential Input Voltage**



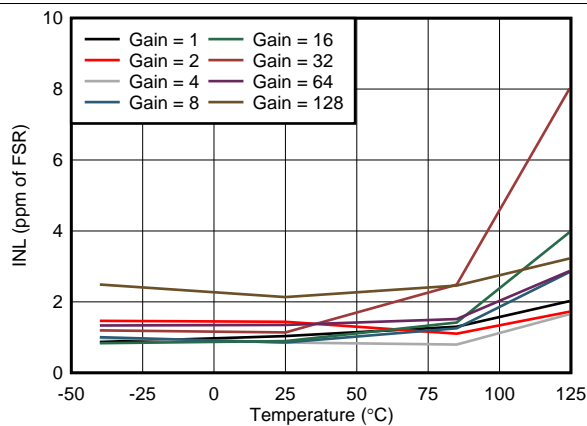
**Figure 14. Differential Input Current vs Differential Input Voltage**



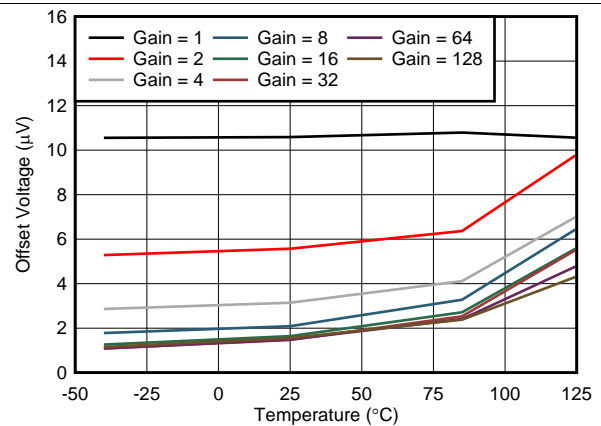
**Figure 15. INL vs Differential Input Voltage**



**Figure 16. INL vs Differential Input Voltage**



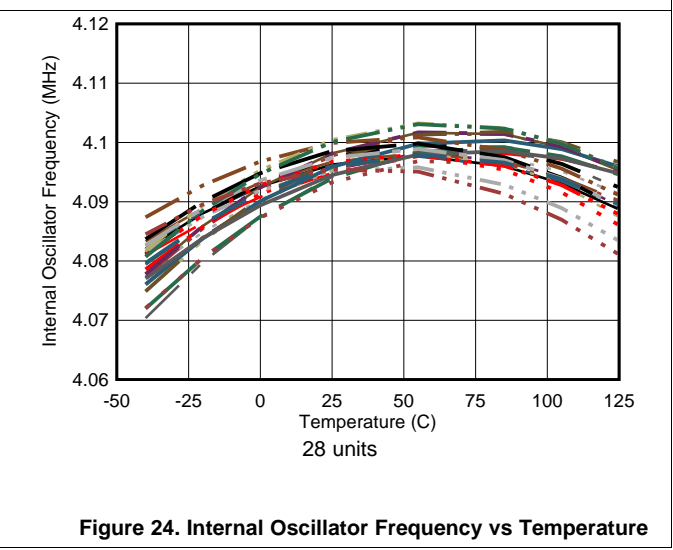
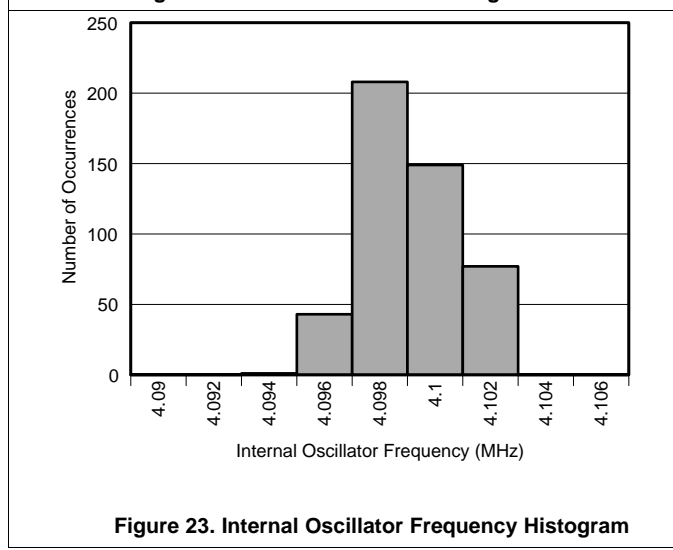
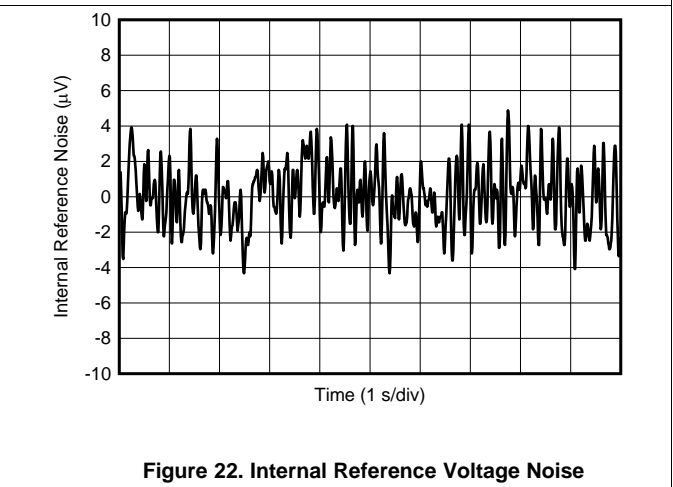
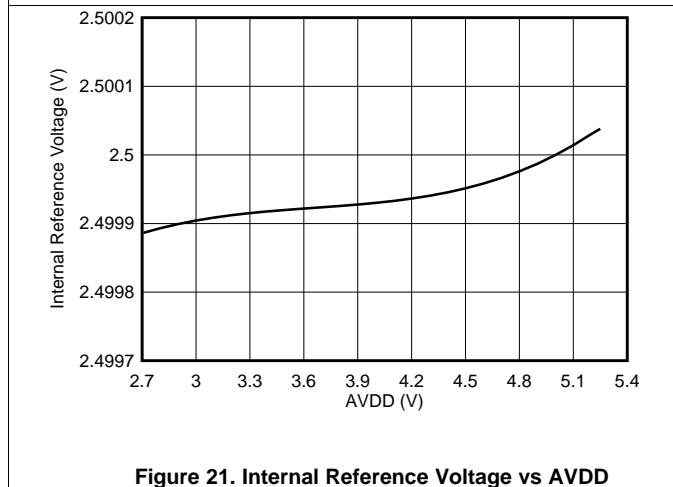
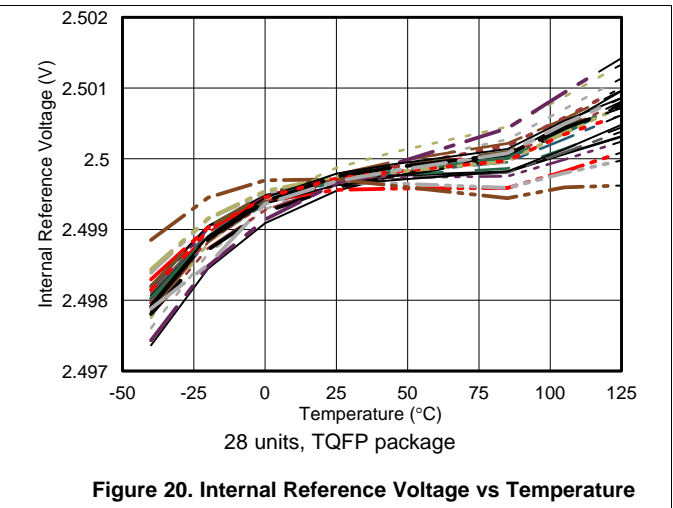
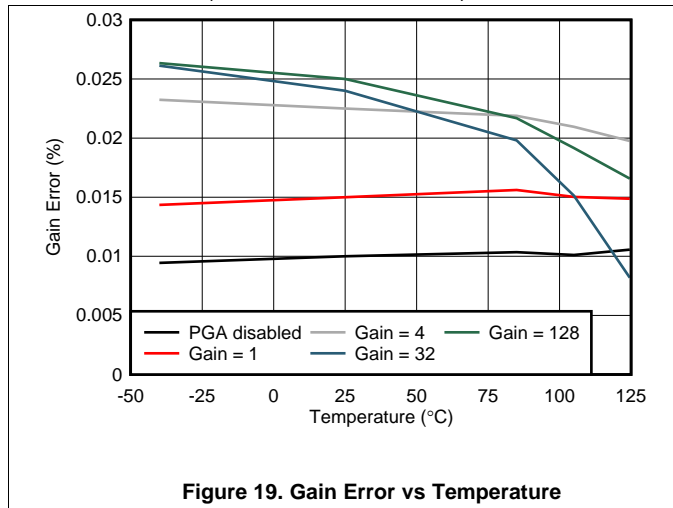
**Figure 17. INL vs Temperature**



**Figure 18. Offset Voltage vs Temperature**

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)



### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

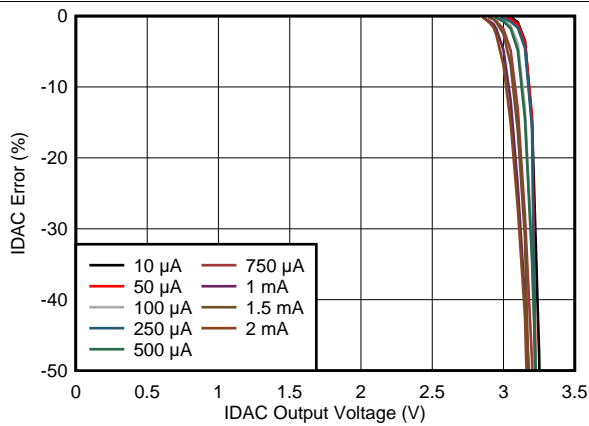


Figure 25. IDAC Accuracy vs Compliance Voltage

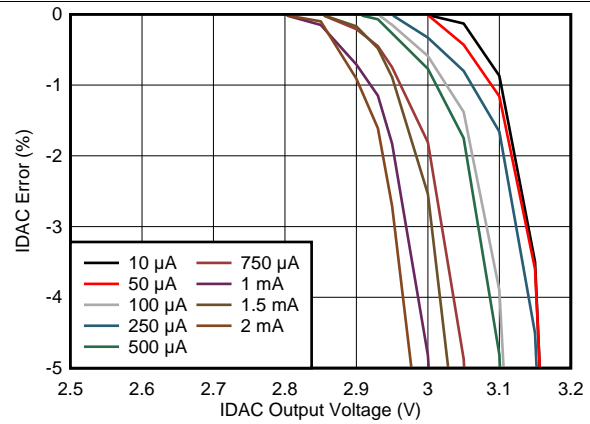


Figure 26. IDAC Accuracy vs Compliance Voltage

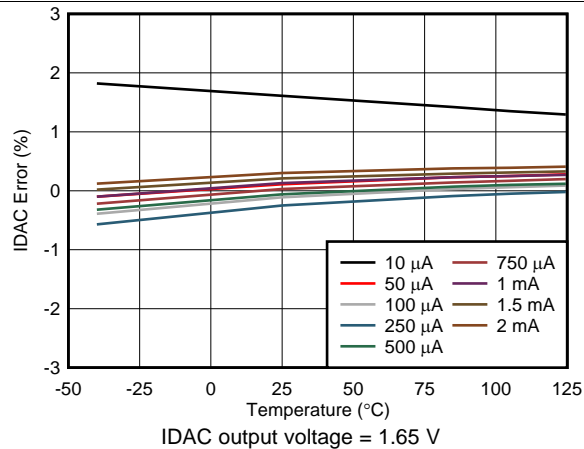


Figure 27. IDAC Accuracy vs Temperature

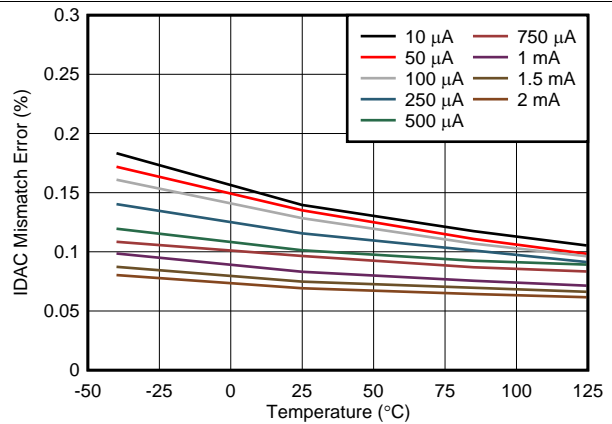


Figure 28. IDAC Matching vs Temperature

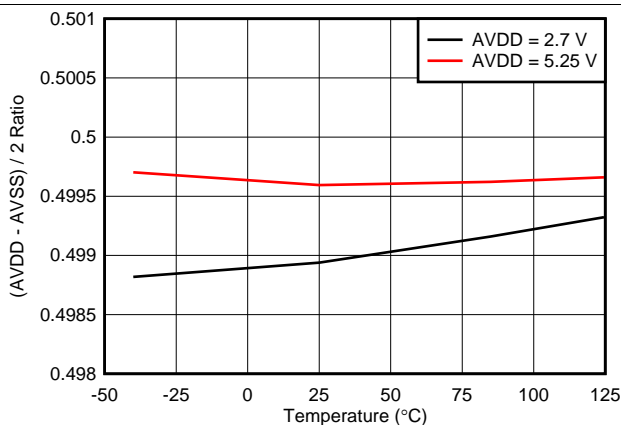


Figure 29. VBIAS Voltage  $[(AVDD - AVSS) / 2]$  vs Temperature

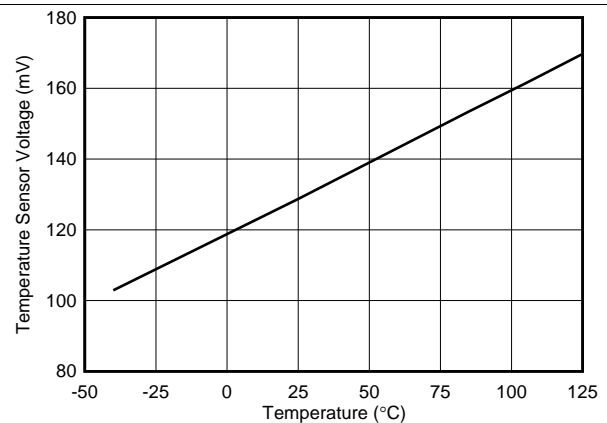


Figure 30. Temperature Sensor Voltage vs Temperature



Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

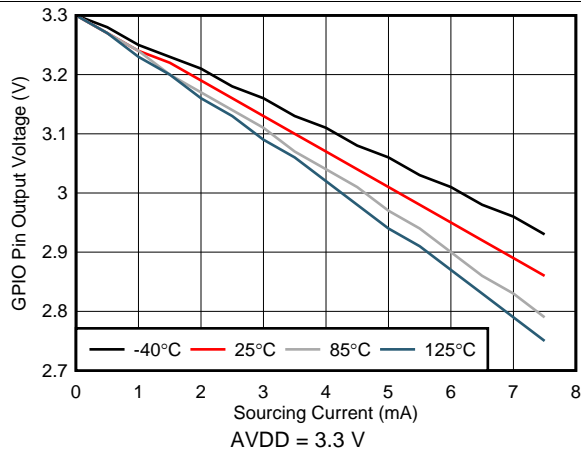


Figure 31. GPIO Pin Output Voltage vs Sourcing Current

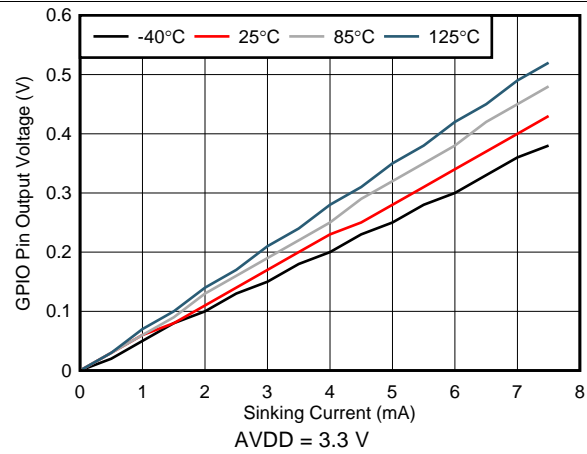


Figure 32. GPIO Pin Output Voltage vs Sinking Current

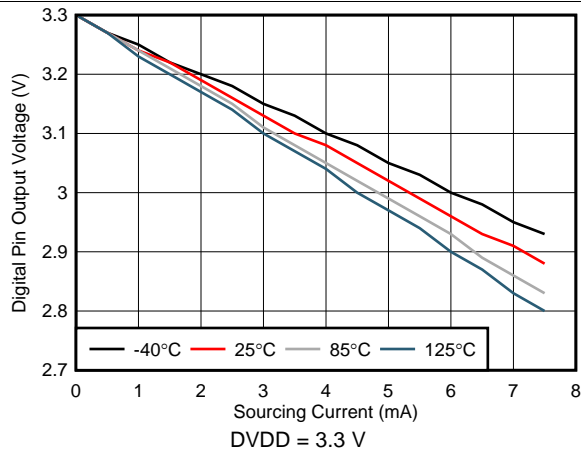


Figure 33. Digital Pin Output Voltage vs Sourcing Current

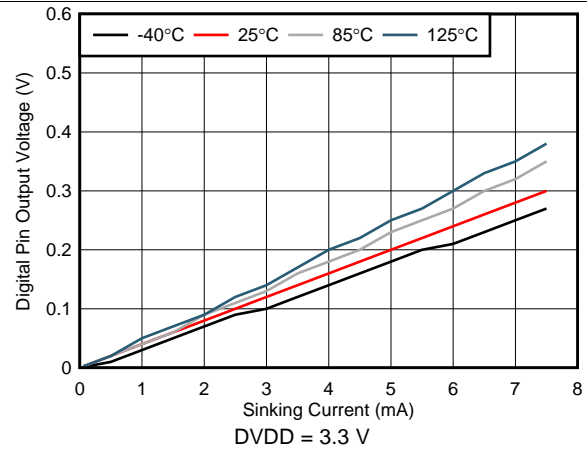


Figure 34. Digital Pin Output Voltage vs Sinking Current

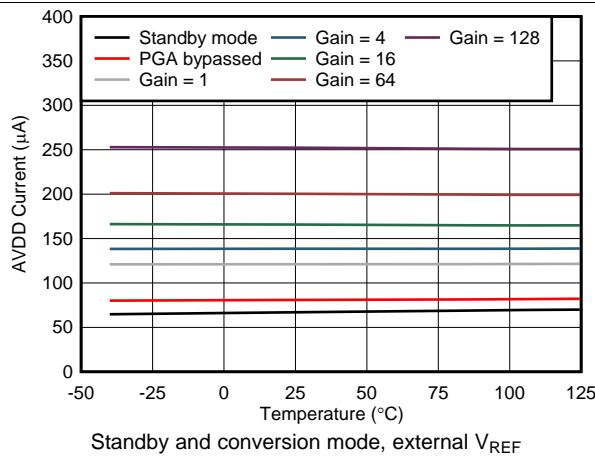


Figure 35. Analog Supply Current vs Temperature

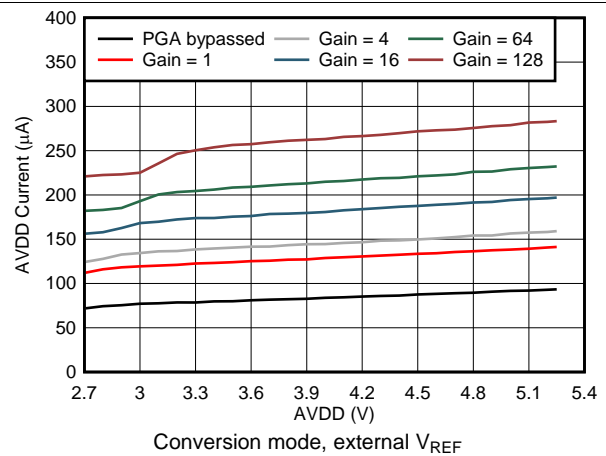


Figure 36. Analog Supply Current vs AVDD

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $AVSS = 0\text{ V}$ ,  $DVDD = IOVDD = 3.3\text{ V}$ , using internal  $V_{REF} = 2.5\text{ V}$ , internal 4.096-MHz oscillator, and PGA enabled (unless otherwise noted)

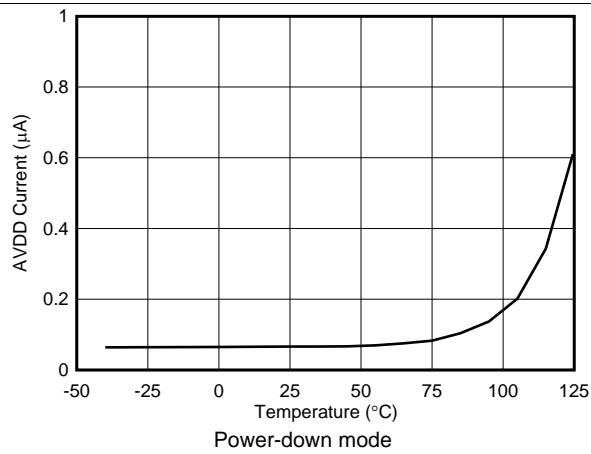


Figure 37. Analog Supply Current vs Temperature

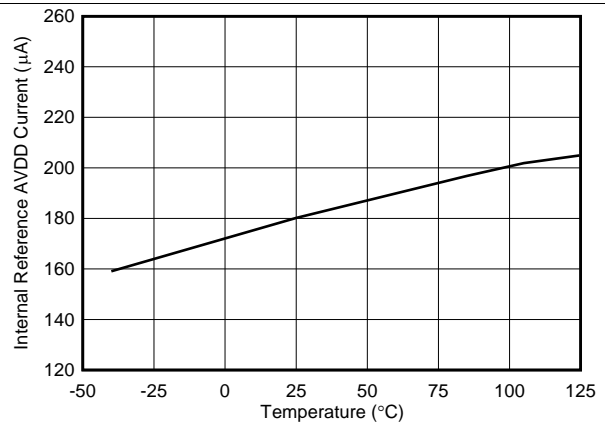


Figure 38. Internal Reference AVDD Current vs Temperature

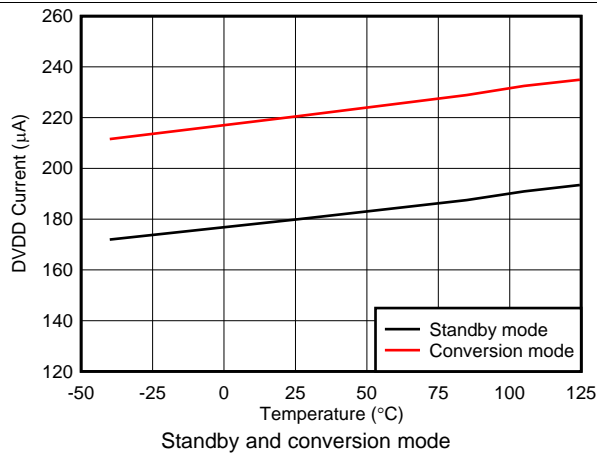


Figure 39. Digital Supply Current vs Temperature

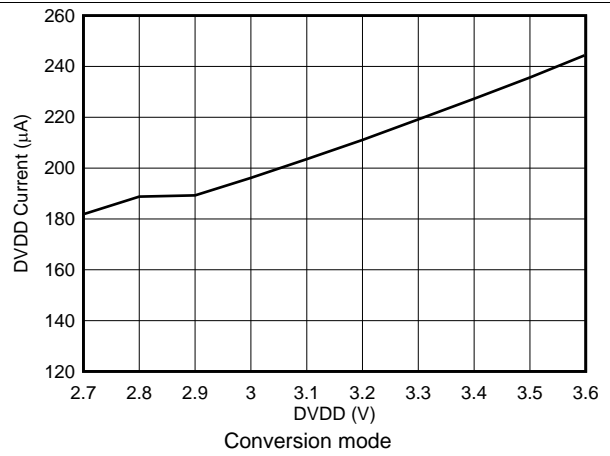


Figure 40. Digital Supply Current vs DVDD

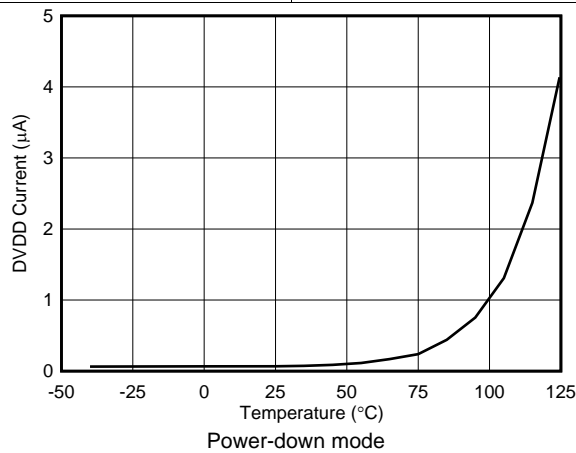


Figure 41. Digital Supply Current vs Temperature

## 8 Parameter Measurement Information

### 8.1 Noise Performance

Delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a  $\Delta\Sigma$  ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called the *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

[Table 1](#) and [Table 2](#) summarize the device noise performance. Data are representative of typical noise performance at  $T_A = 25^\circ\text{C}$  using the internal 2.5-V reference. Data shown are based on 512 consecutive samples from a single device with inputs internally shorted. [Table 1](#) lists the input-referred root mean square noise in units of  $\mu\text{V}_{\text{RMS}}$  for the conditions shown. Peak-to-peak ( $\mu\text{V}_{\text{PP}}$ ) values are shown in parentheses. [Table 2](#) lists the corresponding data in effective resolution calculated from  $\mu\text{V}_{\text{RMS}}$  values using [Equation 1](#). Noise-free resolution is calculated from  $\mu\text{V}_{\text{PP}}$  values using [Equation 2](#).

The input-referred noise ([Table 1](#)) only changes marginally when using an external low-noise reference, such as the [REF5025](#). To calculate effective resolution and noise-free resolution when using a reference voltage other than 2.5 V, use [Equation 1](#) and [Equation 2](#):

$$\text{Effective Resolution} = \ln[(2 \cdot V_{\text{REF}} / \text{Gain}) / V_{\text{RMS-Noise}}] / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln[(2 \cdot V_{\text{REF}} / \text{Gain}) / V_{\text{PP-Noise}}] / \ln(2) \quad (2)$$

Noise performance with the PGA bypassed are identical to the noise performance of the device with gain = 1.

**Table 1. Noise in  $\mu\text{V}_{\text{RMS}}$  ( $\mu\text{V}_{\text{PP}}$ ) at  $\text{AVDD} = 3.3 \text{ V}$ ,  $\text{AVSS} = 0 \text{ V}$ , PGA Enabled, and Internal 2.5-V Reference**

| DATA RATE (SPS) | GAIN        |             |             |           |           |           |           |             |
|-----------------|-------------|-------------|-------------|-----------|-----------|-----------|-----------|-------------|
|                 | 1           | 2           | 4           | 8         | 16        | 32        | 64        | 128         |
| 2.5             | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 5               | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 10              | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 16.6            | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 20              | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 50              | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.60) |
| 60              | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.2) | 0.60 (0.90) |
| 100             | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.4) | 0.60 (1.3)  |
| 200             | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.4) | 1.2 (1.9) | 0.60 (1.7)  |
| 400             | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (2.8) | 1.2 (2.9) | 0.60 (2.3)  |
| 800             | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (4.0) | 1.2 (3.8) | 0.60 (3.2)  |
| 1000            | 76.3 (76.3) | 38.1 (38.1) | 19.1 (19.1) | 9.5 (9.5) | 4.8 (4.8) | 2.4 (5.1) | 1.2 (4.3) | 0.60 (3.8)  |
| 2000            | 76.3 (83)   | 38.1 (80)   | 19.1 (32)   | 9.5 (17)  | 4.8 (11)  | 2.4 (6.7) | 1.2 (6.6) | 1.0 (6.5)   |
| 4000            | 103 (629)   | 38.1 (404)  | 24 (160)    | 12 (70)   | 6.4 (39)  | 3.3 (21)  | 3.1 (21)  | 2.6 (20)    |

**Table 2. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise)  
at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, and Internal 2.5-V Reference**

| DATA RATE (SPS) | GAIN      |           |             |           |             |             |             |             |
|-----------------|-----------|-----------|-------------|-----------|-------------|-------------|-------------|-------------|
|                 | 1         | 2         | 4           | 8         | 16          | 32          | 64          | 128         |
| 2.5             | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (16)     |
| 5               | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (16)     |
| 10              | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (16)     |
| 16.6            | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (16)     |
| 20              | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (16)     |
| 50              | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (15.5)   |
| 60              | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (16)     | 16 (15.4)   |
| 100             | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (15.8)   | 16 (14.9)   |
| 200             | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (16)     | 16 (15.3)   | 16 (14.5)   |
| 400             | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (15.8)   | 16 (14.7)   | 16 (14.0)   |
| 800             | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (16)     | 16 (15.2)   | 16 (14.3)   | 16 (13.6)   |
| 1000            | 16 (16)   | 16 (16)   | 16 (16)     | 16 (16)   | 16 (15.8)   | 16 (14.9)   | 16 (14.2)   | 16 (13.3)   |
| 2000            | 16 (15.9) | 16 (14.9) | 16 (15.3)   | 16 (15.2) | 16 (14.8)   | 16 (14.5)   | 16 (13.5)   | 15.2 (12.6) |
| 4000            | 16 (13.0) | 16 (12.6) | 15.7 (12.9) | 16 (13.1) | 15.6 (13.0) | 15.5 (12.9) | 14.4 (11.9) | 13.6 (10.9) |

## 9 Detailed Description

### 9.1 Overview

The ADS114S06B and ADS114S08B are precision 16-bit, delta-sigma ( $\Delta\Sigma$ ) ADCs with an integrated analog front end (AFE) to simplify precision sensor connections. The ADC provides output data rates from 2.5 SPS to 4000 SPS for flexibility in resolution and data rates over a wide range of applications. The low-noise and low-drift architecture make these devices suitable for precise measurement of low-voltage sensors, such as load cells and temperature sensors.

The ADS114S0xB incorporate several features that simplify precision sensor measurements. Key integrated features include:

- Low-noise, CMOS PGA
- Low-drift, 2.5-V voltage reference
- Two sets of buffered external reference inputs
- Dual, matched, sensor-excitation current sources (IDACs)
- Internal 4.096-MHz oscillator
- Temperature sensor
- Four general-purpose input/output pins (GPIOs)

As described in the [Functional Block Diagram](#) section, these devices provide 12 (ADS114S08B) or six (ADS114S06B) analog inputs that are configurable as either single-ended inputs, differential inputs, or any combination of the two. Many of the analog inputs have additional features as programmed by the user. The analog inputs can be programmed to enable the following extended features:

- Two sensor excitation current sources: all analog input pins (and REFP1 and REFN1 on the ADS114S06B)
- Sensor biasing voltage (VBIAS): pins AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AINCOM
- Four GPIO pins: AIN8, AIN9, AIN10, AIN11 (ADS114S08B only, the ADS114S06B has dedicated GPIOs)
- Sensor burn-out current sources: analog input pins selected for ADC input

Following the input multiplexer (MUX), the ADC features a high input-impedance, low-noise, programmable gain amplifier (PGA), eliminating the need for an external amplifier. The PGA gain is programmable from 1 to 128 in binary steps. The PGA can be bypassed to allow the input range to extend 50 mV below ground or above supply.

An inherently stable delta-sigma modulator measures the ratio of the input voltage to the reference voltage to provide the ADC result. The ADC operates with the internal 2.5-V reference, or with up to two external reference inputs. The REFOUT pin provides the buffered 2.5-V internal voltage reference output that can be used to bias external circuitry.

The digital filter provides settled data with 50-Hz and 60-Hz line-cycle rejection at data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS, 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and 60-Hz rejection at a data rate of 60 SPS.

Two programmable excitation current sources provide bias to resistive sensors [such as resistance temperature detectors (RTDs) or thermistors]. The ADC integrates several system monitors for read back, such as temperature sensor and supply monitors. Four GPIO pins are available as either dedicated pins (ADS114S06B) or combined with analog input pins (ADS114S08B).

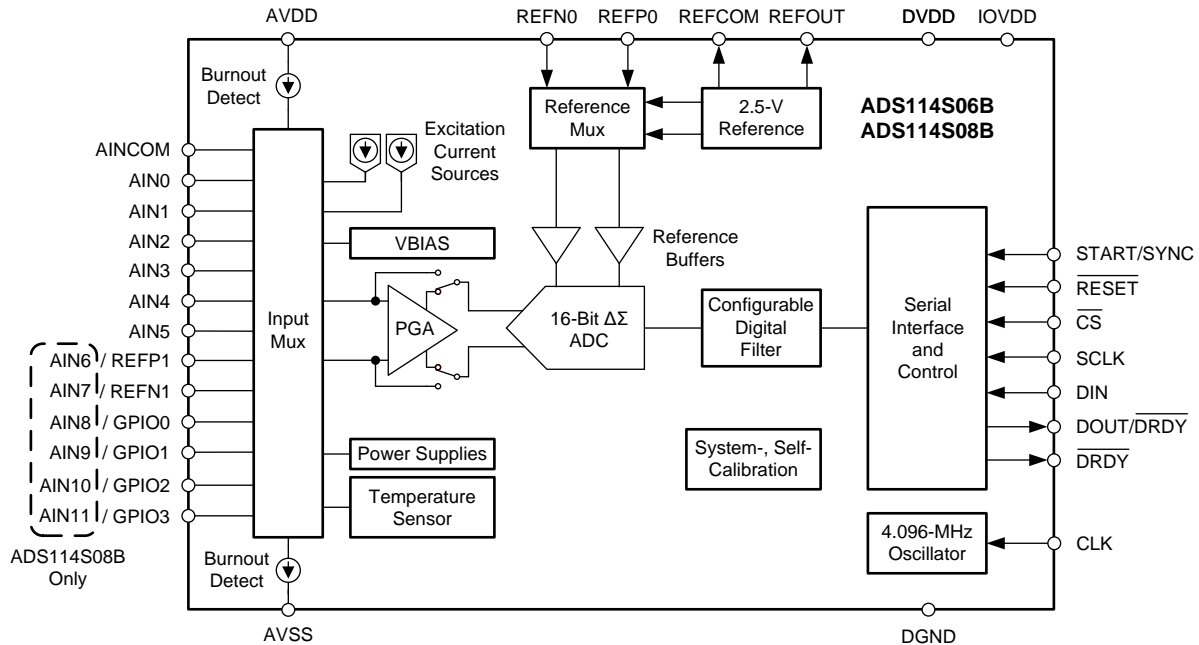
The ADS114S0xB system clock is either provided by the internal low-drift, 4.096-MHz oscillator or an external clock source on the CLK input.

The SPI-compatible serial interface is used to read the conversion data and also to configure and control the ADC. The serial interface consists of four signals: CS, SCLK, DIN, and DOUT/DRDY. The dual function DOUT/DRDY output indicates when conversion data are ready and also provides the data output. The serial interface can be implemented with as little as three connections by tying CS low. Start ADC conversions with either the START/SYNC pin or with commands. The ADC can be programmed for a continuous conversion mode or to perform single-shot conversions.

## Overview (continued)

The AVDD analog supply operates with bipolar supplies from  $\pm 1.5$  V to  $\pm 2.625$  V or with a unipolar supply from 2.7 V to 5.25 V. For unipolar-supply operation, use the VBIAS voltage to bias isolated (floating) sensors. The digital supplies operate with unipolar supplies only. The DVDD digital power supply operates from 2.7 V to 3.6 V and the IOVDD supply operates from DVDD to 5.25 V.

## 9.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

## 9.3 Feature Description

### 9.3.1 Multiplexer

The ADS114S0xB contains a flexible input multiplexer; see [Figure 42](#). Select any of the six (ADS114S06B) or 12 (ADS114S08B) analog inputs as the positive or negative input for the PGA using the MUX\_P[3:0] and MUX\_N[3:0] bits in the input multiplexer register (02h). In addition, AINCOM can be selected as the positive or negative PGA input. AINCOM is treated as a regular analog input, as is AINx. Use AINCOM in single-ended measurement applications as the common input for the other analog inputs.

The multiplexer also routes the excitation current sources to drive resistive sensors (bridges, RTDs, and thermistors) and can provide bias voltages for unbiased sensors (unbiased thermocouples for example) to analog input pins.

The ADS114S0xB also contain a set of system monitor functions measured through the multiplexer. The inputs can be shorted together at mid-supply  $[(AVDD + AVSS) / 2]$  to measure and calibrate the input offset of the analog front-end and the ADC. The system monitor also includes a temperature sensor that provides a measurement of the device temperature. The system monitor can also measure the analog and digital supplies, measuring  $[(AVDD - AVSS) / 4]$  for the analog supply or  $DVDD / 4$  for the digital supply. Finally, the system monitor contains a set of burn-out current sources that pull the inputs to either supply if the sensor has burned out and has a high impedance so that the ADC measures a full-scale reading.

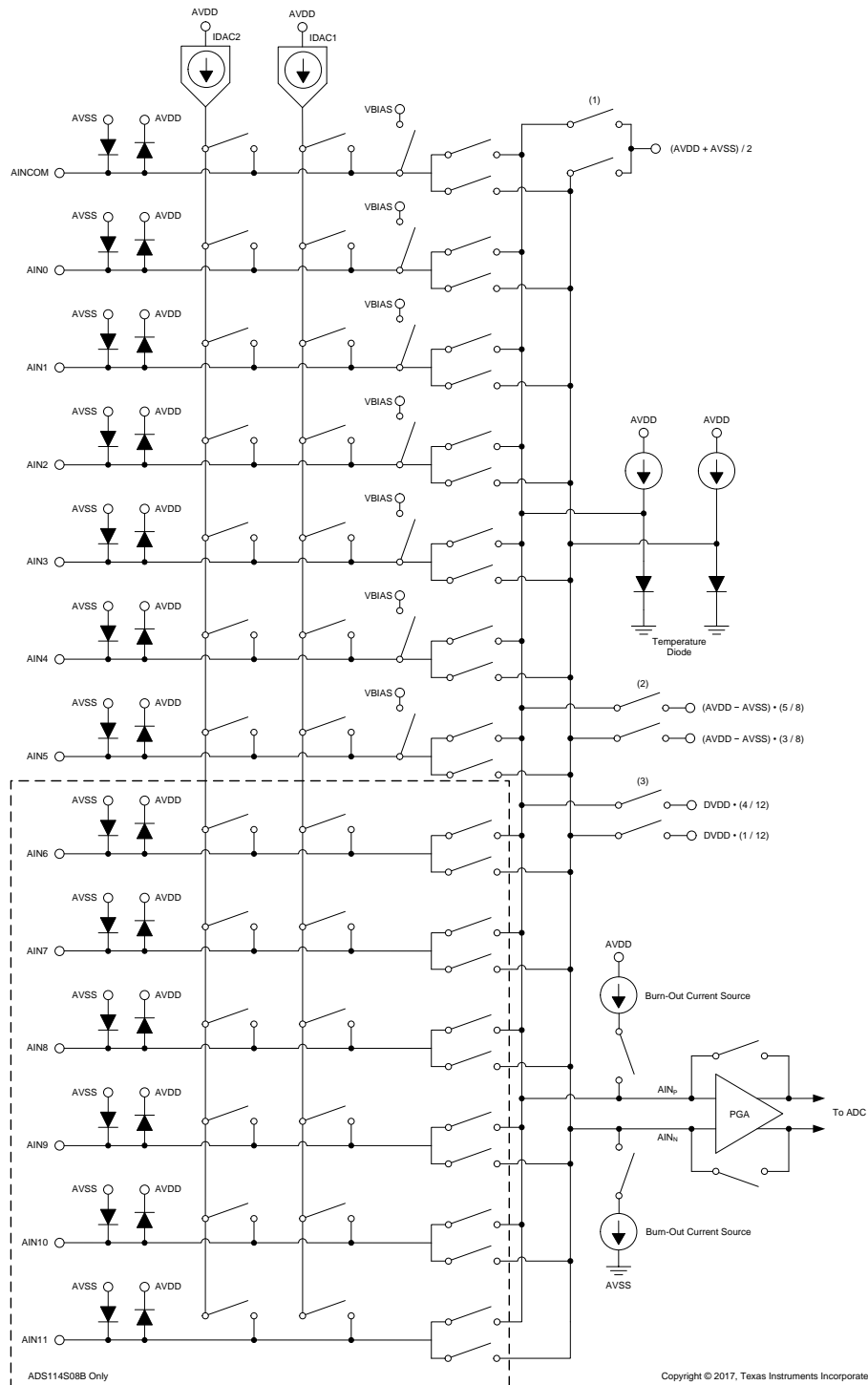
The multiplexer implements a break-before-make circuit. When changing the multiplexer channels using the MUX\_P[3:0] and MUX\_N[3:0] bits, the device first disconnects the PGA inputs from the analog inputs and connects them to mid-supply for  $2 \cdot t_{CLK}$ . In the next step, the PGA inputs connect to the selected new analog input channels. This break-before-make behavior ensures the ADC always starts from a known state and that the analog inputs are not momentarily shorted together.

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by [Equation 3](#):

$$AVSS - 0.3 \text{ V} < V_{(AINx)} < AVDD + 0.3 \text{ V} \quad (3)$$

External Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the [Absolute Maximum Ratings](#) table). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

Feature Description (continued)



- (1)  $AIN_P$  and  $AIN_N$  are connected together to  $(AVDD + AVSS) / 2$  for offset measurement.
- (2) Measurement for the analog supply equivalent to  $(AVDD - AVSS) / 4$ .
- (3) Measurement for the analog supply equivalent to  $DVDD / 4$ .

Figure 42. Analog Input Multiplexer



## Feature Description (continued)

### 9.3.2 Low-Noise Programmable Gain Amplifier

The ADS114S06B and ADS114S08B feature a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). Figure 43 shows a simplified diagram of the PGA. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter and an antialiasing filter on the output.

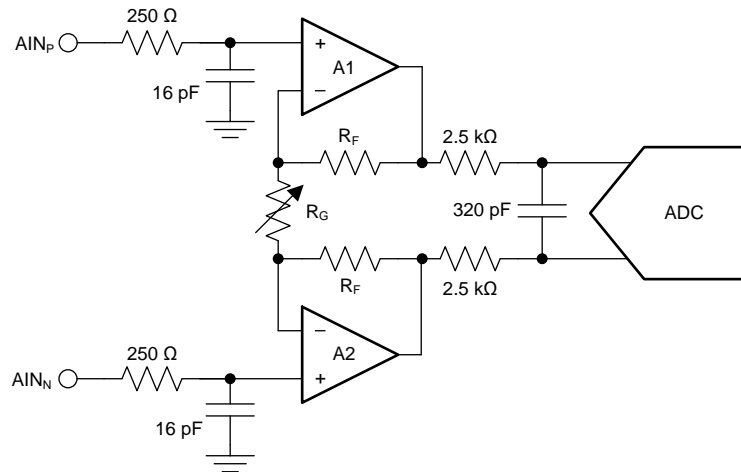


Figure 43. Simplified PGA Diagram

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128 using the GAIN[2:0] bits in the gain setting register (03h). Gain is changed inside the device using a variable resistor,  $R_G$ . The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 4:

$$\text{FSR} = \pm V_{\text{REF}} / \text{Gain} \quad (4)$$

Table 3 shows the corresponding full-scale ranges when using the internal 2.5-V reference.

Table 3. PGA Full-Scale Range

| GAIN SETTING | FSR           |
|--------------|---------------|
| 1            | $\pm 2.5$ V   |
| 2            | $\pm 1.25$ V  |
| 4            | $\pm 0.625$ V |
| 8            | $\pm 0.313$ V |
| 16           | $\pm 0.156$ V |
| 32           | $\pm 0.078$ V |
| 64           | $\pm 0.039$ V |
| 128          | $\pm 0.020$ V |

The PGA must be enabled with the PGA\_EN[1:0] bits of the gain setting register (03h). Setting these bits to 00 powers down and bypasses the PGA. A setting of 01 enables the PGA. The 10 and 11 settings are reserved and must not be written to the device.

With the PGA enabled, gains 64 and 128 are established in the digital domain. When the device is set to 64 or 128, the PGA is set to a gain of 32, and additional gain is established with digital scaling. The input-referred noise does still improve compared to the gain = 32 setting because the PGA is biased with a higher supply current to reduce noise.

### 9.3.2.1 PGA Input-Voltage Requirements

As with many amplifiers, the PGA has an absolute input voltage range requirement that cannot be exceeded. The maximum and minimum absolute input voltages are limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages ( $V_{AINP}$  and  $V_{AINN}$ ) depend on the PGA gain, the maximum differential input voltage ( $V_{INMAX}$ ), and the tolerance of the analog power-supply voltages ( $AVDD$  and  $AVSS$ ). Use the maximum voltage expected in the application for  $V_{INMAX}$ . The absolute positive and negative input voltages must be within the specified range, as shown in Equation 5:

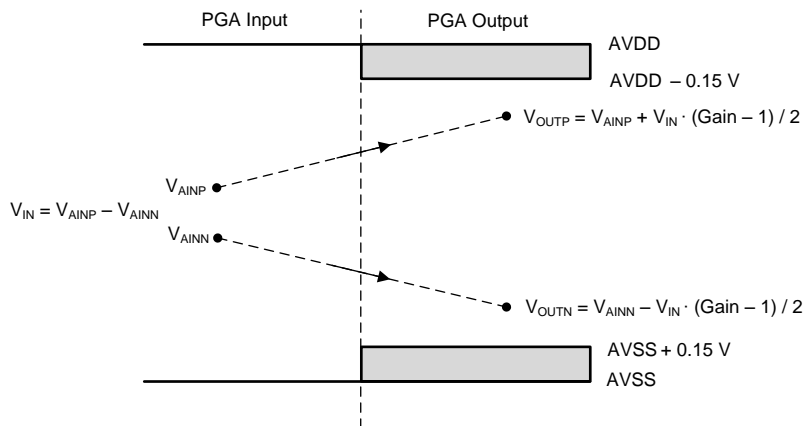
$$AVSS + 0.15 \text{ V} + |V_{INMAX}| \cdot (\text{Gain} - 1) / 2 < V_{AINP}, V_{AINN} < AVDD - 0.15 \text{ V} - |V_{INMAX}| \cdot (\text{Gain} - 1) / 2$$

where

- $V_{AINP}, V_{AINN}$  = absolute input voltage
  - $V_{INMAX} = V_{AINP} - V_{AINN}$  = maximum differential input voltage
- (5)

As mentioned in the previous section, PGA gain settings of 64 and 128 are scaled in the digital domain and are not implemented with the amplifier. When using the PGA in gains of 64 and 128, set the gain in Equation 5 to 32 to calculate the absolute input voltage range.

The relationship between the PGA input to the PGA output is shown graphically in Figure 44. The PGA output voltages ( $V_{OUTP}$ ,  $V_{OUTN}$ ) depend on the PGA gain and the input voltage magnitudes. For linear operation, the PGA output voltages must not exceed  $AVDD - 0.15 \text{ V}$  or  $AVSS + 0.15 \text{ V}$ . Note that the diagram depicts a positive differential input voltage that results in a positive differential output voltage.



**Figure 44. PGA Input/Output Range**

Download the [ADS1x4S0x design calculator](http://www.ti.com) from [www.ti.com](http://www.ti.com). This calculator can be used to determine the input voltage range of the PGA.

### 9.3.2.2 Bypassing the PGA

At a gain of 1, the device can be configured to disable and bypass the low-noise PGA. Disabling the PGA lowers the overall power consumption and also removes the restrictions of Equation 5 for the input voltage range. If the PGA is bypassed, the ADC absolute input voltage range extends beyond the  $AVDD$  and  $AVSS$  power supplies, allowing input voltages at or below ground. The absolute input voltage range when the PGA is bypassed is shown in Equation 6:

$$AVSS - 0.05 \text{ V} < V_{AINP}, V_{AINN} < AVDD + 0.05 \text{ V}$$
(6)

In order to measure single-ended signals that are referenced to  $AVSS$  ( $AIN_P = V_{IN}$ ,  $AIN_N = AVSS$ ), the PGA must be bypassed. The PGA is bypassed and powered down by setting the  $PGA\_EN[1:0]$  bits to 00 in the gain setting register (03h).

For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

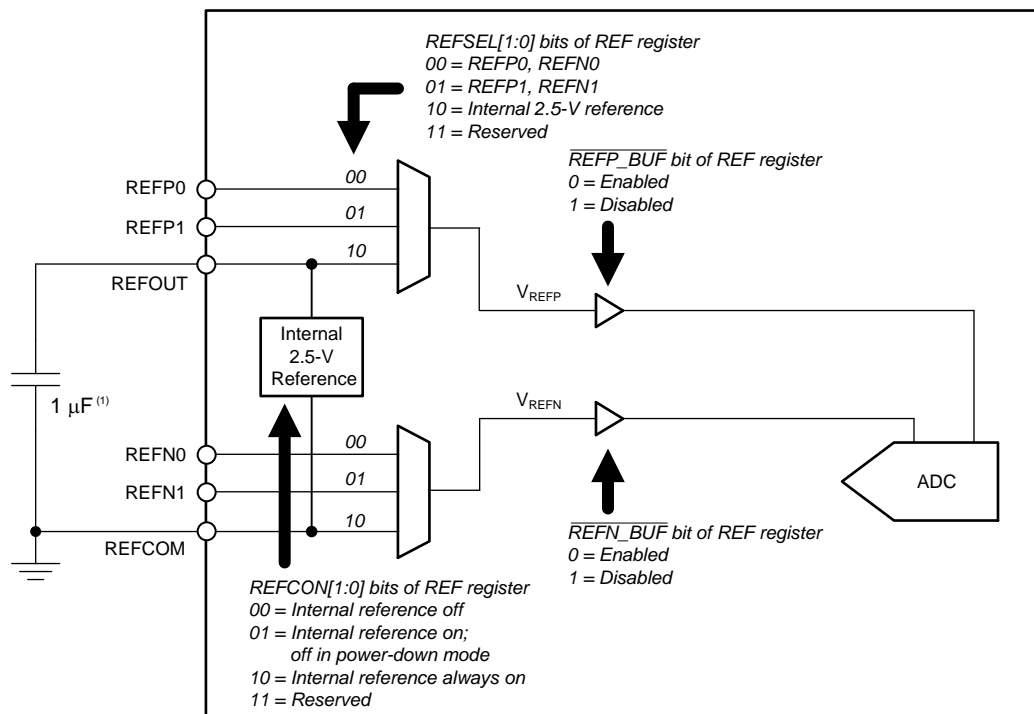
### 9.3.3 Voltage Reference

The devices require a reference voltage for operation. The ADS114S0xB offers an integrated low-drift 2.5-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the ADS114S08B offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1). The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs, whereas REFP1 and REFN1 are shared with inputs AIN6 and AIN7 (respectively) on the ADS114S08B. The specified external reference voltage range is 0.5 V to AVDD. The reference voltage is shown in Equation 7, where  $V_{(REFPx)}$  and  $V_{(REFNx)}$  are the absolute positive and absolute negative reference voltages.

$$V_{REF} = V_{(REFPx)} - V_{(REFNx)} \quad (7)$$

The polarity of the reference voltage internal to the ADC must be positive. The magnitude of the reference voltage together with the PGA gain establishes the ADC full-scale differential input range as defined by  $FSR = \pm V_{REF} / \text{Gain}$ .

Figure 45 shows the block diagram of the reference multiplexer. The ADC reference multiplexer selects between the internal reference and two external references (REF0 and REF1). The reference multiplexer is programmed with the REFSEL[1:0] bits in the reference control register (05h). By default, the external reference pair REFP0, REFN0 is selected.



(1) The internal reference requires a minimum 1-μF capacitor connected from REFOUT to REFCOM.

Figure 45. Reference Multiplexer Block Diagram

### 9.3.3.1 Internal Reference

The ADC integrates a precision, low-drift, 2.5-V reference. The internal reference is enabled by setting REFCON[1:0] to 10 (reference is always on) or 01 (reference is on, but powers down in power-down mode) in the reference control register (05h). By default, the internal voltage reference is powered down. To select the internal reference for use with the ADC, set the REFSEL[1:0] bits to 10. The REFOUT pin provides a buffered reference output voltage when the internal reference voltage is enabled. The negative reference output is the REFCOM pin, as shown in [Figure 45](#). Connect a capacitor in the range of 1  $\mu$ F to 47  $\mu$ F between REFOUT and REFCOM. Larger capacitor values help filter more noise at the expense of a longer reference start-up time.

The capacitor is not required if the internal reference is not used. However, the internal reference must be powered on if using the IDACs.

The internal reference requires a start-up time that must be accounted for before starting a conversion, as shown in [Table 4](#).

**Table 4. Internal Reference Settling Time**

| REFOUT CAPACITOR | SETTLING ERROR | SETTLING TIME (ms) |
|------------------|----------------|--------------------|
| 1 $\mu$ F        | 0.01%          | 4.5                |
|                  | 0.001%         | 5.9                |
| 10 $\mu$ F       | 0.01%          | 4.9                |
|                  | 0.001%         | 6.3                |
| 47 $\mu$ F       | 0.01%          | 5.5                |
|                  | 0.001%         | 7.0                |

### 9.3.3.2 External Reference

The ADS114S0xB provides two external reference inputs selectable through the reference multiplexer. The reference inputs are differential with independent positive and negative inputs. REFP0 and REFN0 or REFP1 and REFN1 can be selected as the ADC reference. REFP1 and REFN1 are shared inputs with analog pins AIN6 and AIN7 in the ADS114S08B.

Without buffering, the reference input impedance is approximately 250 k $\Omega$ . The reference input current can lead to possible errors from either high reference source impedance or through reference input filtering. To reduce the input current, use either internal or external reference buffers. In most applications external reference buffering is not necessary.

Connect a bypass capacitor across the external reference input pins if an external reference is used. Follow the specified absolute and differential reference voltage requirements.

### 9.3.3.3 Reference Buffers

The device has two individually selectable reference input buffers to lower the reference input current. Use the REFP\_BUF and REFN\_BUF bits in the reference control register (05h) to enable or disable the positive and negative reference buffers respectively. These bits are active low. Writing a 1 to REFP\_BUF or REFN\_BUF disables the reference buffers.

The reference buffers are recommended to be disabled when the internal reference is selected for measurements. The positive reference buffer is recommended to be disabled when REFPx is at AVDD and the negative reference buffer is recommended to be disabled when REFNx is at AVSS.

### 9.3.4 Clock Source

The ADS114S0xB system clock is either provided by the internal low-drift 4.096-MHz oscillator or an external clock source on the CLK input. Use the CLK bit within the data rate register (04h) to select the internal 4.096-MHz oscillator or an external clock source.

The device defaults to using the internal oscillator. If the device is reset (from either the  $\overline{\text{RESET}}$  pin, or the RESET command), then the clock source returns to using the internal oscillator.

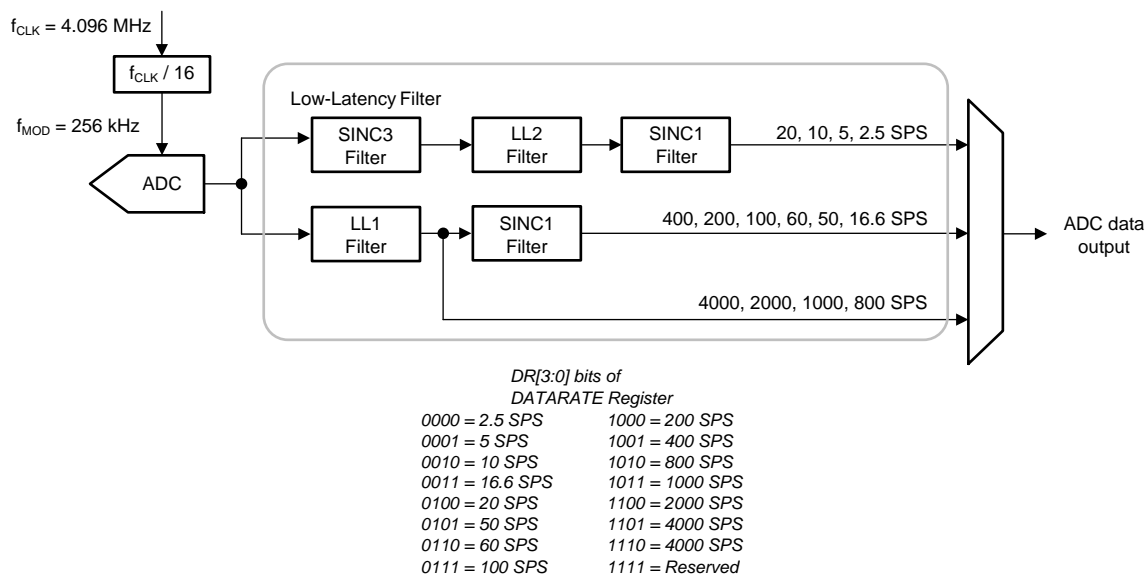
### 9.3.5 Delta-Sigma Modulator

A delta-sigma ( $\Delta\Sigma$ ) modulator is used in the devices to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of  $f_{\text{MOD}} = f_{\text{CLK}} / 16$ , where  $f_{\text{CLK}}$  is either provided by the internal 4.096-MHz oscillator or the external clock source.

### 9.3.6 Digital Filter

The devices offer digital filter options for decimation of the digital data stream coming from the delta-sigma modulator. The implementation of the digital filter is determined by the data rate setting. Figure 46 shows the digital filter implementation.

The low-latency digital filter is a finite impulse response (FIR) filter that provides settled data, given that the analog input signal has settled to the final value before the conversion is started. This digital filter implementation is especially useful when multiple channels must be scanned in minimal time.



NOTE: LL filter = low-latency filter.

Figure 46. Digital Filter Architecture

The device requires a set number of modulator clocks to output a single ADC conversion data. This number is known as the oversampling ratio (OSR). The OSR of the digital filter is set using the DR[3:0] bits in the data rate register. The data rate is determined by [Equation 8](#).

$$\text{Data Rate} = f_{\text{MOD}} / \text{OSR} \quad (8)$$

The relationship between the data rate and oversampling ratio is shown in [Table 5](#).

**Table 5. ADC Data Rates and Digital Filter Oversampling Ratios**

| NOMINAL DATA RATE (SPS) <sup>(1)</sup> | DATA RATE REGISTER DR[3:0] | OVERSAMPLING RATIO <sup>(2)</sup> |
|--|----------------------------|-----------------------------------|
| 2.5                                    | 0000                       | 102400                            |
| 5                                      | 0001                       | 51200                             |
| 10                                     | 0010                       | 25600                             |
| 16.6                                   | 0011                       | 15360                             |
| 20                                     | 0100                       | 12800                             |
| 50                                     | 0101                       | 5120                              |
| 60                                     | 0110                       | 4264                              |
| 100                                    | 0111                       | 2560                              |
| 200                                    | 1000                       | 1280                              |
| 400                                    | 1001                       | 640                               |
| 800                                    | 1010                       | 320                               |
| 1000                                   | 1011                       | 256                               |
| 2000                                   | 1100                       | 128                               |
| 4000                                   | 1101                       | 64                                |

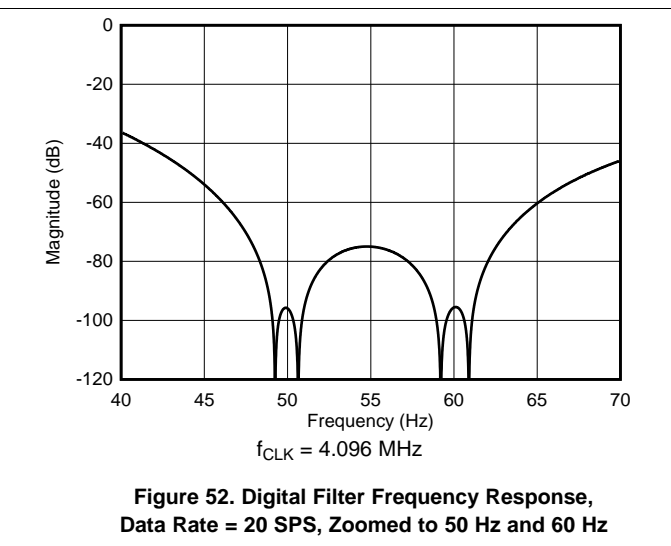
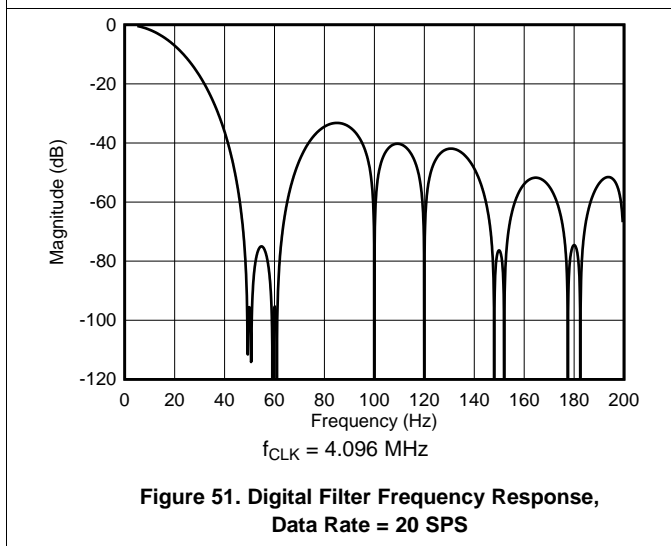
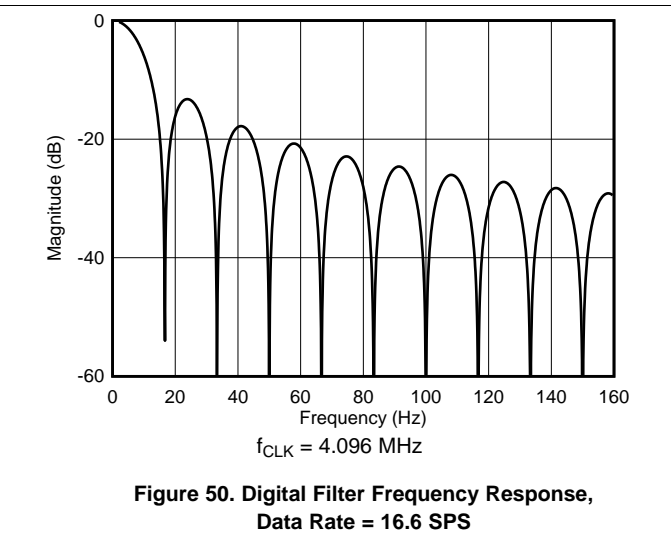
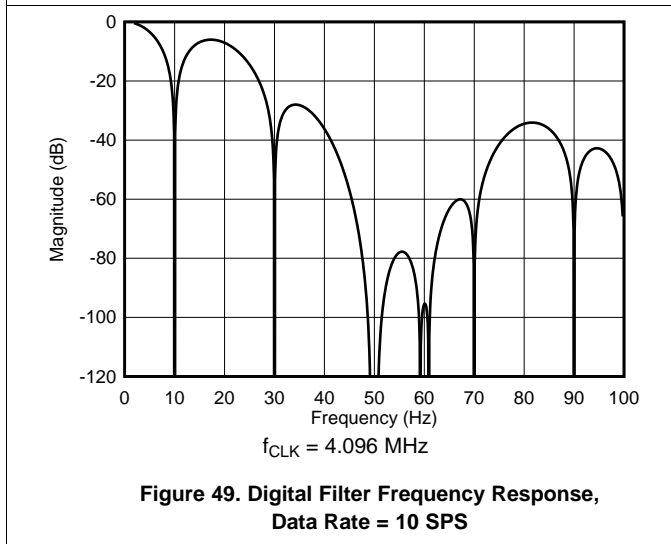
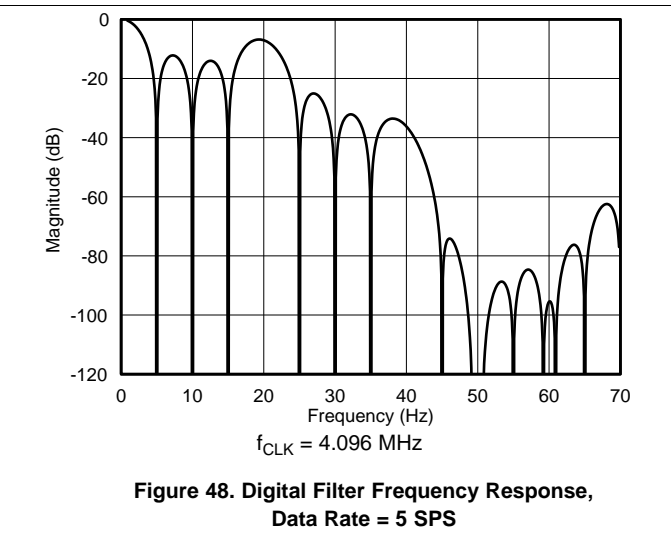
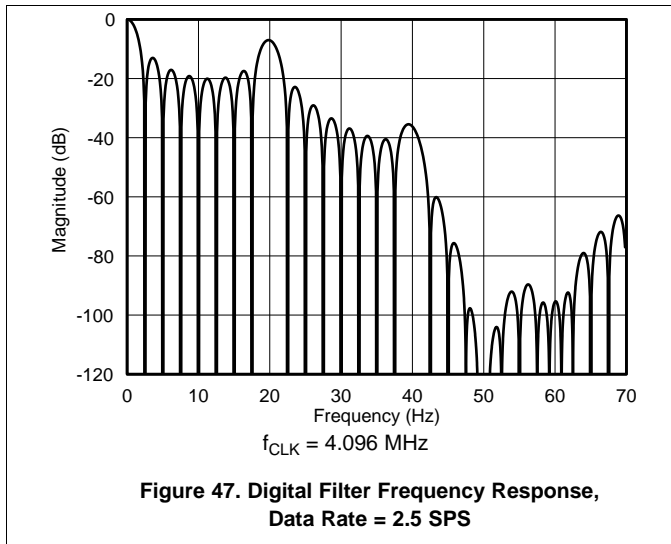
- (1) Valid for the internal oscillator or an external 4.096-MHz clock. The data rate scales with internal oscillator or external clock frequency.
- (2) The oversampling ratio is  $f_{\text{MOD}}$  divided by the data rate;  $f_{\text{MOD}} = f_{\text{CLK}} / 16$ .

### 9.3.6.1 Digital Filter Frequency Response

The digital filter provides many data rate options for rejecting 50-Hz and 60-Hz line cycle noise. At data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS, the filter rejects both 50-Hz and 60-Hz line frequencies. At data rates of 16.6 SPS and 50 SPS, the filter has a notch at 50 Hz. At a 60-SPS data rate, the filter has a notch at 60 Hz.

For detailed frequency response plots showing line cycle noise rejection, download the [ADS1x4S0x design calculator](#) from [www.ti.com](http://www.ti.com).

Figure 47 to Figure 61 illustrate the frequency response of the digital filter for different data rates. Table 6 lists the bandwidth of the digital filter for each data rate.



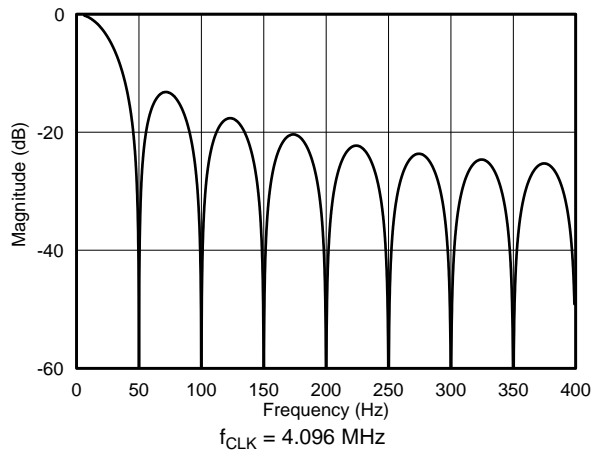


Figure 53. Digital Filter Frequency Response, Data Rate = 50 SPS

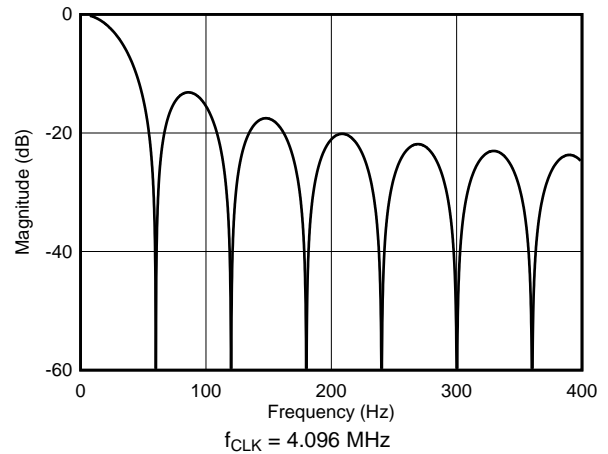


Figure 54. Digital Filter Frequency Response, Data Rate = 60 SPS

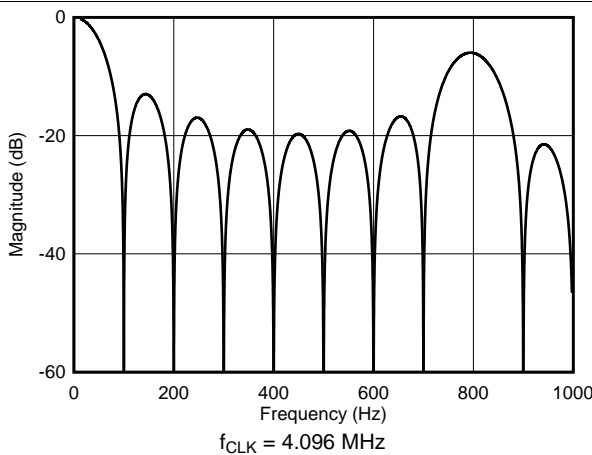


Figure 55. Digital Filter Frequency Response, Data Rate = 100 SPS

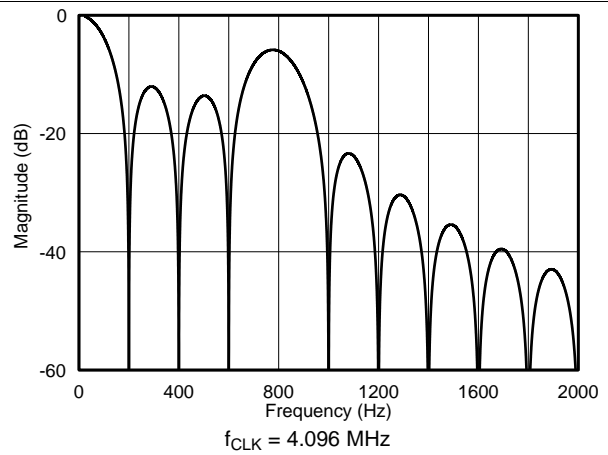


Figure 56. Digital Filter Frequency Response, Data Rate = 200 SPS

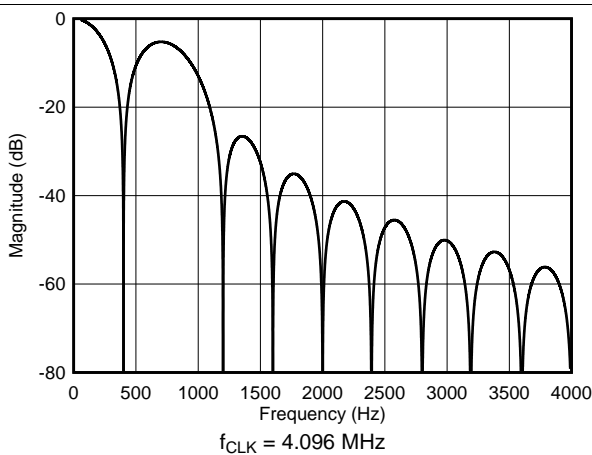


Figure 57. Digital Filter Frequency Response, Data Rate = 400 SPS

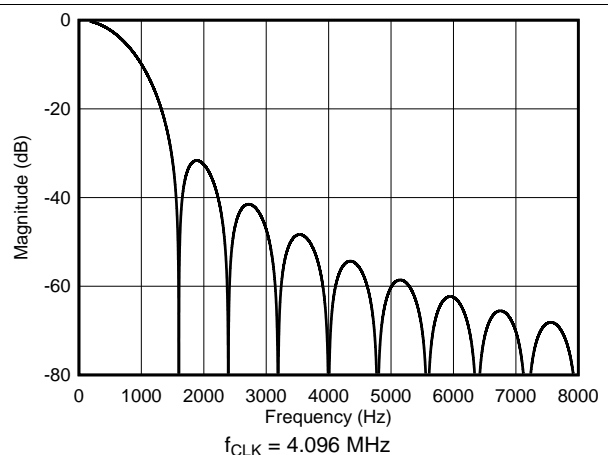


Figure 58. Digital Filter Frequency Response, Data Rate = 800 SPS



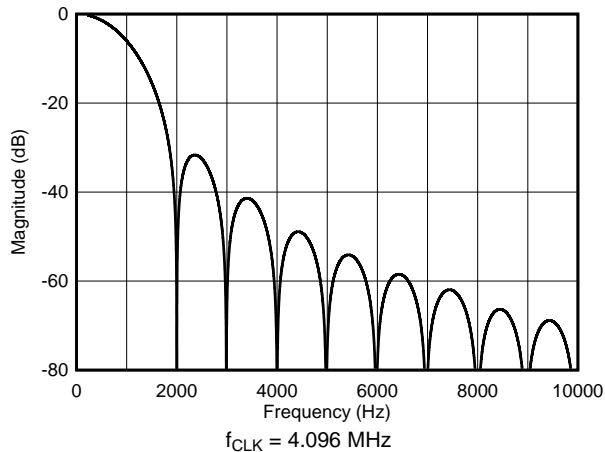


Figure 59. Digital Filter Frequency Response, Data Rate = 1 kSPS

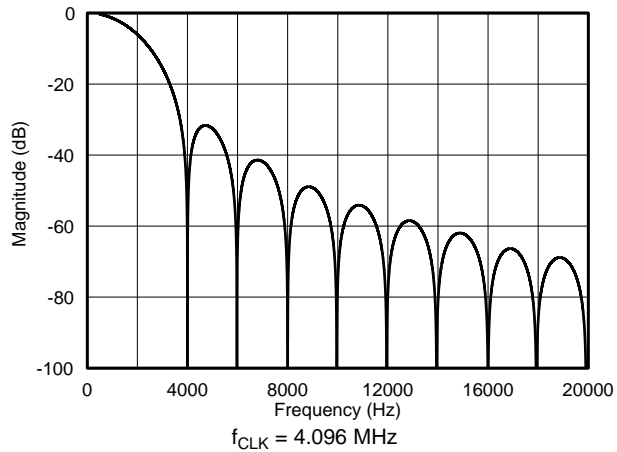


Figure 60. Digital Filter Frequency Response, Data Rate = 2 kSPS

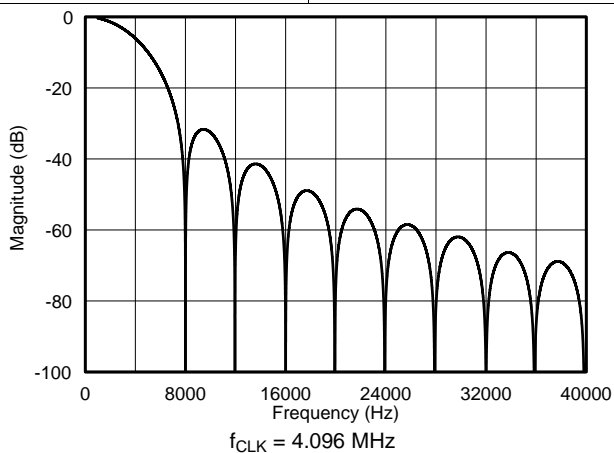


Figure 61. Digital Filter Frequency Response, Data Rate = 4 kSPS

Table 6. Digital Filter Bandwidth

| NOMINAL DATA RATE (SPS) <sup>(1)</sup> | -3-dB BANDWIDTH (Hz) <sup>(1)</sup> |
|--|-------------------------------------|
| 2.5                                    | 1.1                                 |
| 5                                      | 2.2                                 |
| 10                                     | 4.7                                 |
| 16.6                                   | 7.4                                 |
| 20                                     | 13.2                                |
| 50                                     | 22.1                                |
| 60                                     | 26.6                                |
| 100                                    | 44.4                                |
| 200                                    | 89.9                                |
| 400                                    | 190                                 |
| 800                                    | 574                                 |
| 1000                                   | 717                                 |
| 2000                                   | 1434                                |
| 4000                                   | 2868                                |

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with  $f_{CLK}$ .

The digital filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. The internal oscillator can vary over temperature as specified in the [Electrical Characteristics](#) table. The data rate, conversion time, and filter notches consequently vary by the same percentage. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.

### 9.3.6.2 Data Conversion Time

The amount of time required to receive data from the ADC depends on more than just the nominal data rate of the device. The data period also depends on the mode of operation and other configurations of the device. In normal operation, the data settles in one data period. However, a small amount of latency exists to set up the device, calculate the conversion data from the modulator samples, and other overhead that adds time to the conversion. For this reason, the first conversion data takes longer than subsequent data conversions.

Table 7 shows the conversion times for the digital filter for each ADC data rate and various conversion modes.

**Table 7. Data Conversion Time**

| NOMINAL DATA RATE <sup>(1)</sup><br>(SPS) | FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE <sup>(2)</sup> |                             | SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE |                             |
|---|---|-----------------------------|--|-----------------------------|
|   | ms  | NUMBER OF $t_{MOD}$ PERIODS | ms   | NUMBER OF $t_{MOD}$ PERIODS |
| 2.5                                       | 406.559   | 104079                      | 400  | 102400                      |
| 5   | 206.559   | 52879                       | 200  | 51200                       |
| 10  | 106.559   | 27279                       | 100  | 25600                       |
| 16.6                                      | 60.309  | 15439                       | 60   | 15360                       |
| 20  | 56.559  | 14479                       | 50   | 12800                       |
| 50  | 20.211  | 5174                        | 20   | 5120                        |
| 60  | 16.965  | 4343                        | 16.66  | 4264                        |
| 100                                       | 10.211  | 2614                        | 10   | 2560                        |
| 200                                       | 5.211   | 1334                        | 5  | 1280                        |
| 400                                       | 2.711   | 694                         | 2.5  | 640                         |
| 800                                       | 1.461   | 374                         | 1.25   | 320                         |
| 1000                                      | 1.211   | 310                         | 1  | 256                         |
| 2000                                      | 0.711   | 182                         | 0.5  | 128                         |
| 4000                                      | 0.461   | 118                         | 0.25   | 64                          |

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with  $f_{CLK}$ .

(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.

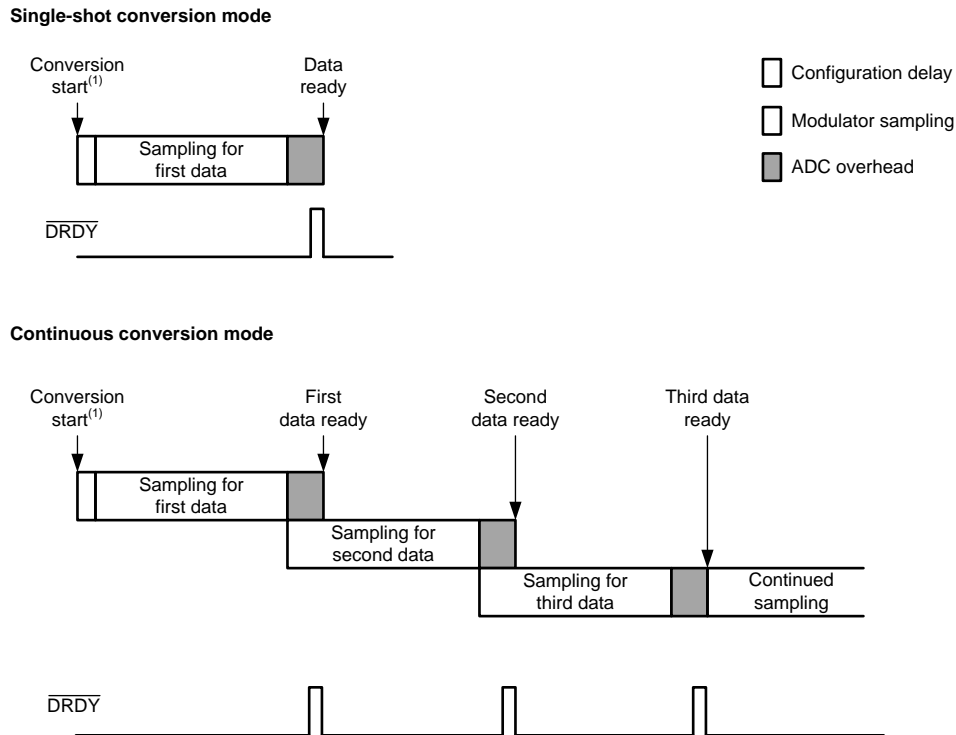
### 9.3.6.3 Note on Conversion Time

Each data period consists of time required for the modulator to sample the analog inputs. However, there is additional time required before the samples become an ADC conversion result.

When a new conversion is started, there is a configuration delay time of  $14 \cdot t_{MOD}$  (where  $t_{MOD} = 16 \cdot t_{CLK}$ ) that is added before the conversion starts. This delay allows for additional settling time for external RC filters on the analog inputs and for the antialiasing filter after the PGA. The configuration delay occurs at the start of a new conversion after a START command is sent, the START/SYNC pin is taken high, or a WREG command is sent to change any configuration register from address 03h to 07h (as described in the [WREG](#) section).

Also, overhead time is needed to convert the modulator samples into an ADC conversion result. This overhead time includes any necessary offset or gain compensation after the digital filter accumulates a data result. The first conversion when the device is in continuous conversion mode (just as in single-shot conversion mode) includes the configuration delay, the modulator sampling time, and the overhead time. The second and subsequent conversions are the normal data period (period as given by the inverse of the data rate).

Figure 62 shows the time sequence for the ADC in both continuous conversion and single-shot conversion modes.



- (1) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.

**Figure 62. Single-Shot Conversion Mode and Continuous Conversion Mode Sequences**

### 9.3.6.4 50-Hz and 60-Hz Line Cycle Rejection

If the ADC connection leads are in close proximity to industrial motors and conductors, coupling of 50-Hz and 60-Hz power line frequencies can occur. The coupled noise interferes with the signal voltage, and can lead to inaccurate or unstable conversions. The digital filter provides enhanced rejection of power-line-coupled noise for data rates of 60 SPS and less. Program the filter to tradeoff data rate and conversion latency versus the desired level of line cycle rejection. Table 8 summarizes the ADC 50-Hz and 60-Hz line-cycle rejection based on  $\pm 1$ -Hz and  $\pm 2$ -Hz tolerance of power-line frequency. The best possible power-line rejection is provided by using an accurate ADC clock.

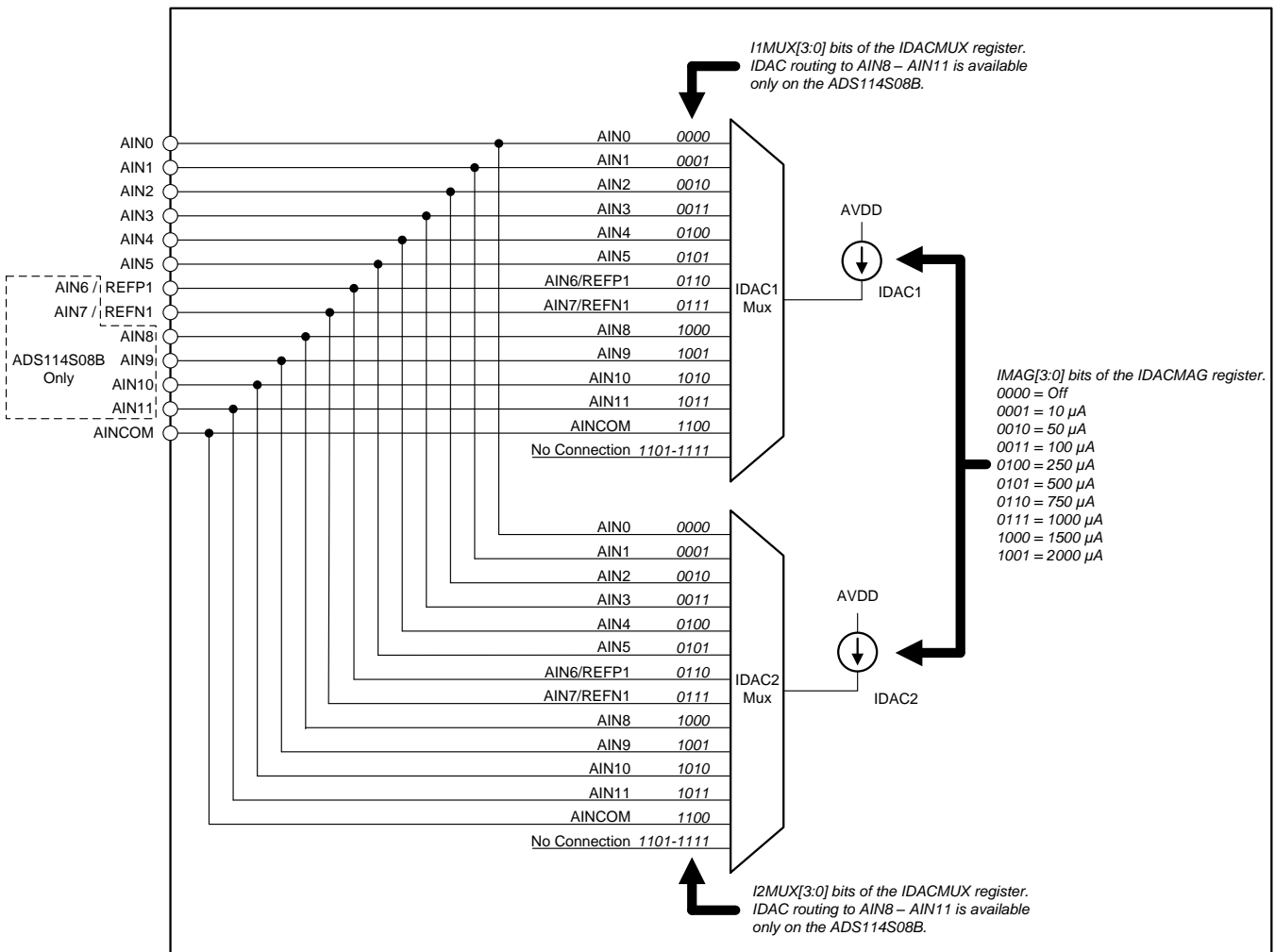
**Table 8. 50-Hz and 60-Hz Line Cycle Rejection**

| DATA RATE (SPS) <sup>(1)</sup> | DIGITAL FILTER LINE CYCLE REJECTION (dB) |                  |                  |                  |
|--------------------------------|--|------------------|------------------|------------------|
|                                | 50 Hz $\pm$ 1 Hz                         | 60 Hz $\pm$ 1 Hz | 50 Hz $\pm$ 2 Hz | 60 Hz $\pm$ 2 Hz |
| 2.5                            | -113.7                                   | -95.4            | -97.7            | -92.4            |
| 5                              | -111.9                                   | -95.4            | -87.6            | -81.8            |
| 10                             | -111.5                                   | -95.4            | -85.7            | -81.0            |
| 16.6                           | -33.8                                    | -20.9            | -27.8            | -20.8            |
| 20                             | -95.4                                    | -95.4            | -75.5            | -80.5            |
| 50                             | -33.8                                    | -15.5            | -27.6            | -15.1            |
| 60                             | -13.4                                    | -35.0            | -12.6            | -29.0            |

- (1)  $f_{CLK} = 4.096$  MHz.

### 9.3.7 Excitation Current Sources (IDACs)

The ADS114S0xB incorporates two integrated, matched current sources (IDAC1, IDAC2). The current sources provide excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing. The current sources are programmable to output values between 10  $\mu\text{A}$  to 2000  $\mu\text{A}$  using the IMAG[3:0] bits in the excitation current register 1 (06h). Each current source can be connected to any of the analog inputs AINx as well as the REFP1 and REFN1 inputs for the ADS114S06B. Both current sources can also be connected to the same pin. The routing of the IDACs is configured by the I1MUX[3:0] and I2MUX[3:0] bits in the excitation current register 2 (07h). In three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the [Typical Application](#) section for more details). [Figure 63](#) details the IDAC connection through the input multiplexer.



Copyright © 2017, Texas Instruments Incorporated

**Figure 63. IDAC Block Diagram**

The internal reference must be enabled for IDAC operation. As any current source, the IDAC requires voltage headroom to the positive supply to operate. This voltage headroom is the compliance voltage. When driving resistive sensors and biasing resistors, take care not to exceed the compliance voltage of the IDACs, otherwise the specified accuracy of the IDAC current may not be met. For IDAC compliance voltage specifications, see the [Electrical Characteristics](#) table.

### 9.3.8 Bias Voltage Generation

The ADS114S0xB provides an internal bias voltage generator, VBIAS, that is set to  $(AVDD + AVSS) / 2$ . The bias voltage is internally buffered and can be established on the analog inputs AIN0 to AIN5 and AINCOM using the VB\_AINx bits in the sensor biasing register (08h). A typical use case for VBIAS is biasing unbiased thermocouples to within the common-mode voltage range of the PGA. A block diagram of the VBIAS voltage generator and connection diagram is shown in Figure 64.

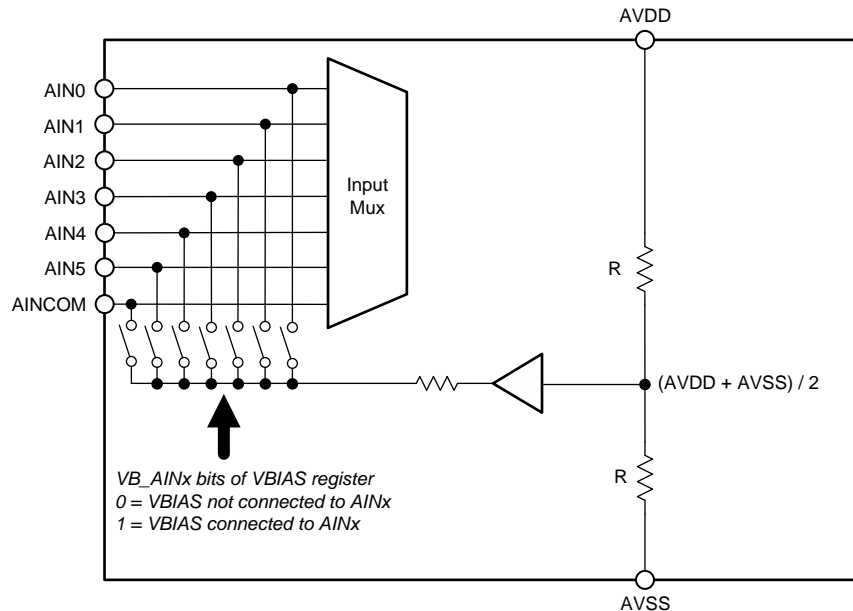


Figure 64. VBIAS Block Diagram

The start-up time of the VBIAS voltage depends on the pin load capacitance. The total capacitance includes any capacitance connected from VBIAS to AVDD, AVSS, and ground. Table 9 lists the VBIAS voltage settling times for various external load capacitances. Ensure the VBIAS voltage is fully settled before starting a conversion.

Table 9. VBIAS Settling Time

| LOAD CAPACITANCE | SETTLING TIME |
|------------------|---------------|
| 0.1 $\mu$ F      | 280 $\mu$ s   |
| 1 $\mu$ F        | 2.8 ms        |
| 10 $\mu$ F       | 28 ms         |

### 9.3.9 System Monitor

The ADS114S0xB provides a set of system monitor functions. These functions measure the device temperature, analog power supply, digital power supply, or use current sources to detect sensor malfunction. System monitor functions are enabled through the SYS\_MON[2:0] bits of the system control register (09h).

#### 9.3.9.1 Internal Temperature Sensor

On-chip diodes provide temperature-sensing capability. Enable the internal temperature sensor by setting SYS\_MON[2:0] = 010 in the system control register (09h). The temperature sensor outputs a voltage proportional to the device temperature as specified in the [Electrical Characteristics](#) table.

When measuring the internal temperature sensor, the analog inputs are disconnected from the ADC and the output voltage of the temperature sensor is routed to the ADC for measurement using the selected PGA gain, data rate, and voltage reference. If enabled, PGA gain must be limited to 4 for the temperature sensor measurement to remain within the allowed absolute input voltage range of the PGA. As a result of the low device junction-to-PCB thermal resistance ( $R_{\theta JB}$ ), the internal device temperature closely tracks the printed circuit board (PCB) temperature.

#### 9.3.9.2 Power Supply Monitors

The ADS114S0xB provides a means for monitoring both the analog and digital power supply (AVDD and DVDD). The power-supply voltages are divided by a resistor network to reduce the voltages to within the ADC input range. The reduced power-supply voltage is routed to the ADC input multiplexer. The analog ( $V_{ANL\text{MON}}$ ) and digital ( $V_{DIG\text{MON}}$ ) power-supply readings are scaled by [Equation 9](#) and [Equation 10](#), respectively:

$$V_{ANL\text{MON}} = (AVDD - AVSS) / 4 \quad (9)$$

$$V_{DIG\text{MON}} = (DVDD - DGND) / 4 \quad (10)$$

Enable the supply voltage monitors using the SYS\_MON[2:0] bits in the system control register (09h). Setting SYS\_MON[2:0] to 011 measures  $V_{ANL\text{MON}}$ , and setting SYS\_MON[2:0] to 100 measures  $V_{DIG\text{MON}}$ .

When the supply voltage monitor is enabled, the analog inputs are disconnected from the ADC and the PGA gain is set to 1, regardless of the GAIN[2:0] bit values in the gain setting register (03h). Supply voltage monitor measurements can be done with either the PGA enabled or PGA disabled via the PGA\_EN[1:0] register. To obtain valid power-supply monitor readings, the reference voltage must be larger than the power-supply measurements shown in [Equation 9](#) and [Equation 10](#).

#### 9.3.9.3 Burn-Out Current Sources

To help detect a possible sensor malfunction, the ADS114S0xB provides selectable current sources to function as burn-out current sources (BOCS) using the SYS\_MON[2:0] bits in the system control register (09h). Current sources are set to values of 0.2  $\mu\text{A}$ , 1  $\mu\text{A}$ , and 10  $\mu\text{A}$  with SYS\_MON[2:0] settings of 101, 110, and 111, respectively.

When enabled, one BOCS sources current to the selected positive analog input ( $\text{AIN}_P$ ) and the other BOCS sinks current from the selected negative analog input ( $\text{AIN}_N$ ). With an open-circuit in a burned out sensor, these BOCSs pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading can indicate a shorted sensor. Distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. The voltage drop across the external filter resistance and the residual resistance of the multiplexer can cause the output to read a value higher than zero.

The ADC readings of a functional sensor can be corrupted when the burn-out current sources are enabled. The burn-out current sources are recommended to be disabled when performing the precision measurement, and are recommended to be enabled only when testing for sensor fault conditions. If the global chop mode is enabled, disable this mode before making a measurement with the burn-out current sources.

### 9.3.10 Status Register

The ADS114S0xB has a one-byte status register (01h) that contains a POR flag to indicate if a start-up or power-on reset condition has occurred and a RDY flag to indicate when a device has started up and is ready for communication.

The status register data field and field description are found in [Figure 77](#) and [Table 17](#).

#### 9.3.10.1 POR Flag

After the power supplies are turned on, the ADC remains in reset until DVDD, IOVDD, and the analog power supply (AVDD – AVSS) voltage exceed the respective power-on reset (POR) voltage thresholds. If a POR event has occurred, the FL\_POR flag (bit 7 of the status register) is set. This flag indicates that a POR event has occurred and has not been cleared. This flag is cleared with a user register write to set the bit to 0. The power-on reset is described further in the [Power-On Reset](#) section.

#### 9.3.10.2 $\overline{\text{RDY}}$ Flag

The  $\overline{\text{RDY}}$  flag indicates that the device has started up and is ready to receive a configuration change. During a reset or POR event, the device is resetting the register map and may not be available. The RDY flag is shown with bit 6 of the status register.

### 9.3.11 General-Purpose Inputs and Outputs (GPIOs)

The ADS114S06B offers four dedicated general-purpose input and output (GPIO) pins, and the ADS114S08B offers four pins (AIN8 to AIN11) that serve a dual purpose as either analog inputs or GPIOs.

Two registers control the function of the GPIO pins. Use the CON[3:0] bits of the GPIO configuration register (11h) to configure a pin as a GPIO pin. The upper four bits (DIR[3:0]) of the GPIO data register (10h) configure the GPIO pin as either an input or an output. The lower four bits (DAT[3:0]) of the GPIO data register contain the input or output GPIO data. If a GPIO pin is configured as an input, the respective DAT[x] bit reads the status of the pin; if a GPIO pin is configured as an output, write the output status to the respective DAT[x] bit. For more information about the use of GPIO pins, see the [Configuration Registers](#) section.

[Figure 65](#) depicts a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the devices are operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken to not load the GPIO pins when used as outputs because large currents can cause droop or noise on the analog supplies. GPIO pins use Schmitt triggered inputs with hysteresis to make the input more resistance to noise; see the [Electrical Characteristics](#) table for GPIO thresholds.

For connections of unused GPIO pins, see the [Unused Inputs and Outputs](#) section.

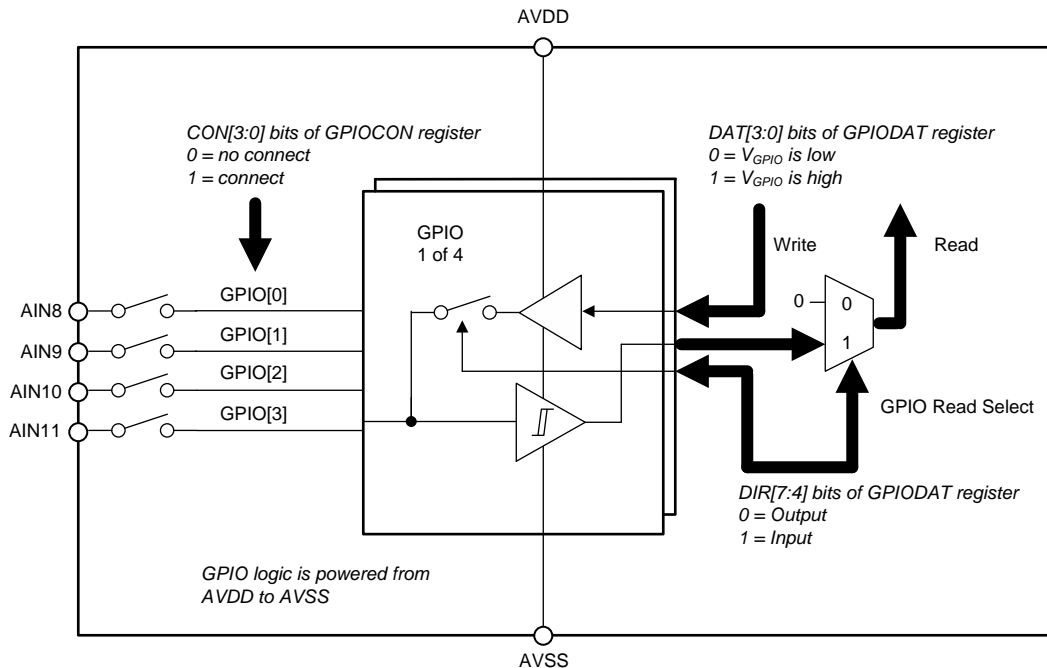


Figure 65. GPIO Block Diagram

9.3.12 Calibration

The ADC incorporates offset and gain calibration commands, as well as user-offset and full-scale (gain) calibration registers to calibrate the ADC. The ADC calibration registers are 16 bits wide. Use calibration to correct internal ADC errors or overall system errors. Calibrate by sending calibration commands to the ADC, or by direct user calibration. In user calibration, the user calculates and writes the correction values to the calibration registers. The ADC performs self or system-offset calibration, or a system gain calibration. Perform offset calibration before system gain calibration. After power-on, wait for the power supplies and reference voltage to fully settle before calibrating.

As shown in Figure 66, the value of the offset calibration register is subtracted from the filter output and then multiplied by the full-scale register value divided by 4000h. The data are then clipped to a 16-bit value to provide the final output.

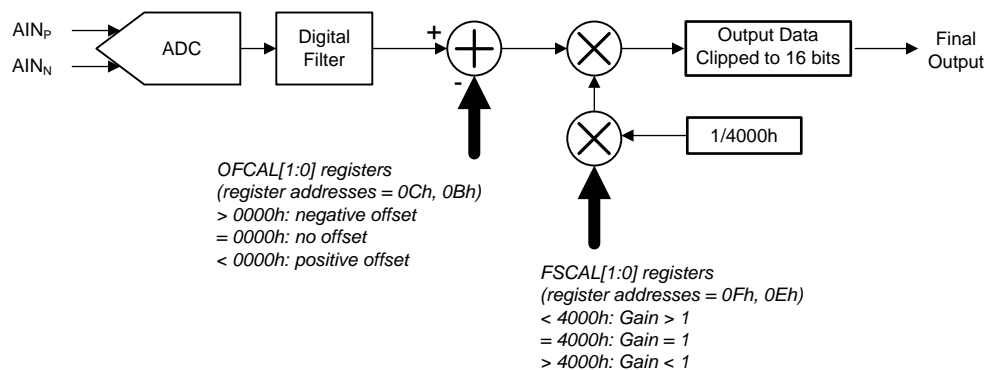


Figure 66. ADC Calibration Block Diagram

Calibration commands cannot be used when the device is in standby mode (when the START/SYNC pin is low, or when the STOP command is issued).



### 9.3.12.1 Offset Calibration

The offset calibration word is 16 bits, consisting of two 8-bit registers, as shown in the two registers starting with [offset calibration register 1](#). The offset value is twos complement format with a maximum positive value equal to 7FFFh, and a maximum negative value equal to 8000h. This value is subtracted from each output reading as an offset correction. A register value equal to 0000h has no offset correction. If global chop mode is enabled, the offset calibration register is disabled. [Table 10](#) shows example settings of the offset register.

**Table 10. Offset Calibration Register Values**

| OFC REGISTER VALUE | OFFSET CALIBRATED OUTPUT CODE <sup>(1)</sup> |
|--------------------|--|
| 0001h              | FFFFh  |
| 0000h              | 0000h  |
| FFFFh              | 0001h  |

(1) Ideal output code with shorted input, excluding ADC noise and offset voltage error.

The user can select how many samples (1, 4, 8, or 16) to average for self or system offset calibration using the CAL\_SAMP[1:0] bits in the system control register (09h). Fewer readings shorten the calibration time but also provide less accuracy. Averaging more readings takes longer but yields a more accurate calibration result by reducing the noise level.

Two commands can be used to perform offset calibration. SFOCAL is a self offset calibration that internally sets the input to mid-scale using the SYS\_MON[2:0] = 001 setting and takes a measurement of the offset. SYOCAL is a system offset calibration where the user must input a null voltage to calibrate the system offset. After either command is issued, the OFC register is updated.

After an offset calibration is performed, the device starts a new conversion and  $\overline{\text{DRDY}}$  falls to indicate a new conversion has completed.

### 9.3.12.2 Gain Calibration

The full-scale (gain) calibration word is 16 bits consisting of two 8-bit registers, as shown in the two registers starting with [gain calibration register 1](#). The gain calibration value is straight binary, normalized to a unity-gain correction factor at a register value equal to 4000h. [Table 11](#) shows register values for selected gain factors. Do not exceed the PGA input range limits during gain calibration.

**Table 11. Gain Calibration Register Values**

| FSC REGISTER VALUE | GAIN FACTOR |
|--------------------|-------------|
| 4333h              | 1.05        |
| 4000h              | 1.00        |
| 3CCCh              | 0.95        |

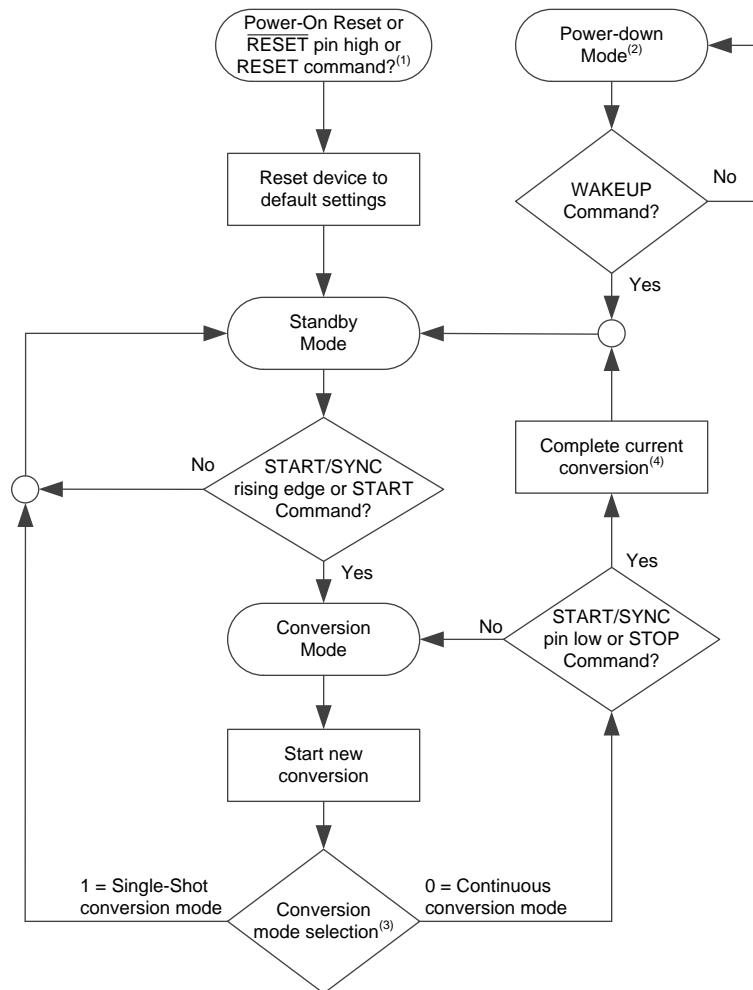
All gains of the ADS114S0xB are factory trimmed to meet the gain error specified in the [Electrical Characteristics](#) table at  $T_A = 25^\circ\text{C}$ . When the gain drift of the devices over temperature is very low, there is typically no need for self gain calibration.

The SYGCAL command initiates a system gain calibration, where the user sets the input to full-scale to remove gain error. After the SYGCAL is issued, the FSC register is updated. As with the offset calibration, the CAL\_SAMP[1:0] bits determine the number of samples used for a gain calibration.

As with an offset calibration, the device starts a new conversion after a gain calibration and  $\overline{\text{DRDY}}$  falls to indicate a new conversion has completed.

## 9.4 Device Functional Modes

The device operates in three different modes: power-down mode, standby mode, and conversion mode. [Figure 67](#) shows a flow chart of the different operating modes and how the device transitions from one mode to another.



- (1) Any reset (power-on, command, or pin), immediately resets the device.
- (2) A POWERDOWN command aborts an ongoing conversion and immediately puts the device into power-down mode.
- (3) The conversion mode is selected with the MODE bit in the data rate register.
- (4) The rising edge of the START/SYNC pin or the START command starts a new conversion without completing the current conversion.

**Figure 67. Operating Flow Chart**

### 9.4.1 Reset

The ADS114S0xB is reset in one of three ways:

- Power-on reset
- RESET pin
- RESET command

When a reset occurs, the configuration registers reset to default values and the device enters standby mode. The device then waits for the rising edge of the START/SYNC pin or a START command to enter conversion mode. If the device had been using an external clock, the reset sets the device to use the internal oscillator as a default configuration. See the [Timing Characteristics](#) section for reset timing information.

## Device Functional Modes (continued)

### 9.4.1.1 Power-On Reset

The ADS114S0xB incorporates a power-on reset circuit that holds the device in reset until all supplies reach approximately 1.65 V. The power-on reset also ensures that the device starts operating in a known state in case a brown-out event occurs, when the supplies have dipped below the minimum operating voltages. When the device completes a POR sequence, the FL\_POR flag in the status register is set high to indicate that a POR has occurred.

Begin communications with the device 2.2 ms after the power supplies reach minimum operating voltages. The only exception is polling the status register for the  $\overline{\text{RDY}}$  bit. If the user polls the  $\overline{\text{RDY}}$  bit, then use an SCLK rate of half the maximum-specified SCLK rate to get a proper reading when the device is making internal configurations. This 2.2-ms POR time is required for the internal oscillator to start up and the device to properly set internal configurations. After the internal configurations are set, the device sets the  $\overline{\text{RDY}}$  bit in the device status register (01h). When this bit is set to 0, user configurations can be programmed into the device. Figure 68 shows the power-on reset timing sequence for the device.

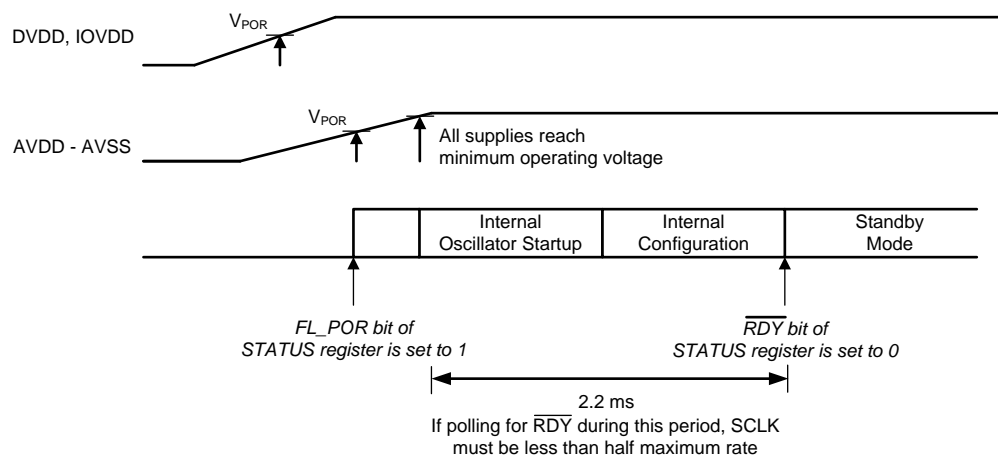


Figure 68. Power-On Reset Timing Sequence

### 9.4.1.2 $\overline{\text{RESET}}$ Pin

Reset the ADC by taking the  $\overline{\text{RESET}}$  pin low for a minimum of  $4 \cdot t_{\text{CLK}}$  cycles, and then returning the pin high. After the rising edge of the  $\overline{\text{RESET}}$  pin, a delay time of  $t_{d(\text{RSSC})}$  is required before sending the first serial interface command or starting a conversion. See the [Timing Characteristics](#) section for reset timing information.

### 9.4.1.3 Reset by Command

Reset the ADC by using the RESET command (06h or 07h). The command is decoded on the seventh SCLK falling edge. After sending the RESET command, a delay time of  $t_{d(\text{RSSC})}$  is required before sending the first serial interface command or starting a conversion. See the [Timing Characteristics](#) section for reset timing information.

## 9.4.2 Power-Down Mode

Power-down mode is entered by sending the POWERDOWN command. In this mode, all analog and digital circuitry is powered down for lowest power consumption regardless of the register settings. Only the internal voltage reference can be configured to stay on during power-down mode in case a faster start-up time is required. All register values retain the current settings during power-down mode. The configuration registers can be read and written in power-down mode. A WAKEUP command must be issued in order to exit power-down mode and to enter standby mode.

When the POWERDOWN command is issued, the device enters power-down mode  $2 \cdot t_{\text{CLK}}$  after the seventh SCLK falling edge of the command. For lowest power consumption (on DVDD and IOVDD), stop the external clock when in power-down mode. TI recommends selecting the internal oscillator before sending the POWERDOWN command to avoid issues with the command decoding.

## Device Functional Modes (continued)

To release the device from POWERDOWN, issue the WAKEUP command to enter standby mode. The device then waits for the rising edge of the START/SYNC pin or a START command to go into conversion mode.

When in power-down mode, the device responds to the RREG, RDATA, and WAKEUP commands. The WREG and RESET commands can also be sent, but are ignored until a WAKEUP command is sent and the internal oscillator resumes operation.

### 9.4.3 Standby Mode

The device powers up in standby mode and automatically enters this mode whenever there is no ongoing conversion. When the STOP command is sent (or the START/SYNC pin is taken low) in continuous conversion mode, or when a conversion completes in single-shot conversion mode, the device enters standby mode.

Standby mode offers several different options and features to lower the power consumption:

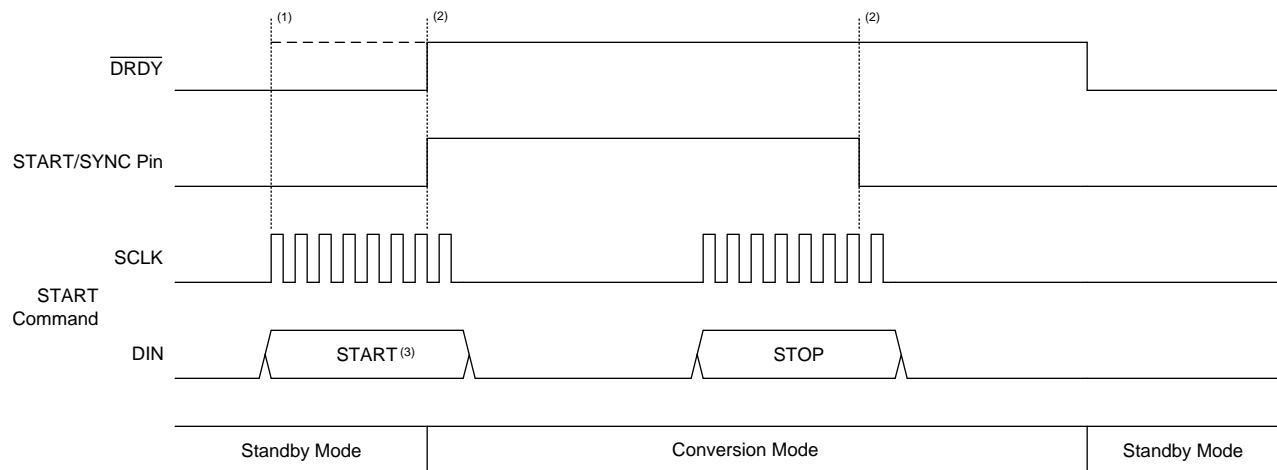
- The PGA can be powered down by setting PGA\_EN[1:0] to 00 in the gain setting register (03h).
- The internal voltage reference can be powered down by setting REFCON[1:0] to 00 in the reference control register (05h). This setting also turns off the IDACs.
- The digital filter is held in reset state.
- The clock to the modulator and digital core is gated to decrease dynamic switching losses.

If powered down in standby mode, the PGA and internal reference can require extra time to power up. Extra delay may be required between power up of the PGA or the internal reference, and the start of conversions. In particular, the reference power up time is dependent on the capacitance between REFOUT and REFCOM.

Calibration commands are not decoded when the device is in standby mode.

### 9.4.4 Conversion Modes

The ADS114S0xB offers two conversion modes: continuous conversion and single-shot conversion mode. Continuous-conversion mode converts indefinitely until stopped by the user. Single-shot conversion mode performs one conversion after the START/SYNC pin is taken high or after the START command is sent. Use the MODE bit in the data rate register (04h) to program the conversion mode. [Figure 69](#) shows how the START/SYNC pin and the START command are used to control ADC conversions.



**Figure 69. Conversion Start and Stop Timing**

- (1)  $\overline{DRDY}$  rises at the first SCLK rising edge or the rising edge of the START/SYNC pin.
- (2) START and STOP commands take effect  $2 \cdot t_{CLK}$  after the seventh SCLK falling edge. The conversion starts  $2 \cdot t_{CLK}$  after the START/SYNC rising edge.
- (3) To synchronize a conversion, the STOP command must be issued prior to the START command. STOP and START commands can be issued without a delay between the commands.

**Figure 69. Conversion Start and Stop Timing**

## Device Functional Modes (continued)

ADC conversions are controlled by the START/SYNC pin or by serial commands. For the device to start converting in continuous conversion or single-shot conversion mode, a START command must be sent or the START/SYNC pin must be taken high. If using commands to control conversions, keep the START/SYNC pin low to avoid possible contentions between the START/SYNC pin and commands.

Conversions can be synchronized to perform a conversion at a particular time. To synchronize the conversion with the START/SYNC pin, take the pin low. The rising edge of the START/SYNC pin starts a new conversion. Similarly, a conversion can be synchronized using the START command. If the device is in standby mode, issue a START command. If the device is in conversion mode, issue a STOP command followed by a START command. The STOP and START commands can be consecutive. A new conversion starts on the seventh SCLK falling edge of the START command.

### 9.4.4.1 Continuous Conversion Mode

The device is configured for continuous conversion mode by setting the MODE bit to 0 in the data rate register (04h). A START command must be sent or the START/SYNC pin must be taken high for the device to start converting continuously. When controlling the device with commands, hold the START/SYNC pin low. Taking the START/SYNC pin low or sending the STOP command stops the device from converting after the currently ongoing conversion completes, indicated by the falling edge of  $\overline{\text{DRDY}}$ . The device enters standby mode thereafter.

For information on the exact timing of continuous conversion mode data, see [Table 7](#).

### 9.4.4.2 Single-Shot Conversion Mode

The device is configured for single-shot conversion mode by setting the MODE bit to 1 in the data rate register (04h). A START command must be sent or the START/SYNC pin must be taken high for the device to start a single conversion. After the conversion completes, the device enters standby mode again. To start a new conversion, the START command must be sent again or the START/SYNC pin must be taken low and then high again.

For information on the exact timing of single-shot conversion mode data, see [Table 7](#).

## 9.5 Programming

### 9.5.1 Serial Interface

The ADC has an SPI-compatible, bidirectional serial interface that is used to read the conversion data as well as to configure and control the ADC. Only SPI mode 1 ( $\overline{\text{CPOL}} = 0$ ,  $\overline{\text{CPHA}} = 1$ ) is supported. The serial interface consists of five control lines:  $\overline{\text{CS}}$ , SCLK, DIN, DOUT/ $\overline{\text{DRDY}}$ , and  $\overline{\text{DRDY}}$  but can be used with only four or even three control signals. If the ADS114S08B or ADS114S06B is the only device connected to the SPI bus, then the  $\overline{\text{CS}}$  input can be tied low so that only SCLK, DIN, and DOUT/ $\overline{\text{DRDY}}$  are required to communicate with the device.

#### 9.5.1.1 Chip Select ( $\overline{\text{CS}}$ )

The  $\overline{\text{CS}}$  pin is an active low input that enables the ADC serial interface for communication and is useful when multiple devices share the same serial bus.  $\overline{\text{CS}}$  must be low during the entire data transaction. When  $\overline{\text{CS}}$  is high, the serial interface is reset, SCLK input activity is ignored (blocking input commands), and the DOUT/ $\overline{\text{DRDY}}$  output enters a high-impedance state. ADC conversions are not affected by the state of  $\overline{\text{CS}}$ . In situations where multiple devices are present on the bus, the dedicated  $\overline{\text{DRDY}}$  pin can provide an uninterrupted monitor of the conversion status and is not affected by  $\overline{\text{CS}}$ . If the serial bus is not shared with another peripheral,  $\overline{\text{CS}}$  can be tied to DGND to permanently enable the ADC interface and DOUT/ $\overline{\text{DRDY}}$  can be used to indicate conversion status. These changes reduce the serial interface from five I/Os to three I/Os.

#### 9.5.1.2 Serial Clock (SCLK)

The serial interface clock is a noise-filtered, Schmidt-triggered input used to clock data into and out of the ADC. Input data to the ADC are latched on the falling SCLK edge and output data from the ADC are updated on the rising SCLK edge. Return SCLK low after the data sequence is complete. Even though the SCLK input has hysteresis, keep SCLK as clean as possible to prevent unintentional SCLK transitions. Avoid ringing and voltage overshoot on the SCLK input. Place a series termination resistor at the SCLK drive pin to help reduce ringing.

#### 9.5.1.3 Serial Data Input (DIN)

The serial data input pin (DIN) is used with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin. During data readback, when no command is intended, keep DIN low.

#### 9.5.1.4 Serial Data Output and Data Ready (DOUT/ $\overline{\text{DRDY}}$ )

The DOUT/ $\overline{\text{DRDY}}$  pin is a dual-function output. The pin functions as the digital data output and the ADC data-ready indication.

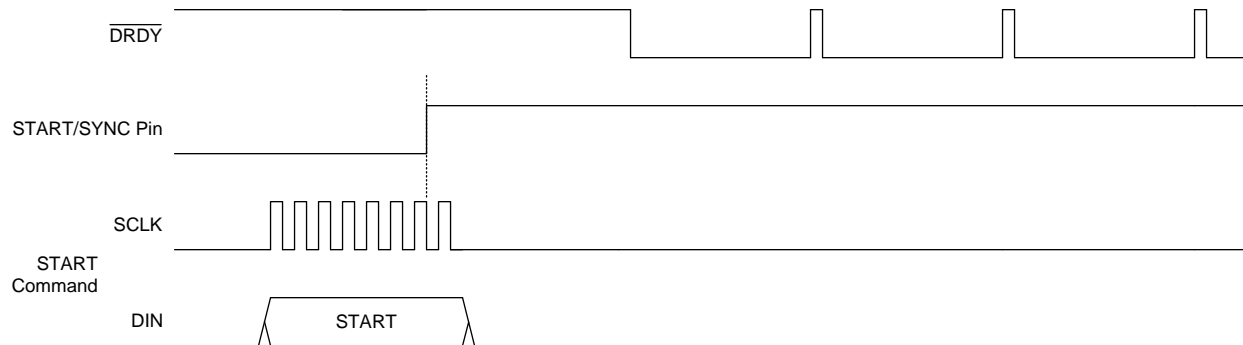
First, this pin is used with SCLK to read conversion and register data from the device. Conversion or register data are shifted out on DOUT/ $\overline{\text{DRDY}}$  on the SCLK rising edge. DOUT/ $\overline{\text{DRDY}}$  goes to a high-impedance state when  $\overline{\text{CS}}$  is high.

Second, the DOUT/ $\overline{\text{DRDY}}$  pin indicates availability of new conversion data. DOUT/ $\overline{\text{DRDY}}$  transitions low at the same time that the  $\overline{\text{DRDY}}$  pin goes low to indicate new conversion data are available. Both signals can be used to detect if new data are ready. However, because DOUT/ $\overline{\text{DRDY}}$  is disabled when  $\overline{\text{CS}}$  is high, use the dedicated  $\overline{\text{DRDY}}$  pin when monitoring conversions on multiple devices on the SPI bus.

## Programming (continued)

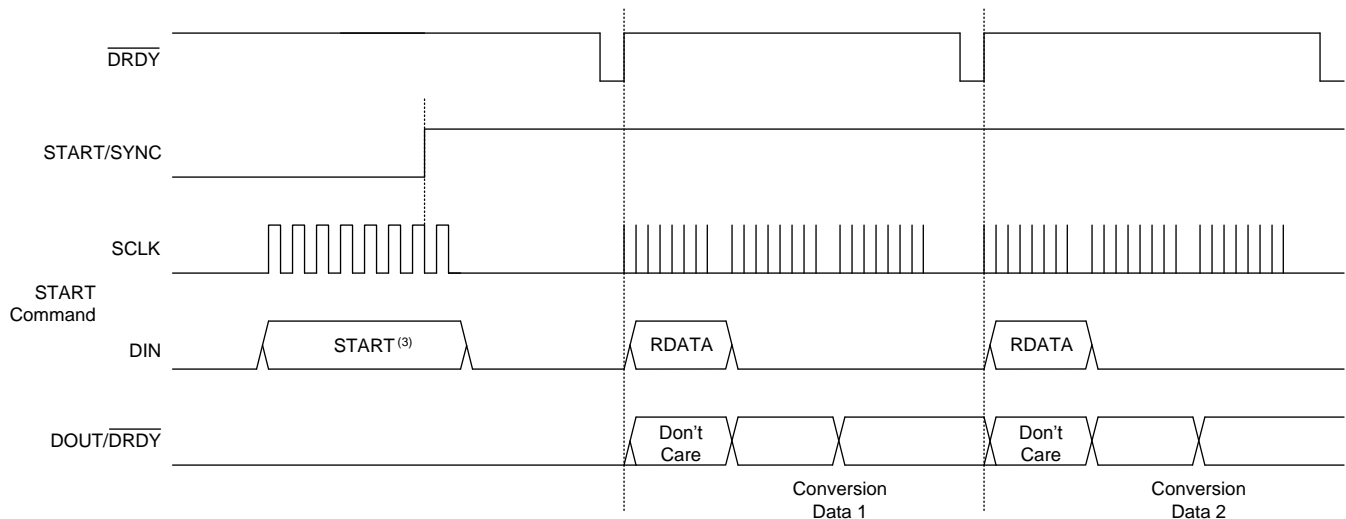
### 9.5.1.5 Data Ready ( $\overline{\text{DRDY}}$ )

The  $\overline{\text{DRDY}}$  pin is an output that transitions low to indicate when conversion data are ready for retrieval. Initially,  $\overline{\text{DRDY}}$  is high at power-on. When converting, the state of  $\overline{\text{DRDY}}$  depends on whether the conversion data are retrieved or not. In continuous conversion mode after  $\overline{\text{DRDY}}$  goes low,  $\overline{\text{DRDY}}$  is driven high on the first SCLK rising edge. If data are not read,  $\overline{\text{DRDY}}$  remains low and then pulses high  $24 \cdot t_{\text{CLK}}$  before the next  $\overline{\text{DRDY}}$  falling edge. The data must be retrieved before the next  $\overline{\text{DRDY}}$  update, otherwise the data are overwritten by new data and any previous data are lost. Figure 70 shows the  $\overline{\text{DRDY}}$  operation without data retrieval. Figure 71 shows the  $\overline{\text{DRDY}}$  operation with data retrieval after each conversion completes.



- (1)  $\overline{\text{DRDY}}$  returns high with the rising edge of the first SCLK after a data ready indication.

Figure 70.  $\overline{\text{DRDY}}$  Operation Without Data Retrieval



- (1)  $\overline{\text{DRDY}}$  returns high with the rising edge of the first SCLK after a data ready indication.

Figure 71.  $\overline{\text{DRDY}}$  Operation With Data Retrieval

### 9.5.1.6 Timeout

The ADS114S0xB offers a serial interface timeout feature that is used to recover communication when a serial interface transmission is interrupted. This feature is especially useful in applications where  $\overline{\text{CS}}$  is permanently tied low and is not used to frame a communication sequence. The SPI interface resets when no valid 8 bits are received within  $2^{15} \cdot t_{\text{CLK}}$ . The timeout feature is enabled by setting the TIMEOUT bit to 1 in the system control register (09h).

## Programming (continued)

### 9.5.2 Data Format

The devices provide 16 bits of data in binary two's complement format. The size of one code (LSB) is calculated using Equation 11.

$$1 \text{ LSB} = (2 \cdot V_{\text{REF}} / \text{Gain}) / 2^{16} = +\text{FS} / 2^{15} \tag{11}$$

A positive full-scale input [ $V_{\text{IN}} \geq (+\text{FS} - 1 \text{ LSB}) = (V_{\text{REF}} / \text{Gain} - 1 \text{ LSB})$ ] produces an output code of 7FFFh and a negative full-scale input ( $V_{\text{IN}} \leq -\text{FS} = -V_{\text{REF}} / \text{Gain}$ ) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

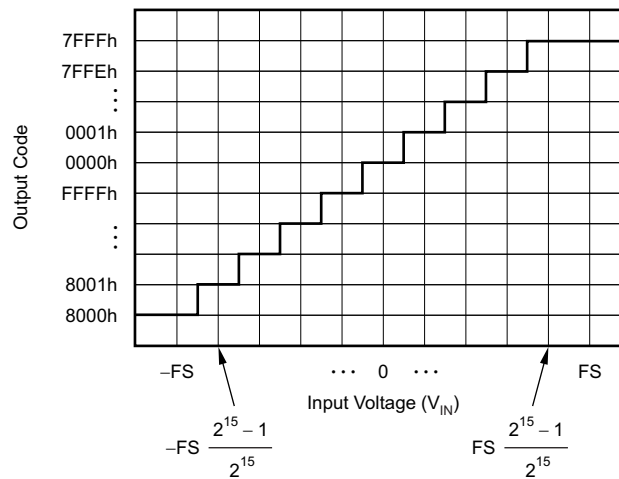
Table 12 summarizes the ideal output codes for different input signals.

**Table 12. Ideal Output Code vs Input Signal**

| INPUT SIGNAL,<br>$V_{\text{IN}} = V_{\text{AINP}} - V_{\text{AINN}}$ | IDEAL OUTPUT CODE <sup>(1)</sup> |
|--|----------------------------------|
| $\geq \text{FS} (2^{15} - 1) / 2^{15}$                               | 7FFFh                            |
| $\text{FS} / 2^{15}$   | 0001h                            |
| 0  | 0000h                            |
| $-\text{FS} / 2^{15}$  | FFFFh                            |
| $\leq -\text{FS}$  | 8000h                            |

(1) Excludes the effects of noise, INL, offset, and gain errors.

Mapping of the analog input signal to the output codes is shown in Figure 72.



**Figure 72. Code Transition Diagram**



### 9.5.3 Commands

Commands are used to control the ADC, access the configuration registers, and retrieve data. Many of the commands are stand-alone (that is, single-byte). The register write and register read commands, however, are multibyte, consisting of two command bytes plus the register data byte or bytes. The commands are listed in [Table 13](#).

**Table 13. Command Definitions**

| COMMAND                                 | DESCRIPTION  | FIRST<br>COMMAND BYTE                | SECOND<br>COMMAND BYTE          |
|---|--|--------------------------------------|---------------------------------|
| <b>Control Commands</b>                 |  |                                      |                                 |
| NOP                                     | No operation   | 0000 0000 (00h)                      | —                               |
| WAKEUP                                  | Wake-up from power-down mode                                 | 0000 001x (02h, 03h) <sup>(1)</sup>  | —                               |
| POWERDOWN                               | Enter power-down mode  | 0000 010x (04h, 05h) <sup>(1)</sup>  | —                               |
| RESET                                   | Reset the device   | 0000 011x (06h, 07h) <sup>(1)</sup>  | —                               |
| START                                   | Start conversions  | 0000 100x (08h, 09h) <sup>(1)</sup>  | —                               |
| STOP                                    | Stop conversions   | 0000 101x (0Ah, 0Bh) <sup>(1)</sup>  | —                               |
| <b>Calibration Commands</b>             |  |                                      |                                 |
| SYOCAL                                  | System offset calibration                                    | 0001 0110 (16h)                      | —                               |
| SYGCAL                                  | System gain calibration                                      | 0001 0111 (17h)                      | —                               |
| SFOCAL                                  | Self offset calibration                                      | 0001 1001 (19h)                      | —                               |
| <b>Data Read Command</b>                |  |                                      |                                 |
| RDATA                                   | Read data  | 0001 001x (12h / 13h) <sup>(1)</sup> | —                               |
| <b>Register Read and Write Commands</b> |  |                                      |                                 |
| RREG                                    | Read <i>nnnnn</i> registers starting at address <i>rrrr</i>  | 001r <i>rrrr</i> <sup>(2)</sup>      | 000n <i>nnnn</i> <sup>(3)</sup> |
| WREG                                    | Write <i>nnnnn</i> registers starting at address <i>rrrr</i> | 010r <i>rrrr</i> <sup>(2)</sup>      | 000n <i>nnnn</i> <sup>(3)</sup> |

(1) x = don't care.

(2) r *rrrr* = starting register address.

(3) n *nnnn* = number of registers to read or write – 1.

Commands can be sent at any time, either during a conversion or when conversions are stopped. However, if register read or write commands are in progress when conversion data are ready, the ADC blocks loading of conversion data to the output shift register. The  $\overline{CS}$  input pin can be taken high between commands; or held low between consecutive commands.  $\overline{CS}$  must stay low for the entire command sequence. Complete the command, or terminate the command before completion by taking  $\overline{CS}$  high. Only send the commands that are listed in [Table 13](#).

#### 9.5.3.1 NOP

NOP is a no-operation command. The NOP command is used to clock out data without clocking in a command.

#### 9.5.3.2 WAKEUP

Issue the WAKEUP command to exit power-down mode and to place the device into standby mode.

When running off the external clock, the external clock must be running before sending the WAKEUP command, otherwise the command is not decoded.

### 9.5.3.3 POWERDOWN

Sending the POWERDOWN command aborts a currently ongoing conversion and puts the device into power-down mode. The device goes into power-down mode  $2 \cdot t_{CLK}$  after the seventh SCLK falling edge of the command.

For lowest power consumption on DVDD and IOVDD, stop the external clock when in power-down mode. The device does not gate the external clock. When running off the external clock, provide at a minimum two additional  $t_{CLK}$ s after the POWERDOWN command is issued, otherwise the device does not enter power-down mode. Alternatively, select the internal oscillator before sending the POWERDOWN command to avoid any issues with decoding of the POWERDOWN and WAKEUP commands.

During power-down mode, the only commands that are available are RREG, RDATA, and WAKEUP.

### 9.5.3.4 RESET

The RESET command resets the digital filter and sets all configuration register values to default settings. A RESET command also puts the device into standby mode. When in standby mode, the device waits for a rising edge on the START/SYNC pin or a START command to resume conversions. After sending the RESET command, a delay time of  $t_{d(RSSC)}$  is required before sending the first serial interface command or starting a conversion. See the [Timing Characteristics](#) section for reset timing information.

If the device had been using an external clock, the reset sets the device to use the internal oscillator as a default configuration.

### 9.5.3.5 START

When the device is configured for continuous conversion mode, issue the START command for the device to start converting. Every time a conversion completes, the device automatically starts a new conversion until the STOP command is sent.

In single-shot conversion mode, the START command is used to start a single conversion. After the conversion completes, the device enters standby mode.

Tie the START/SYNC pin low when the device is controlled through the START and STOP commands. The START command is not decoded if the START/SYNC pin is high. If the device is already in conversion mode, the START command has no effect.

### 9.5.3.6 STOP

The STOP command is used in continuous conversion mode to stop the device from converting. The current conversion is allowed to complete. After DRDY transitions low, the device enters standby mode. The STOP command has no effect in single-shot conversion mode.

Hold the START/SYNC pin low when the device is controlled through START and STOP commands.

### 9.5.3.7 SYOCAL

The SYOCAL command initiates a system offset calibration. For a system offset calibration, the inputs must be externally shorted to a voltage within the input range, ideally near the mid-supply voltage of  $(AVDD + AVSS) / 2$ . The OFC registers are updated when the command completes. Calibration commands must be issued in conversion mode.

### 9.5.3.8 SYGCAL

The SYGCAL command initiates the system gain calibration. For a system gain calibration, the input must be externally set to full-scale. The FSC registers are updated after this operation. Calibration commands must be issued in conversion mode.

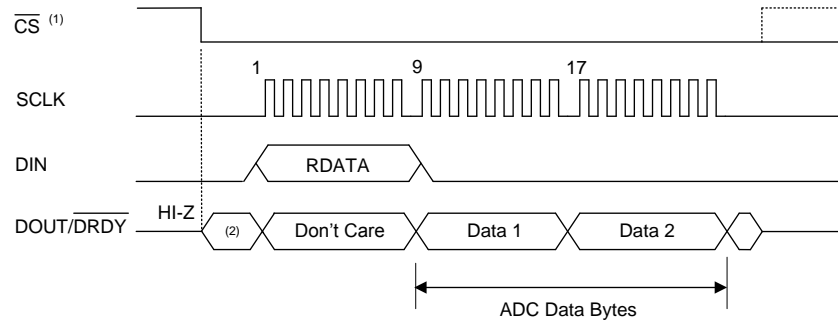
### 9.5.3.9 SFOCAL

The SFOCAL command initiates a self offset calibration. The device internally shorts the inputs to mid-supply and performs the calibration. The OFC registers are updated after this operation. Calibration commands must be issued in conversion mode.

### 9.5.3.10 RDATA

Read conversion data from the device with the RDATA command at any time. Figure 73 shows the read data sequence. The MSB of the conversion data is output on the first SCLK rising edge after the command. An RDATA command must be sent for each read operation. The ADC does not respond to commands until the read operation is complete, or terminated by taking  $\overline{CS}$  high. New data indicated by the  $\overline{DRDY}$  and  $DOUT/\overline{DRDY}$  will not corrupt a read of conversion data with RDATA.

After all bytes are read, the data-byte sequence is repeated by continuing SCLK.



(1)  $\overline{CS}$  can be tied low. If  $\overline{CS}$  is low,  $DOUT/\overline{DRDY}$  asserts low with  $\overline{DRDY}$ .

(2)  $DOUT/\overline{DRDY}$  is driven low with  $\overline{DRDY}$ . If a read operation occurs after the  $\overline{DRDY}$  falling edge, then  $DOUT/\overline{DRDY}$  can be high or low.

**Figure 73. Read Data Sequence**

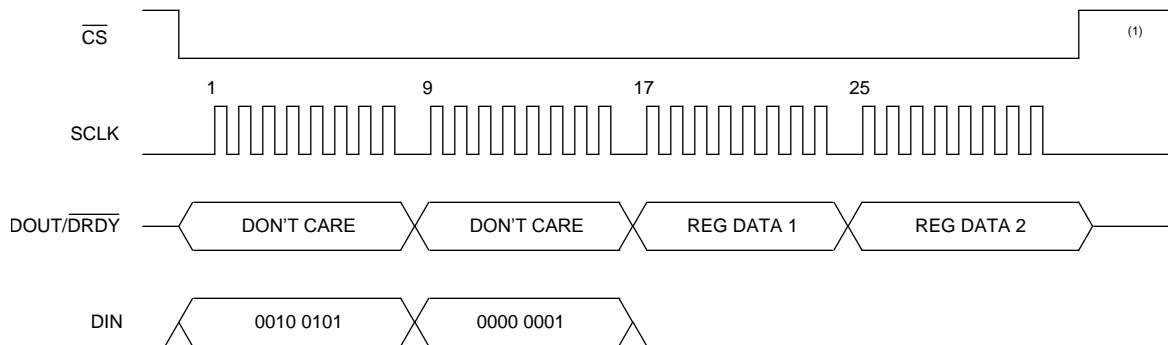
### 9.5.3.11 RREG

Use the RREG command to read the device register data. Read the register data one register at a time, or read a block of register data. The starting register address can be any register in the register map. The RREG command consists of two bytes. The first byte specifies the starting register address: 001r rrrr, where r rrrr is the starting register address. The second command byte is the number of registers to read (minus 1): 000n nnnn, where n nnnn is the number of registers to read minus 1.

After the read command is sent, the ADC responds with one or more register data bytes, most significant bit first. If the byte count exceeds the last register address, the ADC begins to output zero data. During the register read operation, any conversion data that becomes available is not loaded to the output shift register to avoid data contention. However, the conversion data can be retrieved later by the RDATA command. After the register read command has started, further commands are blocked until one of the following conditions are met:

- The read operation is completed
- The read operation is terminated by taking  $\overline{CS}$  high
- The read operation is terminated by a serial interface timeout
- The ADC is reset by toggling the  $\overline{RESET}$  pin

Figure 74 shows a two-register read operation example. As shown, the commands required to read data from two registers starting at register REF (address = 05h) are: command byte 1 = 25h and command byte 2 = 01h. Keep DIN low after the two command bytes are sent.



(1)  $\overline{CS}$  can be set high or kept low between commands. If kept low, the command must be completed.

**Figure 74. Read Register Sequence**

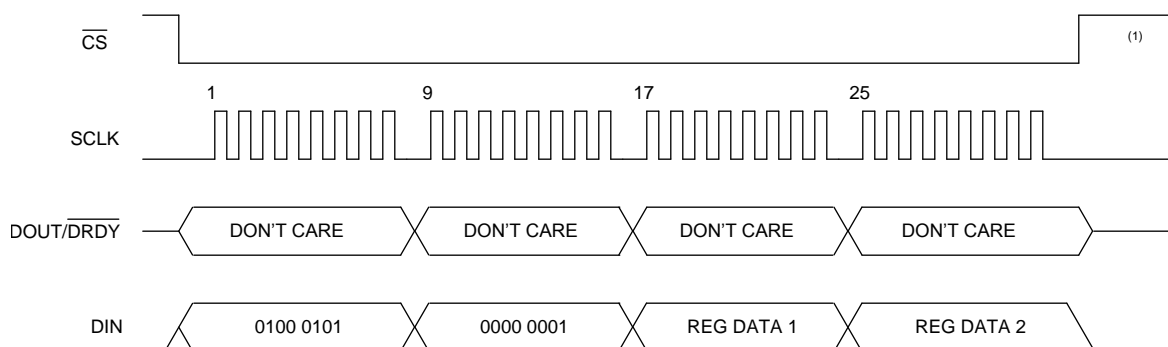
### 9.5.3.12 WREG

Use the WREG command to write the device register data. The register data are written one register at a time or as a block of register data. The starting register address is any register in the register map.

The WREG command consists of two bytes. The first byte specifies the starting register address: 010r rrrr, where *r rrrr* is the starting register address. The second command byte is the number of registers to write (minus 1): 000n nnnn, where *n nnnn* is the number of registers to write minus 1. The following byte (or bytes) is the register data, most significant bit first. If the byte count exceeds the last register address, the ADC ignores the data. After the register write command has started, further commands are blocked until one of the following conditions are met:

- The write operation is completed
- The write operation is terminated by taking  $\overline{CS}$  high
- The write operation is terminated by a serial interface timeout
- The ADC is reset by toggling the  $\overline{RESET}$  pin

Figure 75 shows a two-register write operation example. As shown, the required commands to write data to two registers starting at register REF (address = 05h) are: command byte 1 = 45h and command byte 2 = 01h.



(1)  $\overline{CS}$  can be set high or kept low between commands. If kept low, the command must be completed.

**Figure 75. Write Register Sequence**

Writing new data to certain configuration registers resets the digital filter and starts a new conversion if a conversion is in progress. Writing to the following registers triggers a new conversion:

- Channel configuration register (02h)
- Gain setting register (03h)
- Data rate register (04h)
- Reference control register (05h), bits [5:0]
- Excitation current register 1 (06h), bits [3:0]
- Excitation current register 2 (07h)
- System control register (09h), bits [7:5]

When the device is configured with WREG, the first data ready indication occurs after the new conversion completes with the configuration settings. The previous conversion data are cleared at restart; therefore read the previous data before the register write operation. Again, a WREG to these registers only starts a new conversion if a conversion is in progress. If the device is in standby mode, the device sets the configuration according to the WREG data, but does not start a conversion until the START/SYNC pin is taken high or a START command is issued.

#### 9.5.4 Interfacing with Multiple Devices

When connecting multiple devices to a single SPI bus, SCLK, DIN, and  $\overline{\text{DOUT/DRDY}}$  can be safely shared by using a dedicated chip-select ( $\overline{\text{CS}}$ ) line for each SPI-enabled device. When  $\overline{\text{CS}}$  transitions high for the respective device,  $\overline{\text{DOUT/DRDY}}$  enters a tri-state mode. Therefore,  $\overline{\text{DOUT/DRDY}}$  cannot be used to indicate when new data are available if  $\overline{\text{CS}}$  is high. Only the dedicated  $\overline{\text{DRDY}}$  pin indicates that new data are available because the  $\overline{\text{DRDY}}$  pin is actively driven even when  $\overline{\text{CS}}$  is high.

In some cases, the  $\overline{\text{DRDY}}$  pin cannot be interfaced to the microcontroller. This scenario can occur if there are insufficient GPIO channels available on the microcontroller or if the serial interface must be galvanically isolated and thus the amount of channels must be limited. In order to evaluate when a new conversion of one of the devices is ready, the microcontroller can periodically drop  $\overline{\text{CS}}$  to the respective device and poll the state of the  $\overline{\text{DOUT/DRDY}}$  pin.

When  $\overline{\text{CS}}$  goes low, the  $\overline{\text{DOUT/DRDY}}$  pin immediately drives either high or low. If the  $\overline{\text{DOUT/DRDY}}$  line drives low, new data are available. If the  $\overline{\text{DOUT/DRDY}}$  line drives high, no new data are available. This procedure requires that  $\overline{\text{DOUT/DRDY}}$  is forced high after reading each conversion result and before taking  $\overline{\text{CS}}$  high. To make sure  $\overline{\text{DOUT/DRDY}}$  is taken high, send a RREG command to read a register where the least significant bit is 1.

## 9.6 Register Map

### 9.6.1 Configuration Registers

The ADS114S0xB register map consists of 18, 8-bit registers. These registers are used to configure and control the device to the desired mode of operation. Access the registers through the serial interface by using the RREG and WREG register commands. After power-on or reset, the registers default to the initial settings, as shown in the *Default* column of [Table 14](#).

Data can be written as a block to multiple registers using a single WREG command. If data are written as a block, the data of certain registers take effect immediately when data are shifted in. Writing new data to certain registers results in a restart of conversions that are in progress. The registers that result in a conversion restart are discussed in the [WREG](#) section.

**Table 14. Configuration Register Map**

| ADDR | REGISTER | DEFAULT | BIT 7        | BIT 6                   | BIT 5                         | BIT 4                         | BIT 3       | BIT 2     | BIT 1       | BIT 0   |  |
|------|----------|---------|--------------|-------------------------|-------------------------------|-------------------------------|-------------|-----------|-------------|---------|--|
| 00h  | ID       | xxh     | RESERVED     |                         |                               |                               |             |           | DEV_ID[2:0] |         |  |
| 01h  | STATUS   | 80h     | FL_POR       | $\overline{\text{RDY}}$ | 0                             | 0                             | 0           | 0         | 0           | 0       |  |
| 02h  | INPMUX   | 01h     | MUXP[3:0]    |                         |                               |                               | MUXN[3:0]   |           |             |         |  |
| 03h  | PGA      | 00h     | 0            | 0                       | 0                             | PGA_EN[1:0]                   |             | GAIN[2:0] |             |         |  |
| 04h  | DATARATE | 14h     | 0            | CLK                     | MODE                          | 1                             |             | DR[3:0]   |             |         |  |
| 05h  | REF      | 10h     | 0            | 0                       | $\overline{\text{REFP\_BUF}}$ | $\overline{\text{REFN\_BUF}}$ | REFSEL[1:0] |           | REFCON[1:0] |         |  |
| 06h  | IDACMAG  | 00h     | 0            | 0                       | 0                             | 0                             | IMAG[3:0]   |           |             |         |  |
| 07h  | IDACMUX  | FFh     | I2MUX[3:0]   |                         |                               |                               | I1MUX[3:0]  |           |             |         |  |
| 08h  | VBIAS    | 00h     | 0            | VB_AINC                 | VB_AIN5                       | VB_AIN4                       | VB_AIN3     | VB_AIN2   | VB_AIN1     | VB_AIN0 |  |
| 09h  | SYS      | 10h     | SYS_MON[2:0] |                         |                               | CAL_SAMP[1:0]                 |             | TIMEOUT   | 0           | 0       |  |
| 0Ah  | RESERVED | 00h     | RESERVED     |                         |                               |                               |             |           |             |         |  |
| 0Bh  | OFCAL0   | 00h     | OFC[7:0]     |                         |                               |                               |             |           |             |         |  |
| 0Ch  | OFCAL1   | 00h     | OFC[15:8]    |                         |                               |                               |             |           |             |         |  |
| 0Dh  | RESERVED | 00h     | RESERVED     |                         |                               |                               |             |           |             |         |  |
| 0Eh  | FSCAL0   | 00h     | FSC[7:0]     |                         |                               |                               |             |           |             |         |  |
| 0Fh  | FSCAL1   | 40h     | FSC[15:8]    |                         |                               |                               |             |           |             |         |  |
| 10h  | GPIODAT  | 00h     | DIR[3:0]     |                         |                               |                               | DAT[3:0]    |           |             |         |  |
| 11h  | GPIOCON  | 00h     | 0            | 0                       | 0                             | 0                             | CON[3:0]    |           |             |         |  |

## 9.6.2 Register Descriptions

Table 15 lists the access codes for the ADS114S0xB registers.

**Table 15. ADS114S0xB Access Type Codes**

| Access Type | Code | Description                            |
|-------------|------|--|
| R           | R    | Read                                   |
| R-W         | R/W  | Read or Write                          |
| W           | W    | Write                                  |
| -n          |      | Value after reset or the default value |

### 9.6.2.1 Device ID Register (address = 00h) [reset = xxh]

**Figure 76. Device ID (ID) Register**

| 7        | 6 | 5 | 4 | 3 | 2           | 1 | 0 |
|----------|---|---|---|---|-------------|---|---|
| RESERVED |   |   |   |   | DEV_ID[2:0] |   |   |
| R-xxh    |   |   |   |   | R-xh        |   |   |

**Table 16. Device ID (ID) Register Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7:3 | RESERVED    | R    | xxh   | <b>Reserved</b><br>Values are subject to change without notice  |
| 2:0 | DEV_ID[2:0] | R    | xh    | <b>Device identifier.</b><br>Identifies the model of the device.<br>000 : Reserved<br>001 : Reserved<br>010 : Reserved<br>011 : Reserved<br>100 : ADS114S08B (12 channels, 16 bits)<br>101 : ADS114S06B (6 channels, 16 bits)<br>110 : Reserved<br>111 : Reserved |

### 9.6.2.2 Device Status Register (address = 01h) [reset = 80h]

**Figure 77. Device Status (STATUS) Register**

| 7      | 6                       | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|-------------------------|------|------|------|------|------|------|
| FL_POR | $\overline{\text{RDY}}$ | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W-1h | R-0h                    | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

**Table 17. Device Status (STATUS) Register Field Descriptions**

| Bit | Field                   | Type | Reset | Description  |
|-----|-------------------------|------|-------|--|
| 7   | FL_POR                  | R/W  | 1h    | <b>POR flag.</b><br>Indicates a power-on reset (POR) event has occurred.<br>0 : Register has been cleared and no POR event has occurred<br>1 : POR event occurred and has not been cleared. Flag must be cleared by user register write (default). |
| 6   | $\overline{\text{RDY}}$ | R    | 0h    | <b>Device ready flag.</b><br>Indicates the device has started up and is ready for communication.<br>0 : ADC ready for communication (default)<br>1 : ADC not ready   |
| 5:0 | RESERVED                | R    | 00h   | <b>Reserved</b><br>Always write 00h  |

**9.6.2.3 Input Multiplexer Register (address = 02h) [reset = 01h]**
**Figure 78. Input Multiplexer (INPMUX) Register**

|           |   |   |   |           |   |   |   |
|-----------|---|---|---|-----------|---|---|---|
| 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
| MUXP[3:0] |   |   |   | MUXN[3:0] |   |   |   |
| R/W-0h    |   |   |   | R/W-1h    |   |   |   |

**Table 18. Input Multiplexer (INPMUX) Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7:4 | MUXP[3:0] | R/W  | 0h    | <b>Positive ADC input selection.</b><br>Selects the ADC positive input channel.<br>0000 : AIN0 (default)<br>0001 : AIN1<br>0010 : AIN2<br>0011 : AIN3<br>0100 : AIN4<br>0101 : AIN5<br>0110 : AIN6 (ADS114S08B only)<br>0111 : AIN7 (ADS114S08B only)<br>1000 : AIN8 (ADS114S08B only)<br>1001 : AIN9 (ADS114S08B only)<br>1010 : AIN10 (ADS114S08B only)<br>1011 : AIN11 (ADS114S08B only)<br>1100 : AINCOM<br>1101 : Reserved<br>1110 : Reserved<br>1111 : Reserved |
| 3:0 | MUXN[3:0] | R/W  | 1h    | <b>Negative ADC input selection.</b><br>Selects the ADC negative input channel.<br>0000 : AIN0<br>0001 : AIN1 (default)<br>0010 : AIN2<br>0011 : AIN3<br>0100 : AIN4<br>0101 : AIN5<br>0110 : AIN6 (ADS114S08B only)<br>0111 : AIN7 (ADS114S08B only)<br>1000 : AIN8 (ADS114S08B only)<br>1001 : AIN9 (ADS114S08B only)<br>1010 : AIN10 (ADS114S08B only)<br>1011 : AIN11 (ADS114S08B only)<br>1100 : AINCOM<br>1101 : Reserved<br>1110 : Reserved<br>1111 : Reserved |



**9.6.2.4 Gain Setting Register (address = 03h) [reset = 00h]**
**Figure 79. Gain Setting (PGA) Register**

|        |        |        |             |   |           |   |   |
|--------|--------|--------|-------------|---|-----------|---|---|
| 7      | 6      | 5      | 4           | 3 | 2         | 1 | 0 |
| 0      | 0      | 0      | PGA_EN[1:0] |   | GAIN[2:0] |   |   |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h      |   | R/W-0h    |   |   |

**Table 19. Gain Setting (PGA) Register Field Descriptions**

| Bit | Field       | Type | Reset | Description  |
|-----|-------------|------|-------|--|
| 7:5 | RESERVED    | R/W  | 0h    | <b>Reserved</b><br>Always write 0h   |
| 4:3 | PGA_EN[1:0] | R/W  | 0h    | <b>PGA enable.</b><br>Enables or bypasses the PGA.<br>00 : PGA is powered down and bypassed. Enables single-ended measurements with unipolar supply (Set gain = 1 <sup>(1)</sup> ) (default)<br>01 : PGA enabled (gain = 1 to 128)<br>10 : Reserved<br>11 : Reserved |
| 2:0 | GAIN[2:0]   | R/W  | 0h    | <b>PGA gain selection.</b><br>Configures the PGA gain.<br>000 : 1 (default)<br>001 : 2<br>010 : 4<br>011 : 8<br>100 : 16<br>101 : 32<br>110 : 64<br>111 : 128  |

(1) When bypassing the PGA, the user must also set GAIN[2:0] to 000.

**9.6.2.5 Data Rate Register (address = 04h) [reset = 14h]**
**Figure 80. Data Rate (DATARATE) Register**

| 7      | 6      | 5      | 4      | 3       | 2 | 1 | 0 |
|--------|--------|--------|--------|---------|---|---|---|
| 0      | CLK    | MODE   | 1      | DR[3:0] |   |   |   |
| R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-4h  |   |   |   |

**Table 20. Data Rate (DATARATE) Register Field Descriptions**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7   | RESERVED | R/W  | 0h    | <b>Reserved</b><br>Always write 0h   |
| 6   | CLK      | R/W  | 0h    | <b>Clock source selection.</b><br>Configures the clock source to use either the internal oscillator or an external clock.<br>0 : Internal 4.096-MHz oscillator (default)<br>1 : External clock   |
| 5   | MODE     | R/W  | 0h    | <b>Conversion mode selection.</b><br>Configures the ADC for either continuous conversion or single-shot conversion mode.<br>0 : Continuous conversion mode (default)<br>1 : Single-shot conversion mode  |
| 4   | RESERVED | R/W  | 1h    | <b>Reserved</b><br>Always write 1h   |
| 3:0 | DR[3:0]  | R/W  | 4h    | <b>Data rate selection.</b><br>Configures the output data rate <sup>(1)</sup> .<br>0000 : 2.5 SPS<br>0001 : 5 SPS<br>0010 : 10 SPS<br>0011 : 16.6 SPS<br>0100 : 20 SPS (default)<br>0101 : 50SPS<br>0110 : 60 SPS<br>0111 : 100 SPS<br>1000 : 200 SPS<br>1001 : 400 SPS<br>1010 : 800 SPS<br>1011 : 1000 SPS<br>1100 : 2000 SPS<br>1101 : 4000 SPS<br>1110 : 4000 SPS<br>1111 : Reserved |

(1) Data rates of 60 Hz or less can offer line-cycle rejection; see the [50-Hz and 60-Hz Line Cycle Rejection](#) section for more information.

**9.6.2.6 Reference Control Register (address = 05h) [reset = 10h]**
**Figure 81. Reference Control (REF) Register**

| 7      | 6      | 5        | 4        | 3           | 2 | 1           | 0 |
|--------|--------|----------|----------|-------------|---|-------------|---|
| 0      | 0      | REFP_BUF | REFN_BUF | REFSEL[1:0] |   | REFCON[1:0] |   |
| R/W-0h | R/W-0h | R/W-0h   | R/W-1h   | R/W-0h      |   | R/W-0h      |   |

**Table 21. Reference Control (REF) Register Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7:6 | RESERVED    | R/W  | 0h    | <b>Reserved</b><br>Always write 0h  |
| 5   | REFP_BUF    | R/W  | 0h    | <b>Positive reference buffer bypass.</b><br>Disables the positive reference buffer. Recommended when $V_{(REFP_x)}$ is close to AVDD.<br>0 : Enabled (default)<br>1 : Disabled  |
| 4   | REFN_BUF    | R/W  | 1h    | <b>Negative reference buffer bypass.</b><br>Disables the negative reference buffer. Recommended when $V_{(REFN_x)}$ is close to AVSS.<br>0 : Enabled<br>1 : Disabled (default)  |
| 3:2 | REFSEL[1:0] | R/W  | 0h    | <b>Reference input selection.</b><br>Selects the reference input source for the ADC.<br>00 : REFP0, REFN0 (default)<br>01 : REFP1, REFN1<br>10 : Internal 2.5-V reference <sup>(1)</sup><br>11 : Reserved   |
| 1:0 | REFCON[1:0] | R/W  | 0h    | <b>Internal voltage reference configuration<sup>(2)</sup>.</b><br>Configures the behavior of the internal voltage reference.<br>00 : Internal reference off (default)<br>01 : Internal reference on, but powers down in power-down mode<br>10 : Internal reference is always on, even in power-down mode<br>11 : Reserved |

(1) Disable the reference buffers when the internal reference is selected for measurements.

(2) The internal voltage reference must be turned on to use the IDACs.

**9.6.2.7 Excitation Current Register 1 (address = 06h) [reset = 00h]**
**Figure 82. Excitation Current Register 1 (IDACMAG)**

|        |        |        |        |           |   |   |   |
|--------|--------|--------|--------|-----------|---|---|---|
| 7      | 6      | 5      | 4      | 3         | 2 | 1 | 0 |
| 0      | 0      | 0      | 0      | IMAG[3:0] |   |   |   |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h    |   |   |   |

**Table 22. Excitation Current Register 1 (IDACMAG) Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7:4 | RESERVED  | R/W  | 0h    | <b>Reserved</b><br>Always write 0h   |
| 3:0 | IMAG[3:0] | R/W  | 0h    | <b>IDAC magnitude selection.</b><br>Selects the value of the excitation current sources. Sets IDAC1 and IDAC2 to the same value.<br>0000 : Off (default)<br>0001 : 10 $\mu$ A<br>0010 : 50 $\mu$ A<br>0011 : 100 $\mu$ A<br>0100 : 250 $\mu$ A<br>0101 : 500 $\mu$ A<br>0110 : 750 $\mu$ A<br>0111 : 1000 $\mu$ A<br>1000 : 1500 $\mu$ A<br>1001 : 2000 $\mu$ A<br>1010–1111 : Off |

**9.6.2.8 Excitation Current Register 2 (address = 07h) [reset = FFh]**
**Figure 83. Excitation Current Register 2 (IDACMUX)**

| 7          | 6 | 5 | 4 | 3          | 2 | 1 | 0 |
|------------|---|---|---|------------|---|---|---|
| I2MUX[3:0] |   |   |   | I1MUX[3:0] |   |   |   |
| R/W-Fh     |   |   |   | R/W-Fh     |   |   |   |

**Table 23. Excitation Current Register 2 (IDACMUX) Register Field Descriptions**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7:4 | I2MUX[3:0] | R/W  | Fh    | <b>IDAC2 output channel selection.</b><br>Selects the output channel for IDAC2.<br>0000 : AIN0<br>0001 : AIN1<br>0010 : AIN2<br>0011 : AIN3<br>0100 : AIN4<br>0101 : AIN5<br>0110 : AIN6 (ADS114S08B), REFP1 (ADS114S06B)<br>0111 : AIN7 (ADS114S08B), REFN1 (ADS114S06B)<br>1000 : AIN8 (ADS114S08B only)<br>1001 : AIN9 (ADS114S08B only)<br>1010 : AIN10 (ADS114S08B only)<br>1011 : AIN11 (ADS114S08B only)<br>1100 : AINCOM<br>1101–1111 : Disconnected (default)           |
| 3:0 | I1MUX[3:0] | R/W  | Fh    | <b>IDAC1 output channel selection.</b><br>Selects the output channel for IDAC1.<br>0000 : AIN0<br>0001 : AIN1<br>0010 : AIN2<br>0011 : AIN3<br>0100 : AIN4<br>0101 : AIN5<br>0110 : AIN6 (ADS114S08B only), REFP1 (ADS114S06B)<br>0111 : AIN7 (ADS114S08B only), REFN1 (ADS114S06B)<br>1000 : AIN8 (ADS114S08B only)<br>1001 : AIN9 (ADS114S08B only)<br>1010 : AIN10 (ADS114S08B only)<br>1011 : AIN11 (ADS114S08B only)<br>1100 : AINCOM<br>1101–1111 : Disconnected (default) |

**9.6.2.9 Sensor Biasing Register (address = 08h) [reset = 00h]**
**Figure 84. Sensor Biasing (VBIAS) Register**

| 7      | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|--------|---------|---------|---------|---------|---------|---------|---------|
| 0      | VB_AINC | VB_AIN5 | VB_AIN4 | VB_AIN3 | VB_AIN2 | VB_AIN1 | VB_AIN0 |
| R/W-0h | R/W-0h  | R/W-0h  | R/W-0h  | R/W-0h  | R/W-0h  | R/W-0h  | R/W-0h  |

**Table 24. Sensor Biasing (VBIAS) Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7   | RESERVED | R/W  | 0h    | <b>Reserved</b><br>Always write 0h  |
| 6   | VB_AINC  | R/W  | 0h    | <b>AINCOM VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AINCOM pin.<br>0 : VBIAS disconnected from AINCOM (default)<br>1 : VBIAS connected to AINCOM |
| 5   | VB_AIN5  | R/W  | 0h    | <b>AIN5 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN5 pin.<br>0 : VBIAS disconnected from AIN5 (default)<br>1 : VBIAS connected to AIN5         |
| 4   | VB_AIN4  | R/W  | 0h    | <b>AIN4 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN4 pin.<br>0 : VBIAS disconnected from AIN4 (default)<br>1 : VBIAS connected to AIN4         |
| 3   | VB_AIN3  | R/W  | 0h    | <b>AIN3 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN3 pin.<br>0 : VBIAS disconnected from AIN3 (default)<br>1 : VBIAS connected to AIN3         |
| 2   | VB_AIN2  | R/W  | 0h    | <b>AIN2 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN2 pin.<br>0 : VBIAS disconnected from AIN2 (default)<br>1 : VBIAS connected to AIN2         |
| 1   | VB_AIN1  | R/W  | 0h    | <b>AIN1 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN1 pin.<br>0 : VBIAS disconnected from AIN1 (default)<br>1 : VBIAS connected to AIN1         |
| 0   | VB_AIN0  | R/W  | 0h    | <b>AIN0 VBIAS selection<sup>(1)</sup>.</b><br>Enables VBIAS on the AIN0 pin.<br>0 : VBIAS disconnected from AIN0 (default)<br>1 : VBIAS connected to AIN0         |

(1) The bias voltage can be selected for multiple analog inputs at the same time.

**9.6.2.10 System Control Register (address = 09h) [reset = 10h]**
**Figure 85. System Control (SYS) Register**

| 7            | 6 | 5             | 4 | 3       | 2 | 1      | 0      |
|--------------|---|---------------|---|---------|---|--------|--------|
| SYS_MON[2:0] |   | CAL_SAMP[1:0] |   | TIMEOUT |   | 0      | 0      |
| R/W-0h       |   | R/W-2h        |   | R/W-0h  |   | R/W-0h | R/W-0h |

**Table 25. System Control (SYS) Register Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7:5 | SYS_MON[2:0]  | R/W  | 0h    | <b>System monitor configuration<sup>(1)</sup>.</b><br>Enables a set of system monitor measurements using the ADC.<br>000 : Disabled (default)<br>001 : PGA inputs shorted to (AVDD + AVSS) / 2 and disconnected from AINx and the multiplexer; gain set by user<br>010 : Internal temperature sensor measurement; PGA must be enabled (PGA_EN[1:0] = 01); gain set by user <sup>(2)</sup><br>011 : (AVDD – AVSS) / 4 measurement; gain set to 1 <sup>(3)</sup><br>100 : DVDD / 4 measurement; gain set to 1 <sup>(3)</sup><br>101 : Burn-out current sources enabled, 0.2- $\mu$ A setting<br>110 : Burn-out current sources enabled, 1- $\mu$ A setting<br>111 : Burn-out current sources enabled, 10- $\mu$ A setting |
| 4:3 | CAL_SAMP[1:0] | R/W  | 2h    | <b>Calibration sample size selection.</b><br>Configures the number of samples averaged for self and system offset and system gain calibration.<br>00 : 1 sample<br>01 : 4 samples<br>10 : 8 samples (default)<br>11 : 16 samples  |
| 2   | TIMEOUT       | R/W  | 0h    | <b>SPI timeout enable.</b><br>Enables the SPI timeout function.<br>0 : Disabled (default)<br>1 : Enabled  |
| 1:0 | RESERVED      | R/W  | 0h    | <b>Reserved</b><br>Always write 0h  |

- (1) With system monitor functions enabled, the AINx multiplexer switches are open for the (AVDD + AVSS) / 2 measurement, the temperature sensor, and the supply monitors.
- (2) When using the internal temperature sensor, gain must be 4 or less to keep the measurement within the PGA input voltage range.
- (3) The PGA gain is automatically set to 1 when the supply monitors are enabled, regardless of the setting in GAIN[2:0].

**9.6.2.11 Reserved Register (address = 0Ah) [reset = 00h]**
**Figure 86. Reserved Register**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   |   |   |   |   |   |   |
| R-00h    |   |   |   |   |   |   |   |

**Table 26. Reserved Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                         |
|-----|----------|------|-------|-------------------------------------|
| 7:0 | RESERVED | R    | 00h   | <b>Reserved</b><br>Always write 00h |

**9.6.2.12 Offset Calibration Register 1 (address = 0Bh) [reset = 00h]**
**Figure 87. Offset Calibration Register 1 (OFCAL0)**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFC[7:0] |   |   |   |   |   |   |   |
| R/W-00h  |   |   |   |   |   |   |   |

**Table 27. Offset Calibration Register 1 (OFCAL0) Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                 |
|-----|----------|------|-------|---|
| 7:0 | OFC[7:0] | R/W  | 00h   | Bits [7:0] of the offset calibration value. |

**9.6.2.13 Offset Calibration Register 2 (address = 0Ch) [reset = 00h]**
**Figure 88. Offset Calibration Register 2 (OFCAL1)**

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFC[15:8] |   |   |   |   |   |   |   |
| R/W-00h   |   |   |   |   |   |   |   |

**Table 28. Offset Calibration Register 2 (OFCAL1) Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                  |
|-----|-----------|------|-------|--|
| 7:0 | OFC[15:8] | R/W  | 00h   | Bits [15:8] of the offset calibration value. |



**9.6.2.14 Reserved Register (address = 0Dh) [reset = 00h]**
**Figure 89. Reserved Register**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   |   |   |   |   |   |   |
| R-00h    |   |   |   |   |   |   |   |

**Table 29. Reserved Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                         |
|-----|----------|------|-------|-------------------------------------|
| 7:0 | RESERVED | R    | 00h   | <b>Reserved</b><br>Always write 00h |

**9.6.2.15 Gain Calibration Register 1 (address = 0Eh) [reset = 00h]**
**Figure 90. Gain Calibration Register 1 (FSCAL0)**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FSC[7:0] |   |   |   |   |   |   |   |
| R/W-00h  |   |   |   |   |   |   |   |

**Table 30. Gain Calibration Register 1 (FSCAL0) Field Descriptions**

| Bit | Field    | Type | Reset | Description                               |
|-----|----------|------|-------|---|
| 7:0 | FSC[7:0] | R/W  | 00h   | Bits [7:0] of the gain calibration value. |

**9.6.2.16 Gain Calibration Register 2 (address = 0Fh) [reset = 40h]**
**Figure 91. Gain Calibration Register 2 (FSCAL1)**

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FSC[15:8] |   |   |   |   |   |   |   |
| R/W-40h   |   |   |   |   |   |   |   |

**Table 31. Gain Calibration Register 2 (FSCAL1) Field Descriptions**

| Bit | Field     | Type | Reset | Description                                |
|-----|-----------|------|-------|--|
| 7:0 | FSC[15:8] | R/W  | 40h   | Bits [15:8] of the gain calibration value. |

**9.6.2.17 GPIO Data Register (address = 10h) [reset = 00h]**
**Figure 92. GPIO Data (GPIODAT) Register**

| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|----------|---|---|---|----------|---|---|---|
| DIR[3:0] |   |   |   | DAT[3:0] |   |   |   |
| R/W-0h   |   |   |   | R/W-0h   |   |   |   |

**Table 32. GPIO Data (GPIODAT) Register Field Descriptions**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7:4 | DIR[3:0] | R/W  | 0h    | <b>GPIO direction.</b><br>Configures the selected GPIO as an input or output.<br>0 : GPIO[x] configured as output (default)<br>1 : GPIO[x] configured as input |
| 3:0 | DAT[3:0] | R/W  | 0h    | <b>GPIO data.</b><br>Contains the data of the GPIO inputs or outputs.<br>0 : GPIO[x] is low (default)<br>1 : GPIO[x] is high                                   |

**9.6.2.18 GPIO Configuration Register (address = 11h) [reset = 00h]**
**Figure 93. GPIO Configuration Register**

| 7    | 6    | 5    | 4    | 3        | 2 | 1 | 0 |
|------|------|------|------|----------|---|---|---|
| 0    | 0    | 0    | 0    | CON[3:0] |   |   |   |
| R-0h | R-0h | R-0h | R-0h | R/W-0h   |   |   |   |

**Table 33. GPIO Configuration (GPIOCON) Register Field Descriptions**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7:4 | RESERVED | R    | 0h    | <b>Reserved</b><br>Always write 0h   |
| 3:0 | CON[3:0] | R/W  | 0h    | <b>GPIO pin configuration.</b><br>Configures the GPIO[x] pin as an analog input or GPIO. CON[x] corresponds to the GPIO[x] pin.<br>0 : GPIO[x] configured as analog input (default) <sup>(1)</sup><br>1 : GPIO[x] configured as GPIO |

(1) On the ADS114S06B, the GPIO pins default as disabled. Set the CON[3:0] bits to enable the respective GPIO pins.

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The ADS114S06B and ADS114S08B are precision, 16-bit,  $\Delta\Sigma$  ADCs that offer many integrated features to simplify the measurement of the most common sensor types (including various types of temperature, flow, and bridge sensors). Primary considerations when designing an application with the ADS114S0xB include analog input filtering, establishing an appropriate reference, and setting the absolute input voltage for the internal PGA. Connecting and configuring the serial interface appropriately is another concern. These considerations are discussed in the following sections.

#### 10.1.1 Serial Interface Connections

The principle serial interface connections for the ADS114S0xB are shown in Figure 94.

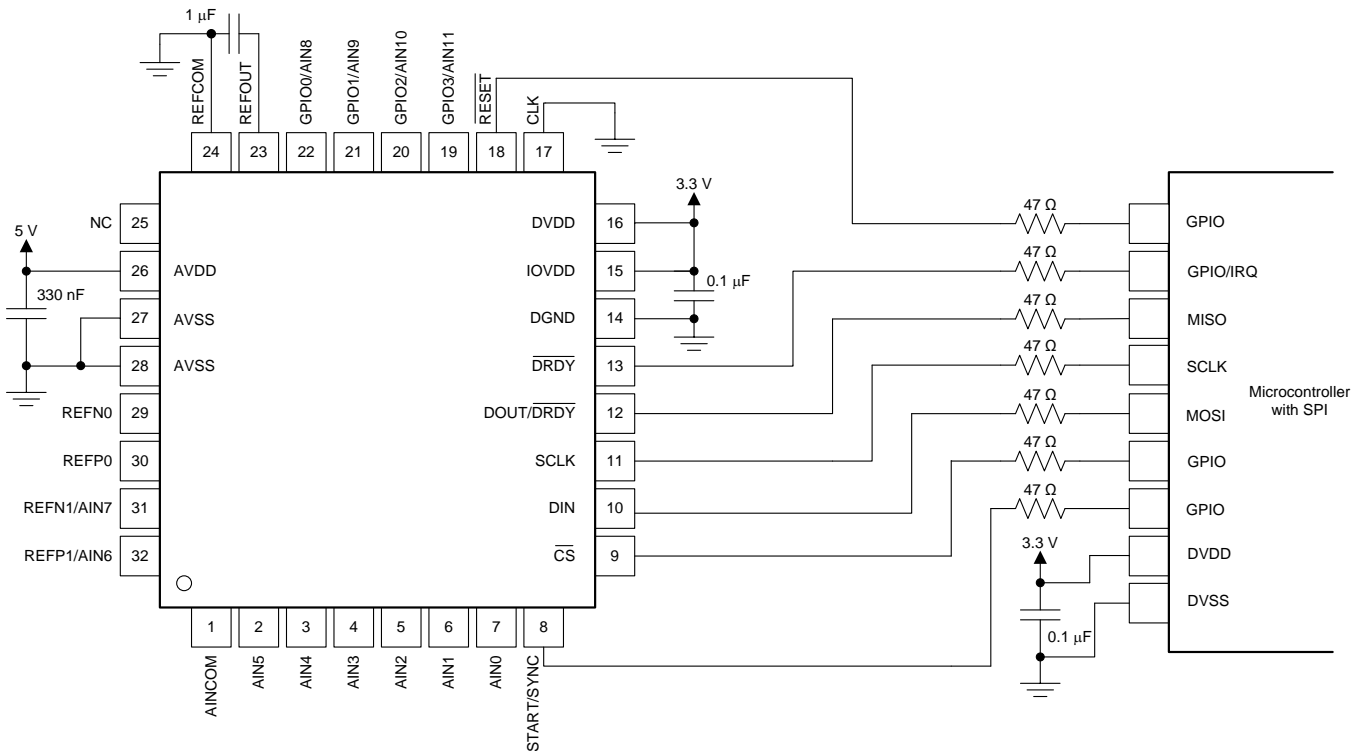


Figure 94. Serial Interface Connections

Most microcontroller SPI peripherals can interface with the ADS114S0xB. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the devices are found in the [Serial Interface](#) section.

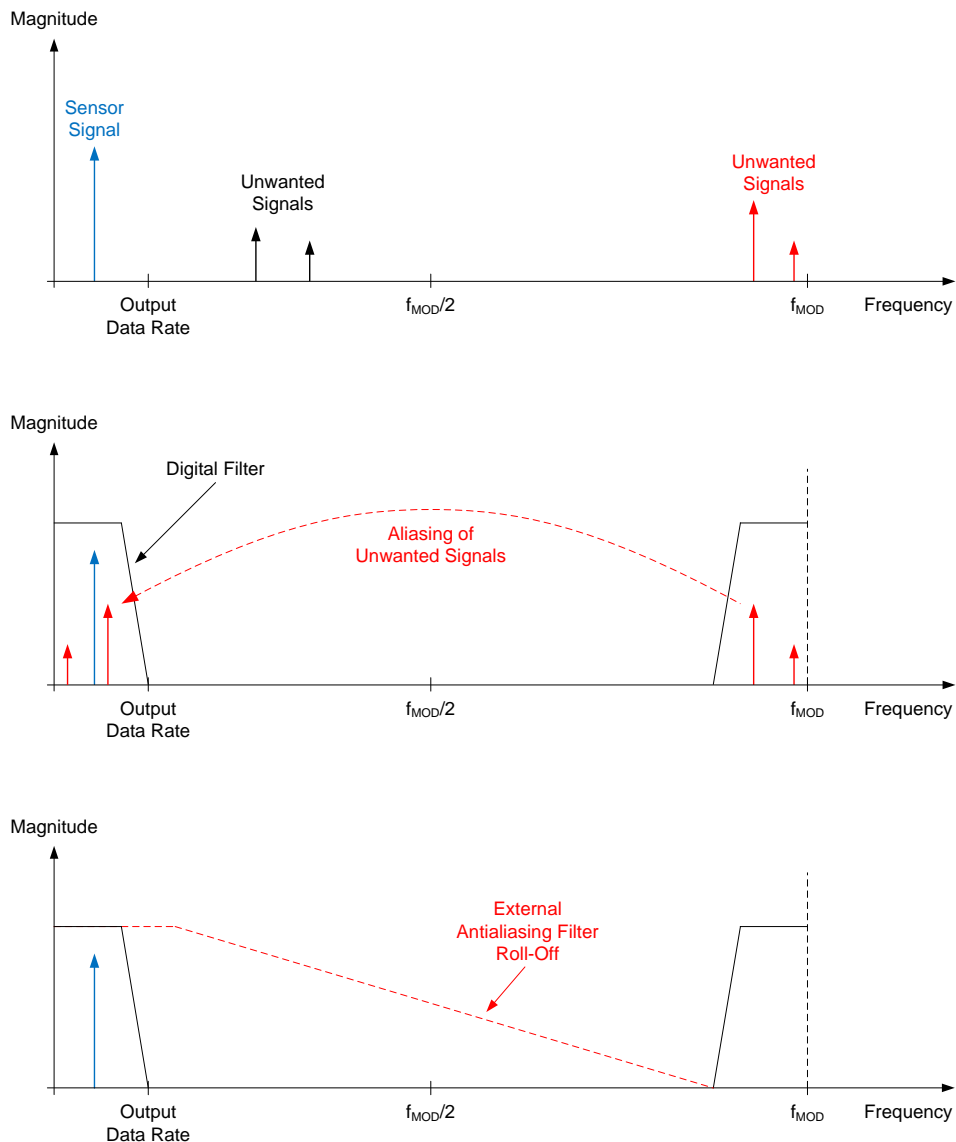
Place 47- $\Omega$  resistors in series with all digital input and output pins ( $\overline{CS}$ , SCLK, DIN, DOUT/ $\overline{DRDY}$ , and  $\overline{DRDY}$ ). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

## Application Information (continued)

### 10.1.2 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Inside a  $\Delta\Sigma$  ADC, the input signal is oversampled at the modulator frequency,  $f_{MOD}$  and not at the output data rate. The filter response of the digital filter repeats at multiples of  $f_{MOD}$ , as shown in Figure 95. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.



**Figure 95. Effect of Aliasing**

## Application Information (continued)

Many sensor signals are inherently band limited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass band when using a  $\Delta\Sigma$  ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either eliminate aliasing, or to reduce the effect of aliasing to a level below the noise floor of the sensor. Ideally, any signal beyond  $f_{\text{MOD}} / 2$  is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS114S0xB attenuates signals to a certain degree, as illustrated in the filter response plots in the [Digital Filter](#) section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; see [Figure 43](#). The cutoff frequency of this filter is approximately 40 MHz and helps reject high-frequency interference.

### 10.1.3 External Reference and Ratiometric Measurements

The full-scale range of the ADS114S0xB is defined by the reference voltage and the PGA gain ( $\text{FSR} = \pm V_{\text{REF}} / \text{Gain}$ ). An external reference can be used instead of the integrated 2.5-V reference to adapt the FSR to the specific system needs. An external reference must be used if  $V_{\text{IN}} > 2.5$  V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement, the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. Because current noise and drift are common to both the sensor measurement and the reference, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

The example in the [Typical Application](#) section describes a system that uses a ratiometric measurement. One excitation current source is used to drive a reference resistor and an RTD. The ADC measurement represents a ratiometric measurement between the RTD value and a known reference resistor value.

### 10.1.4 Establishing a Proper Input Voltage

The ADS114S0xB can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully-differential signals (which can be either unipolar or bipolar). However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground ( $V_{\text{AINN}} = 0$  V) are commonly called *single-ended signals*. The input voltage of a single-ended signal consequently varies between 0 V and  $V_{\text{IN}}$ . If the PGA is disabled and bypassed, the input voltage of the ADS114S0xB can be as low as 50 mV below AVSS and as large as 50 mV above AVDD. Therefore, set the PGA\_EN bits to 10 in the gain setting register (03h) to measure single-ended signals when a unipolar analog supply is used ( $\text{AVSS} = 0$  V). Only a gain of 1 is possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100  $\Omega$  referenced to GND is a typical example. The ADS114S0xB can directly measure the signal across the load resistor using a unipolar supply, the internal 2.5-V reference, and gain = 1 when the PGA is bypassed.

If gain is needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS114S0xB to meet the input voltage requirement of the PGA. Signals where the negative analog input ( $\text{AIN}_N$ ) is fixed at a voltage other than 0 V are referred to as *pseudo-differential signals*. The input voltage of a pseudo-differential signal varies between  $V_{\text{AINN}}$  and  $V_{\text{AINN}} + V_{\text{IN}}$ .

## Application Information (continued)

Fully-differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

The ADS114S0xB can measure pseudo-differential and fully-differential signals both with the PGA enabled or bypassed. However, the PGA must be enabled in order to measure any input with a gain greater than 1. The input voltage must meet the input and output voltage restrictions of the PGA, as explained in the [PGA Input-Voltage Requirements](#) section when the PGA is enabled. Setting the input voltage at or near  $(AVSS + AVDD) / 2$  in most cases satisfies the PGA input voltage requirements.

Signals where both the positive and negative inputs are always  $\geq 0$  V are called *unipolar signals*. These signals can in general be measured with the ADS114S0xB using a unipolar analog supply ( $AVSS = 0$  V). As mentioned previously, the PGA must be bypassed in order to measure single-ended, unipolar signals when using a unipolar supply.

A signal is called *bipolar* when either the positive or negative input can swing below 0 V. A bipolar analog supply (such as  $AVDD = 2.5$  V,  $AVSS = -2.5$  V) is required in order to measure bipolar signals with the ADS114S0xB. A typical application task is measuring a single-ended, bipolar,  $\pm 10$ -V signal where  $AIN_N$  is fixed at 0 V and  $AIN_P$  swings between  $-10$  V and 10 V. The ADS114S0xB cannot directly measure this signal because the 10-V signal exceeds the analog power-supply limits. However, one possible solution is to use a bipolar analog supply ( $AVDD = 2.5$  V,  $AVSS = -2.5$  V), gain = 1, and a resistor divider in front of the ADS114S0xB. The resistor divider must divide the voltage down to  $\leq \pm 2.5$  V to be able to measure the voltage using the internal 2.5-V reference.

### 10.1.5 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog and reference inputs floating, or connect the inputs to mid-supply or to AVDD. Connecting unused analog or reference inputs to AVSS is possible as well, but can yield higher leakage currents than the previously mentioned options. REFNO is an exception; leave the REFNO pin floating when not in use or tie the pin to AVSS.

GPIO pins operate on levels based on the analog supply. Do not float GPIO pins that are configured as digital inputs. Tie unused GPIO pins that are configured as digital inputs to the appropriate levels, AVDD or AVSS, including when in power-down mode. Tie unused GPIO output pins to AVSS through a pulldown resistor and set the output to 0 in the GPIO data register. For unused GPIO pins on the ADS114S06B, leave the GPIOCON register set to the default register values and connect these GPIO pins in the same manner as for an unused analog input.

Do not float unused digital inputs; excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, IOVDD or DGND, even when in power-down mode. Connections for unused digital inputs are listed below.

- Tie the  $\overline{CS}$  pin to DGND if  $\overline{CS}$  is not used
- Tie the CLK pin to DGND if the internal oscillator is used
- Tie the START/SYNC pin to DGND to control conversions by commands
- Tie the  $\overline{RESET}$  pin to IOVDD if the  $\overline{RESET}$  pin is not used
- If the  $\overline{DRDY}$  output is not used, leave the  $\overline{DRDY}$  pin unconnected or tie the  $\overline{DRDY}$  pin to IOVDD using a weak pullup resistor

## Application Information (continued)

### 10.1.6 Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS114S0xB in continuous conversion mode. The dedicated DRDY pin is used to indicate availability of new conversion data.

```

Power-up so that all supplies reach minimum operating levels;
Delay for a minimum of 2.2 ms to allow power supplies to settle and power-up reset to complete;

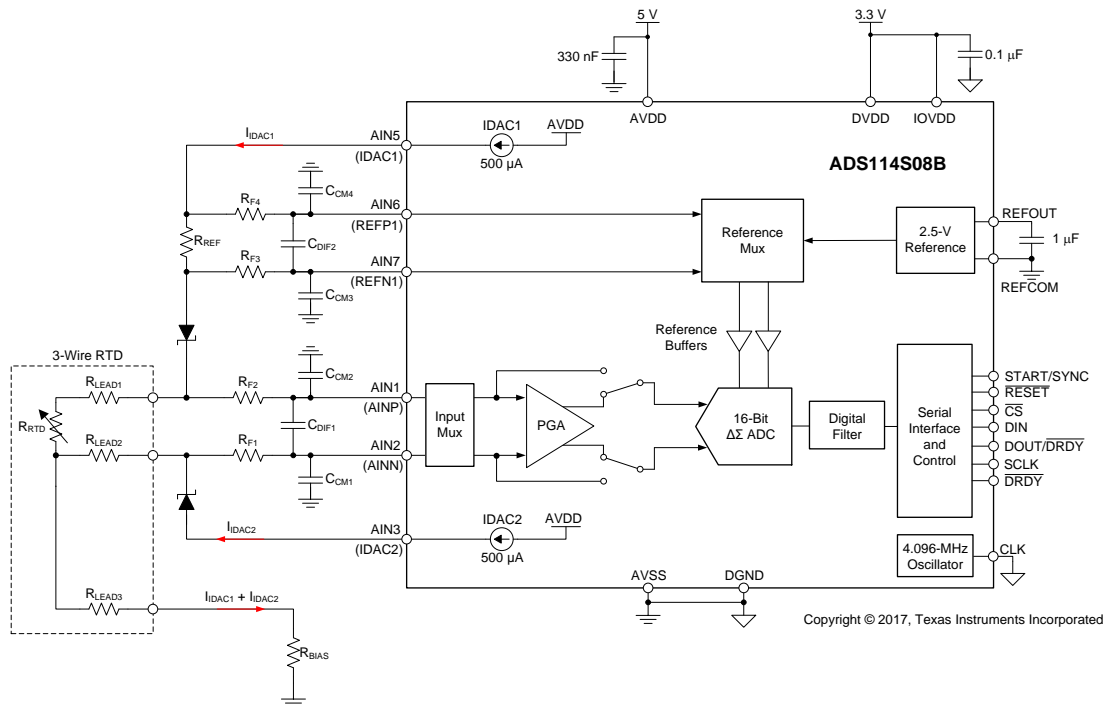
Configure the SPI interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA =1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an
output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;

Set CS to the device low;
Delay for a minimum of  $t_{d(CSSC)}$ ;
Send the RESET command (06h) to make sure the device is properly reset after power-up; //Optional
Delay for a minimum of  $4096 \cdot t_{CLK}$ ;
Read the status register using the RREG command to check that the RDY bit is 0; //Optional
Clear the FL_POR flag by writing 00h to the status register; //Optional
Write the respective register configuration with the WREG command;
For verification, read back all configuration registers with the RREG command;
Send the START command (08h) to start converting in continuous conversion mode;
Delay for a minimum of  $t_{d(SCCS)}$ ;
Clear CS to high (resets the serial interface);
Loop
{
  Wait for DRDY to transition low;
  Take CS low;
  Delay for a minimum of  $t_{d(CSSC)}$ ;
  Send the RDATA command;
  Send 16 SCLK rising edges to read out conversion data on DOUT/DRDY;
  Delay for a minimum of  $t_{d(SCCS)}$ ;
  Clear CS to high;
}
Take CS low;
Delay for a minimum of  $t_{d(CSSC)}$ ;
Send the STOP command (0Ah) to stop conversions and put the device in standby mode;
Delay for a minimum of  $t_{d(SCCS)}$ ;
Clear CS to high;

```

## 10.2 Typical Application

Figure 96 shows a fault-protected, filtered, 3-wire RTD application circuit with hardware-based, lead-wire compensation. Two IDAC current sources provide the lead-wire compensation. One IDAC current source (IDAC1) provides excitation to the RTD element. The ADC reference voltage (pins AIN6 and AIN7) is derived from the voltage across resistor  $R_{REF}$  sourcing the same IDAC1 current, providing ratiometric cancellation of current-source drift. The other current source (IDAC2) has the same current setting, providing cancellation of lead-wire resistance by generating a voltage drop across lead-wire resistance  $R_{LEAD2}$  equal to the voltage drop of  $R_{LEAD1}$ . Because the  $R_{RTD}$  voltage is measured differentially at ADC pins AIN1 and AIN2, the voltages across the lead wire resistance cancel. Resistor  $R_{BIAS}$  level-shifts the RTD signal to within the ADC specified input range. The current sources are provided by two additional pins (AIN5 and AIN3) that connect to the RTD through blocking diodes. The additional pins are used to route the RTD excitation currents around the input filter resistors, avoiding the voltage drop otherwise caused by the filter resistors  $R_{F1}$  and  $R_{F4}$ . The diodes protect the ADC inputs in the event of a miswired connection. The input filter resistors limit the input fault currents flowing into the ADC.



**Figure 96. 3-Wire RTD Application**

### 10.2.1 Design Requirements

Table 34 shows the design requirements of the 3-wire RTD application.

**Table 34. Design Requirements**

| DESIGN PARAMETER          | VALUE                       |
|---------------------------|-----------------------------|
| ADC supply voltage        | 4.75 V (minimum)            |
| RTD sensor type           | 3-wire Pt100                |
| RTD resistance range      | 20 $\Omega$ to 400 $\Omega$ |
| RTD lead resistance range | 0 $\Omega$ to 10 $\Omega$   |
| RTD self heating          | 1 mW                        |
| Accuracy <sup>(1)</sup>   | $\pm 0.1 \Omega$            |

(1)  $T_A = 25^\circ\text{C}$ . After offset and full-scale calibration.



## 10.2.2 Detailed Design Procedure

The key considerations in the design of a 3-wire RTD circuit are the accuracy, the lead wire compensation, and the sensor self-heating. As the design values of [Table 35](#) show, several values of excitation currents are available. The resolution is expressed in units of noise-free resolution (NFR). Noise-free resolution is resolution with no code flicker. The selection of excitation currents trades off resolution against sensor self-heating. In general, measurement resolution improves with increasing excitation current. Increasing the excitation current beyond 1000  $\mu\text{A}$  results in no further improvement in resolution for this example circuit. The design procedure is based on a 500- $\mu\text{A}$  excitation current, because this level of current results in very low sensor self-heating (0.4 mW).

**Table 35. RTD Circuit Design Parameters**

| I <sub>IDAC</sub> ( $\mu\text{A}$ ) | NFR (bits) | P <sub>RTD</sub> (mW) | V <sub>RTD</sub> (V) | Gain (V/V) | V <sub>REFMIN</sub> <sup>(1)</sup> (V) | V <sub>REF</sub> <sup>(2)</sup> (V) | R <sub>REF</sub> (k $\Omega$ ) | V <sub>AINNLM</sub> <sup>(3)</sup> (V) | V <sub>AINPLM</sub> <sup>(4)</sup> (V) | R <sub>BIAS</sub> (k $\Omega$ ) | V <sub>RTDN</sub> <sup>(5)</sup> (V) | V <sub>RTDP</sub> <sup>(6)</sup> (V) | V <sub>IDAC1</sub> <sup>(7)</sup> (V) |
|-------------------------------------|------------|-----------------------|----------------------|------------|--|-------------------------------------|--------------------------------|--|--|---------------------------------|--------------------------------------|--------------------------------------|---------------------------------------|
| 50                                  | 16.8       | 0.001                 | 0.02                 | 32         | 0.64                                   | 0.70                                | 18                             | 0.6                                    | 4.1                                    | 7.10                            | 0.7                                  | 0.7                                  | 1.9                                   |
| 100                                 | 17.8       | 0.004                 | 0.04                 | 32         | 1.28                                   | 1.41                                | 14.1                           | 0.9                                    | 3.8                                    | 5.10                            | 1.0                                  | 1.1                                  | 2.8                                   |
| 250                                 | 18.8       | 0.025                 | 0.10                 | 16         | 1.60                                   | 1.76                                | 7.04                           | 1.1                                    | 3.7                                    | 2.30                            | 1.2                                  | 1.3                                  | 3.3                                   |
| 500                                 | 19.1       | 0.100                 | 0.20                 | 8          | 1.60                                   | 1.76                                | 3.52                           | 1.0                                    | 3.8                                    | 1.10                            | 1.1                                  | 1.3                                  | 3.4                                   |
| 750                                 | 18.9       | 0.225                 | 0.30                 | 4          | 1.20                                   | 1.32                                | 1.76                           | 0.8                                    | 4.0                                    | 0.57                            | 0.9                                  | 1.2                                  | 2.8                                   |
| 1000                                | 19.3       | 0.400                 | 0.40                 | 4          | 1.60                                   | 1.76                                | 1.76                           | 0.9                                    | 3.9                                    | 0.50                            | 1.0                                  | 1.4                                  | 3.5                                   |
| 1500                                | 19.1       | 0.900                 | 0.60                 | 2          | 1.20                                   | 1.32                                | 0.88                           | 0.6                                    | 4.2                                    | 0.23                            | 0.7                                  | 1.3                                  | 3.0                                   |
| 2000                                | 18.3       | 1.600                 | 0.80                 | 1          | 0.80                                   | 0.90                                | 0.45                           | 0.3                                    | 4.5                                    | 0.10                            | 0.4                                  | 1.2                                  | 2.4                                   |

- (1) V<sub>REFMIN</sub> is the minimum reference voltage required by the design.
- (2) V<sub>REF</sub> is the design target reference voltage allowing for 10% overrange.
- (3) V<sub>AINNLM</sub> is the absolute minimum input voltage required by the ADC.
- (4) V<sub>AINPLM</sub> is the absolute maximum input voltage required by the ADC.
- (5) V<sub>RTDN</sub> is the design target negative input voltage.
- (6) V<sub>RTDP</sub> is the design target positive input voltage.
- (7) V<sub>IDAC1</sub> is the design target IDAC1 loop voltage.

Initially, R<sub>LEAD1</sub> and R<sub>LEAD2</sub> are considered to be 0  $\Omega$ . Route the IDAC1 current through the external reference resistor, R<sub>REF</sub>. IDAC1 generates the ADC reference voltage, V<sub>REF</sub>, across the reference resistor. This voltage is defined by [Equation 12](#):

$$V_{REF} = I_{IDAC1} \cdot R_{REF} \quad (12)$$

Route the second current (IDAC2) to the second RTD lead.

Program the IDAC value by using the IDACMAG register; however, only the IDAC1 current flows through the reference resistor and RTD. The IDAC1 current excites the RTD to produce a voltage proportional to the RTD resistance. The RTD voltage is defined by [Equation 13](#):

$$V_{RTD} = R_{RTD} \cdot I_{IDAC1} \quad (13)$$

The ADC amplifies the RTD signal voltage (V<sub>RTD</sub>) and measures the resulting voltage against the reference voltage to produce a proportional digital output code, as shown in [Equation 14](#) through [Equation 16](#).

$$\text{Code} \propto V_{RTD} \cdot \text{Gain} / V_{REF} \quad (14)$$

$$\text{Code} \propto (R_{RTD} \cdot I_{IDAC1}) \cdot \text{Gain} / (I_{IDAC1} \cdot R_{REF}) \quad (15)$$

$$\text{Code} \propto (R_{RTD} \cdot \text{Gain}) / R_{REF} \quad (16)$$

As shown in [Equation 16](#), the RTD measurement depends on the value of the RTD, the PGA gain, and the reference resistor R<sub>REF</sub>, but not on the IDAC1 value. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter.

The second excitation current (IDAC2) provides a second voltage drop across the second RTD lead resistance, R<sub>LEAD2</sub>. The second voltage drop compensates the voltage drop caused by I<sub>IDAC1</sub> and R<sub>LEAD1</sub>. The leads of a 3-wire RTD typically have the same length; therefore, the lead resistance is typically identical. Taking the lead resistance into account (R<sub>LEADx</sub>  $\neq$  0), the differential voltage (V<sub>IN</sub>) across ADC inputs AIN8 and AIN9 is shown in [Equation 17](#):

$$V_{IN} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \quad (17)$$

If R<sub>LEAD1</sub> = R<sub>LEAD2</sub> and I<sub>IDAC1</sub> = I<sub>IDAC2</sub>, the expression for V<sub>IN</sub> reduces to [Equation 18](#):

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \quad (18)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated as long as the lead resistance values and the IDAC values are matched.

Using [Equation 13](#), the value of RTD resistance (400 Ω, maximum) and the excitation current (500 μA) yields an RTD voltage of  $V_{RTD} = 500 \mu\text{A} \cdot 400 \Omega = 0.2 \text{ V}$ . Use the maximum gain of 8 in order to limit the corresponding loop voltage of IDAC1. Gain = 8 requires a minimum reference voltage  $V_{REFMIN} = 0.2 \text{ V} \cdot 8 = 1.6 \text{ V}$ . To provide margin for the ADC operating range, increase the target reference voltage by 10% ( $V_{REF} = 1.6 \text{ V} \cdot 1.1 = 1.76 \text{ V}$ ). Calculate the value of the reference resistor, as shown in [Equation 19](#):

$$R_{REF} = V_{REF} / I_{IDAC1} = 1.76 \text{ V} / 500 \mu\text{A} = 3.52 \text{ k}\Omega \quad (19)$$

For this example application, 3.5 kΩ is chosen for  $R_{REF}$ . For best results, use a precision reference resistor  $R_{REF}$  with a low temperature drift (< 10 ppm/°C). Any change in  $R_{REF}$  is reflected in the measurement as a gain error.

The next step in the design is determining the value of the  $R_{BIAS}$  resistor, in order to level shift the RTD voltage to meet the ADC absolute input-voltage specification. The required level-shift voltage is determined by calculating the minimum absolute voltage ( $V_{AINNLIM}$ ) as shown in [Equation 20](#):

$$AVSS + 0.15 + V_{RTDMAX} \cdot (\text{Gain} - 1) / 2 \leq V_{AINNLIM}$$

where

- $V_{RTDMAX}$  = maximum differential RTD voltage = 0.2 V
  - Gain = 8
  - AVSS = 0 V
- (20)

The result of the equation requires a minimum absolute input voltage ( $V_{RTDN}$ ) > 0.85 V. Therefore, the RTD voltage must be level shifted by a minimum of 0.85 V. To meet this requirement, a target level-shift value of 1 V is chosen to provide extra margin. Calculate the value of  $R_{BIAS}$  as shown in [Equation 21](#):

$$R_{BIAS} = V_{AINN} / (I_{IDAC1} + I_{IDAC2}) = 1 \text{ V} / (2 \cdot 500 \mu\text{A}) = 1 \text{ k}\Omega \quad (21)$$

After the level-shift voltage is determined, verify that the positive RTD voltage ( $V_{RTDP}$ ) is less than the maximum absolute input voltage ( $V_{AINPLIM}$ ), as shown in [Equation 22](#):

$$V_{AINPLIM} \leq AVDD - 0.15 - V_{RTDMAX} \cdot (\text{Gain} - 1) / 2$$

where

- $V_{RTDMAX}$  = maximum differential RTD voltage = 0.2 V
  - Gain = 8
  - AVDD = 4.75 V (minimum)
- (22)

Solving [Equation 22](#) results in a required  $V_{RTDP}$  of less than 3.9 V. Calculate the  $V_{RTDP}$  input voltage by [Equation 23](#):

$$V_{AINP} = V_{RTDN} + I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) = 1 \text{ V} + 500 \mu\text{A} \cdot (400 \Omega + 10 \Omega) = 1.2 \text{ V} \quad (23)$$

Because 1.2 V is less than the 3.9-V maximum input voltage limit, the absolute positive and negative RTD voltages are within the ADC specified input range.

The next step in the design is to verify that the IDACs have enough voltage headroom (compliance voltage) to operate. The loop voltage of the excitation current must be less than the supply voltage minus the specified IDAC compliance voltage. Calculate the voltage drop developed across each IDAC current path to AVSS. In this circuit, IDAC1 has the largest voltage drop developed across its current path. The IDAC1 calculation is sufficient to satisfy IDAC2 because the IDAC2 voltage drop is always less than IDAC1 voltage drop. The sum of voltages in the IDAC1 loop is shown in [Equation 24](#):

$$V_{IDAC1} = [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{BIAS})] + [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1} + R_{REF})] + V_D$$

where

- $V_D$  = external blocking diode voltage
- (24)

The equation results in a loop voltage of  $V_{IDAC1} = 3.0 \text{ V}$ . The worst-case current source compliance voltage is:  $(AVDD - 0.4 \text{ V}) = (4.75 \text{ V} - 0.4 \text{ V}) = 4.35 \text{ V}$ . The  $V_{IDAC1}$  loop voltage is less than the specified current source compliance voltage ( $3.0 \text{ V} < 4.35 \text{ V}$ ).

Many applications benefit from using an analog filter at the inputs to remove noise and interference from the signal. Filter components are placed on the ADC inputs ( $R_{F1}$ ,  $R_{F2}$ ,  $C_{DIF1}$ ,  $C_{CM1}$ , and  $C_{CM2}$ ), as well as on the reference inputs ( $R_{F3}$ ,  $R_{F4}$ ,  $C_{DIF2}$ ,  $C_{CM3}$ , and  $C_{CM4}$ ). The filters remove both differential and common-mode noise. The application shows a differential input noise filter formed by  $R_{F1}$ ,  $R_{F2}$  and  $C_{DIF1}$ , with additional differential mode capacitance provided by the common-mode filter capacitors,  $C_{CM1}$  and  $C_{CM2}$ . Calculate the differential –3-dB cutoff frequency as shown in [Equation 25](#):

$$f_{DIF} = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot (C_{DIF1} + C_{CM1} || C_{CM2})] \quad (25)$$

The common-mode noise filter is formed by components  $R_{F1}$ ,  $R_{F2}$ ,  $C_{CM1}$ , and  $C_{CM2}$ . Calculate the common-mode signal –3-dB cutoff frequency, as shown in [Equation 26](#):

$$f_{CM} = 1 / (2\pi \cdot R_{F1} \cdot C_{CM1}) = 1 / (2\pi \cdot R_{F2} \cdot C_{CM2}) \quad (26)$$

Mismatches in the common-mode filter components convert common-mode noise into differential noise. To reduce the effect of mismatch, use a differential mode filter with a corner frequency that is at least 10 times lower than the common-mode filter corner frequency. The low-frequency differential filter removes the common-mode converted noise. The filter resistors ( $R_{Fx}$ ) also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AINx) of the device to safe levels when an overvoltage occurs on the inputs.

Filter resistors lead to an offset voltage error due to the dc input current leakage flowing into and out of the device. Remove this voltage error by system offset calibration. Resistor values that are too large generate excess thermal noise and degrade the overall noise performance. The recommended range of the filter resistor values is 100  $\Omega$  to 10 k $\Omega$ . The properties of the capacitors are important because the capacitors are connected to the signal; use high-quality COG ceramics or film-type capacitors.

For consistent noise performance across the full range of RTD measurements, match the corner frequencies of the input and reference filter. See the [RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Application Report](#) for detailed information on matching the input and reference filter.

### 10.2.2.1 Register Settings

The register settings for this design are shown in [Table 36](#).

**Table 36. Register Settings**

| REGISTER | NAME                  | SETTING | DESCRIPTION  |
|----------|-----------------------|---------|--|
| 02h      | INPMUX                | 12h     | Select $AIN_P = AIN1$ and $AIN_N = AIN2$   |
| 03h      | PGA                   | 0Bh     | PGA enabled, PGA Gain = 8  |
| 04h      | DATARATE              | 14h     | Continuous conversion mode, 20-SPS data rate   |
| 05h      | REF                   | 06h     | Positive and negative reference buffers enabled, REFP1 and REFN1 reference inputs selected, internal reference always on |
| 06h      | IDACMAG               | 05h     | IDAC magnitude set to 500 $\mu$ A  |
| 07h      | IDACMUX               | 35h     | IDAC2 set to AIN3, IDAC1 set to AIN5   |
| 08h      | VBIAS                 | 00h     |  |
| 09h      | SYS                   | 10h     |  |
| 0Ah      | OFCAL0 <sup>(1)</sup> | xxh     |  |
| 0Bh      | OFCAL1                | xxh     |  |
| 0Ch      | OFCAL2                | xxh     |  |
| 0Dh      | FSCAL0 <sup>(1)</sup> | xxh     |  |
| 0Eh      | FSCAL1                | xxh     |  |
| 0Fh      | FSCAL2                | xxh     |  |
| 10h      | GPIODAT               | 00h     |  |
| 11h      | GPIOCON               | 00h     |  |

(1) A two-point offset and gain calibration removes errors from the  $R_{REF}$  tolerance. The results are used for the OFC and FSC registers.

### 10.2.3 Application Curves

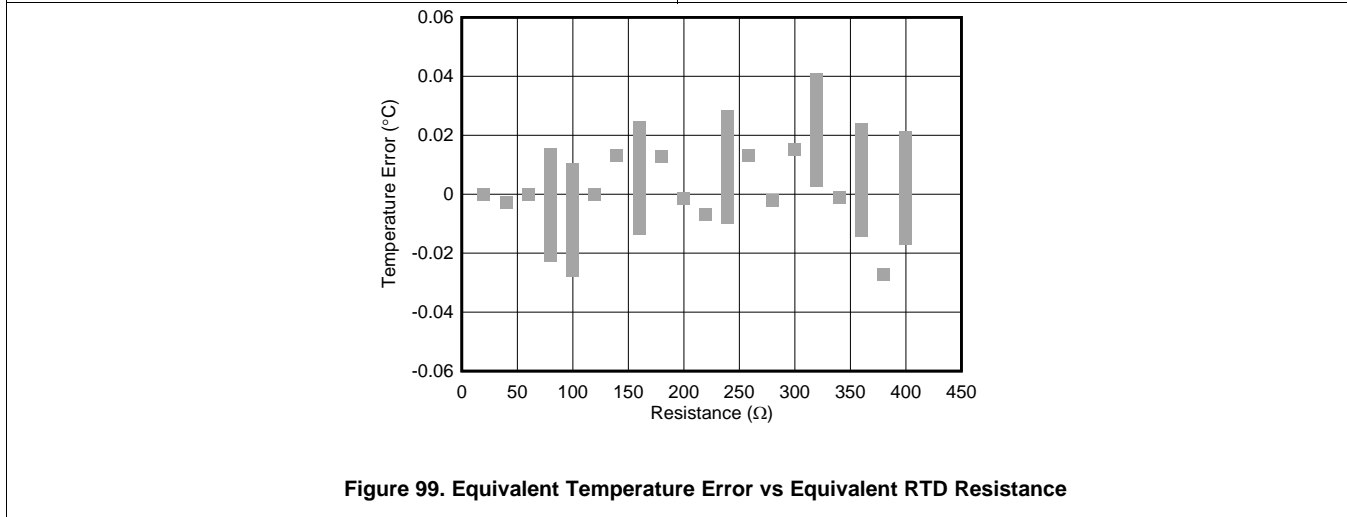
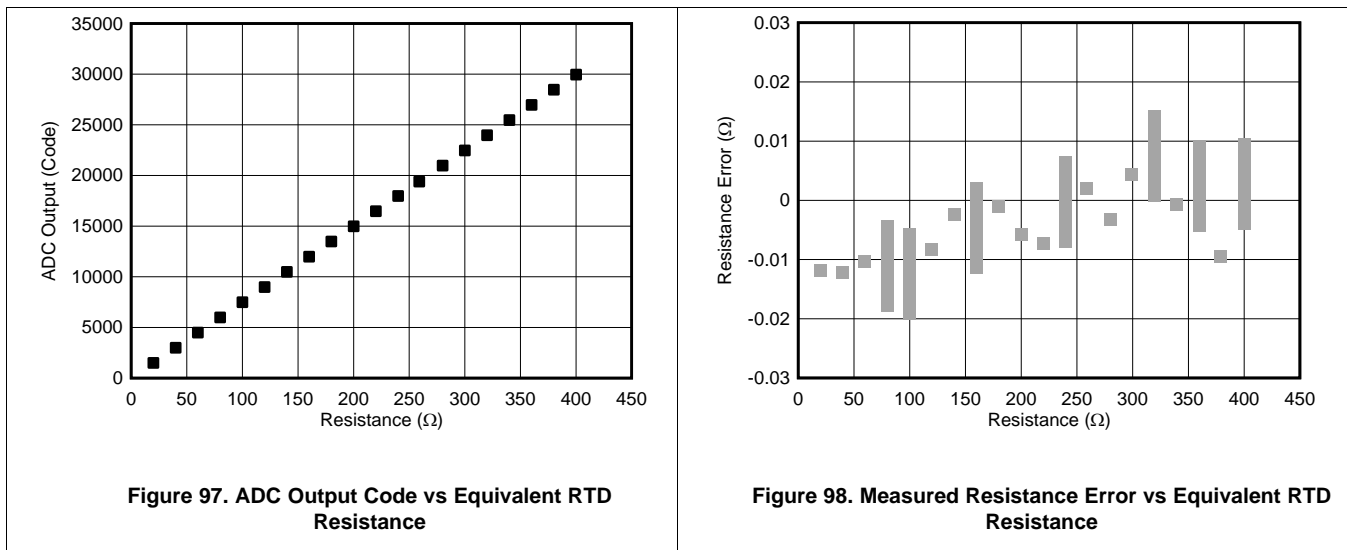
To test the accuracy of the acquisition circuit, a series of calibrated high-precision discrete resistors are used as an input to the system. Measurements are taken at  $T_A = 25^\circ\text{C}$ . Figure 97 displays the resistance measurement over an input span from  $20\ \Omega$  to  $400\ \Omega$ . Any offset error is generally attributed to the offset of the ADC, and the gain error can be attributed to the accuracy of the  $R_{REF}$  resistor and the ADC. The  $R_{REF}$  value is also calibrated to reduce the gain error contribution.

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors that generally dominate the total system error. The simplest calibration method is a linear, or two-point calibration that applies an equal and opposite gain and offset term to cancel the measured system gain and offset error. In this particular tested application, the gain and offset error was very small, and did not require additional calibration other than the self offset and gain calibration provided by the device. The resulting measured resistance error is shown in Figure 98.

The results in Figure 98 are converted to temperature accuracy by dividing the results by the RTD sensitivity ( $\alpha$ ) at the measured resistance. Over the full resistance input range, the maximum total measured error is  $\pm 0.0190\ \Omega$ . Equation 27 uses the measured resistance error and the RTD sensitivity at  $0^\circ\text{C}$  to calculate the measured temperature accuracy.

$$\text{Error } (^\circ\text{C}) = \text{Error } (\Omega) / \alpha_{@0^\circ\text{C}} = \pm 0.0190\ \Omega / 0.39083\ \Omega / ^\circ\text{C} = \pm 0.049^\circ\text{C} \tag{27}$$

Figure 99 displays the calculated temperature accuracy of the circuit assuming a linear RTD resistance to temperature response. This figure does not include any linearity compensation of the RTD, but Figure 99 does remove offset and gain error, which can be calibrated with the OFC and FSC registers.



### 10.3 Do's and Don'ts

- Do partition the analog, digital, and power-supply circuitry into separate sections on the PCB.
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified PGA input voltage range under all input conditions.
- Do float unused analog input pins to minimize input leakage current on all other analog inputs. Connecting unused pins to AVDD is the next best option.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout linear regulator (LDO) to reduce ripple voltage generated by switch-mode power supplies. Reducing ripple is especially important for AVDD where the supply noise can affect the performance.
- Don't cross analog and digital signals.
- Don't allow the analog and digital power supply voltages to exceed 5.5 V under any condition, including during power-up and power-down.

Do's and Don'ts (continued)

Figure 100 shows the do's and don'ts of the ADC circuit connections.

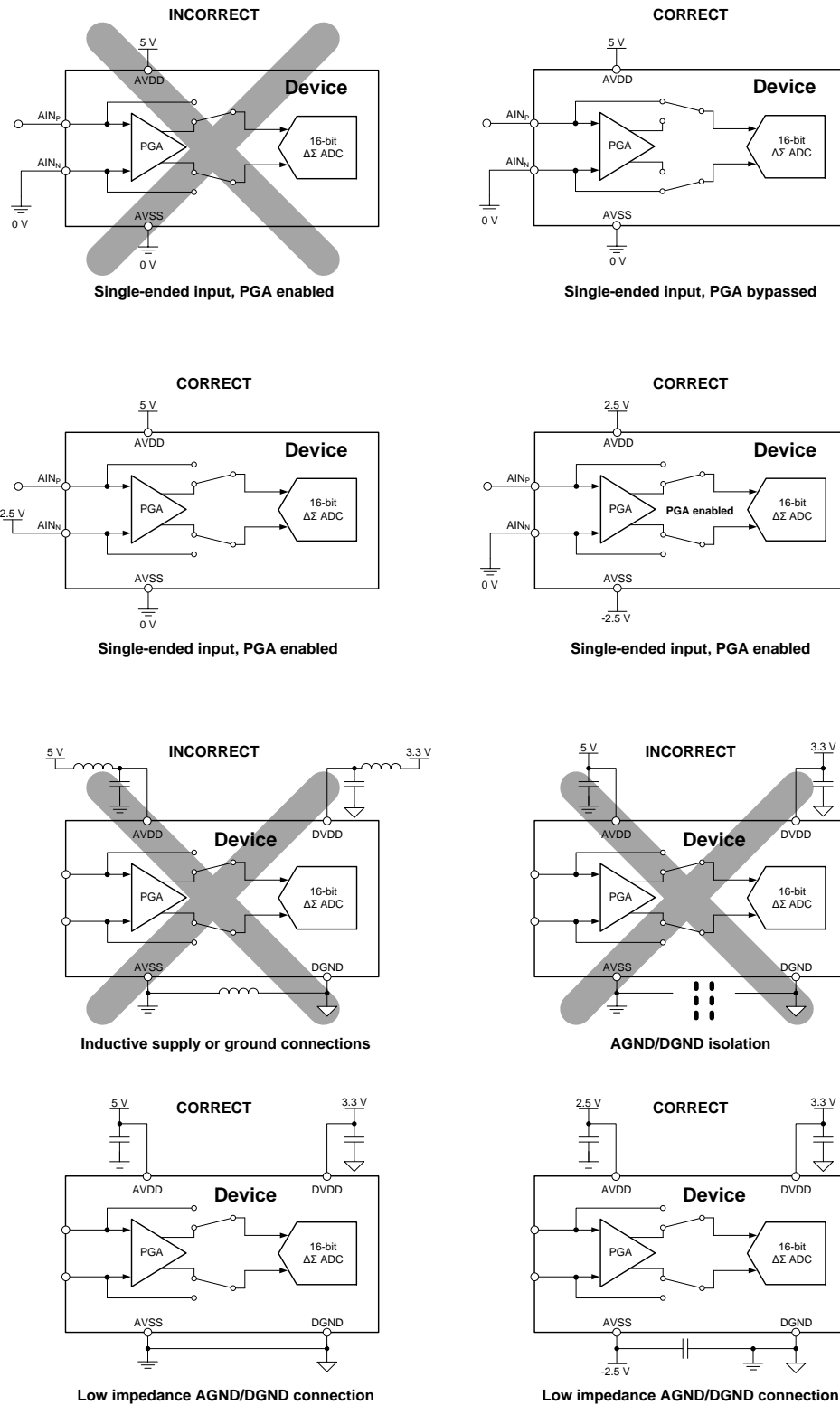


Figure 100. Do's and Don'ts Circuit Connections

## 11 Power Supply Recommendations

### 11.1 Power Supplies

The ADS114S0xB require three power supplies: analog (AVDD, AVSS), digital core (DVDD, DGND), and digital I/O (IOVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = -2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supplies. DVDD is used to power the digital circuits of the devices. IOVDD sets the digital I/O levels (with the exception of the GPIO levels that are set by the analog supply of AVDD and AVSS). IOVDD must be equal to or larger than DVDD.

### 11.2 Power-Supply Sequencing

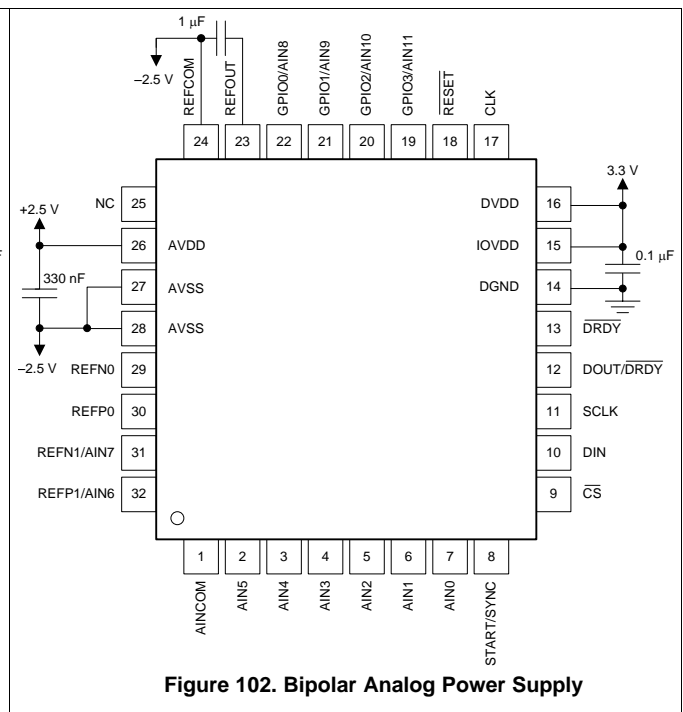
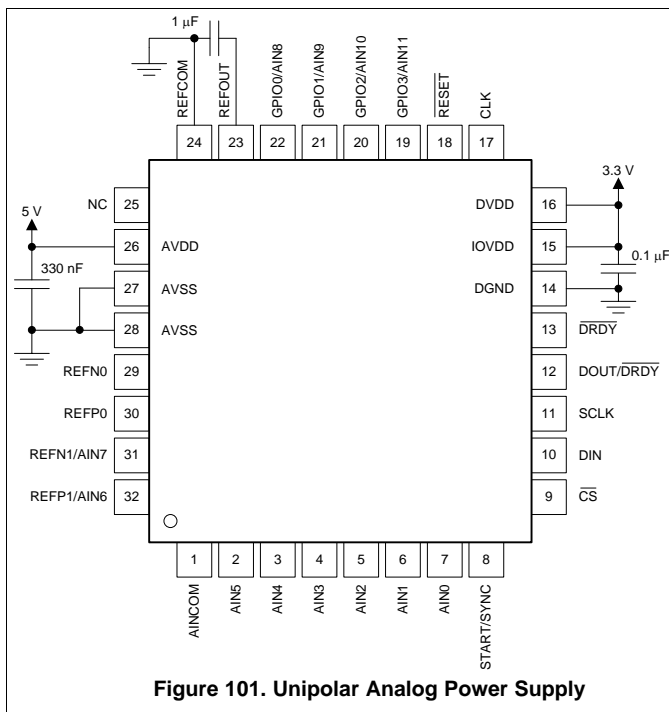
AVDD and DVDD may be powered up in any order. However, IOVDD is recommended to be powered up before or at the same time as DVDD. If DVDD comes up before IOVDD, a reset of the device using the  $\overline{\text{RESET}}$  pin or the RESET command may be required.

### 11.3 Power-On Reset

An internal POR is released after all three supplies exceed approximately 1.65 V. Each supply has an individual POR circuit. A brownout condition on any of the three supplies triggers a reset of the complete device.

### 11.4 Power-Supply Decoupling

Good power-supply decoupling is important to achieve best performance. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1- $\mu\text{F}$  capacitor to DGND. Figure 101 and Figure 102 show typical power-supply decoupling examples for unipolar and bipolar analog supplies, respectively. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. Use multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. To reduce inductance on the supply pins, avoid the use of vias for connecting the capacitors to the supply pins. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital grounds together as close to the device as possible.

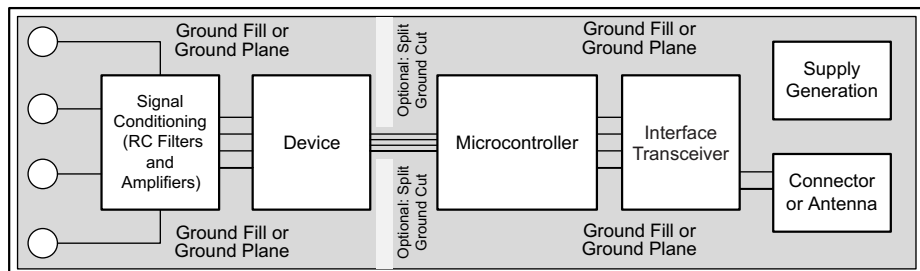




## 12 Layout

### 12.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in [Figure 103](#). Although [Figure 103](#) provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.



**Figure 103. System Component Placement**

The following basic recommendations for layout of the ADS114S0xB help achieve the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but this (splitting) is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents will flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as AIN0, AIN1 and AIN2, AIN3). The differential capacitors must be of high quality. The best ceramic chip capacitors are COG (NPO) that have stable properties and low noise characteristics.



## 12.2 Layout Example

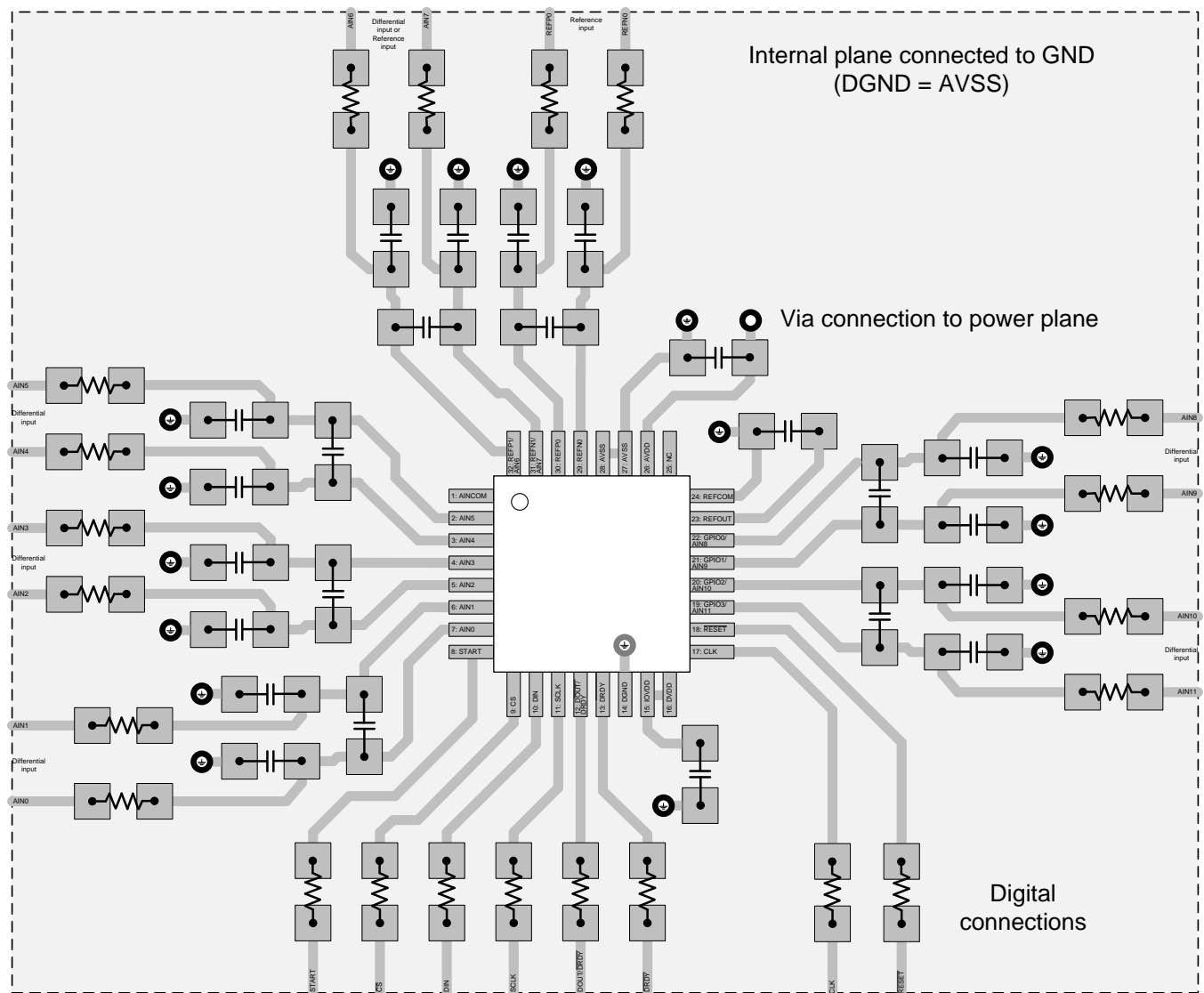


Figure 104. ADS114S0xB Layout Example

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 Development Support

[ADS1x4S0x Design Calculator](#)

### 13.2 Documentation Support

#### 13.2.1 Related Documentation

For related documentation see the following:

- [ADS114S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 16-Bit, Delta-Sigma ADC with PGA and Voltage Reference](#)
- [ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference](#)
- [REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference](#)
- [RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Application Report](#)
- [3-Wire RTD Measurement System Reference Design, -200°C to 850°C](#)

### 13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 37. Related Links**

| PARTS      | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ADS114S06B | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ADS114S08B | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.6 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADS114S06BIPBS   | ACTIVE        | TQFP         | PBS             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | 114S06B                 | <a href="#">Samples</a> |
| ADS114S06BIPBSR  | ACTIVE        | TQFP         | PBS             | 32   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | 114S06B                 | <a href="#">Samples</a> |
| ADS114S06BIRHBR  | ACTIVE        | VQFN         | RHB             | 32   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | ADS<br>114S06B          | <a href="#">Samples</a> |
| ADS114S06BIRHBT  | ACTIVE        | VQFN         | RHB             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | ADS<br>114S06B          | <a href="#">Samples</a> |
| ADS114S08BIPBS   | ACTIVE        | TQFP         | PBS             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | 114S08B                 | <a href="#">Samples</a> |
| ADS114S08BIPBSR  | ACTIVE        | TQFP         | PBS             | 32   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | 114S08B                 | <a href="#">Samples</a> |
| ADS114S08BIRHBR  | ACTIVE        | VQFN         | RHB             | 32   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | ADS<br>114S08B          | <a href="#">Samples</a> |
| ADS114S08BIRHBT  | ACTIVE        | VQFN         | RHB             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 125   | ADS<br>114S08B          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

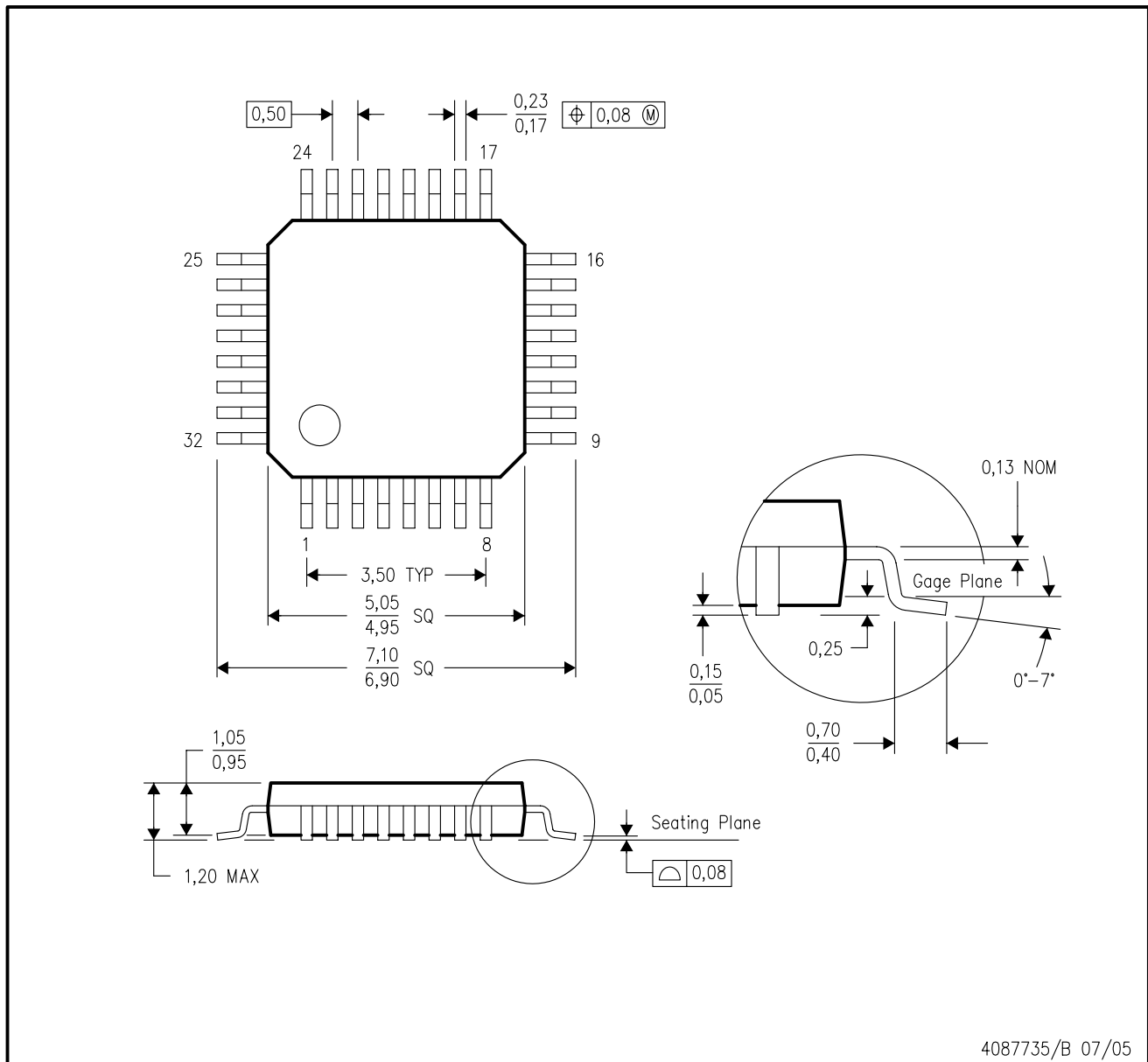
<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PBS (S-PQFP-G32)

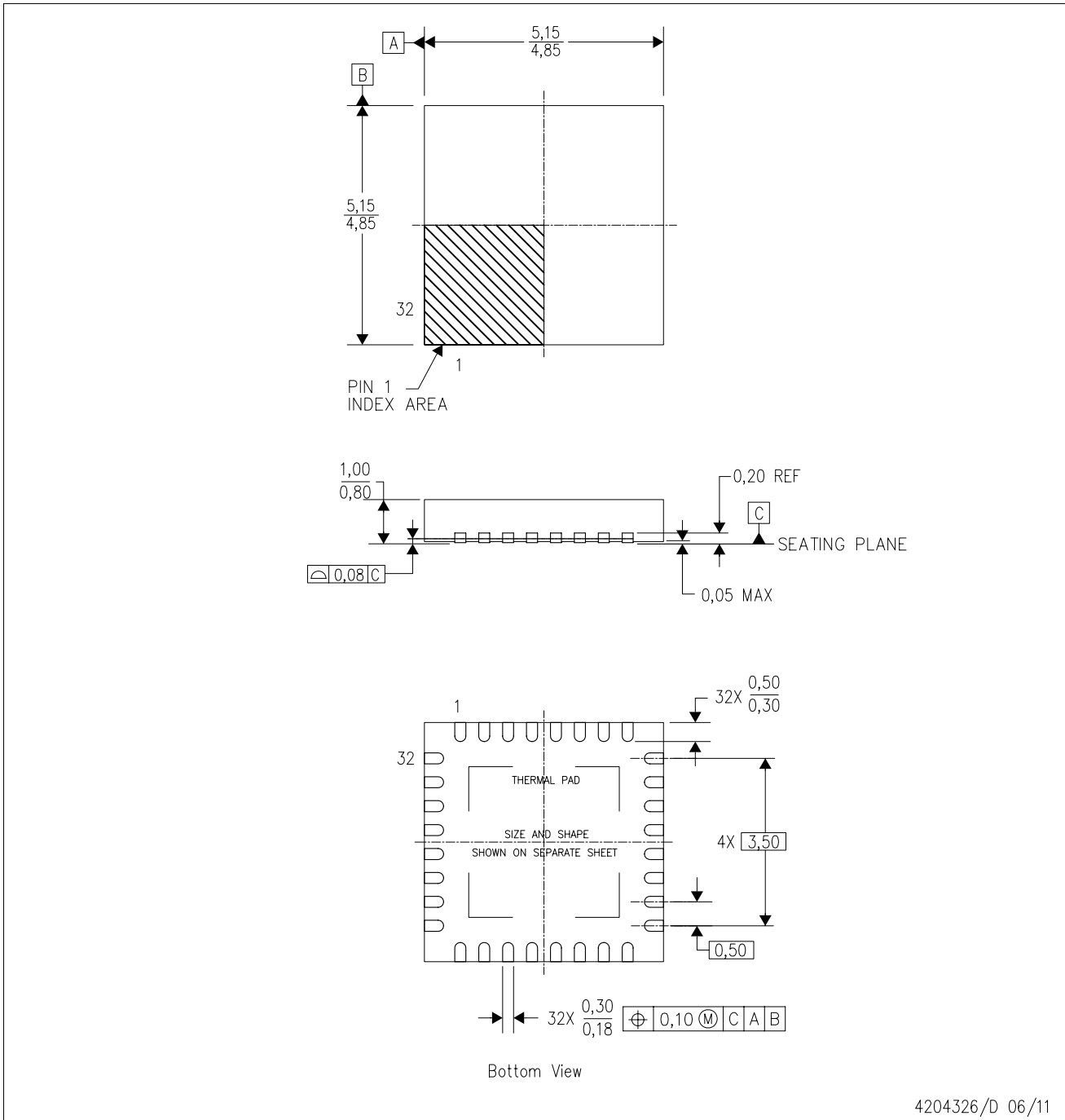
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

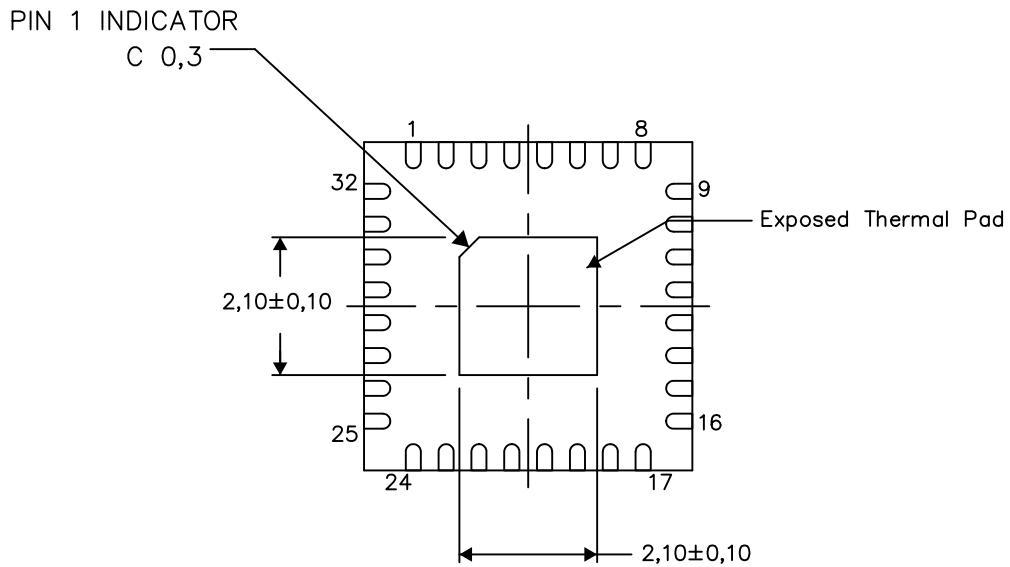
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356-5/AC 05/15

NOTE: A. All linear dimensions are in millimeters



## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.