16-Bit, High-Speed, 2.7V to 5.5V *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS8317

FEATURES

- **16 Bits No Missing Codes (Full-Supply Range, High or Low Grade)**
- **Very Low Noise: 5LSB$_{PP}$**
- **Excellent Linearity:**
  ±0.8LSB typ, ±1.5LSB max INL
  +0.7LSB typ, +1.25LSB max DNL
  ±1mV max Offset
  ±16LSB typ Gain Error
- ***micro*Power:**
  10mW at 5V, 250kHz
  4mW at 2.7V, 200kHz
  2mW at 2.7V, 100kHz
  0.2mW at 2.7V, 10kHz
- **Packages: MSOP-8, SON-8**
- **Pin-Compatible with the ADS8321**
- **Serial (SPI™/SSI) Interface**

APPLICATIONS

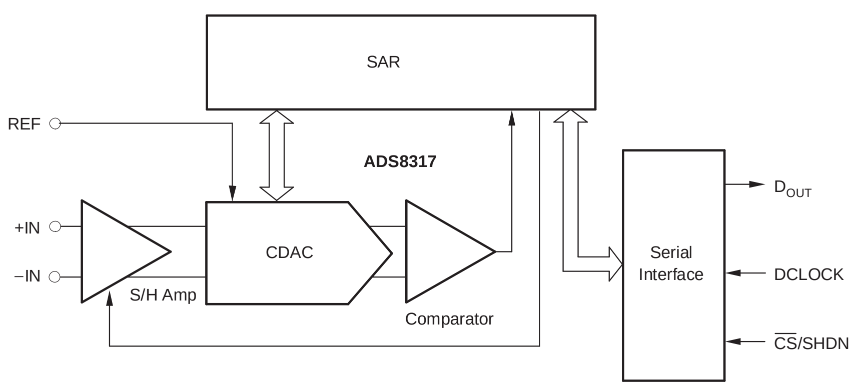
- **Battery-Operated Systems**
- **Remote Data Acquisition**
- **Isolated Data Acquisition**
- **Simultaneous Sampling, Multichannel Systems**
- **Industrial Controls**
- **Robotics**
- **Vibration Analysis**

DESCRIPTION

The ADS8317 is a 16-bit, sampling, analog-to-digital (A/D) converter specified for a supply voltage range from 2.7V to 5.5V. It requires very little power, even when operating at the full data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode. For example, the average power dissipation is less than 0.2mW at a 10kHz data rate.

The ADS8317 offers excellent linearity and very low noise and distortion. It also features a synchronous serial (SPI/SSI-compatible) interface and a differential input. The reference voltage can be set to any level within the range of 0.1V to V_{DD}/2.

Low power and small size make the ADS8317 ideal for portable and battery-operated systems. It is also an excellent fit for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition. The ADS8317 is available in MSOP-8 and SON-8 packages. The SON package size is the same as a 3x3 QFN package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB) (2)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8317I	±2	16	MSOP-8	DGK	–40°C to +85°C	D17	ADS8317IDGKT	Tape and Reel, 250
							ADS8317IDGKR	Tape and Reel, 2500
ADS8317IB	±1.5	16	MSOP-8	DGK	–40°C to +85°C	D17	ADS8317IBDGKT	Tape and Reel, 250
							ADS8317IBDGKR	Tape and Reel, 2500
ADS8317I	±2	16	SON-8	DRB	–40°C to +85°C	D17	ADS8317IDRBT	Tape and Reel, 250
							ADS8317IDRBR	Tape and Reel, 2500
ADS8317IB	±1.5	16	SON-8	DRB	–40°C to +85°C	D17	ADS8317IBDRBT	Tape and Reel, 250
							ADS8317IBDRBR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.
(2) ***Maximum Integral Linearity Error*** specifies a 5V power supply and 2.5V reference voltage.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS8317	UNIT
Supply voltage, V_{DD} to GND	–0.3 to +7	V
Analog input voltage(2)	–0.3 to V_{DD} + 0.3	V
Reference input voltage(2)	–0.3 to V_{DD} + 0.3	V
Digital input voltage(2)	–0.3 to V_{DD} + 0.3	V
Input current to any pin except supply	–20 to +20	mA
Power dissipation	See Dissipation Ratings Table	
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating free-air temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A ≤ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGK	+39.1°C/W	+206.3°C/W	4.847mW/°C	606mW	388mW	315mW
DRB	+5°C/W	+45.8°C/W	3.7mW/°C	370mW	204mW	148mW

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, GND to V_{DD}	Low-voltage levels	2.7		3.6	V
	5V logic levels	4.5	5.0	5.5	V
Reference input voltage		1		$V_{DD}/2$	V
Analog input voltage	–IN to GND	–0.2		V_{DD} + 0.2	V
	+IN to GND	–0.2		V_{DD} + 0.2	V
	+IN – (–IN)	$–V_{REF}$		$+V_{REF}$	V
Operating junction temperature, T_J		–40		+125	°C

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V

At –40°C to +85°C, V_{REF} = +2.5V, –IN = +2.5V, f_{SAMPLE} = 250kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8317I			ADS8317IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Full-scale range	FSR	+IN – (–IN)	$–V_{REF}$		V_{REF}	$–V_{REF}$		V_{REF}	V
Absolute input range		+IN	–0.1		V_{DD} + 0.1	–0.1		V_{DD} + 0.1	V
Input resistance	R_{ON}	Hold		5			5		GΩ
		Sampling		50	100		50	100	Ω
Input capacitance		During sampling		24			24		pF
Input leakage current				±50			±50		nA
Differential input capacitance		+IN to –IN, during sampling		20			20		pF
Full-power bandwidth	FSBW	f_S sinewave, SINAD = 60dB		500			500		kHz
DC ACCURACY									
Resolution			16			16			Bits
No missing codes	NMC			16	16		16	16	Bits
Integral linearity error	INL		–2	±1.5	+2	–1.5	±0.8	+1.5	LSB
Differential linearity error	DNL		–1	±1	+2	–1	+0.7,–0.5	+1.25	LSB
Offset error	V_{OS}		–2	±0.75	+2	–1	±0.5	+1	mV
Offset error drift	TCV_{OS}			±3			±3		µV/°C
Gain error	G_{ERR}	Positive	–32	±16	+32	–32	±16	+32	LSB
		Negative	–32	±16	+32	–32	±16	+32	LSB
Gain error drift	TCG_{ERR}			±0.1			±0.1		ppm/°C
Bipolar zero error			–2	±0.75	+2	–1	±0.5	+1	mV
Bipolar zero error drift				±3			±3		µV/°C
Noise				50			50		µVRMS
Power-supply rejection	PSRR	4.75V ≤ V_{DD} ≤ 5.25V		1			1		LSB
SAMPLING DYNAMICS									
Conversion time (16 DCLOCKs)	t_{CONV}	24kHz ≤ f_{CLK} ≤ 6.0MHz	2.667		666.7	2.667		666.7	µs
Acquisition time (4.5 DCLOCKs)	t_{AQ}	f_{CLK} = 6.0MHz	0.75			0.75			µs
Throughput rate (22 DCLOCKs)					250			250	kSPS
Clock frequency			0.024		6.0	0.024		6.0	MHz

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At –40°C to +85°C, V_{REF} = +2.5V, –IN = +2.5V, f_{SAMPLE} = 250kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8317I			ADS8317IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC ACCURACY									
Total harmonic distortion	THD	$5V_{PP}$ sinewave at 2kHz		–102			–106		dB
		$5V_{PP}$ sinewave at 10kHz		–100			–104		dB
Spurious-free dynamic range	SFDR	$5V_{PP}$ sinewave at 2kHz		106			110		dB
		$5V_{PP}$ sinewave at 10kHz		104			109		dB
Signal-to-noise ratio	SNR	$5V_{PP}$ sinewave at 2kHz		89.6			90		dB
		$5V_{PP}$ sinewave at 10kHz		89.6			90		dB
Signal-to-noise + distortion	SINAD	$5V_{PP}$ sinewave at 2kHz		89.5			89.9		dB
		$5V_{PP}$ sinewave at 10kHz		89.4			89.8		dB
Effective number of bits	ENOB	$5V_{PP}$ sinewave at 2kHz		14.57			14.65		Bits
		$5V_{PP}$ sinewave at 10kHz		14.56			14.63		Bits
VOLTAGE REFERENCE INPUT									
Reference voltage			0.5		$V_{DD}/2$	0.5		$V_{DD}/2$	V
Reference input resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5		GΩ
		$\overline{CS}$ = V_{DD}		5			5		GΩ
Reference input capacitance				24			24		pF
Reference input current		f_S = 250kHz		35	52		35	52	µA
		f_S = 200kHz		25	38		25	38	µA
		f_S = 100kHz		10	15		10	15	µA
		f_S = 10kHz		1	2		1	2	µA
		$\overline{CS}$ = V_{DD}		0.1			0.1		µA
DIGITAL INPUTS(1)									
Logic family				CMOS			CMOS		
High-level input voltage	V_{IH}		0.7 × V_{DD}		V_{DD} + 0.3	0.7 × V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.3		0.3 × V_{DD}	–0.3		0.3 × V_{DD}	V
Input current	I_{IN}	V_I = V_{DD} or GND	–50		+50	–50		+50	nA
Input capacitance	C_I			5			5		pF
DIGITAL OUTPUTS(1)									
Logic family				CMOS			CMOS		
High-level output voltage	V_{OH}	V_{DD} = 4.5V, I_{OH} = –100µA	4.44			4.44			V
Low-level output voltage	V_{OL}	V_{DD} = 4.5V, I_{OL} = 100µA			0.5			0.5	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND	–50		+50	–50		+50	nA
Output capacitance	C_O			5			5		pF
Load capacitance	C_L				30			30	pF
Data format				Binary twos complement			Binary twos complement		

(1) Applies for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.

ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V

At –40°C to +85°C, V_{REF} = +1.25V, –IN = 1.25V, f_{SAMPLE} = 200kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8317I MIN	ADS8317I TYP	ADS8317I MAX	ADS8317IB MIN	ADS8317IB TYP	ADS8317IB MAX	UNIT
ANALOG INPUT									
Full-scale range	FSR	+IN – (–IN)	$-V_{REF}$		V_{REF}	$-V_{REF}$		V_{REF}	V
Absolute input range		+IN	–0.1		V_{DD} + 0.1	–0.1		V_{DD} + 0.1	V
Input resistance	R_{ON}	Hold		5			5		GΩ
		Sampling		100	150		100	150	Ω
Input capacitance		During sampling		24			24		pF
Input leakage current				±50			±50		nA
Differential input capacitance		+IN to –IN, during sampling		20			20		pF
Full-power bandwidth	FSBW	f_S sinewave, SINAD = 60dB		1000			1000		kHz
DC ACCURACY									
Resolution			16			16			Bits
No missing codes	NMC			16	16		16	16	Bits
Integral linearity error	INL		–3	±2	+3	–2	±1.5	+2	LSB
Differential linearity error	DNL		–1	+1.5,–1	+2.5	–1	±1	+2	LSB
Offset error	V_{OS}		–2	±1	+2	–1	±0.5	+1	mV
Offset error drift	TCV_{OS}			±0.4			±0.4		µV/°C
Gain error	G_{ERR}	Positive	–32	±16	+32	–32	±16	+32	LSB
		Negative	–32	±16	+32	–32	±16	+32	LSB
Gain error drift	TCG_{ERR}			±0.15			±0.15		ppm/°C
Bipolar zero error			–2	±0.8	+2	–1	±0.4	+1	mV
Bipolar zero error drift				±0.2			±0.2		µV/°C
Noise				50			50		µVRMS
Power-supply rejection	PSRR	2.7V ≤ V_{DD} ≤ 3.6V		1			1		LSB
SAMPLING DYNAMICS									
Conversion time (16 DCLOCKs)	t_{CONV}	24kHz ≤ f_{CLK} ≤ 4.8MHz	3.333		666.7	3.333		666.7	µs
Acquisition time (4.5 DCLOCKs)	t_{AQ}	f_{CLK} = 4.8MHz	0.9375			0.9375			µs
Throughput rate (22 DCLOCKs)					200			200	kSPS
Clock frequency			0.024		4.8	0.024		4.8	MHz
AC ACCURACY									
Total harmonic distortion	THD	2.5V_{PP} sinewave at 2kHz		–104			–107		dB
		2.5V_{PP} sinewave at 10kHz		–101			–106		dB
Spurious-free dynamic range	SFDR	2.5V_{PP} sinewave at 2kHz		106			108		dB
		2.5V_{PP} sinewave at 10kHz		104			107		dB
Signal-to-noise ratio	SNR	2.5V_{PP} sinewave at 2kHz		84.8			85		dB
		2.5V_{PP} sinewave at 10kHz		84.8			85		dB
Signal-to-noise + distortion	SINAD	2.5V_{PP} sinewave at 2kHz		84.7			84.9		dB
		2.5V_{PP} sinewave at 10kHz		84.7			84.8		dB
Effective number of bits	ENOB	2.5V_{PP} sinewave at 2kHz		13.77			13.8		Bits
		2.5V_{PP} sinewave at 10kHz		13.77			13.79		Bits
VOLTAGE REFERENCE INPUT									
Reference voltage			1		$V_{DD}/2$	1		$V_{DD}/2$	V
Reference input resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5		kΩ
		$\overline{CS}$ = V_{DD}		5			5		GΩ
Reference input capacitance				20			20		pF
Reference input current		f_S = 200kHz		9	14		9	14	µA
		f_S = 100kHz		3	5		3	5	µA
		f_S = 10kHz		0.5	1		0.5	1	µA
		$\overline{CS}$ = V_{DD}		0.1			0.1		µA

ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At –40°C to +85°C, V_{REF} = +1.25V, –IN = 1.25V, f_{SAMPLE} = 200kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8317I			ADS8317IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS(1)									
Logic family				LVCMOS			LVCMOS		
High-level input voltage	V_{IH}	V_{DD} = 3.6V	2		V_{DD} + 0.3	2		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	V_{DD} = 2.7V	–0.3		0.8	–0.3		0.3 × V_{DD}	V
Input current	I_{IN}	V_I = V_{DD} or GND	–50		+50	–50		+50	nA
Input capacitance	C_I			5			5		pF
DIGITAL OUTPUTS(1)									
Logic family				LVCMOS			LVCMOS		
High-level output voltage	V_{OH}	V_{DD} = 2.7V, I_{OH} = –100μA	V_{DD} – 0.2			V_{DD} – 0.2			V
Low-level output voltage	V_{OL}	V_{DD} = 2.7V, I_{OL} = 100μA			0.2			0.2	V
High-impedance state output current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND	–50		+50	–50		+50	nA
Output capacitance	C_O			5			5		pF
Load capacitance	C_L				30			30	pF
Data format				Binary twos complement			Binary twos complement		

(1) Applies for 5.0V nominal supply: V_{DD} (min) = 2.7V and V_{DD} (max) = 3.6V.

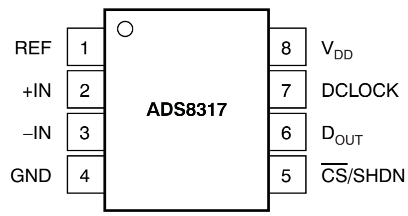
ELECTRICAL CHARACTERISTICS: GENERAL

At –40°C to +85°C, –IN = GND, and f_{DCLOCK} = 24 × f_{SAMPLE}, unless otherwise noted.

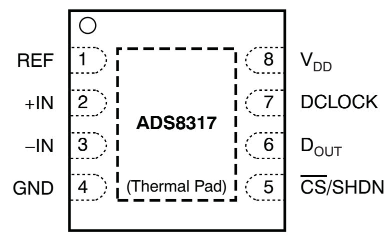
PARAMETER		TEST CONDITIONS	ADS8317I			ADS8317IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Power supply	V_{DD}	Low-voltage levels	2.7		3.6	2.7		3.6	V
		5V logic levels	4.5		5.5	4.5		5.5	V
Operating supply current	I_{DD}	V_{DD} = 2.7V, f_S = 10kHz, f_{DCLOCK} = 4.8MHz		0.065	0.085		0.065	0.085	mA
		V_{DD} = 2.7V, f_S = 100kHz, f_{DCLOCK} = 4.8MHz		0.7	1.0		0.7	1.0	mA
		V_{DD} = 2.7V, f_S = 200kHz, f_{DCLOCK} = 4.8MHz		1.4	2.0		1.4	2.0	mA
		V_{DD} = 5V, f_S = 200kHz, f_{DCLOCK} = 6MHz		1.5	2.5		1.5	2.5	mA
		V_{DD} = 5V, f_S = 250kHz, f_{DCLOCK} = 6MHz		2.0	3.0		2.0	3.0	mA
Power-down supply current	I_{DD}	V_{DD} = 2.7V		0.1			0.1		μA
		V_{DD} = 5V		0.2			0.2		μA
Power dissipation		V_{DD} = 2.7V, f_S = 10kHz, f_{DCLOCK} = 4.8MHz		0.18	0.23		0.18	0.23	mW
		V_{DD} = 2.7V, f_S = 100kHz, f_{DCLOCK} = 4.8MHz		1.9	2.7		1.9	2.7	mW
		V_{DD} = 2.7V, f_S = 200kHz, f_{DCLOCK} = 4.8MHz		3.8	5.4		3.8	5.4	mW
		V_{DD} = 5V, f_S = 200kHz, f_{DCLOCK} = 6MHz		7.5	12.5		7.5	12.5	mW
		V_{DD} = 5V, f_S = 250kHz, f_{DCLOCK} = 6MHz		10	15		10	15	mW
Power dissipation in power-down		V_{DD} = 2.7V, $\overline{CS}$ = V_{DD}		0.3			0.3		μW
		V_{DD} = 5V, $\overline{CS}$ = V_{DD}		0.6			0.6		μW

PIN CONFIGURATION

**DGK PACKAGE
MSOP-8
(TOP VIEW)**



**DRB PACKAGE
SON-8
(TOP VIEW)**

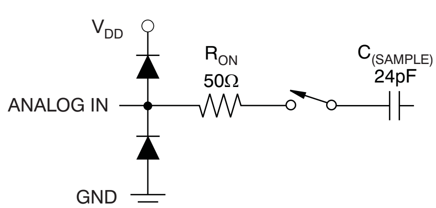


(1) The DRB package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance.

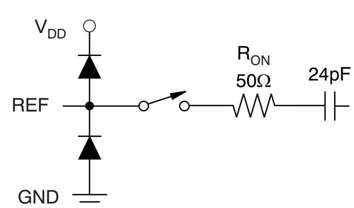
TERMINAL FUNCTIONS

TERMINAL			
NAME	**NO.**	**I/O**	**DESCRIPTION**
REF	1	Analog input	Reference input
+IN	2	Analog input	Noninverting analog input
–IN	3	Analog input	Inverting analog input
GND	4	Power-supply connection	Ground
$\overline{CS}$/SHDN	5	Digital input	Chip select when low; Shutdown mode when high.
D_{OUT}	6	Digital output	Serial output data word
DCLOCK	7	Digital input	Data clock synchronizes the serial data transfer and determines conversion speed.
V_{DD}	8	Power-supply connection	Power supply

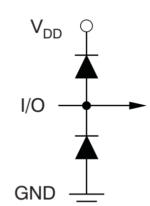
Equivalent Input Circuits (V_{DD} = 5.0V)



Diode Turn-On Voltage: 0.35V
Equivalent Analog Input Circuit

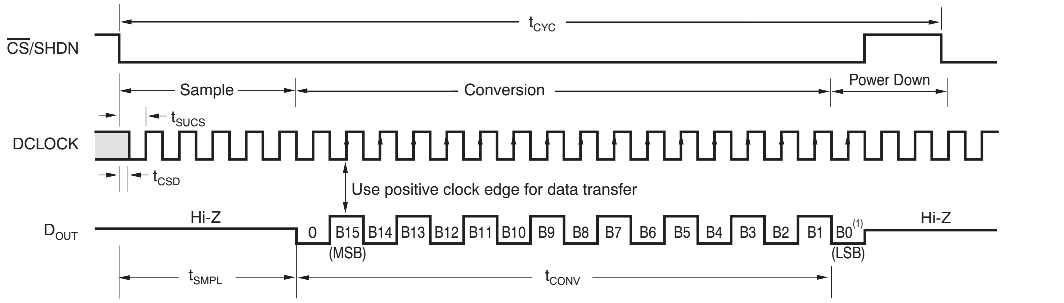


Equivalent Reference Input Circuit

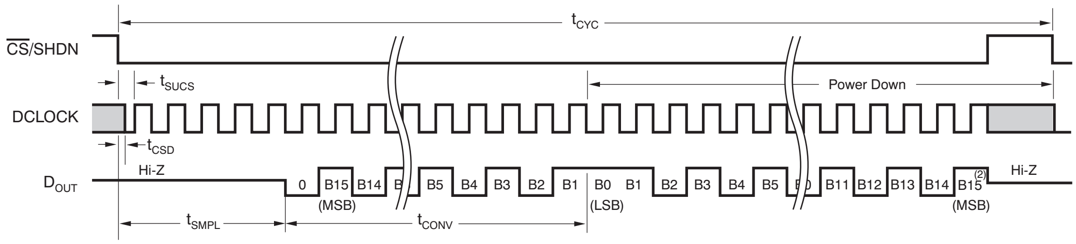


Equivalent Digital Input/Output Circuit

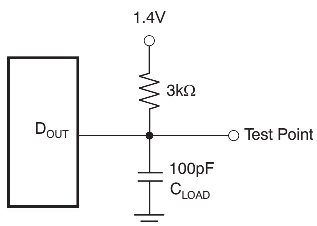
TIMING INFORMATION



NOTE: (1) A minimum of 22 clock cycles are required for 16-bit conversion; 24 clock cycles are shown. If $\overline{CS}$ remains low at the end of conversion, a new data stream is shifted out with LSB-first data followed by zeroes indefinitely.

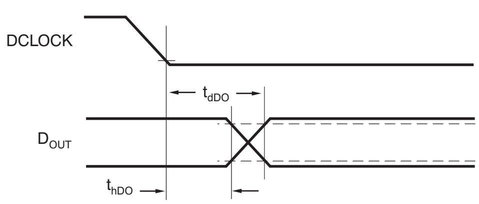


NOTE: (2) After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D converter will output zeroes indefinitely.

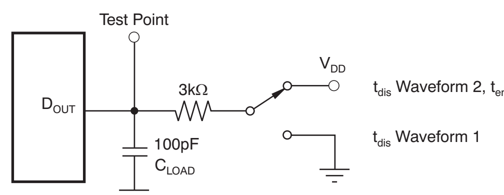


Load Circuit for t_{dDO}, t_r, and t_f

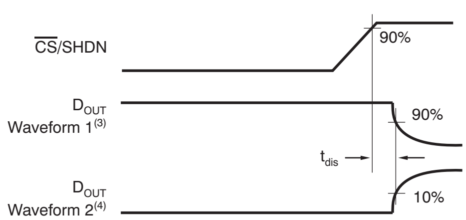
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



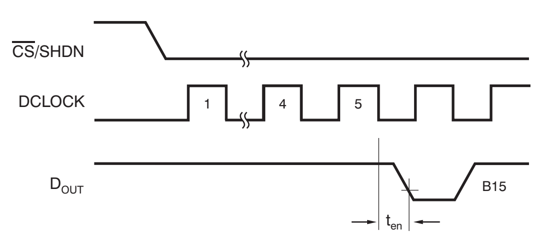
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



Voltage Waveforms for t_{en}

NOTES: (3) Waveform 1 is for an output with internal conditions such that the output is high unless disabled by the output control.
(4) Waveform 2 is for an output with internal conditions such that the output is low unless disabled by the output control.

Figure 1. Timing Diagrams

TIMING INFORMATION (continued)

Timing Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SMPL}	Analog input sample time	4.5		5.0	DCLOCKs
t_{CONV}	Conversion time		16		DCLOCKs
t_{CYC}	Complete cycle time	22			DCLOCKs
t_{CSD}	$\overline{CS}$ falling to DCLOCK low			0	ns
t_{SUCS}	$\overline{CS}$ falling to DCLOCK rising	20			ns
t_{HDO}	DCLOCK falling to current D_{OUT} not valid	5	15		ns
t_{DIS}	$\overline{CS}$ rising to D_{OUT} 3-state		70	100	ns
t_{EN}	DCLOCK falling to D_{OUT} enabled		20	50	ns
t_F	D_{OUT} fall time		5	25	ns
t_R	D_{OUT} rise time		7	25	ns

TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = 25°C, V_{REF} = 2.5V, f_{SAMPLE} = 250kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

INTEGRAL LINEARITY ERROR vs CODE

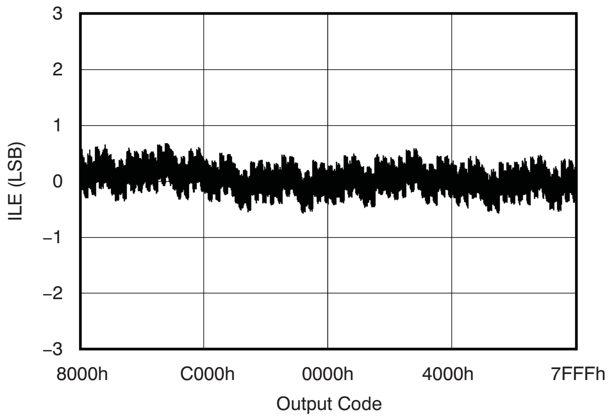


Figure 2.

DIFFERENTIAL LINEARITY ERROR vs CODE

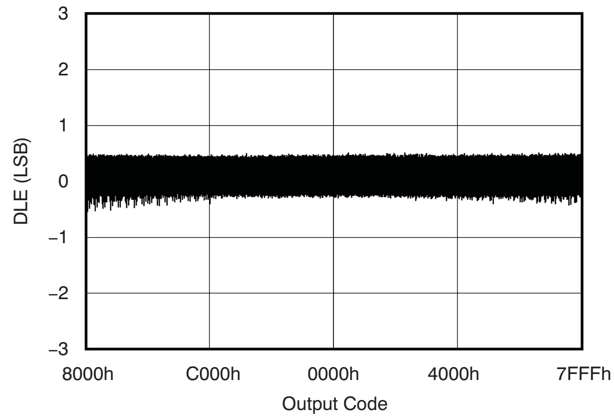


Figure 3.

SUPPLY CURRENT vs TEMPERATURE

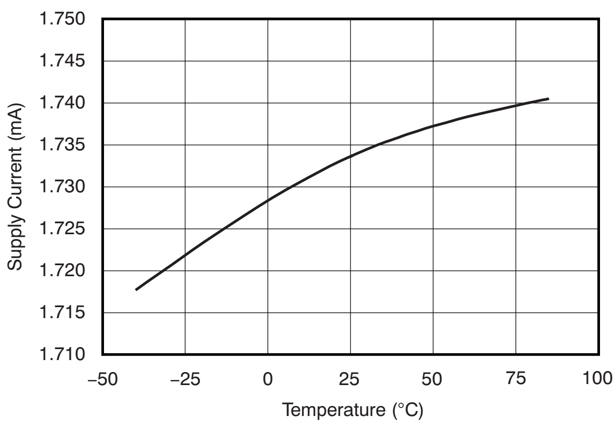


Figure 4.

CHANGE IN OFFSET vs TEMPERATURE

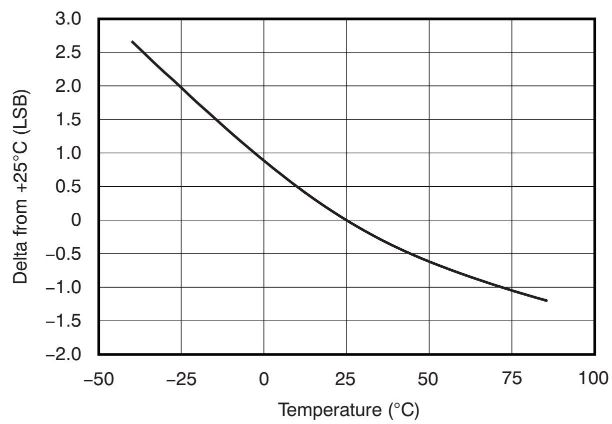


Figure 5.

CHANGE IN BIPOLAR ZERO ERROR vs TEMPERATURE

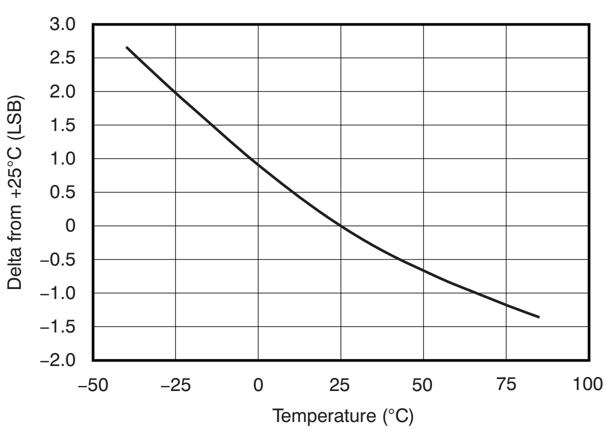


Figure 6.

CHANGE IN GAIN vs TEMPERATURE

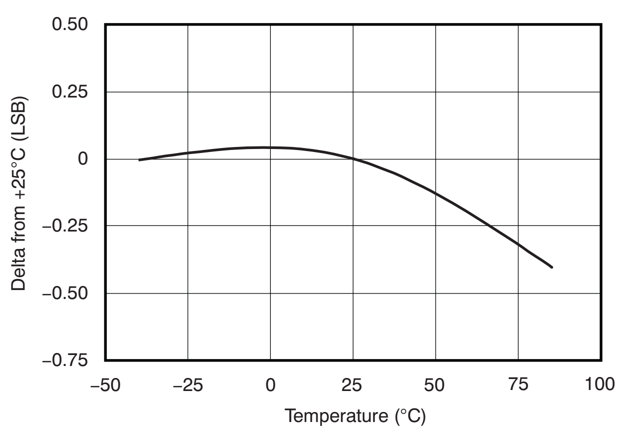


Figure 7.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = 25°C, V_{REF} = 2.5V, f_{SAMPLE} = 250kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

POWER-DOWN CURRENT vs TEMPERATURE

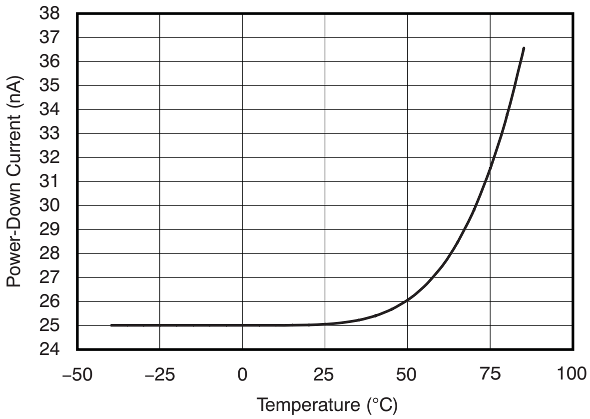


Figure 8.

SUPPLY CURRENT vs SAMPLING RATE

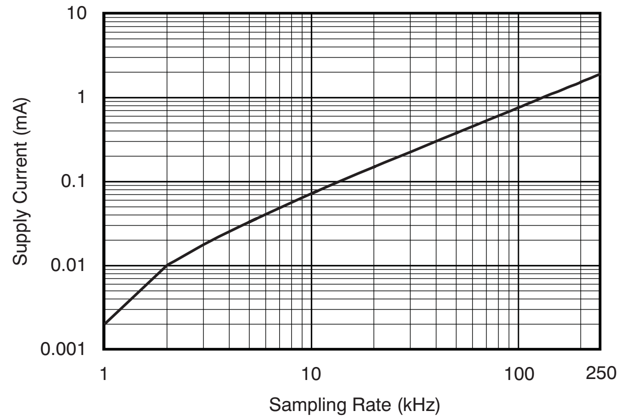


Figure 9.

REFERENCE CURRENT vs SAMPLING RATE

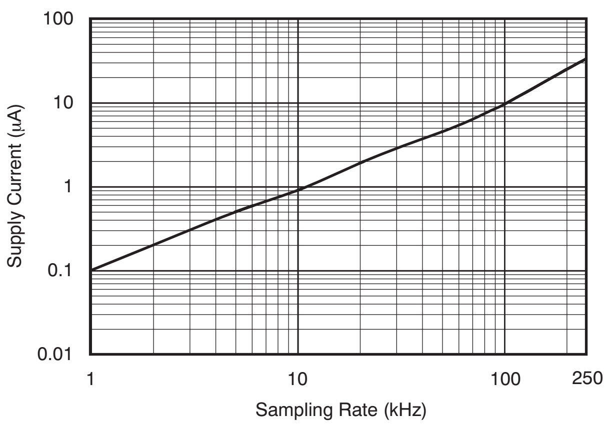


Figure 10.

FREQUENCY SPECTRUM
(8192 point FFT, f_{IN} = 1.9836kHz, –0.2dB)

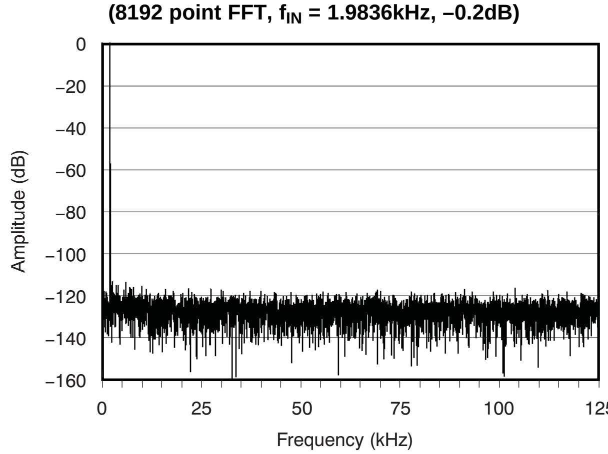


Figure 11.

FREQUENCY SPECTRUM
(8192 Point FFT, f_{IN} = 9.9792kHz, –0.2dB)

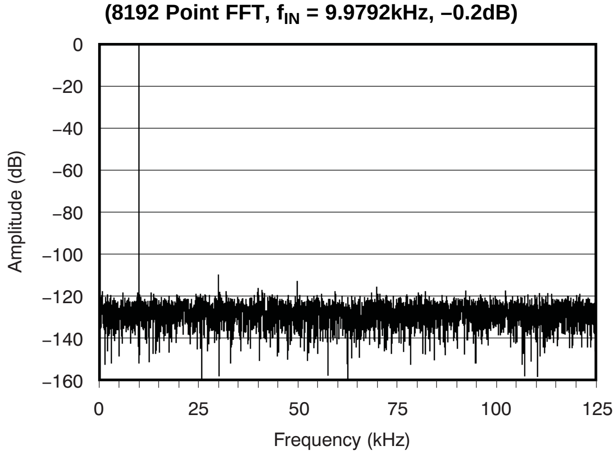


Figure 12.

SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

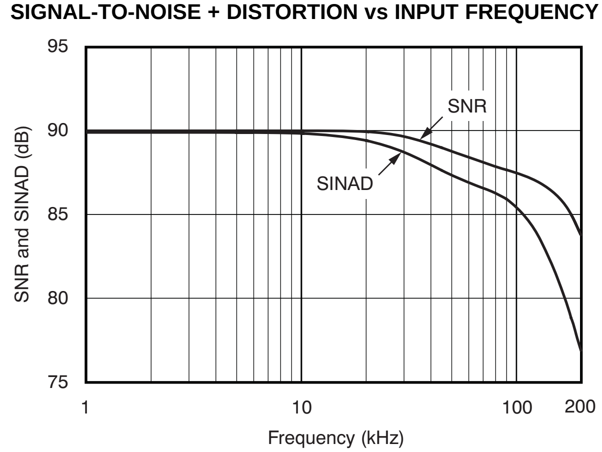


Figure 13.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = 25°C, V_{REF} = 2.5V, f_{SAMPLE} = 250kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

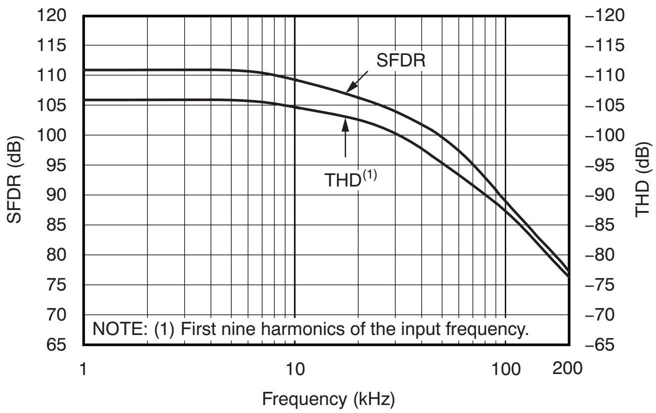


Figure 14.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

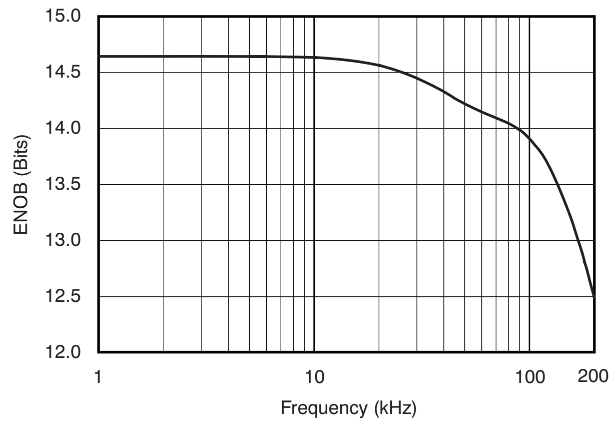


Figure 15.

CHANGE IN SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

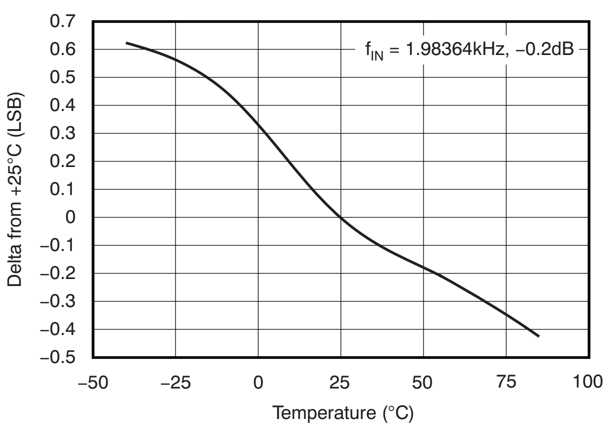


Figure 16.

CHANGE IN SIGNAL-TO-NOISE + DISTORTION vs INPUT LEVEL

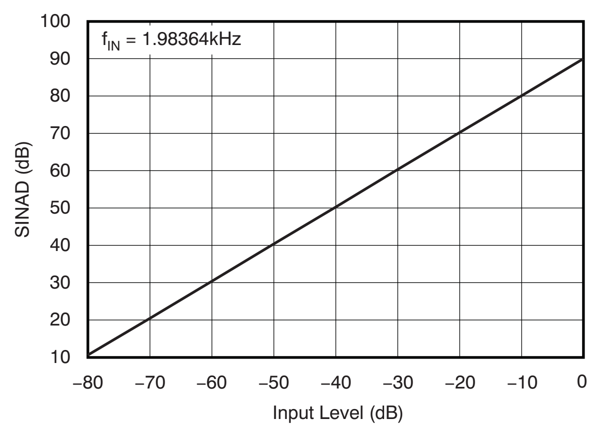


Figure 17.

PEAK-TO-PEAK NOISE FOR A DC INPUT vs REFERENCE VOLTAGE

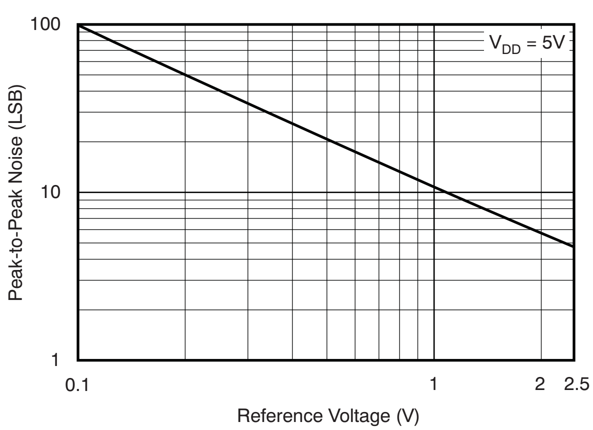


Figure 18.

OUTPUT CODE HISTOGRAM FOR A DC INPUT (8192 Conversions)

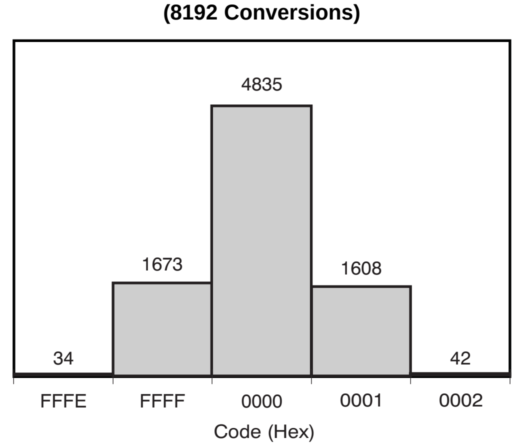


Figure 19.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = 25°C, V_{REF} = 1.25V, f_{SAMPLE} = 200kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

INTEGRAL LINEARITY ERROR vs CODE

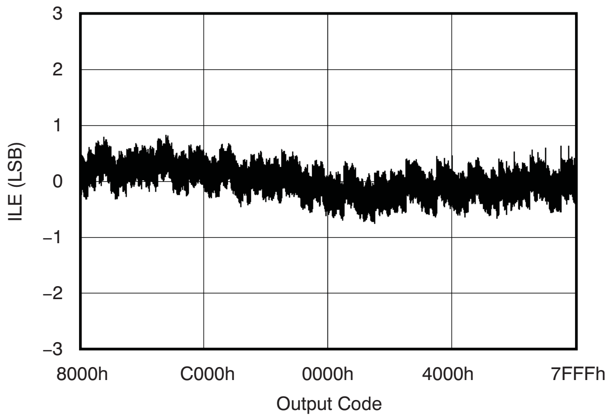


Figure 20.

DIFFERENTIAL LINEARITY ERROR vs CODE

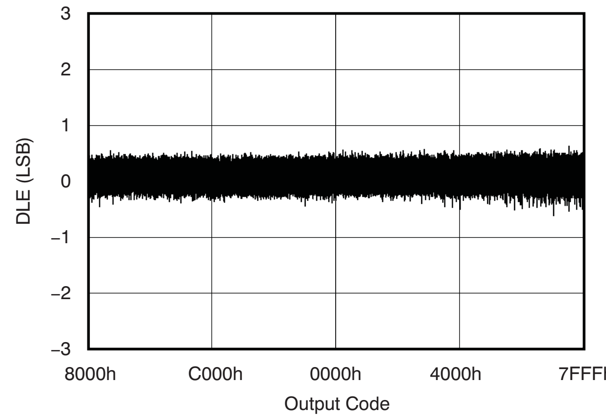


Figure 21.

SUPPLY CURRENT vs TEMPERATURE

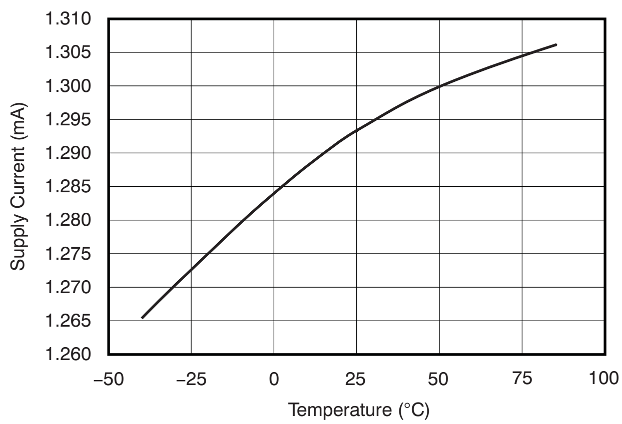


Figure 22.

CHANGE IN OFFSET vs TEMPERATURE

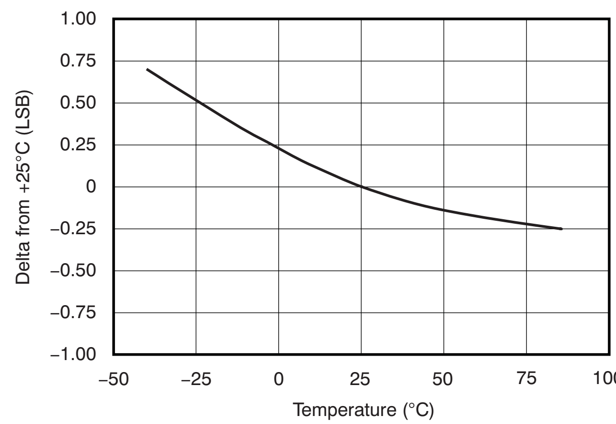


Figure 23.

CHANGE IN BIPOLAR ZERO ERROR vs TEMPERATURE

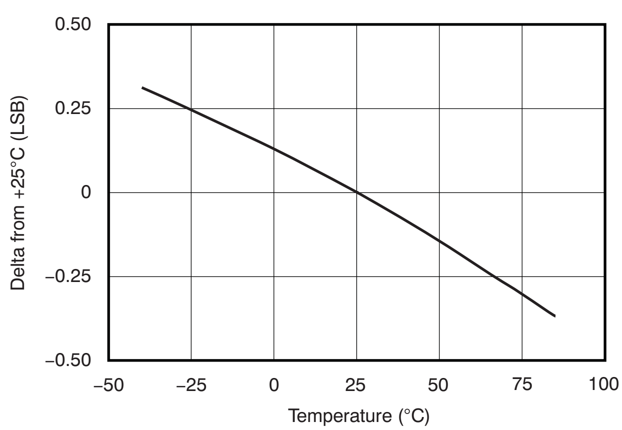


Figure 24.

CHANGE IN GAIN vs TEMPERATURE

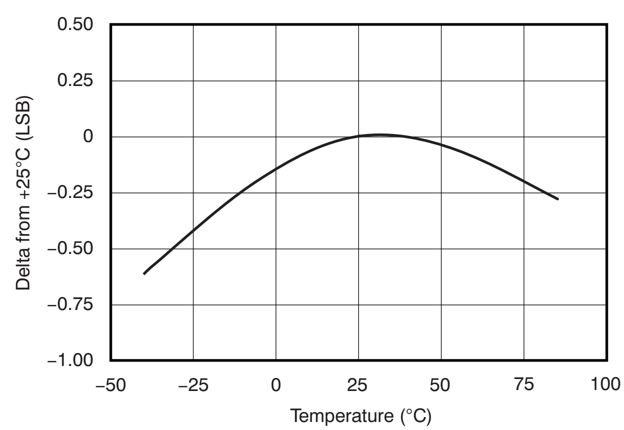


Figure 25.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = 25°C, V_{REF} = 1.25V, f_{SAMPLE} = 200kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

POWER-DOWN CURRENT vs TEMPERATURE

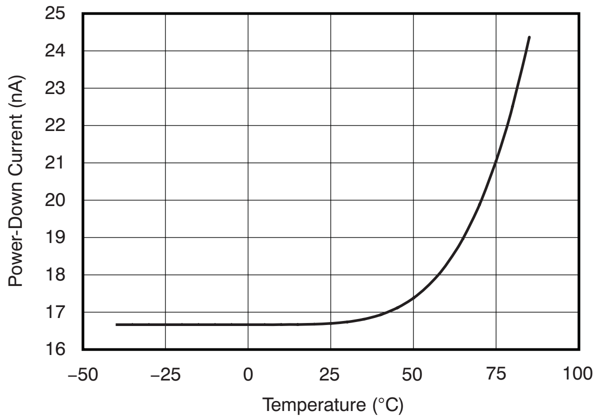


Figure 26.

SUPPLY CURRENT vs SAMPLING RATE

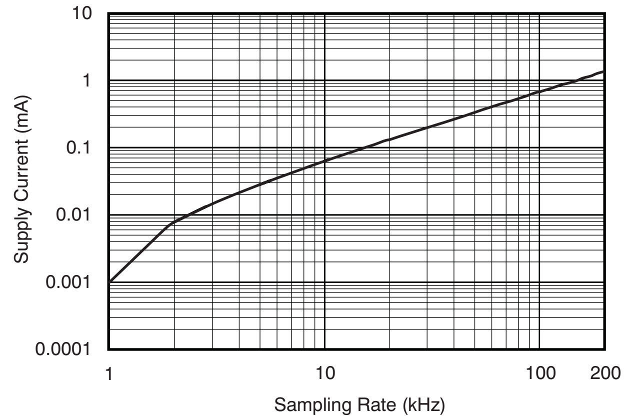


Figure 27.

REFERENCE CURRENT vs SAMPLING RATE

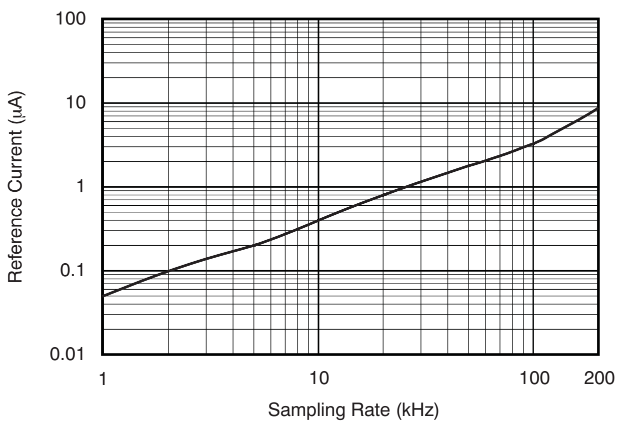


Figure 28.

FREQUENCY SPECTRUM
(8192 Point FFT, f_IN = 1.9775kHz, –0.2dB)

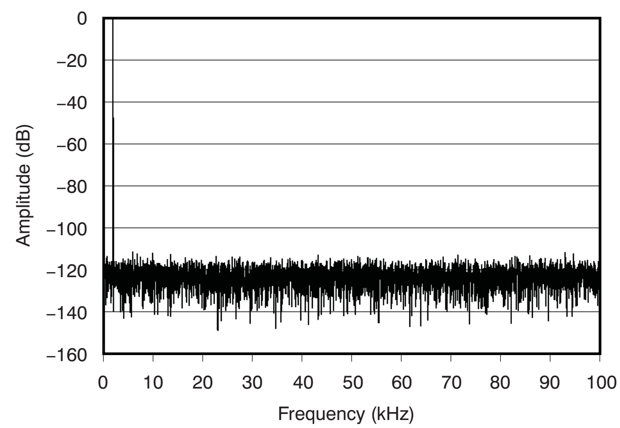


Figure 29.

FREQUENCY SPECTRUM
(8192 Point FFT, f_{IN} = 9.9854kHz, –0.2dB)

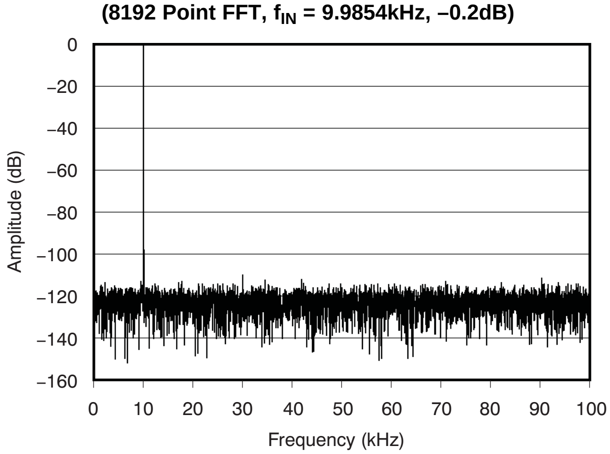


Figure 30.

SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

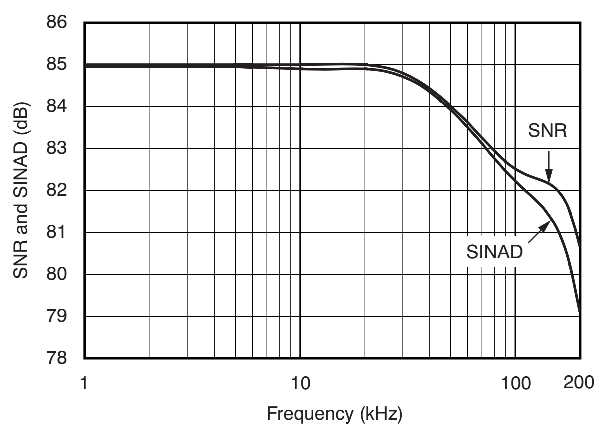


Figure 31.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = 25°C, V_{REF} = 1.25V, f_{SAMPLE} = 200kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

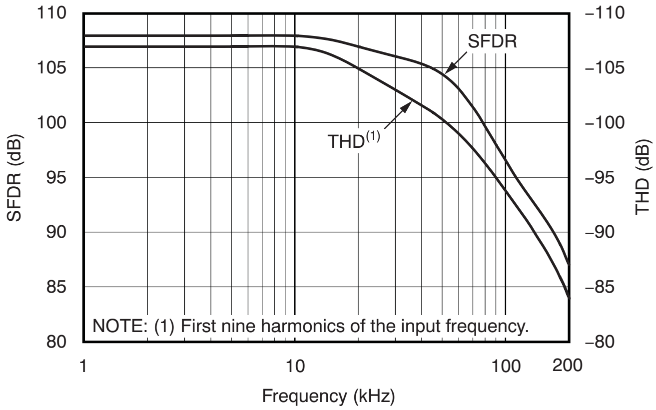


Figure 32.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

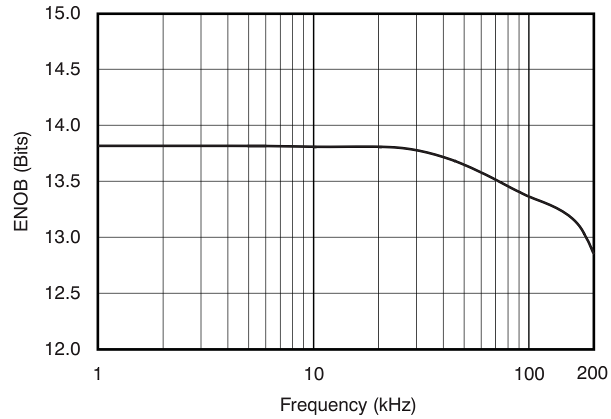


Figure 33.

CHANGE IN SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

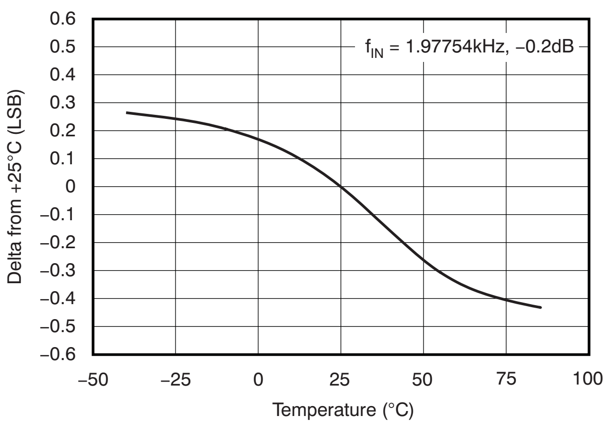


Figure 34.

SIGNAL-TO-NOISE + DISTORTION vs INPUT LEVEL

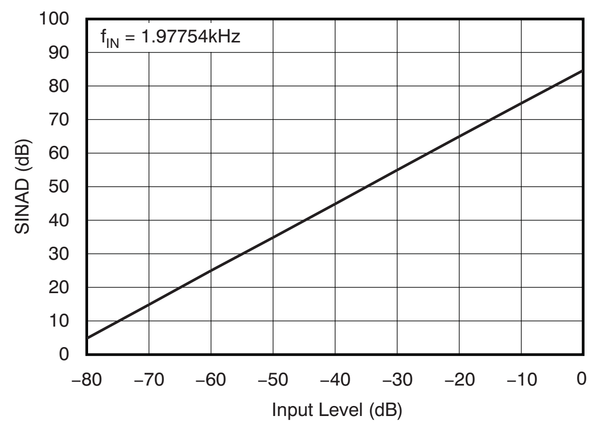


Figure 35.

OUTPUT CODE HISTOGRAM FOR A DC INPUT (8192 Conversions)

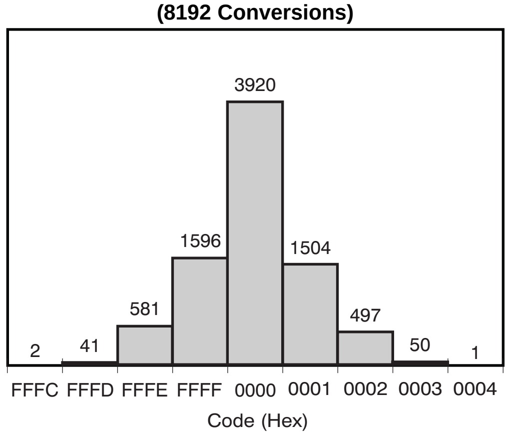


Figure 36.

THEORY OF OPERATION

The ADS8317 is a classic Successive Approximation Register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6μ CMOS process. The architecture and fabrication process allow the ADS8317 to acquire and convert an analog signal at up to 250,000 conversions per second while consuming less than 10mW from V_{DD}.

Differential linearity for the ADS8317 is factory-adjusted via a package-level trim procedure. The state of the trim elements is stored in non-volatile memory and is continuously updated after each acquisition cycle, just prior to the start of the successive approximation operation. This process ensures that one complete conversion cycle always returns the part to its factory-adjusted state in the event of a power interruption.

The ADS8317 requires an external reference, an external clock, and a single power source (V_{DD}). The external reference can be any voltage between 0.1V and V_{DD}/2. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8317.

The external clock can vary between 24kHz (1kHz throughput) and 6.0MHz (250kHz throughput). The duty cycle of the clock is not significant, as long as the minimum high and low times are at least 200ns (V_{DD} = 4.75V or greater). The minimum clock frequency is set by the leakage on the internal capacitors to the ADS8317.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially (most significant bit first) on the D_{OUT} pin.

The digital data that are provided on the D_{OUT} pin are for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8317 after the conversion is complete and to obtain the serial data least significant bit first. See the *Digital Timing* section for more information.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8317: single-ended or differential, as shown in Figure 37. When the input is single-ended, the –IN input is held at a fixed voltage. The +IN input swings around the same voltage and the peak-to-peak amplitude is 2 × V_{REF}. The value of V_{REF} determines the range over which the common voltage may vary, as shown in Figure 38 and Figure 39.

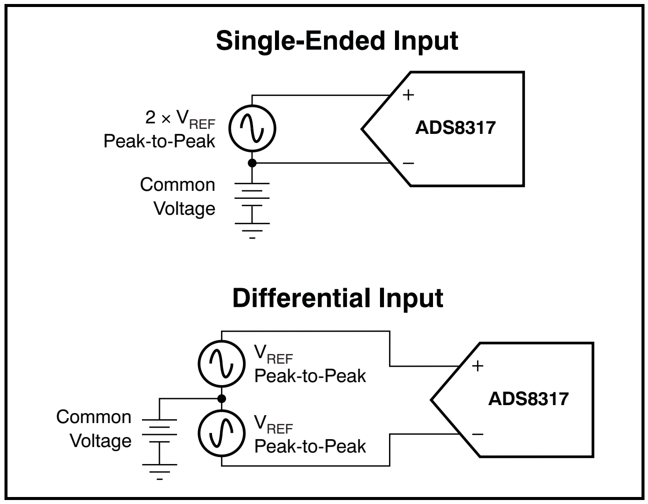


Figure 37. Methods of Driving the ADS8317—Single-Ended or Differential

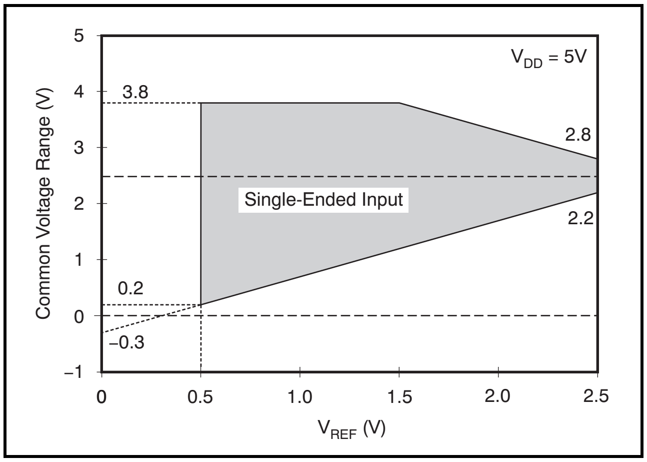


Figure 38. Single-Ended 5V Input, Common Voltage Range vs V_{REF}

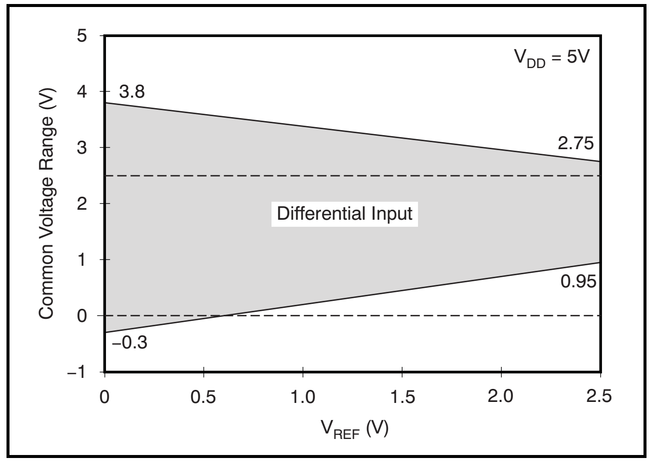


Figure 40. Differential 5V Input, Common Voltage Range vs V_{REF}

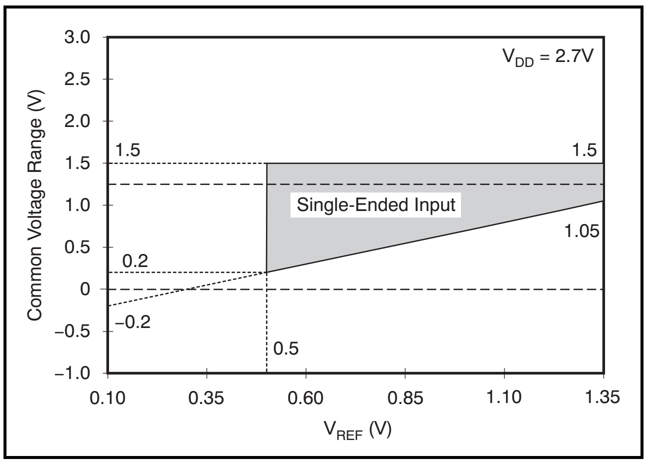


Figure 39. Single-Ended 2.7V Input, Common Voltage Range vs V_{REF}

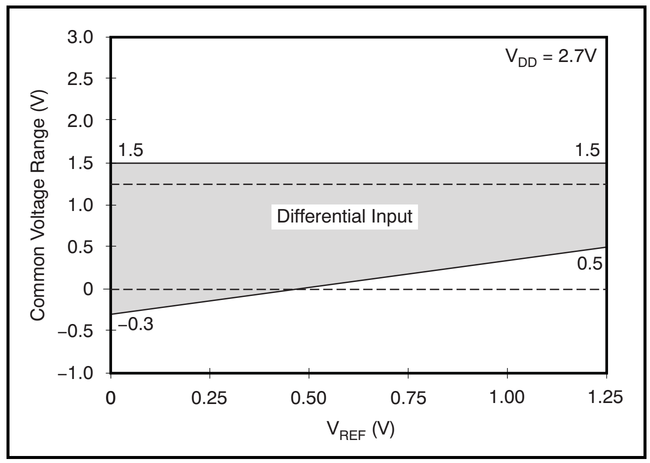


Figure 41. Differential 2.7V Input, Common Voltage Range vs V_{REF}

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or +IN – (–IN). A voltage or signal is common to both of these inputs. The peak-to-peak amplitude of each input is V_{REF} about this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the difference voltage is 2 × V_{REF}. The value of V_{REF} also determines the range of the voltage that may be common to both inputs, as shown in Figure 41 and Figure 40.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this matching is not observed, the two inputs could have different settling times. This difference may result in offset error, gain error, and linearity error that change with both temperature and input voltage. If the impedance cannot be matched, the errors can be lessened by giving the ADS8317 additional acquisition time.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8317 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (24pF) to 16-bit settling level within 4.5 clock cycles. When the converter goes into the hold mode, or while it is in the power-down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN input should always remain within the range of GND – 300mV to V_{DD} + 300mW. The –IN input should always remain within the range of GND – 300mV to 4V. Outside of these ranges, the converter linearity may not meet specifications. To obtain maximum performance from the ADS8317, an input circuit such as that shown in Figure 42 is recommended.

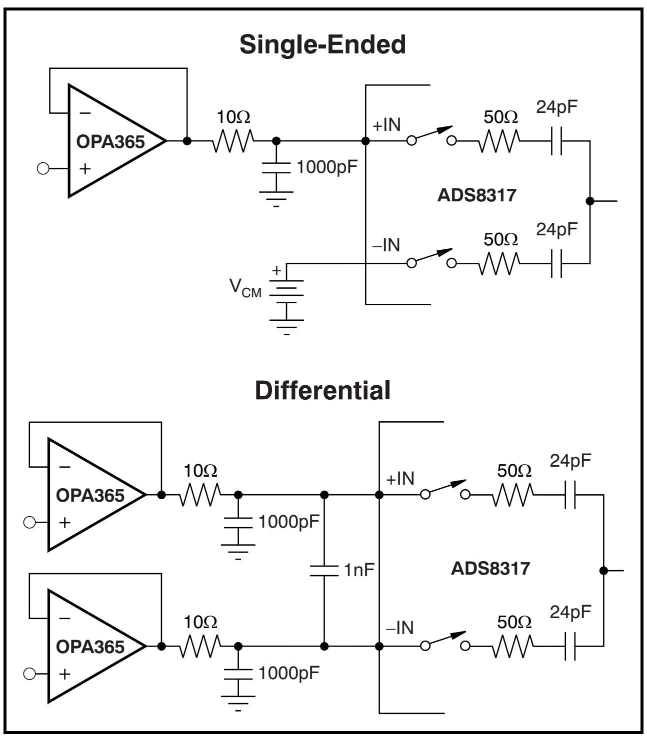


Figure 42. Single-Ended and Differential Methods of Interfacing the ADS8317

REFERENCE INPUT

The external reference sets the analog input range. The ADS8317 operates with a reference in the range of 0.1V to V_{DD}/2. There are several important implications to this specification.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This reduction is often referred to as the least significant bit (LSB) size and is equal to the reference voltage divided by 65,536. This relationship means that any offset or gain error inherent in the A/D converter appears to increase (in terms of LSB size) as the reference voltage is reduced. For a reference voltage of 2.5V, the value of the LSB is 76.3μV, and for a reference voltage of 1.25V, the LSB is 38.15μV.

The noise inherent in the converter also appears to increase with a lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 5LSB peak-to-peak of potential error to the output code. When the external reference is 1.25V, the potential error contribution from the internal noise is almost two times larger (9LSB). The errors arising from the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult Figure 18, *Peak-to-Peak Noise for a DC Input vs Reference Voltage*. Note that the Effective Number Of Bits (ENOB) figure is calculated based on the converter signal-to-(noise + distortion) ratio with a 2kHz, 0dB input signal. SINAD is related to ENOB as follows:

$$SINAD = 6.02 \times ENOB + 1.76$$

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Due to the lower LSB size, the converter is also more sensitive to external sources of error, such as nearby digital signals and electromagnetic interference.

The equivalent input circuit for the reference voltage is presented in Figure 43. At the same time, an equivalent capacitor of 24pF is switched. To obtain optimum performance from the ADS8317, special care must be taken in designing the interface circuit to the reference input pin. To ensure a stable reference voltage, a 47μF tantalum capacitor with low ESR should be connected as close as possible to the input pin. If a high output impedance reference source is used, an additional operational amplifier with a current-limiting resistor must be placed in front of the capacitors.

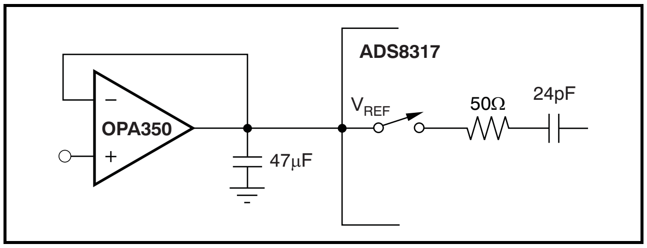


Figure 43. Input Reference Circuit and Interface

When the ADS8317 is in power-down mode, the input resistance of the reference pin has a value of 5GΩ. Because the input capacitors must be recharged before the next conversion starts, an operational amplifier with good dynamic characteristics, such as the OPA350, should be used to buffer the reference input.

Noise

The transition noise of the ADS8317 itself is extremely low, as shown in Figure 19 and Figure 36; it is much lower than competing A/D converters. These histograms were generated by applying a low-noise DC input and initiating 8192 conversions. The digital output of the A/D converter varies in output code because of the internal noise of the ADS8317. This variance is true for all 16-bit, SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions represent 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6, which yields the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. The ADS8317, with five output codes for the ±3σ distribution, yields less than ±0.8LSB of transition noise. Remember that to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be less than 50μV.

Averaging

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging four conversion results reduces the transition noise from ±0.8LSB to ±0.4LSB. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This configuration works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio improves by 3dB.

DIGITAL INTERFACE

Signal Levels

The ADS8317 has a wide range of power-supply voltage. The A/D converter, as well as the digital interface circuit, is designed to accept and operate from 2.7V up to 5.5V. This voltage range accommodates different logic levels. When the ADS8317 power-supply voltage is in the range of 4.5V to 5.5V (5V logic level), the ADS8317 can be connected directly to another 5V, CMOS-integrated circuit. When the ADS8317 power-supply voltage is in the range of 2.7V to 3.6V (3V logic level), the ADS8317 can be connected directly to another 3.3V LVCMOS integrated circuit.

Serial Interface

The ADS8317 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as illustrated in the *Timing Information* section and *Timing Characteristics* . The DCLOCK signal synchronizes the data transfer, with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal.

After the fifth falling DCLOCK edge, D_{OUT} is enabled and outputs a low value for one clock period. For the next 16 DCLOCK periods, D_{OUT} outputs the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks repeat the output data, but in a least significant bit first format.

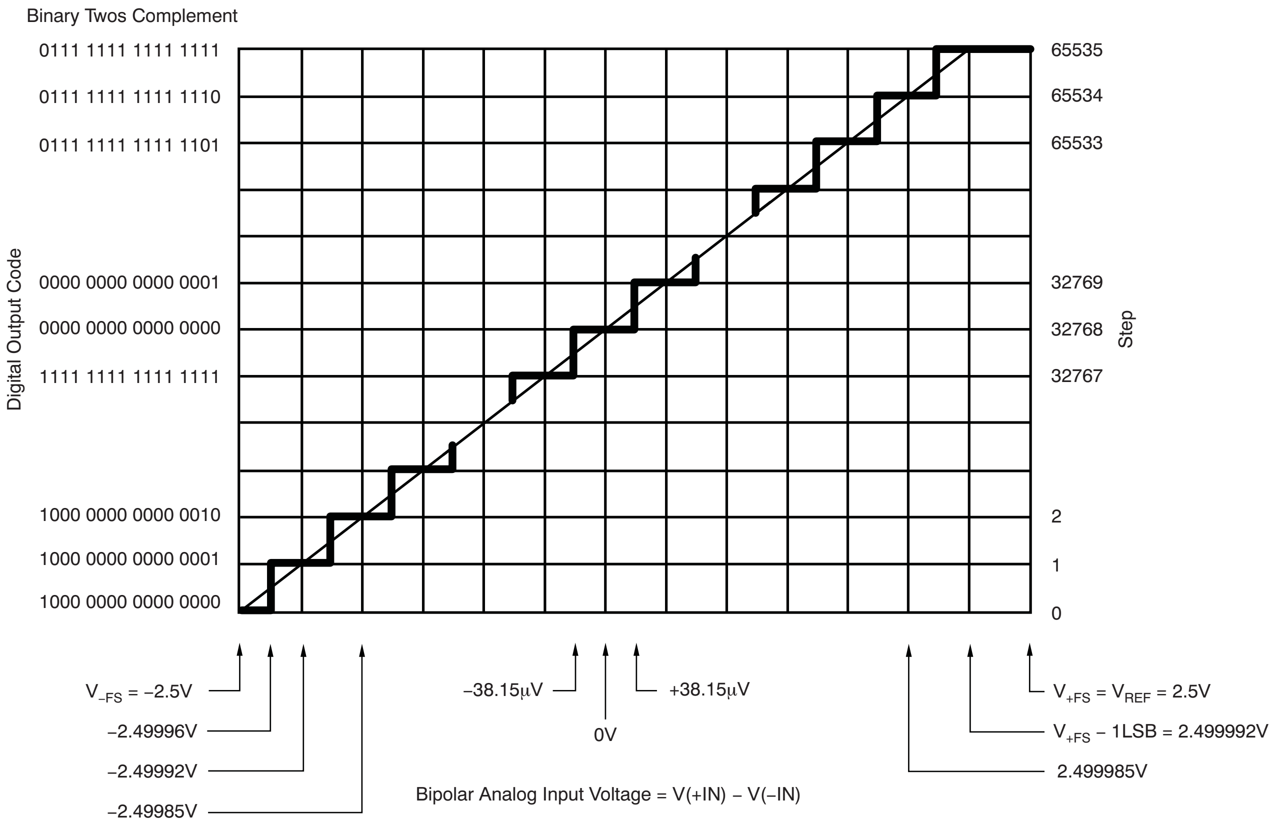
After the most significant bit (B15) has been repeated, D_{OUT} will 3-state. Subsequent clocks have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken high and returned low.

Data Format

The output data from the ADS8317 are in binary twos complement format, as shown in Table 1 and Figure 44. The table and figure represent the ideal output code for the given input voltage and do not include the effects of offset, gain error, or noise.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT BINARY TWOS COMPLEMENT	
Full-scale range	2 × V_{REF}		
Least significant bit (LSB)	2 × V_{REF}/65536	**Binary Code**	**Hex Code**
+Full scale	+V_{REF} – 1 LSB	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
Midscale – 1 LSB	0V – 1 LSB	1111 1111 1111 1111	FFFF
–Full scale	–V_{REF}	1000 0000 0000 0000	8000



16-BIT	Twos Complement Output	Bipolar Analog Input
−Full-Scale Code	V_{-FS} = 8000h	$V_{CODE} = -V_{REF}$
Midscale Code	V_{MS} = 0000h	V_{CODE} = 0V
+Full-Scale Code	V_{+FS} = 7FFFh	$V_{CODE} = V_{REF}$ − 1LSB

Figure 44. Ideal Conversion Characteristics (Conditions: V_{CM} = 2.5V, V_{REF} = 2.5V)

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS8317 to convert at up to a 250kHz rate while requiring very little power. However, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8317 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that satisfies the system requirements.

In addition, the ADS8317 goes into Power-Down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is high (see the Timing Characteristics section). Ideally, each conversion should occur as quickly as possible, preferably at a 6.0MHz clock rate. This way, the converter spends the longest possible time in power-down mode. This is very important because the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously until power-down mode is entered.

Figure 9 and Figure 27 illustrate the current consumption of the ADS8317 versus sample rate. For these graphs, the converter is clocked at maximum speed regardless of the sample rate. $\overline{CS}$ is held high during the remaining sample period.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when $\overline{CS}$ is high. $\overline{CS}$ low only shuts down the analog section. The digital section completely shuts down only when $\overline{CS}$ is high. Thus, if $\overline{CS}$ is left low at the end of a conversion, and the converter is continually clocked, the power consumption is not as low as when $\overline{CS}$ is high.

Short Cycling

Another way to save power is to use the $\overline{CS}$ signal to short-cycle the conversion. The ADS8317 places the latest data bit on the D_{OUT} line as it is generated; therefore, the converter can easily be *short-cycled*. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ high) after the 14th bit has been clocked out.

This technique can also be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first *n* bits, where *n* might be as low as 3 or 4. This technique results in lower power dissipation in both the converter and the rest of the system because they spend more time in power-down mode.

POWER-ON RESET

The ADS8317 bias circuit is self-starting. There may be a static current (approximately 1.5mA with V_{DD} = 5V) after power-on, unless the circuit is powered down. It is recommended to run a single test conversion (configured the same as any regular conversion) after the power supply reaches at least 2.4V to ensure the device is put into power-down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8317 circuitry. This caution is particularly true if the reference voltage is low and/or the conversion rate is high. At a 250kHz conversion rate, the ADS8317 makes a bit decision every 167ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level, all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high-power devices, to name a few potential sources. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter DCLOCK signal because the phase difference between the glitch and DCLOCK changes with time and temperature, causing sporadic misoperation.

With these considerations in mind, power to the ADS8317 should be clean and well-bypassed. A 0.1μF ceramic bypass capacitor should be placed as close as possible to the ADS8317 package. In addition, a 1μF to 10μF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 47μF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8317 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Texas Instruments' OPA365 op amp provides optimum performance for buffering the signal inputs; the OPA350 can be used to effectively buffer the reference input.

Also, keep in mind that the ADS8317 offers no inherent rejection of noise or voltage variation in regards to the reference input. This characteristic is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out, as described in the previous paragraph, voltage variation resulting from the line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin on the ADS8317 should be placed on a clean ground point. In many cases, this point is the analog ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figure 45 shows an example of a basic data acquisition system. The ADS8317 input range is connected to 2.5V or 4.096V. The 5Ω resistor and 1μF to 10μF capacitor filters the microcontroller noise on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of noise. Operational amplifiers and voltage reference are connected to the analog power supply, AV_{DD}.

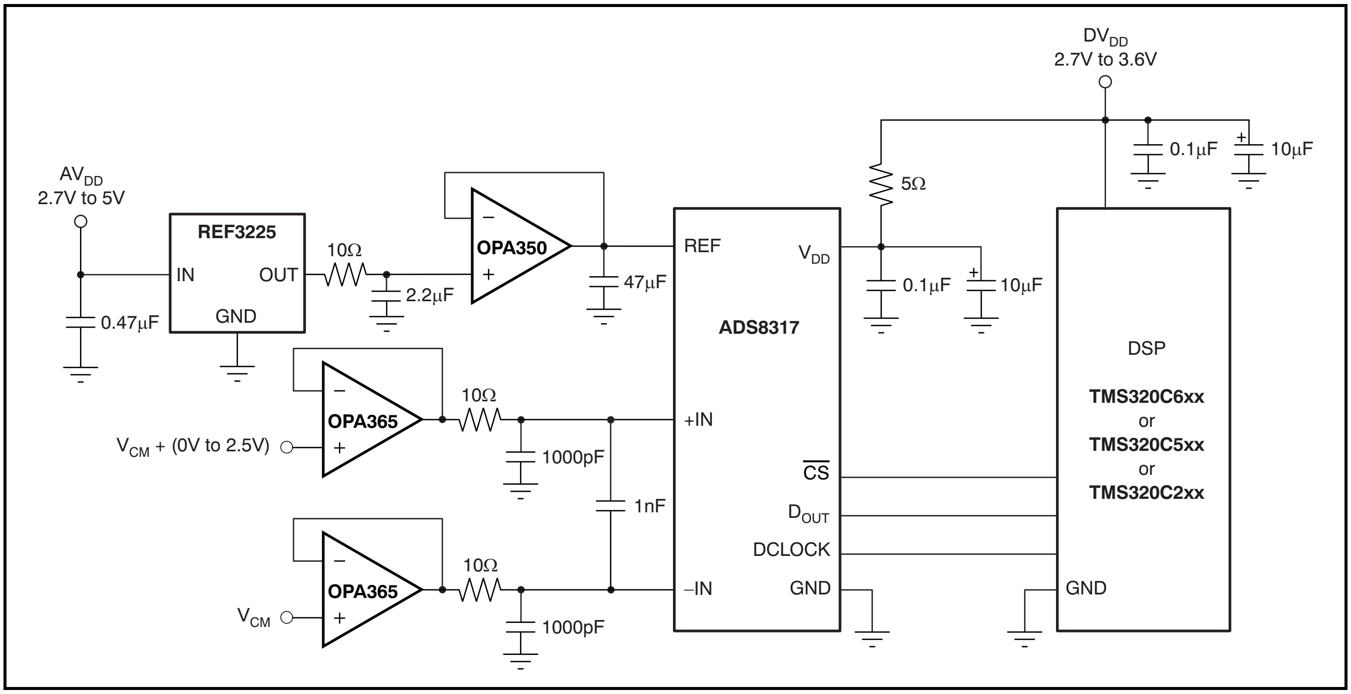


Figure 45. Example of a Basic Data Acquisition System

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2008) to Revision D **Page**

- Changed SON-8 (DRB) package availability ... 1
- Deleted lead temperature specification ... 2
- Added missing mu symbol to High-level output voltage test condition ... 4
- Added missing mu symbol to Low-level output voltage test condition ... 4
- Changed X-axis unit from mA to µA in Figure 10 ... 11
- Changed Figure 38 ... 17
- Changed Figure 39 ... 17
- Changed Figure 40 title (typo) ... 17
- Added missing mu symbol to the value of the LSB, 76.3V ... 18

Changes from Revision B (May 2008) to Revision C **Page**

- Changed 2nd timing diagram from the top in Figure 1 ... 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8317IBDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IBDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IBDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IBDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D17	Samples
ADS8317IDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D17	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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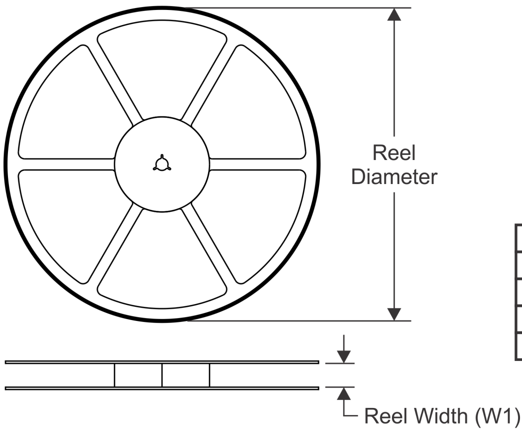
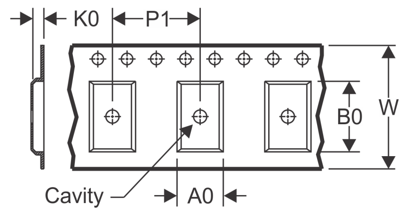
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

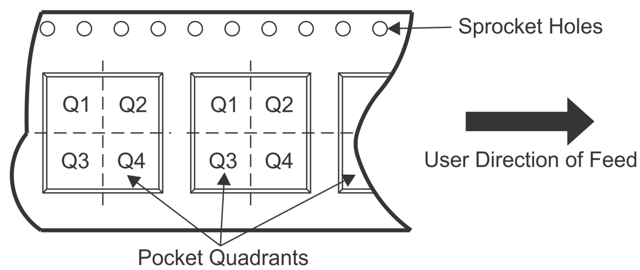


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

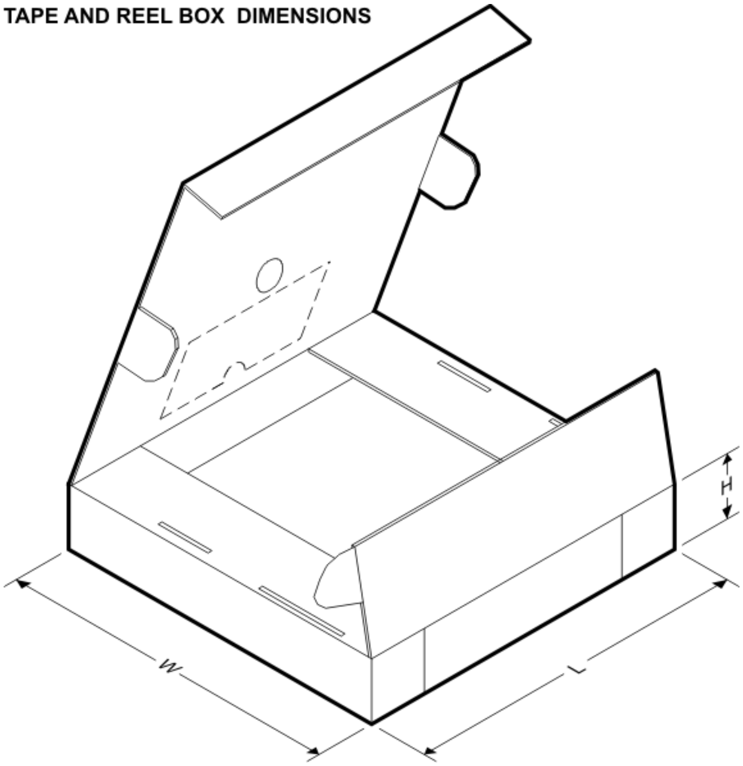
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8317IBDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8317IBDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8317IBDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8317IBDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8317IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8317IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8317IDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8317IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

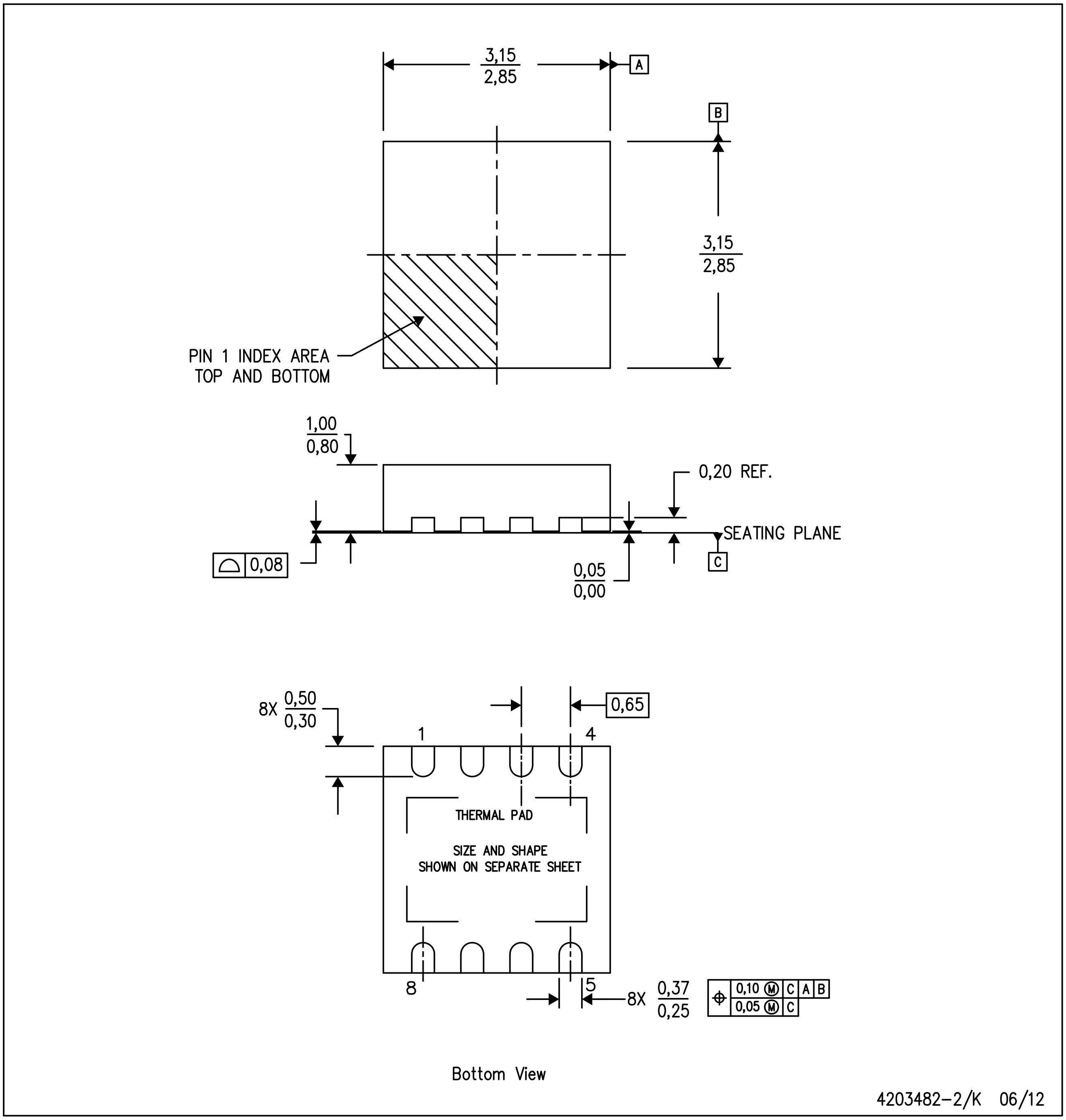
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8317IBDGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
ADS8317IBDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8317IBDRBR	SON	DRB	8	3000	336.6	336.6	28.6
ADS8317IBDRBT	SON	DRB	8	250	210.0	185.0	35.0
ADS8317IDGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
ADS8317IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8317IDRBR	SON	DRB	8	3000	336.6	336.6	28.6
ADS8317IDRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

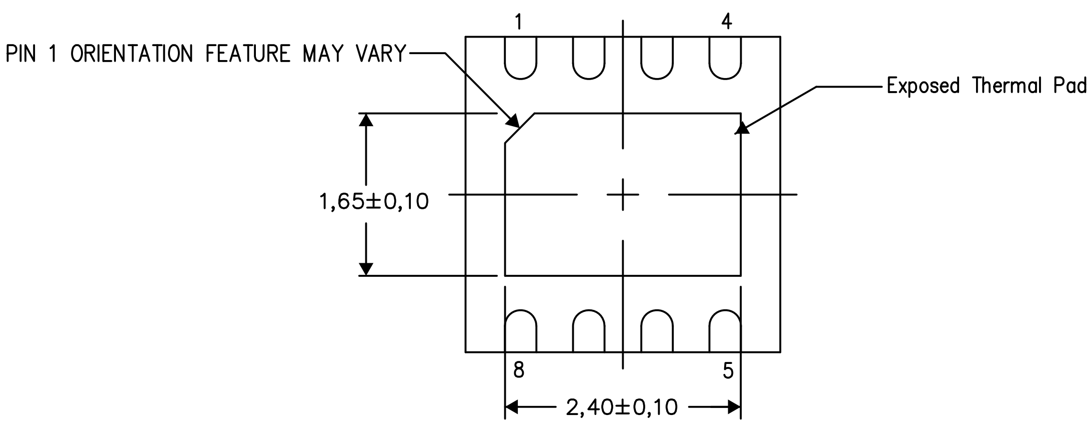
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



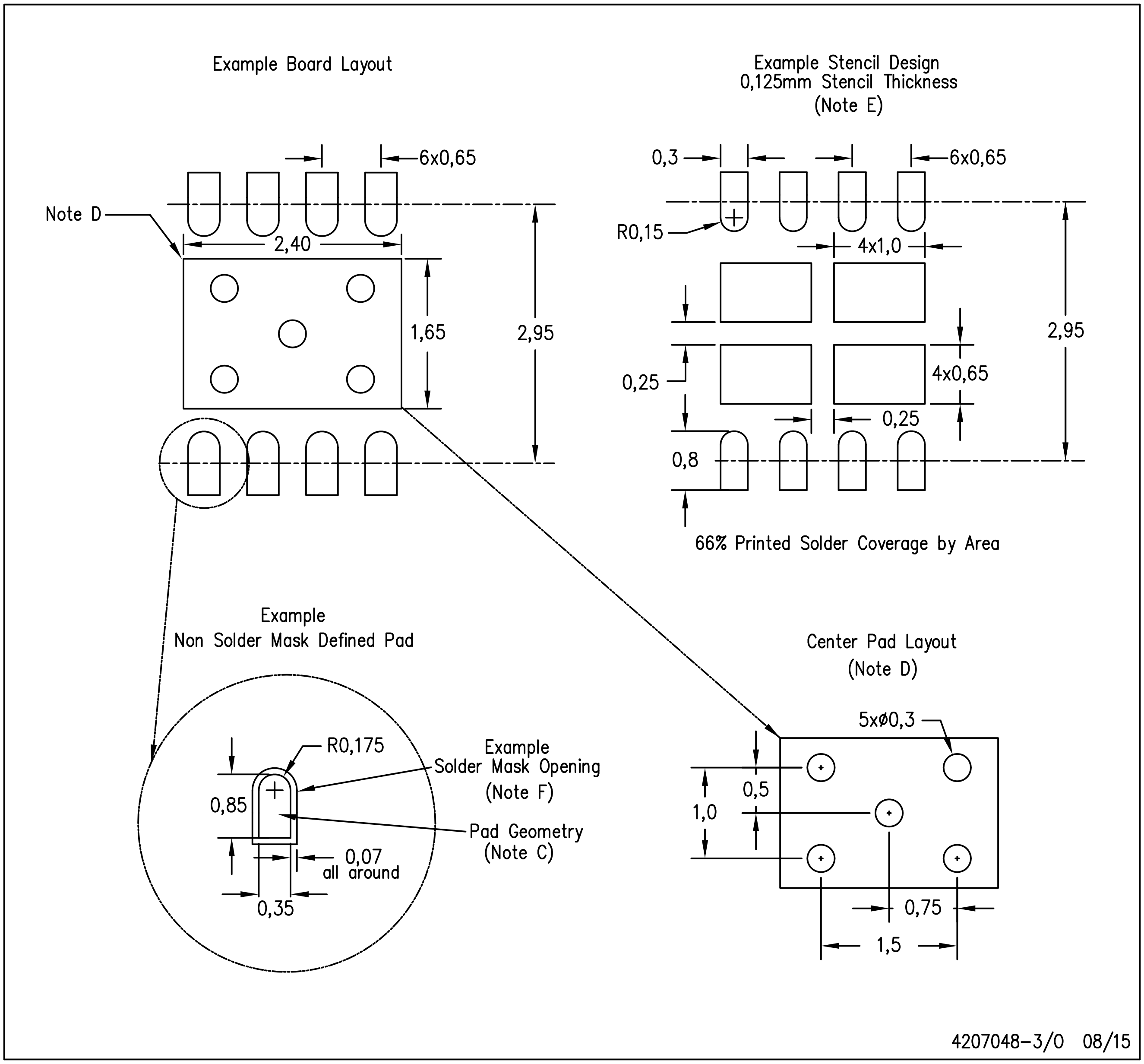
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/T 08/15

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

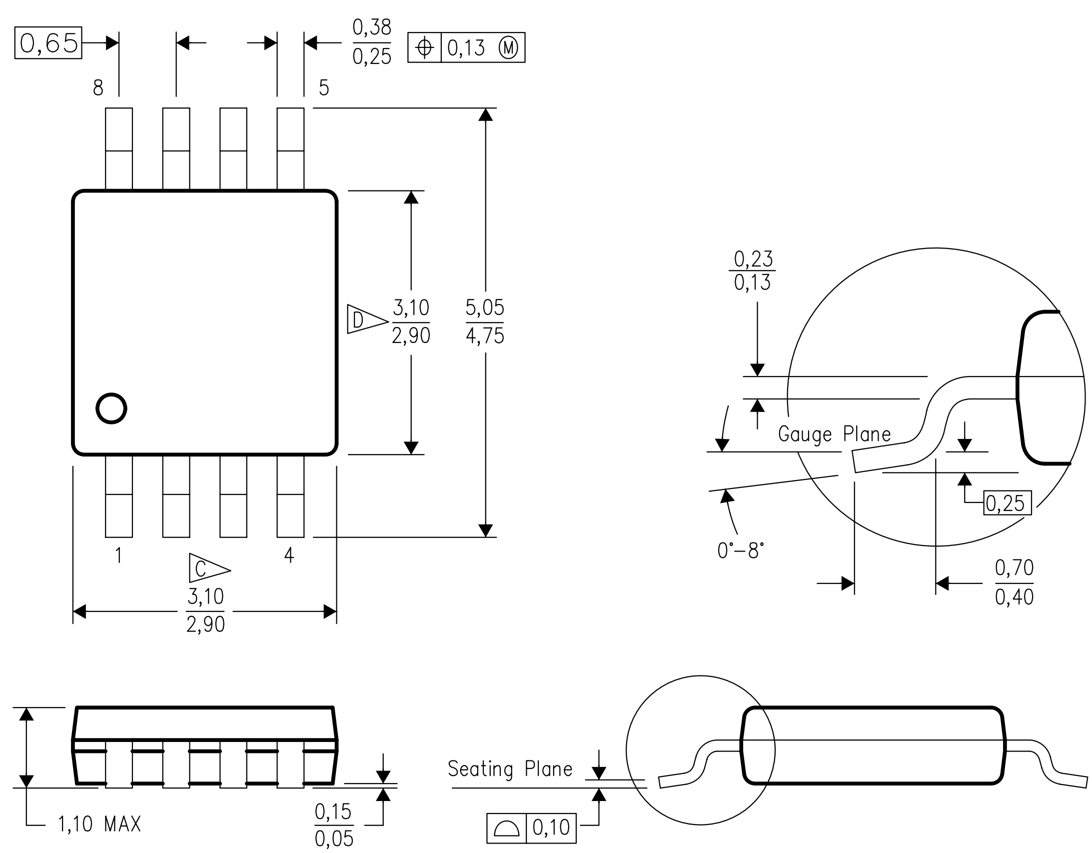
C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances.

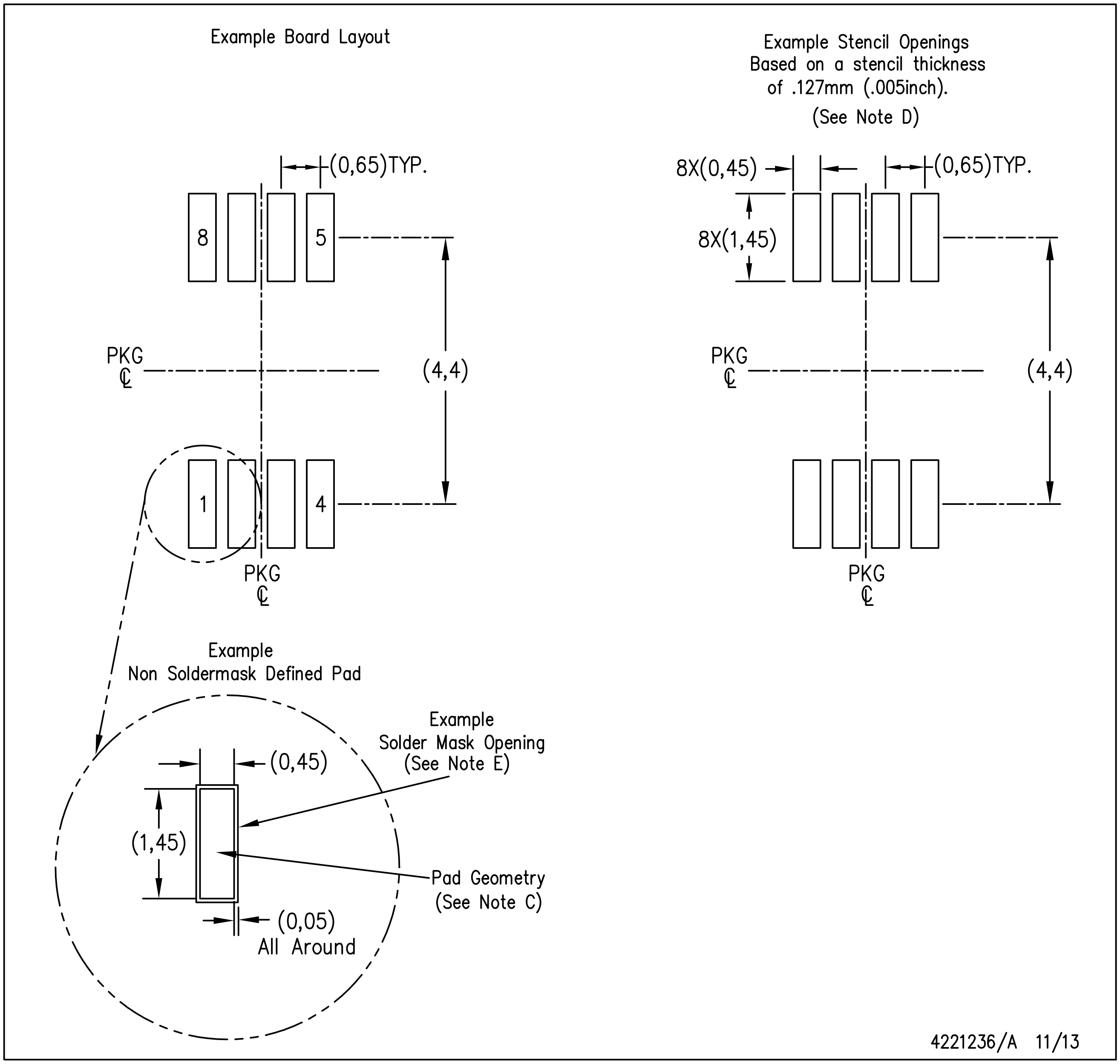
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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