ADC12048 12-Bit Plus Sign 216 kHz 8-Channel Sampling Analog-to-Digital Converter

Check for Samples: ADC12048

FEATURES

- **8-Channel Programmable Differential or Single-Ended Multiplexer**
- **Programmable Acquisition Times and User-Controllable Throughput Rates**
- **Programmable Data Bus Width (8/13 bits)**
- **Built-in Sample-and-Hold**
- **Programmable Auto-Calibration and Auto-Zero cycles**
- **Low Power Standby Mode**
- **No Missing Codes**

APPLICATIONS

- **Medical Instrumentation**
- **Process Control Systems**
- **Test Equipment**
- **Data Logging**
- **Inertial Guidance**

KEY SPECIFICATIONS

- **(f_{CLK} = 12 MHz)**
- **Resolution: 12-Bits + Sign**
- **13-Bit Conversion Time: 3.6 µs, Max**
- **13-Bit Throughput Rate: 216 ksamples/s, Min**
- **Integral Linearity Error (ILE): ±1 LSB, Max**
- **Single Supply: +5 V ±10%**
- **V_{IN} Range: GND to V_A+**
- **Power Consumption**
  - **Normal Operation: 34 mW, Max**
  - **Stand-By Mode: 75 µw, Max**

DESCRIPTION

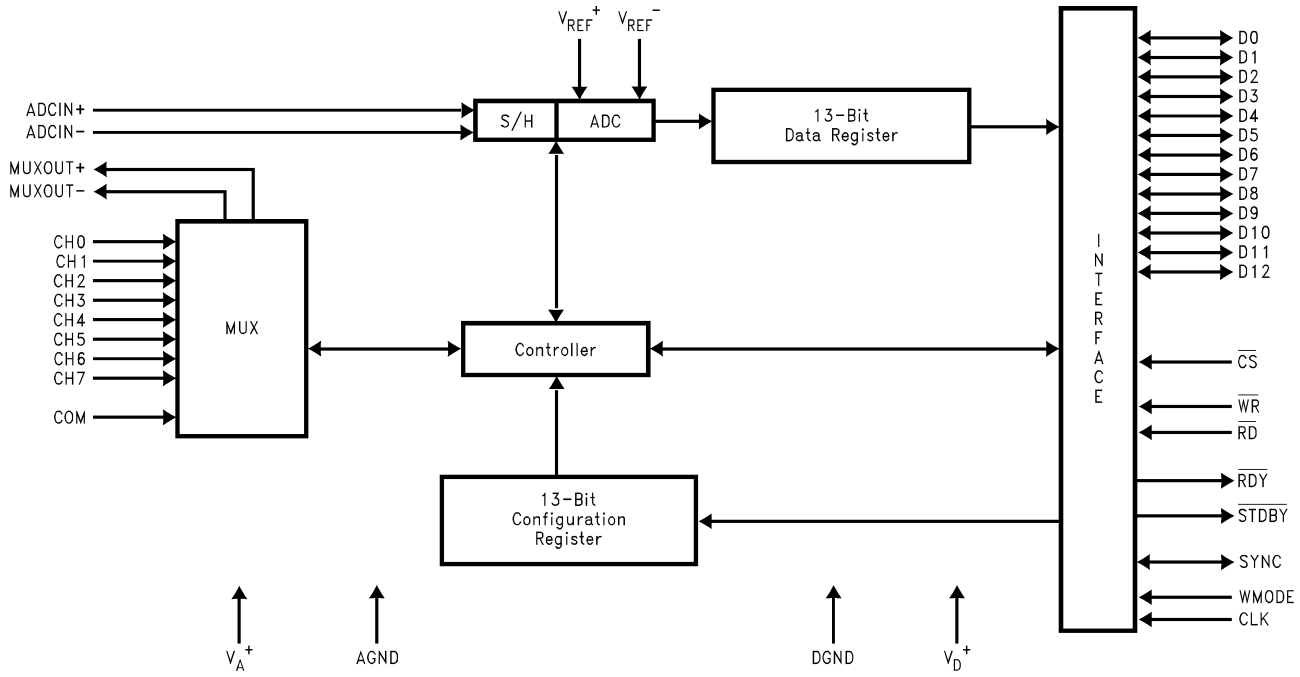
Operating from a single 5V power supply, the ADC12048 is a 12 bit + sign, parallel I/O, self-calibrating, sampling analog-to-digital converter (ADC) with an eight input fully differential analog multiplexer. The maximum sampling rate is 216 kHz. On request, the ADC goes through a self-calibration process that adjusts linearity, zero and full-scale errors.

The ADC12048's 8-channel multiplexer is software programmable to operate in a variety of combinations of single-ended, differential, or pseudo-differential modes. The fully differential MUX and the 12-bit + sign ADC allows for the difference between two signals to be digitized.

The ADC12048 can be configured to work with many popular microprocessors/microcontrollers and DSPs including TI's HPC family, Intel386 and 8051, TMS320C25, Motorola MC68HC11/16, Hitachi 64180 and Analog Devices ADSP21xx.

For complementary voltage references see the LM4040, LM4041 or LM9140.

Block Diagram



Connection Diagrams

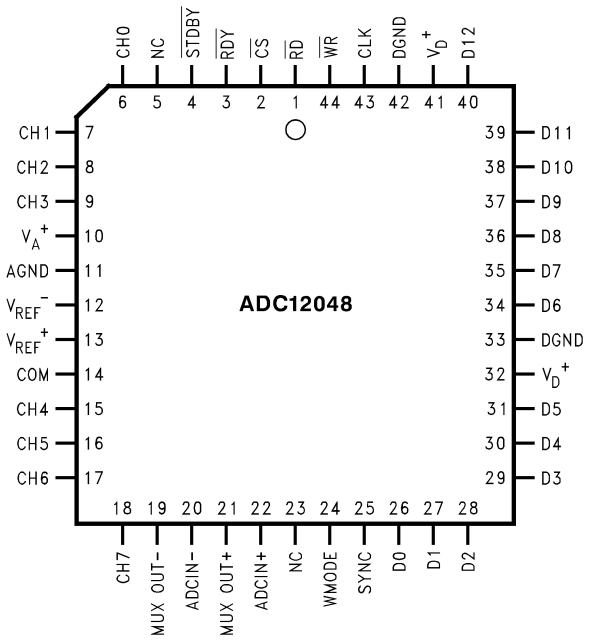


Figure 1. PLCC Package
See Package Number FN0044A

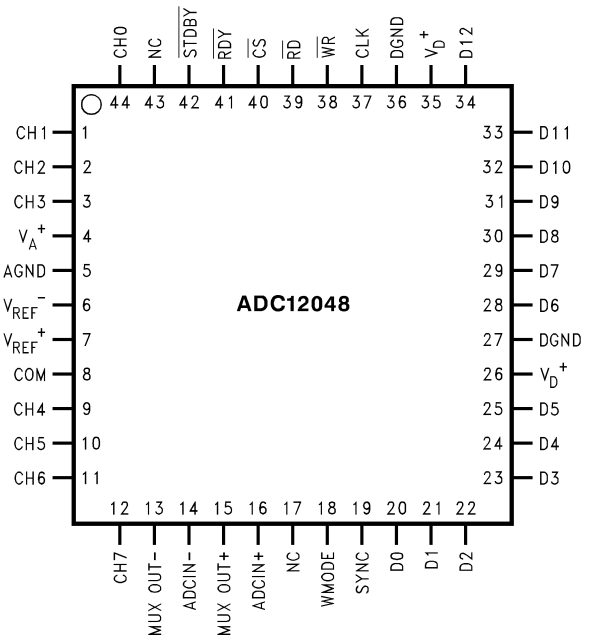


Figure 2. LQFP Package
See Package Number PGB0044A

PIN DESCRIPTION

PLCC Pkg. Pin Number	PQFP Pkg. Pin Number	Pin Name	Description
6 7 8 9 15 16 17 18	44 1 2 3 9 10 11 12	CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7	The eight analog inputs to the Multiplexer. Active channels are selected based on the contents of bits b3–b0 of the Configuration register. Refer to INPUT MULTIPLEXER for more details.
14	8	COM	This pin is another analog input pin used as a pseudo ground when the multiplexer is configured in single-ended mode.
13	7	$V_{REF}+$	Positive reference input. The operating voltage range for this input is $1V \le V_{REF}+ \le V_A+$ (see Figure 7 and Figure 8). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitors. The capacitors should be placed as close to the part as possible.
12	6	$V_{REF}-$	Negative reference input. The operating voltage range for this input is $0V \le V_{REF}- \le V_{REF}+ -1$ (see Figure 7 and Figure 8). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
19 21	13 15	MUX OUT− MUX OUT+	The inverting (negative) and non-inverting (positive) outputs of the multiplexer. The analog inputs to the MUX selected by bits b3–b0 of the Configuration register appear at these pins.
20 22	14 16	ADCIN− ADCIN+	ADC inputs. The inverting (negative) and non-inverting (positive) inputs into the ADC.
24	18	WMODE	The logic state of this pin at power-up determines which edge of the write signal ($\overline{WR}$) will latch in data from the data bus. If tied low, the ADC12048 will latch in data on the **rising** edge of the $\overline{WR}$ signal. If tied to a logic **high**, data will he latched in on the **falling** edge of the $\overline{WR}$ signal. The state of this pin should not be changed after power-up.
25	19	SYNC	The SYNC pin can be programmed as an **input** or an **output**. The Configuration register's bit b8 controls the function of this pin. When programmed as an **input** pin (b8 = 1), a rising edge on this pin causes the ADC's sample-and-hold to hold the analog input signal and begin conversion. When programmed as an **output** pin (b8 = 0), the SYNC pin goes high when a conversion begins and returns low when completed.
26–31 34–40	20–25 29–34	D0–D5 D6–D12	13-bit Data bus of the ADC12048. D12 is the most significant bit and D0 is the least significant. The BW (bus width) bit of the Configuration register (b12) selects between an 8-bit or 13-bit data bus width. When the **BW** bit is **cleared** (BW = 0), D7–D0 are active and D12–D8 are always in TRI-STATE. When the **BW** bit is **set** (BW = 1), D12–D0 are active.
43	37	CLK	The clock input pin used to drive the ADC12048. The operating range is 0.05 MHz to 12 MHz.
44	38	$\overline{WR}$	$\overline{WR}$ is the active low WRITE control input pin. A logic low on this pin and the $\overline{CS}$ will enable the input buffers of the data pins D12–D0. The signal at this pin is used by the ADC12048 to latch in data on D12–D0. The sense of the WMODE pin at power-up will determine which edge of the $\overline{WR}$ signal the ADC12048 will latch in data. See WMODE pin description.
1	39	$\overline{RD}$	$\overline{RD}$ is the active low read control input pin. A logic low on this pin and $\overline{CS}$ will enable the active output buffers to drive the data bus.
2	40	$\overline{CS}$	$\overline{CS}$ is the active low Chip Select input pin. Used in conjunction with the $\overline{WR}$ and $\overline{RD}$ signals to control the active data bus input/output buffers of the data bus.
3	41	$\overline{RDY}$	$\overline{RDY}$ is an active low output pin. The signal at this pin indicates when a requested function has begun or ended. Refer to Functional Description and Digital Timing Diagrams for more detail.
4	42	$\overline{STDBY}$	This is the standby active low output pin. This pin is low when the ADC12048 is in the standby mode and high when the ADC12048 is out of the standby mode or has been requested to leave the standby mode.

PIN DESCRIPTION (continued)

PLCC Pkg. Pin Number	PQFP Pkg. Pin Number	Pin Name	Description
10	4	V_A+	Analog supply input pin. The device operating supply voltage range is +5V ±10%. Accuracy is ensured only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to AGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.
11	5	AGND	Analog ground pin. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.
32 and 41	26 and 35	V_D+	Digital supply input pins. The device operating supply voltage range is +5V ±10%. Accuracy is ensured only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to DGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.
33 and 42	27 and 36	DGND	Digital ground pin. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_A+ and V_D+)			6.0V
Voltage at all Inputs			−0.3V to V^+ + 0.3V
$\|V_A+ - V_D+\|$			300 mV
|AGND − DGND|			300 mV
Input Current at Any Pin[4]			±30 mA
Package Input Current[4]			±120 mA
Power Dissipation at T_A = 25°C[5]			875 mW
Storage Temperature			−65°C to +150°C
Lead Temperature	PGB Package	Vapor Phase (60 sec.)	210°C
		Infared (15 sec.)	220°C
	FN Package	Infared (15 sec.)	300°C
ESD Susceptibility[6]			3.0 kV

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > (V_A+ or V_D+)), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.
(5) The maximum power dissipation must he derated at elevated temperatures and is dictated by T_{Jmax}, (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C, and the typical thermal resistance (θ_{JA}) of the ADC12048 in the FN package, when board mounted, is 55°C/W, and in the PGB package, when board mounted, is 67.8°C/W.
(6) Human body model, 100 pF discharged through 1.5 kΩ resistor.

Operating Ratings (1)(2)(3)(4)(5)(6)

Temperature Range	($T_{min} \le T_A \le T_{max}$)	−40°C ≤ T_A ≤ 85°C
Supply Voltage	V_A+, V_D+	4.5V to 5.5V
	$\lvert V_A+ - V_D+\rvert$	≤100 mV
|AGND − DGND|		≤100 mV
V_{IN} Voltage Range at all Inputs		GND ≤ V_{IN} ≤ V_A+
V_{REF}+ Input Voltage		1V ≤ V_{REF}+ ≤ V_A+
V_{REF}− Input Voltage		0 ≤ V_{REF}− ≤ V_{REF}+ − 1V
V_{REF}+ − V_{REF}−		1V ≤ V_{REF} ≤ V_A+
V_{REF} Common Mode (7)		0.1 V_A+ ≤ V_{REFCM} ≤ 0.6 V_A+

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise specified.
(3) Each input and output is protected by a nominal 6.5V breakdown voltage zener diode to GND; as shown below, input voltage magnitude up to 0.3V above V_A+ or 0.3V below GND will not damage the ADC12048. There are parasitic diodes that exist between the inputs and the power supply rails and errors in the A/D conversion can occur if these diodes are forward biased by more than 50 mV. As an example, if V_A+ is 4.50 V_{DC}, full-scale input voltage must be ≤ 4.55 V_{DC} to ensure accurate conversions. See Figure 3
(4) V_A+ and V_D+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy. Refer to POWER SUPPLY CONSIDERATIONS section for a detailed discussion.
(5) Accuracy is ensured when operating at f_{CLK} = 12 MHz.
(6) With the test condition for V_{REF} (V_{REF}+ − V_{REF}−) given as +4.096V, the 12-bit LSB is 1.000 mV.
(7) V_{REFCM} (Reference Voltage Common Mode Range) is defined as $\left(\frac{V_{REF}^+ + V_{REF}^-}{2}\right)$

Converter DC Characteristics

The following specifications apply to the ADC12048 for V_A+ = V_D+ = 5V, V_{REF}+ = 4.096V, V_{REF}− = 0.0V, 12-bit + sign conversion mode, f_{CLK} = 12.0 MHz, R_S = 25Ω, source impedance for V_{REF}+ and V_{REF}− ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage (V_{INCM}), and minimum acquisition time, unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
	Resolution with No Missing Codes	After Auto-Cal		**13**	Bits (max)
ILE	Integral Linearity Error	After Auto-Cal (3)(4)	±0.6	**±1**	LSB (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Zero Error	After Auto-Cal (5)(4)			
		V_{INCM} = 5.0V		**±5.5**	LSB (max)
		V_{INCM} = 2.048V		**±2.5**	LSB (max)
		V_{INCM} = 0V		**±5.5**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (3)(4)	±1.0	**±2.5**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (3)(4)	±1.0	**±2.5**	LSB (max)
	DC Common Mode Error	After Auto-Ca (6)	±2	**±5.5**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (7)	±1		LSB

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).
(3) Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero.
(4) The ADC12048's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainly of ±0.20 LSB.
(5) Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between −1 to 0 and 0 to +1 (see Figure 12).
(6) The DC common-mode error is measured with both inputs shorted together and driven from 0V to 5V. The measured value is referred to the resulting output value when the inputs are driven with a 2.5V input.
(7) Total Unadjusted Error (TUE) includes offset, full scale linearity and MUX errors.

Power Supply Characteristics

The following specifications apply to the ADC12048 for $V_A+ = V_D+ = 5V$, $V_{REF}+ = 4.096V$, $V_{REF}- = 0.0V$, 12-bit + sign conversion mode, $f_{CLK} = 12.0$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}-$ ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage, and minimum acquisition time, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
PSS	Power Supply Sensitivity	$V_D+ = V_A+ = 5.0V$ ±10% (3)			
	Zero Error	$V_{REF}+ = 4.096V$	±0.1		LSB
	Full-Scale Error	$V_{REF}- = 0V$	±0.5		LSB
	Linearity Error		±0.1		LSB
I_D+	V_D+ Digital Supply Current	Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13.			
		$f_{CLK} = 12.0$ MHz, Reset Mode	850		µA
		$f_{CLK} = 12.0$ MHz, Conversion	2.45	**2.8**	mA (max)
I_A+	V_A+ Analog Supply Current	Start Command (Performing a conversion) with SYNC configured as an input and driven with a 214 kHz signal. Bus width set to 13.			
		$f_{CLK} = 12.0$ MHz, Reset Mode	2.3		mA
		$f_{CLK} = 12.0$ MHz, Conversion	2.3	**4.0**	mA (max)
I_{ST}	Standby Supply Current	Standby Mode			
	($I_D+ + I_A+$)	f_{CLK} = Stopped	5	**15**	µA (max)
		$f_{CLK} = 12.0$ MHz	100	**120**	µA (max)

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).
(3) Power Supply Sensitivity is measured after an Auto-Zero and Auto Calibration cycle has been completed with V_A+ and V_D+ at the specified extremes.

Analog MUX Inputs Characteristics

The following specifications apply to the ADC12048 for $V_A+ = V_{D+} = 5V$, $V_{REF}+ = 4.096V$, $V_{REF}- = 0.0V$, 12-Bit + sign conversion mode, $f_{CLK} = 12.0$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}+$ ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage, and minimum acquisition time, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
I_{ON}	MUX ON Channel Leakage Current	ON Channel = 5V, OFF Channel = 0V	0.05	**1.0**	µA (min)
		ON Channel = 0V, OFF Channel = 5V	−0.05	**−1.0**	µA (max)
I_{OFF}	MUX OFF Channel Leakage Current	ON Channel = 5V, OFF Channel = 0V	0.05	**1.0**	µA (min)
		ON Channel = 0V, OFF Channel = 5V	−0.05	**−1.0**	µA (max)
I_{ADCIN}	ADCIN Input Leakage Current		0.05	**2.0**	µA (max)
R_{ON}	MUX On Resistance	$V_{IN} = 2.5V$	310	**500**	Ω (max)
	MUX Channel-to-Channel R_{ON} Matching	$V_{IN} = 2.5V$	±20%		Ω
C_{MUX}	MUX Channel and COM Input Capacitance		10		pF
C_{ADC}	ADCIN Input Capacitance		70		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

Reference Inputs

The following specifications apply to the ADC12048 for $V_A+ = V_D+ = 5V$, $V_{REF}+ = 4.096V$, $V_{REF}- = 0.0V$, 12-bit + sign conversion mode, $f_{CLK} = 12.0$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}-$ ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage, and minimum acquisition time, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
I_{REF}	Reference Input Current	$V_{REF}+$ 4.096V, V_{REF-} = 0V			
		Analog Input Signal: 1 kHz (3)	145		µA
		80 kHz	136		µA
C_{REF}	Reference Input Capacitance		85		pF

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).
(3) The reference input current is a DC average current drawn by the reference input with a full-scale sinewave input. The ADC12048 is continuously converting with a throughput rate of 206 kHz.

Digital Logic Input/Output Characteristics

The following specifications apply to the ADC12048 for $V_A+ = V_D+ = 5V$, $V_{REF}+ = 4.096V$, $V_{REF}- = 0.0V$, 12-bit + sign conversion mode, $f_{CLK} = 12.0$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}-$ ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage, and minimum acquisition time, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
V_{IH}	Logic High Input Voltage	$V_A+ = V_D+ = 5.5V$		**2.0**	V (min)
V_{IL}	Logic Low Input Voltage	$V_A+ = V_D+ = 4.5V$		**0.8**	V (max)
I_{IH}	Logic High Input Current	$V_{IN} = 5V$	0.035	**2.0**	µA (max)
I_{IL}	Logic Low Input Current	$V_{IN} = 0V$	−0.035	**−2.0**	µA (max)
V_{OH}	Logic High Output Voltage	$V_A+ = V_D+ = 4.5V$ $I_{OUT} = -1.6$ mA		**2.4**	V (min)
V_{OL}	Logic Low Output Voltage	$V_A+ = V_D+ = 4.5V$ $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OFF}	TRI-STATE Output Leakage Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$		**±2.0**	µA (max)
C_{IN}	D12–D0 Input Capacitance		10		pF

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

Converter AC Characteristics

The following specifications apply to the ADC12048 for $V_S+ = V_D+ = 5V$, $V_{REF}+ = 4.096V$, $V_{REF}- = 0.0V$, 12-bit + sign conversion mode, $f_{CLK} = 12.0$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}-$ ≤ 1Ω, fully differential input with fixed 2.048V common-mode voltage, and minimum acquisition time, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Unit (Limit)
t_Z	Auto Zero Time		78	**78 clks + 120 ns**	clks (max)
t_{CAL}	Full Calibration Time		4946	**4946 clks + 120 ns**	clks (max)
	CLK Duty Cycle		50		%
				40	% (min)
				60	% (max)
t_{CONV}	Conversion Time	Sync-Out Mode	44	**44**	clks (max)
$t_{AcqSYNCOUT}$	Acquisition Time (Programmable)	Minimum for 13 Bits	9	**9 clks + 120 ns**	clks (max)
		Maximum for 13 Bits	79	**79 clks + 120 ns**	clks (max)

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

Digital Timing Characteristics

The following specifications apply to the ADC12048, 13-bit data bus width, $V_A+ = V_D+ = 5V$, $f_{CLK} = 12$ MHz, $t_f = 3$ ns and $C_L = 50$ pF on data I/O lines

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limit)
t_{TPR}	Throughput Rate	Sync-Out Mode (SYNC Bit = "0") 9 Clock Cycles of Acquisition Time	222		kHz
t_{CSWR}	Falling Edge of $\overline{CS}$ to Falling Edge of $\overline{WR}$		0		ns
t_{WRCS}	Active Edge of $\overline{WR}$ to Rising Edge of $\overline{CS}$		0		ns
t_{WR}	$\overline{WR}$ Pulse Width		20	**30**	ns (min)
$t_{WRSETFalling}$	Write Setup Time	WMODE = "1"		**20**	ns (min)
$t_{WRHOLDFalling}$	Write Hold Time	WMODE = "1"		**5**	ns (min)
$t_{WRSETRising}$	Write Setup Time	WMODE = "0"		**20**	ns (min)
$t_{WRHOLDRising}$	Write Hold Time	WMODE = "0"		**5**	ns (min)
t_{CSRD}	Falling Edge of $\overline{CS}$ to Falling Edge of $\overline{RD}$		0		ns
t_{RDCS}	Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{CS}$		0		ns
t_{RDDATA}	Falling Edge of $\overline{RD}$ to Valid Data	8-Bit Mode (BW Bit = "0")	40	**58**	ns (max)
t_{RDDATA}	Falling Edge of $\overline{RD}$ to Valid Data	13-Bit Mode (BW Bit = "1")	26	**44**	ns (max)
t_{RDHOLD}	Read Hold Time		23	**32**	ns (max)
t_{RDRDY}	Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{RDY}$		24	**38**	ns (max)
t_{WRRDY}	Active Edge of $\overline{WR}$ to Rising Edge of $\overline{RDY}$	WMODE = "1"	42	**65**	ns (max)
t_{STNDBY}	Active Edge of $\overline{WR}$ to Falling Edge of $\overline{STDBY}$	WMODE = "0". Writing the Standby Command into the Configuration Register	200	**230**	ns (max)
t_{STDONE}	Active Edge of $\overline{WR}$ to Rising Edge of $\overline{STDBY}$	WMODE = "0". Writing the RESET Command into the Configuration Register	30	**45**	ns (max)
t_{STDRDY}	Active Edge of $\overline{WR}$ to Falling Edge of $\overline{RDY}$	WMODE = "0". Writing the RESET Command into the Configuration Register	1.4	**2.5**	ms (max)
t_{SYNC}	Minimum SYNC Pulse Width		5	**10**	ns (min)

(1) Typicals are at $T_A = 25°C$ and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

Digital Timing Diagrams

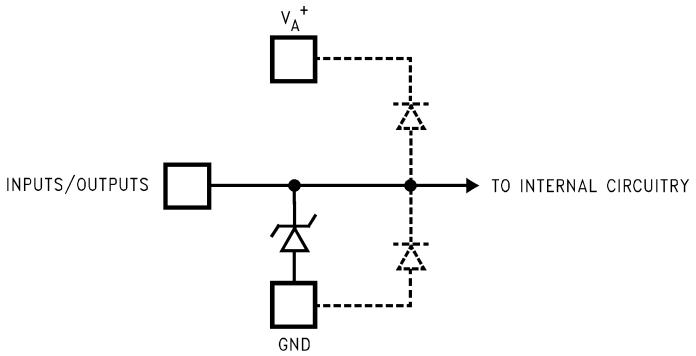


Figure 3.

Figure 4. Electrical Characteristics

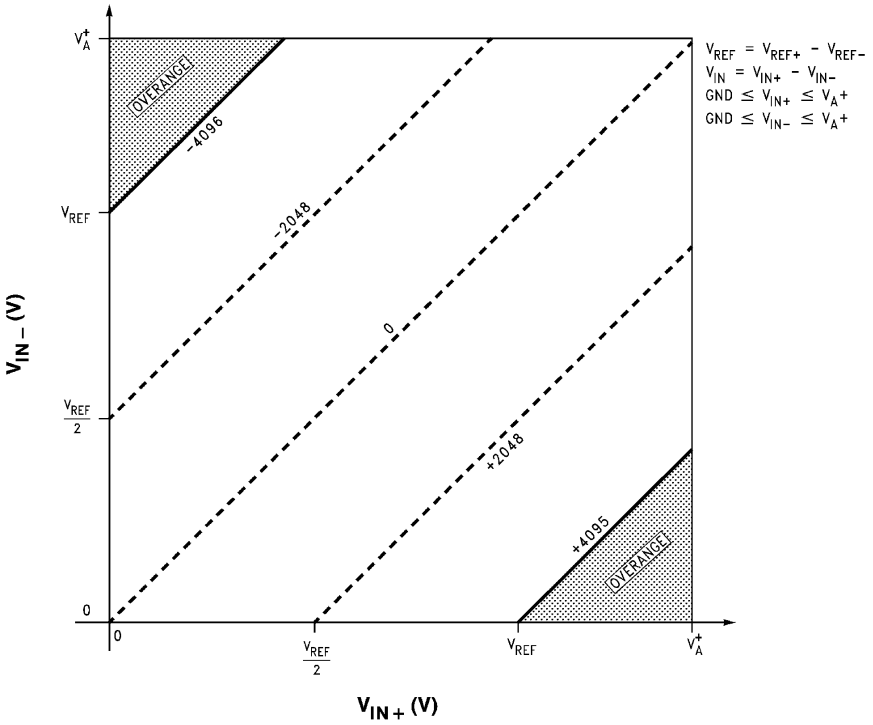


Figure 5. Output Digital Code vs the Operating Input Voltage Range (General Case)

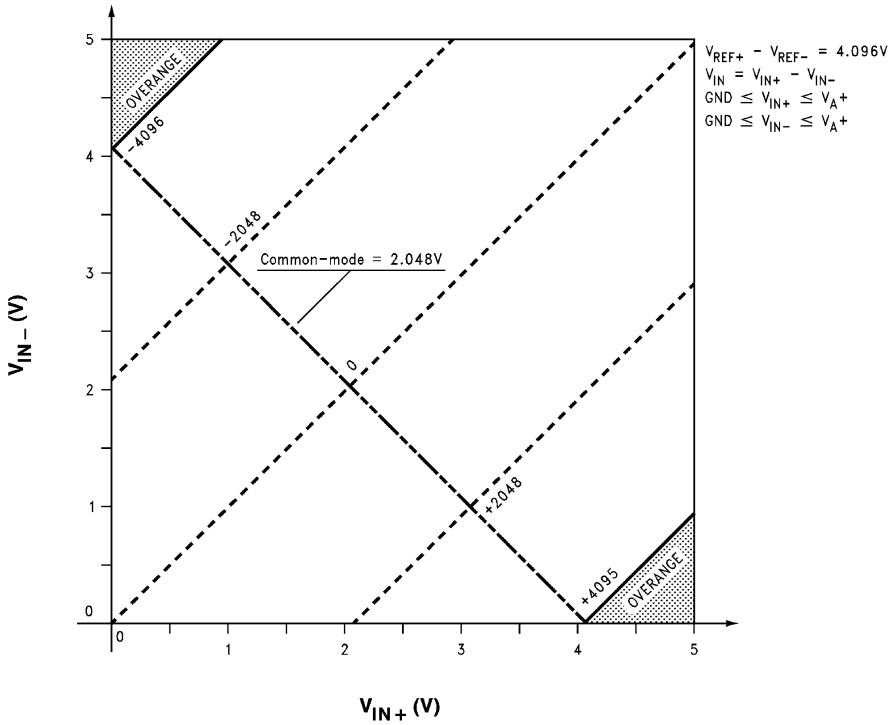


Figure 6. Output Digital Code vs the Operating Input Voltage Range for V_{REF} = 4.096V

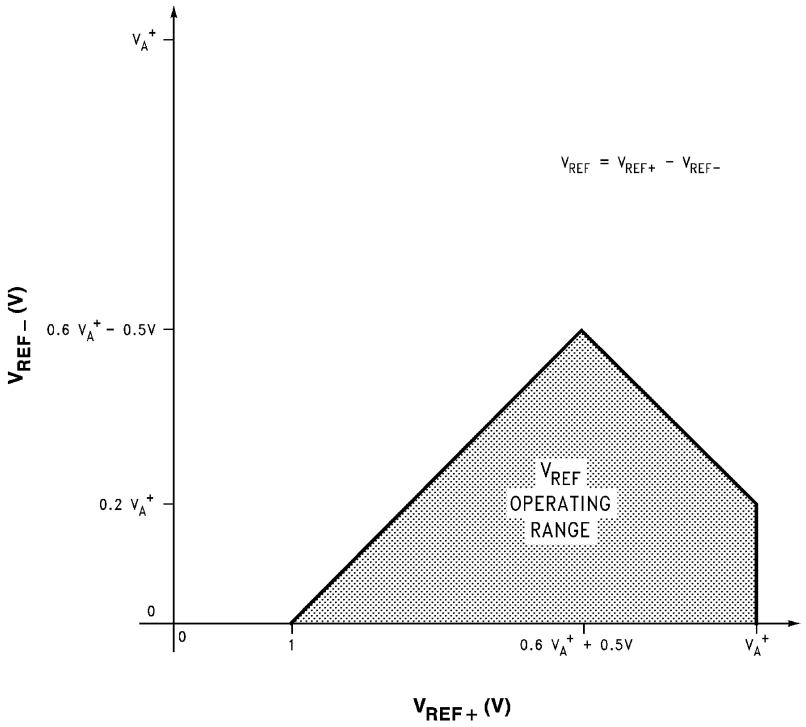


Figure 7. V_{REF} Operating Range (General Case)

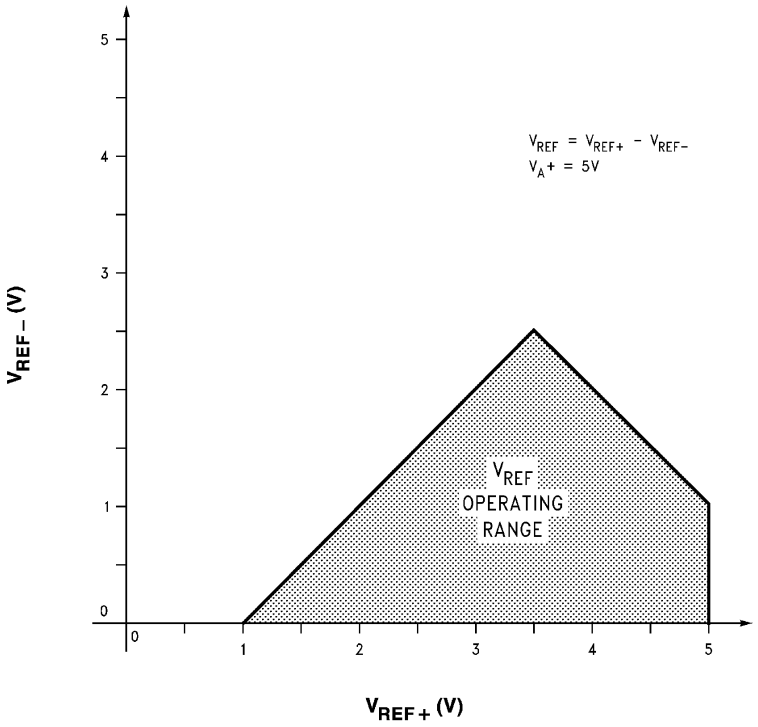


Figure 8. V_{REF} Operating Range for V_A = 5V

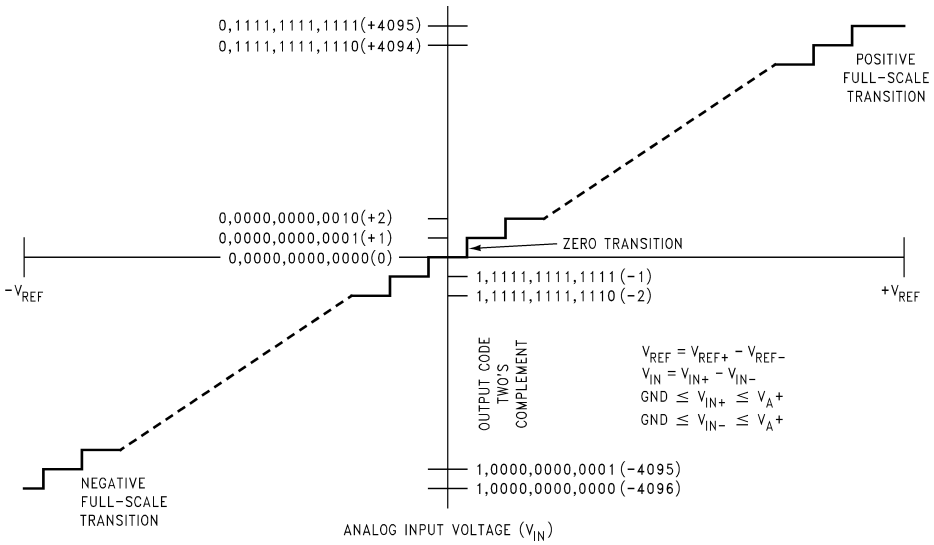


Figure 9. Transfer Characteristic

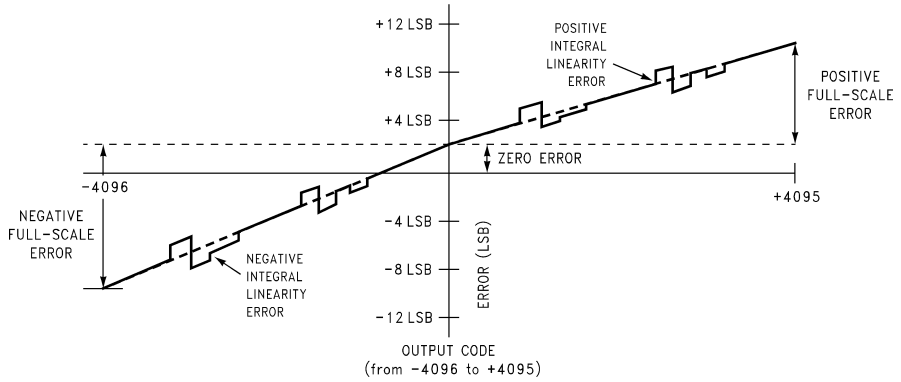


Figure 10. Simplified Error vs Output Code without Auto-Calibration or Auto-Zero Cycles

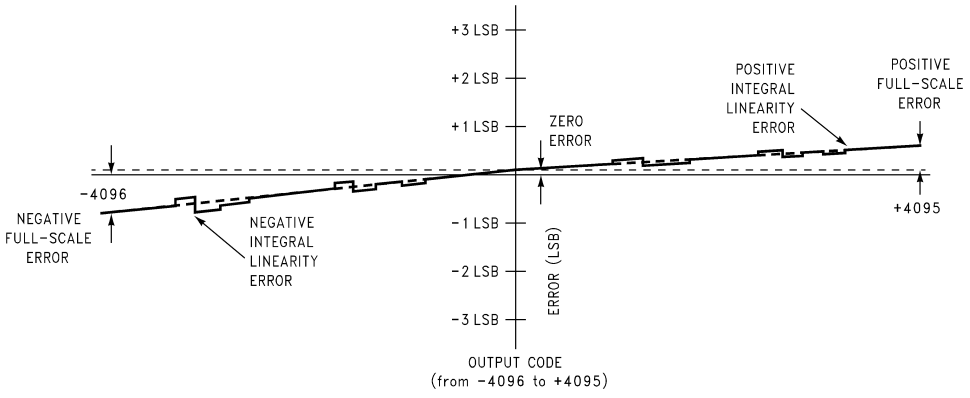


Figure 11. Simplified Error vs Output Code after Auto-Calibration Cycle

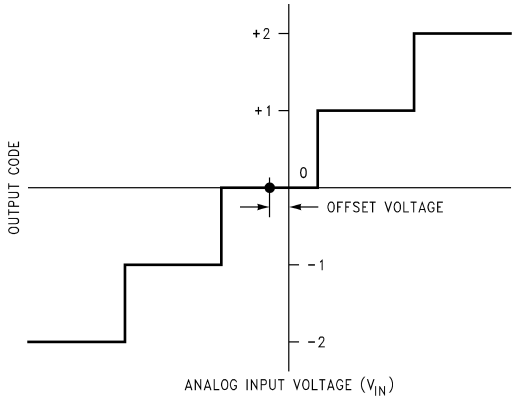


Figure 12. Offset or Zero Error Voltage (3)

Timing Diagrams

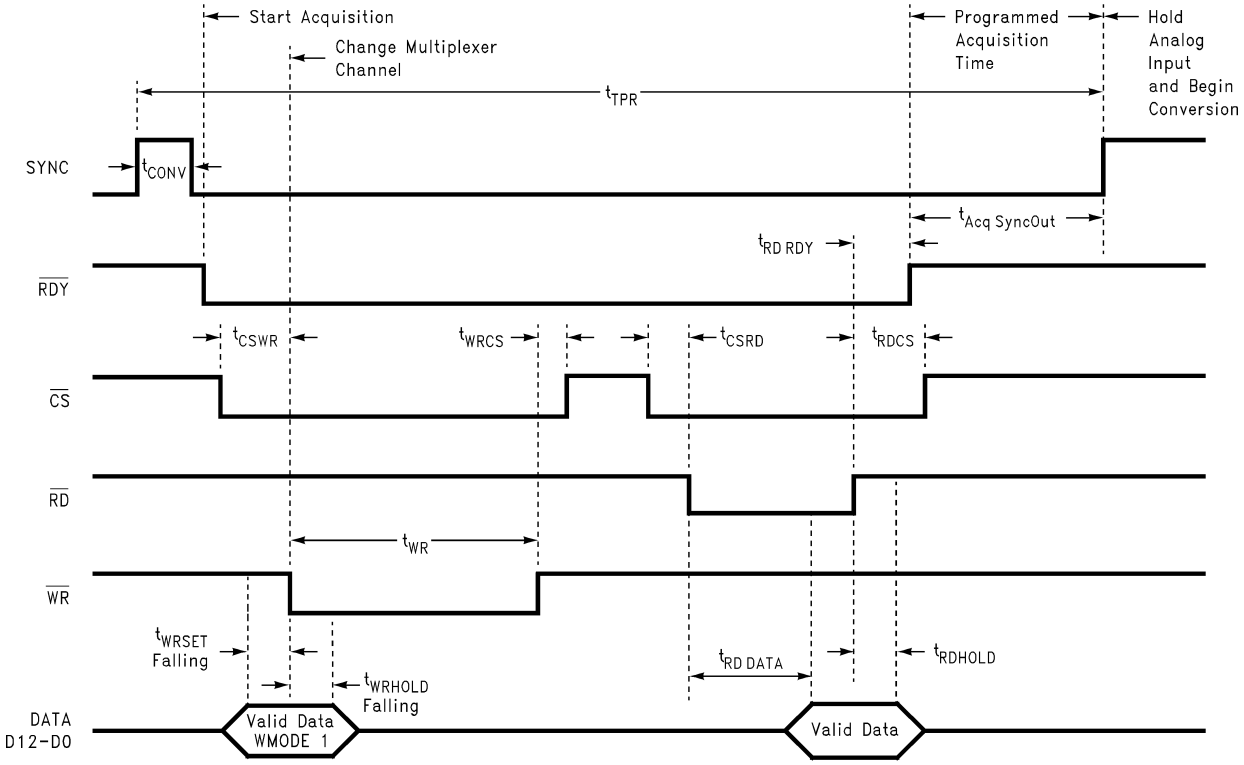


Figure 13. Sync-Out Write (WMODE = 1, BW = 1), Read and Convert Cycles

(3) Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between −1 to 0 and 0 to +1 (see Figure 12).

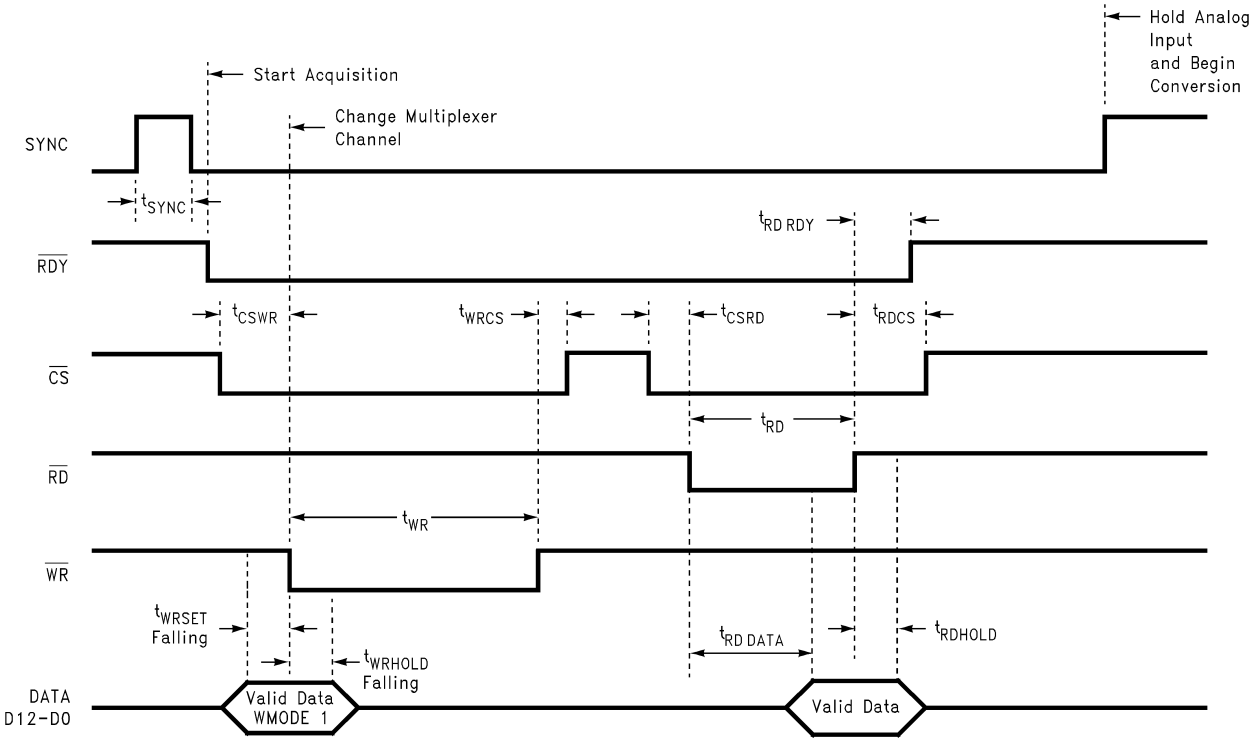


Figure 14. Sync-In Write (WMODE = 1, BW = 1), Read and Convert Cycles

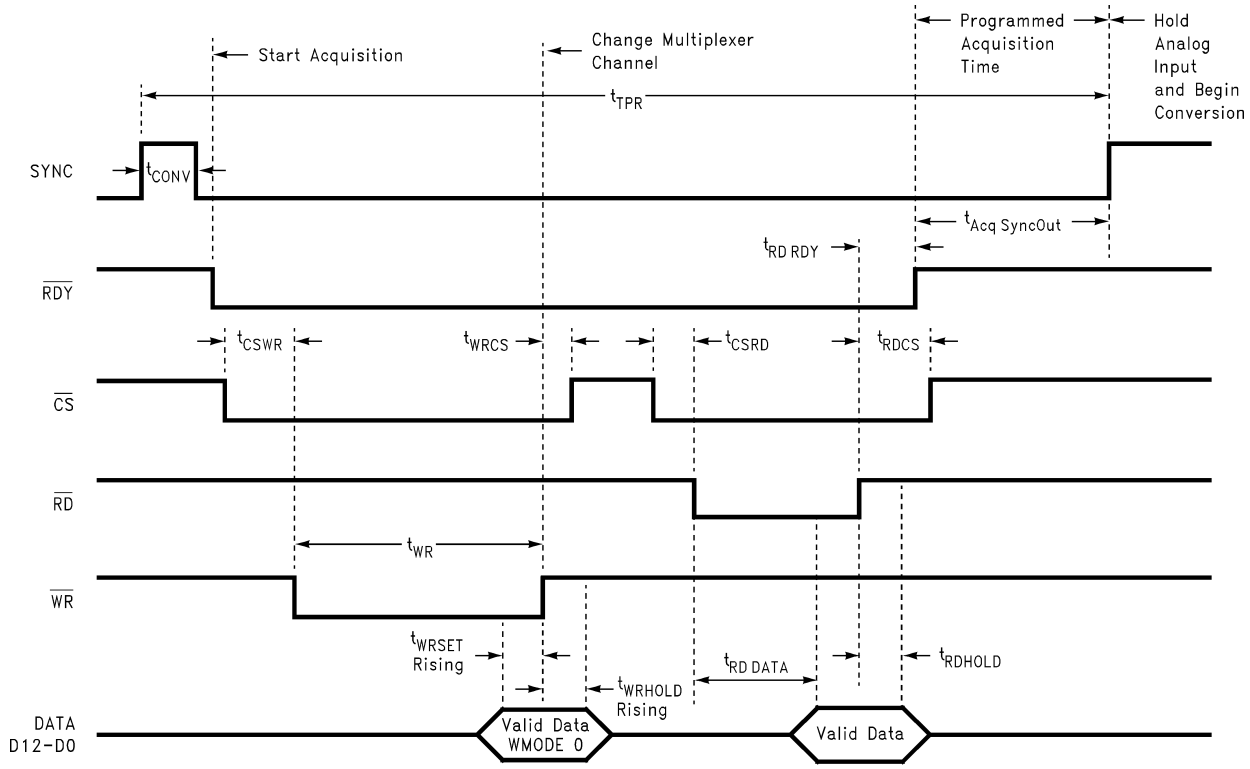


Figure 15. Sync-Out Write (WMODE = 0, BW = 1), Read and Convert Cycles

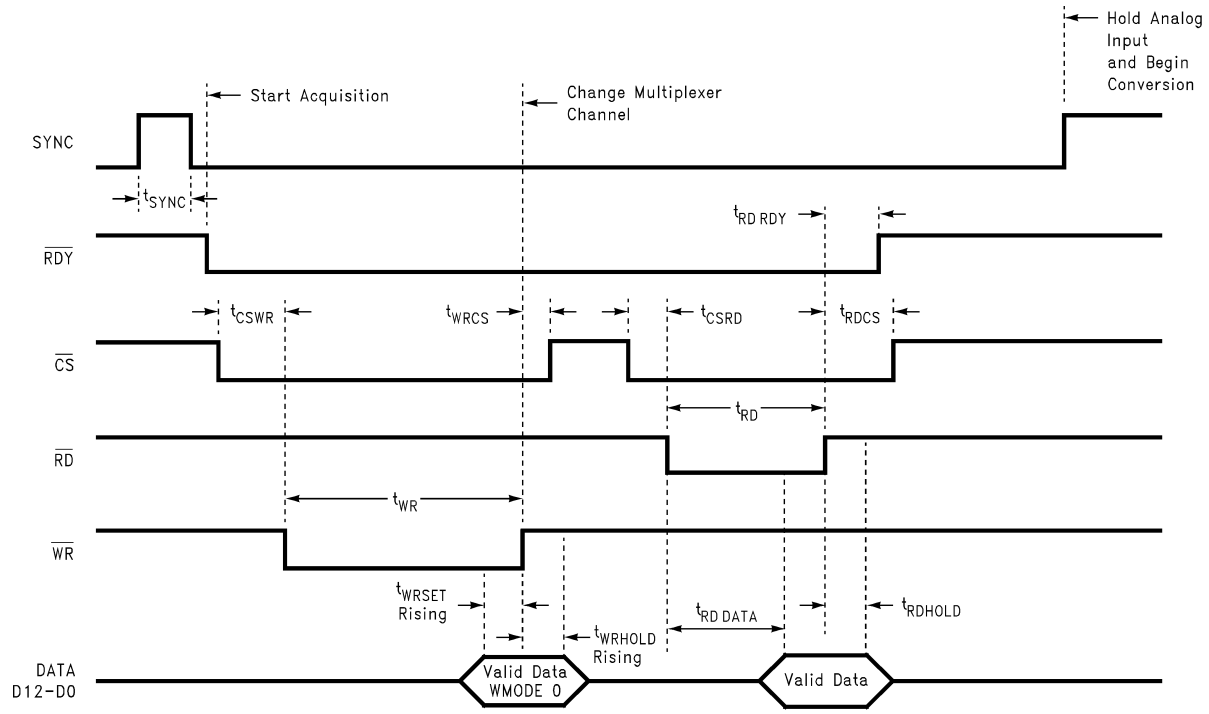
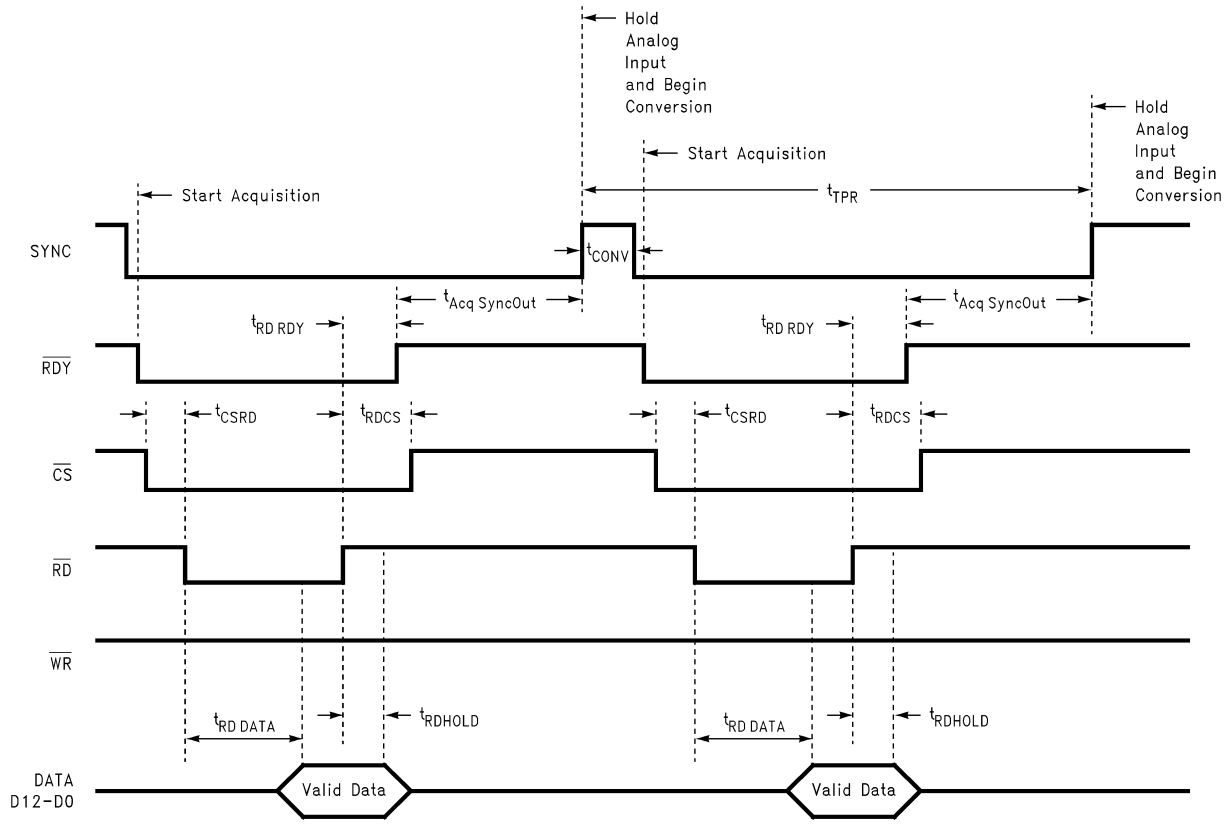
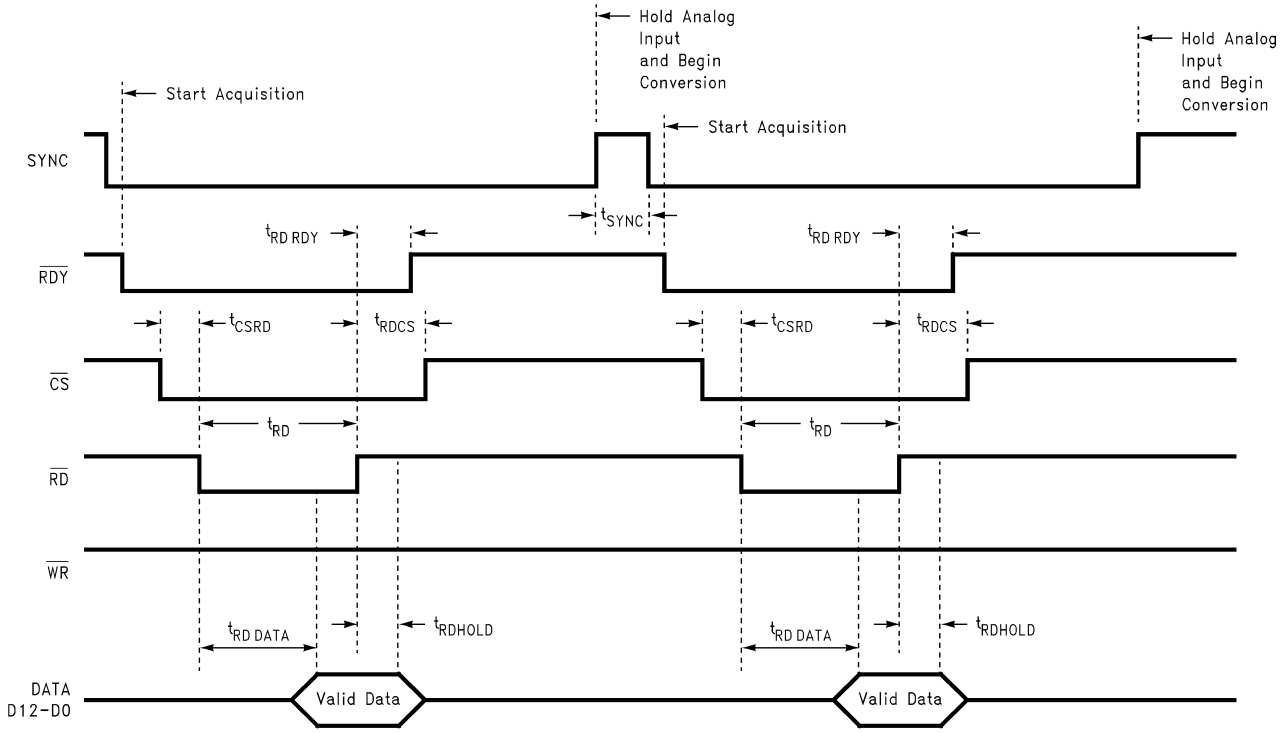


Figure 16. Sync-In Write (WMODE = 0, BW = 1), Read and Convert Cycles



The MUX channel is the channel selected on the most recent write cycle.

Figure 17. Sync-Out Read and Convert Cycles.



The MUX channel is the channel selected on the most recent write cycle.

Figure 18. Sync-In Read and Convert Cycles.

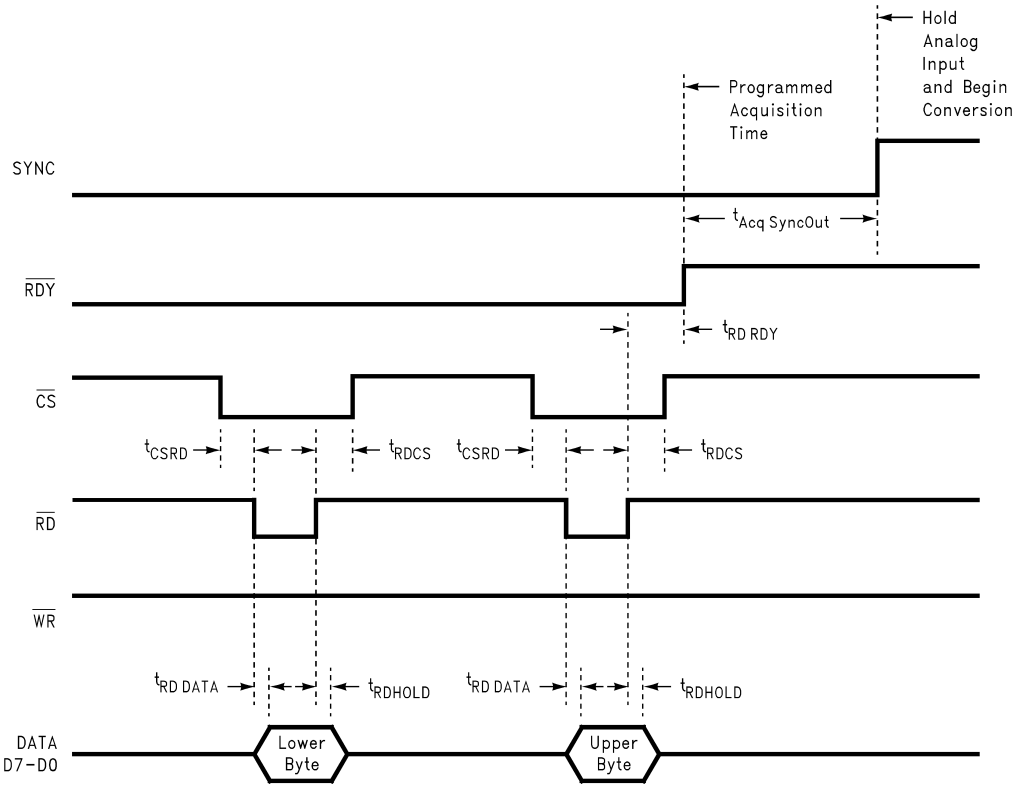


Figure 19. 8-Bit Bus Read Cycle (Sync-Out)

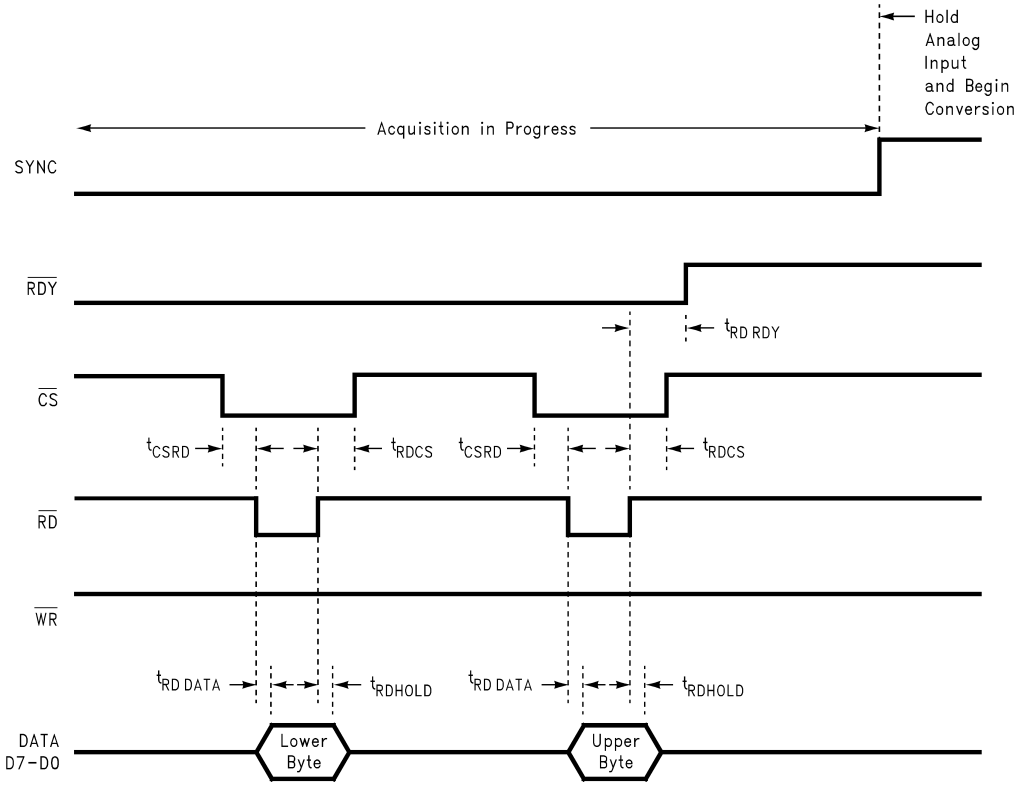


Figure 20. 8-Bit Bus Read Cycle (Sync-In)

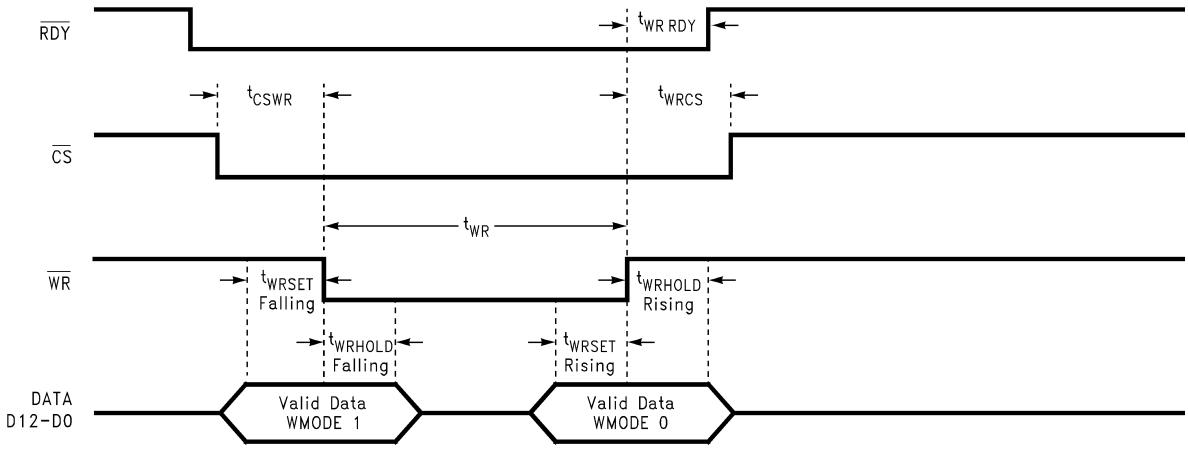


Figure 21. Write Signal Negates $\overline{\text{RDY}}$ (Writing the Standby, Auto-Cal or Auto-Zero Command)

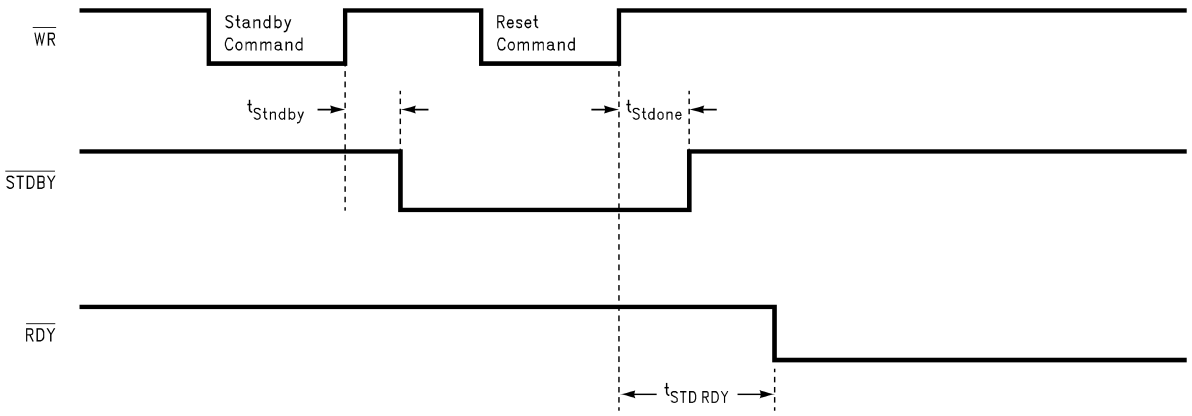


Figure 22. Standby and Reset Timing (13-Bit Data Bus Width)

Typical Performance Characteristics

See Figure 4(1)

Integral Linearity Error (INL) Change vs. Clock Frequency

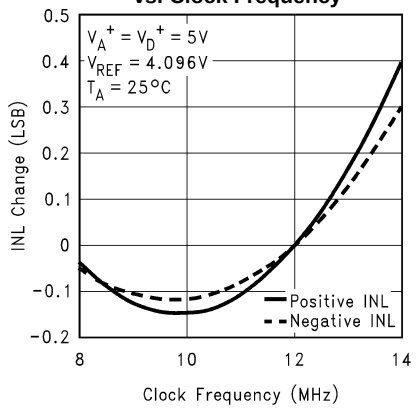


Figure 23.

Full-Scale Error Change vs. Clock Frequency

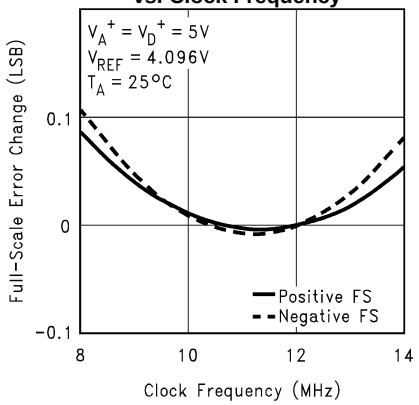


Figure 24.

Zero Error Change vs. Clock Frequency

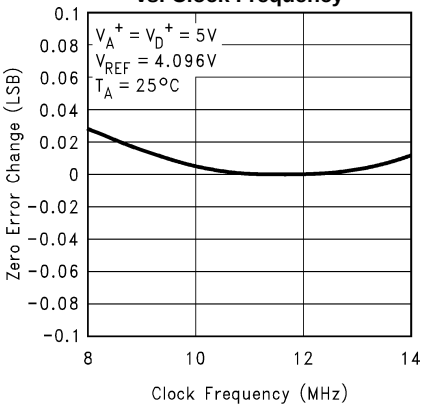


Figure 25.

Integral Linearity Error (INL) Change vs. Temperature

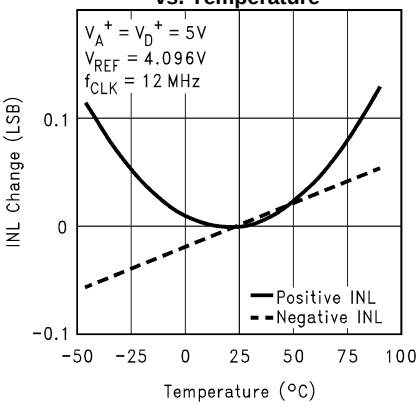


Figure 26.

Full-Scale Error Change vs. Temperature

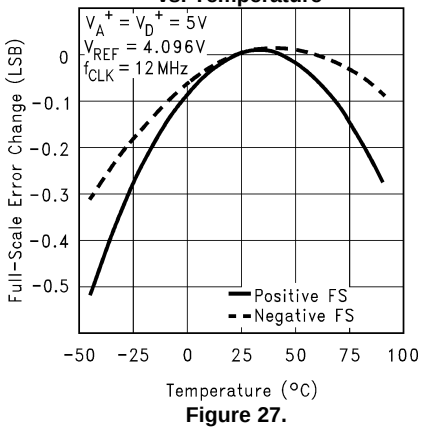


Figure 27.

Zero Error Change vs. Temperature

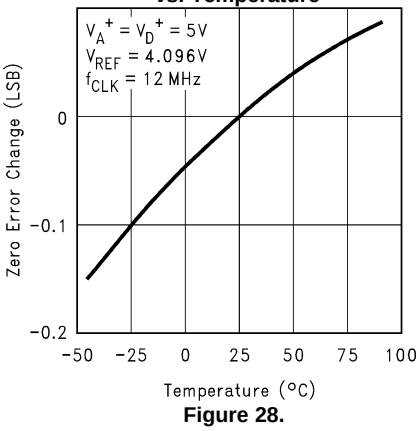


Figure 28.

(1) The ADC12048 parts used to gather the information for these curves were auto-calibrated prior to taking the measurements at each test condition. The auto-calibration cycle cancels any first order drifts due to test conditions. However, each measurement has a repeatability uncertainty error of 0.2 LSB. See Note 4 under the Converter DC Characteristics Table.

Typical Performance Characteristics (continued)

See Figure 4(1)

Integral Linearity Error (INL) Change vs. Reference Voltage

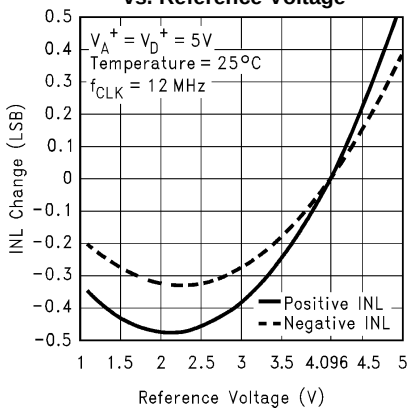


Figure 29.

Full-Scale Error Change vs. Reference Voltage

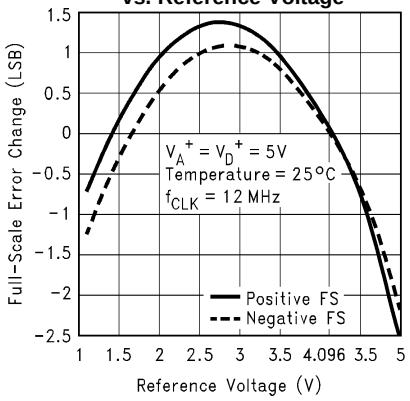


Figure 30.

Zero Error Change vs. Reference Voltage

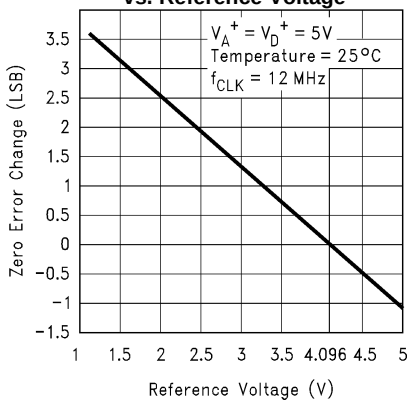


Figure 31.

Integral Linearity Error (INL) Change vs. Supply Voltage

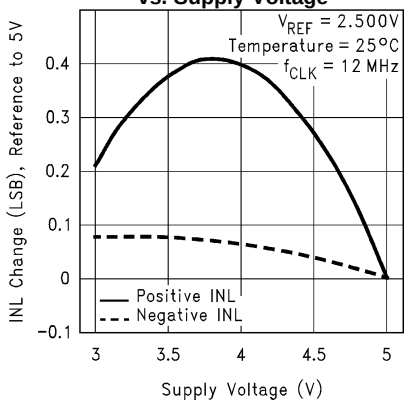


Figure 32.

Full-Scale Error Change vs. Supply Voltage

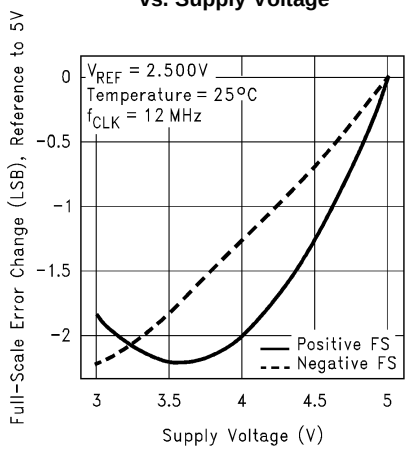


Figure 33.

Zero Error Change vs. Supply Voltage

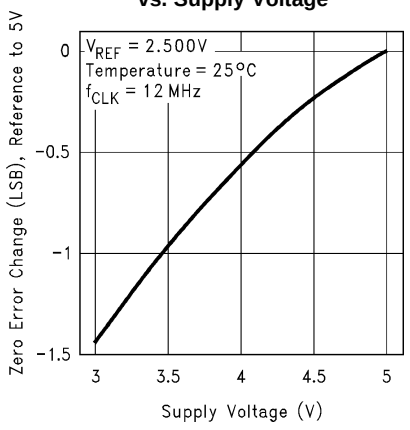


Figure 34.

Typical Performance Characteristics

See Figure 4(1)

Supply Currents vs. Clock Frequency

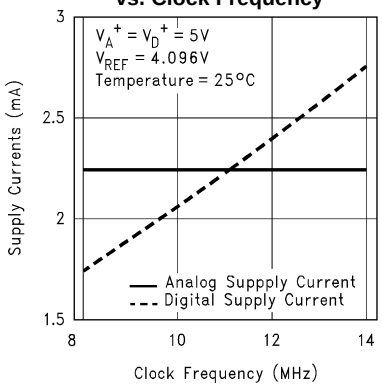


Figure 35.

Reference Currents vs. Clock Frequency

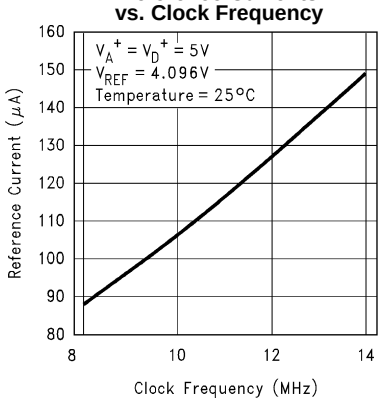


Figure 36.

Analog Supply Current vs. Temperature

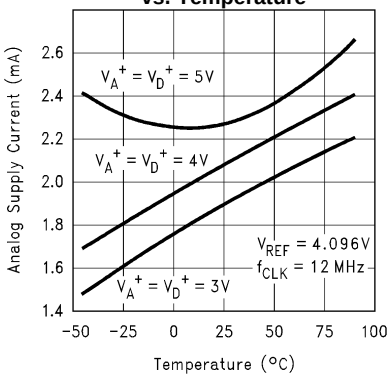


Figure 37.

Digital Supply Current vs. Temperature

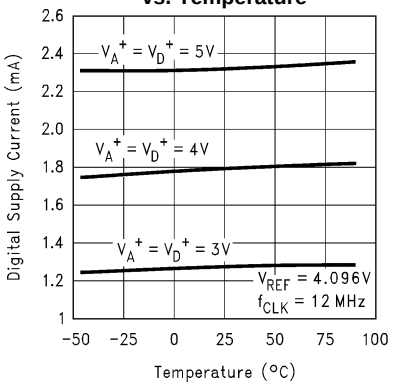


Figure 38.

Full Scale Differential 1,099 Hz Sine Wave Input

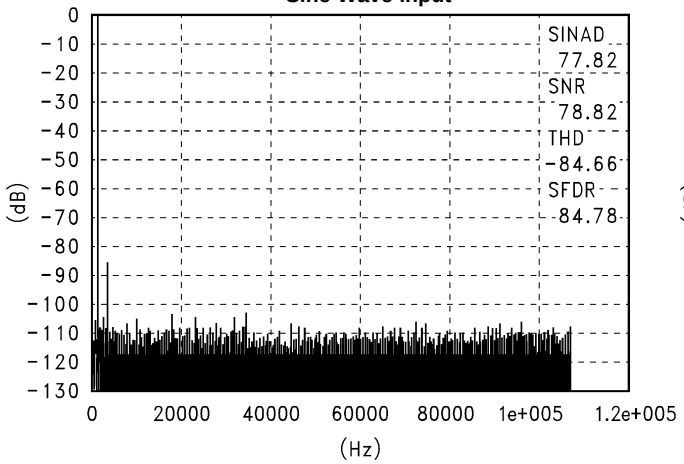


Figure 39.

Full Scale Differential 18,677 Hz Sine Wave Input

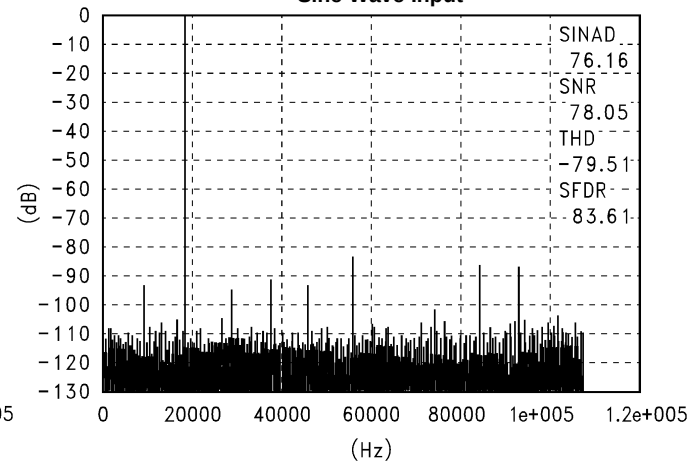


Figure 40.

(1) These typical curves were measured during continuous conversions with a positive half-scale DC input. A 240 ns $\overline{RD}$ pulse was applied 25 ns after the $\overline{RDY}$ signal went low. The data bus lines were loaded with 2 HC family CMOS inputs (C_L ~ 20 pF).

Typical Performance Characteristics (continued)

See Figure 4(1)

Full Scale Differential 38,452 Hz Sine Wave Input

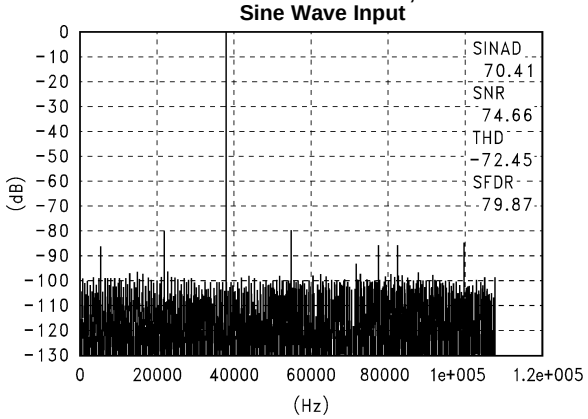


Figure 41.

Full Scale Differential 79,468 Hz Sine Wave Input

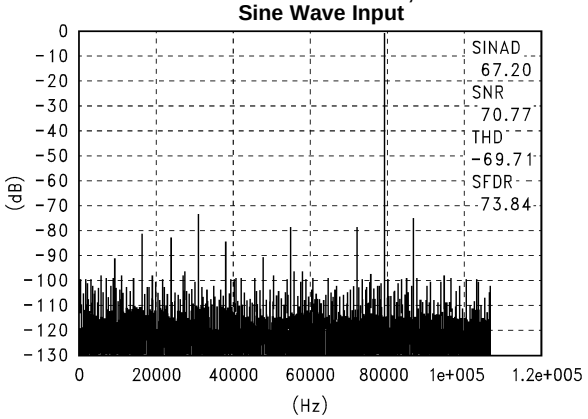


Figure 42.

Half Scale Differential 1 kHz Sine Wave Input, f_S = 153.6 kHz

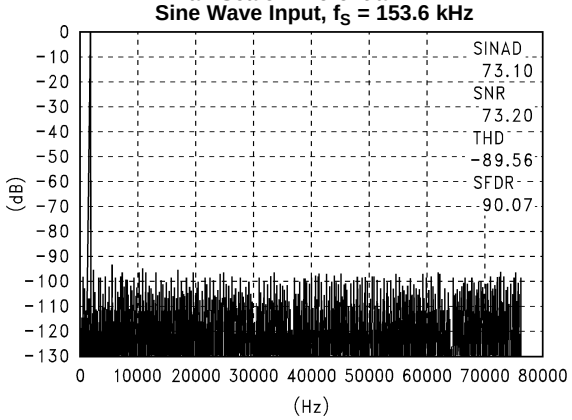


Figure 43.

Half Scale Differential 20 kHz Sine Wave Input, f_S = 153.6 kHz

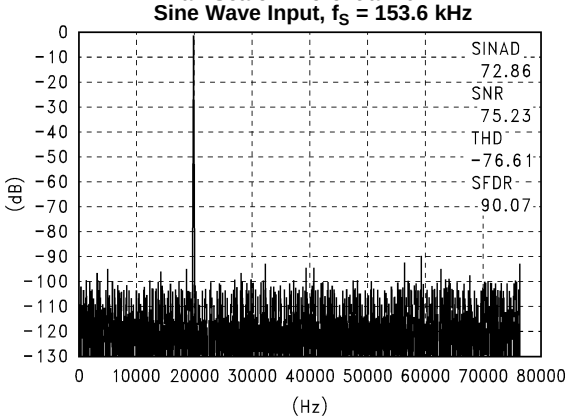


Figure 44.

Half Scale Differential 40 kHz Sine Wave Input, f_S = 153.6 kHz

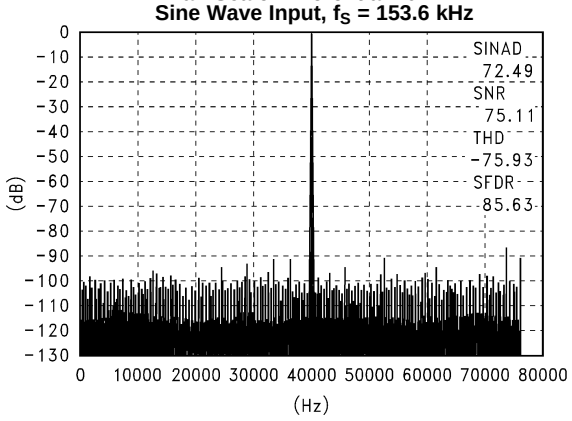


Figure 45.

Half Scale Differential 75 kHz Sine Wave Input, f_S = 153.6 kHz

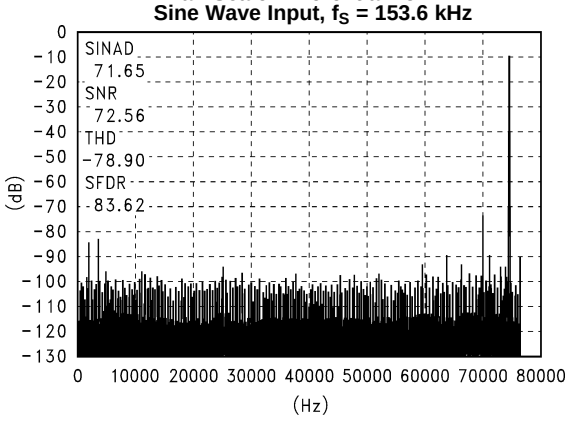


Figure 46.

REGISTER BIT DESCRIPTION

CONFIGURATION REGISTER (Write Only)

This is a 13-bit write-only register that is used to program the functionality of the ADC12048. All data written to the ADC12048 will always go to this register only. The contents of this register cannot be read.

MSB												LSB
b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
BW	COMMAND FIELD			SYNC	HB	SE	ACQ TIME		MUX ADDRESS			

Power on State: 0100Hex

b_3–b_0: The MUX ADDRESS bits configure the analog input MUX. They select which input channels of the MUX will connect to the MUXOUT+ and MUXOUT− pins. (Refer to INPUT MULTIPLEXER for more details on the MUX.) **Power-up** value is 0000.

Table 1. MUX Channel Assignment

b_3	b_2	b_1	b_0	MUXOUT+	MUXOUT−
0	0	0	0	CH0	CH1
0	0	0	1	CH1	CH0
0	0	1	0	CH2	CH3
0	0	1	1	CH3	CH2
0	1	0	0	CH4	CH5
0	1	0	1	CH5	CH4
0	1	1	0	CH6	CH7
0	1	1	1	CH7	CH6
1	0	0	0	CH0	COM
1	0	0	1	CH1	COM
1	0	1	0	CH2	COM
1	0	1	1	CH3	COM
1	1	0	0	CH4	COM
1	1	0	1	CH5	COM
1	1	1	0	CH6	COM
1	1	1	1	CH7	COM

b_5–b_4: The ACQ TIME bits select one of four possible acquistion times in SYNC-OUT mode. (Refer to SELECTABLE ACQUISITION TIME.)

b_5	b_4	Clocks
0	0	9
0	1	15
1	0	47
1	1	79

b_6: When the Single-Ended bit (SE bit) is set, conversion results will be limited to positive values only and any negative conversion results will appear as a code of zero in the Data register. The SE bit is cleared at **power-up.**

b_7: The High Byte bit (HB) is meaningful only in 8-bit mode (BW bit b_{12} = “0”) and is a don't care condition in 13-bit mode (BW bit b_{12} = “1”). This bit is used to access the upper byte of the Configuration Register in 8-bit mode. When this bit is set and bit b_{12} = 0, the next byte written to the ADC12048 will program the upper byte of the Configuration register. The HB bit will automatically be cleared when data is written to the upper byte of the Configuration register, allowing the lower byte to be accessed with the next write. The HB bit is cleared at **power-up.**

b_8: The SYNC bit. When the SYNC bit is set, the SYNC pin is programmed as an input and the converter is in synchronous mode. In this mode a rising edge on the SYNC pin causes the ADC to hold the input signal and begin a conversion. When b_{15} cleared, the SYNC pin is programmed as an output and the converter is in an asynchronous mode. In this mode the signal at the SYNC pin indicates the status of the converter. The SYNC pin is high when a conversion is taking place. The SYNC bit is set at **power-up.**

b_{11}–b_9: The command field. These bits select the mode of operation of the ADC12048. **Power-up** value is 000.

b_{11}	b_{10}	b_9	Command (1)
0	0	0	Standby command. This puts the ADC in a low power consumption mode
0	0	1	Ful-Cal command. This will cause the ADC to perform a self-calibrating cycle that will correct linearity and zero errors.
0	1	0	Auto-zero command. This will cause the ADC to perform an auto-zero cycle that corrects offset errors.
0	1	1	Reset command. This puts the ADC in an idle mode.
1	0	0	Start command. This will put the converter in a start mode, preparing it to perform a conversion. If in asynchronous mode (b_8 = “0”), conversions will immediately begin after the programmed acquisition time has ended. In synchronous mode (b_8 = “1”), conversions will begin after a rising edge appears on the SYNC pin.

(1) Any other values placed in the command field are meaningless. However, if a code of 101 or 110 is placed in the command field and the $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ go low at the same time, the ADC12048 will enter a test mode. These test modes are only to be used by the manufacturer of this device. A hardware power-off and power-on reset must be done to get out of these test modes.

b_{12}: This is the Bus Width (BW) bit. When this bit is a '0' the ADC12048 is configured to interface with an 8-bit data bus; data pins D_7–D_0 are active and pins D_{12}–D_9 are in TRI-STATE. When the BW bit is a '1', the ADC12048 is configured to interface with a 16-bit data bus and data pins D_{13}–D_0 are all active. The BW bit is a '0' at **power-up.**

DATA REGISTER (Read Only)

This is a 13-bit read only register that holds the 12-bit +sign conversion result in two's compliment form. All reads performed from the ADC12048 will place the contents of this register on the data bus. When reading the data register in 8-bit mode, the sign bit is extended (b_{12} through b_8 all contain the sign bit).

MSB												LSB
b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
sign	Conversion Data											

Power on State: 0000Hex

b_{11}–b_0: b_{11} is the most significant bit and b_0 is the least significant bit of the conversion result.

b_{12}: This bit contains the sign of the conversion result: 0 for positive results and 1 for negative.

Functional Description

The ADC12048 is programmed through a digital interface that supports an 8-bit or 16-bit data bus. The digital interface consists of a 13-bit data input/output bus (D_{12}–D_0), digital control signals and two internal registers: a **write** only 13-bit **Configuration** register and a **read** only 13-bit **Data** register.

The Configuration register programs the functionality of the ADC12048. The 13 bits of the Configuration register are divided into 7 fields. Each field controls a specific function of the ADC12048: the channel selection of the MUX, the acquisition time, synchronous or asynchronous conversions, mode of operation and the data bus size.

Features and Operating Modes

SELECTABLE BUS WIDTH

The ADC12048 can be programmed to interface with an 8-bit or 16-bit data bus. The BW bit (b_{12}) in the Configuration register controls the bus size. The bus width is set to **8 bits** (D_7–D_0 are active and D_{12}–D_8 are in TRI-STATE) if the BW bit is cleared or **13 bits** (D_{12}–D_0 are active) if the BW bit is set. At **power-up** the bus width defaults to 8 bits and any initial programming of the ADC12048 should take this into consideration.

In **8-bit** mode the Configuration register is byte accessible. The HB bit in the lower byte of the Configuration register is used to access the upper byte. If the HB bit is set with a write to the lower byte, the next byte written to the ADC will be placed in the upper byte of the Configuration register. After data is written to the upper byte of the Configuration register, the HB bit will automatically be cleared, causing the next byte written to the ADC to go to the lower byte of the Configuration register. When reading the ADC in 8-bit mode, the first read cycle places the lower byte of the Data register on the data bus followed by the upper byte during the next read cycle.

In **13-bit** mode the HB bit is a don't care condition and all bits of the data register and Configuration register are accessible with a single read or write cycle. Since the bus width of the ADC12048 defaults to 8 bits after power-up, the first action when 13-bit mode is desired must be set to the bus width to 13 bits.

WMODE

The WMODE pin is used to determine the active edge of the write pulse. The state of this pin determines which edge of the $\overline{WR}$ signal will cause the ADC to latch in data. This is processor dependent. If the processor has valid data on the bus during the falling edge of the $\overline{WR}$ signal, the WMODE pin must be tied to V_D+. This will cause the ADC to latch the data on the falling edge of the $\overline{WR}$ signal. If data is valid on the rising edge of the $\overline{WR}$ signal, the WMODE pin must be tied to DGND causing the ADC to latch in the data on the rising edge of the $\overline{WR}$ signal.

INPUT MULTIPLEXER

The ADC12048 has an eight channel input multiplexer with a COM input that can be used in a single-ended, pseudo-differential or fully-differential mode. The MUX select bits (b_3–b_0) in the Configuration register determine which channels will appear at the MUXOUT+ and MUXOUT− multiplexer output pins. (Refer to Register Bit Description.) Analog signal conditioning with fixed-gain amplifiers, programmable-gain amplifiers, filters and other processing circuits can be used at the output of the multiplexer before being applied to the ADC inputs. The ADCIN+ and ADCIN− are the fully differential non-inverting (positive) and inverting (negative) inputs to the analog-to-digital converter (ADC) of the ADC12048. If no external signal conditioning is required on the signal output of the multiplexer, MUXOUT+ should be connected to ADCIN+ and MUXOUT− should be connected to ADCIN−.

The analog input multiplexer can be set up to operate in either one of eight differential or eight single-ended (the COM input as the zero reference) modes. In the differential mode, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The input channel pairs can be connected to the MUXOUT+ and MUXOUT− pins in any order. In the single-ended mode, one of the input channels, CH0 through CH7, can be assigned to MUXOUT+ while the MUXOUT− is always assigned to the COM input.

STANDBY MODE

The ADC12048 has a low power consumption mode (75 µW @5V). This mode is entered when a Standby command is written in the command field of the Configuration register. A logic low appearing on the $\overline{STDBY}$ output pin indicates that the ADC12048 is in the Standby mode. Any command other than the Standby command written to the Configuration register will get the ADC12048 out of the Standby mode. The $\overline{STDBY}$ pin will immediately switch to a logic “1” as soon as the ADC12048 is requested to get out of the standby mode. The $\overline{RDY}$ pin will then be asserted low when the ADC is actually out of the Standby mode and ready for normal operation. The ADC12048 defaults to the Standby mode following a hardware **power-up.** This can be verified by examining the logic low status of the $\overline{STDBY}$ pin.

SYNC/ASYNC MODE

The ADC12048 may be programmed to operate in synchronous (SYNC-IN) or asynchronous (SYNC-OUT) mode. To enter synchronous mode, the SYNC bit in the Configuration register must be set. The ADC12048 is in synchronous mode after a hardware **power-up.** In this mode, the SYNC pin is programmed as an input and conversions are synchronized to the rising edges of the signal applied at the SYNC pin. Acquisition time can also be controlled by the SYNC signal when in synchronous mode. Refer to Figure 14 and Figure 18. When the SYNC bit is cleared, the ADC is in asynchronous mode and the SYNC pin is programmed as an output. In asynchronous mode, the signal at the SYNC pin indicates the status of the converter. This pin is high when the converter is performing a conversion. Refer to Figure 17 and Figure 15.

SELECTABLE ACQUISITION TIME

The ADC12048's internal sample/hold circuitry samples an input voltage by connecting the input to an internal sampling capacitor (approximately 70 pF) through an effective resistance equal to the multiplexer “On” resistance (300Ω max) plus the “On” resistance of the analog switch at the input to the sample/hold circuit (2500Ω typical) and the effective output resistance of the source. For conversion results to be accurate, the period during which the sampling capacitor is connected to the source (the “acquisition time”) must be long enough to charge the capacitor to within a small fraction of an LSB of the input voltage. An acquisition time of 750 ns is sufficient when the external source resistance is less than 1 kΩ and any active or reactive source circuitry settles to 12 bits in less than 500 ns. When source resistance or source settling time increase beyond these limits, the acquisition time must also be increased to preserve precision.

In asynchronous (SYNC-OUT) mode, the acquisition time is controlled by an internal counter. The minimum acquisition period is 9 clock cycles, which corresponds to the nominal value of 750 ns when the clock frequency is 12 MHz. Bits b_4 and b_5 of the Configuration Register are used to select the acquisition time from among four possible values (9, 15, 47, or 79 clock cycles). Since acquisition time in the asynchronous mode is based on counting clock cycles, it is also inversely proportional to clock frequency:

$$T_{ACQ}(\mu s) = \frac{\text{number of clock cycles}}{f_{CLK}\,(\text{MHz})} \tag{1}$$

Note that the actual acquisition time will be longer than T_{ACQ} because acquisition begins either when the multiplexer channel is changed or when $\overline{RDY}$ goes low, if the multiplexer channel is not changed. After a read is performed, $\overline{RDY}$ goes high, which starts the T_{ACQ} counter (see Figure 13).

In synchronous (SYNC-IN) mode, bits b_4 and b_5 are ignored, and the acquisition time depends on the sync signal applied at the SYNC pin. If a new MUX channel is selected at the start of the conversion, the acquisition period begins on the active edge of the $\overline{WR}$ signal that latches in the new MUX channel. If no new MUX channel is selected, the acquisition period begins on the falling edge of $\overline{RDY}$, which occurs at the end of the previous conversion (or at the end of an autozero or autocalibration procedure). The acquisition period ends when SYNC goes high.

To estimate the acquisition time necessary for accurate conversions when the source resistance is greater than 1 kΩ, use the following expression:

$$T_{ACQMIN}\,(\mu s) = \frac{0.75(R_S + R_M + R_{S/H})}{1\,k\Omega + R_M + R_{S/H}}$$

$$= \frac{0.75(R_S + 2800)}{3800} \tag{2}$$

where

- R_S is the source resistance
- R_M is the MUX “On” resistance
- $R_{S/H}$ is the sample/hold “On” resistance

If the settling time of the source is greater than 500 ns, the acquisition time should be about 300 ns longer than the settling time for a “well-behaved”, smooth settling characteristic.

FULL CALIBRATION CYCLE

A full calibration cycle compensates for the ADC's linearity and offset errors. The converter's DC specifications are specified only after a full calibration has been performed. A full calibration cycle is initiated by writing a Ful-Cal command to the ADC12048. During a full calibration, the offset error is measured eight times, averaged and a correction coefficient is created. The offset correction coefficient is stored in an internal offset correction register.

The overall linearity correction is achieved by correctng the internal DAC's capacitor mismatches. Each capacitor is compared eight times against all remaining smaller value capacitors. The errors are averaged and correction coefficients are created.

Once the converter has been calibrated, an arithmetic logic unit (ALU) uses the offset and linearity correction coefficients to reduce the conversion offset and linearity errors to within specified limits.

AUTO-ZERO CYCLE

During an auto-zero cycle, the offset is measured only once and a correction coefficient is created and stored in an internal offset register. An auto-zero cycle is initiated by writing an Auto-Zero command to the ADC12048.

DIGITAL INTERFACE

The digital control signals are $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{RDY}$ and $\overline{STDBY}$. Specific timing relationships are associated with the interaction of these signals. Refer to Digital Timing Diagrams for detailed timing specifications. The active low $\overline{RDY}$ signal indicates when a certain event begins and ends. It is recommended that the ADC12048 should only be accessed when the $\overline{RDY}$ signal is low. It is in this state that the ADC12048 is ready to accept a new command. This will minimize the effect of noise generated by a switching data bus on the ADC. The only exception to this is when the ADC12048 is in the standby mode at which time the $\overline{RDY}$ is high and the $\overline{STDBY}$ signal is low. The ADC12048 is in the standby mode at power up or when a STANDBY command is issued. A Ful-Cal, Auto-Zero, Reset or Start command will get the ADC12048 out of the standby mode. This may be observed by monitoring the status of the $\overline{RDY}$ and $\overline{STDBY}$ signals. The $\overline{RDY}$ signal will go low and the $\overline{STDBY}$ signal high when the ADC12048 leaves the standby mode.

The following describes the state of the digital control signals for each programmed event in both 8-bit and 13-bit mode. $\overline{RDY}$ should be low before each command is issued except for the case when the device is in standby mode.

FUL-CAL OR AUTO-ZERO COMMAND

8-bit mode: The first write to the ADC12048 will place the data in the lower byte of the Configuration register. This byte must set the HB bit (b_7) to allow access to the upper byte of the Configuration register during the next write cycle. During the second write cycle, the Ful-Cal or Auto-Zero command must be issued. The edge of the second write pulse on the $\overline{WR}$ pin will force the $\overline{RDY}$ signal high. At this time the converter begins executing a full calibration or auto-zero cycle. The $\overline{RDY}$ signal will automatically go low when the full calibration or auto-zero cycle is done.

13-bit mode: In a single write cycle the Ful-Cal or Auto-Zero command must be written to the ADC12048. The edge of the $\overline{WR}$ signal will force the $\overline{RDY}$ high. At this time the converter begins executing a full calibration or auto-zero cycle. The $\overline{RDY}$ signal will automatically go low when the full calibration or auto-zero cycle is done.

STARTING A CONVERSION: START COMMAND

In order to completely describe the events associated with the Start command, both the SYNC-OUT and SYNC-IN modes must be considered.

SYNC-OUT/Asynchronous

8-bit mode: The first byte written to the ADC12048 should set the MUX channel, the acquisition time and the HB bit. The second byte should clear the SYNC bit, write the START command and clear the BW bit. In order to initiate a conversion, two reads must be performed from the ADC12048. The rising edge of the second read pulse will force the $\overline{RDY}$ pin high and begin the programmed acquisition time selected by bits b_5 and b_4 of the configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The $\overline{RDY}$ and SYNC signal will fall low when the conversion is done. At this time new information, such as a new MUX channel, acquisition time and operational command can be written into the configuration register or it can remain unchanged. Assuming that the START command is in the Configuration register, the previous conversion can be read. The first read places the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. The rising edge on the second read pulse will begin another conversion sequence and raise the $\overline{RDY}$ and SYNC signals appropriately.

13-bit mode: The MUX channel and the acquisition time should be set, the SYNC bit cleared and the START command issued with a single write to the ADC12048. In order to initiate a conversion, a single read must be performed from the ADC12048. The rising edge of the read signal will force the $\overline{RDY}$ signal high and begin the programmed acquisition time selected by bits b_5 and b_4 of the configuration register. The SYNC pin will go high indicating that a conversion sequence has begun following the end of the acquisition period. The $\overline{RDY}$ and SYNC signal will fall low when the conversion is done. At this time new information, such as a new MUX channel,

acquisition time and operational command can be written into the configuration register or it can remain unchanged. With the START command in the Configuration register, a read from the ADC12048 will place the entire 13-bit conversion result stored in the data register on the data bus. The rising edge of the read pulse will immediately force the $\overline{RDY}$ output high. The SYNC will then go high following the elapse of the programmed acquisition time in the configuration register's bits b_5 and b_4.

SYNC-IN/Synchronous

For the SYNC-IN case, it is assumed that a series of SYNC pulses at the desired sampling rate are applied at the SYNC pin of the ADC12048.

8-bit mode: The first byte written to the ADC12048 should set the MUX channel and the HB bit. The second byte should set the SYNC bit, write the START command and clear the BW bit.

A rising edge on the SYNC pin or the second rising edge of two consecutive reads from the ADC12048 will force the $\overline{RDY}$ signal high. It is recommended that the action of reading from the ADC12048 (not the rising edge of the SYNC signal) be used to raise the $\overline{RDY}$ signal. In the SYNC-IN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The rising edge of the SYNC also ends the acquisition period. The acquisition period begins following a write cycle containing MUX channel information. The selected MUX channel is sampled after the rising edge of the $\overline{WR}$ signal until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins. The $\overline{RDY}$ signal will go low when the conversion is done. A new MUX channel and/or operational command may be written into the Configuration register at this time, if needed. Two consecutive read cycles are required to retrieve the entire 13-bit conversion result from the ADC12048's data register. The first read will place the lower byte of the conversion result contained in the Data register on the data bus. The second read will place the upper byte of the conversion result stored in the Data register on the data bus. With the START command in the configuration register, the rising edge of the second read pulse will raise the $\overline{RDY}$ signal high and begin a conversion cycle following a rising edge on the SYNC pin.

13-bit mode: The MUX channel should be selected, the SYNC bit should be set and the START command issued with a single write to the ADC12048. A rising edge on the SYNC pin or on the $\overline{RD}$ pin will force the $\overline{RDY}$ signal high. It is recommended that the action of reading from the ADC12048 (not the rising edge of the SYNC signal) be used to raise the $\overline{RDY}$ signal. This will ensure that the conversion result is read during the acquisition period of the next conversion cycle, eliminating a read from the ADC12048 while it is performing a conversion. Noise generated by accessing the ADC12048 while it is converting may degrade the conversion result. In the SYNC-IN mode, only the rising edge of the SYNC signal will begin a conversion cycle. The $\overline{RDY}$ signal will go low when the conversion cycle is done. The acquisition time is controlled by the SYNC signal. The acquisition period begins following a write cycle containing MUX channel information. The selected MUX channel is sampled after the rising edge of the $\overline{WR}$ signal until the rising edge of the SYNC pulse, at which time the signal will be held and conversion begins. A new MUX channel and/or operational command may be written into the Configuration register at this time, if needed. With the START command in the Configuration register, a read from the ADC12048 will place the entire conversion result stored in the Data register on the data bus and the rising edge of the read pulse will force the $\overline{RDY}$ signal high. The selected MUX channel will be sampled until a rising edge appears on the SYNC pin, at which the time sampled signal will be held and a conversion cycle started.

STANDBY COMMAND

8-bit mode: The first byte written to the ADC12048 should set the HB bit in the Configuration register (bit b_7). The second byte must issue the Standby command (bits b_{11}, b_{10}, b_9 = 0, 0, 0).

13-bit mode: The Standby command must be issued to the ADC12048 in single write (bits b_{11}, b_{10}, b_9 = 0, 0, 0).

RESET

The RESET command places the ADC12048 into a ready state and forces the $\overline{RDY}$ signal low. The RESET command can be used to interrupt the ADC12048 while it is performing a conversion, full-calibration or auto-zero cycle. It can also be used to get the ADC12048 out of the standby mode.

Analog Application Information

REFERENCE VOLTAGE

The ADC12048 has two reference inputs, V_{REF}+ and V_{REF}−. They define the zero to full-scale range of the analog input signals over which 4095 positive and 4096 negative codes exist. The reference inputs can be connected to span the entire supply voltage range (V_{REF}− = AGND, V_{REF}+ = V_A+) or they can be connected to different voltages when other input spans are required. The reference inputs of the ADC12048 have transient capacitive switching currents. The voltage sources driving V_{REF}+ and V_{REF}− must have very low output impedance and noise and must be adequately bypassed. The circuit in Figure 48 is an example of a very stable reference source.

The ADC12048 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. This technique relaxes the system reference requirements because the analog input voltage moves with the ADC's reference. The system power supply can be used as the reference voltage by connecting the V_{REF}+ pin to V_A+ and the V_{REF}− pin to AGND. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

The reference voltage inputs are not fully differential. The ADC12048 will not generate correct conversions if (V_{REF}+) – (V_{REF}−) is below 1V. Figure 47 shows the allowable relationship between V_{REF}+ and V_{REF}−.

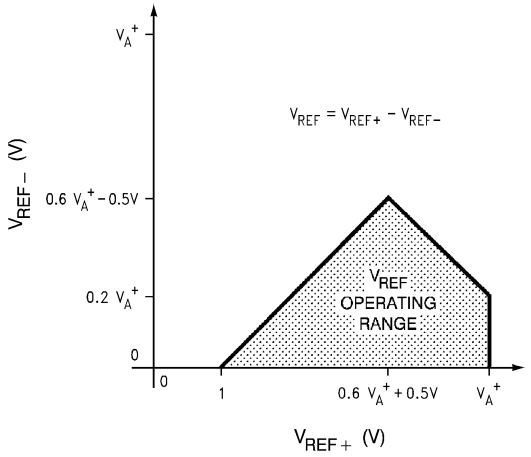
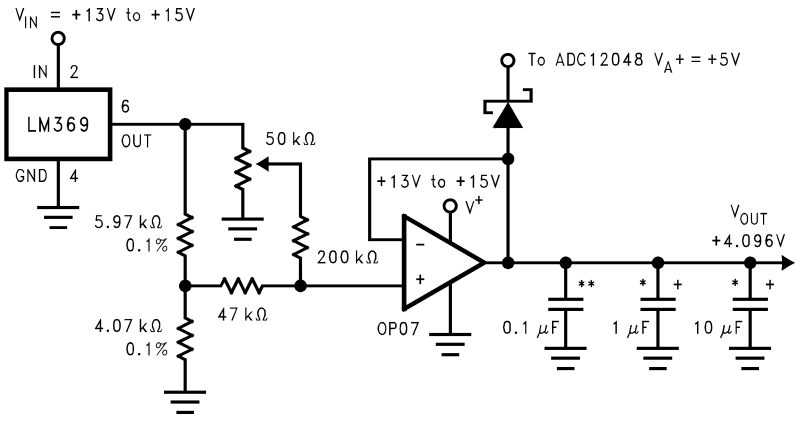


Figure 47. V_{REF} Operating Range



*Tantalum
**Ceramic

Figure 48. Low Drift Extremely Stable Reference Circuit

Part Number	Output Voltage Tolerance	Temperature Coefficient
LM4041CI-Adj	±0.5%	±100ppm/°C
LM4040AI-4.1	±0.1%	±100ppm/°C
LM4050	±0.2%	±50ppm/°C
LM4121	±0.1%	±50ppm/°C
LM9140BYZ-4.1	±0.5%	±25ppm/°C
Circuit of Figure 48	Adjustable	±2ppm/°C

OUTPUT DIGITAL CODE VERSUS ANALOG INPUT VOLTAGE

The ADC12048's fully differential 12-bit + sign ADC generates a two's complement output that is found by using the equation shown below:

$$\text{Output code} = \frac{(V_{IN}^{+} - V_{IN}^{-})\,(4096)}{(V_{REF}^{+} - V_{REF}^{-})} \tag{3}$$

Round off the result to the nearest integer value between −4096 and 4095.

INPUT CURRENT

At the start of the acquisition window ($t_{AcqSYNOUT}$) a charging current (due to capacitive switching) flows through the analog input pins (CH0–CH7, ADCIN+ and ADCIN−, and the COM). The peak value of this input current will depend on the amplitude and frequency of the input voltage applied, the source impedance and the input switch ON resistance. With the MUXOUT+ connected to the ADCIN+ and the MUXOUT− connected to the ADCIN− the on resistance is typically 2800Ω. Bypassing the MUX and using just the ADCIN+ and ADCIN− inputs the on resistance is typically 2500Ω.

For low impedance voltage sources (<1000Ω for 12 MHz operation), the input charging current will decay to a value that will not introduce any conversion errors before the end of the default sample-and-hold (S/H) acquisition time (9 clock cycles). For higher source impedances (>1000Ω for 12 MHz operation), the S/H acquisition time should be increased to allow the charging current to settle within specified limits. In asynchronous mode, the acquisition time may be increased to 15, 47 or 79 clock cycles. If different acquisition times are needed, the synchronous mode can be used to fully control the acquisition time.

INPUT BYPASS CAPACITANCE

External capacitors (0.01 µF–0.1 µF) can be connected between the analog input pins (CH0–CH7) and the analog ground to filter any noise caused by inconductive pickup associated with long leads.

POWER SUPPLY CONSIDERATIONS

Decoupling and bypassing the power supply on a high resolution ADC is an important design task. Noise spikes on the V_A+ (analog supply) or V_D+ (digital supply) can cause conversion errors. The analog comparator used in the ADC will respond to power supply noise and will make erroneous conversion decisions. The ADC is especially sensitive to power supply spikes that occur during the auto-zero or linearity calibration cycles.

The ADC12048 is designed to operate from a single +5V power supply. The separate supply and ground pins for the analog and digital portions of the circuit allow separate external bypassing. To minimize power supply noise and ripple, adequate bypass capacitors should be placed directly between power supply pins and their associated grounds. Both supply pins should be connected to the same supply source. In systems with separate analog and digital supplies, the ADC should be powered from the analog supply. At least a 10 µF tantalum electrolytic capacitor in parallel with a 0.1 µF monolithic ceramic capacitor is recommended for bypassing each power supply. The key consideration for these capacitors is to have low series resistance and inductance. The capacitors should be placed as close as physically possible to the supply and ground pins with the smaller capacitor closer to the device. The capacitors also should have the shortest possible leads in order to minimize series lead inductance. Surface mount chip capacitors are optimal in this respect and should be used when possible.

When the power supply regulator is not local on the board, adequate bypassing (a high value electrolytic capacitor) should be placed at the power entry point. The value of the capacitor depends on the total supply current of the circuits on the PC board. All supply currents should be supplied by the capacitor instead of being drawn from the external supply lines, while the external supply charges the capacitor at a steady rate.

The ADC has two V_D+ and DGND pins. It is recommended that each of these V_D+ pins be separately bypassed to DGND with a 0.1 µF plus a 10 µF capacitor. The layout diagram of Figure 49 shows the recommended placement for the supply bypass capacitors.

PC BOARD LAYOUT AND GROUNDING CONSIDERATIONS

To get the best possible performance from the ADC12048, the printed circuit boards should have separate analog and digital ground planes. The reason for using two ground planes is to prevent digital and analog ground currents from sharing the same path until they reach a very low impedance power supply point. This will prevent noisy digital switching currents from being injected into the analog ground.

Figure 49 illustrates a favorable layout for ground planes, power supply and reference input bypass capacitors. It shows a layout using a 44-pin PLCC socket and through-hole assembly. A similar approach should be used for the PQFP package.

The analog ground plane should encompass the area under the analog pins and any other analog components such as the reference circuit, input amplifiers, signal conditioning circuits, and analog signal traces.

The digital ground plane should encompass the area under the digital circuits and the digital input/output pins of the ADC12048. Having a continuous digital ground plane under the data and clock traces is very important. This reduces the overshoot/undershoot and high frequency ringing on these lines that can be capacitively coupled to analog circuitry sections through stray capacitances.

The AGND and DGND in the ADC12048 are not internally connected together. They should be connected together on the PC board right at the chip. This will provide the shortest return path for the signals being exchanged between the internal analog and digital sections of the ADC.

It is also a good design practice to have power plane layers in the PC board. This will improve the supply bypassing (an effective distributed capacitance between power and ground plane layers) and voltage drops on the supply lines. However, power planes are not as essential as ground planes are for satisfactory performance. If power planes are used, they should be separated into two planes and the area and connections should follow the same guidelines as mentioned for the ground planes. Each power plane should be laid out over its associated ground planes, avoiding any overlap between power and ground planes of different types. When the power planes are not used, it is recommended to use separate supply traces for the V_A+ and V_D+ pins from a low impedance supply point (the regulator output or the power entry point to the PC board). This will help ensure that the noisy digital supply does not corrupt the analog supply.

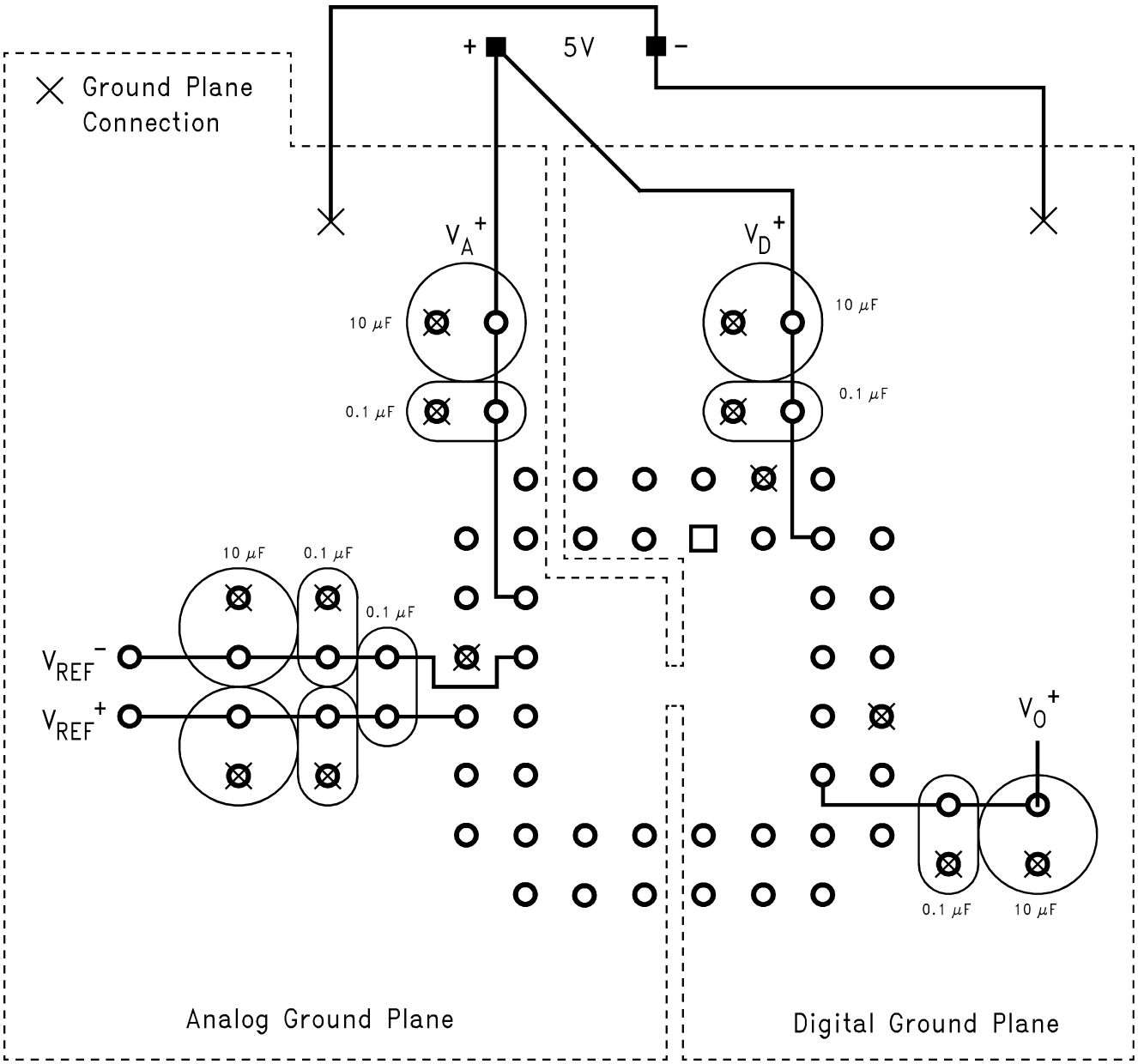


Figure 49. Top View of Printed Circuit Board for a 44-Pin PLCC ADC12048

When measuring AC input signals, any crosstalk between analog input/output lines and the reference lines (CH0–CH7, MUXOUT±, ADC IN±, V_{REF}±) should be minimized. Crosstalk is minimized by reducing any stray capacitance between the lines. This can be done by increasing the clearance between traces, keeping the traces as short as possible, shielding traces from each other by placing them on different sides of the AGND plane, or running AGND traces between them.

Figure 49 also shows the reference input bypass capacitors. Here the reference inputs are considered to be differential. The performance improves by having a 0.1 µF capacitor between the V_{REF}+ and V_{REF}−, and by bypassing in a manner similar to that described for the supply pins. When a single ended reference is used, V_{REF}− is connected to AGND and only two capacitors are used between V_{REF}+ and V_{REF}− (0.1 µF + 10 µF). It is recommended to directly connect the AGND side of these capacitors to the V_{REF}− instead of connecting V_{REF}− and the ground sides of the capacitors separately to the ground planes. This provides a significantly lower-impedance connection when using surface mount technology.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	31

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12048CIV/NOPB	ACTIVE	PLCC	FN	44	25	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	ADC12048CIV	Samples
ADC12048CIVF/NOPB	ACTIVE	QFP	PGB	44	96	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12048 CIVF >R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

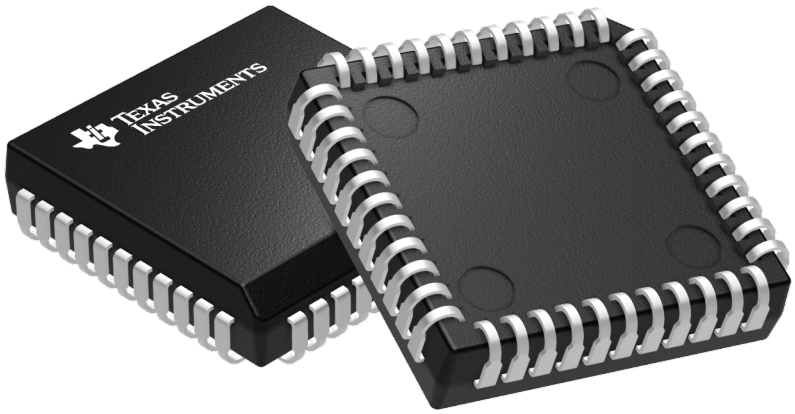
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

FN 44 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

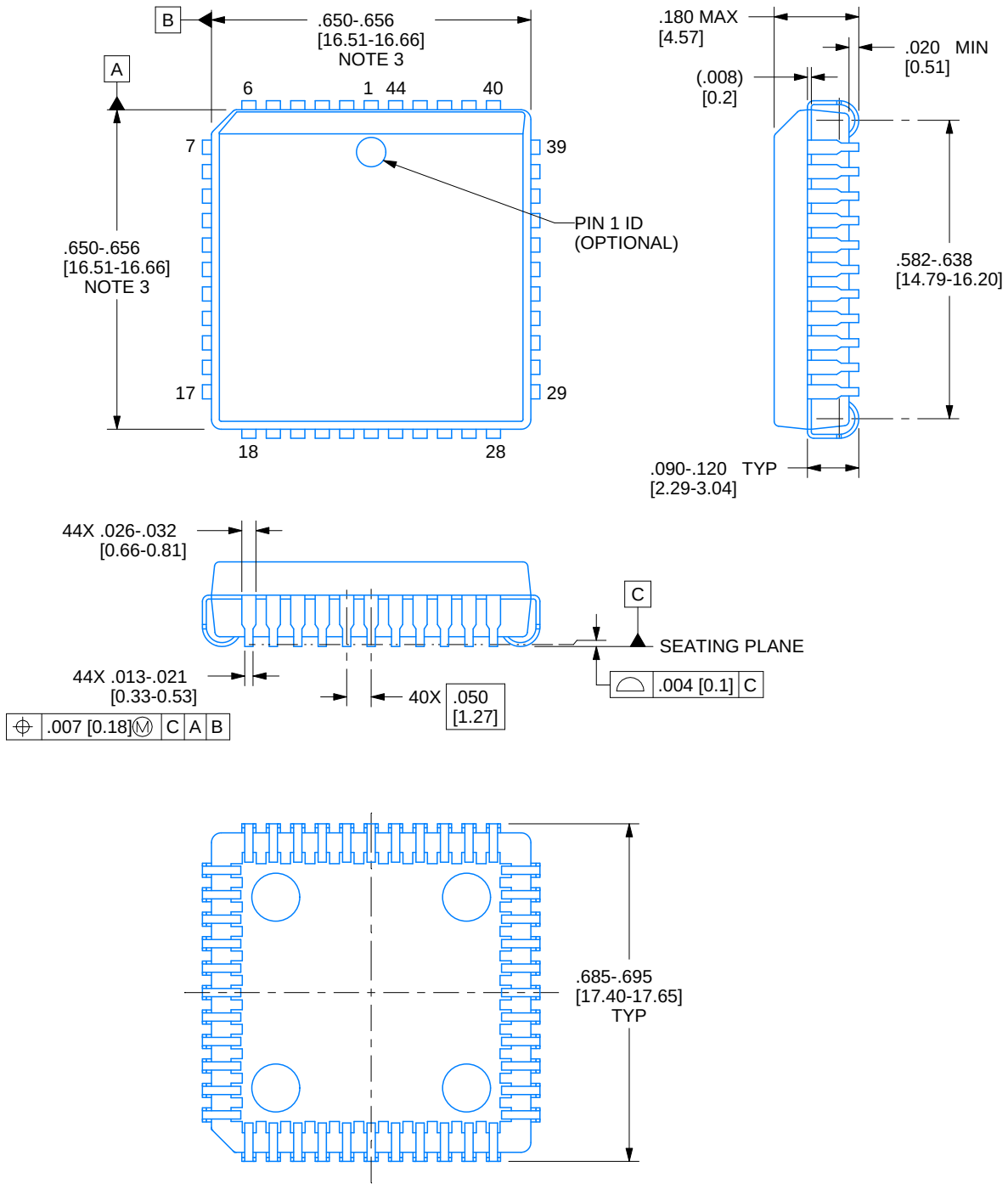
4040005-4/C

PACKAGE OUTLINE

FN0044A

PLCC - 4.57 mm max height

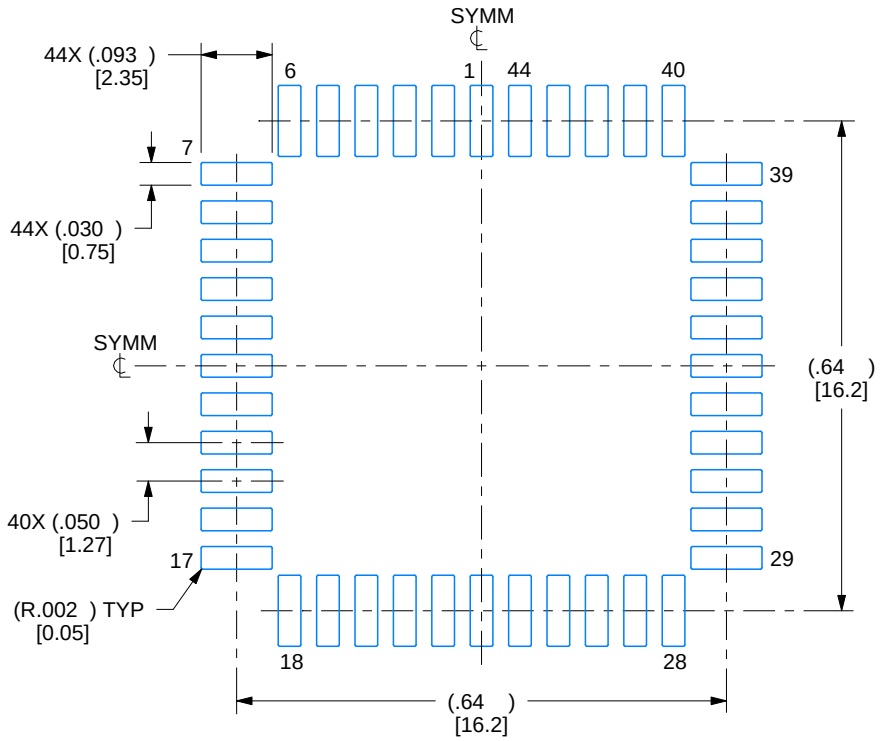
PLASTIC CHIP CARRIER



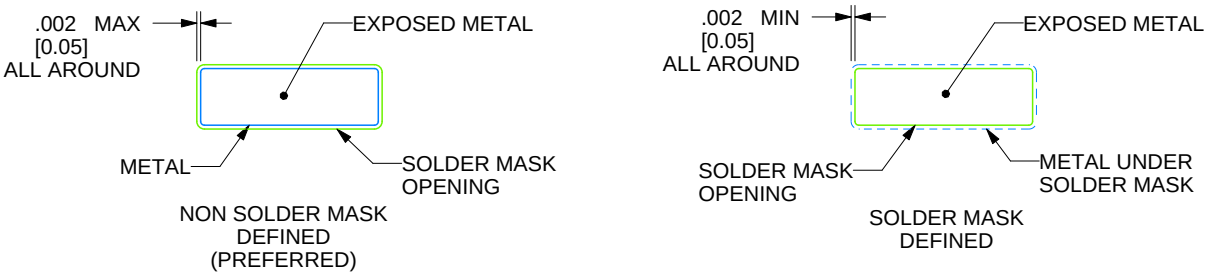
4215154/A 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X

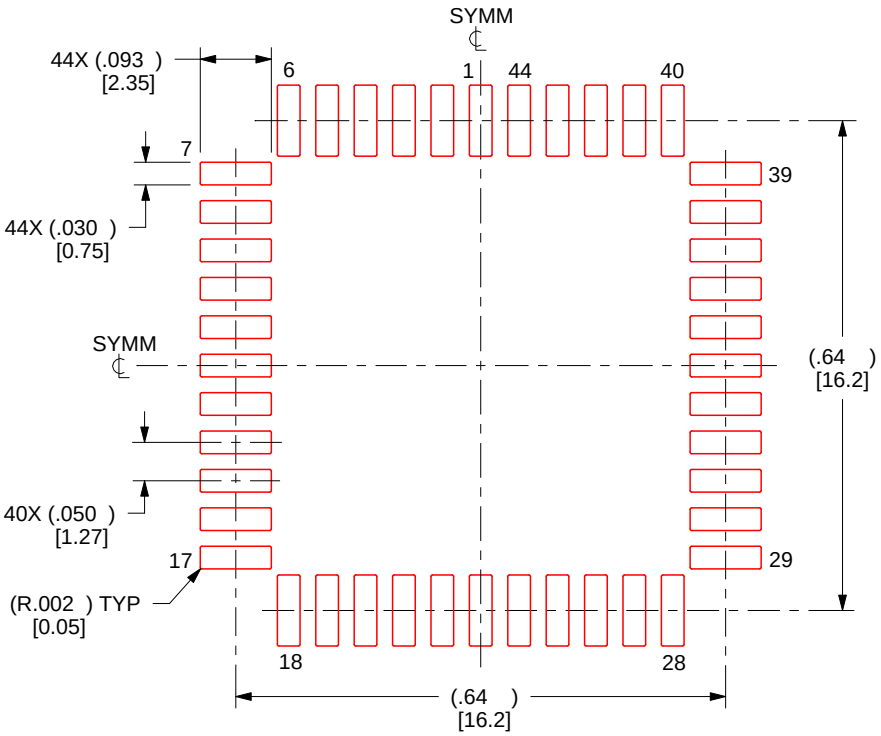


SOLDER MASK DETAILS

4215154/A 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265