ADS9110 18 位、2MSPS、15mW SAR ADC，具有 multiSPI™ 接口

1 特性

- 采样率：2MSPS
- 无延迟输出
- 出色的直流和交流性能：
  - 积分非线性 (INL)：±0.5 最低有效位 (LSB)（典型值），±1.5 LSB（最大值）
  - 微分非线性 (DNL)：±0.75 LSB（最大值），18 位无丢码 (NMC)
  - 信噪比 (SNR)：100dB
  - 总谐波失真 (THD)：-118dB
- 宽输入范围：
  - 单极差分输入范围：±V_{REF}
  - V_{REF} 输入范围：2.5V 至 5V，与 AVDD 无关
- 低功耗：
  - 2MSPS 时为 9mW（仅限 AVDD）
  - 2MSPS 时为 15mW（总功耗）
  - 灵活的低功耗模式，可根据吞吐量调节功率
- multiSPI：增强型串行接口
- 符合 JESD8-7A 标准的数字 I/O（1.8V DVDD 时）
- 在 -40°C 至 +85°C 的工业温度范围内完全额定运行
- 小型封装：4mm × 4mm 超薄四方扁平无引线 (VQFN) 封装

2 应用

- 测试和测量
- 医疗成像
- 高精度、高速工业领域

3 说明

ADS9110 是一款 18 位、2MSPS、逐次逼近寄存器 (SAR) 模数转换器 (ADC)，在典型工作条件下具有 ±0.5 LSB INL 和 100dB SNR 规范值。 高吞吐量使得开发者能够对输入信号进行过采样，从而提高测量的动态范围和精度。

该器件支持单极全差分模拟输入信号，并采用 2.5V 至 5V 的外部基准电压，能够提供宽输入选择范围，无需额外进行输入调节。

该器件以 2MSPS 全吞吐量运行时的功耗仅为 15mW。 吞吐量较低时，可灵活使用低功耗模式（NAP 和 PD）来降低功耗。

集成的 multiSPI 串行接口向后兼容传统 SPI™ 协议。 此外，该器件的可配置功能还能够简化电路板布局、时序和固件，并且以低时钟速度运行时能够获得高吞吐量，因此可轻松连接各种微控制器、数字信号处理器 (DSP) 以及现场可编程门阵列 (FPGA)。

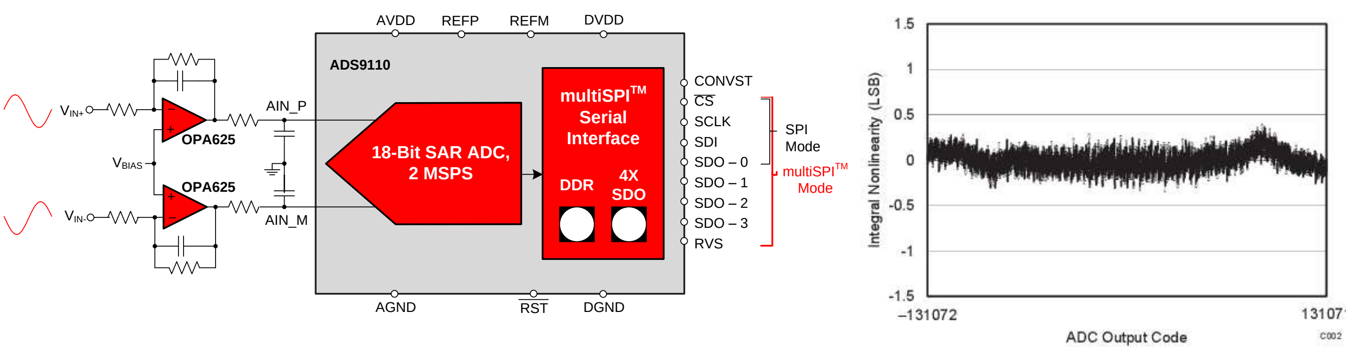
该器件采用节省空间的 4mm × 4mm VQFN 封装，支持符合 JESD8-7A 标准的 I/O 和标准工业温度范围。

器件信息

部件号	封装	封装尺寸（标称值）
ADS9110	VQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图以及积分非线性度与代码间的关系图



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4 修订历史记录

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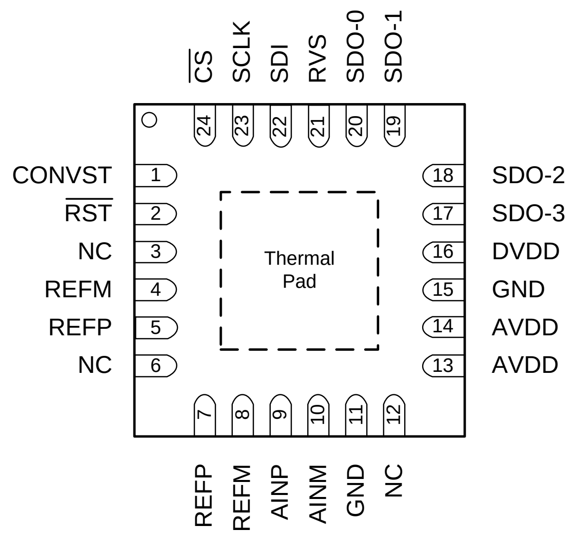
5 Pin Configuration and Functions

RGE Package
VQFN-24
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AINM	10	Analog input	Negative analog input
AINP	9	Analog input	Positive analog input
AVDD	13, 14	Power supply	Analog power supply for the device
CONVST	1	Digital input	Conversion start input pin for the device. A CONVST rising edge brings the device from ACQ state to CNV state.
$\overline{\text{CS}}$	24	Digital input	Chip-select input pin for the device; active low The device takes control of the data bus when $\overline{\text{CS}}$ is low. The SDO-x pins go to tri-state when $\overline{\text{CS}}$ is high.
DVDD	16	Power supply	Interface supply
GND	11, 15	Power supply	Ground
NC	3, 6, 12	No connection	These pins must be left floating with no external connection
REFM	4, 8	Analog input	Reference ground potential
REFP	5, 7	Analog input	Reference voltage input
$\overline{\text{RST}}$	2	Digital input	Asynchronous reset input pin for the device. A low pulse on the $\overline{\text{RST}}$ pin resets the device and all register bits return to their default state.
RVS	21	Digital output	Multi-function output pin for the device. With $\overline{\text{CS}}$ held high, RVS reflects the status of the internal ADCST signal. With $\overline{\text{CS}}$ low, the status of RVS depends on the output protocol selection.
SCLK	23	Digital input	Clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	22	Digital input	Serial data input pin for the device. This pin is used to feed the data or command into the device.
SDO-0	20	Digital output	Serial communication: data output 0
SDO-1	19	Digital output	Serial communication: data output 1
SDO-2	18	Digital output	Serial communication: data output 2
SDO-3	17	Digital output	Serial communication: data output 3
Thermal pad		Supply	Exposed thermal pad; connecting this pin to GND is recommended

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	2.1	V
DVDD to GND	–0.3	2.1	V
REFP to REFM	–0.3	5.5	V
REFM to GND	–0.1	0.1	V
Analog (AINP, AINM) to GND	–0.3	REFP + 0.3	V
Digital input ($\overline{RST}$, CONVST, $\overline{CS}$, SCLK, SDI) to GND	–0.3	DVDD + 0.3	V
Digital output (RVS, SDO-0, SDO-1, SDO-2, SDO-3) to GND	–0.3	DVDD + 0.3	V
Operating temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		1.8		V
DVDD	Digital supply voltage		1.8		V
REFP	Positive reference		5		V

6.4 Thermal Information

THERMAL METRIC(1)		ADS9110	UNITS
		RGE (VQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range (AINP – AINM)(1)		$-V_{REF}$		V_{REF}	V
V_{IN}	Absolute input voltage (AINP and AINM to REFGND)		–0.1		V_{REF} + 0.1	V
V_{CM}	Common-mode voltage range (AINP + AINM) / 2		(V_{REF} / 2) – 0.1	V_{REF} / 2	(V_{REF} / 2) + 0.1	V
C_{IN}	Input capacitance	In sample mode		60		pF
		In hold mode		4		pF
I_{IL}	Input leakage current			±1		µA
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		2.5		5	V
I_{REF}	Reference input current	Average current, V_{REF} = 5 V, 2-kHz, full-scale input, throughput = 2 MSPS		1.25		mA
DC ACCURACY						
	Resolution			18		Bits
NMC	No missing codes		18			Bits
INL	Integral nonlinearity	In LSBs	–1.5	±0.5(2)	1.5	LSB(3)
		In ppm	–5.7	±2	5.7	ppm
DNL	Differential nonlinearity		–0.75	±0.4(2)	0.75	LSB(3)
$E_{(IO)}$	Input offset error		–1	±0.05(2)	1	mV
dV_{OS}/dT	Input offset thermal drift			1		µV/°C
G_E	Gain error		–0.01	±0.005(2)	0.01	%FS
G_E/dT	Gain error thermal drift			0.25		ppm/°C
	Transition noise			0.9		LSB(3)
CMRR	Common-mode rejection ratio	At dc to 20 kHz		80		dB
AC ACCURACY(4)						
SINAD	Signal-to-noise + distortion	f_{IN} = 2 kHz	98	99.9		dB
		f_{IN} = 100 kHz		95.4		dB
		f_{IN} = 500 kHz		89		dB
SNR	Signal-to-noise ratio	f_{IN} = 2 kHz	98.1	100		dB
		f_{IN} = 100 kHz		95.5		dB
		f_{IN} = 500 kHz		89.3		dB
THD	Total harmonic distortion(5)	f_{IN} = 2 kHz		–118		dB
		f_{IN} = 100 kHz		–111		dB
		f_{IN} = 500 kHz		–101		dB
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		123		dB
		f_{IN} = 100 kHz		116		dB
		f_{IN} = 500 kHz		106		dB

(1) Ideal input span, does not include gain or offset errors.
(2) See Figure 9, Figure 10, Figure 25, and Figure 26 for statistical distribution data for INL, DNL, offset, and gain error parameters.
(3) LSB = least-significant bit. 1 LSB at 18 bits is approximately 3.8 ppm.
(4) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.1 dB below full-scale, unless otherwise specified.
(5) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics (continued)

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS(6)						
V_{IH}	High-level input voltage		0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 DVDD	V
DIGITAL OUTPUTS(6)						
V_{OH}	High-level output voltage	I_{OH} = 2-mA source	DVDD – 0.45			V
V_{OL}	Low-level output voltage	I_{OH} = 2-mA sink			0.45	V
POWER SUPPLY						
AVDD	Analog supply voltage		1.65	1.8	1.95	V
DVDD	Digital supply voltage		1.65	1.8	1.95	V
IDD	AVDD supply current (AVDD = 1.8 V)	Active, fastest throughput		5	6.25	mA
		Static, ACQ state		3.7		mA
		Low-power, NAP mode		500		µA
		Power-down, PD state		1		µA
P_D	AVDD power dissipation (AVDD = 1.8 V)	Active, fastest throughput		9	11.25	mW
		Static, ACQ state		6.6		mW
		Low-power, NAP mode		900		µW
		Power-down, PD state		1.8		µW
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		85	°C

(6) As per the JESD8-7A standard. Specified by design; not production tested.

6.6 Timing Requirements: Conversion Cycle

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 1.

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
f_{cycle}	Sampling frequency			2	MHz
t_{cycle}	ADC cycle time period	500			ns
t_{wh_CONVST}	Pulse duration: CONVST high	30			ns
t_{wl_CONVST}	Pulse duration: CONVST low	30			ns
t_{acq}	Acquisition time	150			ns
t_{qt_acq}	Quiet acquisition time (1)	25			ns
t_{d_cnvcap}	Quiet aperture time (1)	10			ns
TIMING SPECIFICATIONS					
t_{conv}	Conversion time	300		340	ns

(1) See Figure 48.

6.7 Timing Requirements: Asynchronous Reset, NAP, and PD

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 2 and Figure 3.

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{wl_RST}	Pulse duration: $\overline{RST}$ low	100			ns
TIMING SPECIFICATIONS					
t_{d_rst}	Delay time: $\overline{RST}$ rising to RVS rising			1250	µs
t_{nap_wkup}	Wake-up time: NAP mode			300	ns
t_{PWRUP}	Power-up time: PD mode			250	µs

6.8 Timing Requirements: SPI-Compatible Serial Interface

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 4.

			MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS						
f_{CLK}	Serial clock frequency				75	MHz
t_{CLK}	Serial clock time period		13.33			ns
t_{ph_CK}	SCLK high time		0.45		0.55	t_{CLK}
t_{pl_CK}	SCLK low time		0.45		0.55	t_{CLK}
t_{su_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge		5			ns
t_{su_CKDI}	Setup time: SDI data valid to the SCLK capture edge		1.2			ns
t_{ht_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI		0.65			ns
t_{ht_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		5			ns
TIMING SPECIFICATIONS						
t_{den_CSDO}	Delay time: $\overline{CS}$ falling to data enable				4.5	ns
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to 3-state				10	ns
t_{d_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO				6.5	ns
$t_{d\_CSRDY\_f}$	Delay time: $\overline{CS}$ falling to RVS falling				5	ns
$t_{d\_CSRDY\_r}$	Delay time: $\overline{CS}$ rising to RVS rising	After NOP operation			10	ns
		After WR or RD operation			70	

6.9 Timing Requirements: Source-Synchronous Serial Interface (External Clock)

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 5.

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
f_{CLK}	Serial clock frequency			100	MHz
t_{CLK}	Serial clock time period	10			ns
TIMING SPECIFICATIONS(1)					
$t_{d\_CKSTR\_r}$	Delay time: SCLK launch edge to RVS rising			8.5	ns
$t_{d\_CKSTR\_f}$	Delay time: SCLK launch edge to RVS falling			8.5	ns
$t_{off\_STRDO\_f}$	Time offset: RVS rising to (next) data valid on SDO	–0.5		0.5	ns
$t_{off\_STRDO\_r}$	Time offset: RVS falling to (next) data valid on SDO	–0.5		0.5	ns

(1) Other parameters are the same as the *Timing Requirements: SPI-Compatible Serial Interface* table.

6.10 Timing Requirements: Source-Synchronous Serial Interface (Internal Clock)

All specifications are for AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{DATA} = 2 MSPS, unless otherwise noted.
All minimum and maximum specifications are for T_A = –40°C to +85°C. All typical values are at T_A = 25°C. See Figure 6.

			MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS(1)						
t_{d_CSSTR}	Delay time: $\overline{CS}$ falling to RVS rising		12		40	ns
$t_{off\_STRDO\_f}$	Time offset: RVS rising to (next) data valid on SDO		–0.5		0.5	ns
$t_{off\_STRDO\_r}$	Time offset: RVS falling to (next) data valid on SDO		–0.5		0.5	ns
t_{STR}	Strobe output time period	INTCLK option	9.9		11.1	ns
		INTCLK / 2 option	19.8		22.2	
		INTCLK / 4 option	39.6		44.4	
t_{ph_STR}	Strobe output high time		0.45		0.55	t_{STR}
t_{pl_STR}	Strobe output low time		0.45		0.55	t_{STR}

(1) Other parameters are the same as the *Timing Requirements: SPI-Compatible Serial Interface* table.

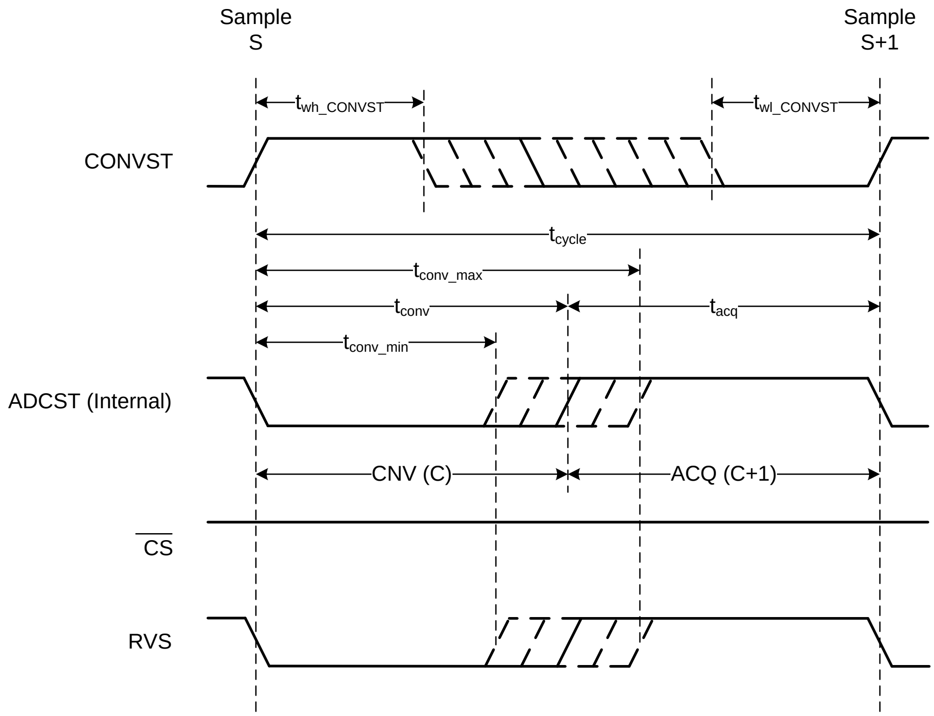


Figure 1. Conversion Cycle Timing Diagram

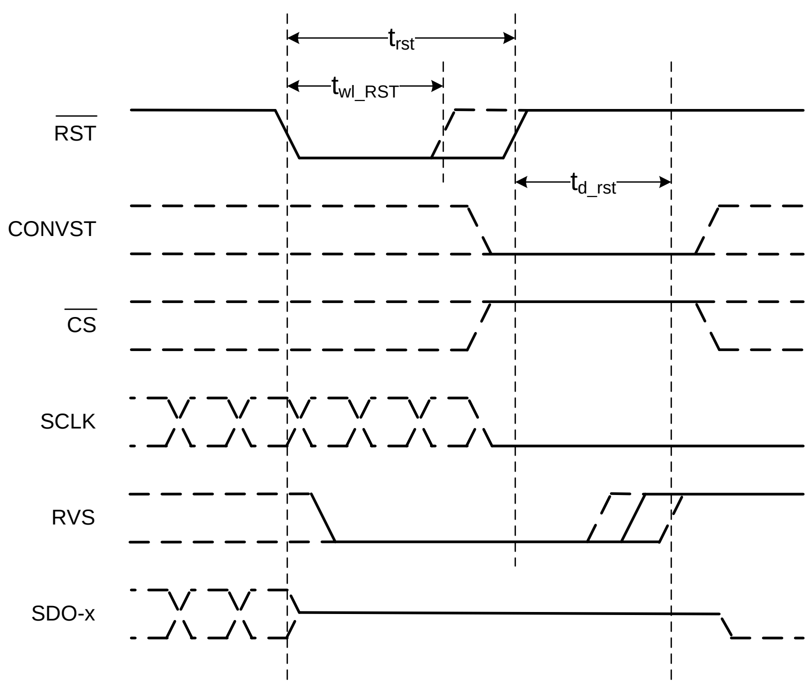


Figure 2. Asynchronous Reset Timing Diagram

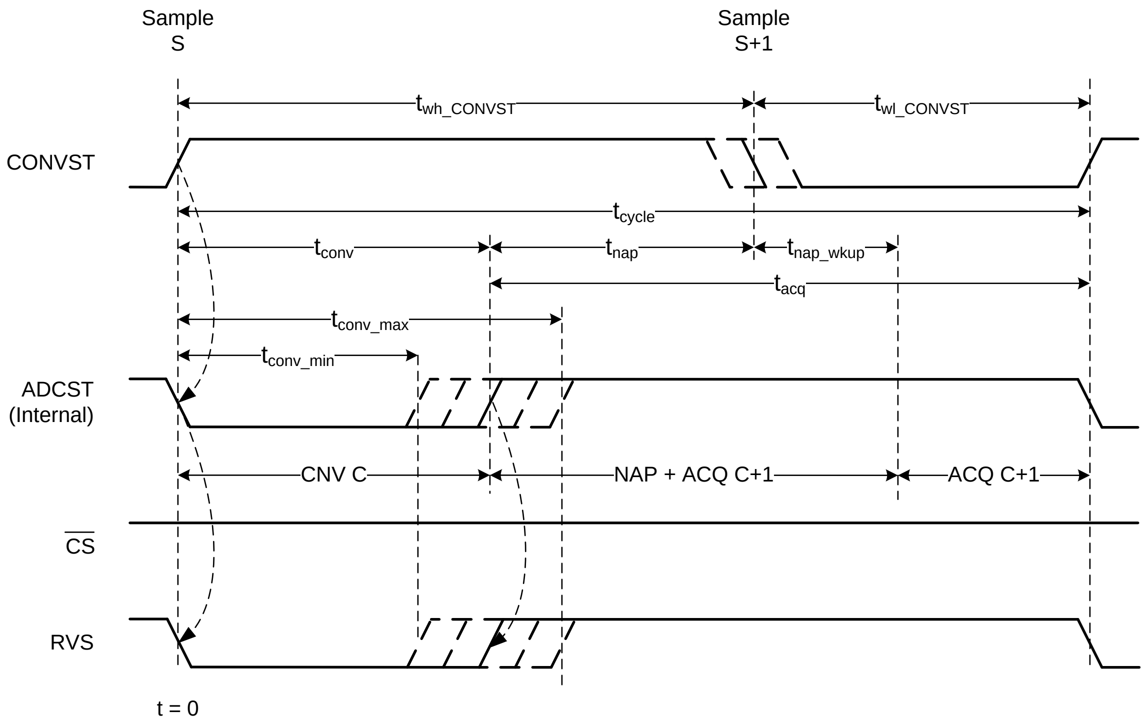
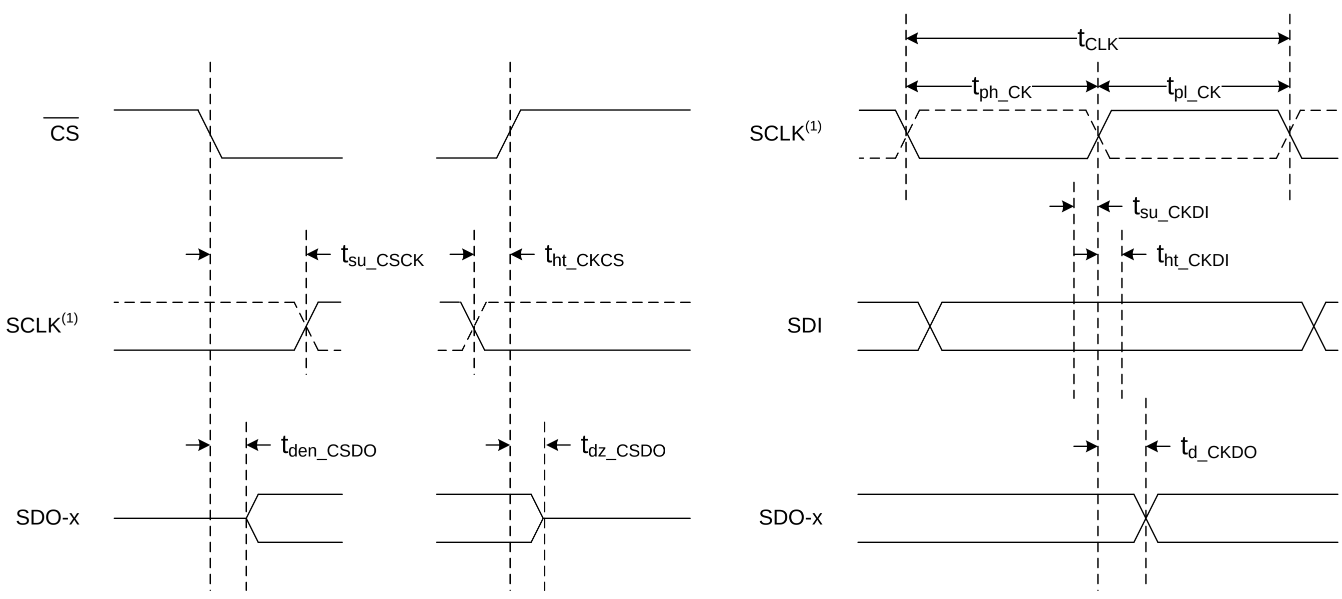


Figure 3. NAP Mode Timing Diagram



(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

Figure 4. SPI-Compatible Serial Interface Timing Diagram

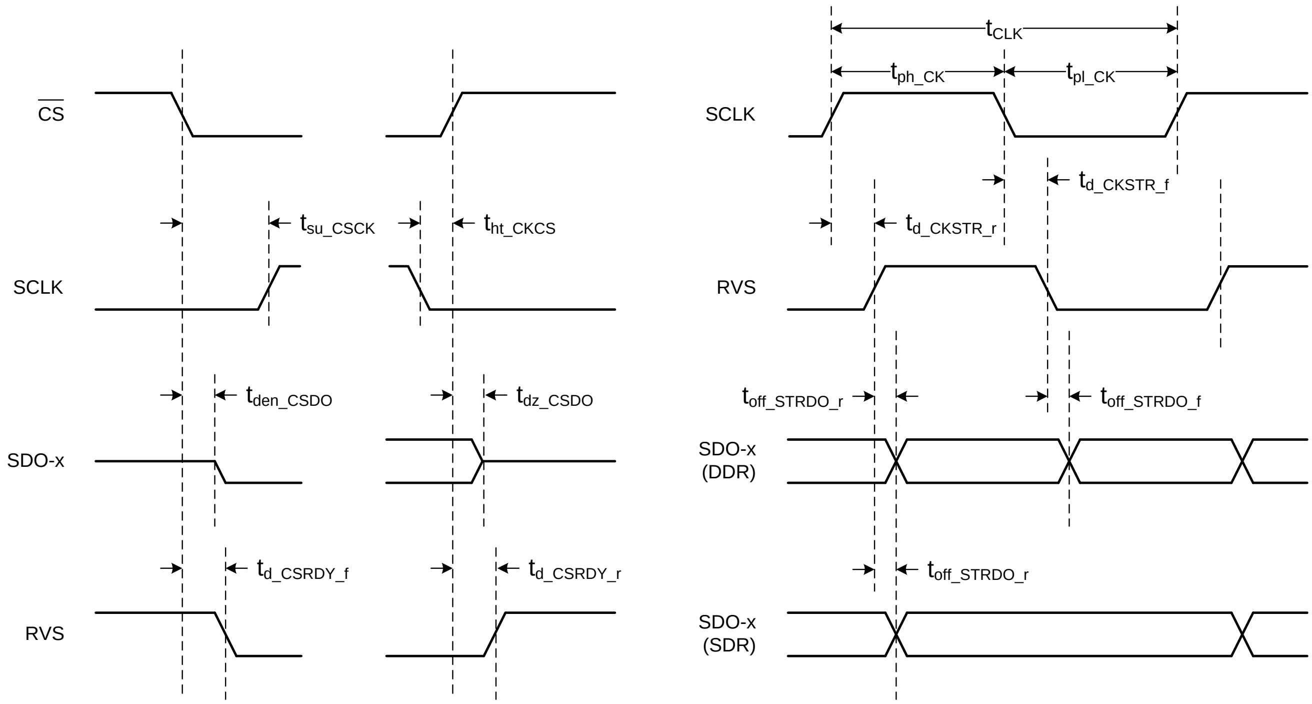


Figure 5. Source-Synchronous Serial Interface Timing Diagram (External Clock)

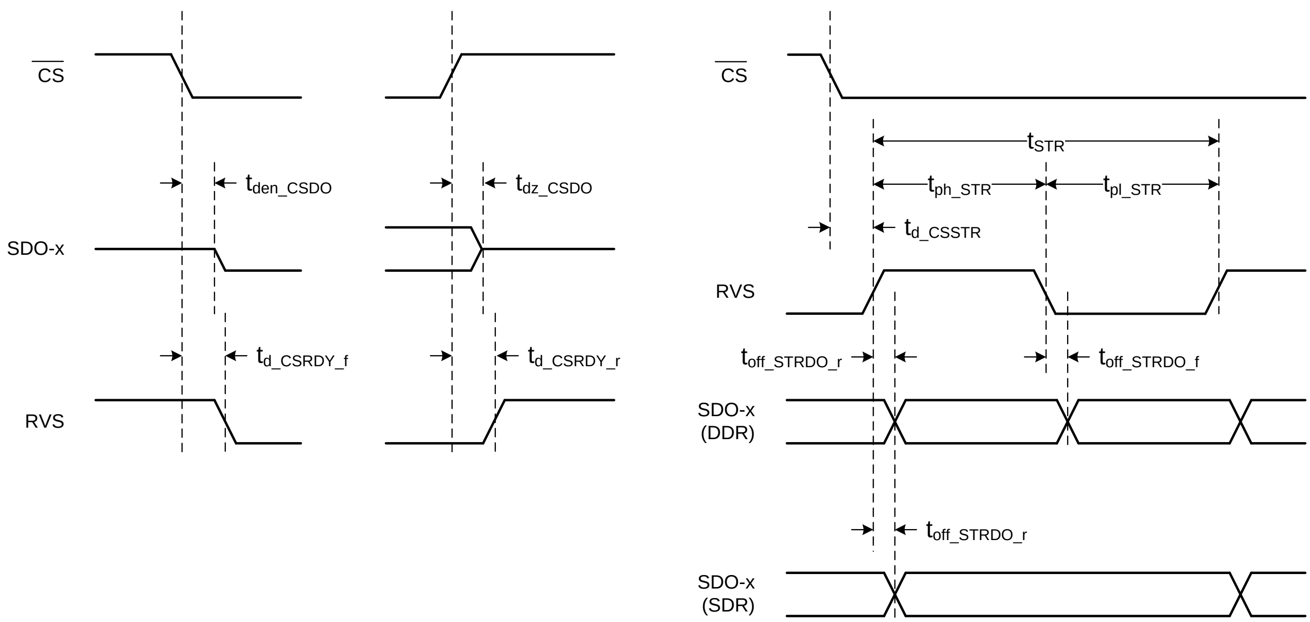
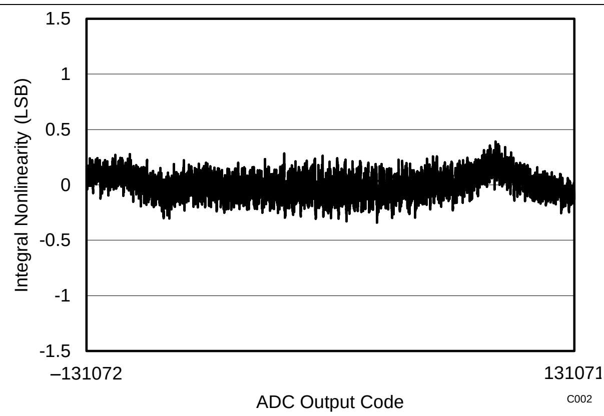


Figure 6. Source-Synchronous Serial Interface Timing Diagram (Internal Clock)

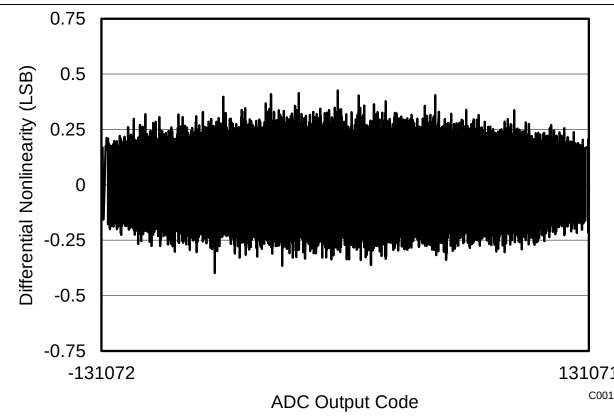
6.11 Typical Characteristics

At T_A = 25°C, AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.



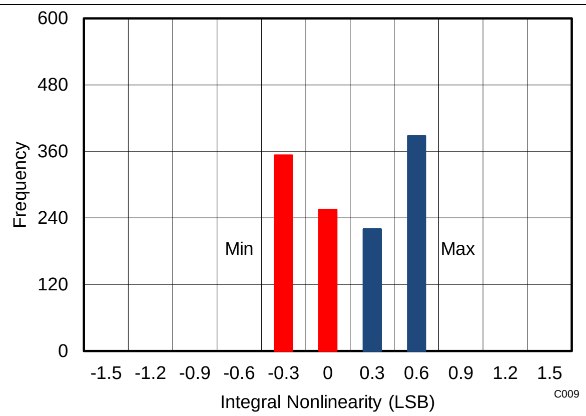
Typical INL = ±0.5 LSB

Figure 7. Typical INL



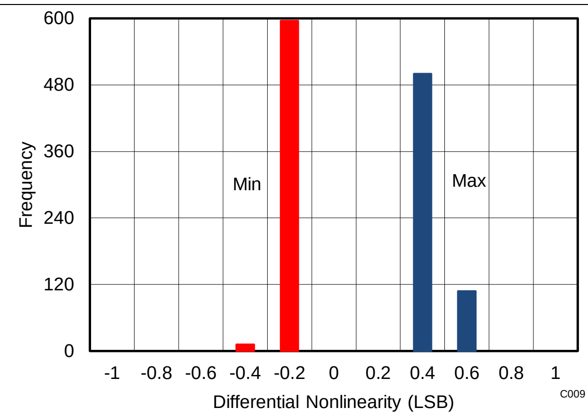
Typical DNL = ±0.4 LSB

Figure 8. Typical DNL



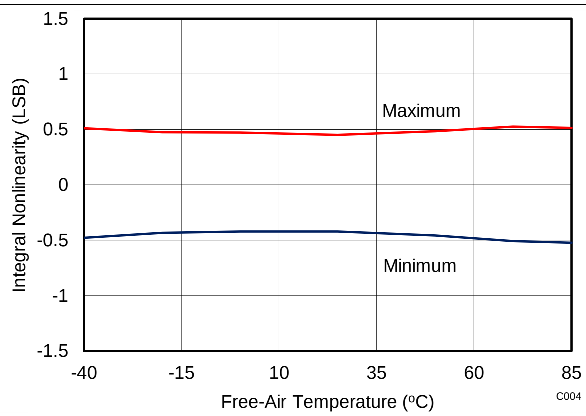
600 devices

Figure 9. Typical INL Distribution



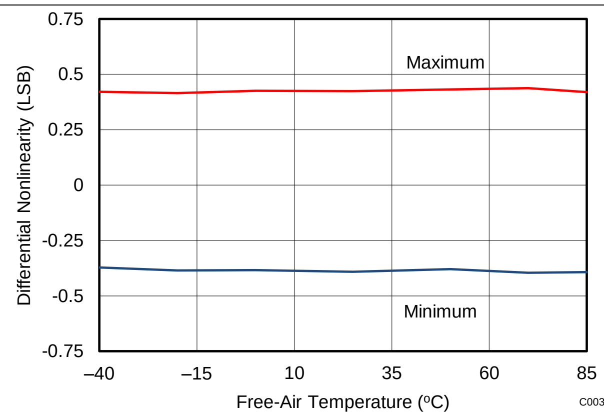
600 devices

Figure 10. Typical DNL Distribution



V_{REF} = 5 V

Figure 11. INL vs Temperature

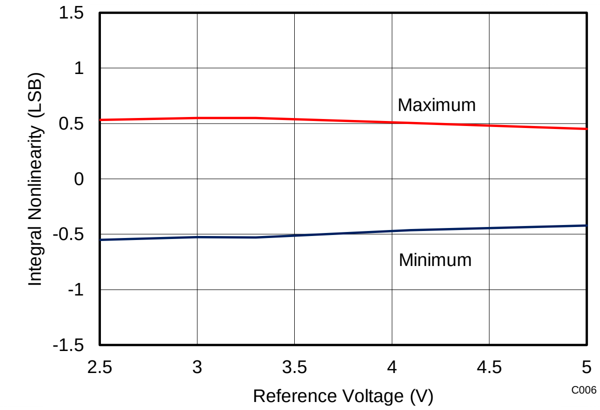


V_{REF} = 5 V

Figure 12. DNL vs Temperature

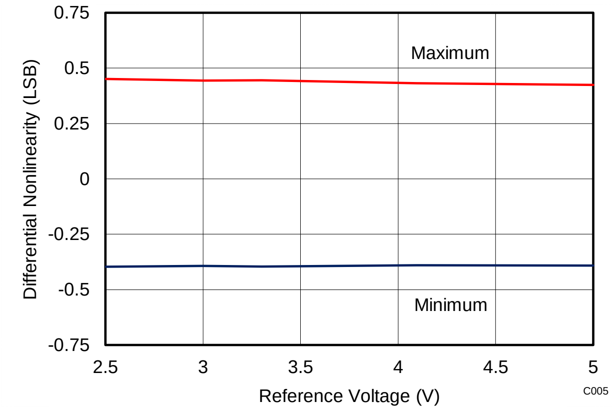
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.



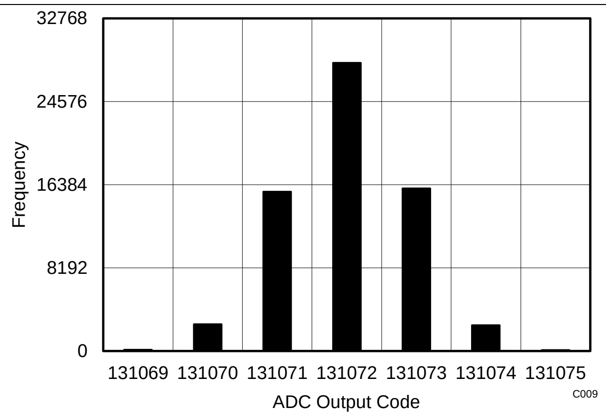
T_A = 25°C

Figure 13. INL vs Reference Voltage



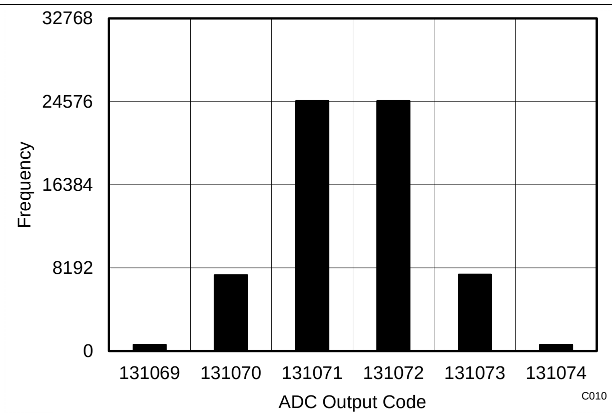
T_A = 25°C

Figure 14. DNL vs Reference Voltage



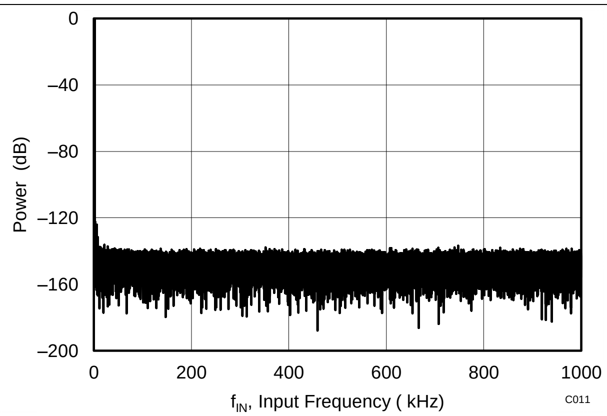
Standard deviation = 0.9 LSB

Figure 15. DC Input Histogram, Code Ceter



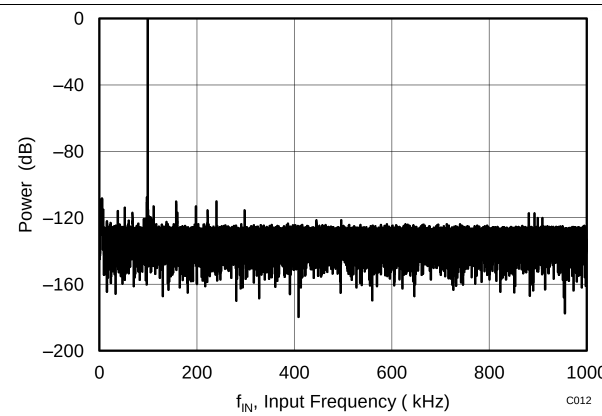
Standard deviation = 0.9 LSB

Figure 16. DC Input Histogram, Code Transition



f_{IN} = 2 kHz, SNR = 100 dB, THD = –120 dB

Figure 17. Typical FFT

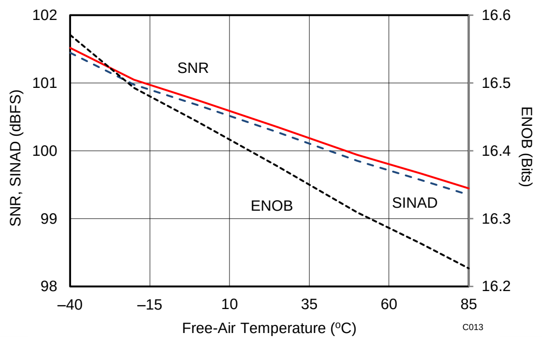


f_{IN} = 100 kHz, SNR = 97.5 dB, THD = –113 dB

Figure 18. Typical FFT

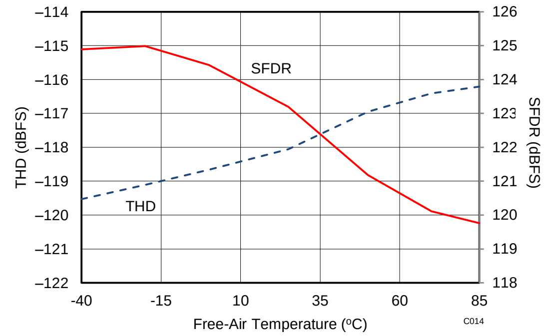
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.



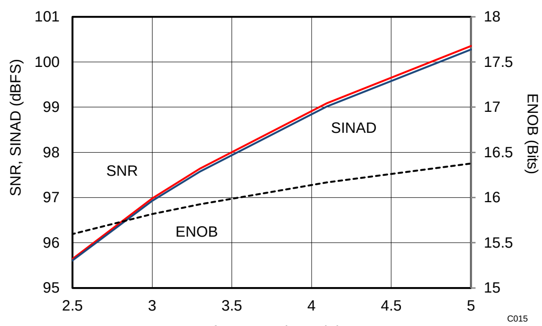
f_{IN} = 2 kHz, V_{REF} = 5 V

Figure 19. Noise Performance vs Temperature



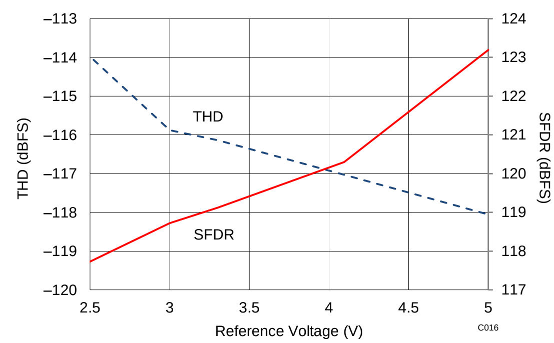
f_{IN} = 2 kHz, V_{REF} = 5 V

Figure 20. Distortion Performance vs Temperature



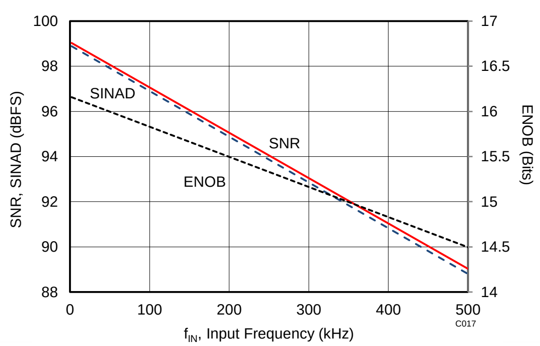
f_{IN} = 2 kHz, T_A = 25°C

Figure 21. Noise Performance vs Reference Voltage



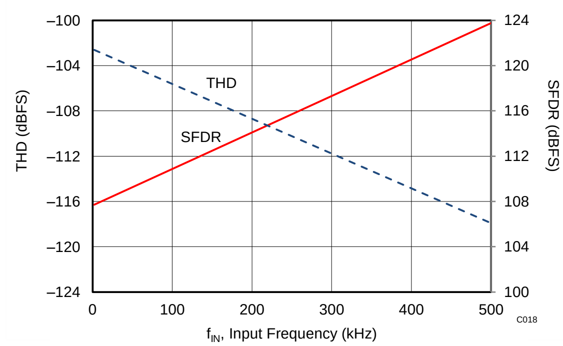
f_{IN} = 2 kHz, T_A = 25°C

Figure 22. Distortion Performance vs Reference Voltage



V_{REF} = 5 V, T_A = 25°C

Figure 23. Noise Performance vs Input Frequency

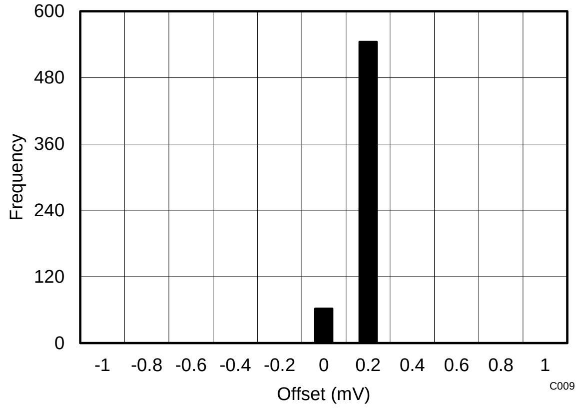


V_{REF} = 5 V, T_A = 25°C

Figure 24. Distortion Performance vs Input Frequency

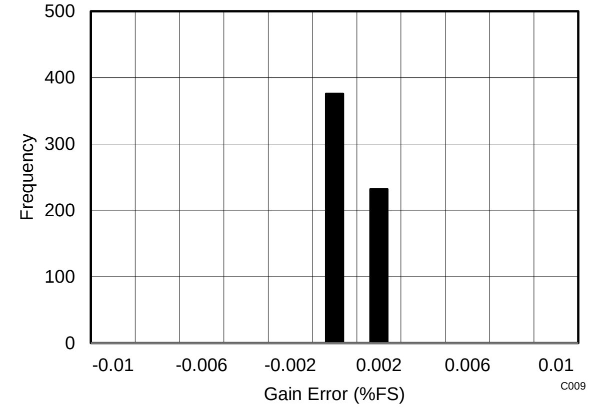
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.



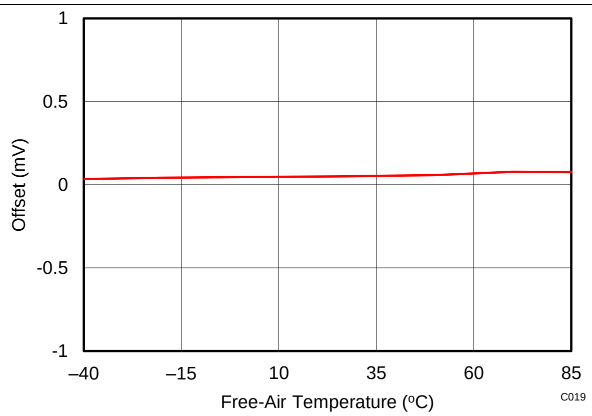
600 devices

Figure 25. Offset Typical Distribution



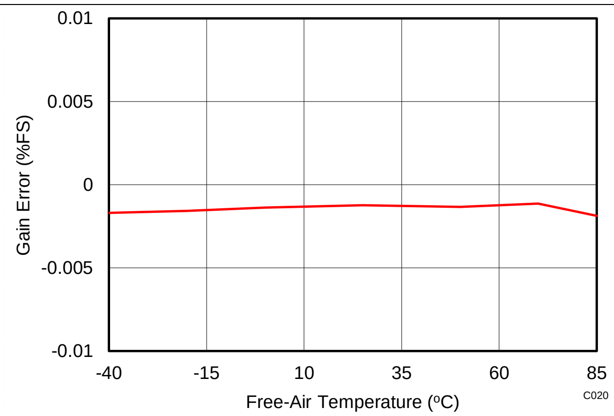
600 devices

Figure 26. Gain Error Typical Distribution



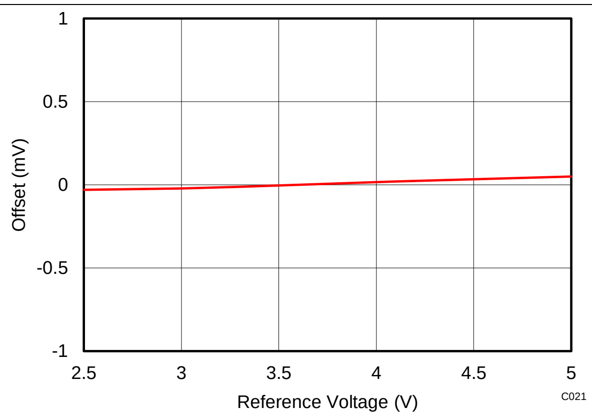
V_{REF} = 5 V

Figure 27. Offset vs Temperature



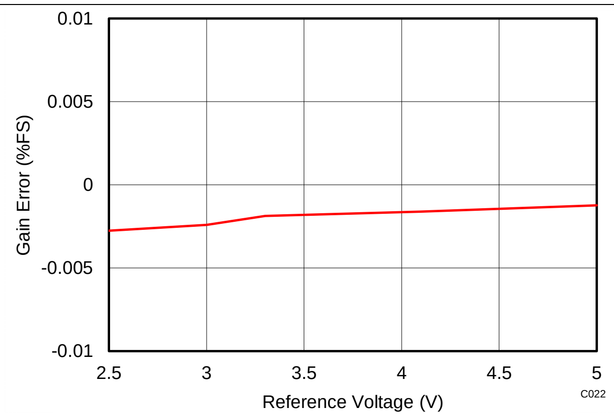
V_{REF} = 5 V

Figure 28. Gain Error vs Temperature



T_A = 25°C

Figure 29. Offset vs Reference Voltage



T_A = 25°C

Figure 30. Gain Error vs Reference Voltage

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 1.8 V, DVDD = 1.8 V, V_{REF} = 5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

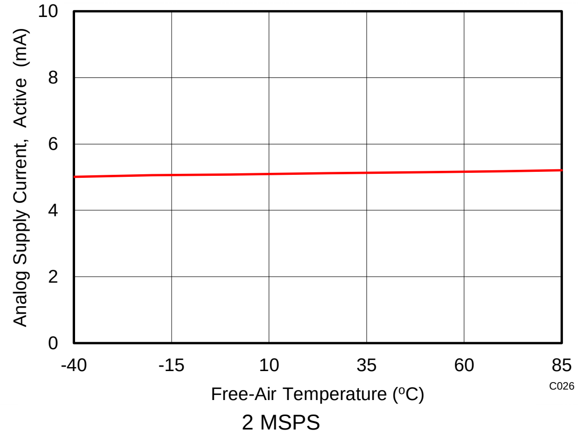


Figure 31. Supply Current vs Temperature

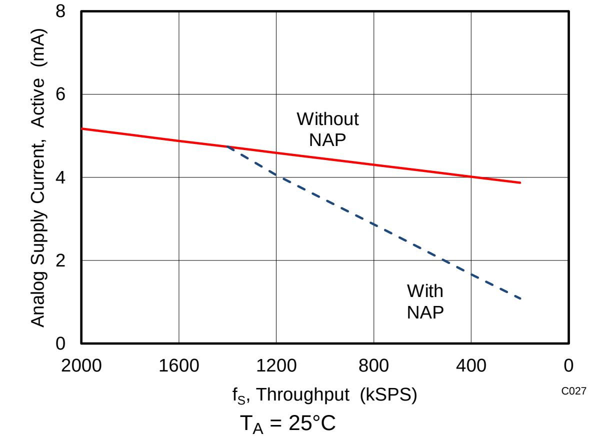


Figure 32. Supply Current vs Throughput

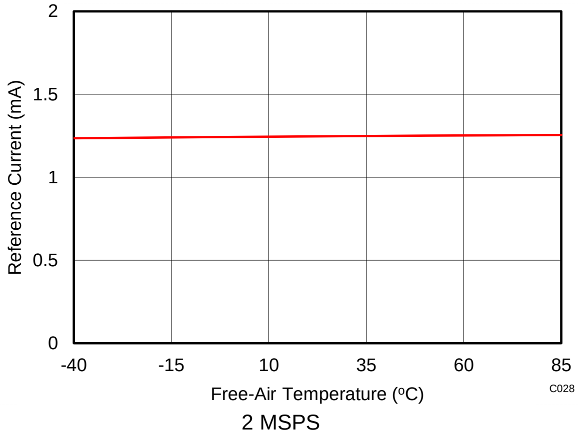


Figure 33. Reference Current vs Temperature

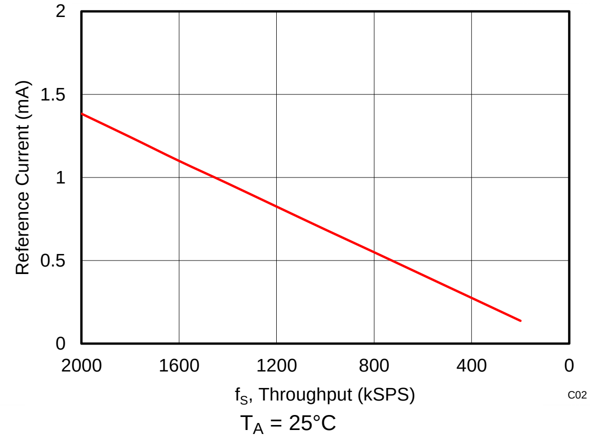


Figure 34. Reference Current vs Throughput

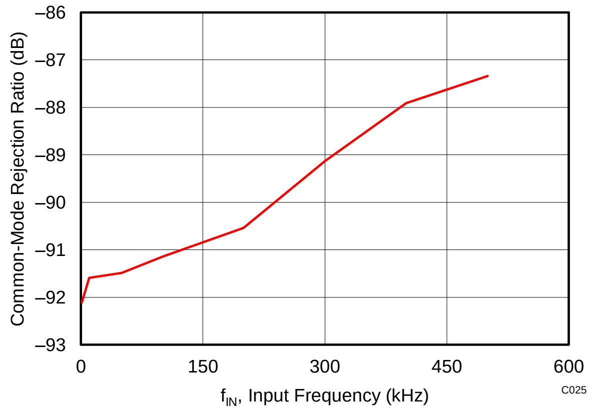


Figure 35. CMRR vs Input Frequency

7 Detailed Description

7.1 Overview

The ADS9110 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) based on the charge redistribution architecture. This compact device features high performance at a high throughput rate and at low power consumption.

The ADS9110 supports unipolar, fully-differential analog input signals and operates with a 2.5-V to 5-V external reference, offering a wide selection of input ranges without additional input scaling.

When a conversion is initiated, the differential input between the AINP and AINM pins is sampled on the internal capacitor array. The ADS9110 uses an internal clock to perform conversions. During the conversion process, both analog inputs are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the AINP and AINM pins and enters acquisition phase.

The device consumes only 15 mW of power when operating at the full 2-MSPS throughput. Power consumption at lower throughputs can be reduced by using the flexible low-power modes (NAP and PD).

The new multiSPI interface simplifies board layout, timing, and firmware, and achieves high throughput at lower clock speeds, thus allowing easy interface to a variety of microprocessors, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

7.2 Functional Block Diagram

From a functional perspective, the device comprises of two modules: the converter module and the interface module, as shown in Figure 36.

The converter module samples and converts the analog input into an equivalent digital output code whereas the interface module facilitates communication and data transfer with the host controller.

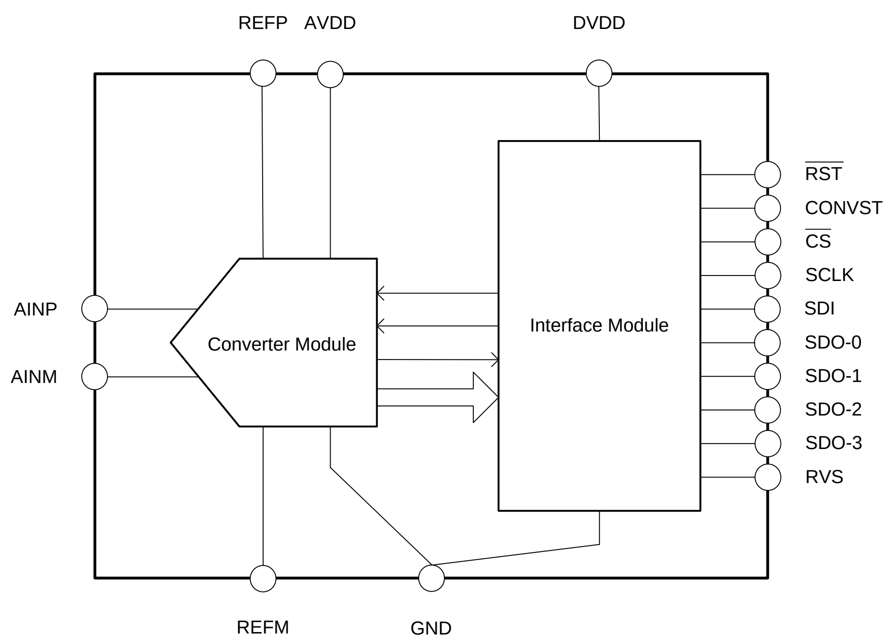


Figure 36. Functional Block Diagram

7.3 Feature Description

7.3.1 Converter Module

As shown in Figure 37, the converter module samples the analog input signal (provided between the AINP and AINM pins), compares this signal with the reference voltage (provided between the pair of REFP and REFM pins), and generates an equivalent digital output code.

The converter module receives $\overline{\text{RST}}$ and CONVST inputs from the interface module and outputs the ADCST signal and the conversion result back to the interface module.

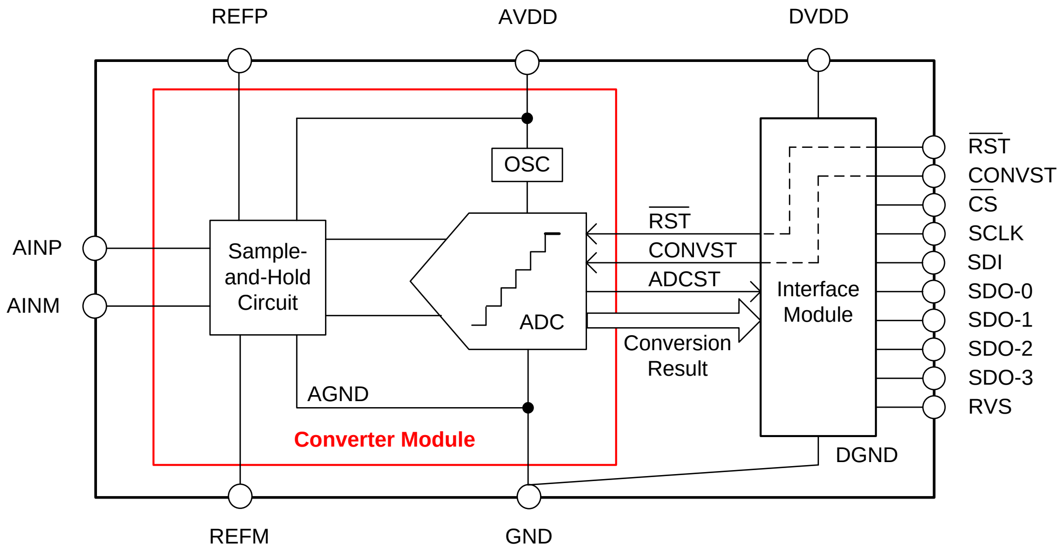


Figure 37. Converter Module

7.3.1.1 Sample-and-Hold Circuit

The device supports unipolar, fully-differential analog input signals. Figure 38 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance (R_{s1} and R_{s2}, typically 30 Ω) in series with an ideal switch (sw_1 and sw_2). The sampling capacitors, C_{s1} and C_{s2}, are typically 60 pF.

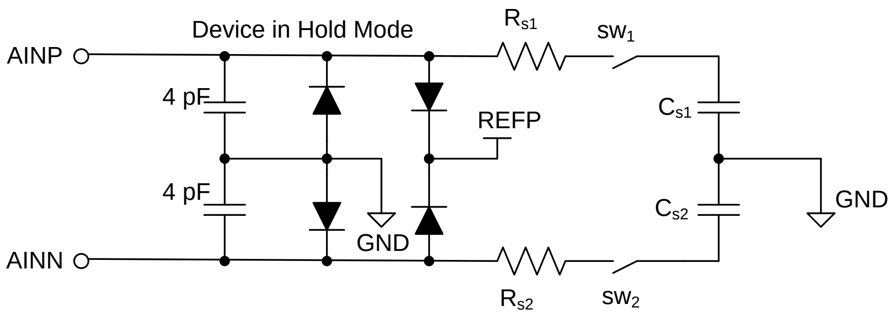


Figure 38. Input Sampling Stage Equivalent Circuit

During the acquisition process (in ACQ state), both positive and negative inputs are individually sampled on C_{s1} and C_{s2}, respectively. During the conversion process (in CNV state), the device converts for the voltage difference between the two sampled values: $V_{AINP} – V_{AINM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to REFP and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

Feature Description (continued)

Equation 1 and Equation 2 show the full-scale voltage range (FSR) and common-mode voltage range (V_{CM}) supported at the analog inputs for any external reference voltage (V_{REF}).

$$FSR = \pm V_{REF} \quad (1)$$

$$V_{CM} = \left(\frac{V_{REF}}{2}\right) \pm 0.1\ V \quad (2)$$

7.3.1.2 External Reference Source

The input range for the device is set by the external voltage applied at the two REFP pins. The REFM pins function as the reference ground and must be connected to each reference capacitor.

The device takes very little static current from the reference pins in the RST and ACQ states. During the conversion process (in CNV state), binary-weighted capacitors are switched onto the reference pins. The switching frequency is proportional to the conversion clock frequency, but the dynamic charge requirements are a function of the absolute values of the input voltage and the reference voltage. Reference capacitors decouple the dynamic reference loads and a low-impedance reference driver is required to keep the voltage regulated to within 1 LSB.

Most reference sources have very high broadband noise. TI recommends filtering the voltage reference source with a 160-Hz filter before being connected to the reference driver, as shown in Figure 39. See the *ADC Reference Driver* section for reference capacitor and driver selection. Also, the reference inputs are sensitive to board layout; thus, the layout guidelines described in the *Layout* section must be followed.

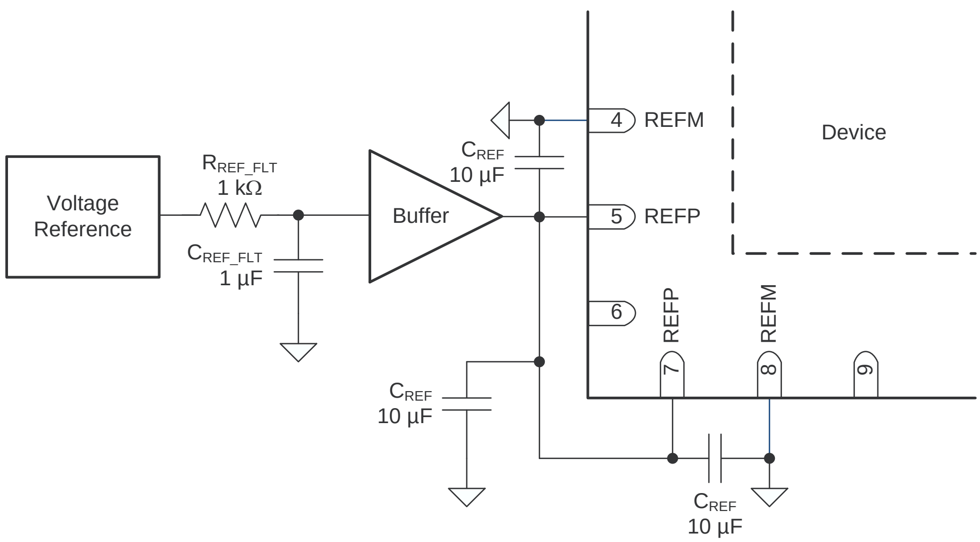


Figure 39. Reference Driver Schematic

7.3.1.3 Internal Oscillator

The device features an internal oscillator (OSC) that provides the conversion clock; see Figure 37. Conversion duration can vary but is bounded by the minimum and maximum value of t_{conv}, as specified in the *Timing Requirements: Conversion Cycle* table.

The interface module can use this internal clock (OSC) or an external clock (provided by the host controller on the SCLK pin) or a combination of the internal and external clocks for executing the data transfer operations between the device and host controller; see the *Interface Module* section for more details.

Feature Description (continued)

7.3.1.4 ADC Transfer Function

The ADS9110 supports unipolar, fully-differential analog inputs. The device output is in twos compliment format. Figure 40 and Table 1 show the ideal transfer characteristics for the device.

The LSB for the ADC is given by Equation 3:

$$1\ \text{LSB} = \frac{FSR}{2^{18}} = 2 \times \frac{V_{REF}}{2^{18}} \tag{3}$$

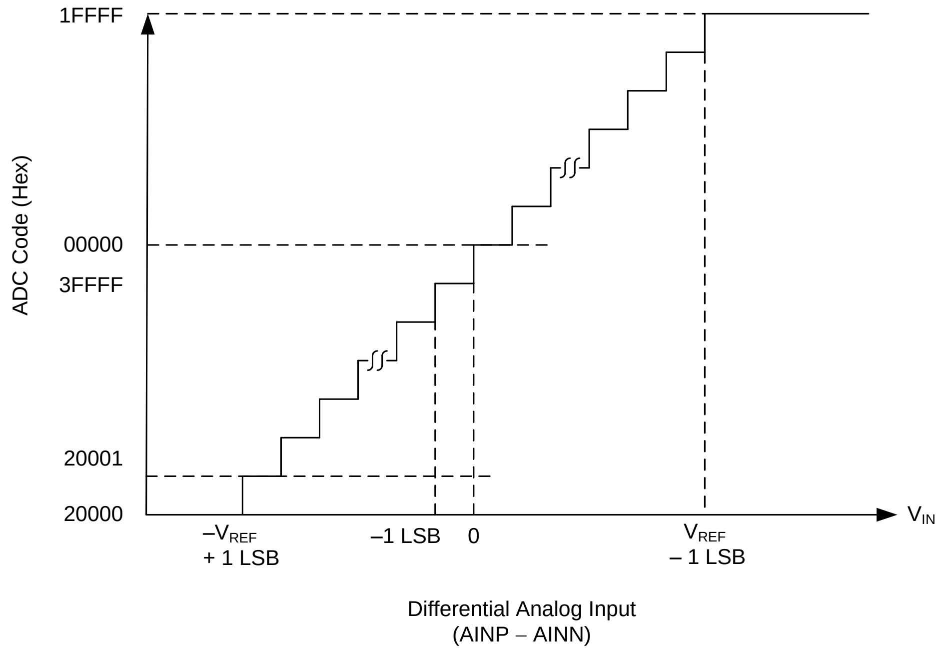


Figure 40. Differential Transfer Characteristics

Table 1. Transfer Characteristics

DIFFERENTIAL ANALOG INPUT VOLTAGE (AINP – AINM)	OUTPUT CODE (Hex)
< $–V_{REF}$	20000
$–V_{REF}$ + 1 LSB	20001
–1 LSB	3FFFF
0	00000
1 LSB	00001
> V_{REF} – 1 LSB	1FFFF

7.3.2 Interface Module

The interface module facilitates the communication and data transfer between the device and the host controller. As shown in Figure 41, the module comprises of shift registers (both input and output), configuration registers, and a protocol unit.

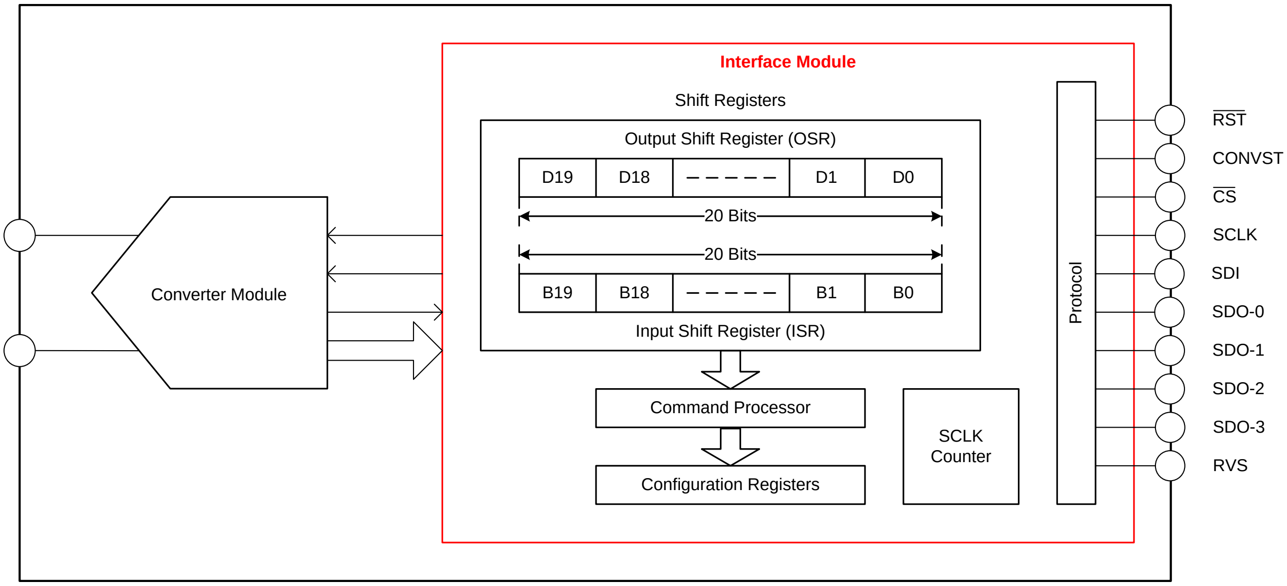


Figure 41. Interface Module

The *Pin Configuration and Functions* section provides descriptions of the interface pins; the *Data Transfer Frame* section details the functions of shift registers, the SCLK counter, and the command processor; the *Data Transfer Protocols* section details supported protocols; and the *Register Maps* section explains the configuration registers and bit settings.

7.4 Device Functional Modes

As shown in Figure 42, the device supports three functional states: RST, ACQ, and CNV. The device state is determined by the status of the CONVST and RST control signals provided by the host controller.

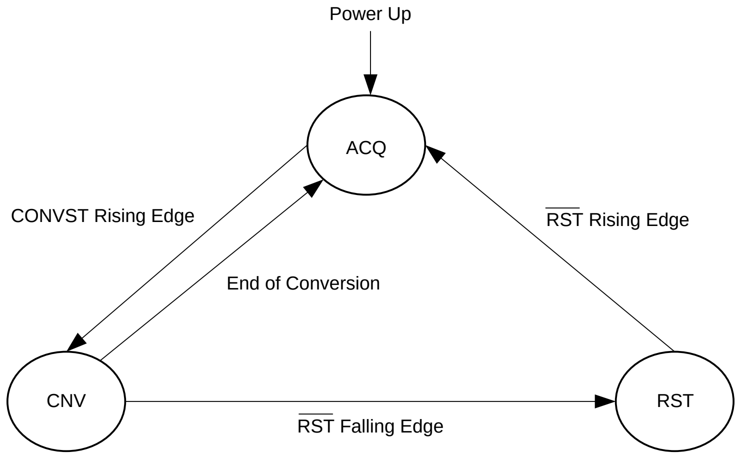


Figure 42. Device Functional States

7.4.1 RST State

In the ADS9110, the RST pin is an asynchronous digital input. To enter RST state, the host controller must pull the RST pin low and keep it low for the t_{wl_RST} duration (as specified in the *Timing Requirements: Asynchronous Reset, NAP, and PD* table).

In RST state, all configuration registers (see the *Register Maps* section) are reset to their default values, the RVS pins remain low, and the SDO-x pins are tri-stated.

To exit RST state, the host controller must pull the RST pin high with CONVST and SCLK held low and CS held high, as shown in Figure 43. After a delay of t_{d_rst}, the device enters ACQ state and the RVS pin goes high.

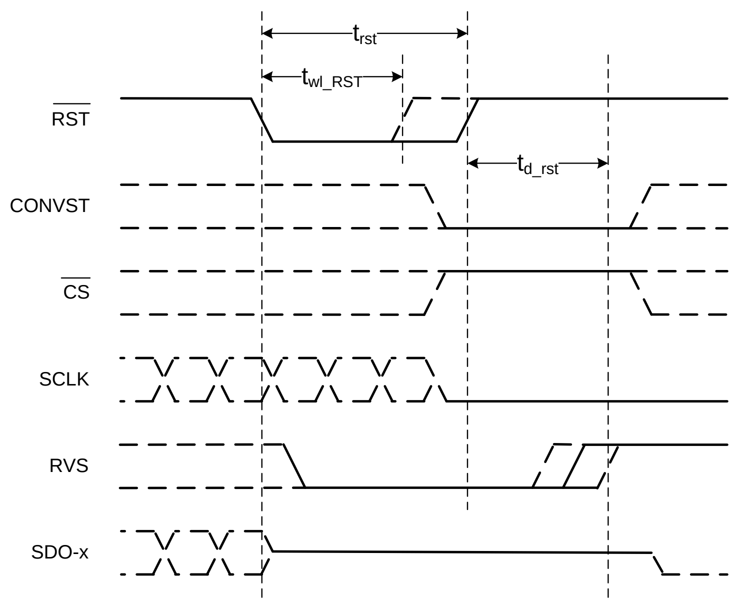


Figure 43. Asynchronous Reset

To operate the device in any of the other two states (ACQ or CNV), RST must be held high. With RST held high, transitions on the CONVST pin determine the functional state of the device.

Device Functional Modes (continued)

Figure 44 shows a typical conversion process. An internal signal, ADCST, goes low during conversion and goes high at the end of conversion. With CS held high, RVS reflects the status of ADCST.

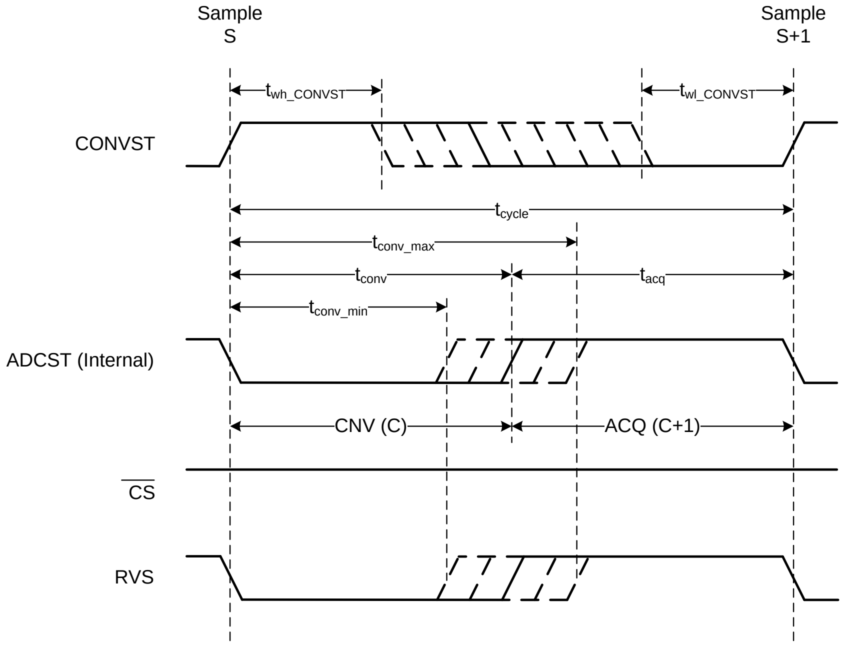


Figure 44. Typical Conversion Process

7.4.2 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state on power-up, after any asynchronous reset, or after end of every conversion.

An RST falling edge takes the device from an ACQ state to a RST state. A CONVST rising edge takes the device from an ACQ state to a CNV state.

The device offers a low-power NAP mode to reduce power consumption in the ACQ state; see the *NAP Mode* section for more details on NAP mode.

7.4.3 CNV State

The device moves from ACQ state to CNV state on a rising edge of the CONVST pin. The conversion process uses an internal clock and the device ignores any further transitions on the CONVST signal until the ongoing conversion is complete (that is, during the time interval of t_{conv}).

At the end of conversion, the device enters ACQ state. The cycle time for the device is given by Equation 4:

$$t_{cycle\text{-}min} = t_{conv} + t_{acq\text{-}min} \quad (4)$$

NOTE

The conversion time, t_{conv}, can vary within the specified limits of t_{conv_min} and t_{conv_max} (as specified in the *Timing Requirements: Conversion Cycle* table). After initiating a conversion, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the t_{conv_max} duration to elapse before initiating a new operation (data transfer or conversion). If RVS is not monitored, substitute t_{conv} in Equation 4 with t_{conv_max}.

7.5 Programming

The device features four configuration registers (as described in the *Register Maps* section) and supports two types of data transfer operations: *data write* (the host configures the device), and *data read* (the host reads data from the device).

To access the internal configuration registers, the device supports the commands listed in Table 2.

Table 2. Supported Commands

OPCODE B[19:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
0000_0000_0000_0000_0000	NOP	No operation
1001_<8-bit address>_0000_0000	RD_REG	Read contents from the <8-bit address>
1010_<8-bit address>_<8-bit data>	WR_REG	Write <8-bit data> to the <8-bit address>
1111_1111_1111_1111_1111	NOP	No operation
Remaining combinations	Reserved	These commands are reserved and treated by the device as no operation

In the ADS9110, any data write to the device is always synchronous to the external clock provided on the SCLK pin. The data read from the device can be synchronized to the same external clock or to an internal clock of the device by programming the configuration registers (see the *Data Transfer Protocols* section for details).

In any data transfer frame, the contents of an internal, 20-bit, output data word are shifted out on the SDO pins. The D[19:2] bits of the 20-bit output data word for any frame (F+1), are determined by the:

- Settings of the DATA_PATN[2:0] bits applicable to frame F+1 (see the DATA_CNTL register) and
- Command issued in frame F

If a valid RD_REG command is executed in frame F, then the D[19:12] bits in frame F+1 reflect the contents of the selected register and the D[11:0] bits are 0s.

If the DATA_PATN[2:0] bits for frame F+1 are set to 1xxb, then the D[19:2] bits in frame F+1 are the fixed data pattern shown in Figure 45.

For all other combinations, the D[19:2] bits for frame F+1 are the latest conversion result.

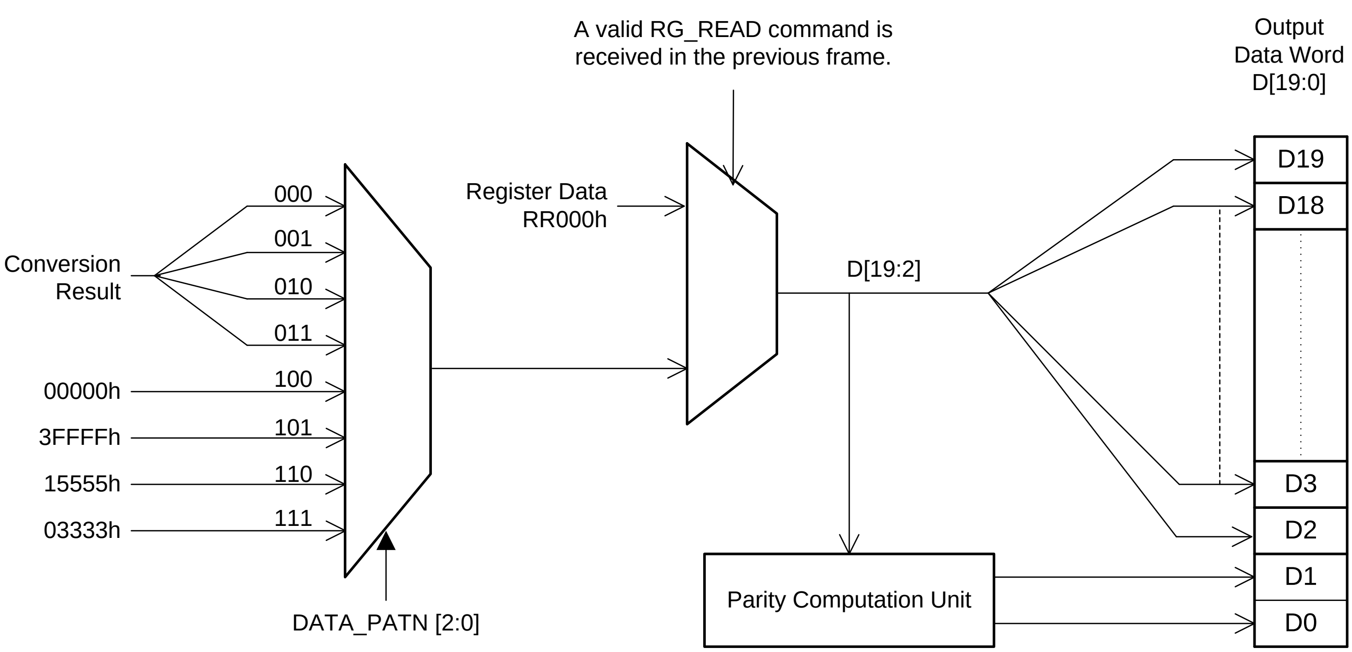


Figure 45. Output Data Word (D[19:0])

Figure 46 shows further details of the parity computation unit illustrated in Figure 45.

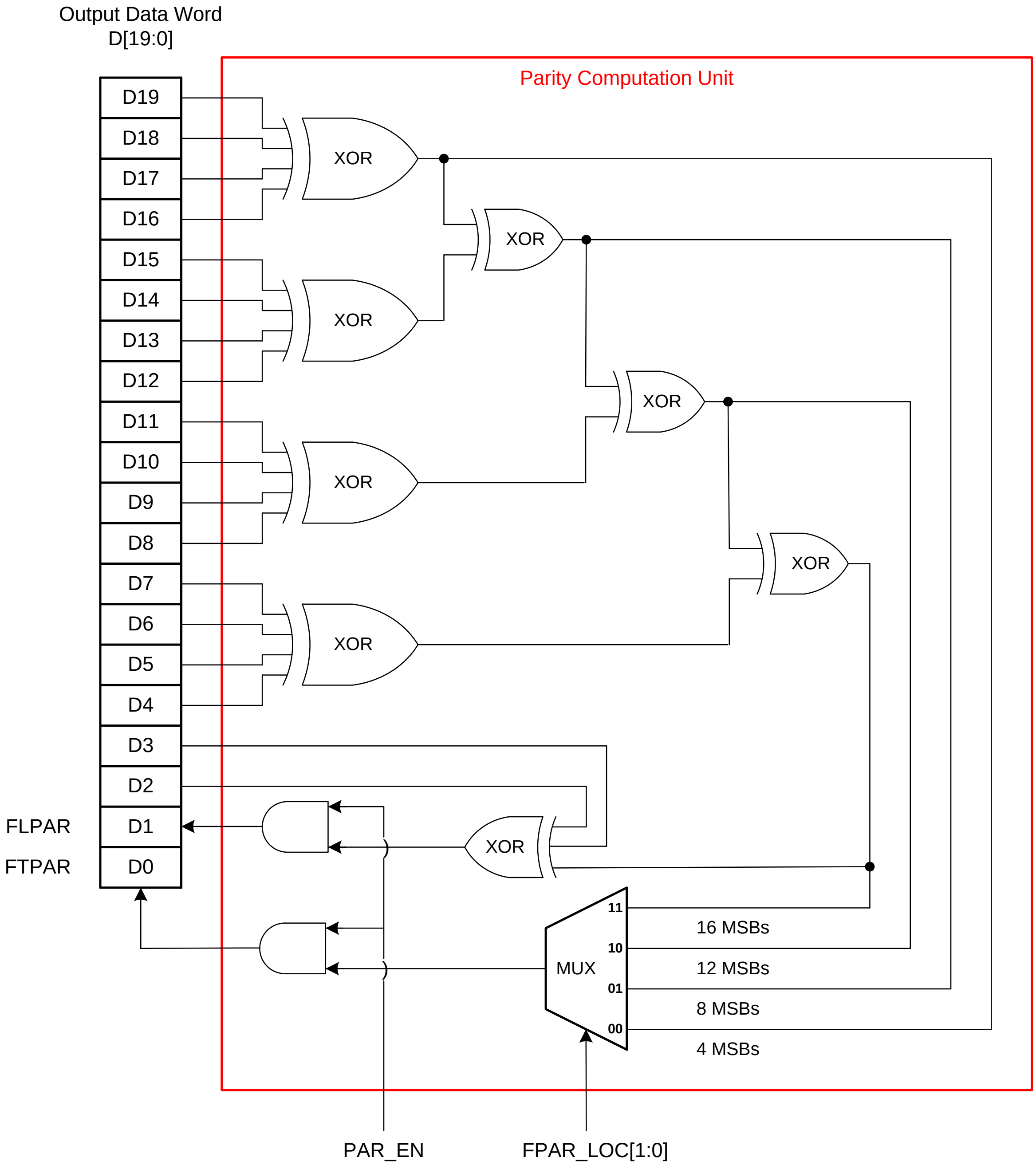


Figure 46. Parity Bits Computation

With the PAR_EN bit set to 0, the D[1] and D[0] bits of the output data word are set to 0 (default configuration).

When the PAR_EN bit is set to 1, the device calculates the parity bits (FLPAR and FTPAR) and appends them as bits D[1] and D[0].

- FLPAR is the even parity calculated on bits D[19:2].
- FTPAR is the even parity calculated on the bits defined by FPAR_LOC[1:0].

See the DATA_CNTL register for more details on the FPAR_LOC[1:0] bit settings.

7.5.1 Data Transfer Frame

A data transfer frame between the device and the host controller is bounded between a $\overline{CS}$ falling edge and the subsequent $\overline{CS}$ rising edge. The host controller can initiate a data transfer frame (as shown in Figure 47) at any time irrespective of the status of the CONVST signal; however, the data read during such a data transfer frame is a function of relative timing between the CONVST and $\overline{CS}$ signals.

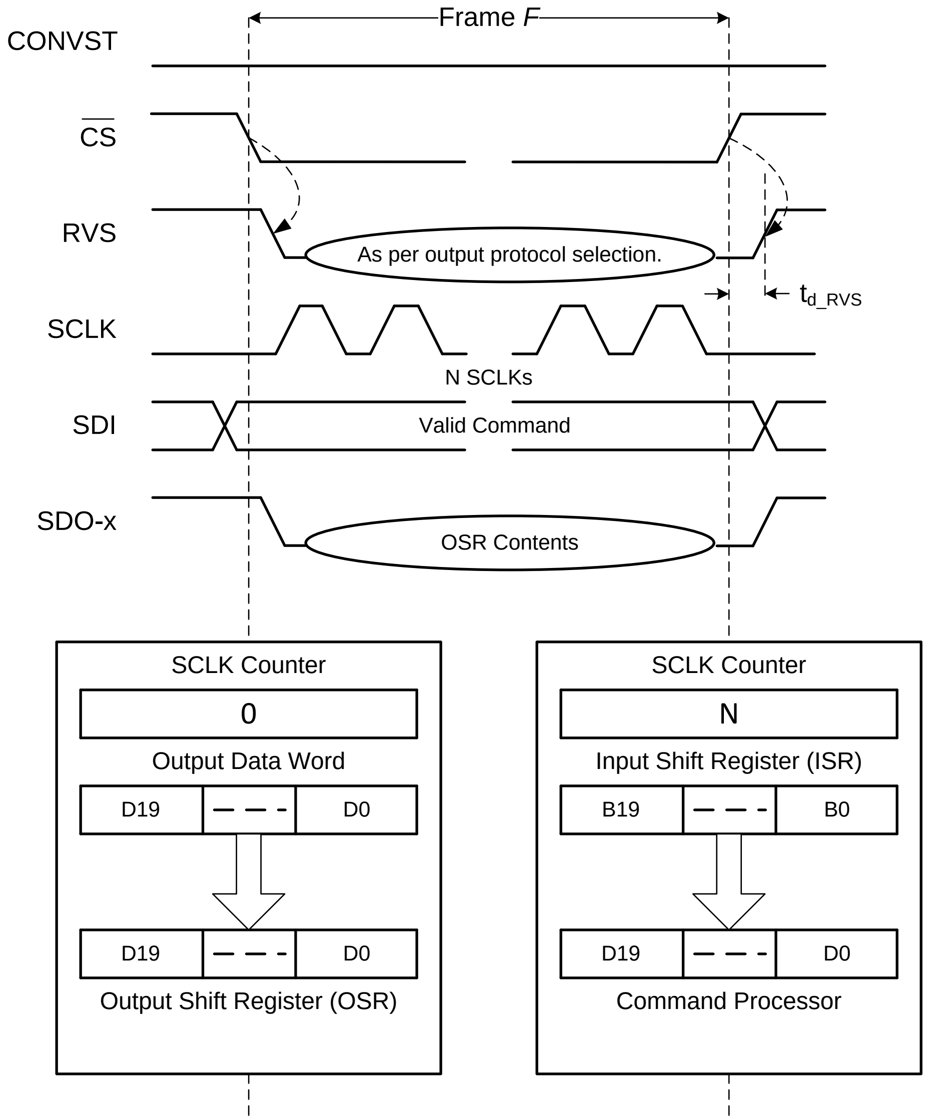


Figure 47. Data Transfer Frame

For this discussion, assume that the CONVST signal remains low.

For a typical data transfer frame F:

1. The host controller pulls $\overline{CS}$ low to initiate a data transfer frame. On the $\overline{CS}$ falling edge:
   – RVS goes low, indicating the beginning of the data transfer frame.
   – The SCLK counter is reset to 0.
   – The device takes control of the data bus. As shown in Figure 47, the 20-bit contents of the output data word (see Figure 45) are loaded in to the 20-bit OSR (see Figure 41).
   – The 20-bit ISR (see Figure 41) is reset to 00000h, corresponding to a NOP command.

2. During the frame, the host controller provides clocks on the SCLK pin:
   – On each SCLK capture edge, the SCLK counter is incremented and the data bit received on the SDI pin is shifted in to the ISR.
   – On each launch edge of the output clock (SCLK in this case), OSR data are shifted out on the selected SDO-x pins.
   – The status of the RVS pin depends on the output protocol selection (see the *Protocols for Reading From the Device* section).
3. The host controller pulls $\overline{CS}$ high to end the data transfer frame. On the $\overline{CS}$ rising edge:
   – The SDO-x pins go to tri-state.
   – RVS goes high (after a delay of t_{d_RVS}).
   – As illustrated in Figure 47, the 20-bit contents of the ISR are transferred to the command processor (see Figure 41) for decoding and further action.

After pulling $\overline{CS}$ high, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the t_{d_RVS} time (see the *Timing Requirements: SPI-Compatible Serial Interface* table) to elapse before initiating a new operation (data transfer or conversion). The delay, t_{d_RVS}, for any data transfer frame F varies based on the data transfer operation executed in the frame F.

At the end of the data transfer frame F:

- If the SCLK counter is < 20, then the device treats the frame F as a *short* data transfer frame. The output data bits transferred during such a short data transfer frame are still valid data; however, the device ignores the data received over the SDI pin (similar to a no operation command). The host controller can use these short data transfer frames to read only the required number of MSB bits from the 20-bit output data word.
- If the SCLK counter = 20, then the device treats the frame F as a *optimal* data transfer frame. At the end of an optimal data transfer frame, the command processor treats the 20-bit contents of the ISR as a valid command word.
- If the SCLK counter > 20, then the device treats the frame F as a *long* data transfer frame. At the end of a long data transfer frame, the command processor treats the 20-bit contents of the ISR as a valid command word. There is no restriction on the maximum number of clocks that can be provided within any data transfer frame F. However, when the host controller provides a long data transfer frame, the last 20 bits shifted into the device prior to the $\overline{CS}$ rising edge must constitute the desired command.

NOTE

This example shows a data transfer synchronous to the external clock provided on the SCLK pin. The device also supports data transfer operations that are synchronous to the internal clock; see the *Protocols for Reading From the Device* section for more details.

7.5.2 Interleaving Conversion Cycles and Data Transfer Frames

The host controller can operate the ADS9110 at the desired throughput by interleaving the conversion cycles and the data transfer frames.

The cycle time of the device, t_{cycle}, is the time difference between two consecutive CONVST rising edges provided by the host controller. The response time of the device, t_{resp}, is the time difference between the host controller initiating a conversion C and the host controller receiving the complete result for conversion C.

Figure 48 shows three conversion cycles, C, C+1, and C+2. Conversion C is initiated by a CONVST rising edge at the t = 0 time and the conversion result becomes available for data transfer at the t_{conv} time. However, this result is loaded into the OSR only on the subsequent $\overline{CS}$ falling edge. This $\overline{CS}$ falling edge must be provided before the completion of the conversion C+1 (that is, before the t_{cycle} + t_{conv} time).

To achieve the rated performance specifications, the host controller must ensure that no digital signals toggle during the quiet acquisition time (t_{qt_acq}) and quiet aperture time (t_{d_cnvcap}). Any noise during t_{d_cnvcap} can negatively affect the result of the ongoing conversion whereas any noise during t_{qt_acq} can negatively affect the result of the subsequent conversion.

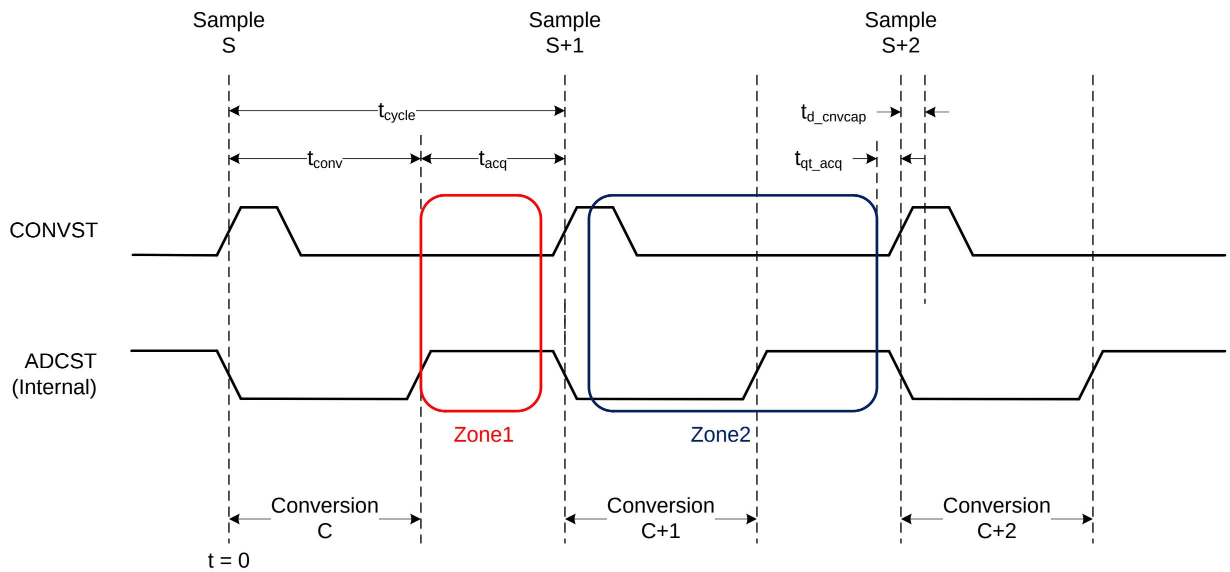


Figure 48. Data Transfer Zones

This architecture allows for two distinct time zones (zone1 and zone2) to transfer data for each conversion. Zone1 and zone2 for conversion C are defined in Table 3.

Table 3. Data Transfer Zones Timing

ZONE	STARTING TIME	ENDING TIME
Zone1 for conversion C	t_{conv}	$t_{cycle} - t_{qt\_acq}$
Zone2 for conversion C	$t_{cycle} + t_{d\_cnvcap}$	$t_{cycle} + t_{cycle} - t_{qt\_acq}$

The response time includes the conversion time and the data transfer time, and is thus a function of the data transfer zone selected.

Figure 49 and Figure 50 illustrate interleaving of three conversion cycles (C, C+1, and C+2) with three data transfer frames (F, F+1, and F+2) in zone1 and in zone2, respectively.

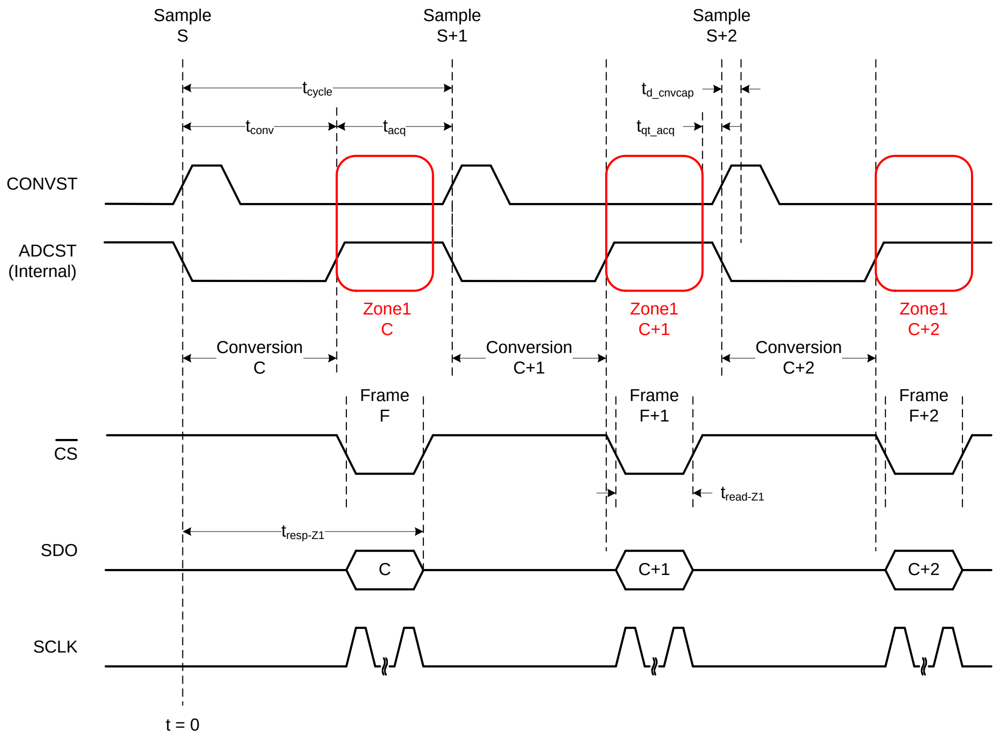


Figure 49. Zone1 Data Transfer

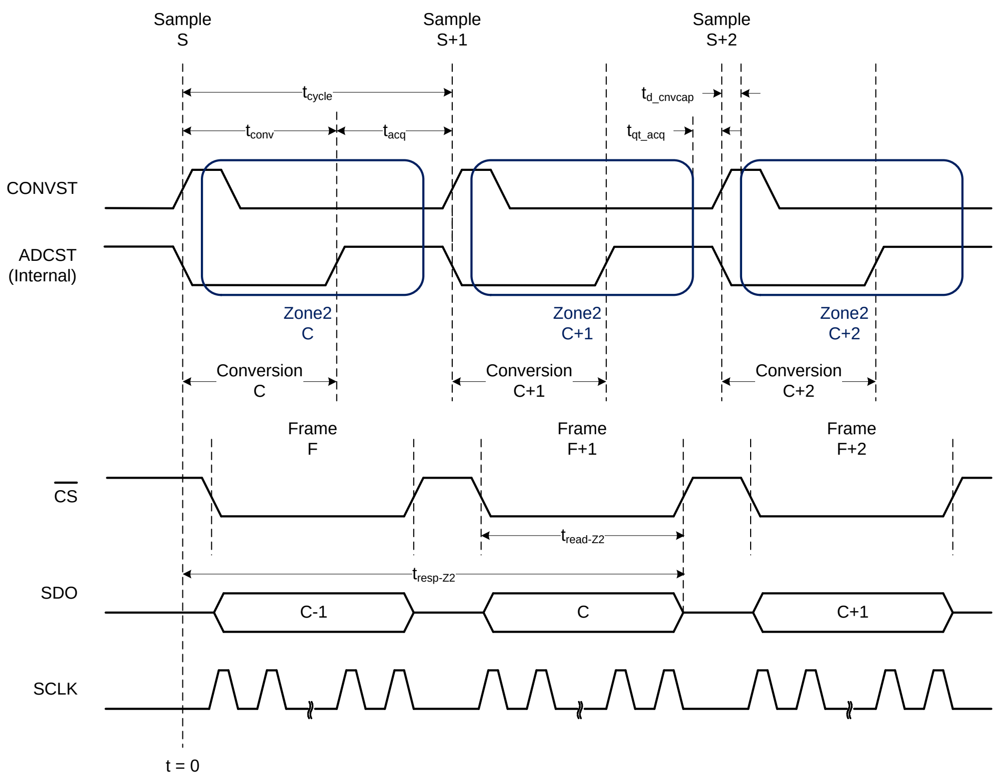


Figure 50. Zone2 Data Transfer

To achieve cycle time, t_{cycle}, the read time in zone1 is given by Equation 5:

$$t_{read\text{-}Z1} \le t_{cycle} - t_{conv} - t_{qt\_acq} \quad (5)$$

For an optimal data transfer frame, Equation 5 results in an SCLK frequency given by Equation 6:

$$f_{SCLK} \ge \frac{20}{t_{read\text{-}Z1}} \quad (6)$$

Then, the zone1 data transfer achieves a response time defined by Equation 7:

$$t_{resp\text{-}Z1\text{-}min} = t_{conv} + t_{read\text{-}Z1} \quad (7)$$

As an example, while operating the ADS9110 at its full throughput of 2 MSPS, the host controller can achieve a response time of 1 µs provided that the data transfer in zone1 is completed within 135 ns. However, to achieve this response time, the SCLK frequency must be greater than 148 MHz.

Note that the device does not support such high SCLK speeds. At lower SCLK speeds, $t_{read\text{-}Z1}$ increases, resulting in slower response times and higher cycle times.

To achieve the same cycle time, t_{cycle}, the read time in zone2 is given by Equation 8:

$$t_{read\text{-}Z2} \le t_{cycle} - t_{d\_cnvcap} - t_{qt\_acq} \quad (8)$$

For an optimal data transfer frame, Equation 8 results in an SCLK frequency given by Equation 9:

$$f_{SCLK} \ge \frac{20}{t_{read\_Z2}} \quad (9)$$

Then, the zone2 data transfer achieves a response time defined by Equation 10:

$$t_{resp\text{-}Z2\text{-}min} = t_{cycle} + t_{d\_cnvcap} + t_{read\text{-}Z2} \quad (10)$$

As an example, the host controller can operate the ADS9110 at its full throughput of 2 MSPS using zone2 data transfer with a 43 MHz SCLK (and a read time of 465 ns). However, zone2 data transfer will result in response time of nearly 2 µs.

Any increase in $t_{read\text{-}Z2}$ increases response time and can increase cycle time.

For a given cycle time, the zone1 data transfer clearly achieves faster response time but also requires a higher SCLK speed (as evident from Equation 5, Equation 6, and Equation 7), whereas the zone2 data transfer clearly requires a lower SCLK speed but supports slower response time (as evident from Equation 8, Equation 9, and Equation 10).

NOTE

In zone2, the data transfer is active when the device is converting for the next analog sample. This digital activity can interfere with the ongoing conversion and cause some degradation in SNR performance.

Additionally, a data transfer frame can begin in zone1 and then extend into zone2; however, the host controller must ensure that no digital transitions occur during the t_{qt_acq} and t_{d_cnvcap} time intervals.

7.5.3 Data Transfer Protocols

The device features a multiSPI interface that allows the host controller to operate at slower SCLK speeds and still achieve the required cycle time with a faster response time. The multiSPI interface module offers two options to reduce the SCLK speed required for data transfer:

1. An option to increase the width of the output data bus
2. An option to enable double data rate (DDR) transfer

These two options can be combined to achieve further reduction in SCLK speed.

Figure 51 shows the delays between the host controller and the device in a typical serial communication.

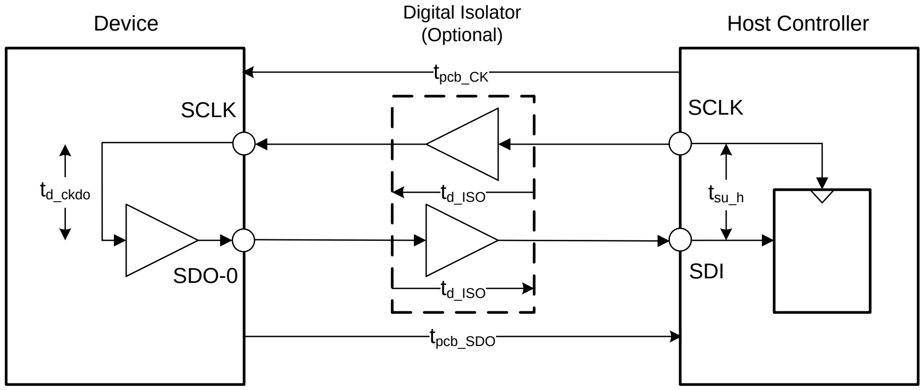


Figure 51. Delays in Serial Communication

The total delay in the path is given by Equation 11:

$$t_{d\_total\_serial} = t_{pcb\_CK} + t_{d\_iso} + t_{d\_ckdo} + t_{d\_iso} + t_{pcb\_SDO} + t_{su\_h} \quad (11)$$

In a standard SPI protocol, the host controller and the device launch and capture data bits on alternate SCLK edges. Therefore, the $t_{d\_total\_serial}$ delay must be kept less than half of the SCLK duration. Equation 12 shows the fastest clock allowed by the SPI protocol.

$$f_{clk\text{-}SPI} \leq \frac{1}{2 \times t_{d\_total\text{-}serial}} \quad (12)$$

Larger values of the $t_{d\_total\_serial}$ delay restrict the maximum SCLK speed for the SPI protocol, resulting in higher read and response times, and can increase cycle times. To remove this restriction on the SCLK speed, the multiSPI interface module supports an *ADC-master* or *source-synchronous* mode of operation.

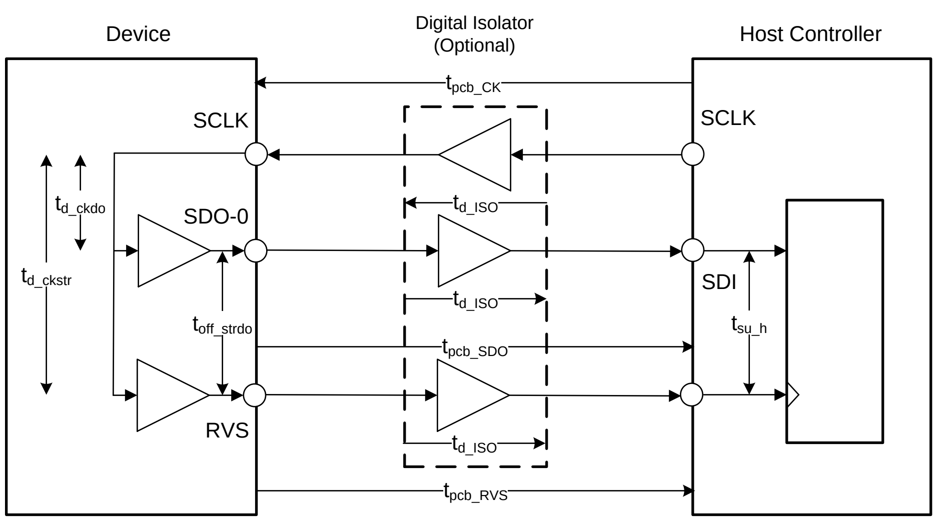


Figure 52. Delays in Source-Synchronous Communication

As illustrated in Figure 52, in ADC-master or source-synchronous mode, the device provides a synchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins).

For a source-synchronous data transfer, the total delay in the path is given by Equation 13:

$$t_{d\_total\_srcsync} = t_{pcb\_RVS} - t_{pcb\_SDO} + t_{su\_h} \quad (13)$$

As illustrated in Equation 11 and Equation 13, the ADC-master or source-synchronous mode completely eliminates the affect of isolator delays and the clock-to-data delays, which are typically the largest contributors in the overall delay computation.

Furthermore, the actual values of t_{pcb_RVS} and t_{pcb_SDO} do not matter. In most cases, the $t_{d\_total\_srcsync}$ delay can be kept at a minimum by routing the RVS and SDO lines together on the PCB. Therefore, the ADC-master or source-synchronous mode allows the host controller and device to operate at much higher SCLK speeds.

7.5.3.1 Protocols for Configuring the Device

As shown in Table 4, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to write data in to the device.

Table 4. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CNTL	SDO_CNTL	DIAGRAM
SPI-00-S	Low	Rising	00h	00h	Figure 53
SPI-01-S	Low	Falling	01h	00h	Figure 54
SPI-10-S	High	Falling	02h	00h	Figure 55
SPI-11-S	High	Rising	03h	00h	Figure 56

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations.

To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.

Figure 53, Figure 54, Figure 55, and Figure 56 detail the four protocols using an optimal, 20-SCLK frame; see the *Timing Requirements: SPI-Compatible Serial Interface* section for associated timing parameters.

NOTE

As explained in the *Data Transfer Frame* section, a valid write operation to the device requires a minimum of 20 SCLKs to be provided within a data transfer frame.

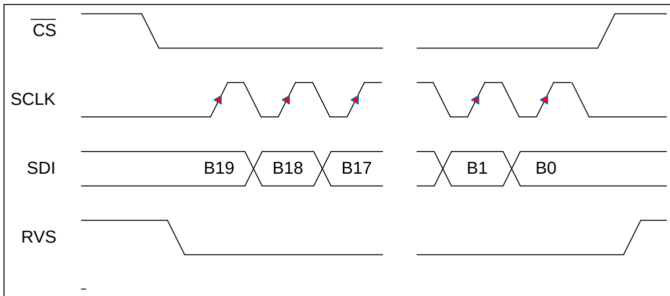


Figure 53. SPI-00-S Protocol, 20 SCLKs

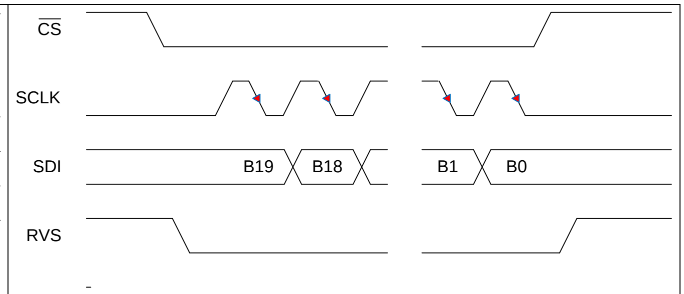


Figure 54. SPI-01-S Protocol, 20 SCLKs

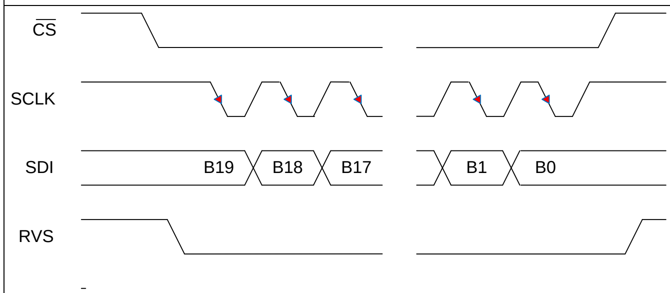


Figure 55. SPI-10-S Protocol, 20 SCLKs

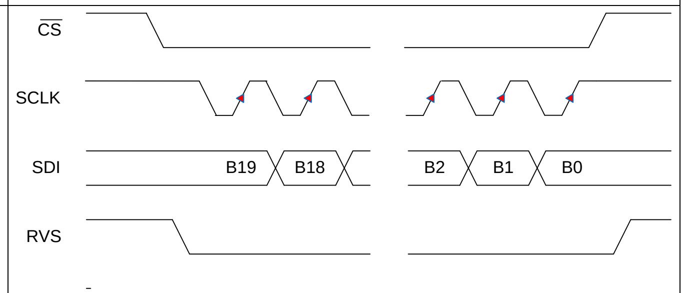


Figure 56. SPI-11-S Protocol, 20 SCLKs

7.5.3.2 Protocols for Reading From the Device

The protocols for the data read operation can be broadly classified into three categories:

1. Legacy, SPI-compatible (SPI-xy-S) protocols,
2. SPI-compatible protocols with bus width options (SPI-xy-D and SPI-xy-Q), and
3. Source-synchronous (SRC) protocols

7.5.3.2.1 Legacy, SPI-Compatible (SYS-xy-S) Protocols

As shown in Table 5, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to read data from the device.

Table 5. SPI Protocols for Reading From the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	DIAGRAM
SPI-00-S	Low	Rising	$\overline{CS}$ falling	00h	00h	Figure 57
SPI-01-S	Low	Falling	1st SCLK rising	01h	00h	Figure 58
SPI-10-S	High	Falling	$\overline{CS}$ falling	02h	00h	Figure 59
SPI-11-S	High	Rising	1st SCLK falling	03h	00h	Figure 60

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CNTL register.

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the *Timing Requirements: SPI-Compatible Serial Interface* table for associated timing parameters.

Figure 57, Figure 58, Figure 59, and Figure 60 explain the details of the four protocols using an optimal, 20-SCLK frame. As explained in the *Data Transfer Frame* section, the host controller can use a *short* data transfer frame to read only the required number of MSB bits from the 20-bit output data word.

With SDO_CNTL[7:0] = 00h, if the host controller uses a long data transfer frame, the device exhibits daisy-chain operation (see the *Multiple Devices: Daisy-Chain Topology* section).

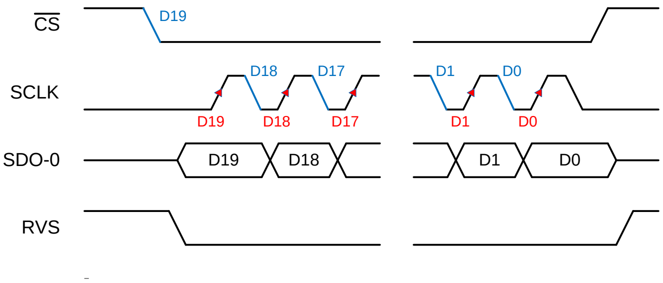


Figure 57. SPI-00-S Protocol, 20 SCLKs

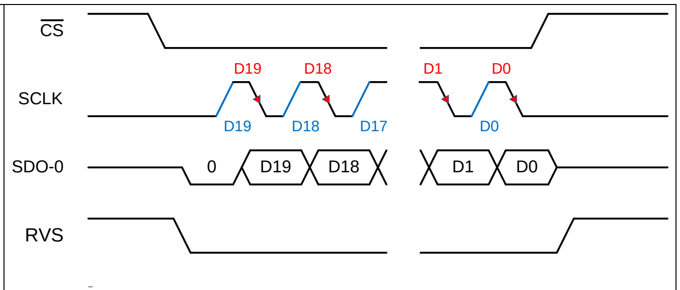


Figure 58. SPI-01-S Protocol, 20 SCLKs

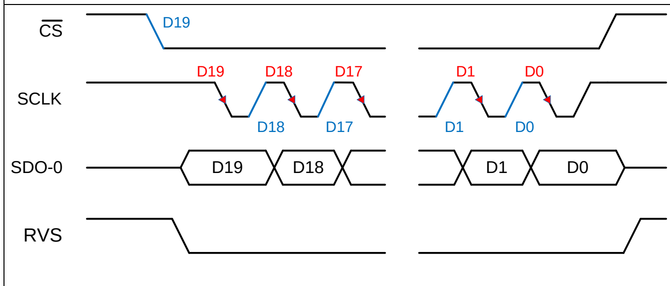


Figure 59. SPI-10-S Protocol, 20 SCLKs

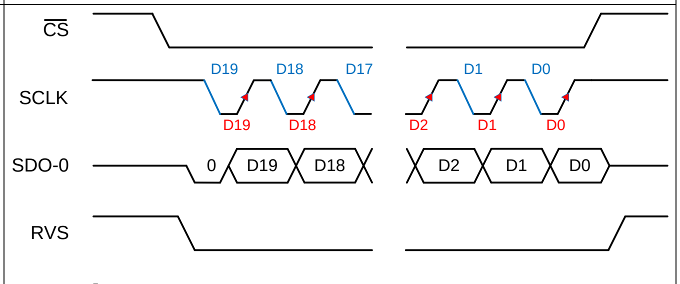


Figure 60. SPI-11-S Protocol, 20 SCLKs

7.5.3.2.2 SPI-Compatible Protocols with Bus Width Options

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or to four bits (quad SDO) when operating with any of the four legacy, SPI-compatible protocols.

Set the SDO_WIDTH[1:0] bits in the SDO_CNTL register to select the SDO bus width.

In dual SDO mode (SDO_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK launch edge.

In quad SDO mode (SDO_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK launch edge.

The SCLK launch edge depends upon the SPI protocol selection (as shown in Table 6).

Table 6. SPI-Compatible Protocols with Bus Width Options

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	DIAGRAM
SPI-00-D	Low	Rising	$\overline{CS}$ falling	00h	08h	Figure 61
SPI-01-D	Low	Falling	First SCLK rising	01h	08h	Figure 62
SPI-10-D	High	Falling	$\overline{CS}$ falling	02h	08h	Figure 63
SPI-11-D	High	Rising	First SCLK falling	03h	08h	Figure 64
SPI-00-Q	Low	Rising	$\overline{CS}$ falling	00h	0Ch	Figure 65
SPI-01-Q	Low	Falling	First SCLK rising	01h	0Ch	Figure 66
SPI-10-Q	High	Falling	$\overline{CS}$ falling	02h	0Ch	Figure 67
SPI-11-Q	High	Rising	First SCLK falling	03h	0Ch	Figure 68

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame.

Figure 61 to Figure 68 illustrate how the wider data bus allows the host controller to read all 20 bits of the output data word using *short* data transfer frames; see the *Timing Requirements: SPI-Compatible Serial Interface* table for associated timing parameters.

NOTE

With SDO_CNTL[7:0] ≠ 00h, a long data transfer frame does not result in daisy-chain operation.

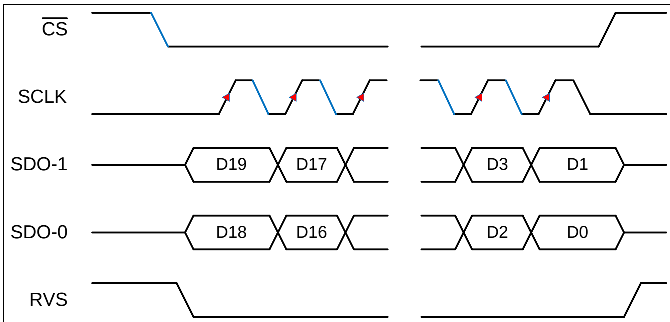


Figure 61. SPI-00-D Protocol

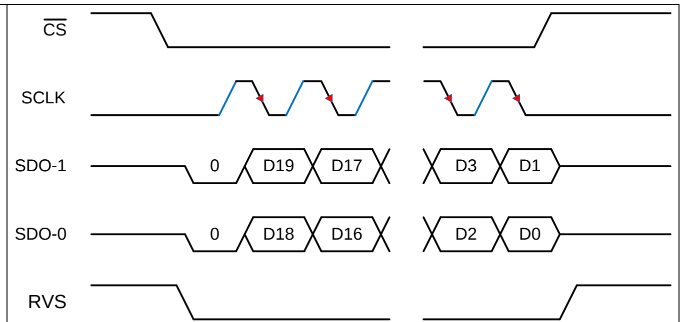


Figure 62. SPI-01-D Protocol

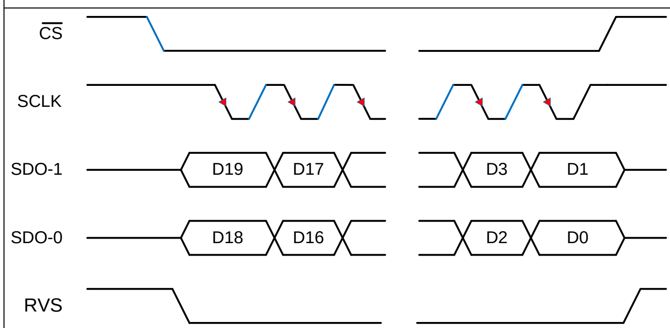


Figure 63. SPI-10-D Protocol

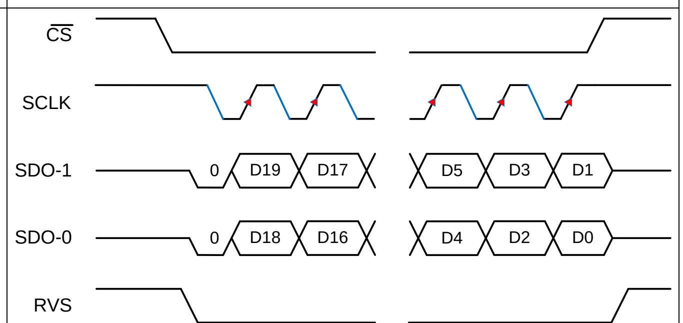


Figure 64. SPI-11-D Protocol

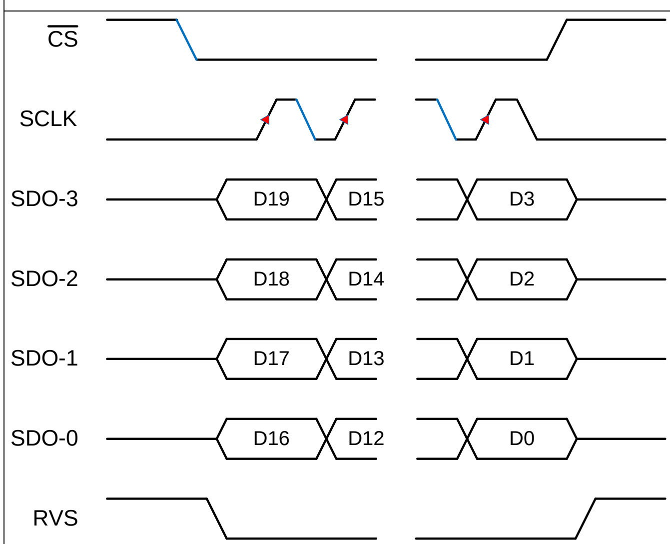


Figure 65. SPI-00-Q Protocol

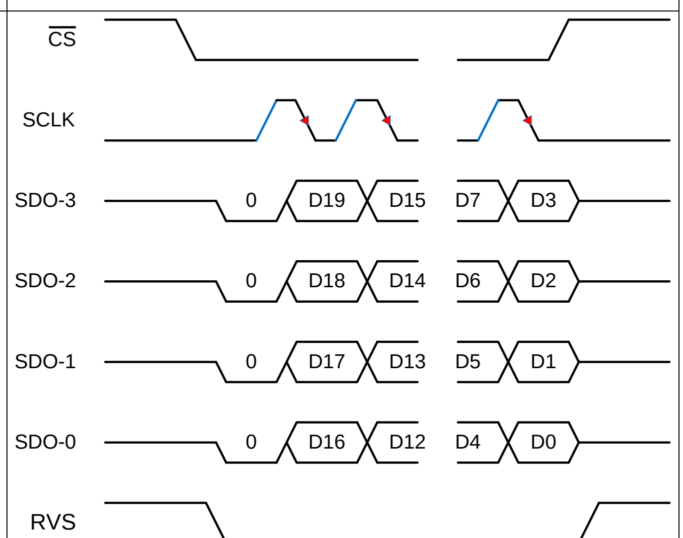


Figure 66. SPI-01-Q Protocol

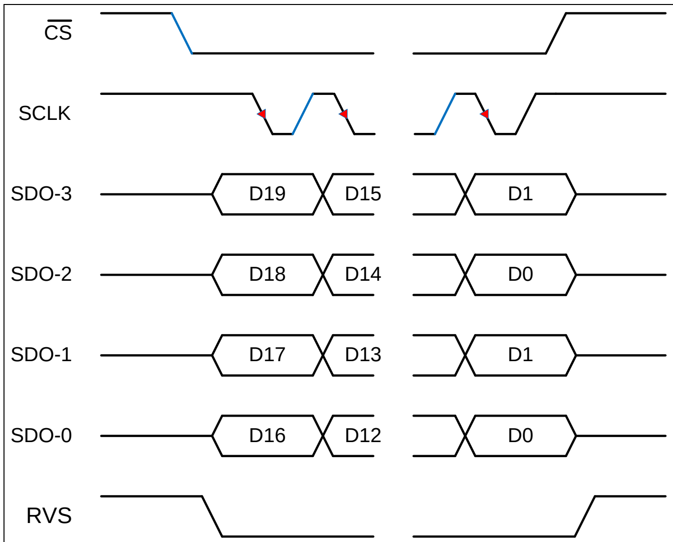


Figure 67. SPI-10-Q Protocol

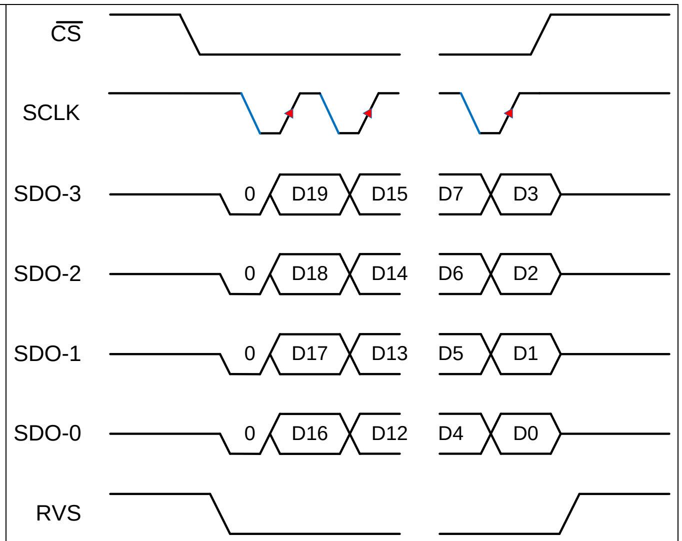


Figure 68. SPI-11-Q Protocol

7.5.3.2.3 Source-Synchronous (SRC) Protocols

As described in the *Data Transfer Protocols* section, the multiSPI interface supports an ADC-master or source-synchronous mode of data transfer between the device and host controller. In this mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the output clock source, data bus width, and data transfer rate.

7.5.3.2.3.1 Output Clock Source Options with SRC Protocols

In all SRC protocols, the RVS pin provides the output clock. The device allows this output clock to be synchronous to either the external clock provided on the SCLK pin or to the internal clock of the device. Furthermore, this internal clock can be divided by a factor of two or four to lower the data rates.

As shown in Figure 69, set the SSYNC_CLK_SEL[1:0] bits in the SDO_CNTL register to select the output clock source.

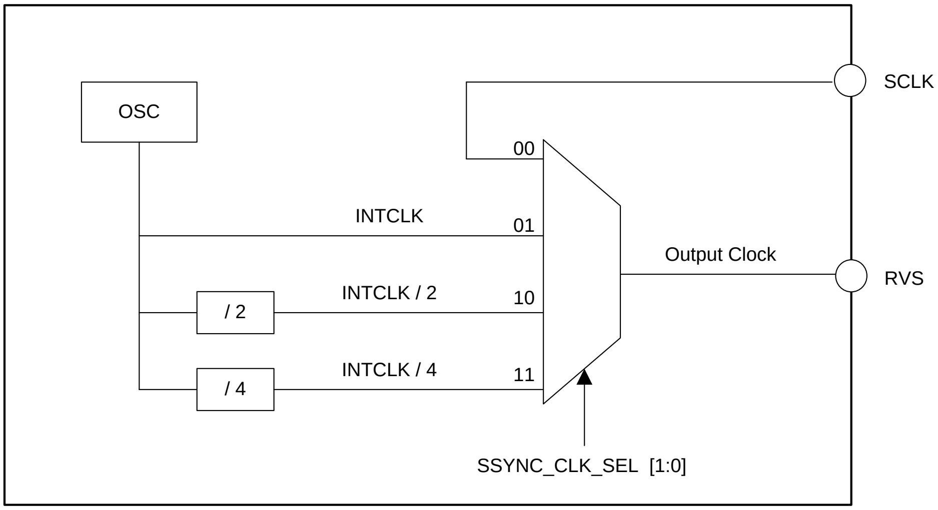


Figure 69. Output Clock Source options with SRC Protocols

7.5.3.2.3.2 Bus Width Options with SRC Protocols

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or to four bits (quad SDO) when operating with any of the SRC protocols. Set the SDO_WIDTH[1:0] bits in the SDO_CNTL register to select the SDO bus width.

In dual SDO mode (SDO_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK rising edge.

In quad SDO mode (SDO_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK rising edge.

7.5.3.2.3.3 Output Data Rate Options with SRC Protocols

The device provides an option to transfer the data to the host controller at single data rate (default, SDR) or at double data rate (DDR). Set the DATA_RATE bit in the SDO_CNTL register to select the data transfer rate.

In SDR mode (DATA_RATE = 0b), the RVS pin toggles from low to high and the output data bits are launched on the SDO pins on the output clock rising edge.

In DDR mode (DTA_RATE = 1b), the RVS pin toggles and the output data bits are launched on the SDO pins on every output clock edge, starting with the first rising edge.

The device supports all 24 combinations of output clock source, bus width, and output data rate, as shown in Table 7.

Table 7. SRC Protocol Combinations

<table>
<tr><th>PROTOCOL</th><th>OUTPUT CLOCK SOURCE</th><th>BUS WIDTH</th><th>OUTPUT DATA RATE</th><th>SDI_CNTL</th><th>SDO_CNTL</th><th>DIAGRAM</th></tr>
<tr><td>SRC-EXT-SS</td><td>SCLK</td><td>Single</td><td>SDR</td><td rowspan="24">00h, 01h, 02h, or 03h</td><td>03h</td><td>Figure 70</td></tr>
<tr><td>SRC-INT-SS</td><td>INTCLK</td><td>Single</td><td>SDR</td><td>43h</td><td rowspan="3">Figure 71</td></tr>
<tr><td>SRC-IB2-SS</td><td>INTCLK / 2</td><td>Single</td><td>SDR</td><td>83h</td></tr>
<tr><td>SRC-IB4-SS</td><td>INTCLK / 4</td><td>Single</td><td>SDR</td><td>C3h</td></tr>
<tr><td>SRC-EXT-DS</td><td>SCLK</td><td>Dual</td><td>SDR</td><td>0Bh</td><td>Figure 74</td></tr>
<tr><td>SRC-INT-DS</td><td>INTCLK</td><td>Dual</td><td>SDR</td><td>4Bh</td><td rowspan="3">Figure 75</td></tr>
<tr><td>SRC-IB2-DS</td><td>INTCLK / 2</td><td>Dual</td><td>SDR</td><td>8Bh</td></tr>
<tr><td>SRC-IB4-DS</td><td>INTCLK / 4</td><td>Dual</td><td>SDR</td><td>CBh</td></tr>
<tr><td>SRC-EXT-QS</td><td>SCLK</td><td>Quad</td><td>SDR</td><td>0Fh</td><td>Figure 78</td></tr>
<tr><td>SRC-INT-QS</td><td>INTCLK</td><td>Quad</td><td>SDR</td><td>4Fh</td><td rowspan="3">Figure 79</td></tr>
<tr><td>SRC-IB2-QS</td><td>INTCLK / 2</td><td>Quad</td><td>SDR</td><td>8Fh</td></tr>
<tr><td>SRC-IB4-QS</td><td>INTCLK / 4</td><td>Quad</td><td>SDR</td><td>CFh</td></tr>
<tr><td>SRC-EXT-SD</td><td>SCLK</td><td>Single</td><td>DDR</td><td>13h</td><td>Figure 72</td></tr>
<tr><td>SRC-INT-SD</td><td>INTCLK</td><td>Single</td><td>DDR</td><td>53h</td><td rowspan="3">Figure 73</td></tr>
<tr><td>SRC-IB2-SD</td><td>INTCLK / 2</td><td>Single</td><td>DDR</td><td>93h</td></tr>
<tr><td>SRC-IB4-SD</td><td>INTCLK / 4</td><td>Single</td><td>DDR</td><td>D3h</td></tr>
<tr><td>SRC-EXT-DD</td><td>SCLK</td><td>Dual</td><td>DDR</td><td>1Bh</td><td>Figure 76</td></tr>
<tr><td>SRC-INT-DD</td><td>INTCLK</td><td>Dual</td><td>DDR</td><td>5Bh</td><td rowspan="3">Figure 77</td></tr>
<tr><td>SRC-IB2-DD</td><td>INTCLK / 2</td><td>Dual</td><td>DDR</td><td>9Bh</td></tr>
<tr><td>SRC-IB4-DD</td><td>INTCLK / 4</td><td>Dual</td><td>DDR</td><td>DBh</td></tr>
<tr><td>SRC-EXT-QD</td><td>SCLK</td><td>Quad</td><td>DDR</td><td>1Fh</td><td>Figure 80</td></tr>
<tr><td>SRC-INT-QD</td><td>INTCLK</td><td>Quad</td><td>DDR</td><td>5Fh</td><td rowspan="3">Figure 81</td></tr>
<tr><td>SRC-IB2-QD</td><td>INTCLK / 2</td><td>Quad</td><td>DDR</td><td>9Fh</td></tr>
<tr><td>SRC-IB4-QD</td><td>INTCLK / 4</td><td>Quad</td><td>DDR</td><td>DFh</td></tr>
</table>

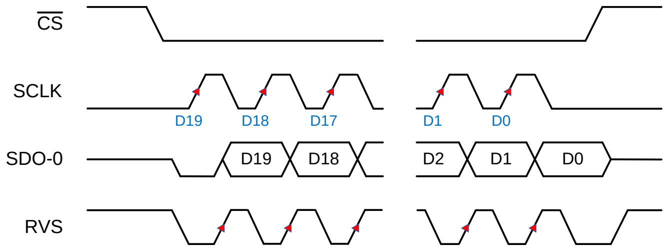


Figure 70. SRC-EXT-SS: SRC, SCLK, Single SDO, SDR

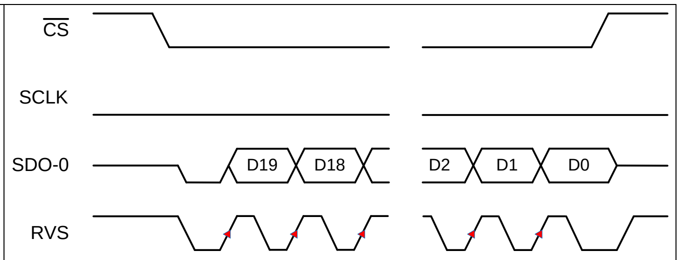


Figure 71. SRC-INT-SS: SRC, INTCLK, Single SDO, SDR

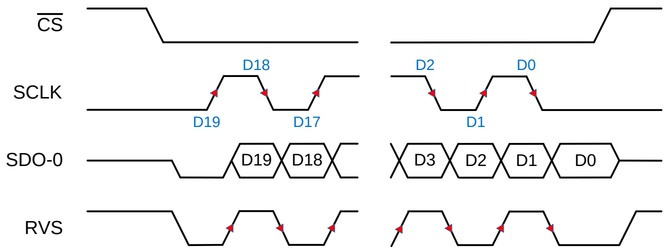


Figure 72. SRC-EXT-SD: SRC, SCLK, Single SDO, DDR

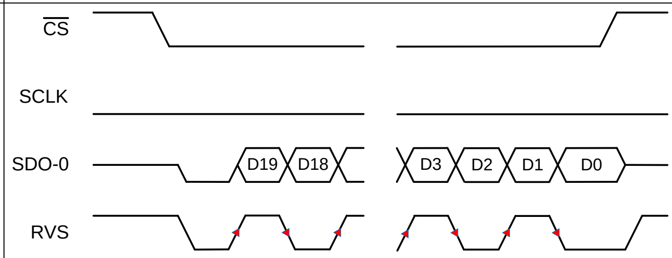


Figure 73. SRC-INT-SD: SRC, INTCLK, Single SDO, DDR

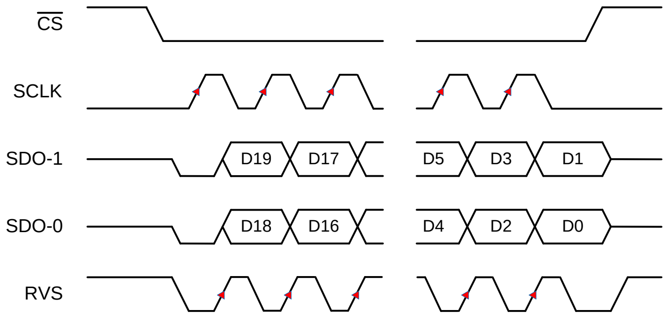


Figure 74. SRC-EXT-DS: SRC, SCLK, Dual SDO, SDR

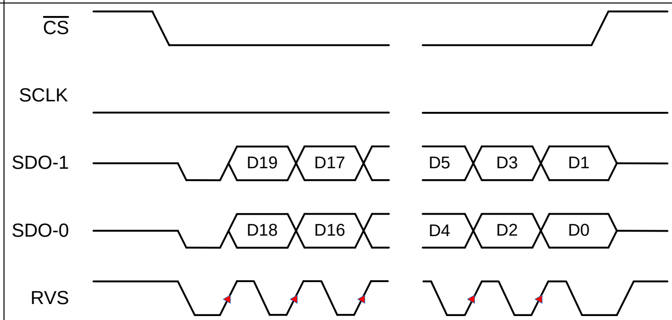


Figure 75. SRC-INT-DS: SRC, INTCLK, Dual SDO, SDR

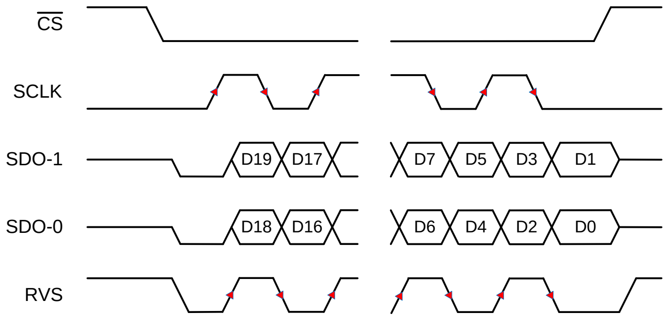


Figure 76. SRC-EXT-DD: SRC, SCLK, Dual SDO, DDR

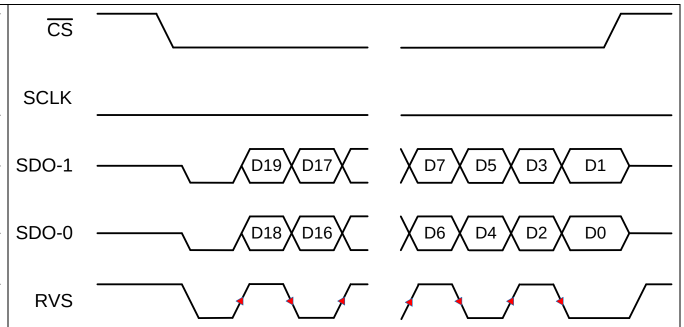


Figure 77. SRC-INT-DD: SRC, INTCLK, Dual SDO, DDR

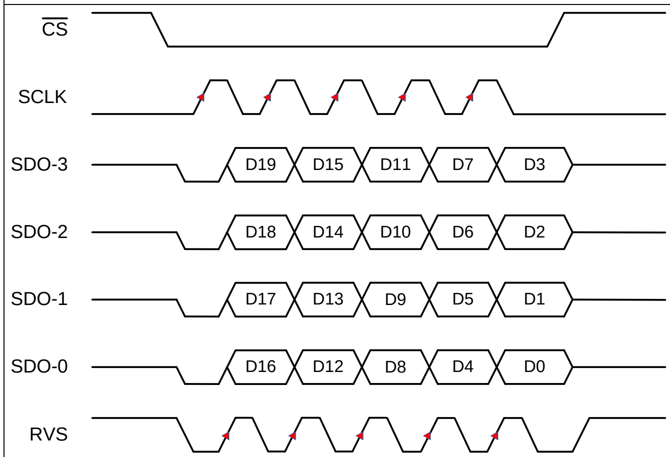


Figure 78. SRC-EXT-QS: SRC, SCLK, Quad SDO, SDR

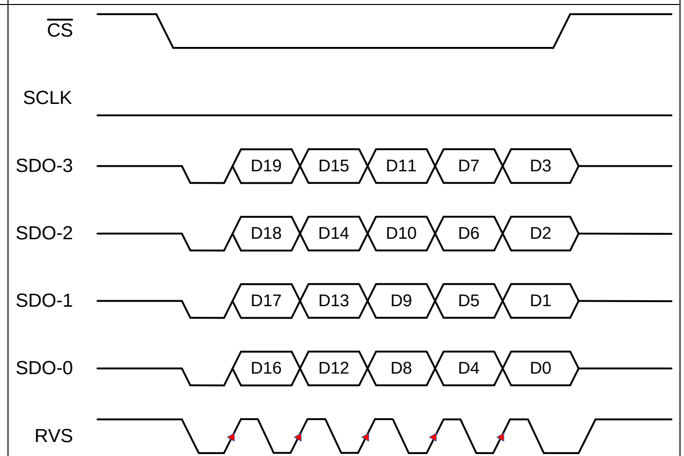


Figure 79. SRC-INT-QS: SRC, INTCLK, Quad SDO, SDR

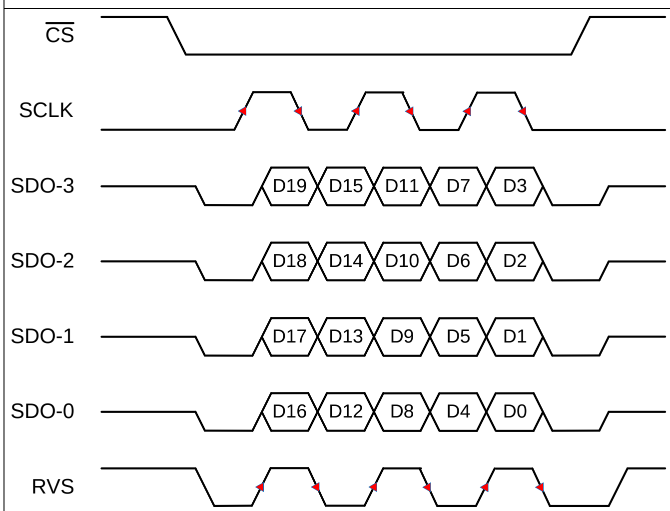


Figure 80. SRC-EXT-QD: SRC, SCLK, Quad SDO, DDR

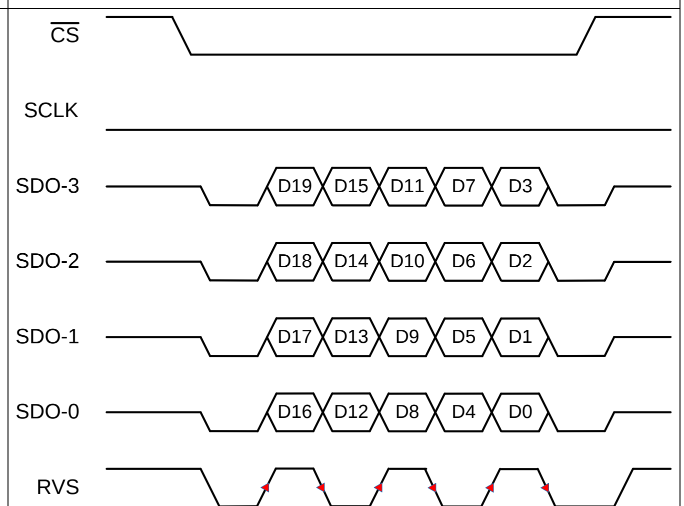


Figure 81. SRC-INT-QD: SRC, INTCLK, Quad SDO, DDR

7.5.4 Device Setup

The multiSPI interface and the device configuration registers offer multiple operation modes. This section describes how to select the hardware connection topology to meet different system requirements.

7.5.4.1 Single Device: All multiSPI Options

Figure 82 shows the connections between a host controller and a stand-alone device to exercise all options provided by the multiSPI interface.

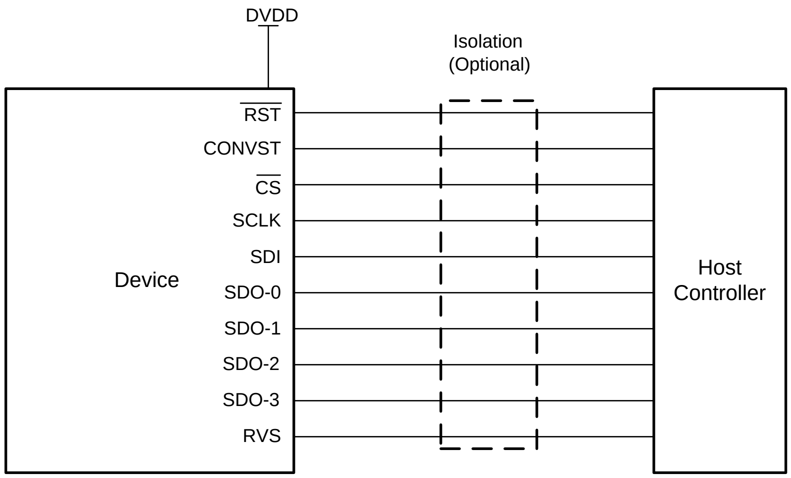


Figure 82. MultiSPI Interface, All Pins

7.5.4.2 Single Device: Minimum Pins for a Standard SPI Interface

Figure 83 shows the minimum-pin interface for applications using a standard SPI protocol.

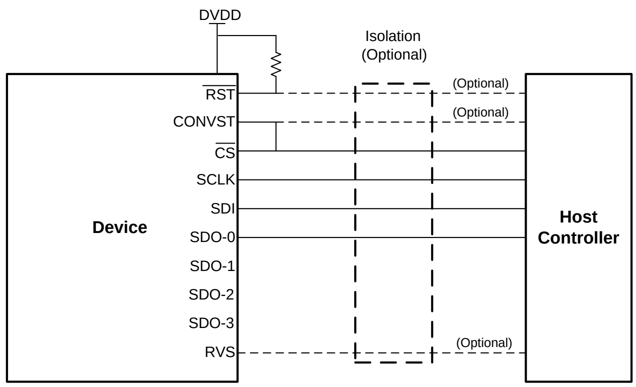


Figure 83. SPI Interface, Minimum Pins

The CS, SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. The CONVST pin can be tied to CS, or can be controlled independently for additional timing flexibility. The RST pin can be tied to DVDD. The RVS pin can be monitored for timing benefits. The SDO-1, SDO-2, and SDO-3 pins have no external connections.

7.5.4.3 *Multiple Devices: Daisy-Chain Topology*

A typical connection diagram showing multiple devices in a daisy-chain topology is shown in Figure 84.

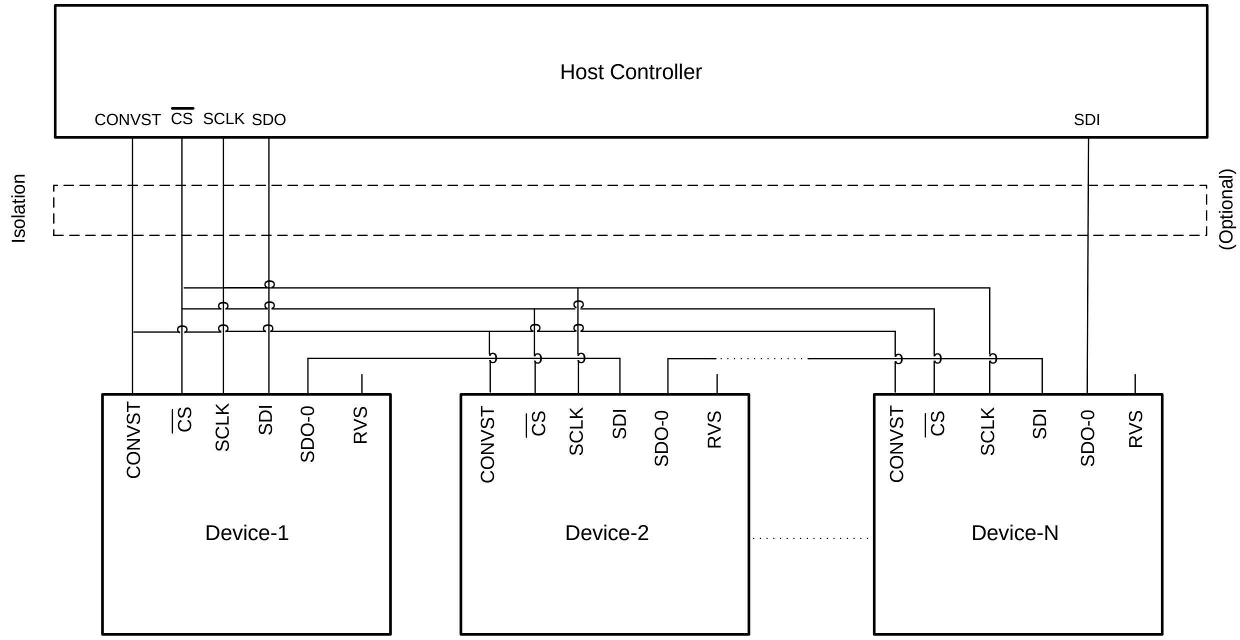


Figure 84. Daisy-Chain Connection Schematic

The CONVST, $\overline{CS}$, and SCLK inputs of all devices are connected together and controlled by a single CONVST, $\overline{CS}$, and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (Device-1) is connected to the SDO pin of the host controller, the SDO-0 output pin of Device-1 is connected to the SDI input pin of Device-2, and so forth. The SDO-0 output pin of the last device in the chain (Device-N) is connected to the SDI pin of the host controller.

To operate multiple devices in a daisy-chain topology, the host controller must program the configuration registers in each device with identical values and must operate with any of the legacy, SPI-compatible protocols for data read and data write operations (SDO_CNT[7:0] = 00h). With these configurations settings, the 20-bit OSR and 20-bit ISR registers collapse to form a single, 20-bit unified shift register (USR), as shown in Figure 85.

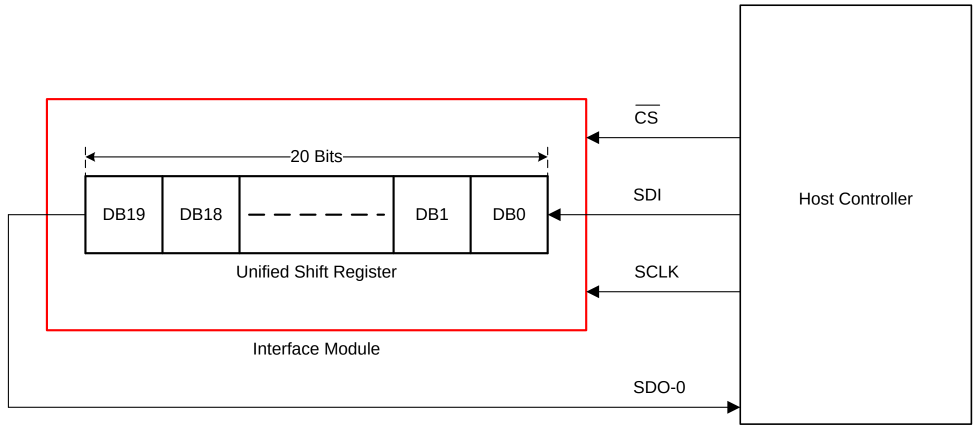


Figure 85. Unified Shift Register Schematic

All devices in the daisy-chain topology sample their analog input signals on the CONVST rising edge. The data transfer frame starts with a $\overline{CS}$ falling edge. On each SCLK launch edge, every device in the chain shifts out the MSB of its USR on to its SDO-0 pin. On every SCLK capture edge, each device in the chain shifts in data received on its SDI pin as the LSB bit of its USR. Therefore, in a daisy-chain configuration, the host controller receives the data of Device-N, followed by the data of Device-N-1, and so forth (in MSB-first fashion). On the $\overline{CS}$ rising edge, each device decodes the contents in its USR and takes appropriate action.

A typical timing diagram for three devices connected in daisy-chain topology and using the SPI-00-S protocol is shown in Figure 86.

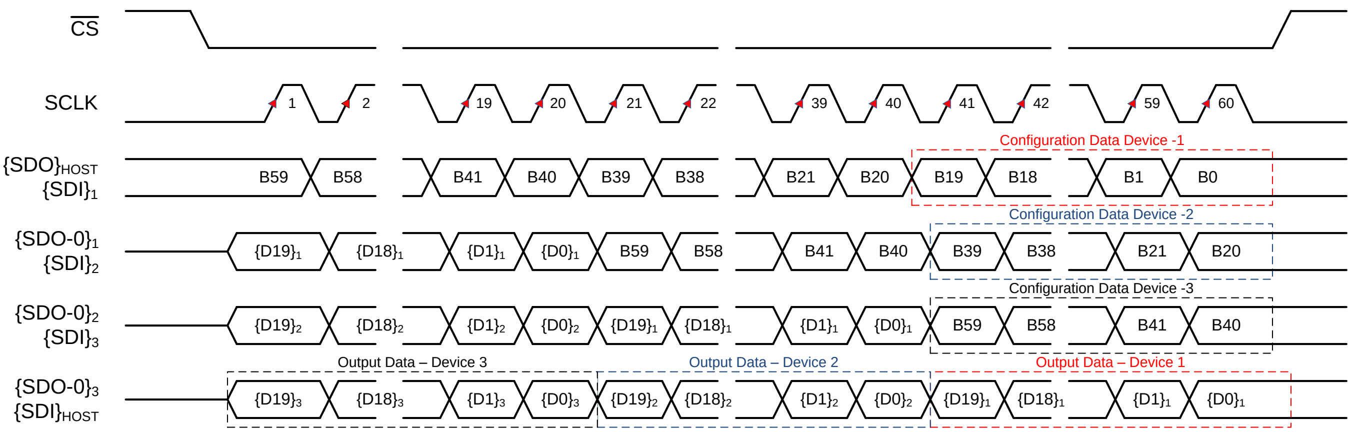


Figure 86. Three Devices in Daisy-Chain Mode Timing Diagram

For N devices connected in daisy-chain topology, an optimal data transfer frame must contain 20 × N SCLK capture edges. For a longer data transfer frame, the host controller must appropriately align the configuration data for each device before bringing $\overline{CS}$ high. A shorter data transfer frame can result in an erroneous device configuration, and *must be avoided*.

Note that the overall throughput of the system is proportionally reduced with the number of devices connected in a daisy-chain topology.

7.5.4.4 Multiple Devices: Star Topology

A typical connection diagram showing multiple devices in the star topology is shown in Figure 87. The CONVST, SDI, and SCLK inputs of all devices are connected together and are controlled by a single CONVST, SDO, and SCLK pin of the host controller, respectively. Similarly, the SDO output pin of all devices are tied together and connected to the a single SDI input pin of the host controller. The $\overline{CS}$ input pin of each device is individually controlled by separate $\overline{CS}$ control lines from the host controller.

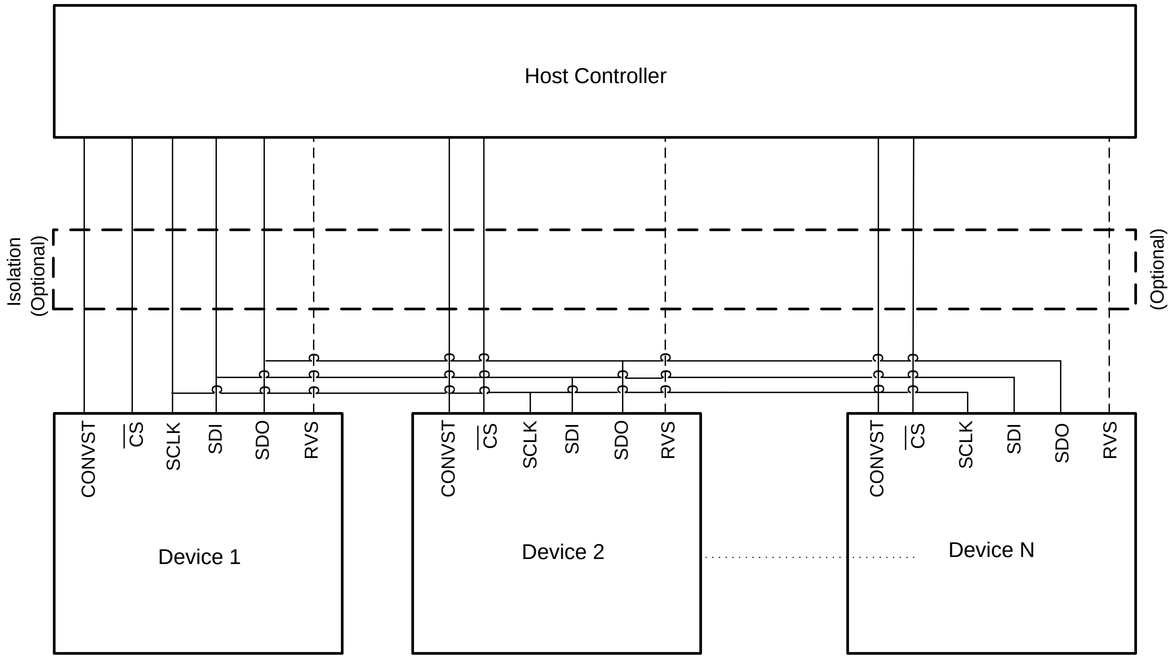


Figure 87. Star Topology Connection Schematic

The timing diagram for N devices connected in the star topology is shown in Figure 88. In order to avoid any conflict related to multiple devices driving the SDO line at the same time, ensure that the host controller pulls down the $\overline{CS}$ signal for only one device at any particular time.

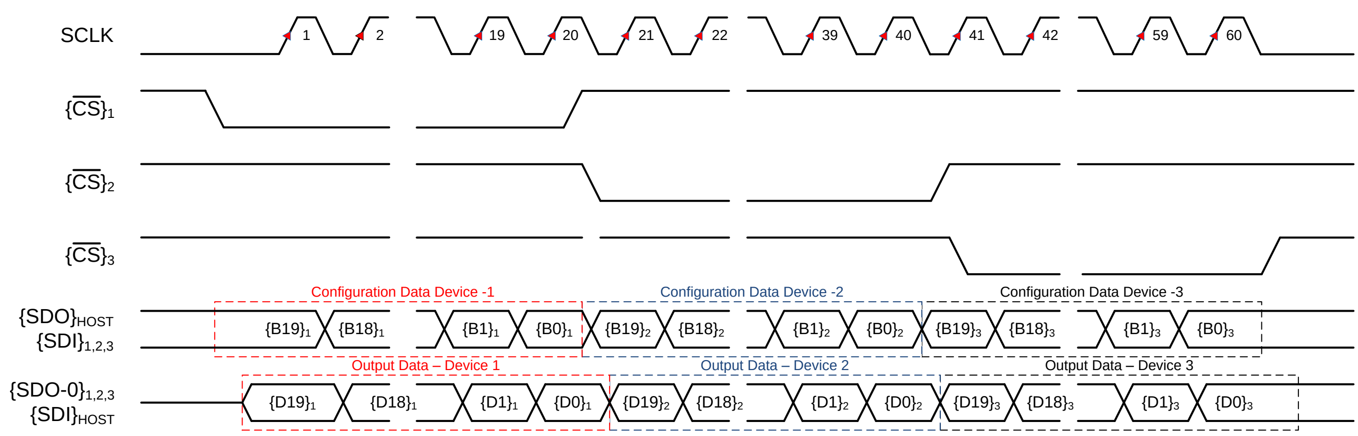


Figure 88. Three Devices Connected in Star Connection Timing Diagram

7.6 Register Maps

7.6.1 Device Configuration and Register Maps

The device features four configuration registers, mapped as described in Table 8.

Table 8. Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER FUNCTION	SECTION
010h	PD_CNTL	Low-power modes control register	PD Control
014h	SDI_CNTL	SDI input protocol selection register	SDI Control
018h	SDO_CNTL	SDO output protocol selection register	SDO Control
01Ch	DATA_CNTL	Output data word configuration register	DATA Control

7.6.1.1 PD_CNTL Register (address = 010h)

This register controls the low-power modes offered by the device and is protected using a key.

Any writes to the PD_CNTL register must be preceded by a write operation with the register address set to 011h and the register data set to 69h.

Figure 89. PD_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	NAP_EN	PDWN
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. PD_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R	000000b	Reserved bits. Reads return 000000b.
1	NAP_EN	R/W	0b	This bit enables NAP mode for the device. 0b = NAP mode is disabled 1b = NAP mode is enabled
0	PDWN	R/W	0b	This bit outputs the device in power-down mode. 0b = Device is powered up 1b = Device is powered down

7.6.1.2 SDI_CNTL Register (address = 014h)

This register configures the protocol used for writing data into the device.

Figure 90. SDI_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SDI_MODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. SDI_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R	000000b	Reserved bits. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for writing data into the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

7.6.1.3 SDO_CNTL Register (address = 018h)

This register configures the protocol for reading data from the device.

Figure 91. SDO_CNTL Register

7	6	5	4	3	2	1	0
SSYNC_CLK_SEL[1:0]		0	DATA_RATE	SDO_WIDTH[1:0]		SDO_MODE[1:0]	
R/W-00b		R-0b	R/W-0b	R/W-00b		R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. SDO_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SSYNC_CLK_SEL[1:0]	R/W	00b	These bits select the source and frequency of the clock for the source-synchronous data transmission and are valid only if SDO_MODE[1:0] = 11b. 00b = External SCLK echo 01b = Internal clock (INTCLK) 10b = Internal clock / 2 (INTCLK / 2) 11b = Internal clock / 4 (INTCLK / 4)
5	0	R	0b	This bit must be always set to 0.
4	DATA_RATE	R/W	0b	This bit is ignored if SDO_MODE[1:0] = 00b. When SDO_MODE[1:0] = 11b: 0b = SDOs are updated at single data rate (SDR) with respect to the output clock 1b = SDOs are updated at double data rate (DDR) with respect to the output clock
3-2	SDO_WIDTH[1:0]	R/W	00b	These bits set the width of the output bus. 0xb = Data are output only on SDO-0 10b = Data are output only on SDO-0 and SDO-1 11b = Data are output on SDO-0, SDO-1, SDO-2, and SDO-3
1-0	SDO_MODE[1:0]	R/W	00b	These bits select the protocol for reading data from the device. 00b = SDO follows the same SPI protocol as SDI; see the SDI_CNTL register 01b = Invalid configuration, not supported by the device 10b = Invalid configuration, not supported by the device 11b = SDO follows the source-synchronous protocol

7.6.1.4 DATA_CNTL Register (address = 01Ch)

This register configures the contents of the 20-bit output data word (D[19:0]).

Figure 92. DATA_CNTL Register

7	6	5	4	3	2	1	0
0	0	FPAR_LOC 0		PAR_EN	DATA_PATN[2:0]		
R-0b	R-0b	R/W-00b		R/W-0b	R/W-000b		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. DATA_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R	00b	Reserved bits. Reads return 00b.
5-4	FPAR_LOC[1:0]	R/W	00b	These bits control the data span for calculating the FTPAR bit (bit D[0] in the output data word). 00b = D[0] reflects even parity calculated for 4 MSB bits 01b = D[0] reflects even parity calculated for 8 MSB bits 10b = D[0] reflects even parity calculated for 12 MSB bits 11b = D[0] reflects even parity calculated for 16 MSB bits
3	PAR_EN	R/W	0b	0b = Output data does not contain any parity information D[1] = 0 D[0] = 0 1b = Parity information is appended to the LSB of the output data D[1] = Even parity calculated on bits D[19:2] D[0] = Even parity computed on the selected number of MSB bits of D[19:2] as per the FPAR_LOC[1:0] setting See Figure 46 for further details of parity computation.
2-0	DATA_PATN[2:0]	R/W	000b	These bits control bits D[19:2] of the output data word. 0xxb = 18-bit conversion output 100b = All 0s 101b = All 1s 110b = Alternating 0s and 1s (that is, 15555h) 111b = Alternating 00s and 11s (that is, 03333h) See Figure 47 for more details.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by an application circuit designed using the ADS9110.

8.1.1 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input signal and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of the ADS9110.

8.1.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (see the *Antialiasing Filter* section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier with Unity Gain Bandwidth (UGB) as described in Equation 14:

$$UGB \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (14)$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in Equation 15.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20} \right)}$$

  where:
  - V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µV,
  - e_{n_RMS} is the amplifier broadband noise density in nV/√Hz,
  - f_{-3dB} is the 3-dB bandwidth of the RC filter, and
  - N_G is the noise gain of the front-end circuit that is equal to 1 in a buffer configuration. (15)

- *Distortion.* Both the ADC and the input driver introduce distortion in a data acquisition block. To ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in Equation 16.

$$THD_{AMP} \leq THD_{ADC} - 10\ (dB) \quad (16)$$

Application Information (continued)

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA™-SPICE simulations before selecting the amplifier.

8.1.3 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher-frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, where the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the inputs of the ADC during the small acquisition time window. For ac signals, keep the filter bandwidth low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as shown in Figure 93). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15 times the specified value of the ADC sampling capacitance. For the ADS9110, the input sampling capacitance is equal to 60 pF, thus it is recommeded to keep C_{FLT} greater than 900 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}}$$

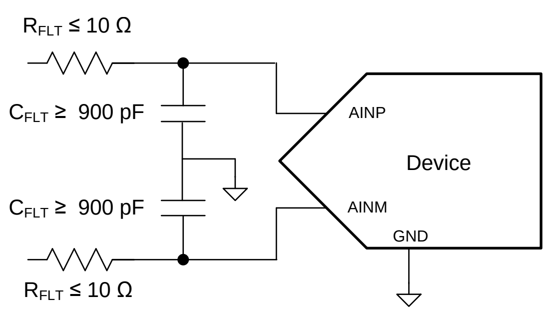


Figure 93. Antialiasing Filter Configuration

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS9110, limiting the value of R_{FLT} to a maximum of 10-Ω is recommended in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced.

The driver amplifier must be selected such that its closed-loop output impedance is at least 5X lesser than the R_{FLT}.

Application Information (continued)

8.1.4 ADC Reference Driver

The external reference source to the ADS9110 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few hundred μV_{RMS}. Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of V_{REF} stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor, CBUF_FLT (see Figure 39), between each pair of REFP and REFM pins for regulating the voltage at the reference input of the ADC. The effective capacitance of any large capacitor reduces with the applied voltage based on the voltage rating and type. Using X7R-type capacitors is strongly recommended.

The amplifier selected as the reference driver must have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pins without any stability issues.

8.2 Typical Application

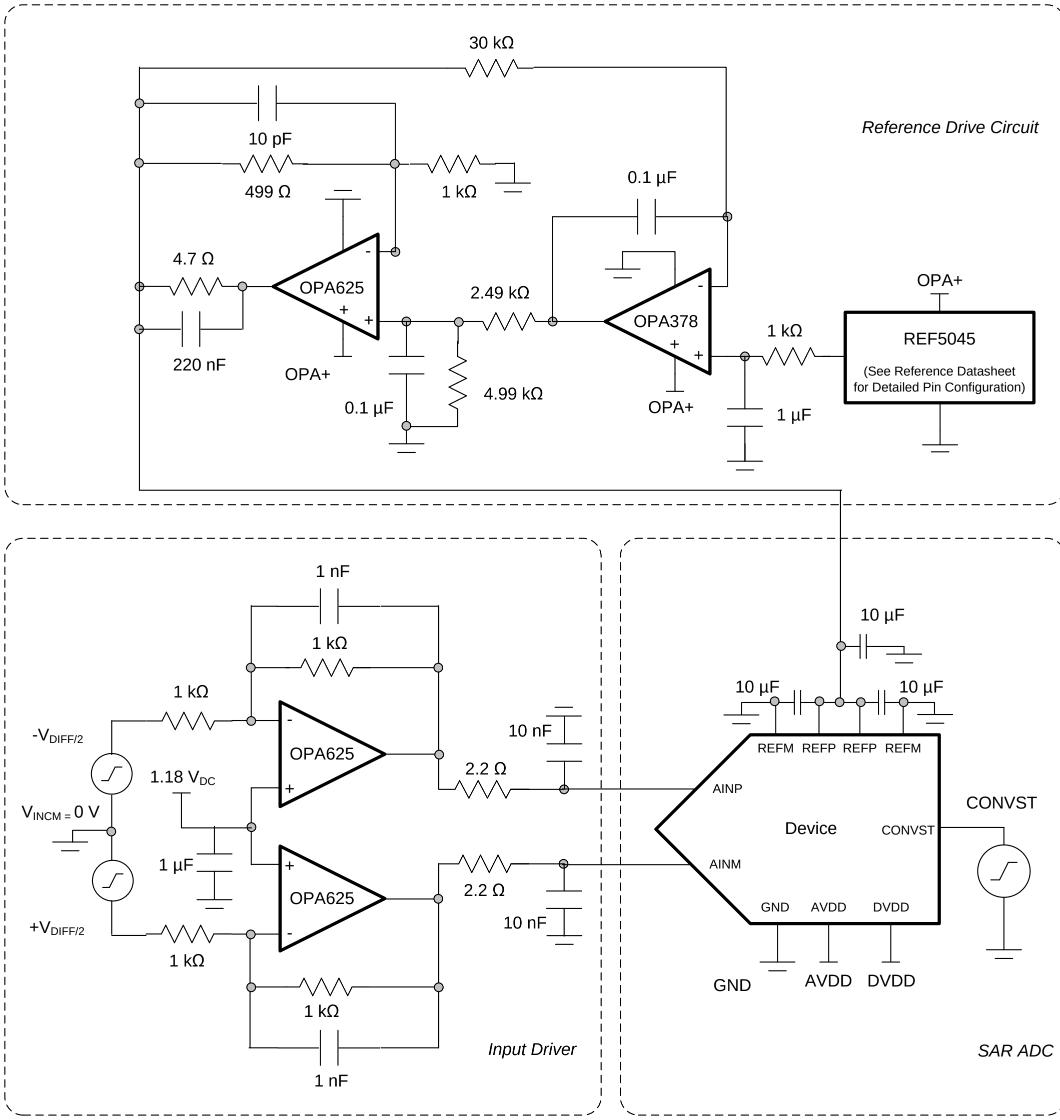


Figure 94. Differential Input DAQ Circuit for Lowest Distortion and Noise at 2 MSPS

8.2.1 Design Requirements

Design an application circuit optimized for using the ADS9110 to achieve:

- > 98.5-dB SNR, < –118-dB THD,
- ±1-LSB linearity, and
- Maximum-specified throughput of 2 MSPS

Typical Application (continued)

8.2.2 Detailed Design Procedure

The application circuits are illustrated in Figure 94. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the *Power-Supply Recommendations* section for suggested guidelines.

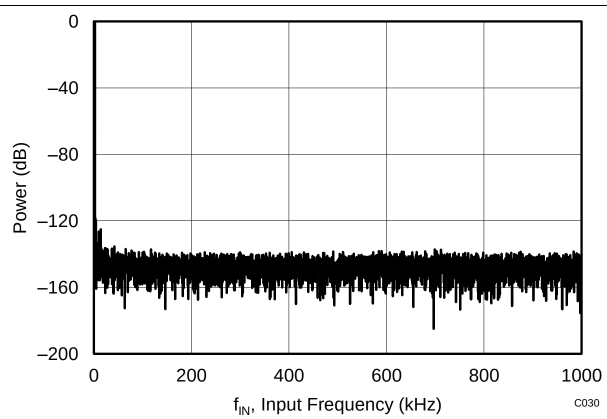
The input signal is processed through the OPA625 (a high-bandwidth, low-distortion, high-precision amplifier in an inverting gain configuration) and a low-pass RC filter before being fed into the ADC. Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the OPA625 in an inverting gain configuration. The low-power OPA625 as an input driver provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. To exercise the complete dynamic range of the ADS9110, the common-mode voltage at the ADS9110 inputs is established at a value of 2.25 V (4.5 V / 2) by using the noninverting pins of the OPA625 amplifiers.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

The reference driver circuit, illustrated in Figure 94, generates a voltage of 4.5 V_{DC} using a single 5-V supply. This circuit is suitable to drive the reference of the ADS9110 at higher sampling rates up to 2 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

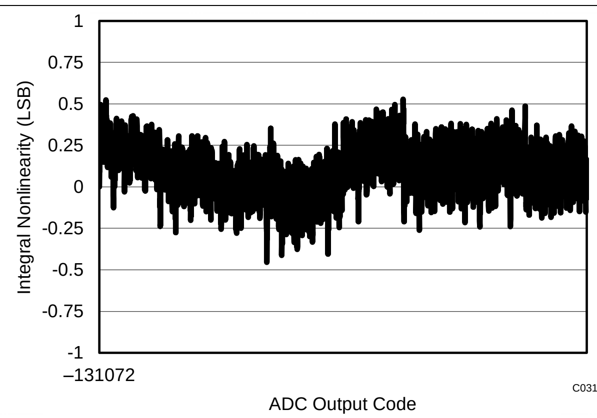
The reference buffer is designed with the OPA625 and OPA378 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The OPA625 is a high-bandwidth amplifier with a very low open-loop output impedance of 1 Ω up to a frequency of 1 MHz. The low open-loop output impedance makes the OPA625 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The relatively higher offset and drift specifications of the OPA625 are corrected by using a dc-correcting amplifier (the OPA378) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA378.

8.2.3 Application Curves



f_{IN} = 2 kHz, SNR = 99 dB, THD = –120 dB

Figure 95. FFT with a 2-kHz Input Signal



Typical INL of ±0.5 LSB

Figure 96. Typical INL

9 Power-Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

9.1 Power-Supply Decoupling

The AVDD and DVDD supply pins cannot share the same decoupling capacitor. As shown in Figure 97, separate 1-µF ceramic capacitors are recommended. These capacitors avoid digital and analog supply crosstalk resulting from dynamic currents during conversion and data transfer.

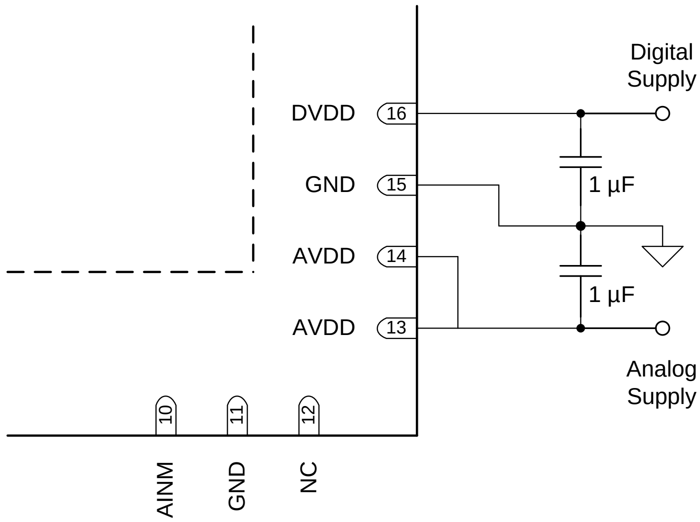


Figure 97. Supply Decoupling

9.2 Power Saving

In normal mode of operation, the device does not power down between conversions, and therefore achieves a high throughput of 2 MSPS. However, the device offers two programmable low-power modes (NAP and PD) to reduce power consumption when the device is operated at lower throughput rates. Figure 98 shows comparative power consumption between the different modes of the device.

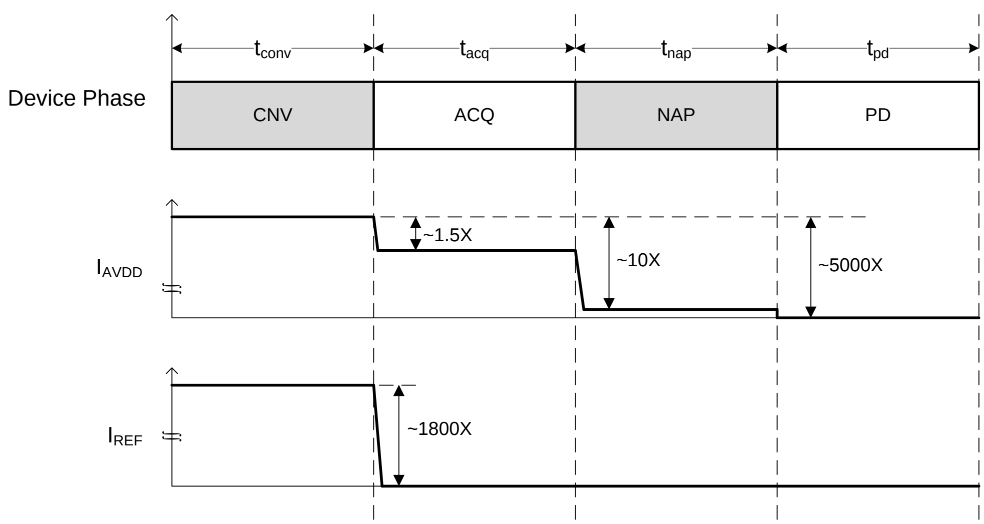


Figure 98. Power Consumption in Different Operating Modes

Power Saving (continued)

9.2.1 NAP Mode

In NAP mode, some of the internal blocks of the device power down to reduce power consumption in the ACQ state.

To enable NAP mode, set the NAP_EN bit in the PD_CNTL register. To exercise NAP mode, keep the CONVST pin high at the end of conversion process. The device then enters NAP mode at the end of conversion and continues in NAP mode until the CONVST pin is held high.

A CONVST falling edge brings the device out of NAP mode; however, the host controller can initiate a new conversion (CONVST rising edge) only after the t_{nap_wkup} time has elapsed.

Figure 99 shows a typical conversion cycle with NAP mode enabled (NAP_EN = 1b).

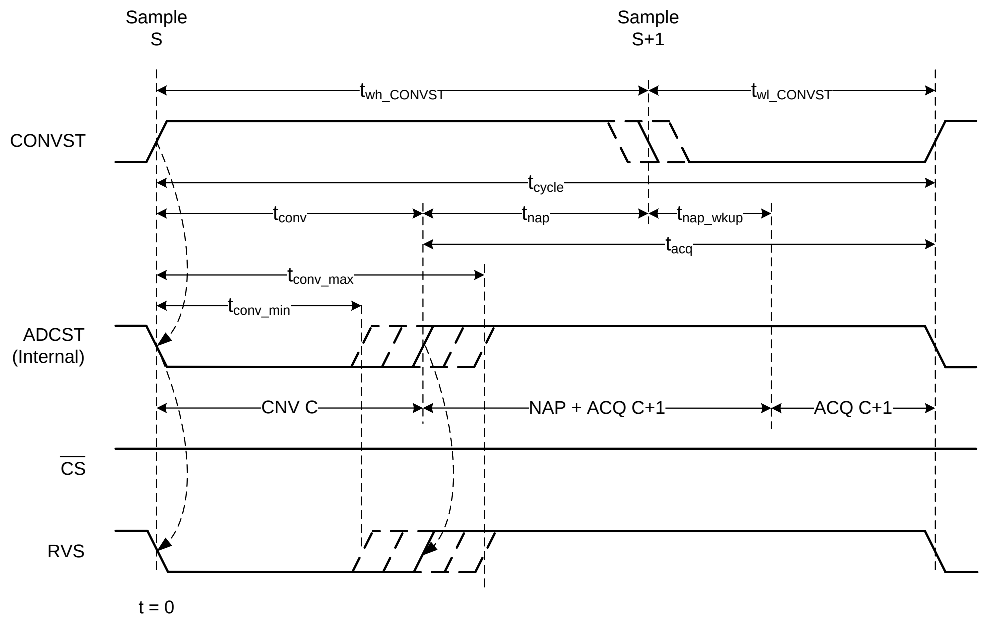


Figure 99. NAP Enabled Conversion Cycle

The cycle time is given by Equation 17.

$$t_{cycle} = t_{conv} + t_{nap} + t_{nap\_wkup} \quad (17)$$

At lower throughputs, cycle time (t_{cycle}) increases but the conversion time (t_{conv}) remains constant, and therefore the device spends more time in NAP mode, thus giving power scaling with throughput as shown in Figure 100.

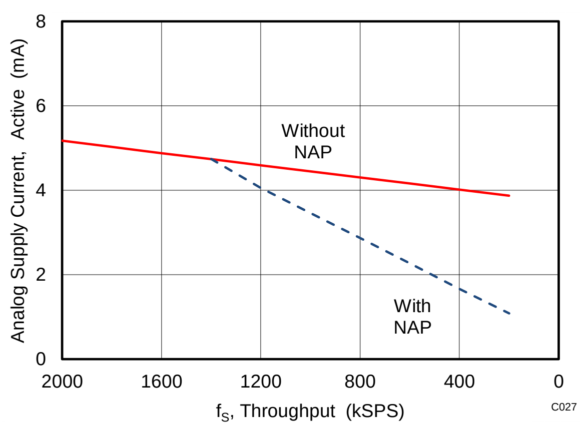


Figure 100. Power Scaling with Throughput with NAP Mode

Power Saving (continued)

9.2.2 PD Mode

The device also features a deep power-down mode (PD) to reduce the power consumption at very low throughput rates.

To enter PD mode:

1. Write 069h to address 011h to unlock the PD_CNTL register.
2. Set the PDWN bit in the PD_CNTL register. The device enters PD mode on the $\overline{CS}$ rising edge.

In PD mode, all analog blocks within the device are powered down; however, the interface remains active and the register contents are also retained. The RVS pin is high, indicating that the device is ready to receive the next command.

To exit PD mode:

1. Reset the PDWN bit in the PD_CNTL register.
2. The RVS pin goes high, indicating that the device has started coming out of PD mode. However, the host controller must wait for the t_{PWRUP} time to elapse before initiating a new conversion.

10 Layout

10.1 Layout Guidelines

This section provides some recommended layout guidelines for achieving optimum performance with the ADS9110 device.

10.1.1 Signal Path

As illustrated in Figure 101, the analog input and reference signals are routed in opposite directions to the digital connections. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Grounding inductance is kept below 1 nH with 15-mil grounding vias and a printed circuit board (PCB) layout design that has at least four layers. Place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize via length to ground.

Pins 11 and 15 of the ADS9110 can be easily grounded with very low inductance by placing at least four 8-mil grounding vias at the ADS9110 thermal pad. Afterwards, pins 11 and 15 can be connected directly to the grounded thermal path.

10.1.3 Decoupling of Power Supplies

Place the AVDD and DVDD supply decoupling capacitors within 20 mil from the supply pins and use a 15-mil via to ground from each capacitor. Avoid placing vias between any supply pin and its decoupling capacitor.

10.1.4 Reference Decoupling

Dynamic currents are also present at the REFP and REFM pins during the conversion phase and excellent decoupling is required to achieve optimum performance. Three 10-µF, X7R-grade, ceramic capacitors with 10-V rating are recommended, placed as illustrated in Figure 101. Select 0603- or 0805-size capacitors to keep ESL low. The REFM pin of each pair must be connected to the decoupling capacitor before a ground via.

10.1.5 Differential Input Decoupling

Dynamic currents are also present at the differential analog inputs of the ADS9110. C0G- or NPO-type capacitors are required to decouple these inputs because their capacitance stays almost constant over the full input voltage range. Lower quality capacitors (such as X5R and X7R) have large capacitance changes over the full input voltage range that can cause degradation in the performance of the ADS9110.

10.2 Layout Example

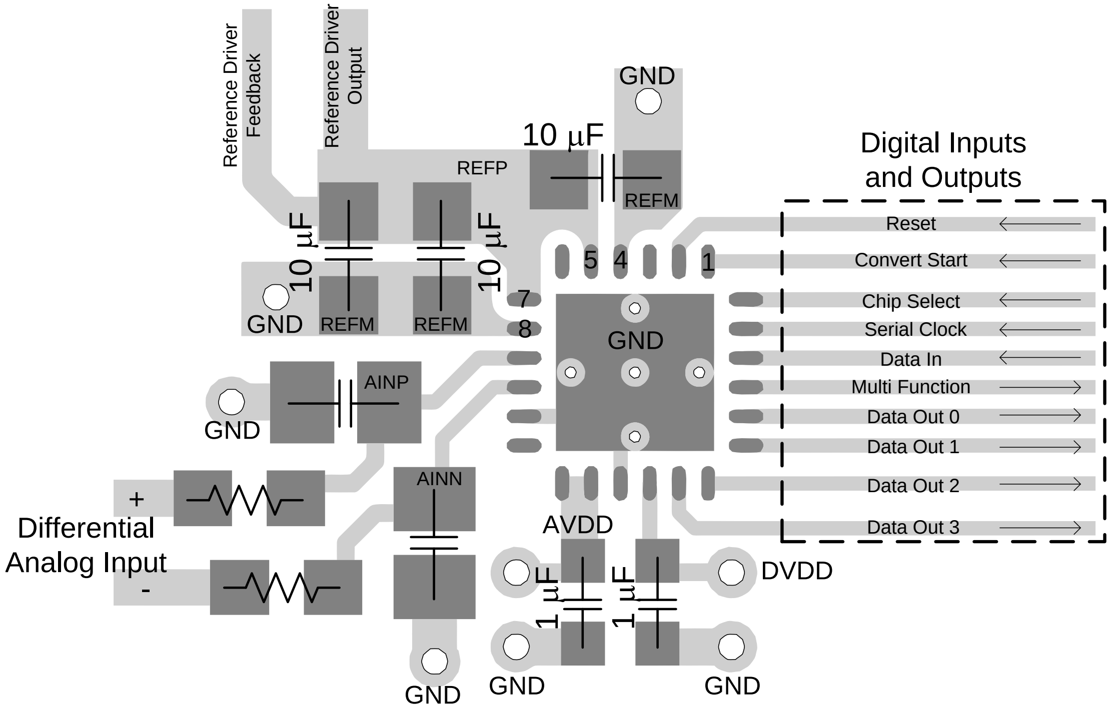


Figure 101. Recommended Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

《OPA378 数据表》，SBOS417

《OPA625 数据表》，SBOS688

《REF5045 数据表》（文献编号 SBOS410）

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS9110IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS9110	Samples
ADS9110IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS9110	Samples

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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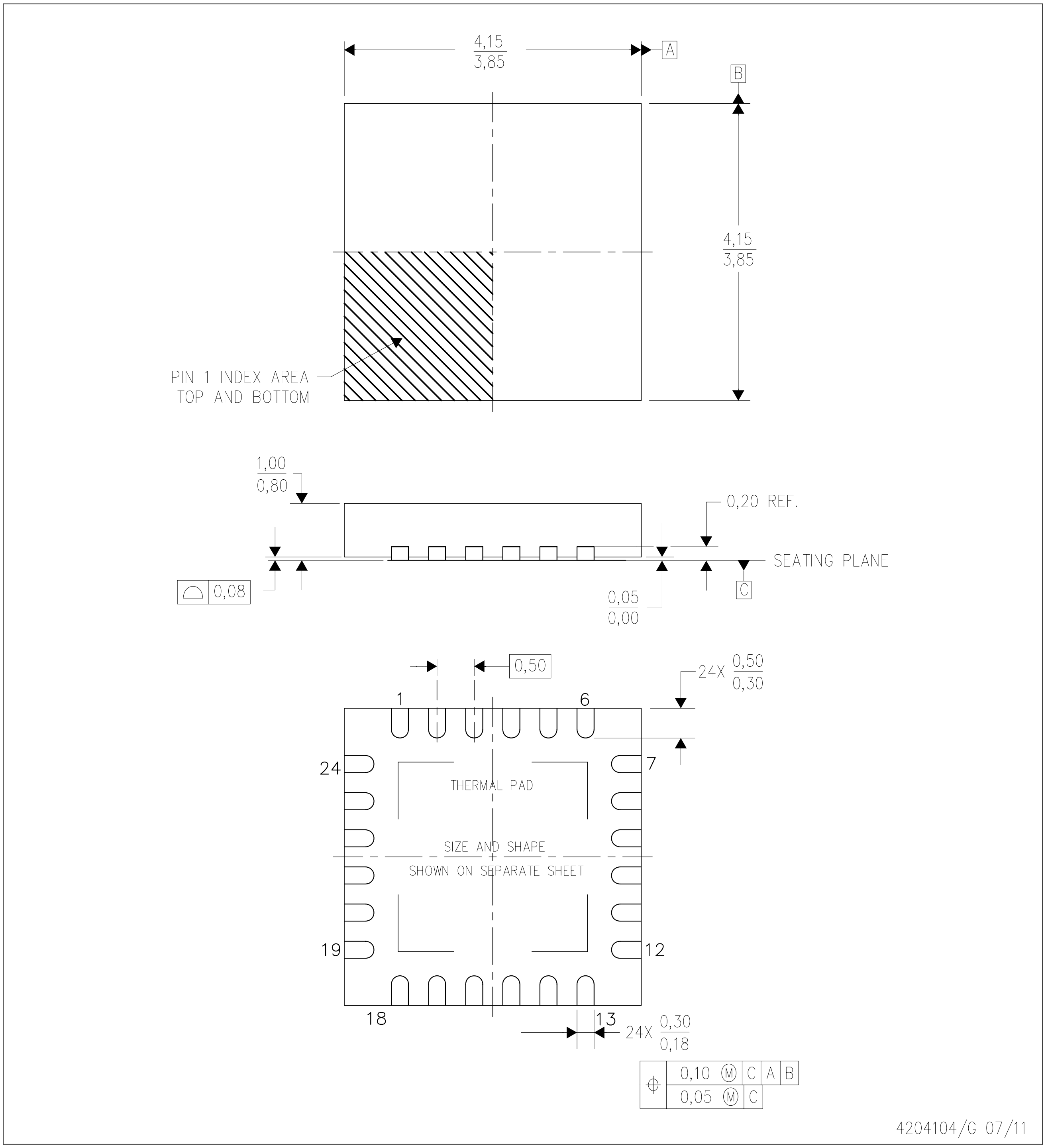
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

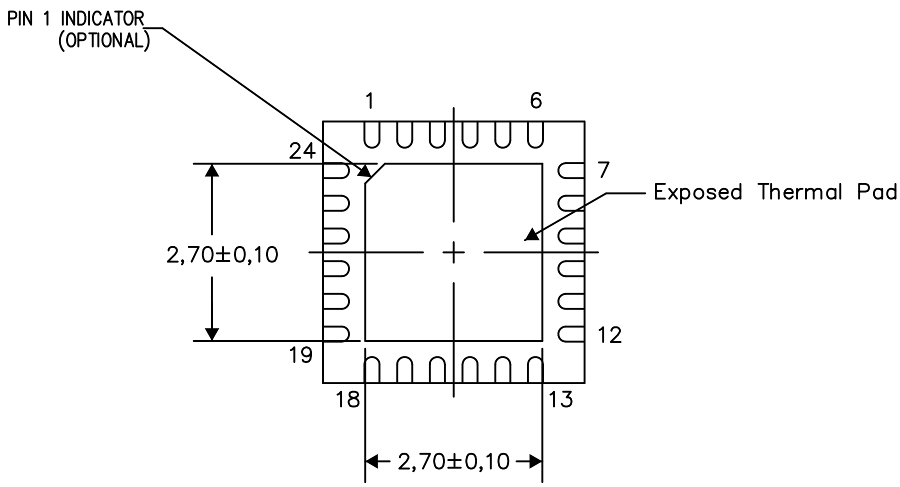
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



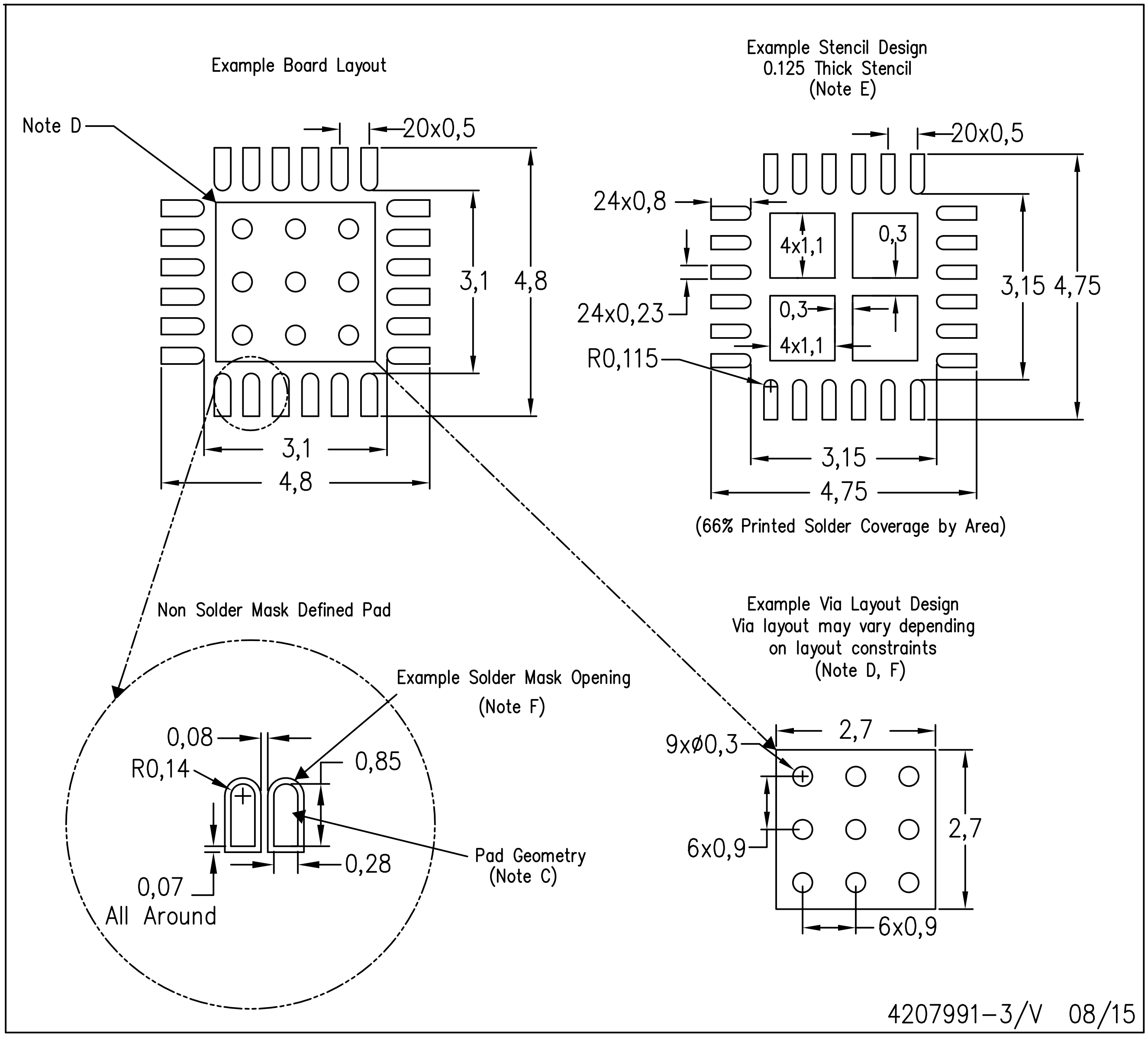
Bottom View

Exposed Thermal Pad Dimensions

4206344-5/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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