

# 16 位, 100kSPS, 串口, 低功耗, 微型, 真差分输入, 逐次逼近寄存器 (SAR) 模数转换器

 查询样片: [ADS8867](#)

## 特性

- 采样速率: **100kHz**
- 无延迟输出
- 单极, 真差分输入范围:  
 $-V_{REF}$  至  $+V_{REF}$
- 宽共模电压范围:  
**0V 至  $V_{REF}$** , 共模抑制比 (CMRR) **90dB** (最小值)
- **SPI™**兼容串行接口, 此接口具有菊花链选项
- 出色的交流和直流性能:
  - 信噪比 (SNR): **96dB**, 总谐波失真 (THD): **-115dB**
  - 积分非线性 (INL):  **$\pm 1.0$  LSB** (最大值)
  - 微分非线性 (DNL):  **$\pm 1.0$  LSB** (最大值), **16 位无丢码 (NMC)**
- 宽运行范围:
  - **AVDD: 2.7V 至 3.6V**
  - **DVDD: 1.65V 至 3.6V** (与 AVDD 无关)
  - **REF: 2.5V 至 5V** (与 AVDD 无关)
  - 工作温度: **-40°C 至 +85°C**
- 低功耗耗散:
  - **100kSPS 时为 0.7mW**
  - **10kSPS 时为 70 $\mu$ W**
- 断电电流 (AVDD): **50nA**
- 满量程阶跃稳定至 **16 位: 1200ns**

- 封装: 微型小外形封装 (**MSOP-10**) 和 小外形尺寸无引线 (**SON-10**) 封装

## 应用范围

- 自动测试设备 (ATE)
- 仪表和处理卡
- 精密医疗设备
- 低功耗、电池供电类仪器

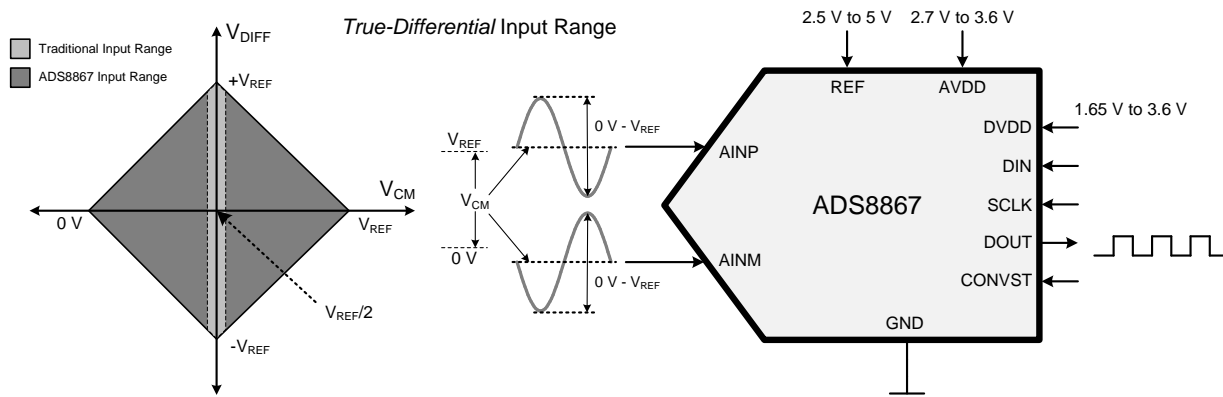
## 说明

ADS8867 是一款 16 位, 100kSPS, 真差分输入, 模数转换器 (ADC)。此器件以 2.5V 至 5V 的外部基准运行, 从而在无需额外的信号调节情况下提供宽信号范围。此基准电压设置独立于, 并且可超过, 模拟电源电压 (AVDD)。

此器件提供一个 SPI 兼容串口, 此串口也支持菊花链操作以实现多个器件级联。

此器件支持单极、真差分模拟输入信号, 此信号的差分输入摆幅为  $-V_{REF}$  至  $+V_{REF}$ 。这个真差分模拟输入结构允许 0V 至  $+V_{REF}$  范围内的任一共模电压值 (当两个输入都在  $-0.1V$  至  $V_{REF}$   $+0.1V$  的运行输入范围内时)。

器件运行针对极低功耗运行进行了优化。功耗直接与速度成比例。这个特性使得 ADS8867 非常适合于低速应用。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TINA is a trademark of Texas Instruments Inc..

SPI is a trademark of Motorola Inc.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**FAMILY INFORMATION<sup>(1)</sup>**

THROUGHPUT	18-BIT, TRUE-DIFFERENTIAL	16-BIT, SINGLE-ENDED	16-BIT, TRUE-DIFFERENTIAL
100 kSPS	ADS8887	ADS8866	ADS8867
250 kSPS	—	—	—
400 kSPS	ADS8885	ADS8864	ADS8865
500 kSPS	—	ADS8319 <sup>(2)</sup>	ADS8318 <sup>(2)</sup>
680 kSPS	ADS8883	ADS8862	ADS8863
1 MSPS	ADS8881	ADS8860	ADS8861

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).
- (2) Pin-to-pin compatible device with AVDD = 5 V.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range, unless otherwise noted.

	VALUE		UNIT
	MIN	MAX	
AINP to GND or AINN to GND	-0.3	REF + 0.3	V
AVDD to GND or DVDD to GND	-0.3	4	V
REF to GND	-0.3	5.7	V
Digital input voltage to GND	-0.3	DVDD + 0.3	V
Digital output to GND	-0.3	DVDD + 0.3	V
Operating temperature range, T <sub>A</sub>	-40	+85	°C
Storage temperature range, T <sub>stg</sub>	-65	+150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *electrical characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		ADS8867		UNITS
		DGS	DRC	
		10 PINS	10 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	151.9	111.1	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	45.4	46.4	
θ <sub>JB</sub>	Junction-to-board thermal resistance	72.2	45.9	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.3	3.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	70.9	45.5	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ ,  $V_{CM} = V_{REF} / 2\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.

Typical specifications are at  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ , and  $DVDD = 3\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>					
Full-scale input span <sup>(1)(2)</sup>	AINP – AINN	$-V_{REF}$		$V_{REF}$	V
Operating input range <sup>(1)(2)</sup>	AINP	-0.1		$V_{REF} + 0.1$	V
	AINN	-0.1		$V_{REF} + 0.1$	V
$V_{CM}$ Input common-mode range		0	$V_{REF} / 2$	$V_{REF}$	V
$C_I$ Input capacitance	AINP and AINN terminal to GND		59		pF
Input leakage current	During acquisition for dc input		5		nA
<b>SYSTEM PERFORMANCE</b>					
Resolution			16		Bits
NMC No missing codes		16			Bits
DNL Differential linearity		-0.99	$\pm 0.5$	1	LSB <sup>(3)</sup>
INL Integral linearity <sup>(4)</sup>		-1	$\pm 0.5$	1	LSB <sup>(3)</sup>
$E_O$ Offset error <sup>(5)</sup>		-4	$\pm 1$	4	mV
Offset error drift with temperature			$\pm 1.5$		$\mu\text{V}/^\circ\text{C}$
$E_G$ Gain error		-0.01	$\pm 0.005$	0.01	%FSR
Gain error drift with temperature			$\pm 0.15$		ppm/ $^\circ\text{C}$
CMRR Common-mode rejection ratio	With common-mode input signal = $5 V_{PP}$ at dc	90	100		dB
PSRR Power-supply rejection ratio	At mid-code		80		dB
Transition noise			0.35		LSB
<b>SAMPLING DYNAMICS</b>					
$t_{conv}$ Conversion time		500		8800	ns
$t_{ACQ}$ Acquisition time		1200			ns
Maximum throughput rate with or without latency				100	kHz
Aperture delay			4		ns
Aperture jitter, RMS			5		ps
Step response	Settling to 16-bit accuracy		1200		ns
Overvoltage recovery	Settling to 16-bit accuracy		1200		ns

(1) Ideal input span, does not include gain or offset error.

(2) Specified for  $V_{CM} = V_{REF} / 2$ . Refer to the [Analog Input](#) section for the effect of  $V_{CM}$  on the full-scale input range.

(3) LSB = least significant bit.

(4) This parameter is the endpoint INL, not best-fit.

(5) Measured relative to actual measured reference.

## ELECTRICAL CHARACTERISTICS (continued)

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ ,  $V_{CM} = V_{REF} / 2\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.

Typical specifications are at  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ , and  $DVDD = 3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC CHARACTERISTICS</b>						
SINAD	Signal-to-noise + distortion <sup>(6)</sup>	At 1 kHz, $V_{REF} = 5\text{ V}$	95	96.4		dB
		At 10 kHz, $V_{REF} = 5\text{ V}$		95.4		dB
		At 49 kHz, $V_{REF} = 5\text{ V}$		91.6		dB
SNR	Signal-to-noise ratio <sup>(6)</sup>	At 1 kHz, $V_{REF} = 5\text{ V}$	95.1	96.5		dB
		At 10 kHz, $V_{REF} = 5\text{ V}$		95.5		dB
		At 49 kHz, $V_{REF} = 5\text{ V}$		92		dB
THD	Total harmonic distortion <sup>(6)(7)</sup>	At 1 kHz, $V_{REF} = 5\text{ V}$		-112		dB
		At 10 kHz, $V_{REF} = 5\text{ V}$		-112		dB
		At 49 kHz, $V_{REF} = 5\text{ V}$		-102		dB
SFDR	Spurious-free dynamic range <sup>(6)</sup>	At 1 kHz, $V_{REF} = 5\text{ V}$		112		dB
		At 10 kHz, $V_{REF} = 5\text{ V}$		112		dB
		At 49 kHz, $V_{REF} = 5\text{ V}$		102		dB
BW <sub>-3dB</sub>	-3-dB small-signal bandwidth			30		MHz
<b>EXTERNAL REFERENCE INPUT</b>						
$V_{REF}$	Input range		2.5		5	V
	Reference input current	During conversion, 100-kHz sample rate, mid-code		35		$\mu\text{A}$
	Reference leakage current			250		nA
$C_{REF}$	Decoupling capacitor at the REF input		10	22		$\mu\text{F}$
<b>POWER-SUPPLY REQUIREMENTS</b>						
Power-supply voltage	AVDD	Analog supply	2.7	3	3.6	V
	DVDD	Digital supply range	1.65	1.8	3.6	V
Supply current	AVDD	100-kHz sample rate, $AVDD = 3\text{ V}$		0.23	0.4	mA
$P_{VA}$	Power dissipation	100-kHz sample rate, $AVDD = 3\text{ V}$		0.7	1.2	mW
		10-kHz sample rate, $AVDD = 3\text{ V}$		70		$\mu\text{W}$
$I_{APD}$	Device power-down current <sup>(8)</sup>			50		nA
<b>DIGITAL INPUTS: LOGIC FAMILY (CMOS)</b>						
$V_{IH}$	High-level input voltage	$1.65\text{ V} < DVDD < 2.3\text{ V}$	$0.8 \times DVDD$		$DVDD + 0.3$	V
		$2.3\text{ V} < DVDD < 3.6\text{ V}$	$0.7 \times DVDD$		$DVDD + 0.3$	V
$V_{IL}$	Low-level input voltage	$1.65\text{ V} < DVDD < 2.3\text{ V}$	-0.3		$0.2 \times DVDD$	V
		$2.3\text{ V} < DVDD < 3.6\text{ V}$	-0.3		$0.3 \times DVDD$	V
$I_{LK}$	Digital input leakage current			$\pm 10$	$\pm 100$	nA
<b>DIGITAL OUTPUTS: LOGIC FAMILY (CMOS)</b>						
$V_{OH}$	High-level output voltage	$I_O = 500\text{-}\mu\text{A}$ source, $C_{LOAD} = 20\text{ pF}$	$0.8 \times DVDD$		$DVDD$	V
$V_{OL}$	Low-level output voltage	$I_O = 500\text{-}\mu\text{A}$ sink, $C_{LOAD} = 20\text{ pF}$	0		$0.2 \times DVDD$	V
<b>TEMPERATURE RANGE</b>						
$T_A$	Operating free-air temperature		-40		+85	$^\circ\text{C}$

(6) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.

(7) Calculated on the first nine harmonics of the input frequency.

(8) The device automatically enters a power-down state at the end of every conversion, and remains in power-down during the acquisition phase.

## TIMING CHARACTERISTICS

### 3-WIRE OPERATION

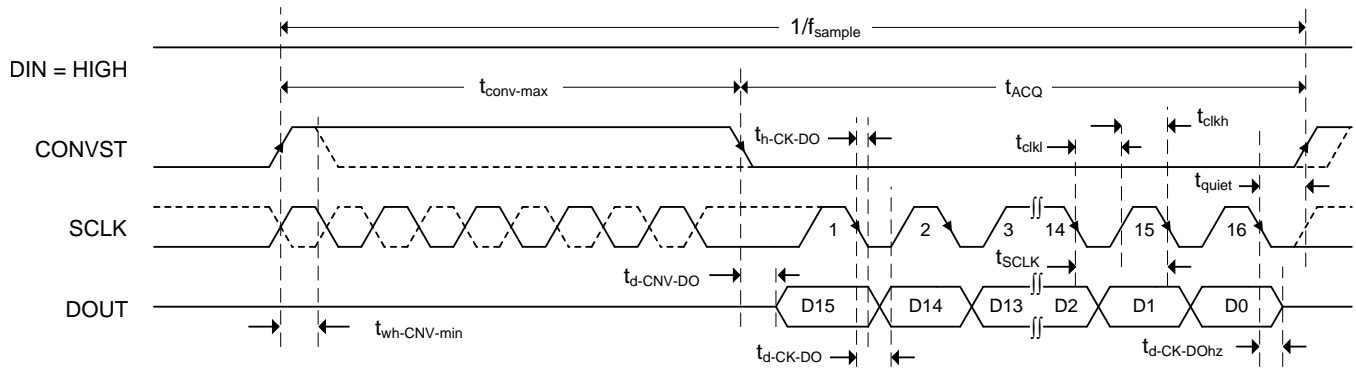


Figure 1. 3-Wire Operation: CONVST Functions as Chip Select

Table 1. TIMING REQUIREMENTS: 3-Wire Operation<sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
$t_{ACQ}$	Acquisition time	1200			ns
$t_{conv}$	Conversion time	500		8800	ns
$1/f_{sample}$	Time between conversions	10000			ns
$t_{wh-CNV}$	Pulse duration: CONVST high	10			ns
$f_{SCLK}$	SCLK frequency			16	MHz
$t_{SCLK}$	SCLK period	62.5			ns
$t_{ckl}$	SCLK low time	0.45		0.55	$t_{SCLK}$
$t_{ckh}$	SCLK high time	0.45		0.55	$t_{SCLK}$
$t_{h-CK-DO}$	SCLK falling edge to current data invalid	3			ns
$t_{d-CK-DO}$	SCLK falling edge to next data valid delay			13.4	ns
$t_{d-CNV-DO}$	Enable time: CONVST low to MSB valid			12.3	ns
$t_{d-CNV-DOhz}$	Disable time: CONVST high or last SCLK falling edge to DOUT 3-state ( $\overline{CS}$ mode)			13.2	ns
$t_{quiet}$	Quiet time	20			ns

(1) All specifications are at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ , and  $DVDD = 3\text{ V}$ , unless otherwise noted.

### 4-WIRE OPERATION

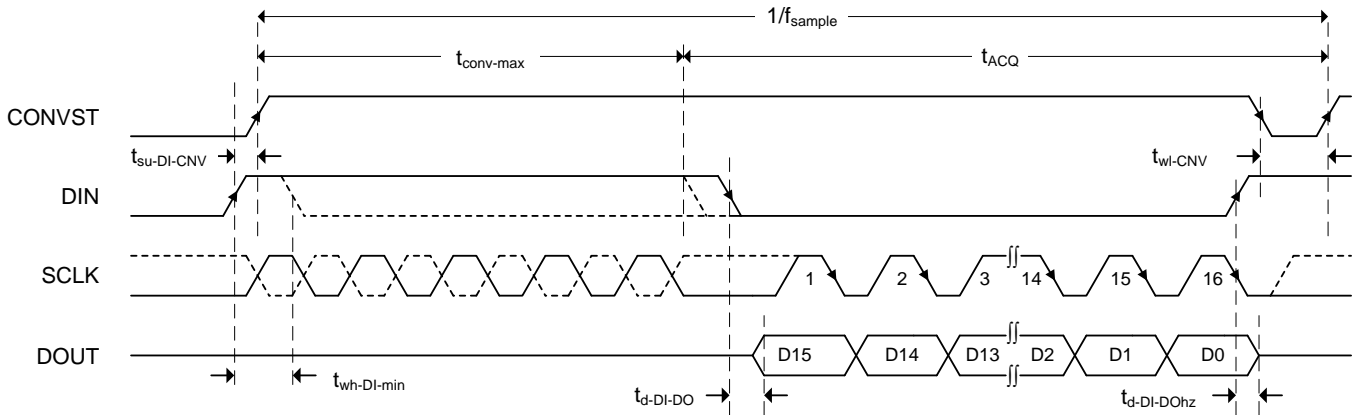


Figure 2. 4-Wire Operation: DIN Functions as Chip Select

Table 2. TIMING REQUIREMENTS: 4-Wire Operation<sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
$t_{ACQ}$	Acquisition time	1200			ns
$t_{conv}$	Conversion time	500		8800	ns
$1/f_{sample}$	Time between conversions	10000			ns
$t_{wh-DI}$	Pulse duration: DIN high	10			ns
$t_{wl-CNV}$	Pulse width: CONVST low	20			ns
$t_{d-DI-DO}$	Delay time: DIN low to MSB valid			12.3	ns
$t_{d-DI-DOhz}$	Delay time: DIN high or last SCLK falling edge to DOUT 3-state			13.2	ns
$t_{su-DI-CNV}$	Setup time: DIN high to CONVST rising edge	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN high from CONVST rising edge	0			ns

(1) All specifications are at  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $AVDD = 3 V$ , and  $DVDD = 3 V$ , unless otherwise noted.

DAISY-CHAIN OPERATION

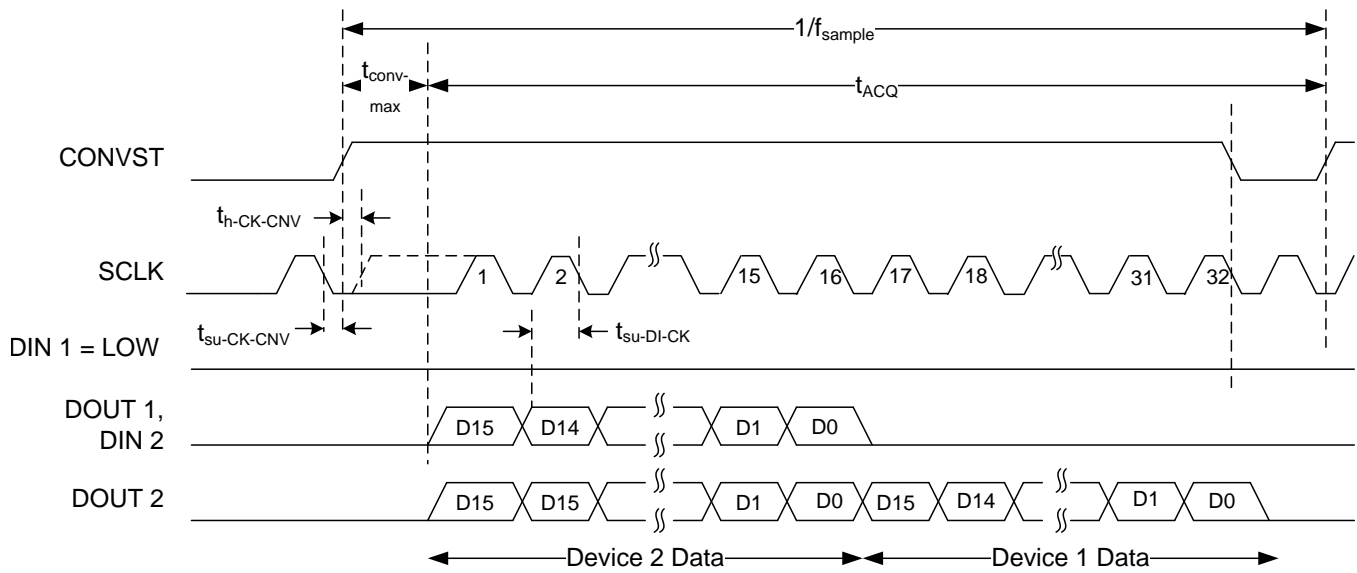


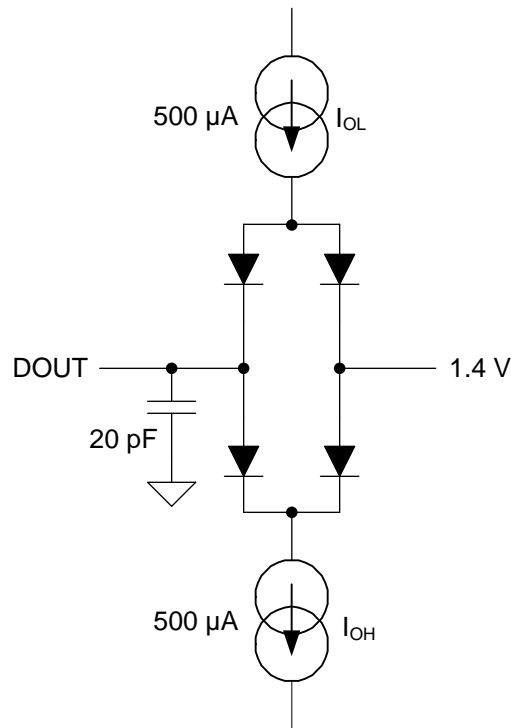
Figure 3. Daisy-Chain Operation: Two Devices

Table 3. TIMING REQUIREMENTS: Daisy-Chain<sup>(1)</sup>

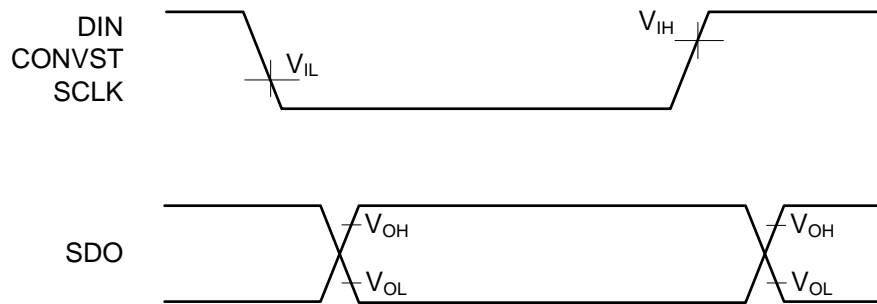
PARAMETER		MIN	TYP	MAX	UNIT
$t_{ACQ}$	Acquisition time	1200			ns
$t_{conv}$	Conversion time	500		8800	ns
$1/f_{sample}$	Time between conversions	10000			ns
$t_{su-CK-CNV}$	Setup time: SCLK valid to CONVST rising edge	5			ns
$t_{h-CK-CNV}$	Hold time: SCLK valid from CONVST rising edge	5			ns
$t_{su-DI-CNV}$	Setup time: DIN low to CONVST rising edge (see )	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN low from CONVST rising edge	0			ns
$t_{su-DI-CK}$	Setup time: DIN valid to SCLK falling edge	1.5			ns

(1) All specifications are at  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $AVDD = 3 V$ , and  $DVDD = 3 V$ , unless otherwise noted.

**EQUIVALENT CIRCUITS**



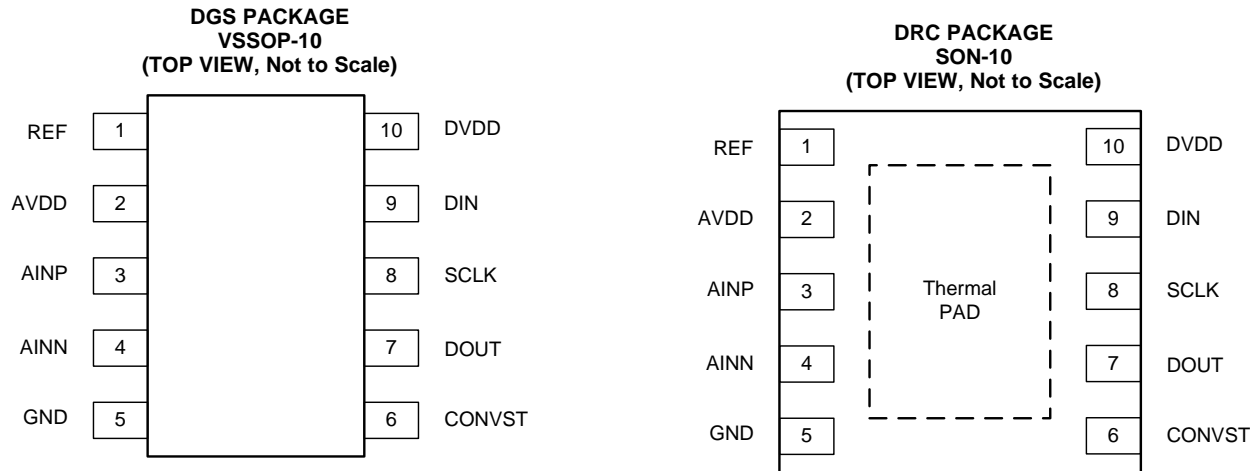
**Figure 4. Load Circuit for Digital Interface Timing**



**Figure 5. Voltage Levels for Timing**



## PIN CONFIGURATIONS



## PIN ASSIGNMENTS

PIN NAME	PIN NUMBER	FUNCTION	DESCRIPTION
AINN	4	Analog input	Inverting analog signal input
AINP	3	Analog input	Noninverting analog signal input
AVDD	2	Analog	Analog power supply. This pin must be decoupled to GND with a 1- $\mu$ F capacitor.
CONVST	6	Digital input	Convert input. This pin also functions as the $\overline{CS}$ input in 3-wire interface mode. Refer to the <a href="#">Description</a> and <a href="#">Timing Characteristics</a> sections for more details.
DIN	9	Digital input	Serial data input. The DIN level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode. Refer to the <a href="#">Description</a> and <a href="#">Timing Characteristics</a> sections for more details.
DOUT	7	Digital output	Serial data output
DVDD	10	Power supply	Digital interface power supply. This pin must be decoupled to GND with a 1- $\mu$ F capacitor.
GND	5	Analog, digital	Device ground. Note that this pin is a common ground pin for both the analog power supply (AVDD) and digital I/O supply (DVDD). The reference return line is also internally connected to this pin.
REF	1	Analog	Positive reference input. This pin must be decoupled with a 10- $\mu$ F or larger capacitor.
SCLK	8	Digital input	Clock input for serial interface. Data output (on DOUT) are synchronized with this clock.
Thermal pad	—	Thermal pad	Exposed thermal pad. Texas Instruments recommends connecting the thermal pad to the printed circuit board (PCB) ground.

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.

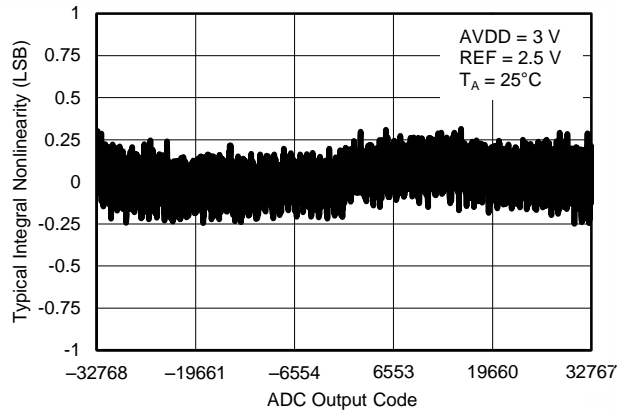


Figure 6. TYPICAL INL ( $V_{REF} = 2.5\text{ V}$ )

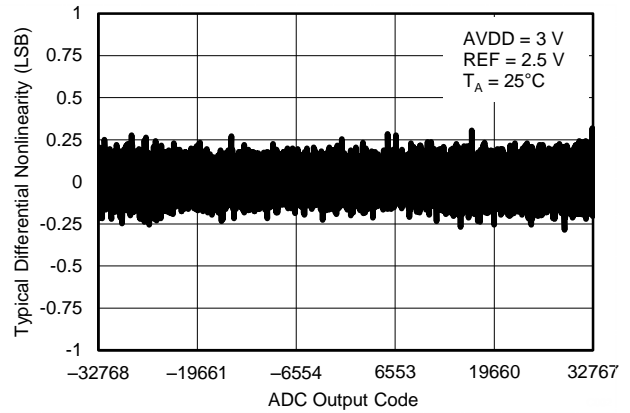


Figure 7. TYPICAL DNL ( $V_{REF} = 2.5\text{ V}$ )

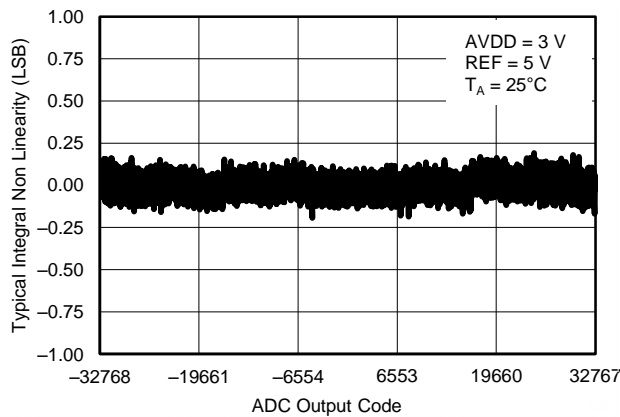


Figure 8. TYPICAL INL ( $V_{REF} = 5\text{ V}$ )

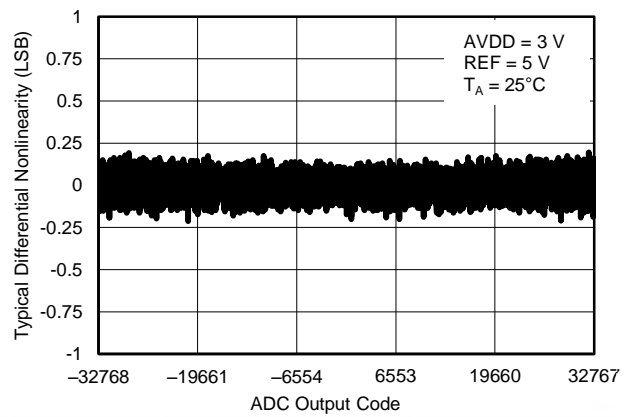


Figure 9. TYPICAL DNL ( $V_{REF} = 5\text{ V}$ )

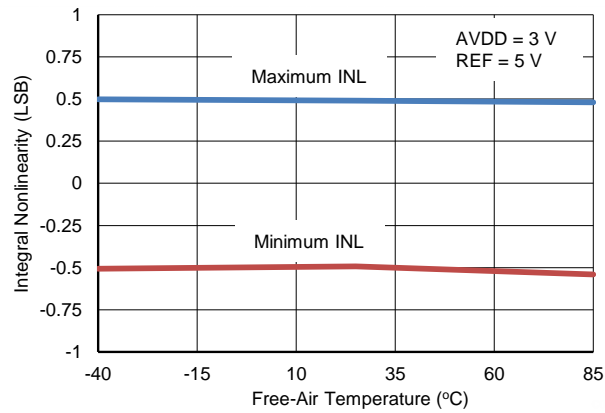


Figure 10. INL vs TEMPERATURE

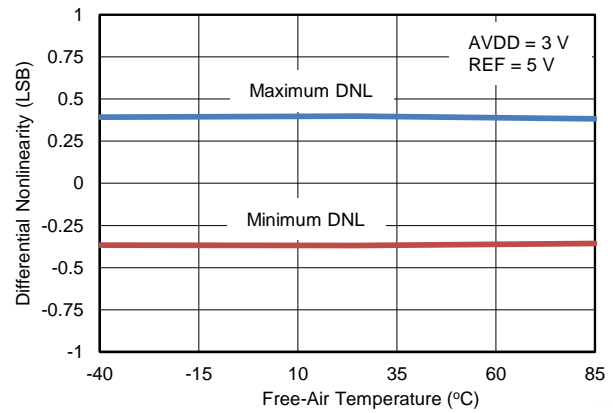
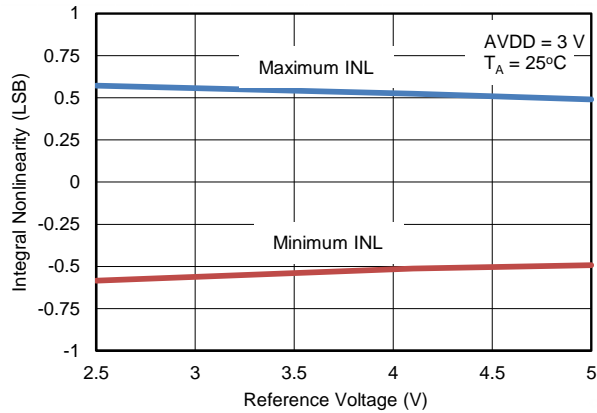


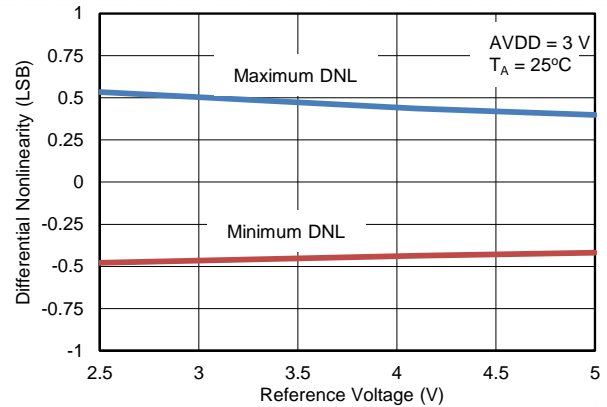
Figure 11. DNL vs TEMPERATURE

**TYPICAL CHARACTERISTICS (continued)**

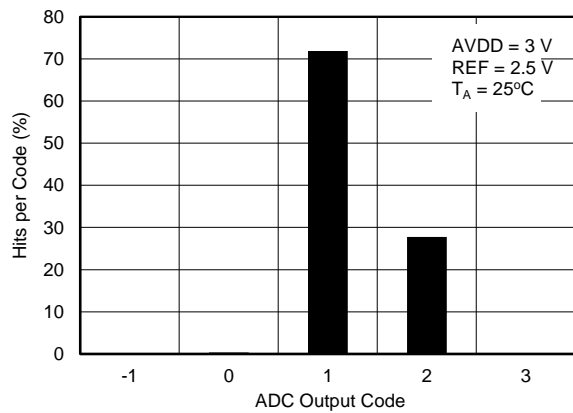
At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.



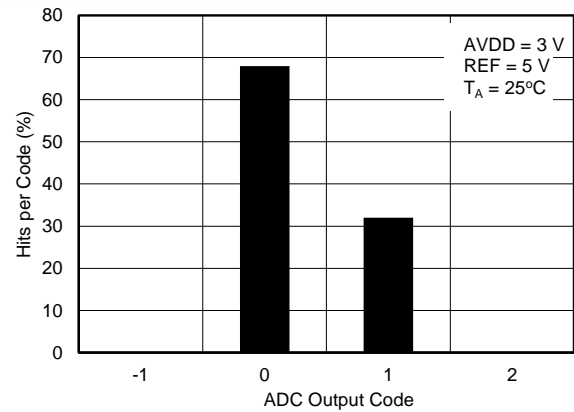
**Figure 12. INL vs REFERENCE VOLTAGE**



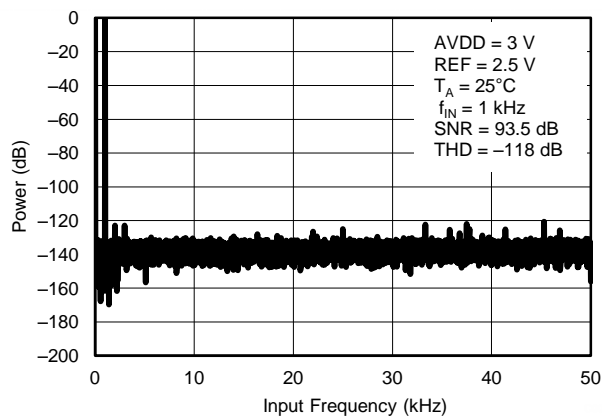
**Figure 13. DNL vs REFERENCE VOLTAGE**



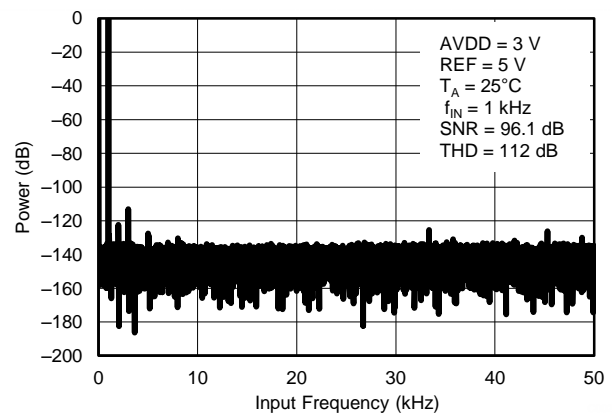
**Figure 14. DC INPUT HISTOGRAM ( $V_{REF} = 2.5\text{ V}$ )**



**Figure 15. DC INPUT HISTOGRAM ( $V_{REF} = 5\text{ V}$ )**



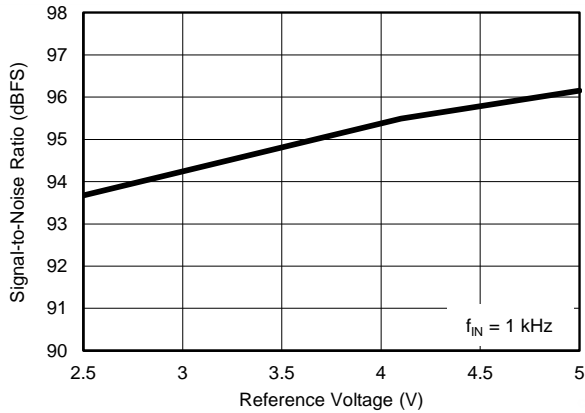
**Figure 16. TYPICAL FFT ( $V_{REF} = 2.5\text{ V}$ )**



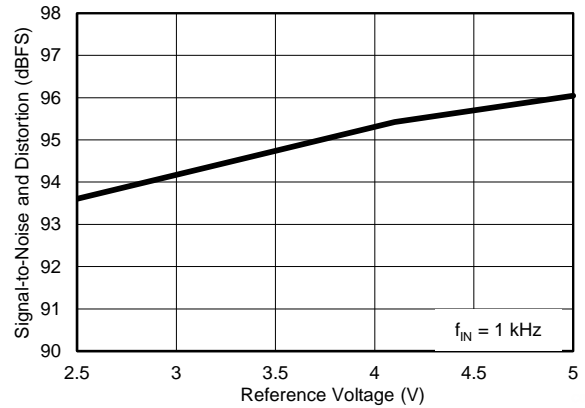
**Figure 17. TYPICAL FFT ( $V_{REF} = 5\text{ V}$ )**

**TYPICAL CHARACTERISTICS (continued)**

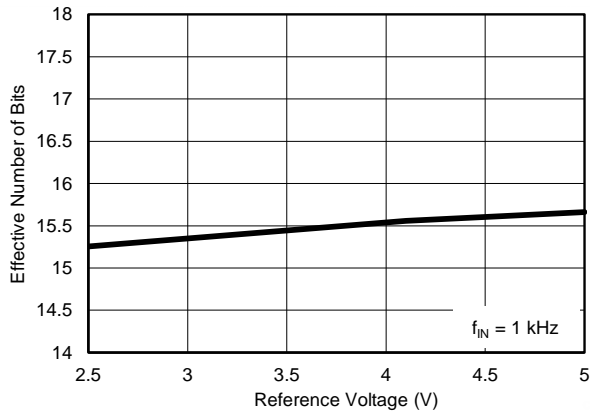
At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.



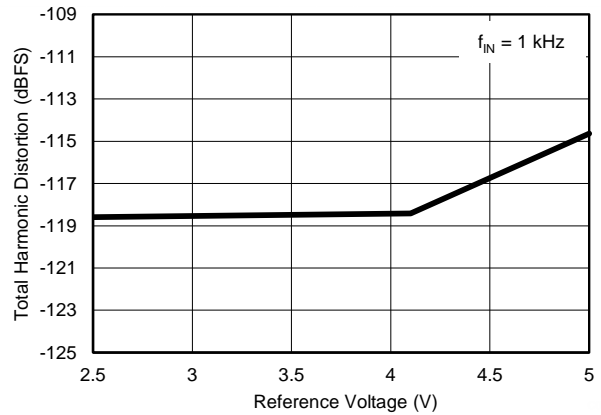
**Figure 18. SNR vs REFERENCE VOLTAGE**



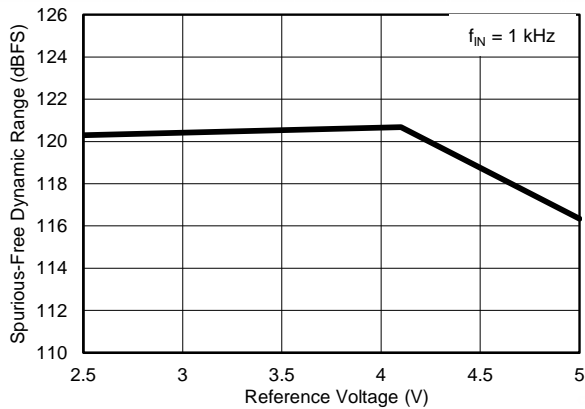
**Figure 19. SINAD vs REFERENCE VOLTAGE**



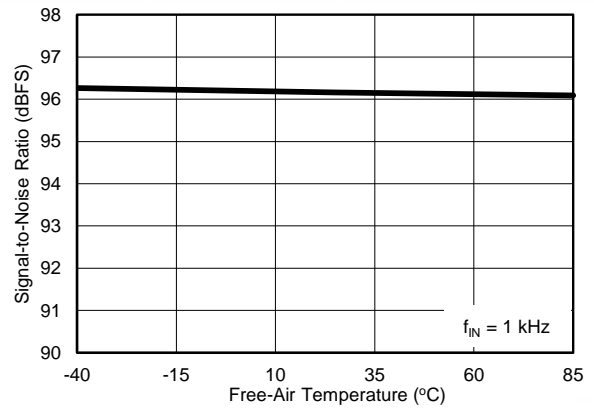
**Figure 20. ENOB vs REFERENCE VOLTAGE**



**Figure 21. THD vs REFERENCE VOLTAGE**



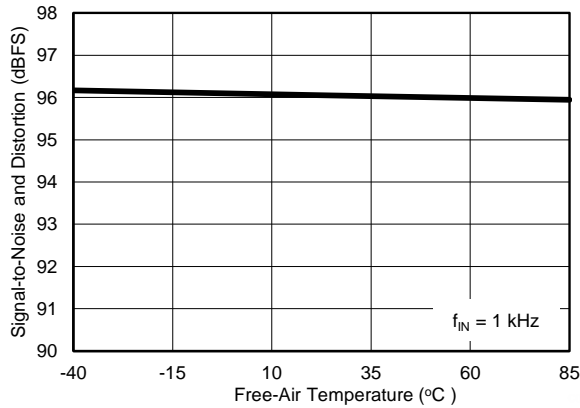
**Figure 22. SFDR vs REFERENCE VOLTAGE**



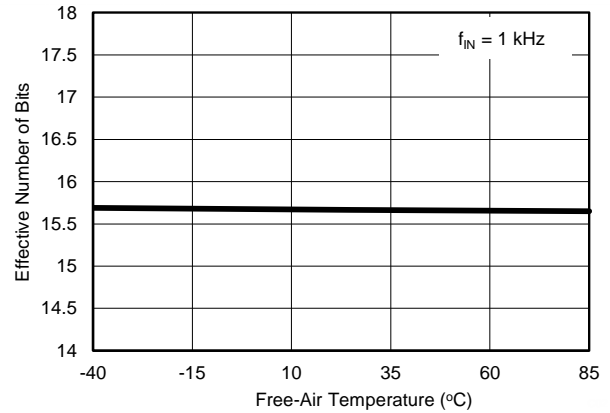
**Figure 23. SNR vs TEMPERATURE**

**TYPICAL CHARACTERISTICS (continued)**

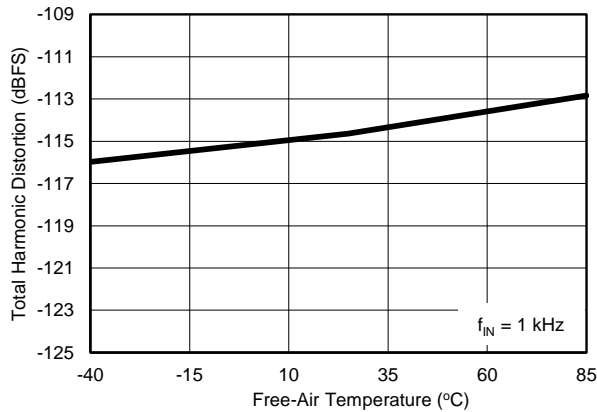
At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.



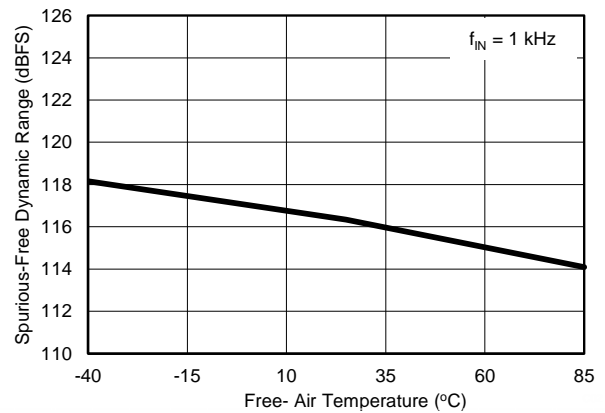
**Figure 24. SINAD vs TEMPERATURE**



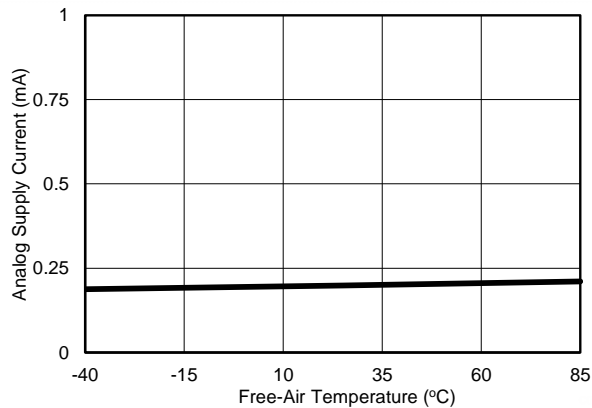
**Figure 25. ENOB vs TEMPERATURE**



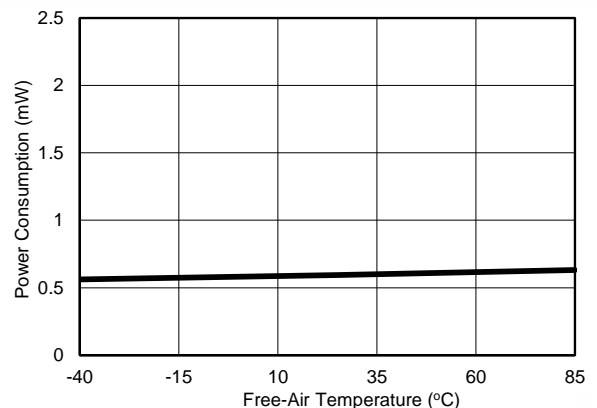
**Figure 26. THD vs TEMPERATURE**



**Figure 27. SFDR vs TEMPERATURE**



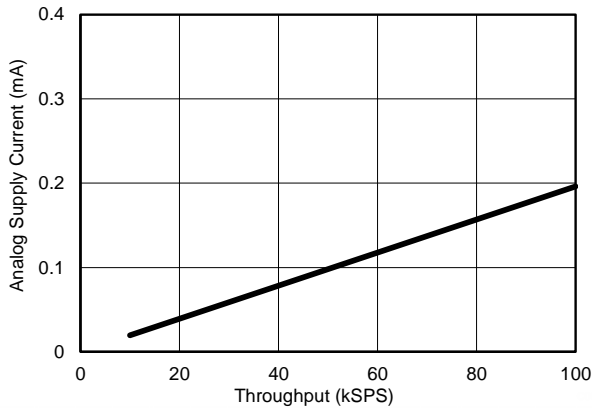
**Figure 28. SUPPLY CURRENT vs TEMPERATURE**



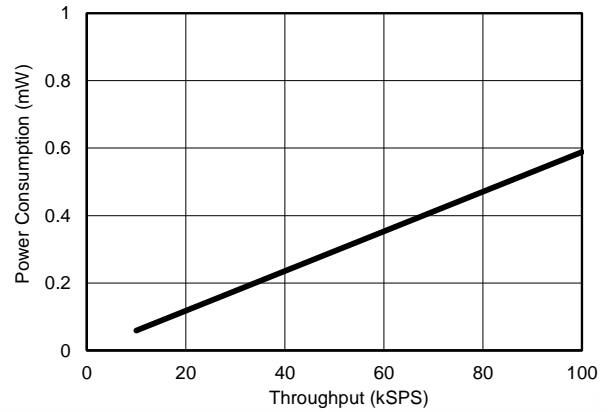
**Figure 29. POWER CONSUMPTION vs TEMPERATURE**

**TYPICAL CHARACTERISTICS (continued)**

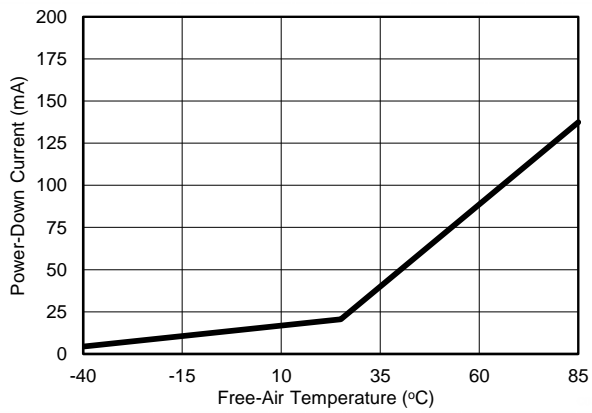
At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.



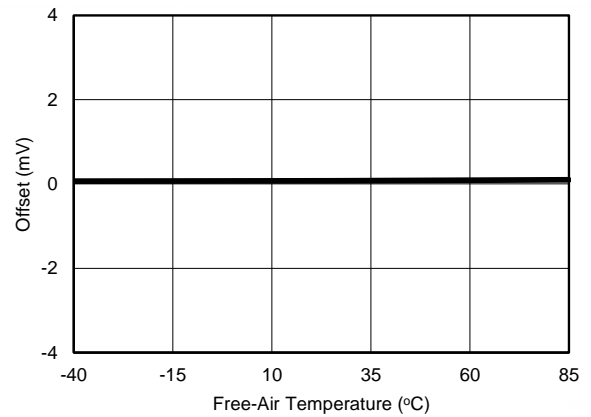
**Figure 30. SUPPLY CURRENT vs THROUGHPUT**



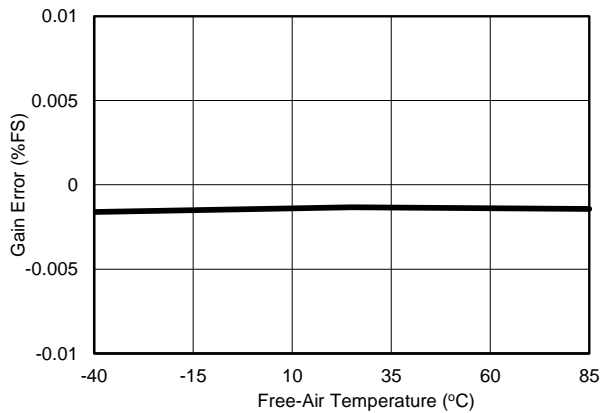
**Figure 31. POWER CONSUMPTION vs THROUGHPUT**



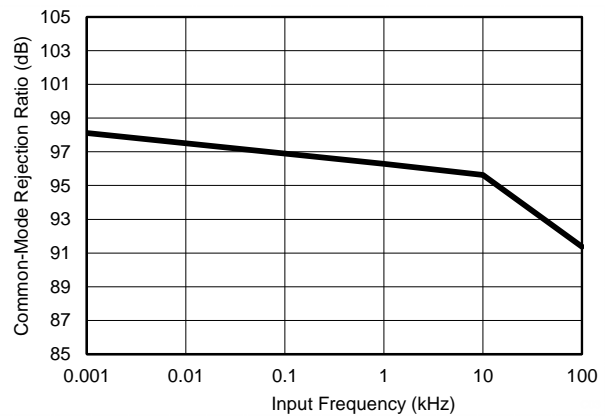
**Figure 32. POWER-DOWN CURRENT vs TEMPERATURE**



**Figure 33. OFFSET vs TEMPERATURE**



**Figure 34. GAIN ERROR vs TEMPERATURE**



**Figure 35. CMRR vs INPUT FREQUENCY**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 100\text{ kSPS}$ , unless otherwise noted.

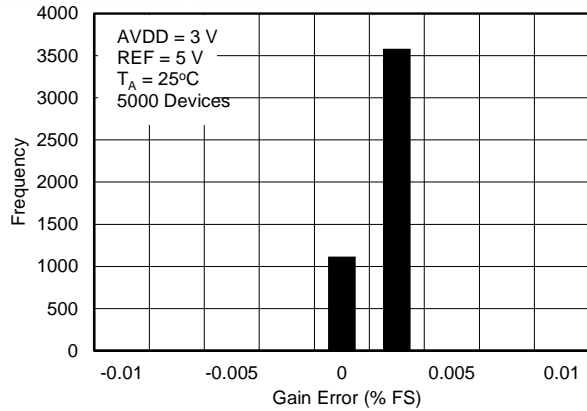


Figure 36. TYPICAL DISTRIBUTION OF GAIN ERROR

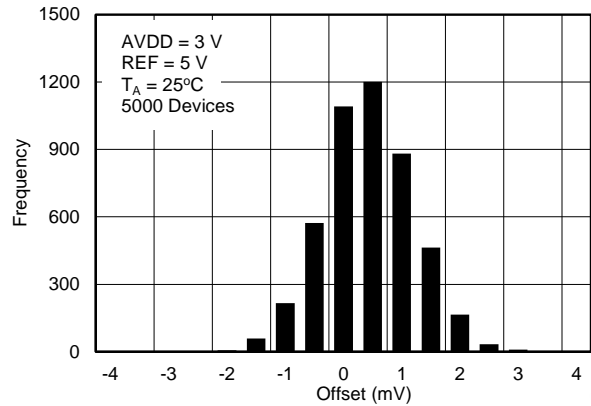


Figure 37. TYPICAL DISTRIBUTION OF OFFSET ERROR

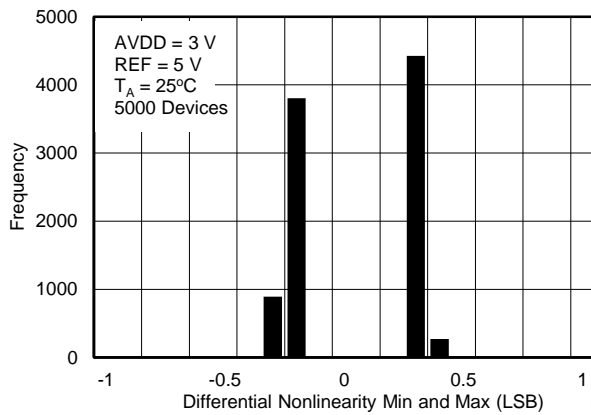


Figure 38. TYPICAL DISTRIBUTION OF DIFFERENTIAL NONLINEARITY (Minimum and Maximum)

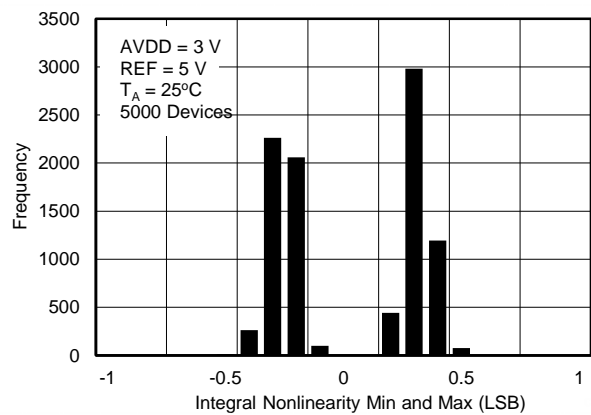


Figure 39. TYPICAL DISTRIBUTION OF INTEGRAL NONLINEARITY (Minimum and Maximum)

## OVERVIEW

The ADS8867 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) from a 16- and 18-bit product family. This compact device features high performance. Power consumption is inherently low and scales linearly with sampling speed. The architecture is based on charge redistribution, which inherently includes a sample-and-hold (S/H) function.

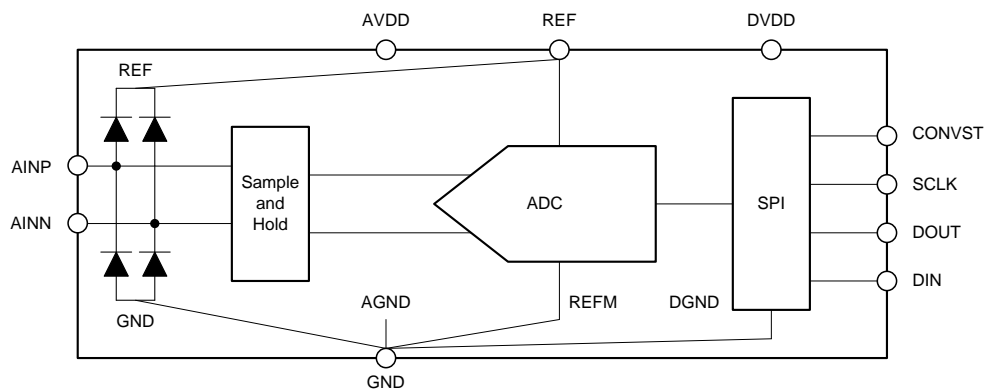
The ADS8867 supports a true-differential analog input across two pins (INP and INN). When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the INP and INN inputs are disconnected from the internal circuit.

The ADS8867 uses an internal clock to perform conversions. The device reconnects the sampling capacitors to the INP and INN pins after conversion and then enters an acquisition phase. During the acquisition phase, the device is powered down and the conversion result can be read.

The device digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs) easy.

## ANALOG INPUT

As shown in [Figure 40](#), the device features a differential analog input. Both positive and negative inputs are individually sampled on 55-pF sampling capacitors and the device converts for the voltage difference between the two sampled values:  $V_{INP} - V_{INN}$ .



**Figure 40. Detailed Block Diagram**



Most differential input SAR ADCs prohibit the input common-mode voltage,  $V_{CM}$  (that is, the average voltage between the inputs), at AINP or AINM from varying more than approximately 10% beyond the mid-scale input value. As shown in Figure 41, the device has a unique common-mode voltage detection and rejection block that does not have this restriction and thus allows  $V_{CM}$  to be set to any value between 0 V and  $V_{REF}$  without degrading device performance.

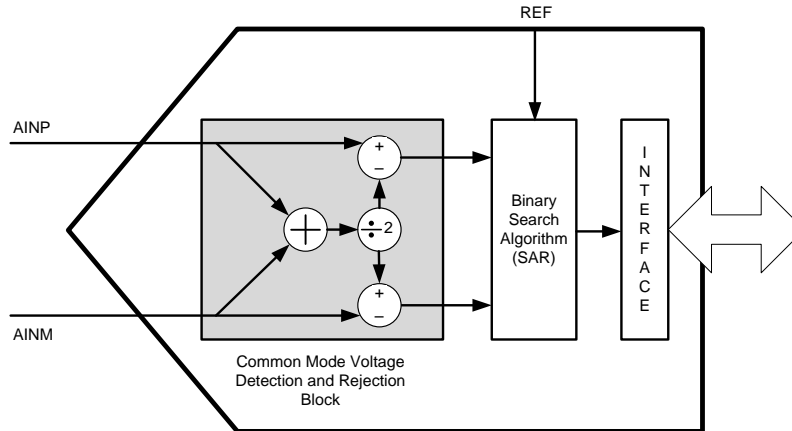


Figure 41. Conceptual Diagram: True Differential Input Structure

Table 4 shows the full-scale input range of the device as a function of input common-mode voltage. The device offers a maximum dynamic range for  $V_{CM} = V_{REF} / 2$ . The differential input with wide common-mode range allows connecting differential signals from sensors without any signal conditioning.

Table 4. Full-Scale Input Range

$V_{CM}$	ABSOLUTE INPUT RANGE		FULL SCALE INPUT RANGE ( $V_{FS}$ )
	$V_{AINP}$	$V_{AINN}$	
$V_{CM} < V_{REF} / 2$	0 to $2 \times V_{CM}$	0 to $2 \times V_{CM}$	$(-2 \times V_{CM})$ to $(2 \times V_{CM})$
$V_{CM} = V_{REF} / 2$	0 to $V_{REF}$	0 to $V_{REF}$	$(-V_{REF})$ to $(V_{REF})$
$V_{CM} > V_{REF} / 2$	$(2 \times V_{CM} - V_{REF})$ to $V_{REF}$	$(2 \times V_{CM} - V_{REF})$ to $V_{REF}$	$(-2 \times (V_{CM} - V_{REF}))$ to $(2 \times (V_{CM} - V_{REF}))$

Figure 42 shows an equivalent circuit of the input sampling stage. The sampling switch is represented by a 96- $\Omega$  resistance in series with the ideal switch. Refer to the ADC Input Driver section for more details on the recommended driving circuits.

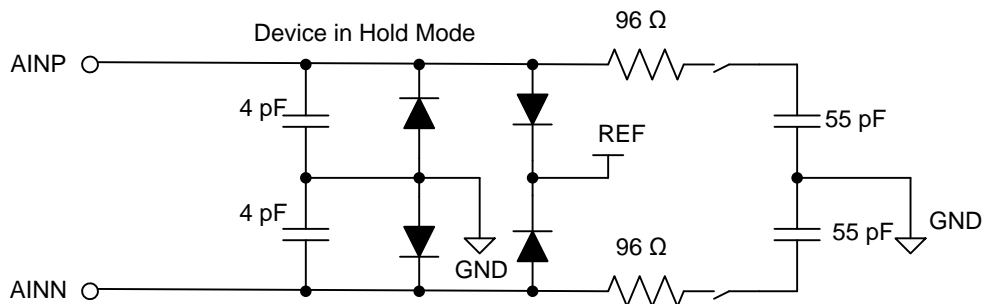
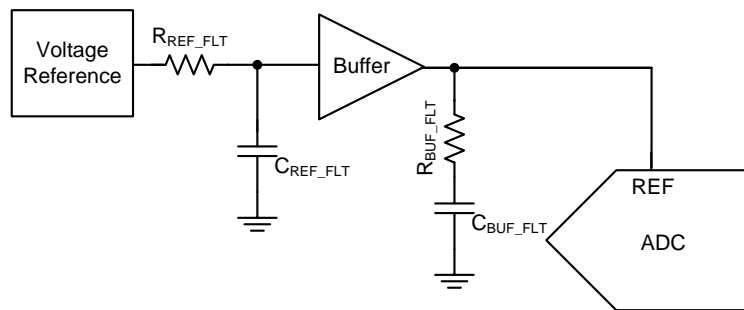


Figure 42. Input Sampling Stage Equivalent Circuit

Figure 40 and Figure 42 illustrate electrostatic discharge (ESD) protection diodes to REF and GND from both analog inputs. Make sure that these diodes do not turn on by keeping the analog inputs within the specified range.

## REFERENCE

The device operates with an external reference voltage and switches binary-weighted capacitors onto the reference terminal (REF pin) during the conversion process. The switching frequency is proportional to the internal conversion clock frequency but the dynamic charge requirements are a function of the absolute value of the input voltage and reference voltage. This dynamic load must be supported by a reference driver circuit without degrading the noise and linearity performance of the device. During the acquisition process, the device automatically powers down and does not take any dynamic current from the external reference source. The basic circuit diagram for such a reference driver circuit for precision ADCs is shown in [Figure 43](#). Refer to the [ADC Reference Driver](#) section for more details on the application circuits.



**Figure 43. Reference Driver Schematic**

## CLOCK

The device uses an internal clock for conversion. Conversion duration may vary but is bounded by the minimum and maximum value of  $t_{conv}$ , as specified in the [Timing Characteristics](#) section. An external SCLK is only used for a serial data read operation. Data are read after a conversion completes and when the device is in acquisition phase for the next sample.

## ADC TRANSFER FUNCTION

The ADS8867 is a unipolar, differential input device. The device output is in twos complement format.

Figure 44 shows ideal characteristics for the device. The full-scale range for the ADC input ( $A_{INP} - A_{INN}$ ) is equal to twice the reference input voltage to the ADC ( $2 \times V_{REF}$ ). The LSB for the ADC is given by Equation 1.

$$1 \text{ LSB} = [2 \times (V_{REF} / 2^{16})] \quad (1)$$

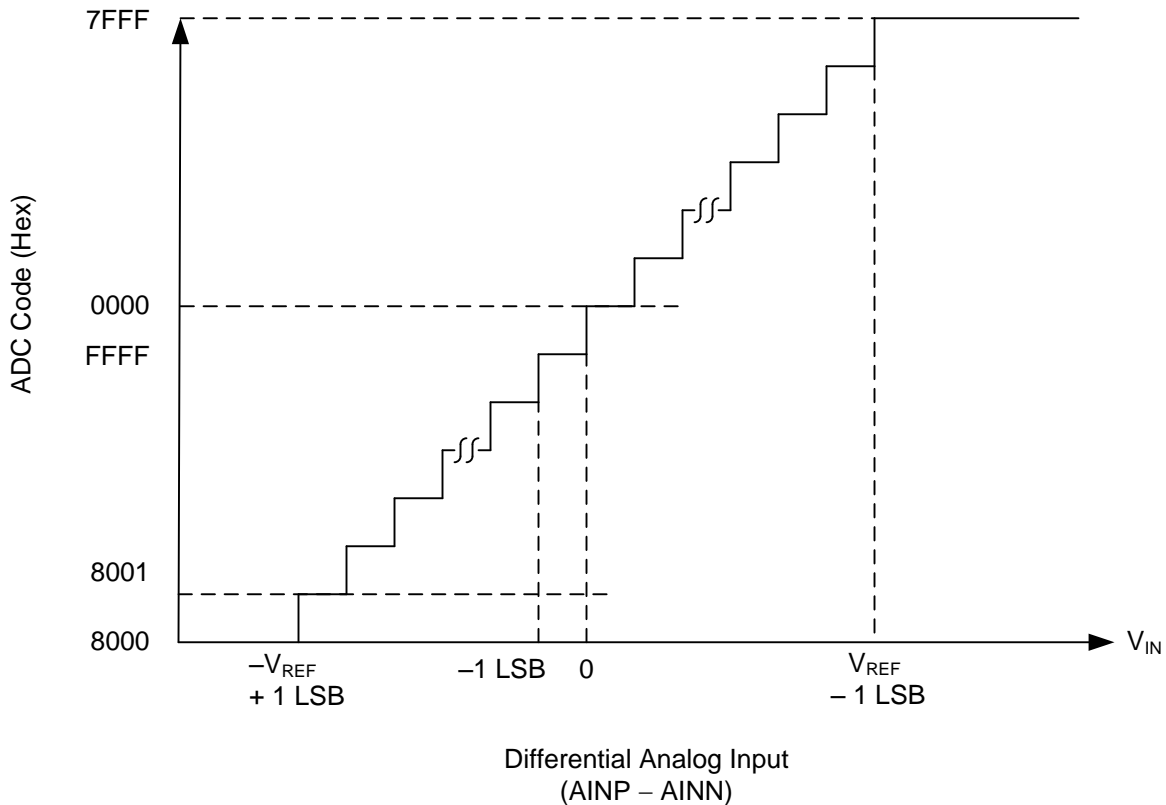


Figure 44. Transfer Characteristics

## DIGITAL INTERFACE

The ADS8867 is a low pin-count device. However, the device offers three different options for interfacing with the digital host.

These options can be broadly classified as being either  $\overline{CS}$  mode (in either a 3- or 4-wire interface) or *daisy-chain mode*. The device operates in  $\overline{CS}$  mode if  $\overline{DIN}$  is high at the  $\overline{CONVST}$  rising edge. If  $\overline{DIN}$  is low at the  $\overline{CONVST}$  rising edge, or if  $\overline{DIN}$  and  $\overline{CONVST}$  are connected together, the device operates in daisy-chain mode.

The 3-wire interface in  $\overline{CS}$  mode is useful for applications that need galvanic isolation on-board. The 4-wire interface in  $\overline{CS}$  mode allows the user to sample the analog input independent of the serial interface timing and, therefore, allows easier control of an individual device while having multiple, similar devices on-board. The daisy-chain mode is provided to hook multiple devices in a chain similar to a shift register and is useful in reducing component count and the number of signal traces on the board.

### $\overline{CS}$ Mode

$\overline{CS}$  mode is selected if  $\overline{DIN}$  is high at the  $\overline{CONVST}$  rising edge. There are two different interface options available in this mode: 3-wire  $\overline{CS}$  mode, and 4-wire  $\overline{CS}$  mode. The following sections discuss these interface options in detail.

### 3-Wire $\overline{CS}$ Mode

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host. In this interface option, DIN can be connected to DVDD and CONVST functions as  $\overline{CS}$  (as shown in Figure 45). As shown in Figure 46, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as  $\overline{CS}$ ) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must return high before the minimum conversion time ( $t_{conv-min}$ ) elapses and is held high until the maximum possible conversion time ( $t_{conv-max}$ ) elapses.

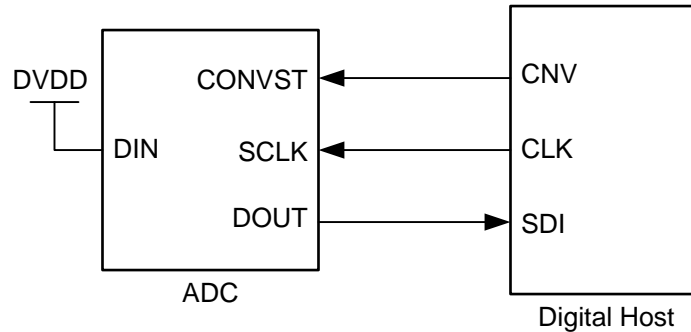


Figure 45. Connection Diagram: 3-Wire  $\overline{CS}$  Mode (DIN = 1)

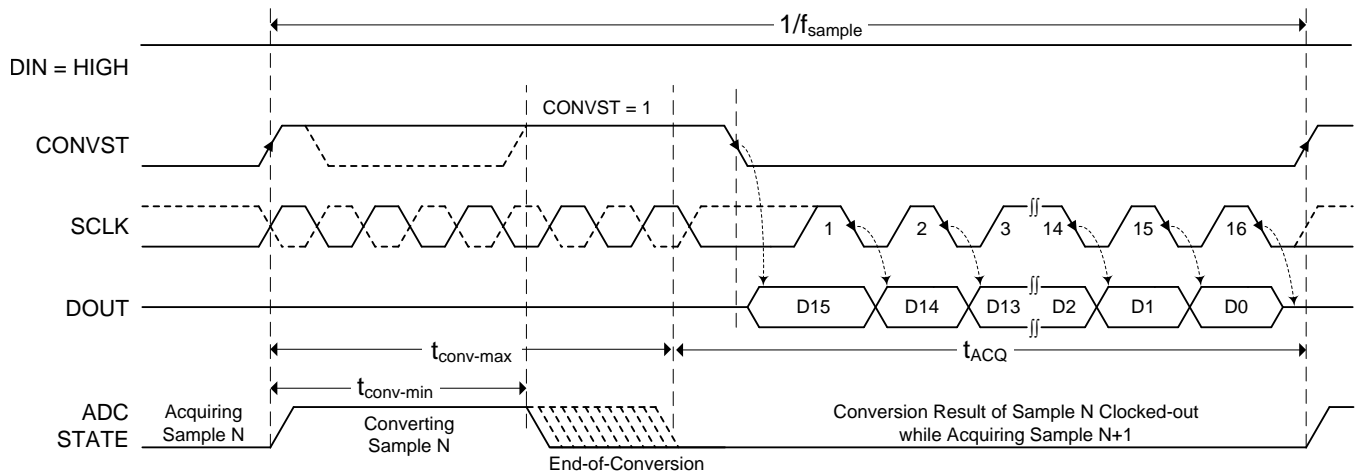


Figure 46. Interface Timing Diagram: 3-Wire  $\overline{CS}$  Mode (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down. CONVST (functioning as  $\overline{CS}$ ) can be brought low after the maximum conversion time ( $t_{conv-max}$ ) elapses. On the CONVST falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided  $t_{h\_CK\_DO}$  is acceptable). DOUT goes to 3-state after the 16th SCLK falling edge or when CONVST goes high, whichever occurs first.

### 4-Wire $\overline{CS}$ Mode

This interface option is useful when one or more ADCs are connected to an SPI-compatible digital host. Figure 47 shows the connection diagram for single ADC, Figure 49 shows the connection diagram for two ADCs.

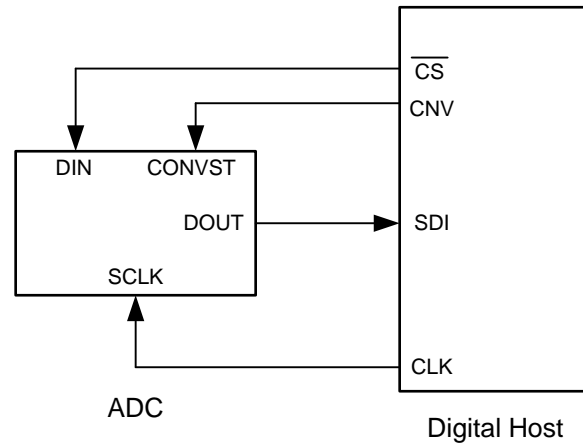


Figure 47. Connection Diagram: Single ADC with 4-Wire  $\overline{CS}$  Mode

In this interface option, DIN is controlled by the digital host and functions as  $\overline{CS}$ . As shown in Figure 48, with DIN high, a CONVST rising edge selects  $\overline{CS}$  mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (functioning as  $\overline{CS}$ ) can be pulled low to select other devices on the board. However, DIN must be pulled high before the minimum conversion time ( $t_{conv-min}$ ) elapses and remains high until the maximum possible conversion time ( $t_{conv-max}$ ) elapses.

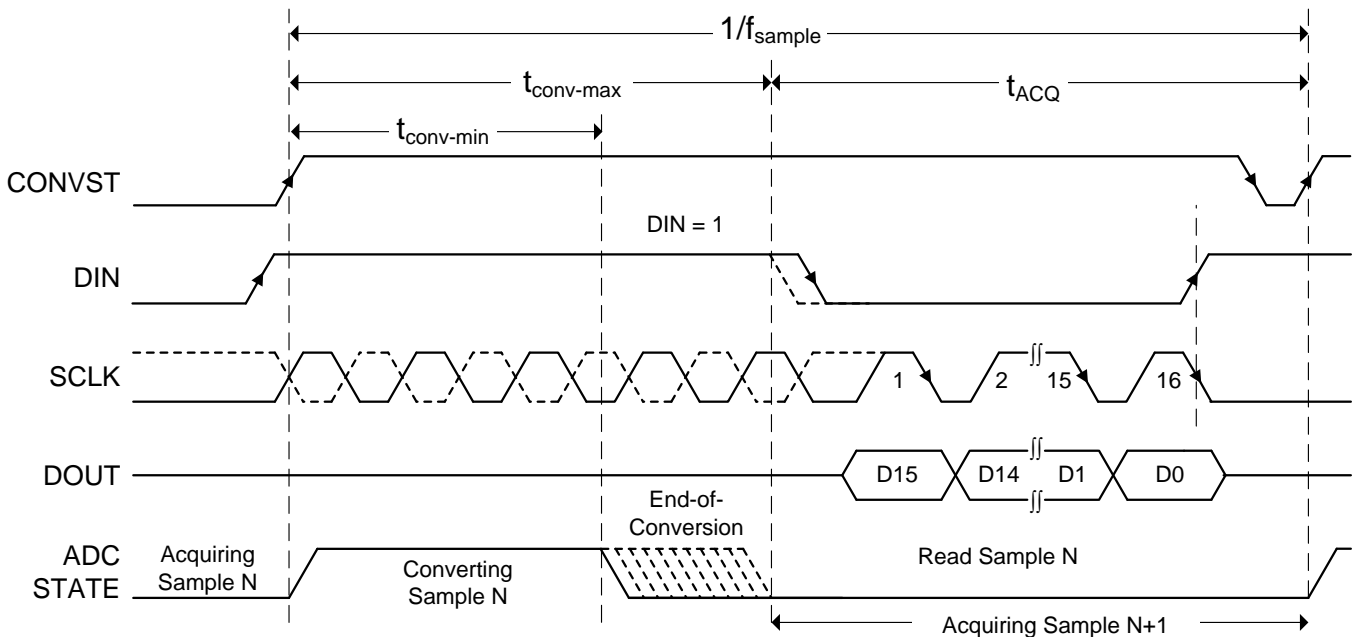


Figure 48. Interface Timing Diagram: Single ADC with 4-Wire  $\overline{CS}$  Mode

When conversion is complete, the device enters acquisition phase and powers down. DIN (functioning as  $\overline{CS}$ ) can be brought low after the maximum conversion time ( $t_{conv-max}$ ) elapses. On the DIN falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided  $t_{h\_CK\_DO}$  is acceptable). DOUT goes to 3-state after the 16th SCLK falling edge or when DIN goes high, whichever occurs first.

As shown in Figure 49, multiple devices can be hooked together on the same data bus. In this case, as shown in Figure 50, the DIN of the second device (functioning as CS for the second device) can go low after the first device data are read and the DOUT of the first device is in 3-state.

Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

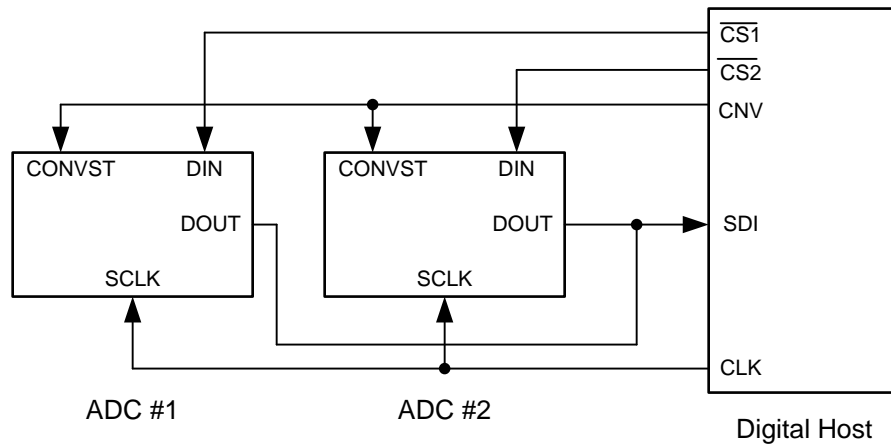


Figure 49. Connection Diagram: Two ADCs with 4-Wire  $\overline{CS}$  Mode

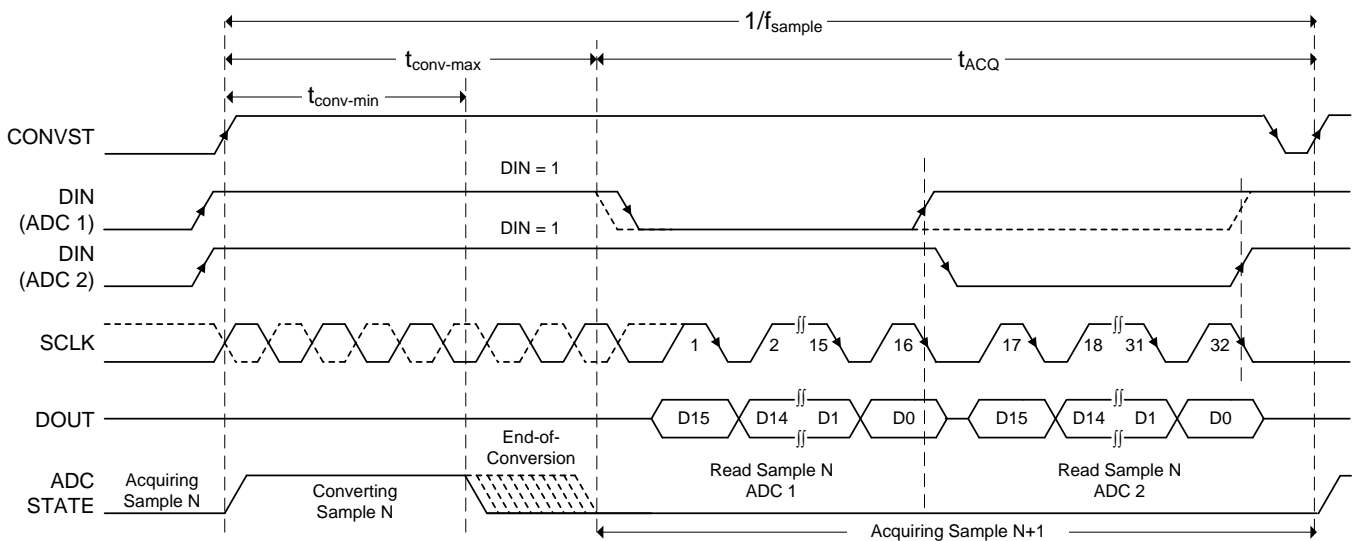


Figure 50. Interface Timing Diagram: Two ADCs with 4-Wire  $\overline{CS}$  Mode

## DAISY-CHAIN MODE

Daisy-chain mode is selected if DIN is low at the time of a CONVST rising edge or if DIN and CONVST are connected together. The following section discusses this interface option in detail.

### Daisy-Chain Mode

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability. Figure 51 shows a connection diagram with  $N$  ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 is connected to GND. The DOUT pin of ADC 1 is connected to the DIN pin of ADC 2, and so on. The DOUT pin of the last ADC in the chain (ADC  $N$ ) is connected to the SDI pin of the digital host.

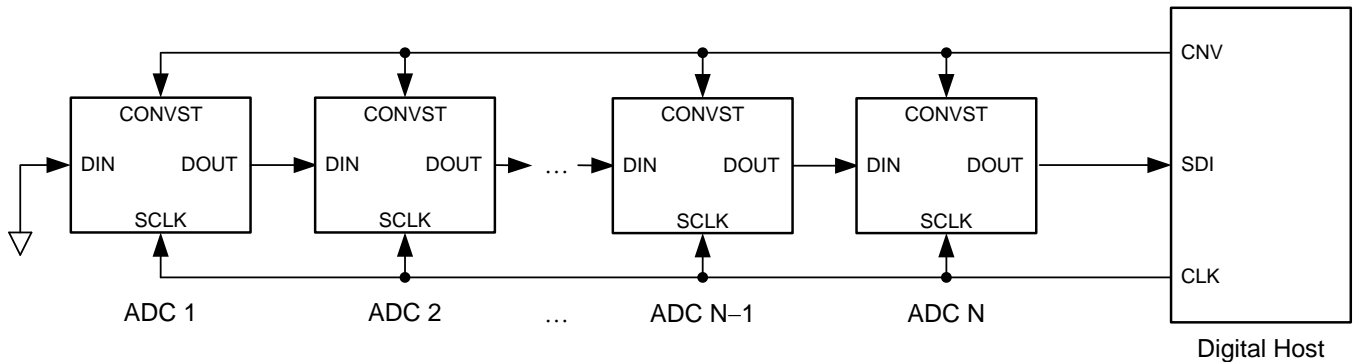


Figure 51. Connection Diagram: Daisy-Chain Mode (DIN = 0)

As shown in Figure 52, the device DOUT pin is driven low when DIN and CONVST are low together. With DIN low, a CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be low at the CONVST rising edge.

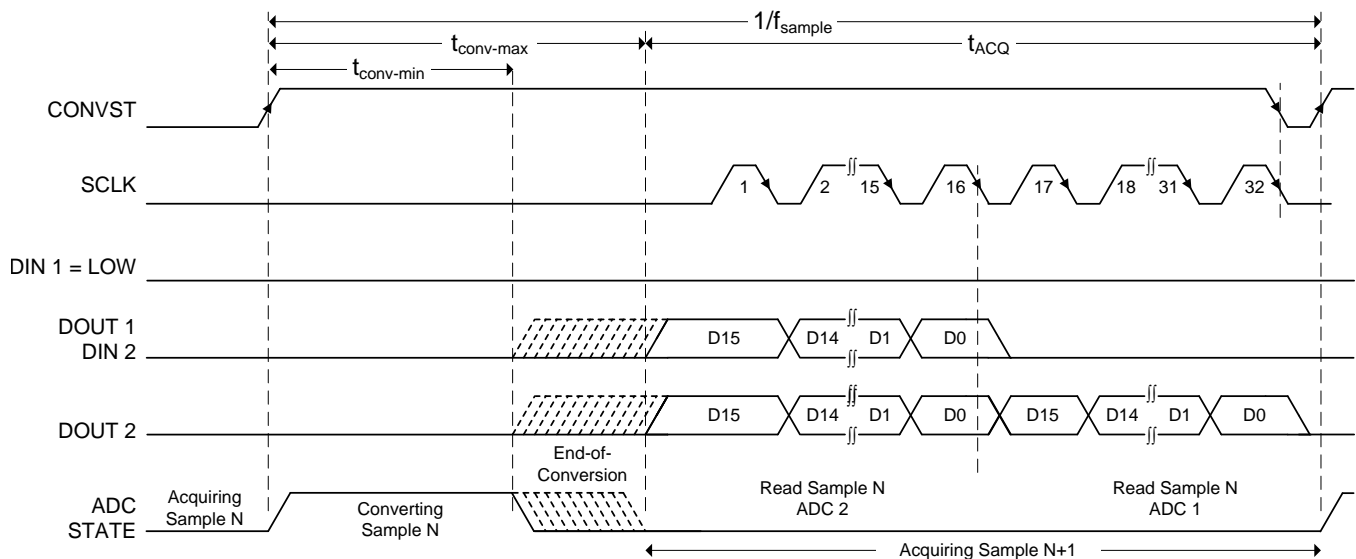


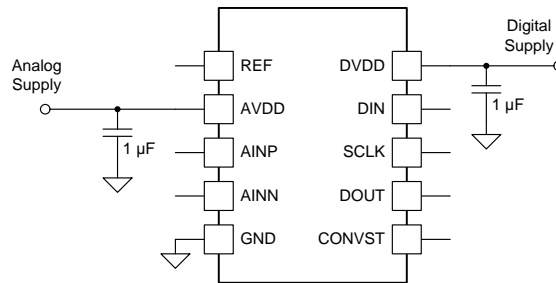
Figure 52. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 16-bit, shift register and also outputs the MSB bit of this conversion result on its own DOUT pin. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the data of ADC N, followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of  $16 \times N$  SCLK falling edges are required to capture the outputs of all  $N$  devices in the chain. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided  $t_{h\_CK\_DO}$  is acceptable).

## POWER SUPPLY

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

Decouple the AVDD and DVDD pins with GND, using individual 1- $\mu$ F decoupling capacitors placed in close proximity to the pin, as shown in [Figure 53](#).



**Figure 53. Supply Decoupling**

## POWER SAVING

The device has an auto power-down feature that powers down the internal circuitry at the end of every conversion. Referring to [Figure 54](#), the input signal is acquired on the sampling capacitors when the device is in a power-down state ( $t_{acq}$ ); at the same time, the result for the previous conversion is available for reading. The device powers up on the start of the next conversion. During conversion phase ( $t_{conv}$ ), the device also consumes current from the reference source (connected to pin REF).



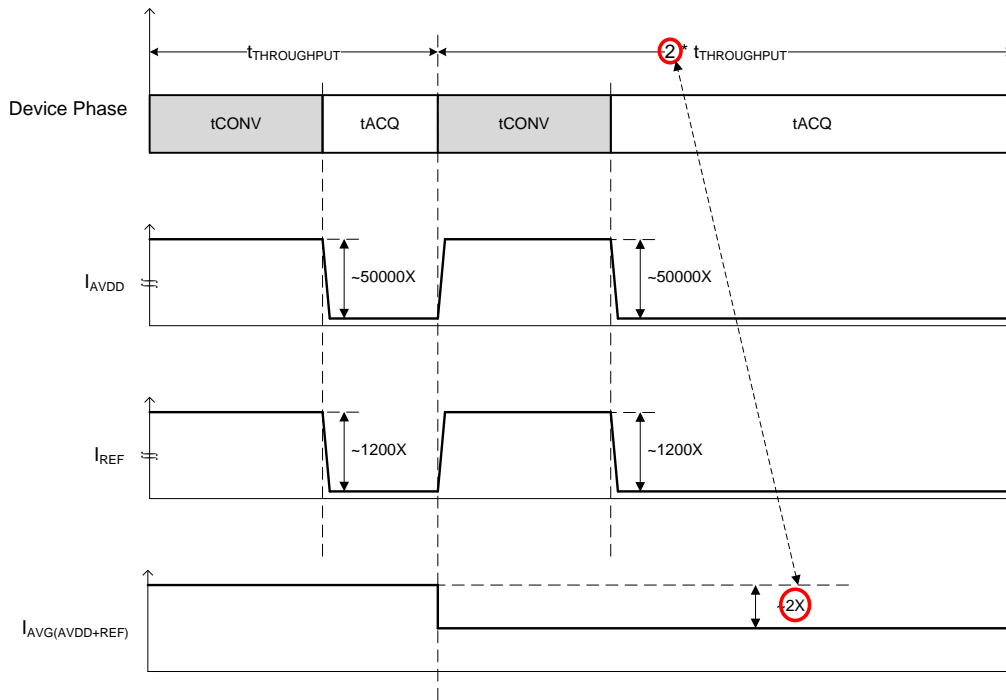


Figure 54. Power Scaling with Throughput

The conversion time,  $t_{conv}$ , is independent of the SCLK frequency. When operating the device at speeds lower than the maximum rated throughput, the conversion time,  $t_{conv}$ , does not change; the device spends more time in power-down state. Therefore, as shown in Figure 55, the device power consumption from the AVDD supply and the external reference source is directly proportional to the speed of operation. Extremely low AVDD power-down current (50 nA, typical) and extremely low external reference leakage current (250 nA, typical), make this device ideal for very low throughput applications (such as pulsed measurements).

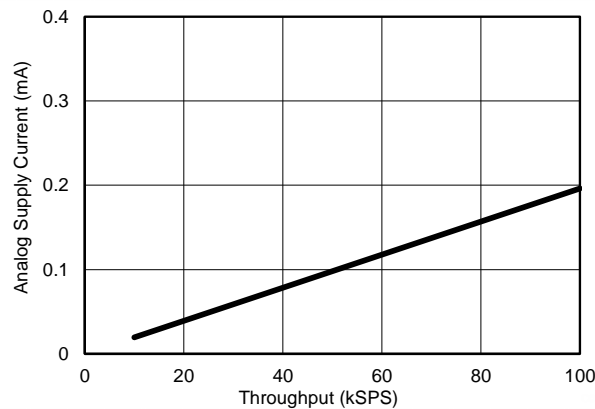


Figure 55. Power Scaling with Throughput

## APPLICATION INFORMATION

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by some application circuits designed using the ADS8867.

### ADC REFERENCE DRIVER

The external reference source to the ADS8867 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few 100  $\mu\text{V}_{\text{RMS}}$ . Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred Hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of  $V_{\text{REF}}$  stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor,  $C_{\text{BUF\_FLT}}$  (refer to Figure 43) for regulating the voltage at the reference input of the ADC. The amplifier selected to drive the reference pin should have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pin without any stability issues.

#### Reference Driver Circuit for $V_{\text{REF}} = 4.5 \text{ V}$

The application circuit in Figure 56 shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8867 at higher sampling rates up to 100 kSPS. The 4.5-V reference voltage in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

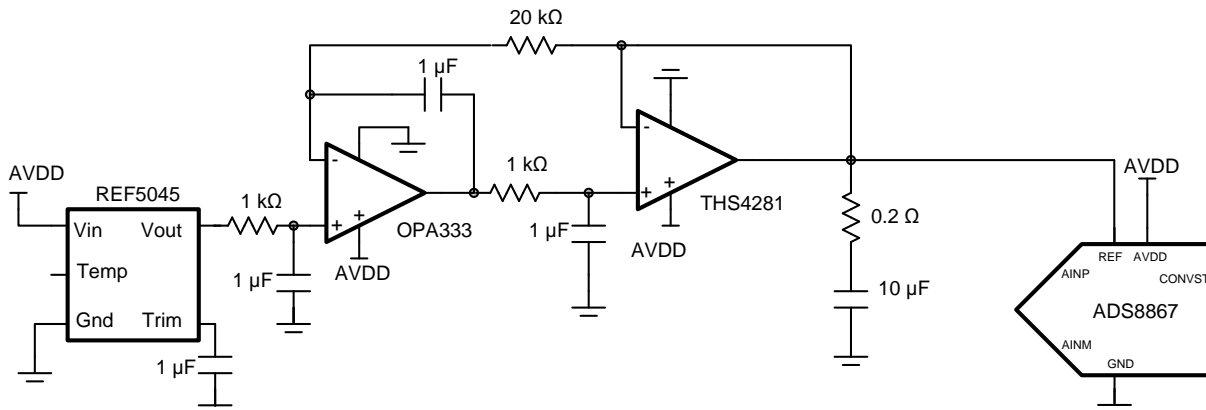


Figure 56. Schematic of Reference Driver Circuit with  $V_{\text{REF}} = 4.5 \text{ V}$

The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1  $\Omega$  at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit Data Acquisition \(DAQ\) Block Optimized for 1- \$\mu\text{s}\$  Full-Scale Step Response \(SLAU512\)](#).

### Reference Driver Circuit for $V_{REF} = 2.5\text{ V}$ in Ultralow Power, Lower Throughput Applications

The application circuit in [Figure 57](#)[Figure 58](#) shows the schematic of a complete reference driver circuit that generates a voltage of 2.5 V dc using a single 3.3-V supply. This ultralow power reference block is suitable to drive the ADS8867 for power-sensitive applications at a relatively lower throughput. This design uses the high-precision [REF3325](#) circuit that provides an accurate 2.5-V reference voltage at an extremely low quiescent current of 5  $\mu\text{A}$ . The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

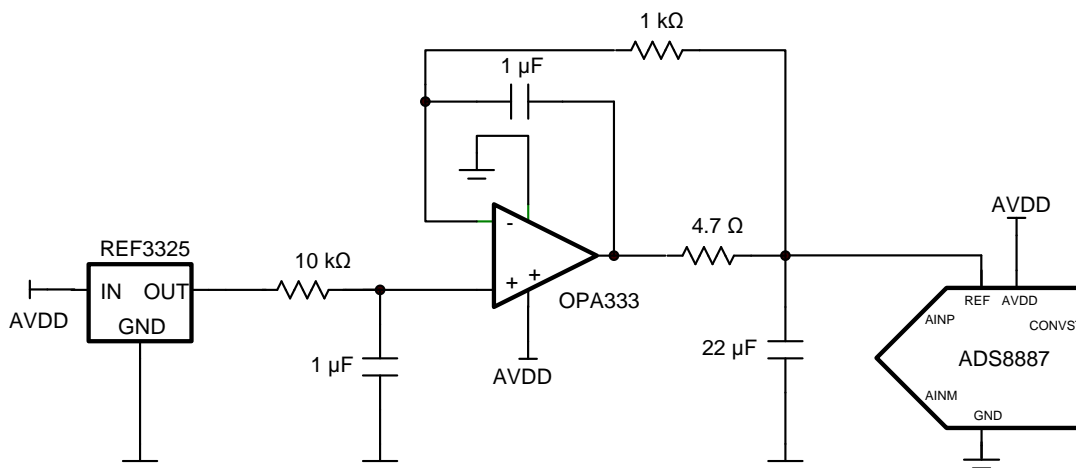


Figure 57. Schematic of Reference Driver Circuit with  $V_{REF} = 2.5\text{ V DC}$

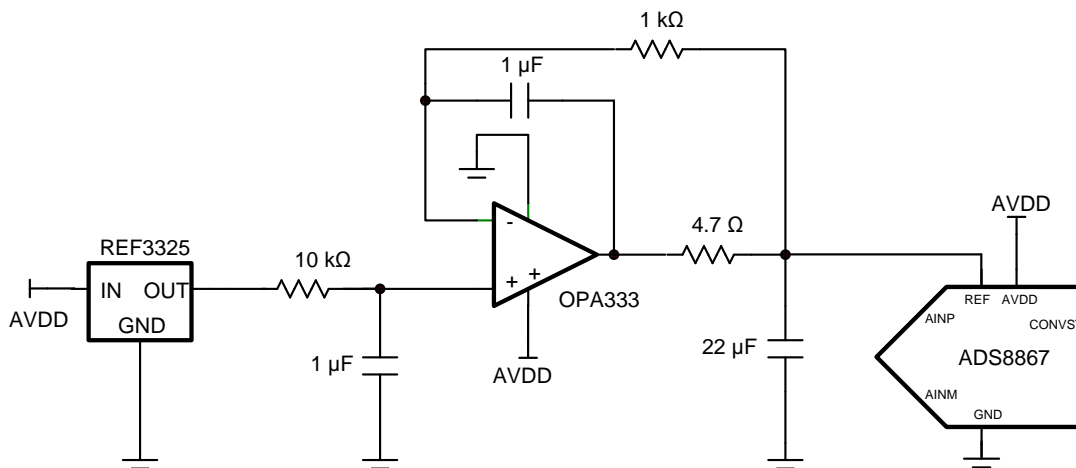


Figure 58. Schematic of Reference Driver Circuit with  $V_{REF} = 2.5\text{ V DC}$

The reference buffer is designed using the low-power [OPA333](#) that can operate from a 3.3-V supply at an extremely low quiescent current of 28  $\mu\text{A}$ . The wideband noise contribution from the amplifier is limited by a low-pass filter of a cutoff frequency equal to 1.5 kHz, formed by a 4.7- $\Omega$  resistor in combination with a 22- $\mu\text{F}$  capacitor. The 4.7- $\Omega$  series resistor creates an additional drop in the reference voltage, which is corrected by a dual-feedback configuration.



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit, 10kSPS Data Acquisition \(DAQ\) Block Optimized for Ultra Low Power < 1mW \(SLAU514\)](#).

## ADC INPUT DRIVER

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 16-bit ADC such as the ADS8867.

### Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (refer to the [Antialiasing Filter](#) section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in [Equation 2](#):

$$\text{Unity - Gain Bandwidth} \geq 4 \times \left( \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (2)$$

- **Noise.** Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in [Equation 3](#).

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{\left( \frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu V_{RMS}$ ,
- $e_{n\_RMS}$  is the amplifier broadband noise density in  $nV/\sqrt{Hz}$ ,
- $f_{-3dB}$  is the 3-dB bandwidth of the RC filter, and
- $N_G$  is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (3)
- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in [Equation 4](#).

$$THD_{AMP} \leq THD_{ADC} - 10 \text{ (dB)} \quad (4)$$

- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within a 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 16-bit accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

## Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the inputs of the ADC during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A differential capacitor,  $C_{FLT}$ , is connected across the inputs of the ADC (as shown in Figure 59). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For the ADS8867, the input sampling capacitance is equal to 59 pF, thus the value of  $C_{FLT}$  should be greater than 590 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

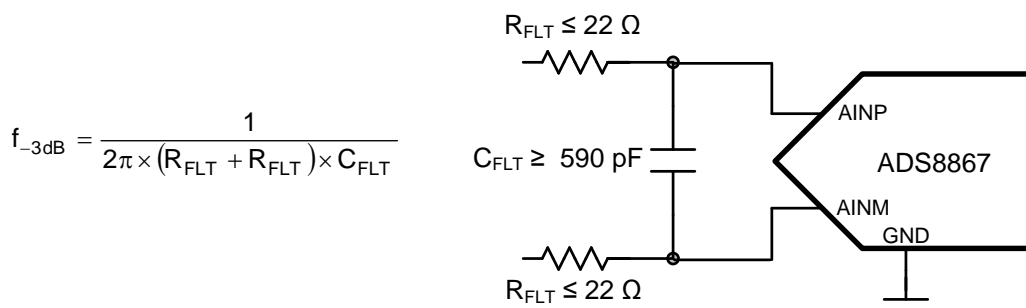


Figure 59. Antialiasing Filter

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{FLT}$ ) are used at the output of the amplifiers. A higher value of  $R_{FLT}$  is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{FLT}$  requires balancing the stability and distortion of the design. For the ADS8867, TI recommends limiting the value of  $R_{FLT}$  to a maximum of 22  $\Omega$  in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22- $\Omega$  resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

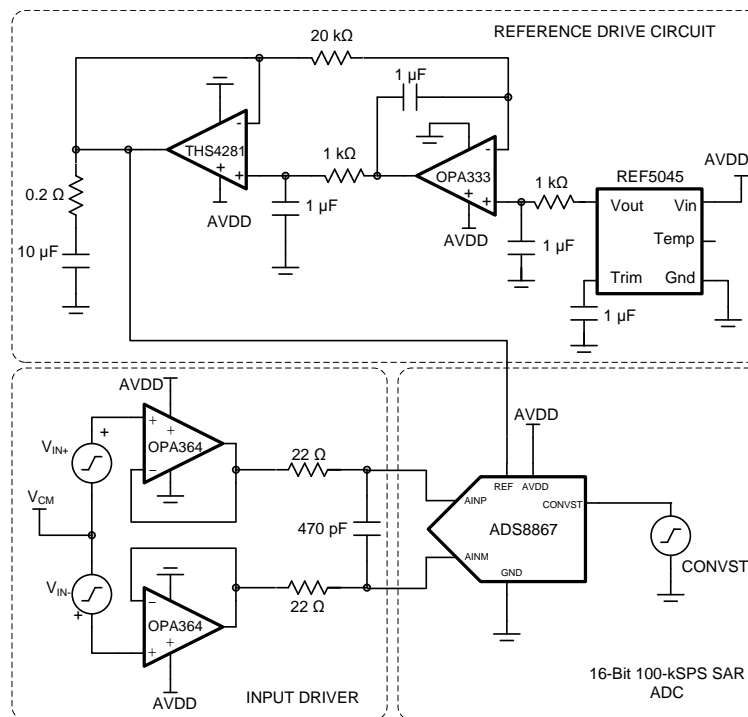
## APPLICATION CIRCUIT EXAMPLES

This section describes some common application circuits using the ADS8867. These data acquisition (DAQ) blocks are optimized for specific input types and performance requirements of the system. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; refer to the [Power Supply](#) section for suggested guidelines.

### DAQ Circuit for a 10- $\mu$ s, Full-Scale Step Response

The application circuit shown in [Figure 60](#) is optimized for using the ADS8867 at the maximum-specified throughput of 100 kSPS for a full-scale step input voltage. Such step input signals are common in multiplexed applications when switching between different channels. In a worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched.

In such applications, the primary design requirement is to ensure that the full-scale step input signal settles to 16-bit accuracy at the ADC inputs. This condition is critical to achieve the excellent linearity specifications of the ADC. Therefore, the bandwidth of the antialiasing RC filter should be large enough to allow optimal settling of the input signal during the ADC acquisition time. The filter capacitor helps reduce the sampling charge injection at the ADC inputs, but degrades the phase margin of the driving amplifier, thereby leading to stability issues. Amplifier stability is maintained by the series isolation resistor. Therefore, the component values of the antialiasing filter should be carefully selected to meet the settling requirements of the system as well as to maintain the stability of the input driving amplifiers.



**Figure 60. DAQ Circuit for 10- $\mu$ s, Full-Scale Step Response**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit Data Acquisition \(DAQ\) Block Optimized for 1- \$\mu\$ s Full-Scale Step Response \(SLAU512\)](#).

### Low-Power DAQ Circuit for Excellent Dynamic Performance at 100 kSPS

The application circuit shown in Figure 61 is optimized for using the ADS8867 at the maximum specified throughput of 100 kSPS for a full-scale sinusoidal signal of 1-kHz frequency. This circuit achieves excellent dynamic performance for the lowest power consumption. The differential ac input signal is processed through low-noise and low-power amplifiers configured as unity-gain buffers and a low-pass, RC filter before being fed into the ADC.

In such applications, the input driver must be low in power and noise as well as able to support rail-to-rail input and output swing with a single supply. A high amplifier bandwidth is also preferred to help attenuate high-frequency distortion. However, oftentimes bandwidth and noise are traded off with the power consumption of the amplifier. This circuit uses the OPA313 as the front-end driving amplifier because this device offers relatively low noise density at ultra-low quiescent currents of 50  $\mu$ A per channel.

The noise contribution from the front-end amplifier is band-limited by the 3-dB bandwidth of the RC filter, which is designed to be 30 kHz in this application. To maintain good phase margin,  $R_{FLT}$  is selected as 47  $\Omega$  instead of the 22- $\Omega$  recommended maximum. The result is a slight degradation in linearity, which is a common tradeoff for very low-power applications.

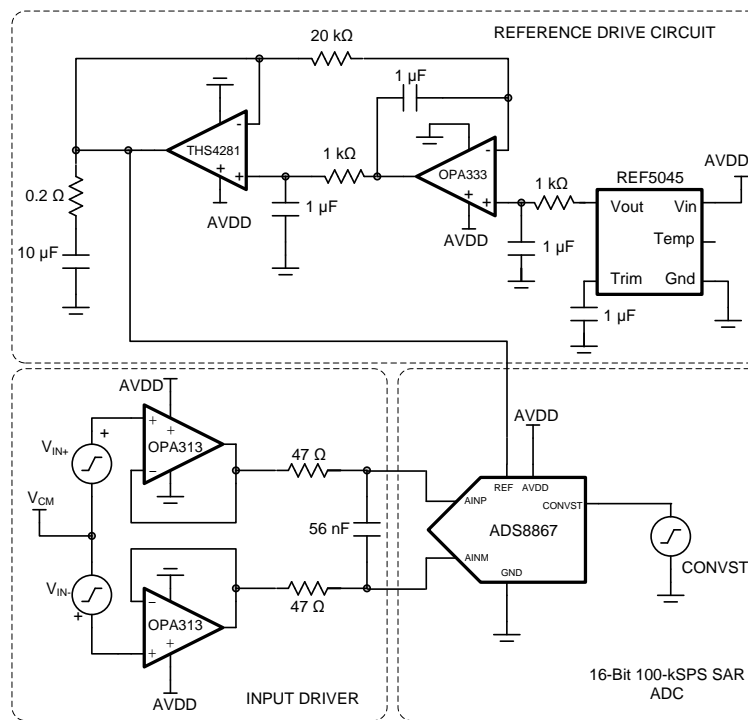


Figure 61. DAQ Circuit for Lowest Power and Excellent Dynamic Performance at 100 kSPS



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit, 1-MSPS Data Acquisition \(DAQ\) Block Optimized for Lowest Power \(SLAU513\)](#).

## DAQ Circuit for Lowest Distortion and Noise Performance at 100 kSPS

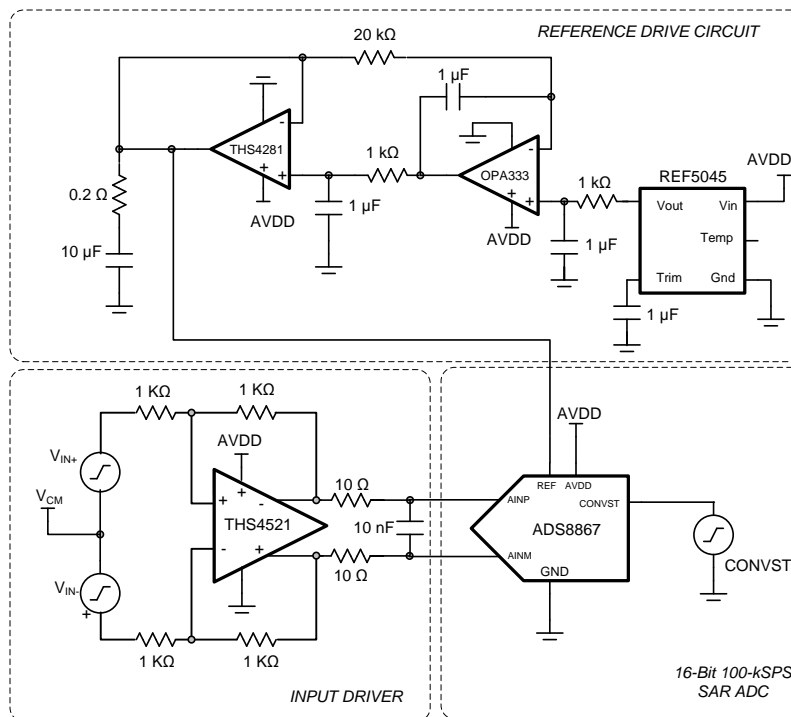
This section describes two application circuits (Figure 62 and Figure 63) that are optimized for using the ADS8867 with lowest distortion and noise performance at a throughput of 100 kSPS. In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in an inverting gain configuration and a low-pass RC filter before being fed into the ADC.

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power THS4521 as an input driver, which provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

### Differential Input Configuration

The circuit in Figure 62 shows a fully-differential DAQ block optimized for low distortion and noise using the THS4521 and ADS8867. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4521 (not shown in Figure 62). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider. However, note that the ADS8867 allows the common-mode input voltage ( $V_{CM}$ ) to be set to any value in the range of 0 V to  $V_{REF}$ .



**Figure 62. Differential Input DAQ Circuit for Lowest Distortion and Noise at 100 kSPS**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit, 1-MSPS Data Acquisition \(DAQ\) Block Optimized for Lowest Distortion and Noise \(SLAU515\)](#).



### Single-Ended to Differential Configuration

The circuit in [Figure 63](#) shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4521 and the ADS8867. This front-end circuit configuration requires a single-ended ac signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4521 (not shown in [Figure 63](#)). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider. However, note that the ADS8867 allows the common-mode input voltage ( $V_{CM}$ ) to be set to any value in the range of 0 V to  $V_{REF}$ .

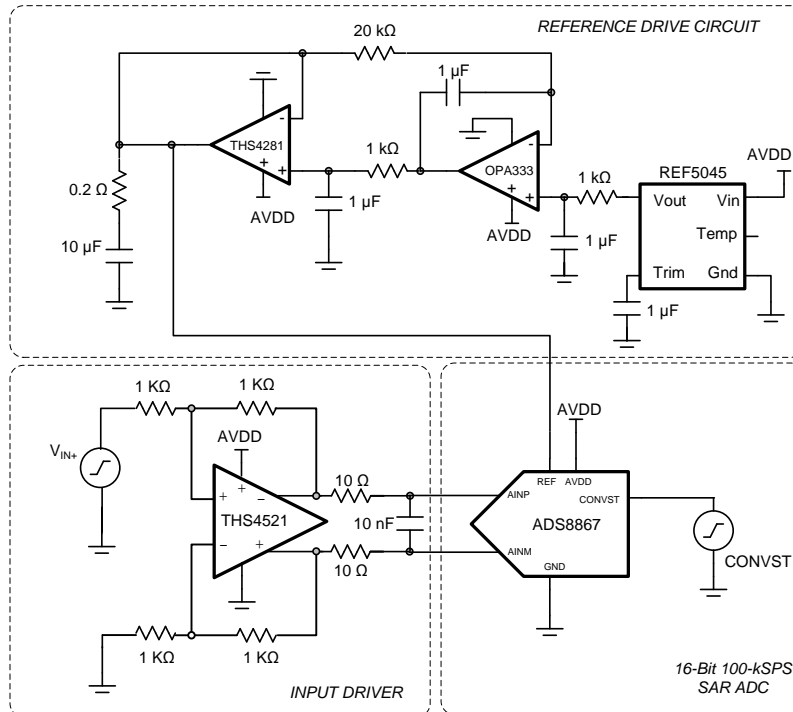
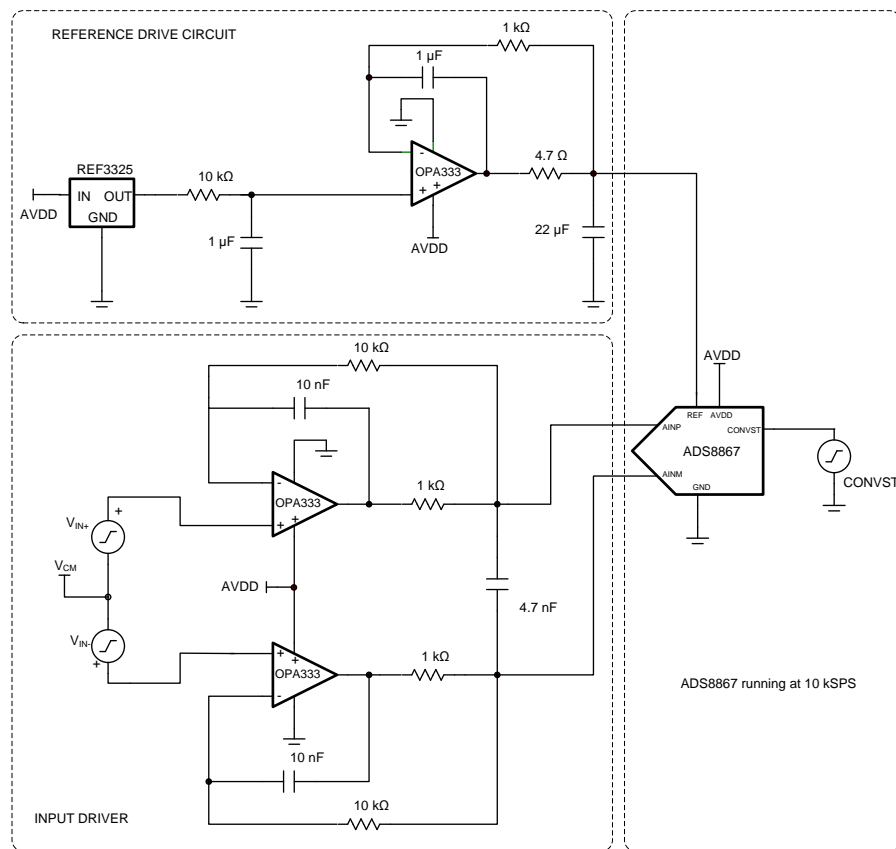


Figure 63. Single-Ended to Differential DAQ Circuit for Lowest Distortion and Noise at 100 kSPS

### Ultralow-Power DAQ Circuit at 10 kSPS

The data acquisition DAQ circuit shown in Figure 64 is optimized for using the ADS8867 at a reduced throughput of 10 kSPS with ultralow-power consumption (< 1 mW) targeted at portable and battery-powered applications.

In order to save power, this circuit is operated on a single 3.3-V supply. The circuit uses extremely low-power, dual amplifiers (such as the OPA2333) with a maximum quiescent current of 28  $\mu$ A per channel to drive the ADC inputs. The input amplifiers are configured in a modified unity-gain buffer configuration. The filter capacitor at the ADC inputs attenuates the sampling charge-injection noise from the ADC but effects the stability of the input amplifiers by degrading the phase margin. This attenuation requires a series isolation resistor to maintain amplifier stability. The value of the series resistor is directly proportional to the open-loop output impedance of the driving amplifier to maintain stability, which is high (in the order of k $\Omega$ ) in the case of low-power amplifiers such as the OPA333. Therefore, a high value of 1 k $\Omega$  is selected for the series resistor at the ADC inputs. However, this series resistor creates an additional voltage drop in the signal path, thereby leading to linearity and distortion issues. The dual-feedback configuration used in Figure 64 corrects for this additional voltage drop and maintains system performance at ultralow-power consumption.



**Figure 64. Ultralow-Power DAQ Circuit at 10 kSPS**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to [18-Bit, 10kSPS Data Acquisition \(DAQ\) Block Optimized for Ultra Low Power < 1mW \(SLAU514\)](#).

## 修订历史记录

请注意：前一修订版的页码可能与当前版本的页码不同。

<b>Changes from Original (May 2013) to Revision A</b>	<b>Page</b>
• Changed 宽共模电压范围特性要点 .....	1
• Changed 特性要点中交流和直流性能 分项 .....	1
• Changed 满量程阶跃稳定 特性要点 .....	1
• Deleted 最后两个应用要点 .....	1
• Changed 说明 部分 .....	1
• Changed 首页图 .....	1
• Added Family Information, Absolute Maximum Ratings, and Thermal Information tables .....	2
• Added Electrical Characteristics table .....	3
• Added <i>Timing Characteristics</i> section .....	5
• Added <i>Pin Configurations</i> section .....	9
• Added <i>Typical Characteristics</i> section .....	10
• Added <i>Overview</i> section .....	16
• Added <i>Application Information</i> section .....	26

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8867IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8867	<a href="#">Samples</a>
ADS8867IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8867	<a href="#">Samples</a>
ADS8867IDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8867	<a href="#">Samples</a>
ADS8867IDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8867	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8867IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8867IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8867IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

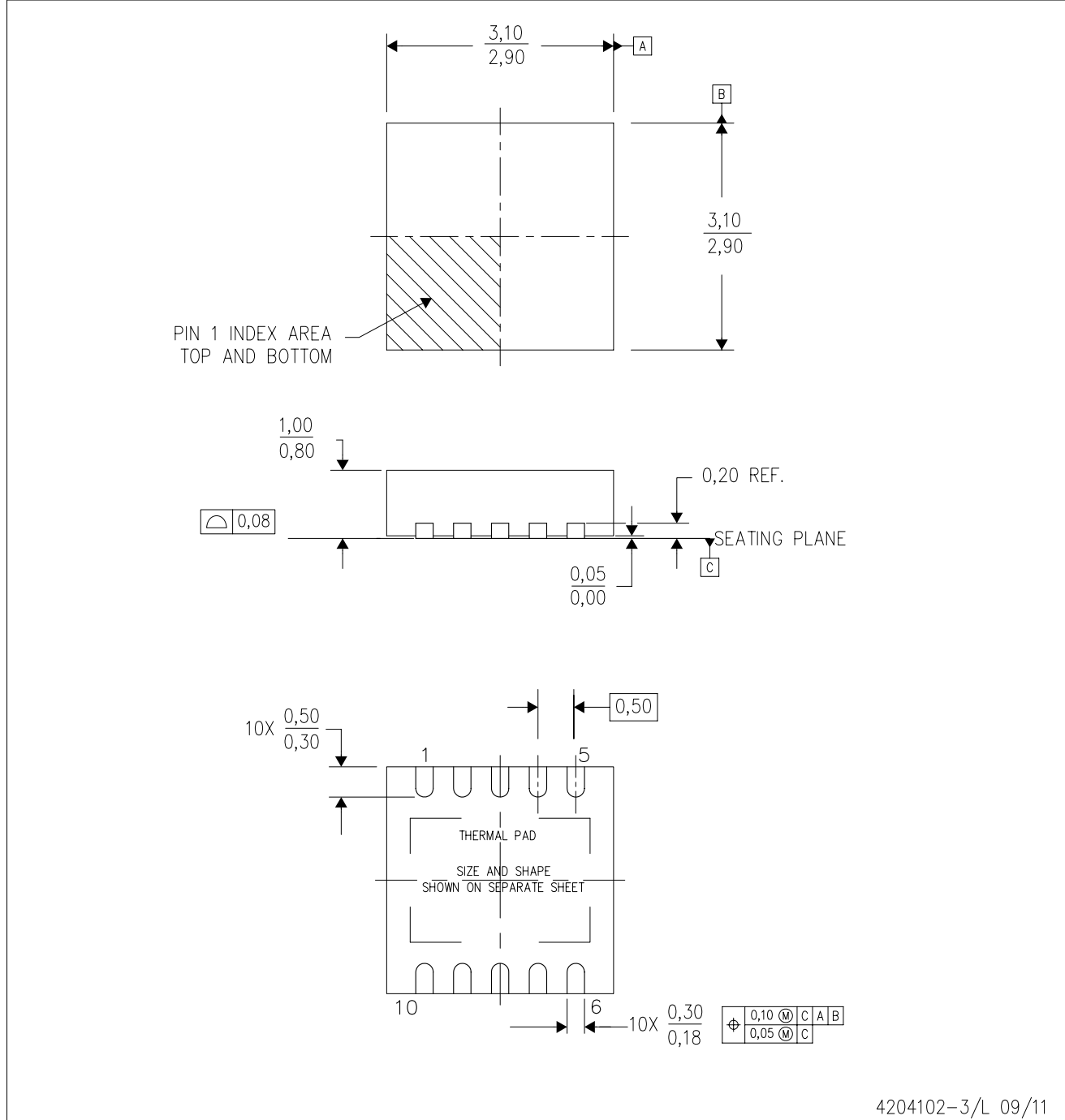
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8867IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8867IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8867IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/L 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present



# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

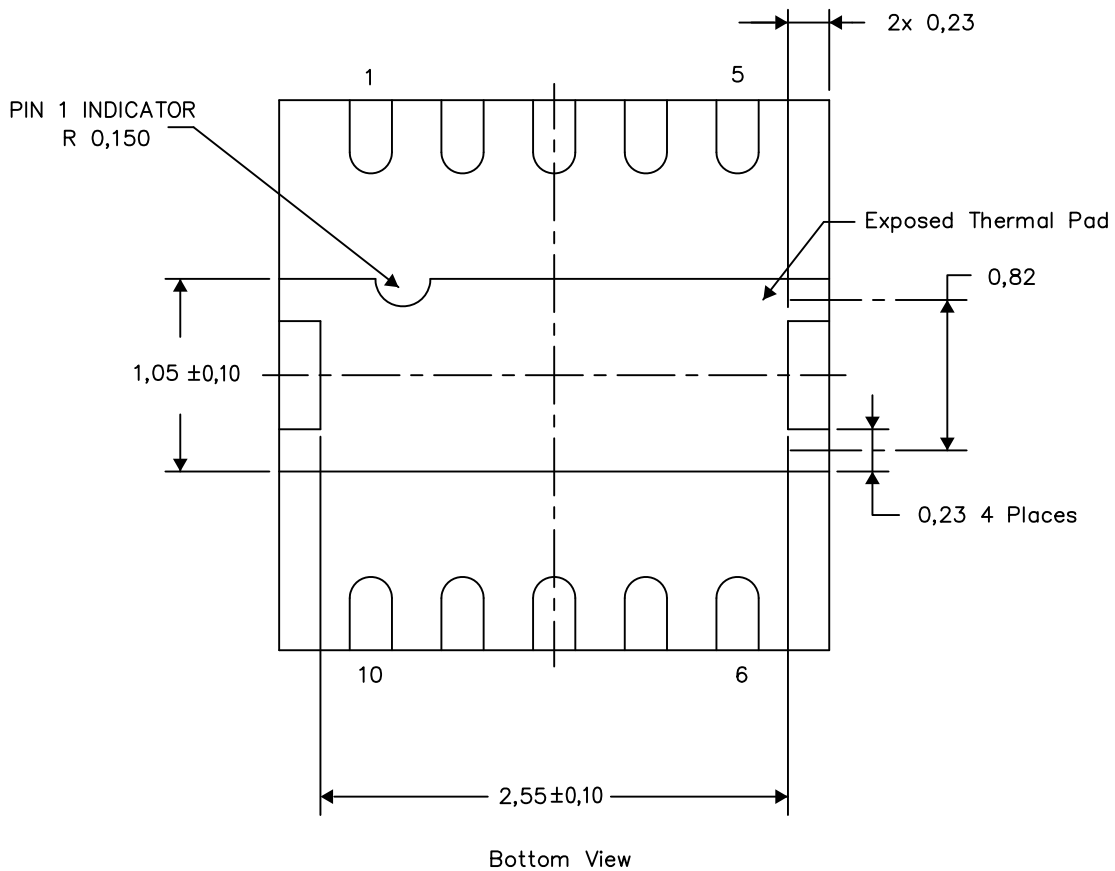
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



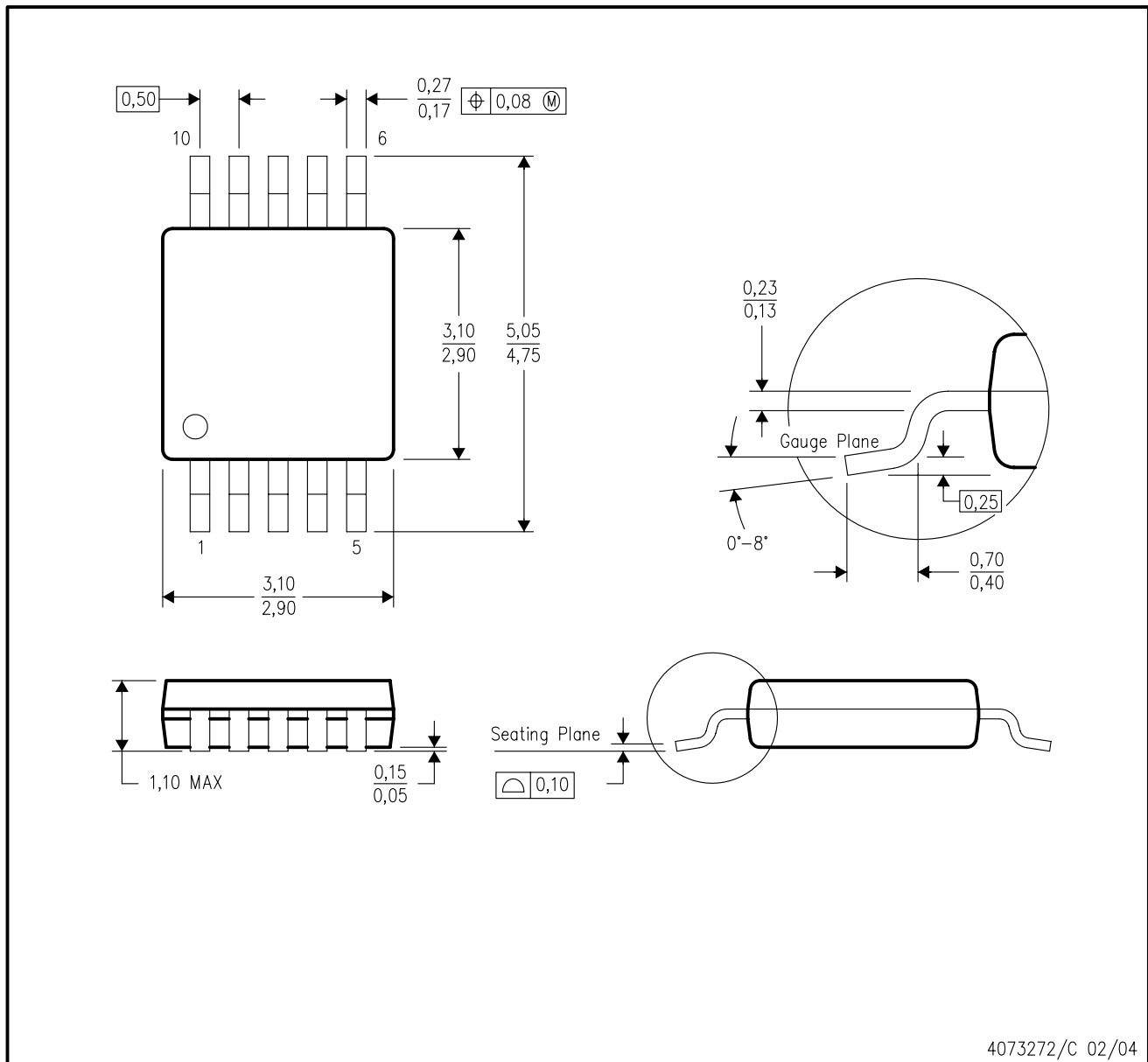
Exposed Thermal Pad Dimensions

4206565-6/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DGS (S-PDSO-G10)

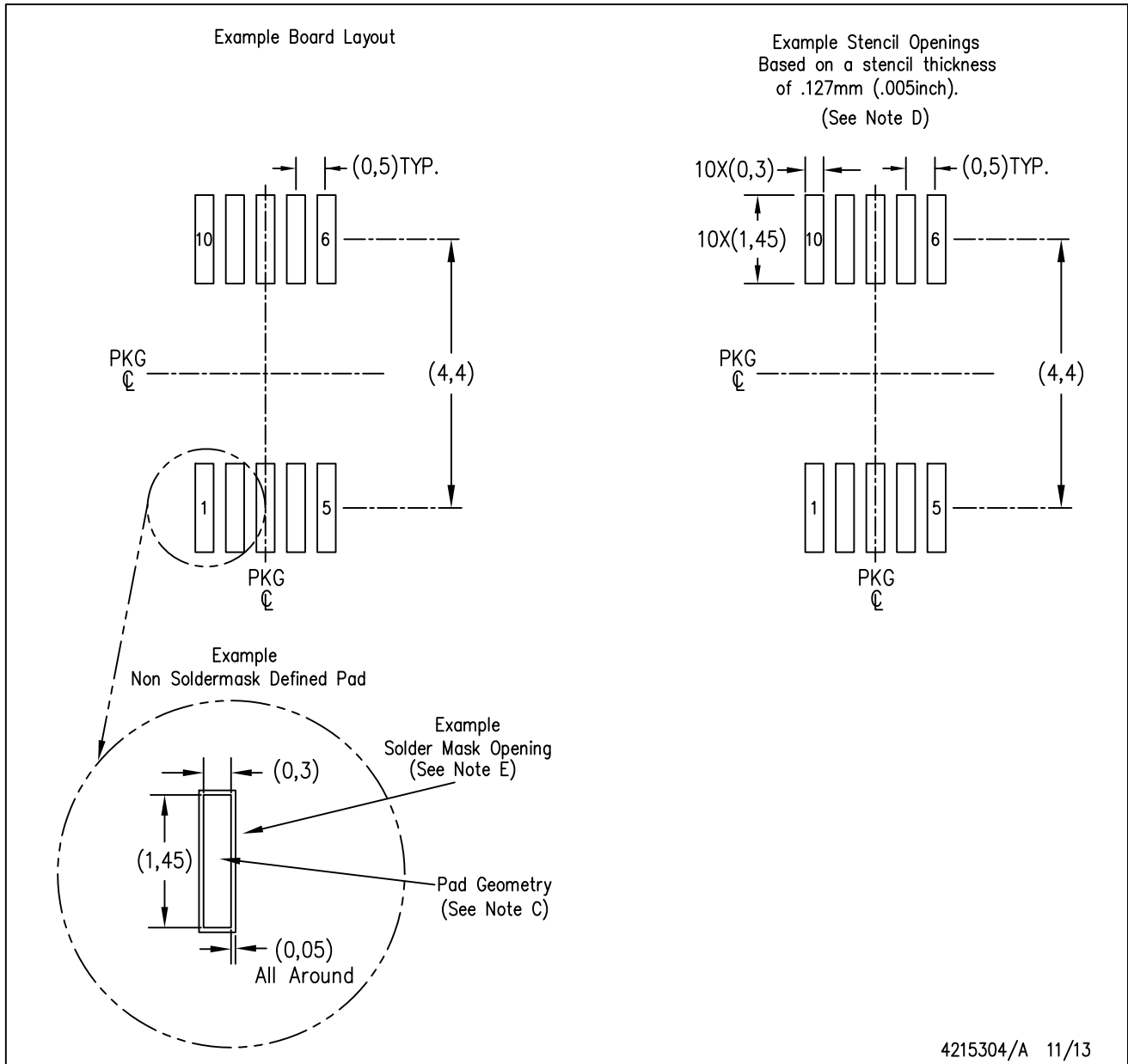
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与美国 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2017 德州仪器半导体技术（上海）有限公司