

# ADS8881x 18 位、1MSPS、串行接口、低功耗、微型、真正差分输入、逐次逼近寄存器 (SAR) 模数转换器

## 1 特性

- 采样速率: 1MHz
- 无延迟输出
- 单极, 真正的差分输入范围:  $-V_{REF}$  至  $+V_{REF}$
- 宽共模电压范围: 0V 至  $V_{REF}$  (共模抑制比 (CMRR) 最小值为 90dB)
- SPI™ 兼容串行接口, 此接口具有菊花链选项
- 出色的交流和直流性能:
  - ADS8881C: 积分非线性 (INL):  $\pm 1$  LSB (典型值),  $\pm 2.0$  LSB (最大值) 微分非线性 (DNL):  $\pm 1.0$  LSB (最大值), 18 位无丢码 (NMC) 信噪比 (SNR): 100dB, 总谐波失真 (THD):  $-115$ dB
  - ADS8881I: INL:  $\pm 1.5$  LSB (典型值),  $\pm 3.0$  LSB (最大值) DNL:  $\pm 1.5$  和  $-1$  LSB (最大值), 18 位 NMC SNR: 100dB, THD:  $-115$ dB
- 宽工作电压范围:
  - AVDD: 2.7V 至 3.6V
  - DVDD: 2.7V 至 3.6V (与 AVDD 无关)
  - REF: 2.5V 至 5V (与 AVDD 无关)
  - 工作温度: ADS8881C:  $0^{\circ}\text{C}$  至  $+70^{\circ}\text{C}$  ADS8881I:  $-40^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$
- 低功耗耗散:
  - 1MSPS 时为 5.5mW
  - 100kSPS 时为 0.55mW
  - 10kSPS 时为 55 $\mu$ W
- 断电电流 (AVDD): 50nA

- 满量程阶跃稳定至 18 位: 290ns
- 封装: MSOP-10 和 VSON-10

## 2 应用

- 自动测试设备 (ATE)
- 仪表和处理卡
- 精密医疗设备
- 低功耗、电池供电类仪器

## 3 说明

ADS8881 是一款 18 位, 1MSPS, 真差分输入, 模数转换器 (ADC)。此器件以 2.5V 至 5V 的外部基准运行, 从而在无需额外的信号调节情况下提供宽信号范围。此基准电压设置独立于, 并且可超过, 模拟电源电压 (AVDD)。

该器件提供一个兼容的 SPI 串口。该串口也支持菊花链操作以实现多个器件级联。一个可选的繁忙指示器位可轻松实现与数字主机的同步。

该器件支持单极真正差分模拟输入信号, 差分输入摆幅为  $-V_{REF}$  至  $V_{REF}$ 。这一真正的差分模拟输入结构可使共模电压达到 0V 至  $V_{REF}$  范围内的任意值 (当两路输入均在  $-0.1\text{V}$  至  $V_{REF} + 0.1\text{V}$  的输入工作电压范围内)。

器件运行针对极低功耗运行进行了优化。功耗直接与速度成比例。该特性使得 ADS8881 非常适合低速应用。

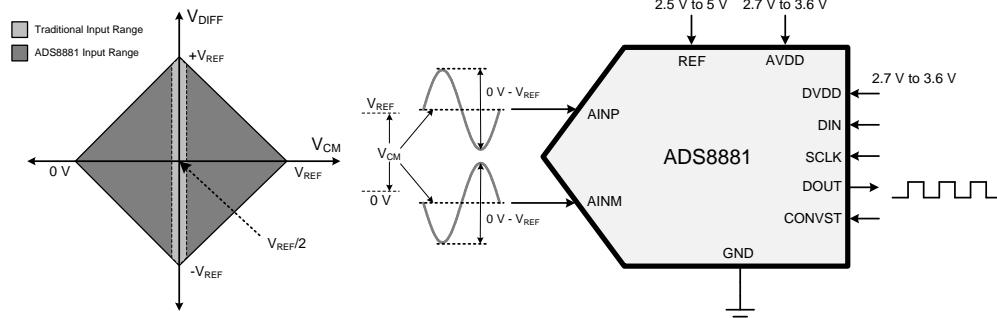
器件信息<sup>(1)</sup>

产品型号	封装	封装尺寸 (标称值)
ADS8881x	VSSOP (10)	3.00mm x 3.00mm
	VSON (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。



真正的差分输入范围



## 目录

1	特性 .....	1	9.2	Functional Block Diagram .....	21
2	应用 .....	1	9.3	Feature Description .....	21
3	说明 .....	1	9.4	Device Functional Modes .....	24
4	修订历史记录 .....	3	<b>10</b>	<b>Application and Implementation .....</b>	<b>33</b>
5	推荐的器件和设计 .....	5	10.1	Application Information .....	33
6	<b>Pin Configurations and Functions .....</b>	<b>6</b>	10.2	Typical Applications .....	36
7	<b>Specifications .....</b>	<b>7</b>	<b>11</b>	<b>Power-Supply Recommendations .....</b>	<b>45</b>
7.1	Absolute Maximum Ratings .....	7	11.1	Power-Supply Decoupling .....	45
7.2	ESD Ratings .....	7	11.2	Power Saving .....	45
7.3	Recommended Operating Conditions .....	7	<b>12</b>	<b>Layout .....</b>	<b>47</b>
7.4	Thermal Information .....	7	12.1	Layout Guidelines .....	47
7.5	Electrical Characteristics .....	8	12.2	Layout Example .....	47
7.6	Timing Requirements: 3-Wire Operation .....	10	<b>13</b>	<b>器件和文档支持 .....</b>	<b>48</b>
7.7	Timing Requirements: 4-Wire Operation .....	11	13.1	文档支持 .....	48
7.8	Timing Requirements: Daisy-Chain .....	12	13.2	相关链接 .....	48
7.9	Typical Characteristics .....	13	13.3	社区资源 .....	48
<b>8</b>	<b>Parametric Measurement Information .....</b>	<b>20</b>	13.4	商标 .....	48
8.1	Equivalent Circuits .....	20	13.5	静电放电警告 .....	49
<b>9</b>	<b>Detailed Description .....</b>	<b>21</b>	13.6	Glossary .....	49
9.1	Overview .....	21	<b>14</b>	<b>机械、封装和可订购信息 .....</b>	<b>49</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (July 2014) to Revision D	Page
• 已添加推荐器件和设计部分 .....	5
• 已更改器件比较表的标题并移至推荐器件和设计部分 .....	5
• Changed ESD Ratings table to current standards, added HBM and CDM data .....	7
• Added timing specifications for different operating temperature ranges for the $t_{conv}$ , $t_{d-CK-DO}$ , and $t_{quiet}$ parameters in the <i>Timing Requirements: 3-Wire Operation</i> table .....	10
• Added timing specifications for different operating temperature ranges for the $t_{conv}$ parameter in <i>Timing Requirements: 4-Wire Operation</i> table .....	11
• Added timing specifications for different operating temperature ranges for the $t_{conv}$ parameter in <i>Timing Requirements: Daisy-Chain</i> table .....	12
• 添加了社区资源部分 .....	48

---

**Changes from Revision B (December 2014) to Revision C** **Page**


---

• 已更改格式以符合最新的数据表标准；已添加新内容并移动现有部分 .....	1
• 已更改 ADS8881 至 ADS8881C 并添加 ADS8881I .....	1
• 已将 ADS8881C 和 ADS8881I 的技术规格分为两项列出（出色的交流和直流性能 特性 要点中） .....	1
• 已更改器件信息表以符合最新标准 .....	1
• 已更新系列信息表并更改脚注 .....	5
• Added Recommended Operating Conditions table .....	7
• Changed LSB footnote to include how to convert LSB to ppm .....	8
• Changed $f_{SCLK}$ parameter maximum specification from 66.6 MHz to 70 MHz in Timing Requirements: 3-Wire Operation table. ....	10
• Changed $t_{SCLK}$ parameter minimum specification from 15 ns to 14.3 ns in Timing Requirements: 3-Wire Operation table. ....	10
• Added more information about validity of data on SCLK edges in all interface modes .....	25
• Changed diagrams and text for better explanation of the daisy-chain feature in the <i>Daisy-Chain Mode</i> section .....	30
• Changed <a href="#">Equation 2</a> and <a href="#">Equation 3</a> .....	34
• Added <i>Layout Guidelines</i> section .....	47

---

**Changes from Revision A (July 2013) to Revision B** **Page**


---

• 已更改 宽共模电压范围 特性 要点) .....	1
• 已添加注 2 至系列信息表 .....	5
• Changed External Reference Input, <i>Reference input current</i> parameter typical specification from 350 to 300 .....	8
• Added External Reference Input, <i>Reference leakage current</i> parameter to Electrical Characteristics .....	8
• Changed Power-Supply Requirements, <i>Power-supply voltage</i> parameter digital interface supply range as a function of SCLK in Electrical Characteristics .....	9
• Added Digital Inputs, <i>Digital input leakage current</i> parameter to Electrical Characteristics .....	9
• Added true-differential input feature details to <i>Analog Input</i> section .....	22
• Deleted shading from <a href="#">Figure 64</a> .....	35
• Deleted shading from <a href="#">Figure 65</a> .....	36
• Deleted shading from <a href="#">Figure 67</a> .....	38
• Deleted shading from <a href="#">Figure 69</a> .....	40
• Deleted shading from <a href="#">Figure 70</a> .....	40
• Deleted shading from <a href="#">Figure 72</a> .....	43
• Added power scaling with throughput feature details to <i>Power Saving</i> section .....	45

---

**Changes from Original (May 2013) to Revision A** **Page**


---

• 已更改 文档状态至“量产数据”；通篇进行 pre-RTM 修改 .....	1
---	---

---

## 5 推荐的器件和设计

**表 1. 器件比较**

吞吐量	18 位, 真正差分	16 位, 单端	16 位, 真正差分
100kSPS	<a href="#">ADS8887</a>	<a href="#">ADS8866</a>	<a href="#">ADS8867</a>
250kSPS	—	<a href="#">ADS8339<sup>(1)</sup></a>	—
400kSPS	<a href="#">ADS8885</a>	<a href="#">ADS8864</a>	<a href="#">ADS8865</a>
500kSPS	—	<a href="#">ADS8319<sup>(1)</sup></a>	<a href="#">ADS8318<sup>(1)(2)</sup></a>
680kSPS	<a href="#">ADS8883</a>	<a href="#">ADS8862</a>	<a href="#">ADS8863</a>
1MSPS	<a href="#">ADS8881</a>	<a href="#">ADS8860</a>	<a href="#">ADS8861</a>

(1) 引脚兼容器件 (AVDD = 5V)。

(2) 符合完全差分输入的相关标准。

**表 2. 配套器件**

器件	说明
<b>精密放大器</b>	
<b>低功耗放大器</b>	
<a href="#">OPA313</a>	1MHz 低功耗、低噪声、轨到轨 I/O 1.8V 运算放大器
<a href="#">OPA333</a>	1.8V、17 $\mu$ A、低功耗、高精度、零漂移 CMOS 运算放大器
<b>低失真放大器</b>	
<a href="#">OPA625</a>	具有功率调节功能的高带宽、高精度、低噪声且失真较低的放大器 SAR ADC 驱动器
<a href="#">OPA350</a>	MicroAmplifier™ 系列高速、单电源、轨到轨运算放大器
<a href="#">OPA320</a>	高精度 20MHz 0.9pA Ib、RRIO CMOS 运算放大器
<a href="#">THS4521</a>	超低功耗、轨到轨输出、完全差分放大器
<b>高速放大器</b>	
<a href="#">THS4281</a>	超低功耗、高速、轨到轨输入/输出、电压反馈运算放大器
<a href="#">THS4031</a>	100MHz 低噪声电压反馈放大器
<b>PGA 和仪表放大器</b>	
<a href="#">INA333</a>	低功耗精密仪表放大器
<a href="#">INA826</a>	高精度、200 $\mu$ A 电源电流、36V 电源仪表放大器
<b>精密基准</b>	
<a href="#">REF50xx</a>	低噪声、极低漂移、高精度电压基准
<a href="#">REF33xx</a>	30ppm/°C 漂移、3.9 $\mu$ A、SOT23-3、SC70-3 电压基准
<a href="#">REF20xx</a>	低漂移、低功耗、双输出 Vref 和 Vref/2 电压基准

**表 3. 推荐的 TI 设计**

设计	说明
<a href="#">TIPD112</a>	适用于多路复用器和步进输入的数据采集 (18 位、1 $\mu$ s 满量程响应) 参考设计
<a href="#">TIPD113</a>	数据采集参考设计 (10kHz 交流、35mW、18 位、1MSPS)
<a href="#">TIPD114</a>	数据采集参考设计 (1kHz 交流、1mW、18 位、1MSPS)
<a href="#">TIPD115</a>	针对最低失真和最低噪声进行优化的 18 位、1MSPS 数据采集参考设计
<a href="#">TIPD116</a>	适用于 ECG 系统的数据采集模块 (离散 LEAD I ECG 实施方案) 参考设计

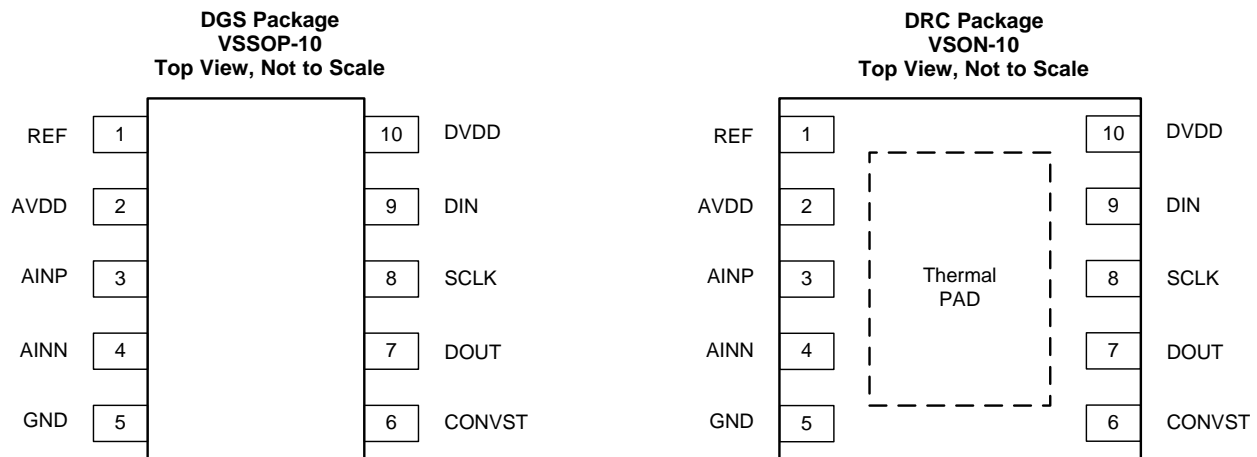
**表 4. 相关文档**

Precision Hub 博客
使用 SAR ADC TINA 模型: 静态特性, 功率调节
使用 SAR ADC TINA 模型: 关于稳定性的诸多问题
SAR ADC 响应时间: 迅速响应, 迅速控制
SAR ADC 输入的相关注意事项

**表 5. 工具与支持**

TINA 模型	IBIS 模型	评估模型
ADS8881 TINA-TI 参考设计	ADS8881 IBIS 模型	ADS8881EVM-PDK

## 6 Pin Configurations and Functions


**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
AINN	4	Analog input	Inverting analog signal input
AINP	3	Analog input	Noninverting analog signal input
AVDD	2	Analog	Analog power supply. This pin must be decoupled to GND with a 1- $\mu$ F capacitor.
CONVST	6	Digital input	Convert input. This pin also functions as the $\overline{CS}$ input in 3-wire interface mode; see the <a href="#">Description</a> and <a href="#">Timing Requirements</a> sections for more details.
DIN	9	Digital input	Serial data input. The DIN level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode; see the <a href="#">Description</a> and <a href="#">Timing Requirements</a> sections for more details.
DOUT	7	Digital output	Serial data output
DVDD	10	Power supply	Digital interface power supply. This pin must be decoupled to GND with a 1- $\mu$ F capacitor.
GND	5	Analog, digital	Device ground. Note that this pin is a common ground pin for both the analog power supply (AVDD) and digital I/O supply (DVDD). The reference return line is also internally connected to this pin.
REF	1	Analog	Positive reference input. This pin must be decoupled with a 10- $\mu$ F or larger capacitor.
SCLK	8	Digital input	Clock input for serial interface. Data output (on DOUT) are synchronized with this clock.
Thermal pad	—	Thermal pad	Exposed thermal pad ( <b>only for the DRC package option</b> ). Texas Instruments recommends connecting the thermal pad to the printed circuit board (PCB) ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
AINP to GND or AINN to GND		-0.3	REF + 0.3	V
AVDD to GND or DVDD to GND		-0.3	4	V
REF to GND		-0.3	5.7	V
Digital input voltage to GND		-0.3	DVDD + 0.3	V
Digital output to GND		-0.3	DVDD + 0.3	V
Operating temperature, T <sub>A</sub>	ADS8881C	0	70	°C
	ADS8881I	-40	85	
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		3		V
DVDD	Digital power supply		3		V
V <sub>REF</sub>	Reference voltage		5		V

### 7.4 Thermal Information

THERMAL METRIC		ADS8881		UNIT
		DGS (VSSOP)	DRC (VSON)	
		10 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	151.9	111.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	45.4	46.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	72.2	45.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.3	3.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	70.9	45.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

## 7.5 Electrical Characteristics

All minimum and maximum specifications are at  $V_{DD} = 3\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ ,  $V_{CM} = V_{REF} / 2\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , over the operating free-air temperature range, unless otherwise noted.

Typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ , and  $DV_{DD} = 3\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>					
Full-scale input span <sup>(1)(2)</sup>	AINP – AINN	$-V_{REF}$		$V_{REF}$	V
Operating input range <sup>(1)(2)</sup>	AINP	-0.1		$V_{REF} + 0.1$	V
	AINN	-0.1		$V_{REF} + 0.1$	
$V_{CM}$ Input common-mode range		0	$V_{REF} / 2$	$V_{REF}$	V
$C_I$ Input capacitance	AINP and AINN terminal to GND		59		pF
<b>EXTERNAL REFERENCE INPUT</b>					
$V_{REF}$ Input range	ADS8881C	3		5	V
	ADS8881I	2.5		5	
Reference input current	During conversion, 1-MHz sample rate, mid-code		300		$\mu\text{A}$
Reference leakage current			250		nA
$C_{REF}$ Decoupling capacitor at the REF input		10	22		$\mu\text{F}$
	Input leakage current	During acquisition for dc input	5		
<b>SYSTEM PERFORMANCE</b>					
Resolution			18		Bits
NMC No missing codes		18			Bits
DNL Differential linearity	ADS8881C	-0.99	$\pm 0.6$	1	LSB <sup>(3)</sup>
	ADS8881I	-0.99	$\pm 0.7$	1.5	
INL Integral linearity <sup>(4)</sup>	ADS8881C	-2	$\pm 1.2$	2	LSB <sup>(3)</sup>
	ADS8881I	-3	$\pm 1.5$	3	
$E_O$ Offset error <sup>(5)</sup>		-4	$\pm 1$	4	mV
	Offset error drift with temperature		$\pm 1.5$		
$E_G$ Gain error		-0.01	$\pm 0.005$	0.01	%FSR
	Gain error drift with temperature		$\pm 0.15$		
CMRR Common-mode rejection ratio		90	100		dB
PSRR Power-supply rejection ratio	At mid-code		80		dB
Transition noise			0.7		LSB
<b>SAMPLING DYNAMICS</b>					
$t_{conv}$ Conversion time		500		710	ns
$t_{ACQ}$ Acquisition time		290			ns
Maximum throughput rate with or without latency				1000	kHz
Aperture delay			4		ns
Aperture jitter, RMS			5		ps
Step response	Settling to 18-bit accuracy		290		ns
Overshoot recovery	Settling to 18-bit accuracy		290		ns

(1) Ideal input span, does not include gain or offset error.

(2) Specified for  $V_{CM} = V_{REF} / 2$ ; see the [Analog Input](#) section for the effect of  $V_{CM}$  on the full-scale input range.

(3) LSB = least significant bit. 1 LSB at 18-bits is approximately 3.8 ppm.

(4) This parameter is the endpoint INL, not best-fit.

(5) Measured relative to actual measured reference.



## Electrical Characteristics (continued)

All minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, V<sub>REF</sub> = 5 V, V<sub>CM</sub> = V<sub>REF</sub> / 2 V, and f<sub>SAMPLE</sub> = 1 MSPS, over the operating free-air temperature range, unless otherwise noted.

Typical specifications are at T<sub>A</sub> = 25°C, AVDD = 3 V, and DVDD = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC CHARACTERISTICS</b>						
SINAD	Signal-to-noise + distortion <sup>(6)</sup>	At 1 kHz, V <sub>REF</sub> = 5 V	98	99.9		dB
		At 10 kHz, V <sub>REF</sub> = 5 V		98.7		
		At 100 kHz, V <sub>REF</sub> = 5 V		93.3		
SNR	Signal-to-noise ratio <sup>(6)</sup>	At 1 kHz, V <sub>REF</sub> = 5 V	98.5	100		dB
		At 10 kHz, V <sub>REF</sub> = 5 V		99.5		
		At 100 kHz, V <sub>REF</sub> = 5 V		93.5		
THD	Total harmonic distortion <sup>(6)(7)</sup>	At 1 kHz, V <sub>REF</sub> = 5 V		-115		dB
		At 10 kHz, V <sub>REF</sub> = 5 V		-112		
		At 100 kHz, V <sub>REF</sub> = 5 V		-102		
SFDR	Spurious-free dynamic range <sup>(6)</sup>	At 1 kHz, V <sub>REF</sub> = 5 V		115		dB
		At 10 kHz, V <sub>REF</sub> = 5 V		112		
		At 100 kHz, V <sub>REF</sub> = 5 V		102		
BW <sub>-3dB</sub>	-3-dB small-signal bandwidth			30		MHz
<b>POWER-SUPPLY REQUIREMENTS</b>						
Power-supply voltage	AVDD	Analog supply	2.7	3	3.6	V
	DVDD	Digital supply range for SCLK > 40 MHz	2.7	3	3.6	
		Digital supply range for SCLK < 40 MHz	1.65	1.8	3.6	
Supply current	AVDD	1-MHz sample rate, AVDD = 3 V		1.8	2.4	mA
P <sub>VA</sub>	Power dissipation	1-MHz sample rate, AVDD = 3 V		5.5	7.2	mW
		100-kHz sample rate, AVDD = 3 V		0.55		
		10-kHz sample rate, AVDD = 3 V		55		
I <sub>APD</sub>	Device power-down current <sup>(8)</sup>			50		nA
<b>DIGITAL INPUTS: LOGIC FAMILY (CMOS)</b>						
V <sub>IH</sub>	High-level input voltage	1.65 V < DVDD < 2.3 V	0.8 × DVDD		DVDD + 0.3	V
		2.3 V < DVDD < 3.6 V	0.7 × DVDD		DVDD + 0.3	
V <sub>IL</sub>	Low-level input voltage	1.65 V < DVDD < 2.3 V	-0.3		0.2 × DVDD	V
		2.3 V < DVDD < 3.6 V	-0.3		0.3 × DVDD	
I <sub>LK</sub>	Digital input leakage current			±10	±100	nA
<b>DIGITAL OUTPUTS: LOGIC FAMILY (CMOS)</b>						
V <sub>OH</sub>	High-level output voltage	I <sub>O</sub> = 500-μA source, C <sub>LOAD</sub> = 20 pF	0.8 × DVDD		DVDD	V
V <sub>OL</sub>	Low-level output voltage	I <sub>O</sub> = 500-μA sink, C <sub>LOAD</sub> = 20 pF	0		0.2 × DVDD	V
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Operating free-air temperature	ADS8881C	0		70	°C
		ADS8881I	-40		85	

(6) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.

(7) Calculated on the first nine harmonics of the input frequency.

(8) The device automatically enters a power-down state at the end of every conversion, and remains in power-down during the acquisition phase.



## 7.7 Timing Requirements: 4-Wire Operation

All specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range, unless otherwise noted.

		MIN	TYP	MAX	UNIT
$t_{ACQ}$	Acquisition time	290			ns
$t_{conv}$	Conversion time	$T_A$ in the range $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	500	710	ns
		$T_A$ in the range $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	500	700	
$t_{conv}$	Conversion time	500			ns
$1/f_{sample}$	Time between conversions	1000			ns
$t_{wh-DI}$	Pulse duration: DIN high	10			ns
$t_{wl-CNV}$	Pulse width: CONVST low	20			ns
$t_{d-DI-DO}$	Delay time: DIN low to MSB valid			12.3	ns
$t_{d-DI-DOhz}$	Delay time: DIN high or last SCLK falling edge to DOUT 3-state			13.2	ns
$t_{su-DI-CNV}$	Setup time: DIN high to CONVST rising edge	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN high from CONVST rising edge (see Figure 63)	0			ns

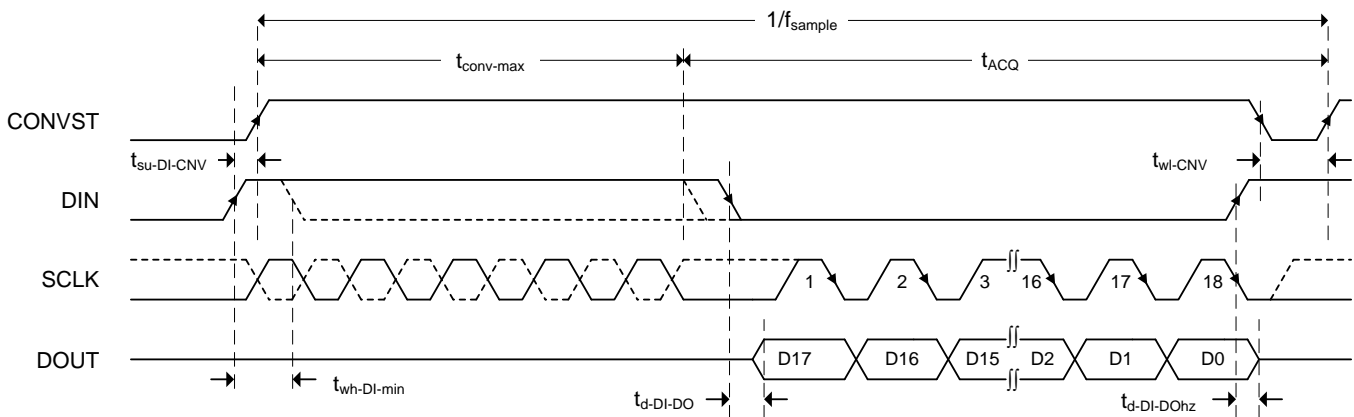


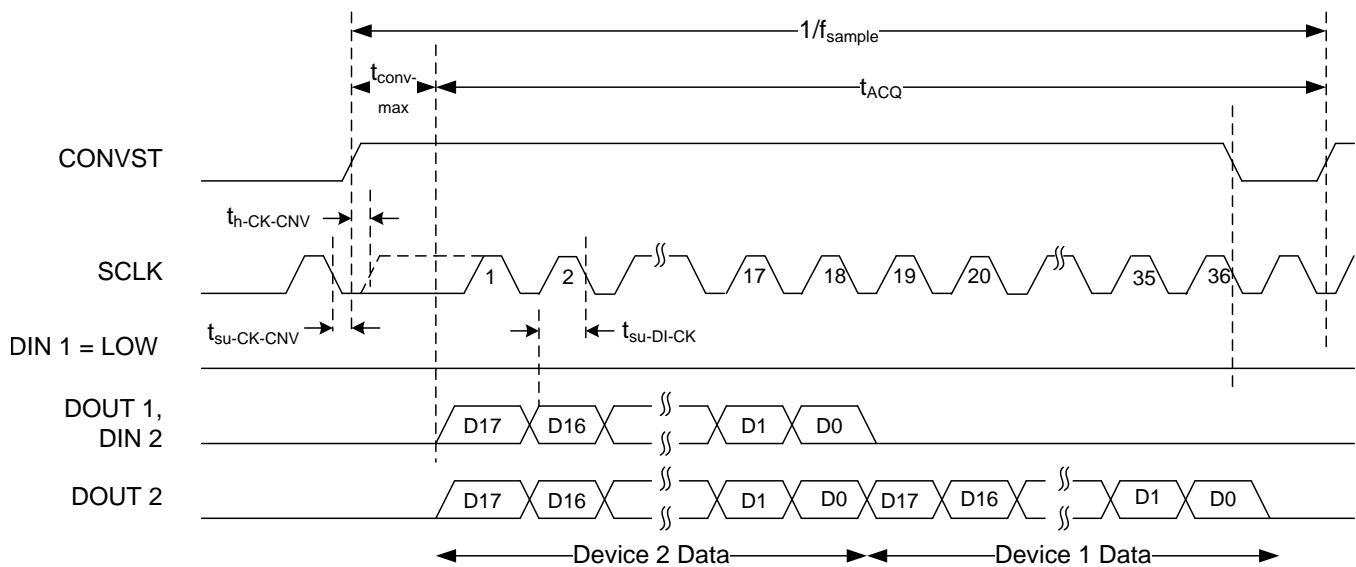
Figure 2. 4-Wire Operation: DIN Functions as Chip Select

NOTE: Figure 2 shows the timing diagram for the *4-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in [Timing Requirements: 4-Wire Operation](#) are also applicable for the *4-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified; see the [Device Functional Modes](#) section for specific details for each interface option.

## 7.8 Timing Requirements: Daisy-Chain

All specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range, unless otherwise noted.

		MIN	TYP	MAX	UNIT
$t_{ACQ}$	Acquisition time	290			ns
$t_{conv}$	Conversion time	$T_A$ in the range -40°C to 85°C	500	710	ns
		$T_A$ in the range 0°C to 70°C	500	700	
$t_{conv}$	Conversion time	500			ns
$1/f_{sample}$	Time between conversions	1000			ns
$t_{su-CK-CNV}$	Setup time: SCLK valid to CONVST rising edge	5			ns
$t_{h-CK-CNV}$	Hold time: SCLK valid from CONVST rising edge	5			ns
$t_{su-DI-CNV}$	Setup time: DIN low to CONVST rising edge (see Figure 2)	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN low from CONVST rising edge (see Figure 63)	0			ns
$t_{su-DI-CK}$	Setup time: DIN valid to SCLK falling edge	1.5			ns



**Figure 3. Daisy-Chain Operation: Two Devices**

NOTE: Figure 3 shows the timing diagram for the *Daisy-Chain Mode Without a Busy Indicator* interface option. However, the timing parameters specified in *Timing Requirements: Daisy-Chain* are also applicable for the *Daisy-Chain Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

## 7.9 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

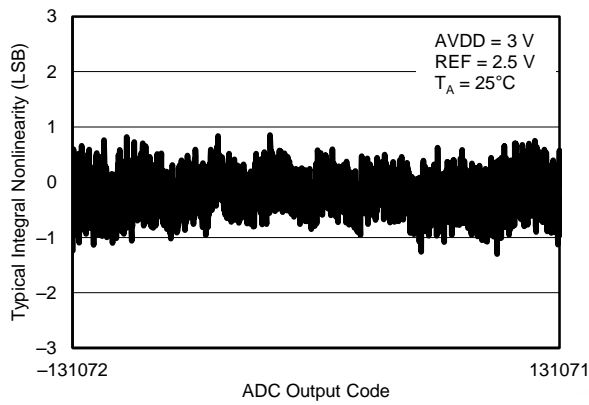


Figure 4. Typical INL ( $V_{REF} = 2.5\text{ V}$ )

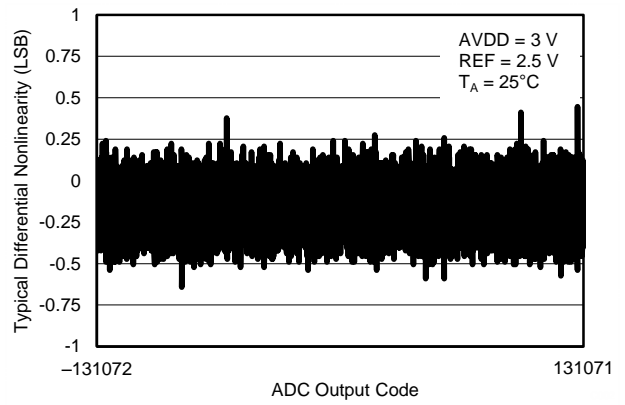


Figure 5. Typical DNL ( $V_{REF} = 2.5\text{ V}$ )

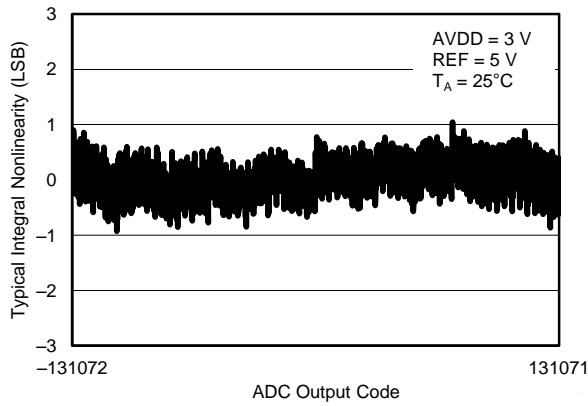


Figure 6. Typical INL ( $V_{REF} = 5\text{ V}$ )

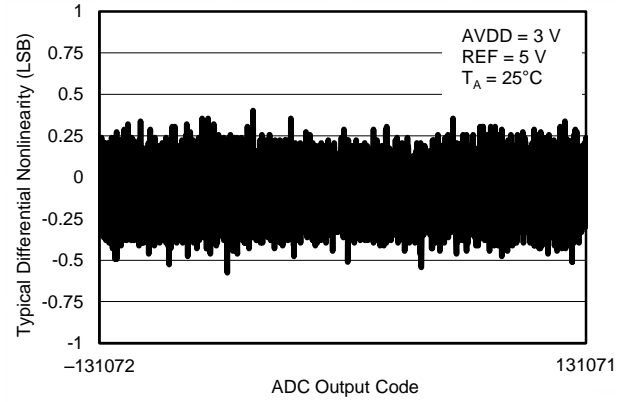


Figure 7. Typical DNL ( $V_{REF} = 5\text{ V}$ )

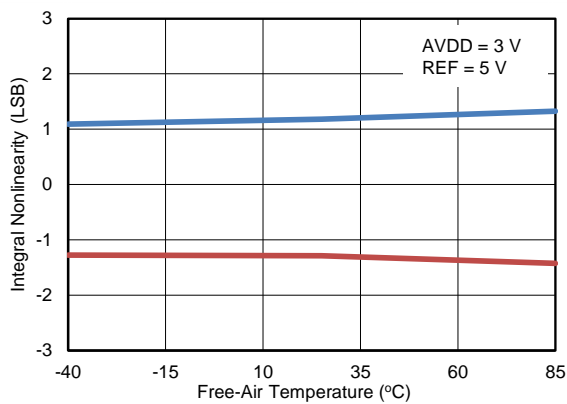


Figure 8. INL vs Temperature

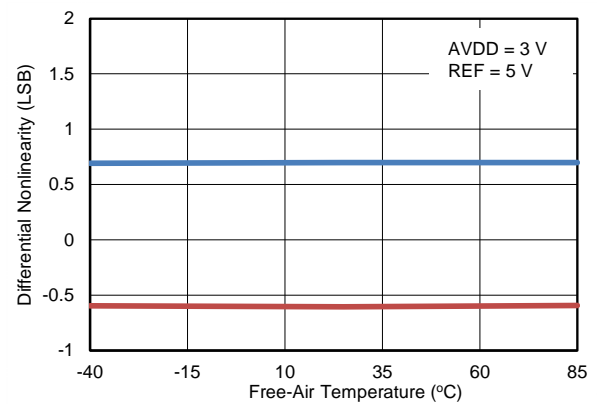


Figure 9. DNL vs Temperature

### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

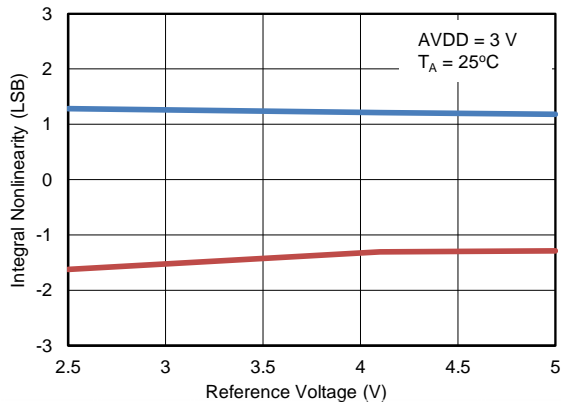


Figure 10. INL vs Reference Voltage

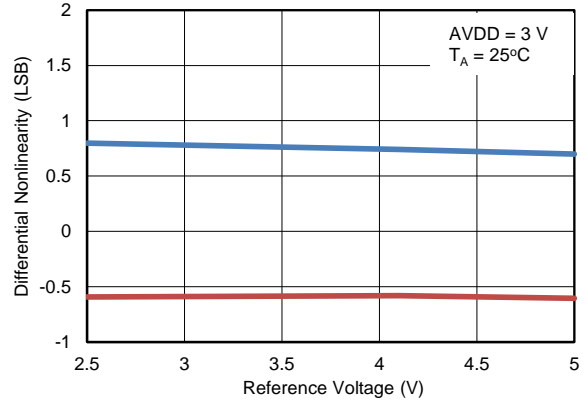


Figure 11. DNL vs Reference Voltage

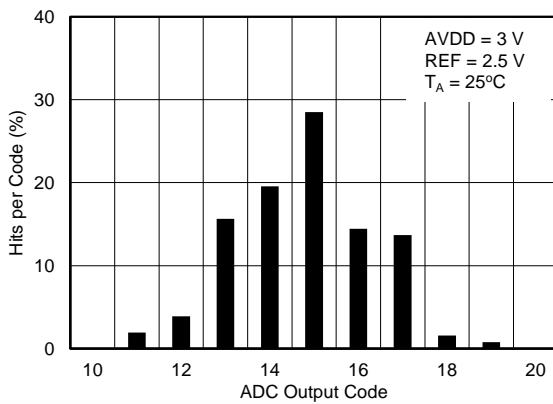


Figure 12. DC Input Histogram ( $V_{REF} = 2.5\text{ V}$ )

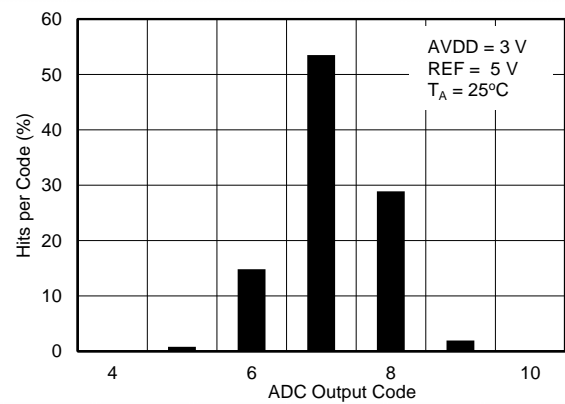


Figure 13. DC Input Histogram ( $V_{REF} = 5\text{ V}$ )

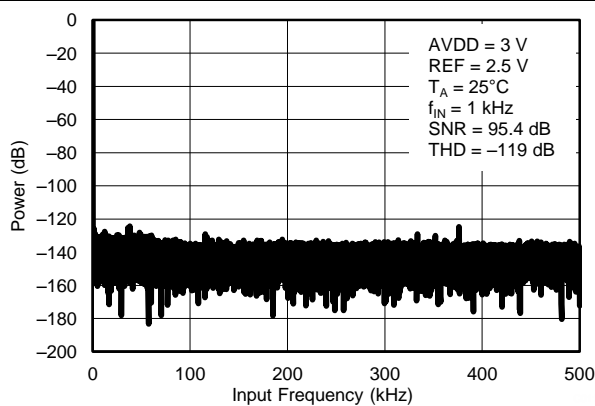


Figure 14. Typical FFT ( $V_{REF} = 2.5\text{ V}$ )

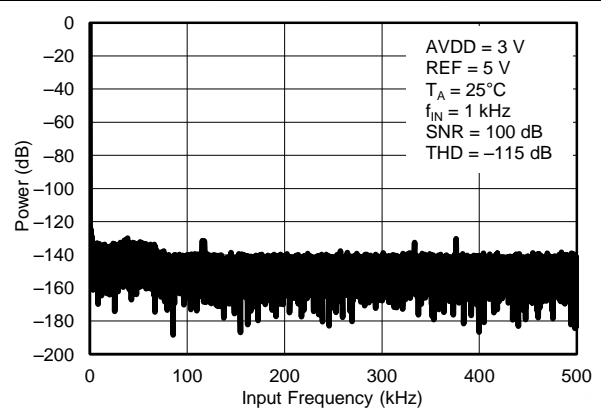
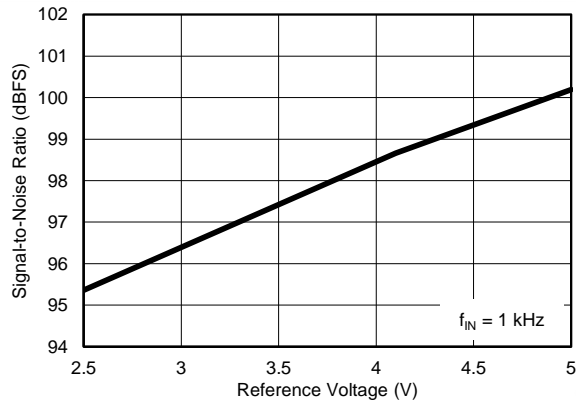


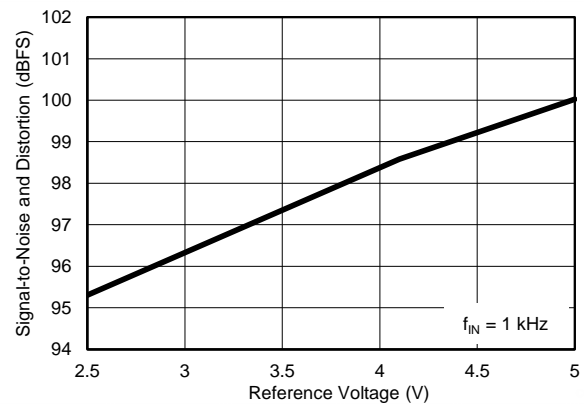
Figure 15. Typical FFT ( $V_{REF} = 5\text{ V}$ )

**Typical Characteristics (continued)**

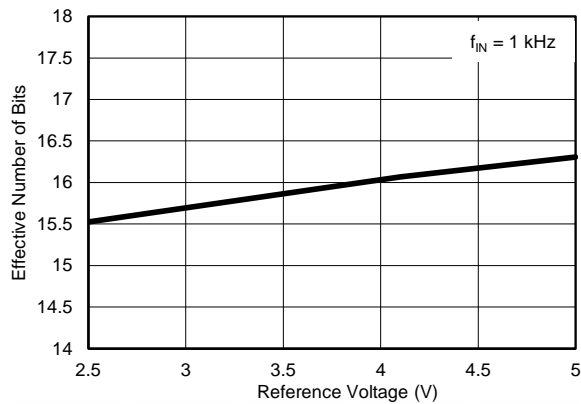
At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.



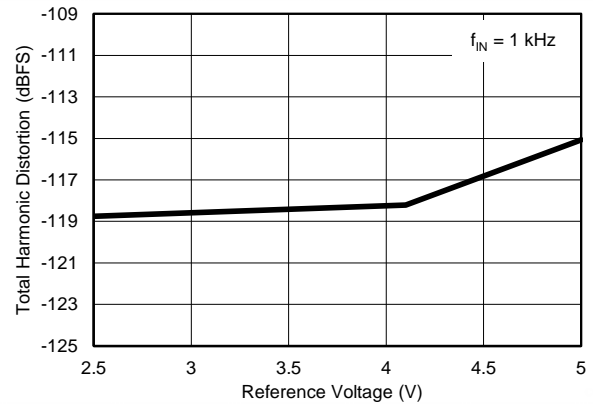
**Figure 16. SNR vs Reference Voltage**



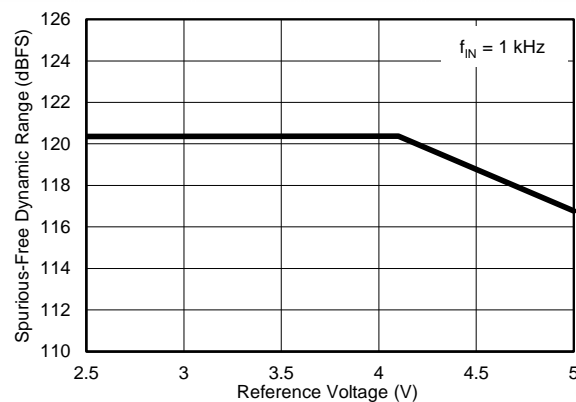
**Figure 17. SINAD vs Reference Voltage**



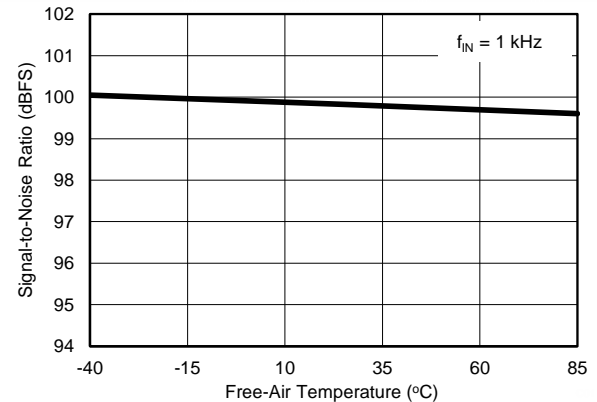
**Figure 18. ENOB vs Reference Voltage**



**Figure 19. THD vs Reference Voltage**



**Figure 20. SFDR vs Reference Voltage**



**Figure 21. SNR vs Temperature**

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

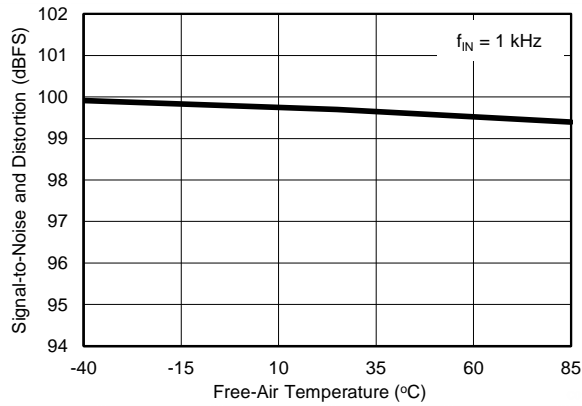


Figure 22. SINAD vs Temperature

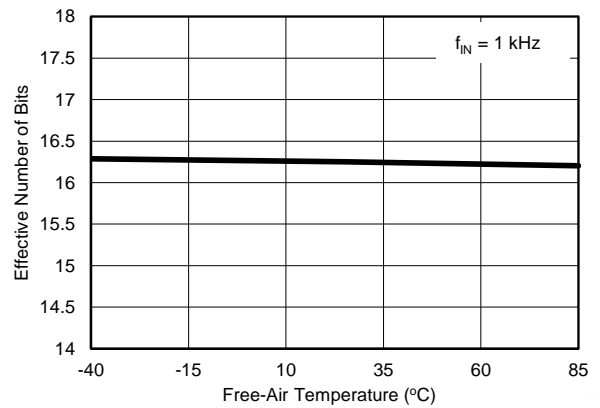


Figure 23. ENOB vs Temperature

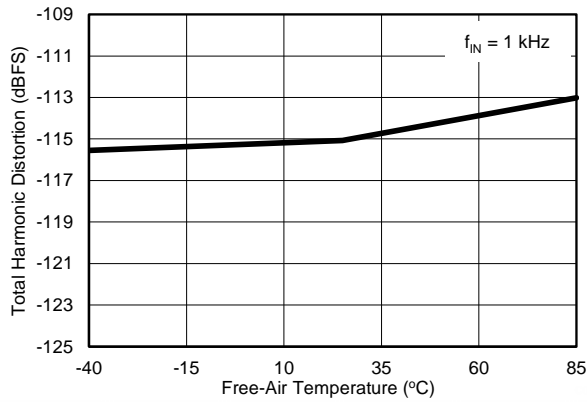


Figure 24. THD vs Temperature

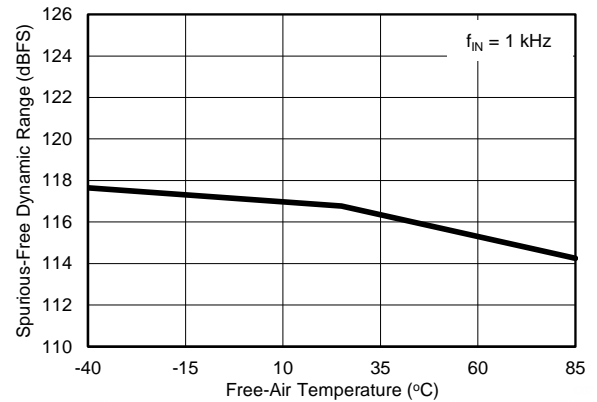


Figure 25. SFDR vs Temperature

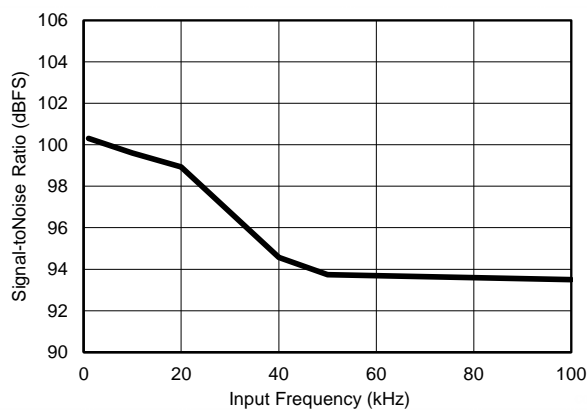


Figure 26. SNR vs Input Frequency

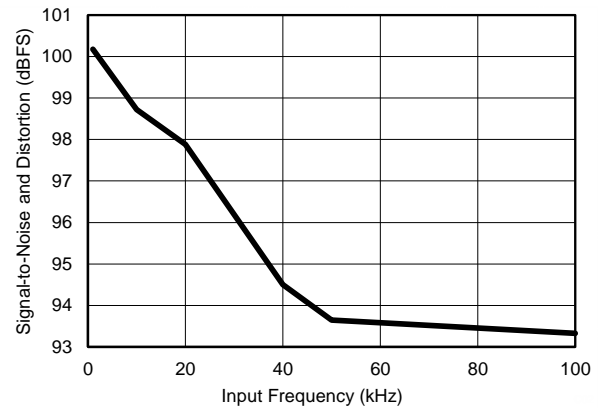


Figure 27. SINAD vs Input Frequency



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = 3\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

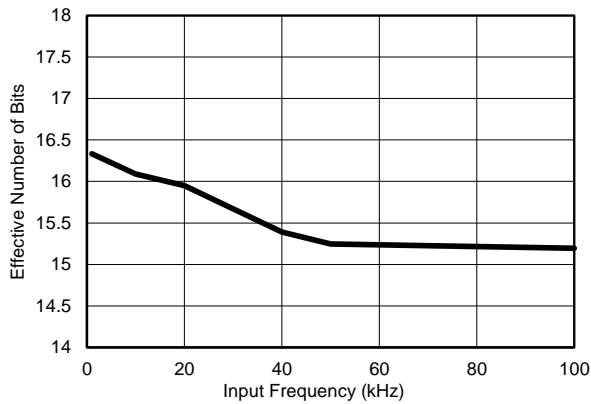


Figure 28. ENOB vs Input Frequency

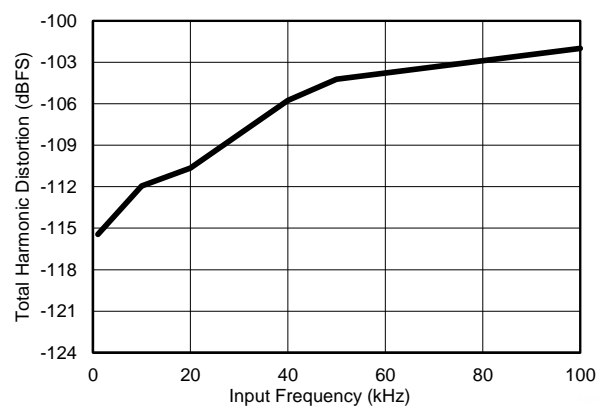


Figure 29. THD vs Input Frequency

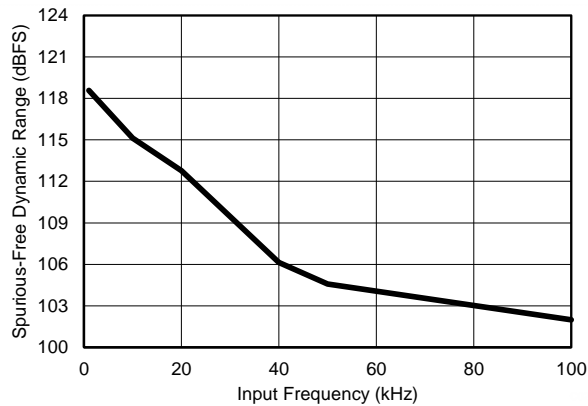


Figure 30. SFDR vs Input Frequency

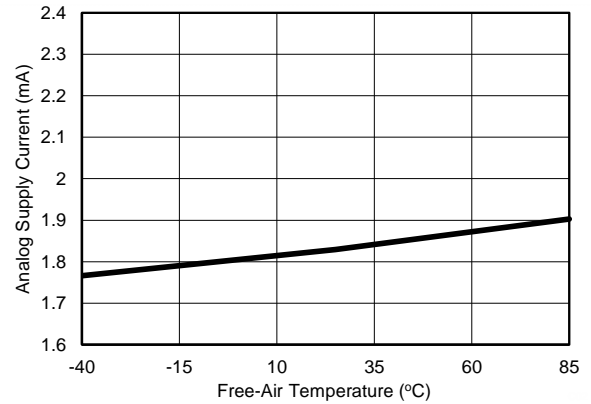


Figure 31. Supply Current vs Temperature

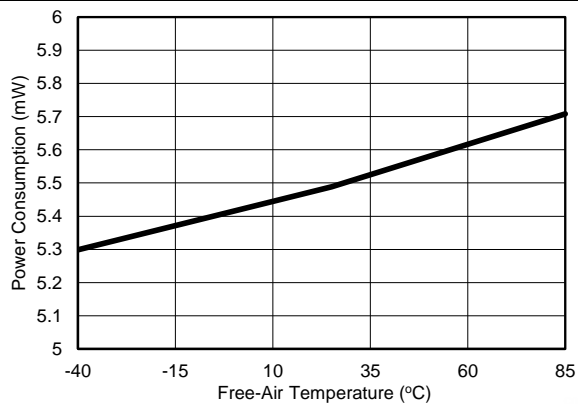


Figure 32. Power Consumption vs Temperature

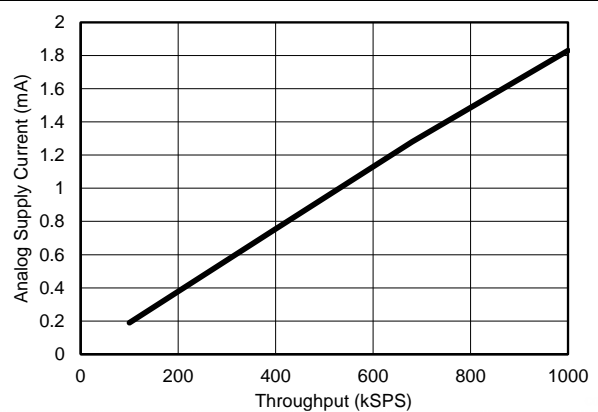


Figure 33. Supply Current vs Throughput

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

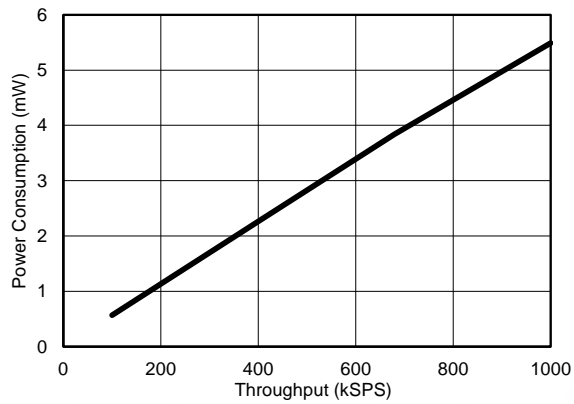


Figure 34. Power Consumption vs Throughput

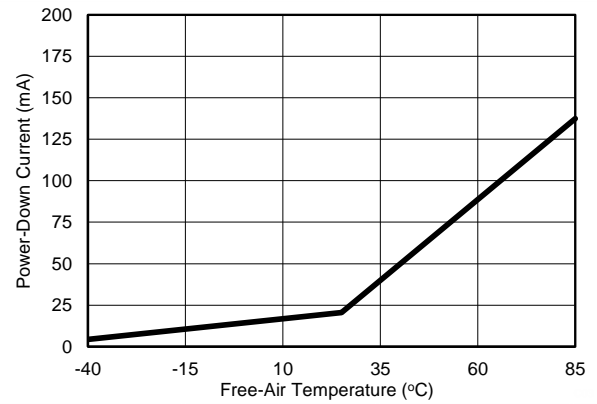


Figure 35. Power-Down Current vs Temperature

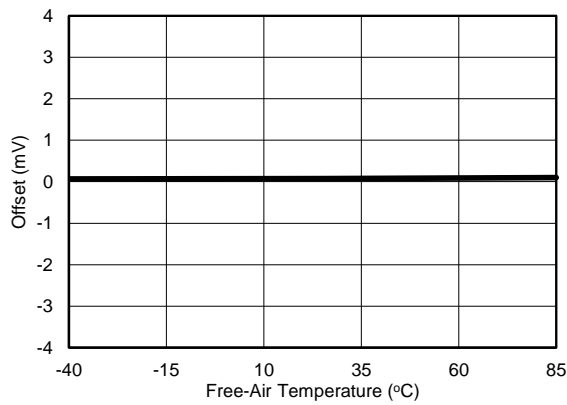


Figure 36. Offset vs Temperature

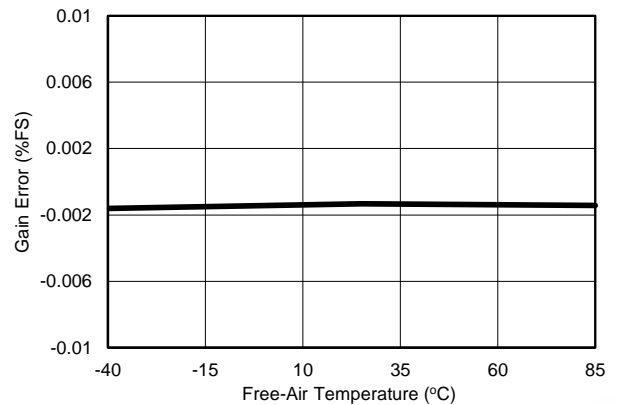


Figure 37. Gain Error vs Temperature

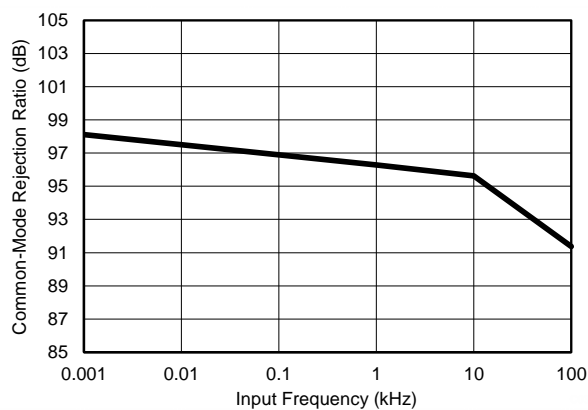


Figure 38. CMRR vs Input Frequency

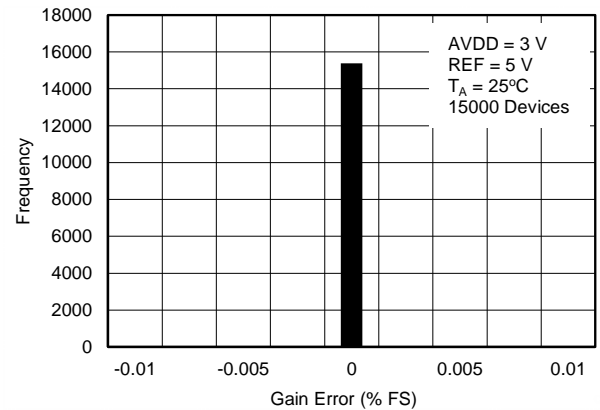


Figure 39. Typical Distribution of Gain Error

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and  $f_{SAMPLE} = 1\text{ MSPS}$ , unless otherwise noted.

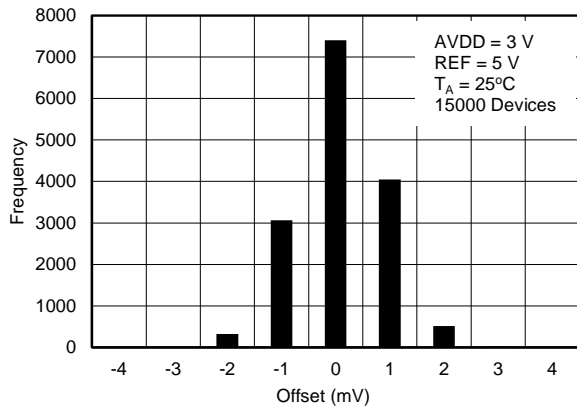


Figure 40. Typical Distribution of Offset Error

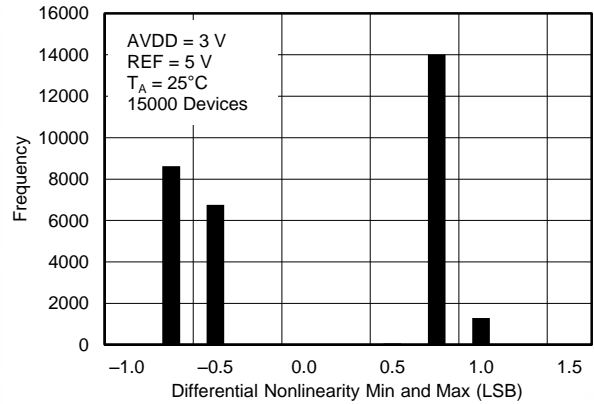


Figure 41. Typical Distribution of Differential Nonlinearity (Minimum and Maximum)

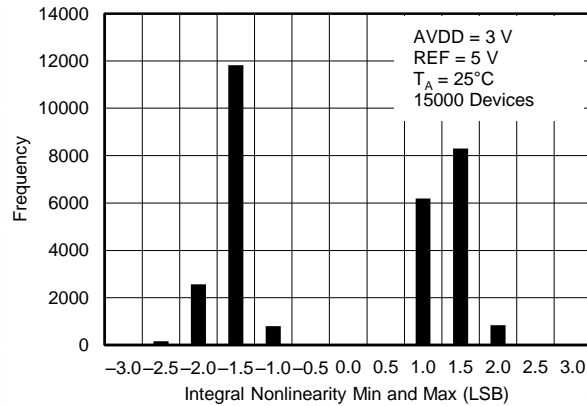


Figure 42. Typical Distribution of Integral Nonlinearity (Minimum and Maximum)

## 8 Parametric Measurement Information

### 8.1 Equivalent Circuits

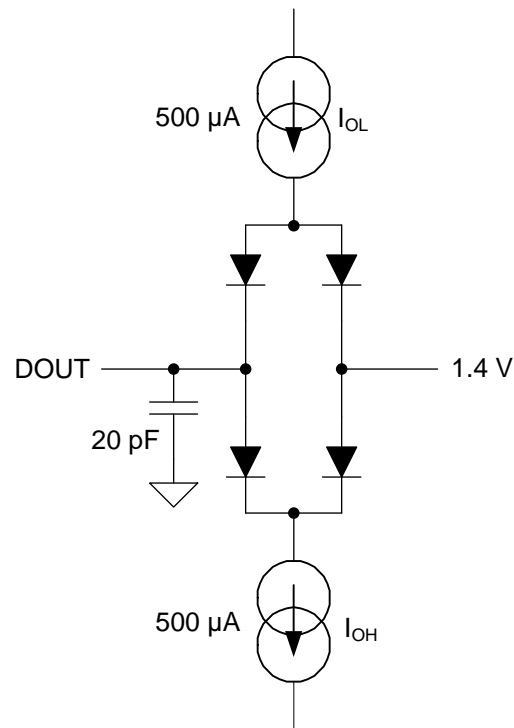


Figure 43. Load Circuit for Digital Interface Timing

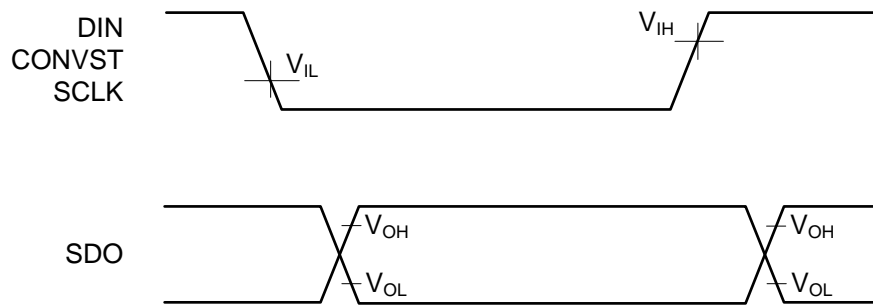


Figure 44. Voltage Levels for Timing

## 9 Detailed Description

### 9.1 Overview

The ADS8881 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) from a 16- and 18-bit device family. This compact device features high performance. Power consumption is inherently low and scales linearly with sampling speed. The architecture is based on charge redistribution that inherently includes a sample-and-hold (S/H) function.

The ADS8881 supports a true-differential analog input across two pins (INP and INN). When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the INP and INN inputs are disconnected from the internal circuit.

The ADS8881 uses an internal clock to perform conversions. The device reconnects the sampling capacitors to the INP and INN pins after conversion and then enters an acquisition phase. During the acquisition phase, the device is powered down and the conversion result can be read.

The device digital output is available in SPI-compatible format, thus making interfacing with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs) easy.

### 9.2 Functional Block Diagram

Figure 45 shows the detailed functional block diagram for the device.

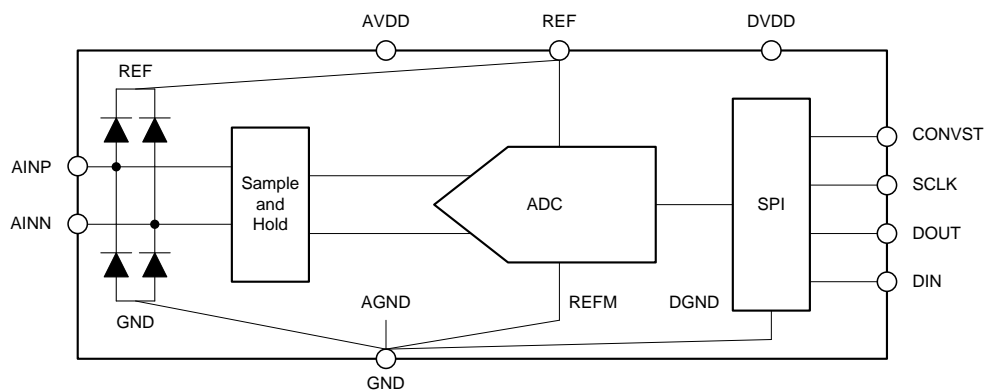


Figure 45. Detailed Block Diagram

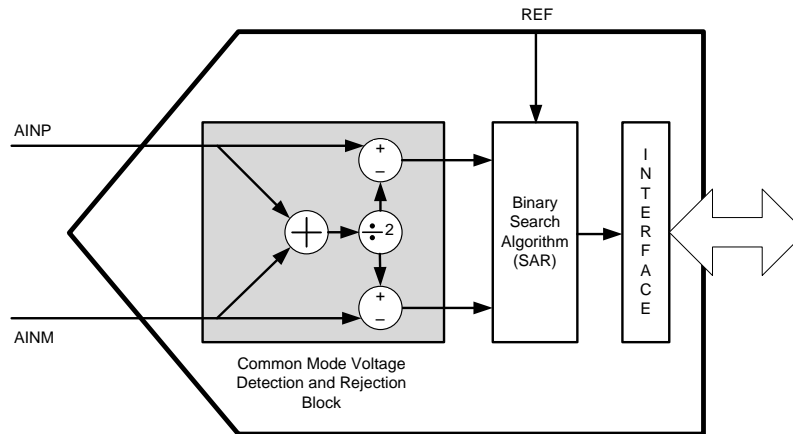
### 9.3 Feature Description

#### 9.3.1 Analog Input

As shown in Figure 45, the device features a differential analog input. Both positive and negative inputs are individually sampled on 55-pF sampling capacitors and the device converts for the voltage difference between the two sampled values:  $V_{INP} - V_{INN}$ .

**Feature Description (continued)**

Most differential input SAR ADCs prohibit the input common-mode voltage,  $V_{CM}$  (that is, the average voltage between the inputs), at AINP or AINM from varying more than approximately 10% beyond the mid-scale input value. As shown in Figure 46, the device has a unique common-mode voltage detection and rejection block that does not have this restriction and thus allows  $V_{CM}$  to be set to any value between 0 V and  $V_{REF}$  without degrading device performance.



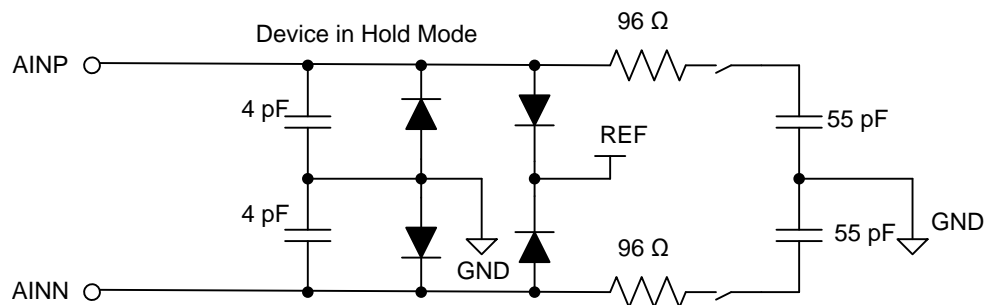
**Figure 46. Conceptual Diagram: True Differential Input Structure**

Table 6 shows the full-scale input range of the device as a function of input common-mode voltage. The device offers a maximum dynamic range for  $V_{CM} = V_{REF} / 2$ . The differential input with wide common-mode range allows connecting differential signals from sensors without any signal conditioning.

**Table 6. Full-Scale Input Range**

$V_{CM}$	ABSOLUTE INPUT RANGE		FULL SCALE INPUT RANGE ( $V_{FS}$ )
	$V_{AINP}$	$V_{AINN}$	
$V_{CM} < V_{REF} / 2$	0 to $2 \times V_{CM}$	0 to $2 \times V_{CM}$	$(-2 \times V_{CM})$ to $(2 \times V_{CM})$
$V_{CM} = V_{REF} / 2$	0 to $V_{REF}$	0 to $V_{REF}$	$(-V_{REF})$ to $(V_{REF})$
$V_{CM} > V_{REF} / 2$	$(2 \times V_{CM} - V_{REF})$ to $V_{REF}$	$(2 \times V_{CM} - V_{REF})$ to $V_{REF}$	$[-2 \times (V_{CM} - V_{REF})]$ to $[2 \times (V_{CM} - V_{REF})]$

Figure 47 shows an equivalent circuit of the input sampling stage. The sampling switch is represented by a 96-Ω resistance in series with the ideal switch; see the *ADC Input Driver* section for more details on the recommended driving circuits.



**Figure 47. Input Sampling Stage Equivalent Circuit**

Figure 45 and Figure 47 illustrate electrostatic discharge (ESD) protection diodes to REF and GND from both analog inputs. Make sure that these diodes do not turn on by keeping the analog inputs within the specified range.

### 9.3.2 Reference

The device operates with an external reference voltage and switches binary-weighted capacitors onto the reference terminal (REF pin) during the conversion process. The switching frequency is proportional to the internal conversion clock frequency but the dynamic charge requirements are a function of the absolute value of the input voltage and reference voltage. This dynamic load must be supported by a reference driver circuit without degrading the noise and linearity performance of the device. During the acquisition process, the device automatically powers down and does not take any dynamic current from the external reference source. The basic circuit diagram for such a reference driver circuit for precision ADCs is shown in [Figure 48](#); see the [ADC Reference Driver](#) section for more details on the application circuits.

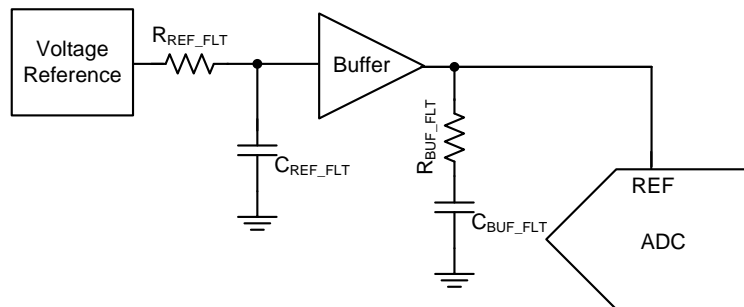


Figure 48. Reference Driver Schematic

### 9.3.3 Clock

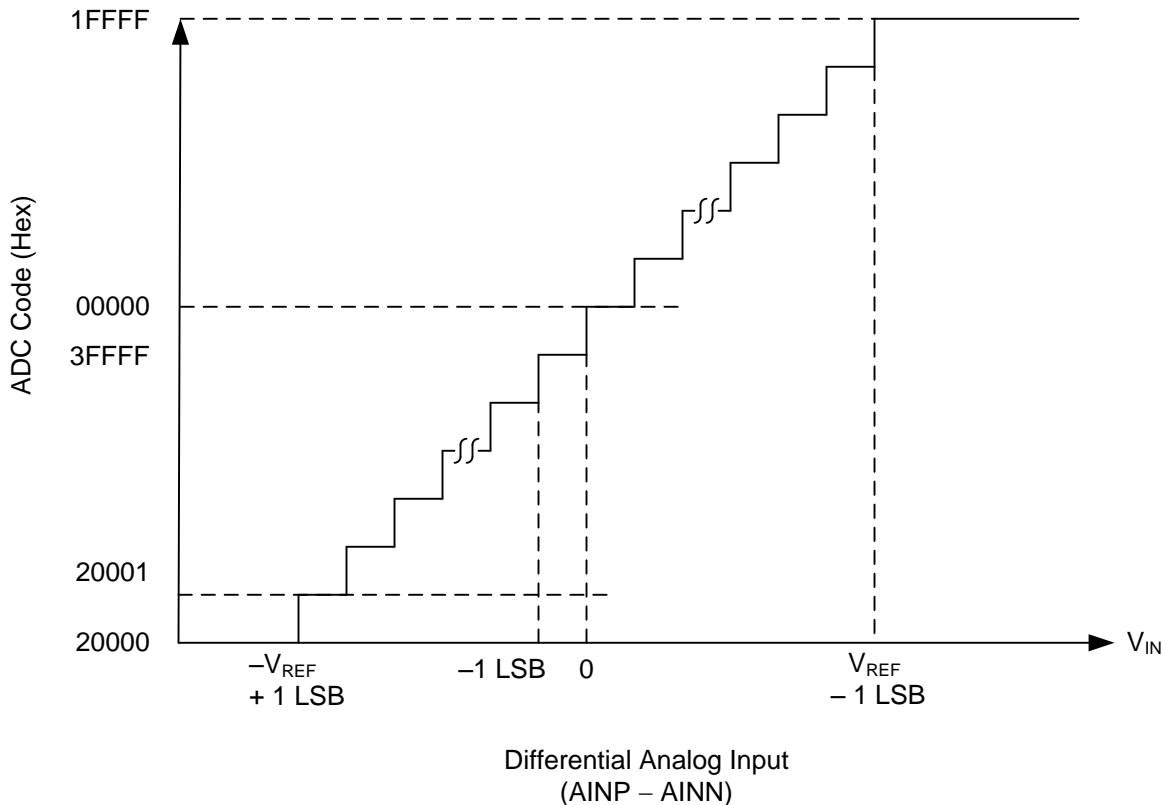
The device uses an internal clock for conversion. Conversion duration may vary but is bounded by the minimum and maximum value of  $t_{conv}$ , as specified in the [Timing Requirements](#) section. An external SCLK is only used for a serial data read operation. Data are read after a conversion completes and when the device is in acquisition phase for the next sample.

### 9.3.4 ADC Transfer Function

The ADS8881 is a unipolar, differential input device. The device output is in twos complement format.

Figure 49 shows ideal characteristics for the device. The full-scale range for the ADC input ( $A_{INP} - A_{INN}$ ) is equal to twice the reference input voltage to the ADC ( $2 \times V_{REF}$ ). The LSB for the ADC is given by Equation 1.

$$1 \text{ LSB} = [2 \times (V_{REF} / 2^{18})] \quad (1)$$



**Figure 49. Differential Transfer Characteristics**

## 9.4 Device Functional Modes

The ADS8881 is a low pin-count device. However, the device offers six different options for interfacing with the digital host.

These options can be broadly classified as being either  $\overline{CS}$  mode (in either a 3- or 4-wire interface) or *daisy-chain mode*. The device operates in  $\overline{CS}$  mode if  $DIN$  is high at the  $CONVST$  rising edge. If  $DIN$  is low at the  $CONVST$  rising edge, or if  $DIN$  and  $CONVST$  are connected together, the device operates in daisy-chain mode. In both modes, the device can either operate with or without a *busy indicator*, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

The 3-wire interface in  $\overline{CS}$  mode is useful for applications that need galvanic isolation on-board. The 4-wire interface in  $\overline{CS}$  mode allows the user to sample the analog input independent of the serial interface timing and, therefore, allows easier control of an individual device while having multiple, similar devices on-board. The daisy-chain mode is provided to hook multiple devices in a chain similar to a shift register and is useful in reducing component count and the number of signal traces on the board.

### 9.4.1 $\overline{CS}$ Mode

$\overline{CS}$  mode is selected if  $DIN$  is high at the  $CONVST$  rising edge. There are four different interface options available in this mode: 3-wire  $\overline{CS}$  mode without a busy indicator, 3-wire  $\overline{CS}$  mode with a busy indicator, 4-wire  $\overline{CS}$  mode without a busy indicator, and 4-wire  $\overline{CS}$  mode with a busy indicator. The following sections discuss these interface options in detail.



## Device Functional Modes (continued)

### 9.4.1.1 3-Wire $\overline{\text{CS}}$ Mode Without a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host. In this interface option, DIN can be connected to DVDD and CONVST functions as  $\overline{\text{CS}}$  (as shown in Figure 50). As shown in Figure 51, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as  $\overline{\text{CS}}$ ) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must return high before the minimum conversion time ( $t_{\text{conv-min}}$ ) elapses and is held high until the maximum possible conversion time ( $t_{\text{conv-max}}$ ) elapses. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

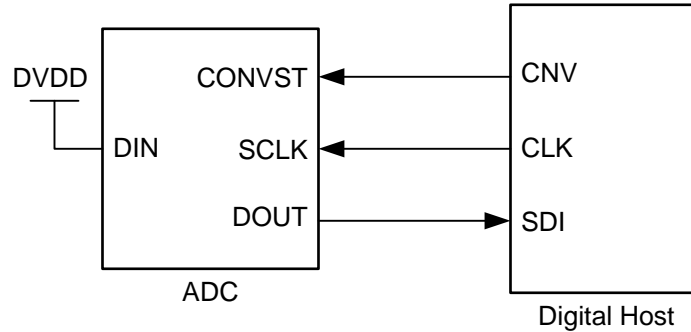


Figure 50. Connection Diagram: 3-Wire  $\overline{\text{CS}}$  Mode Without a Busy Indicator (DIN = 1)

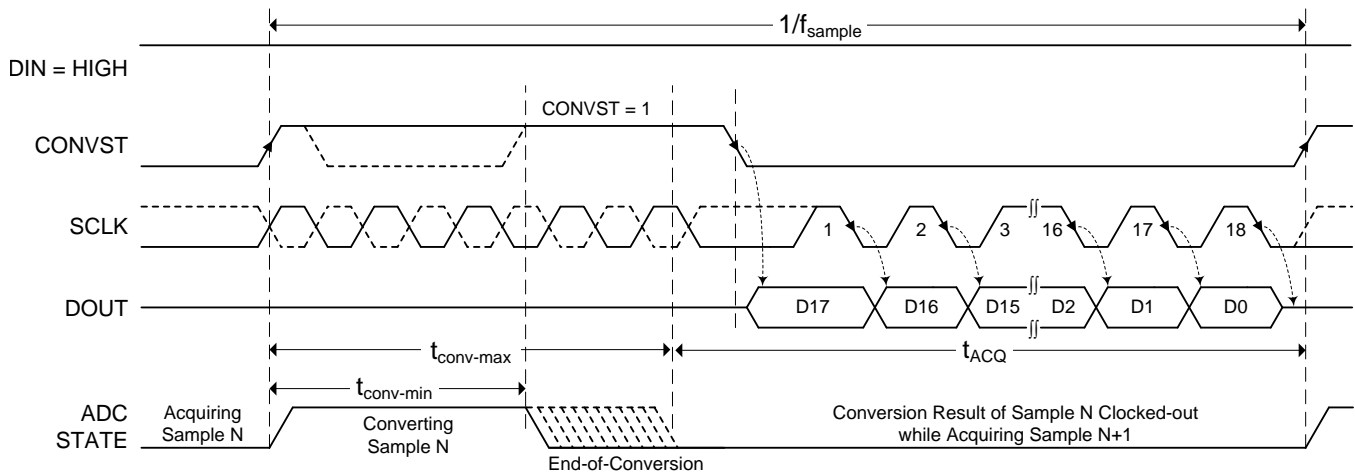


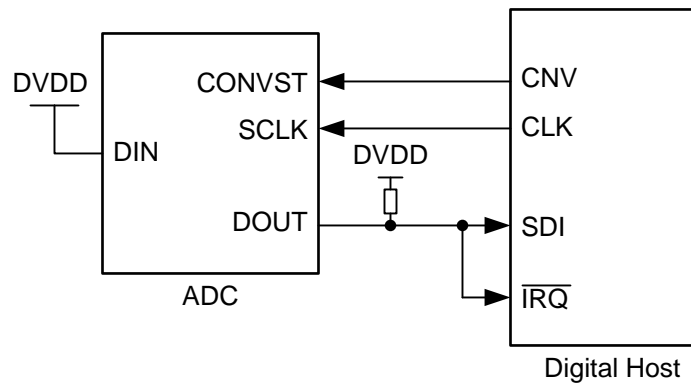
Figure 51. Interface Timing Diagram: 3-Wire  $\overline{\text{CS}}$  Mode (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down. CONVST (functioning as  $\overline{\text{CS}}$ ) can be brought low after the maximum conversion time ( $t_{\text{conv-max}}$ ) elapses. On the CONVST falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the  $t_{\text{h\_CK\_DO-min}}$  time frame. DOUT goes to 3-state after the 18th SCLK falling edge or when CONVST goes high, whichever occurs first.

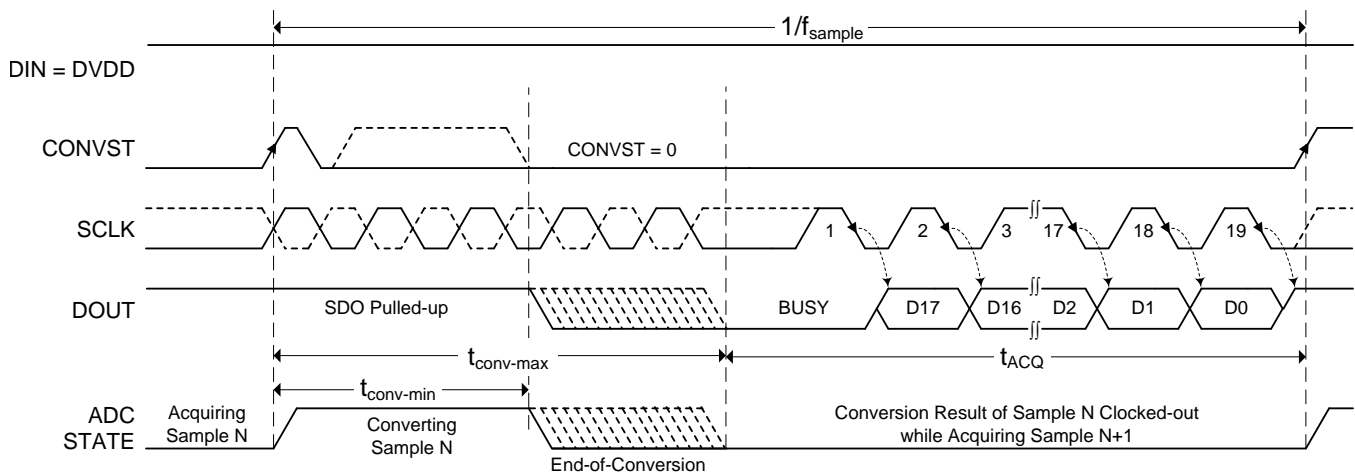
**Device Functional Modes (continued)**

**9.4.1.2 3-Wire  $\overline{\text{CS}}$  Mode With a Busy Indicator**

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, DIN can be connected to DVDD and CONVST functions as  $\overline{\text{CS}}$  (as shown in Figure 52). The pull-up resistor on the DOUT pin ensures that the IRQ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 53, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as  $\overline{\text{CS}}$ ) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must be pulled low before the minimum conversion time ( $t_{\text{conv-min}}$ ) elapses and must remain low until the maximum possible conversion time ( $t_{\text{conv-max}}$ ) elapses. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.



**Figure 52. Connection Diagram: 3-Wire  $\overline{\text{CS}}$  Mode With a Busy Indicator**



**Figure 53. Interface Timing Diagram: 3-Wire  $\overline{\text{CS}}$  Mode With a Busy Indicator (DIN = 1)**

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the IRQ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the  $t_{\text{h\_CK\_DO-min}}$  time frame. DOUT goes to 3-state after the 19th SCLK falling edge or when CONVST goes high, whichever occurs first.

## Device Functional Modes (continued)

### 9.4.1.3 4-Wire $\overline{\text{CS}}$ Mode Without a Busy Indicator

This interface option is useful when one or more ADCs are connected to an SPI-compatible digital host. Figure 54 shows the connection diagram for single ADC; see Figure 56 for the connection diagram for two ADCs.

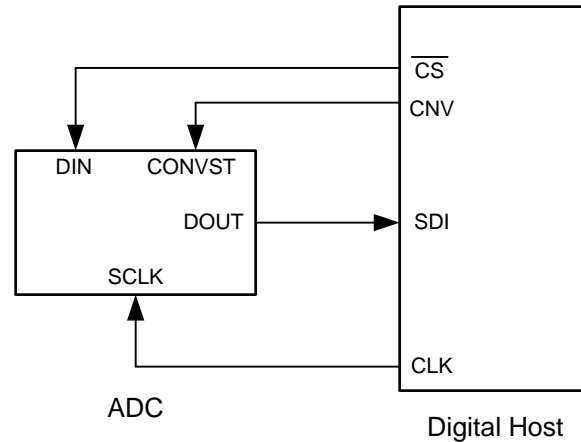


Figure 54. Connection Diagram: Single ADC With 4-Wire  $\overline{\text{CS}}$  Mode Without a Busy Indicator

In this interface option, DIN is controlled by the digital host and functions as  $\overline{\text{CS}}$ . As shown in Figure 55, with DIN high, a CONVST rising edge selects  $\overline{\text{CS}}$  mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (functioning as  $\overline{\text{CS}}$ ) can be pulled low to select other devices on the board. However, DIN must be pulled high before the minimum conversion time ( $t_{\text{conv-min}}$ ) elapses and remains high until the maximum possible conversion time ( $t_{\text{conv-max}}$ ) elapses. A high level on DIN at the end of the conversion ensures the device does not generate a busy indicator.

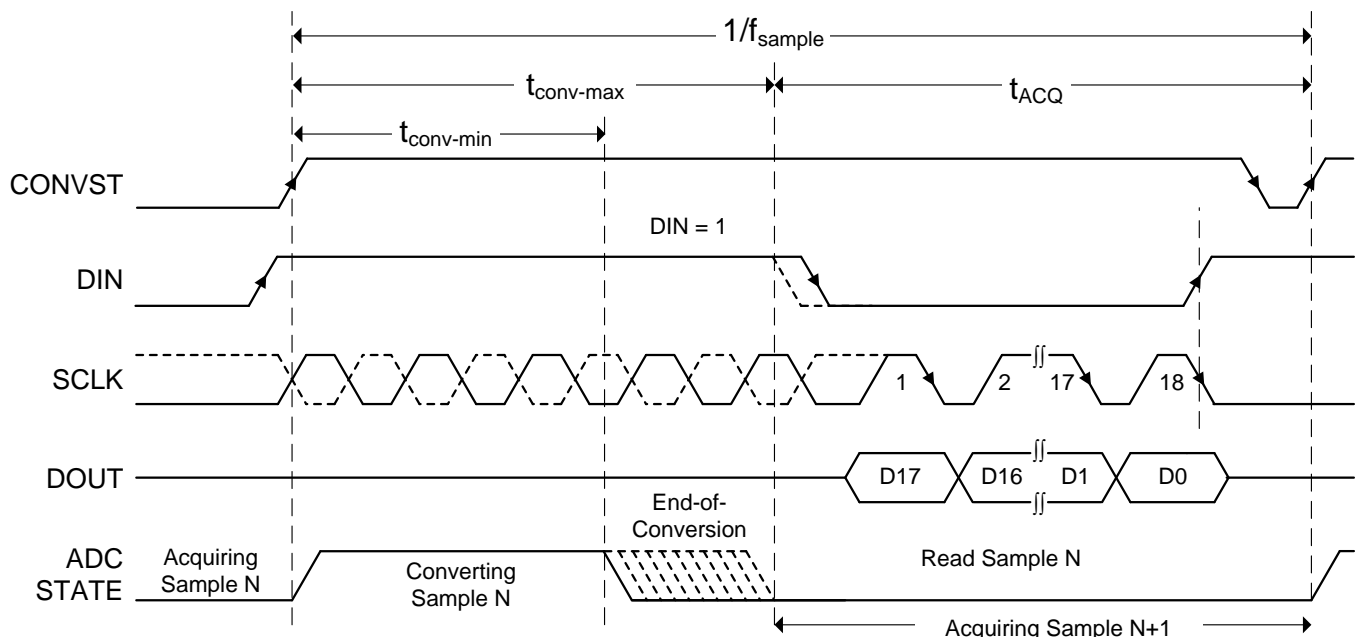


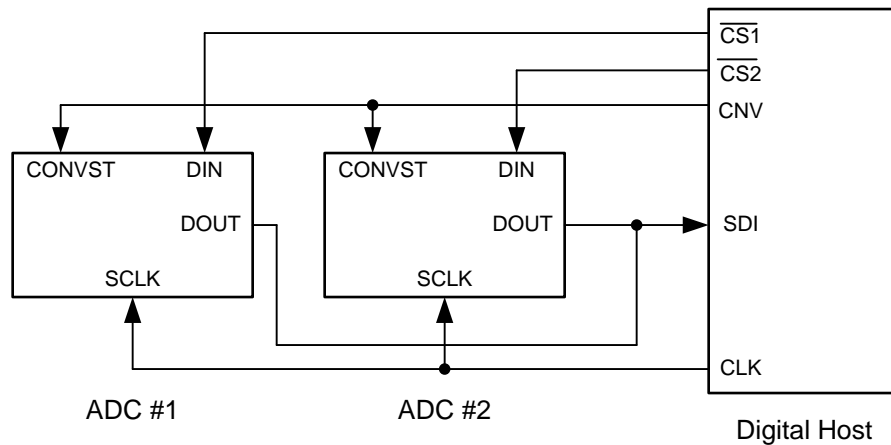
Figure 55. Interface Timing Diagram: Single ADC With 4-Wire  $\overline{\text{CS}}$  Mode

**Device Functional Modes (continued)**

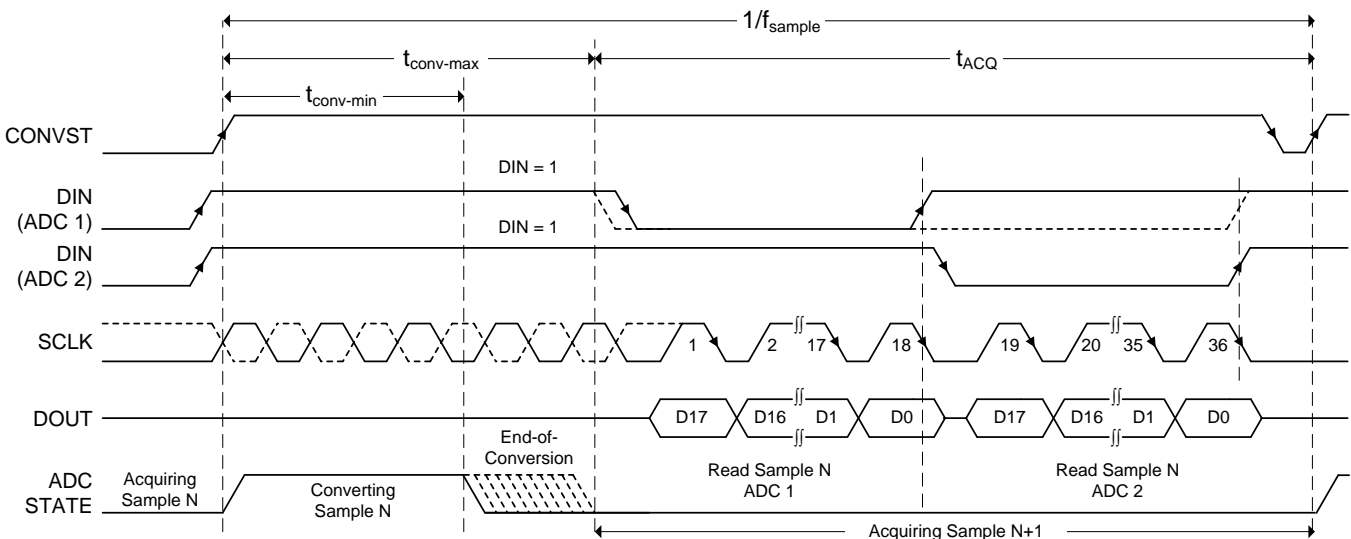
When conversion is complete, the device enters acquisition phase and powers down. DIN (functioning as  $\overline{CS}$ ) can be brought low after the maximum conversion time ( $t_{conv-max}$ ) elapses. On the DIN falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the  $t_{h\_CK\_DO-min}$  time frame. DOUT goes to 3-state after the 18th SCLK falling edge or when DIN goes high, whichever occurs first.

As shown in Figure 56, multiple devices can be hooked together on the same data bus. In this case, as shown in Figure 57, the DIN of the second device (functioning as  $\overline{CS}$  for the second device) can go low after the first device data are read and the DOUT of the first device is in 3-state.

Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.



**Figure 56. Connection Diagram: Two ADCs With 4-Wire  $\overline{CS}$  Mode Without a Busy Indicator**



**Figure 57. Interface Timing Diagram: Two ADCs With 4-Wire  $\overline{CS}$  Mode**

## Device Functional Modes (continued)

### 9.4.1.4 4-Wire $\overline{\text{CS}}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, the analog sample is least affected by clock jitter because the CONVST signal (used to sample the input) is independent of the data read operation. In this interface option, DIN is controlled by the digital host and functions as  $\overline{\text{CS}}$  (as shown in Figure 58). The pull-up resistor on the DOUT pin ensures that the  $\overline{\text{IRQ}}$  pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 59, when DIN is high, a CONVST rising edge selects  $\overline{\text{CS}}$  mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held high from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (acting as  $\overline{\text{CS}}$ ) can be pulled low to select other devices on the board. However, DIN must be pulled low before the minimum conversion time ( $t_{\text{conv-min}}$ ) elapses and remains low until the maximum possible conversion time ( $t_{\text{conv-max}}$ ) elapses. A low level on the DIN input at the end of a conversion ensures the device generates a busy indicator.

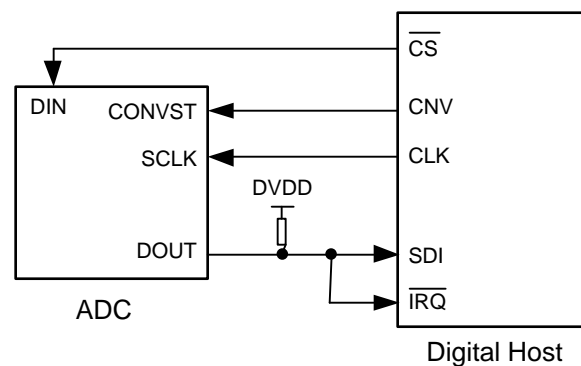


Figure 58. Connection Diagram: 4-Wire  $\overline{\text{CS}}$  Mode With a Busy Indicator

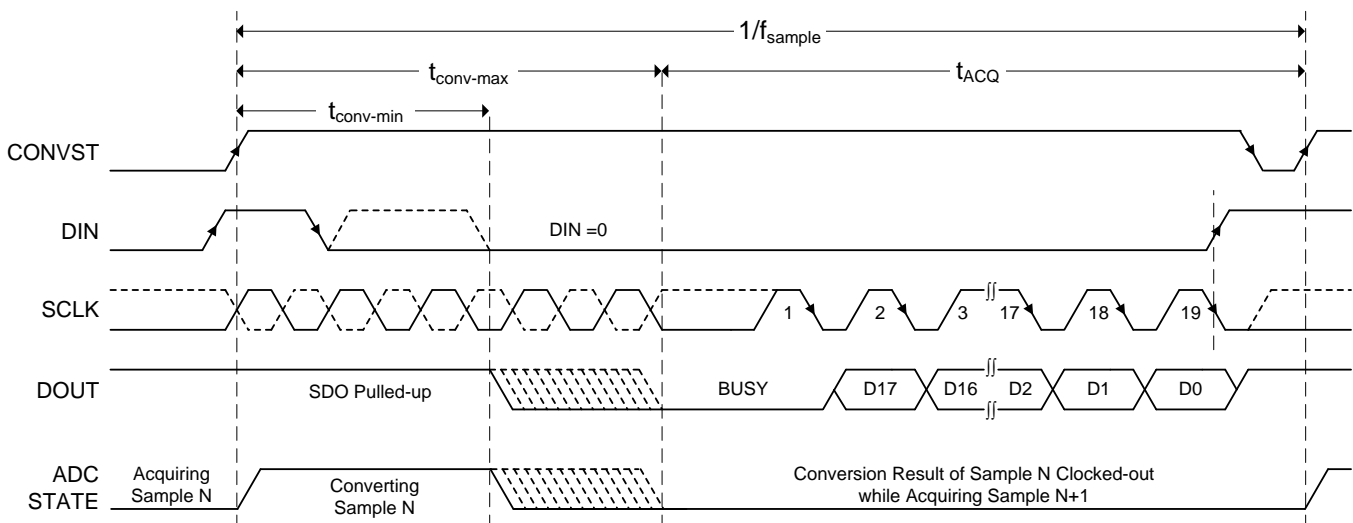


Figure 59. Interface Timing Diagram: 4-Wire  $\overline{\text{CS}}$  Mode With a Busy Indicator

## Device Functional Modes (continued)

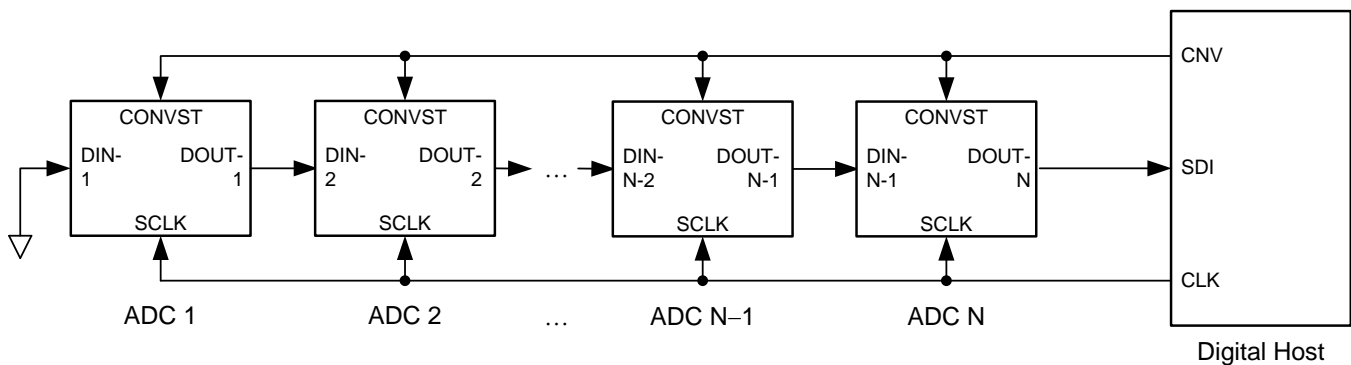
When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the  $\overline{\text{IRQ}}$  pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the  $t_{h\_CK\_DO\_min}$  time frame. DOUT goes to 3-state after the 19th SCLK falling edge or when DIN goes high, whichever occurs first. Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

### 9.4.2 Daisy-Chain Mode

Daisy-chain mode is selected if DIN is low at the time of a CONVST rising edge or if DIN and CONVST are connected together. Similar to  $\overline{\text{CS}}$  mode, this mode features operation with or without a busy indicator. The following sections discuss these interface modes in detail.

#### 9.4.2.1 Daisy-Chain Mode Without a Busy Indicator

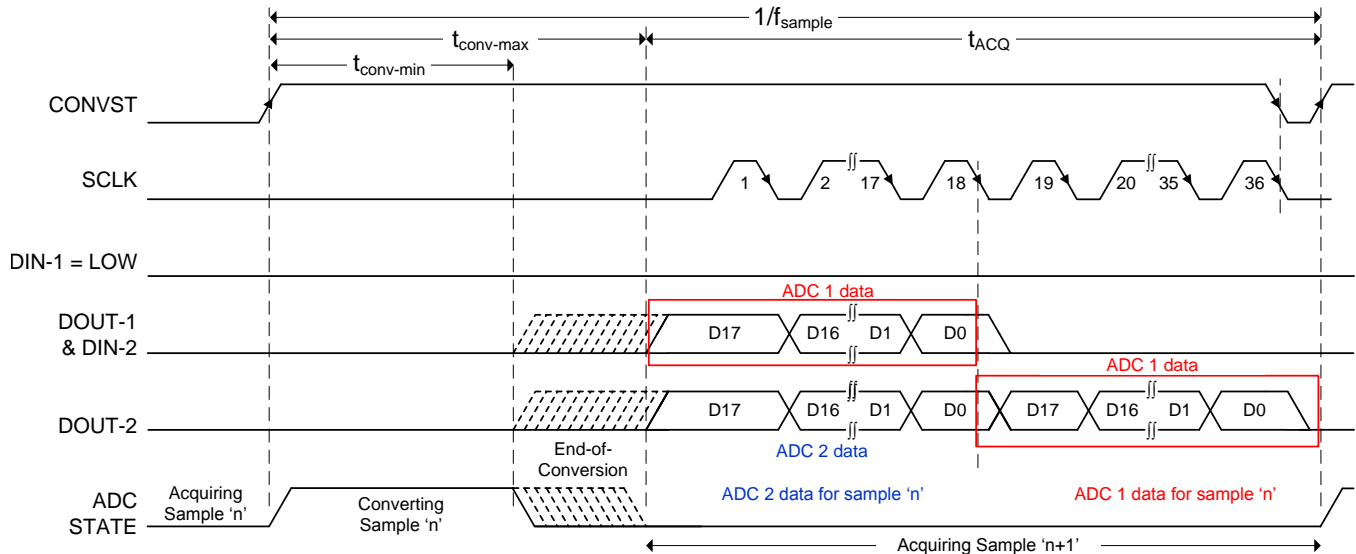
This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability. Figure 60 shows a connection diagram with  $N$  ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to GND. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI pin of the digital host.



**Figure 60. Connection Diagram: Daisy-Chain Mode Without a Busy Indicator (DIN = 0)**

### Device Functional Modes (continued)

As shown in Figure 61, the device DOUT pin is driven low when DIN and CONVST are low together. With DIN low, a CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be low at the CONVST rising edge so that the device does not generate a busy indicator at the end of the conversion.



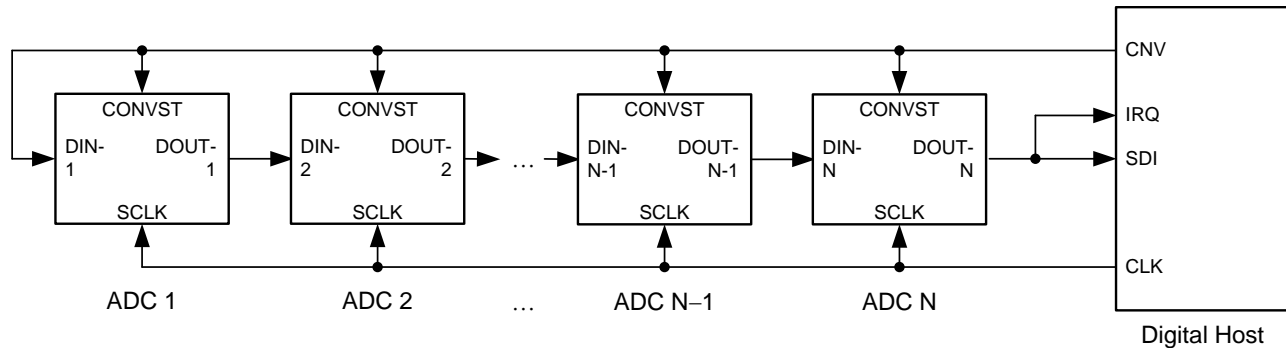
**Figure 61. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode**

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 18-bit, shift register and also outputs the MSB bit of this conversion result on its own DOUT pin. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the data of ADC N, followed by the data of ADC N-1, and so on (in MSB-first fashion). A total of  $18 \times N$  SCLK falling edges are required to capture the outputs of all N devices in the chain. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the  $t_{h\_CK\_DO-min}$  time frame.

## Device Functional Modes (continued)

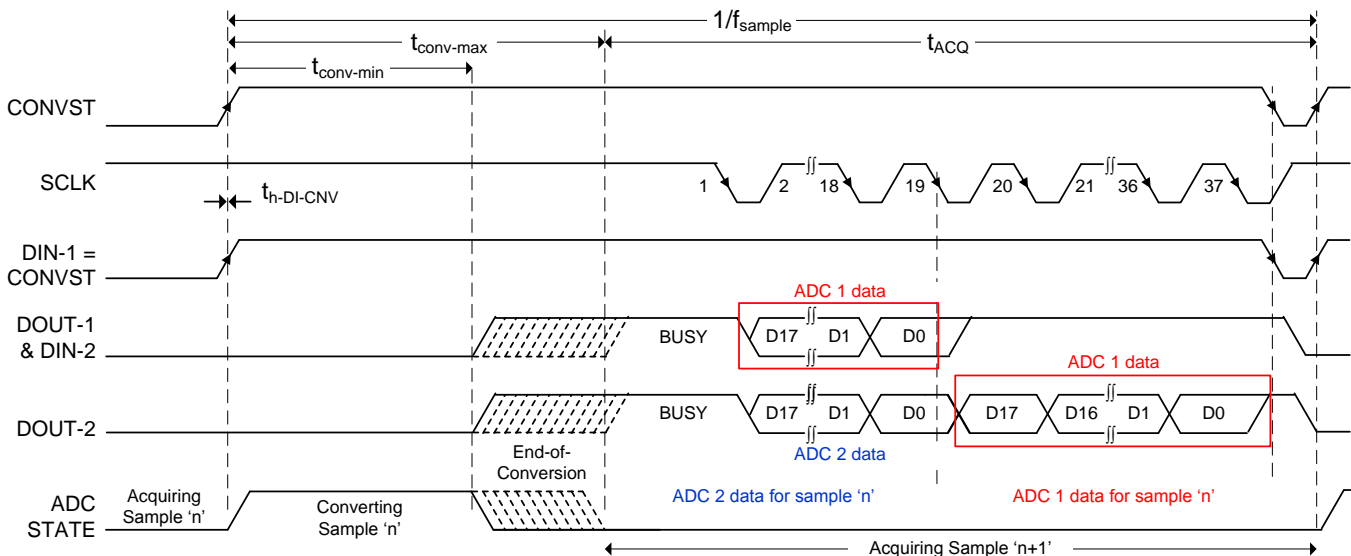
### 9.4.2.2 Daisy-Chain Mode With a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability and an interrupt-driven data transfer is desired. Figure 62 shows a connection diagram with  $N$  ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to its CONVST. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI and IRQ pins of the digital host.



**Figure 62. Connection Diagram: Daisy-Chain Mode With a Busy Indicator (DIN = 0)**

As shown in Figure 63, the device DOUT pin is driven low when DIN and CONVST are low together. A CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be high at the CONVST rising edge so that the device generates a busy indicator at the end of the conversion.



**Figure 63. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode With a Busy Indicator**



## Device Functional Modes (continued)

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 18-bit, shift register and also forces its DOUT pin high, thereby providing a low-to-high transition on the IRQ pin of the digital host. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the interrupt signal followed by the data of ADC N followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of  $(18 \times N) + 1$  SCLK falling edges are required to capture the outputs of all  $N$  devices in the chain. Fast sampling rates require a high-frequency SCLK and data must be read at the SCLK falling edges. For slow sampling rates and SCLK frequency  $\leq 36$  MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at the SCLK falling edge requires the digital host to clock in the data during the  $t_{h\_CK\_DO-min}$  time frame. Note that the busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

NOTE: For SCLK  $\leq 36$  MHz, SPI mode-3 (CPOL = 1, CPHA = 1) allows reading the conversion results of  $N$  ADCs in  $18 \times N$  SCLK cycles because the busy indicator bit is not clocked in by the host.

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by some application circuits designed using the ADS8881.

#### 10.1.1 ADC Reference Driver

The external reference source to the ADS8881 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few hundred  $\mu V_{RMS}$ . Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of  $V_{REF}$  stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor,  $C_{BUF\_FLT}$  (see [Figure 48](#)) for regulating the voltage at the reference input of the ADC. The amplifier selected to drive the reference pin must have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pin without any stability issues.

#### 10.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 18-bit ADC such as the ADS8881.

## Application Information (continued)

### 10.1.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (see the [Antialiasing Filter](#) section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier bandwidth as described in [Equation 2](#):

$$\text{Unity - Gain Bandwidth} \geq 4 \times \left( \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (2)$$

- **Noise.** Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in [Equation 3](#).

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{\left( \frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu V$ ,
- $e_{n\_RMS}$  is the amplifier broadband noise density in  $nV/\sqrt{Hz}$ ,
- $f_{-3dB}$  is the 3-dB bandwidth of the RC filter, and
- $N_G$  is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration. (3)
- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in [Equation 4](#).

$$\text{THD}_{AMP} \leq \text{THD}_{ADC} - 10 \text{ (dB)} \quad (4)$$

- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA™-SPICE simulations before selecting the amplifier.

### 10.1.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the inputs of the ADC during the small acquisition time window. For ac signals, keep the filter bandwidth low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.

## Application Information (continued)

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A differential filter capacitor,  $C_{FLT}$ , is connected across the inputs of the ADC (as shown in Figure 64). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor must be at least 10 times the specified value of the ADC sampling capacitance. For the ADS8881, the input sampling capacitance is equal to 59 pF, thus the value of  $C_{FLT}$  must be greater than 590 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

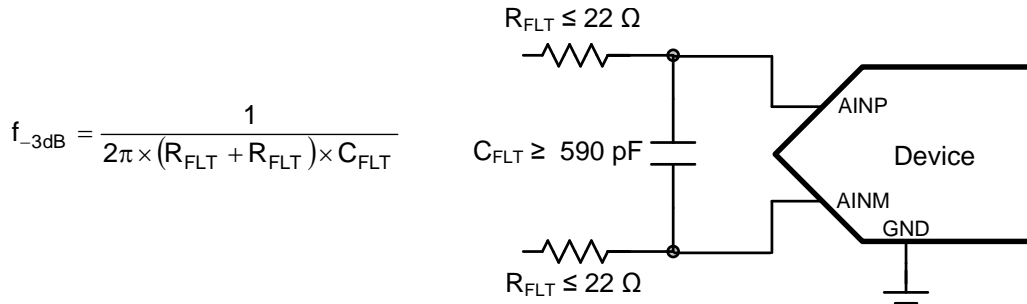


Figure 64. Antialiasing Filter

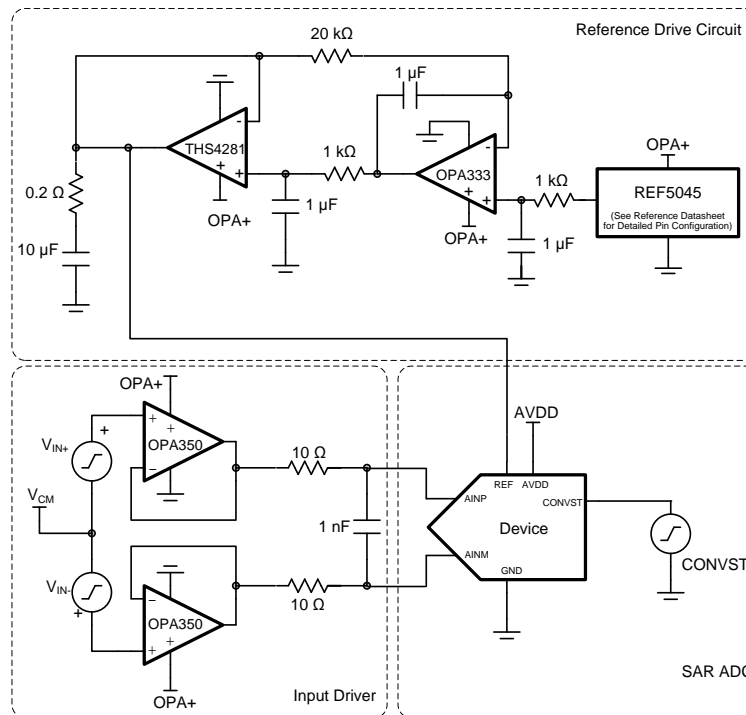
Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{FLT}$ ) are used at the output of the amplifiers. A higher value of  $R_{FLT}$  is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{FLT}$  requires balancing the stability and distortion of the design. For the ADS8881, TI recommends limiting the value of  $R_{FLT}$  to a maximum of 22  $\Omega$  in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth must be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22- $\Omega$  resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

This section describes some common application circuits using the ADS8881. These data acquisition (DAQ) blocks are optimized for specific input types and performance requirements of the system. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the [Power Supply](#) section for suggested guidelines.

## 10.2 Typical Applications

### 10.2.1 DAQ Circuit for a 1- $\mu$ s, Full-Scale Step Response



**Figure 65. DAQ Circuit for a 1- $\mu$ s, Full-Scale Step Response**

#### 10.2.1.1 Design Requirements

Step input signals are common in multiplexed applications when switching between different channels. In a worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched.

Design an application circuit optimized for using the ADS8881 to achieve

- full-scale step input settling to 18-bit accuracy and
- INL of  $< \pm 2$  LSB and
- maximum specified throughput of 1 MSPS

#### 10.2.1.2 Detailed Design Procedure

The application circuit is shown in [Figure 65](#).

In such applications, the primary design requirement is to ensure that the full-scale step input signal settles to 18-bit accuracy at the ADC inputs. This condition is critical to achieve the excellent linearity specifications of the ADC. Therefore, the bandwidth of the antialiasing RC filter must be large enough to allow optimal settling of the input signal during the ADC acquisition time. The filter capacitor helps reduce the sampling charge injection at the ADC inputs, but degrades the phase margin of the driving amplifier, thereby leading to stability issues. Amplifier stability is maintained by the series isolation resistor.

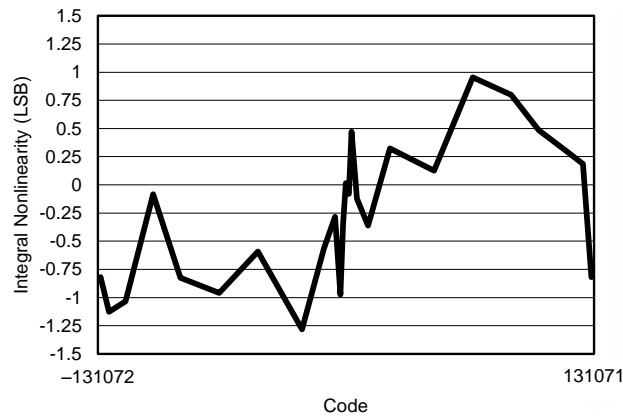
The application circuit in [Figure 65](#) shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

**Typical Applications (continued)**

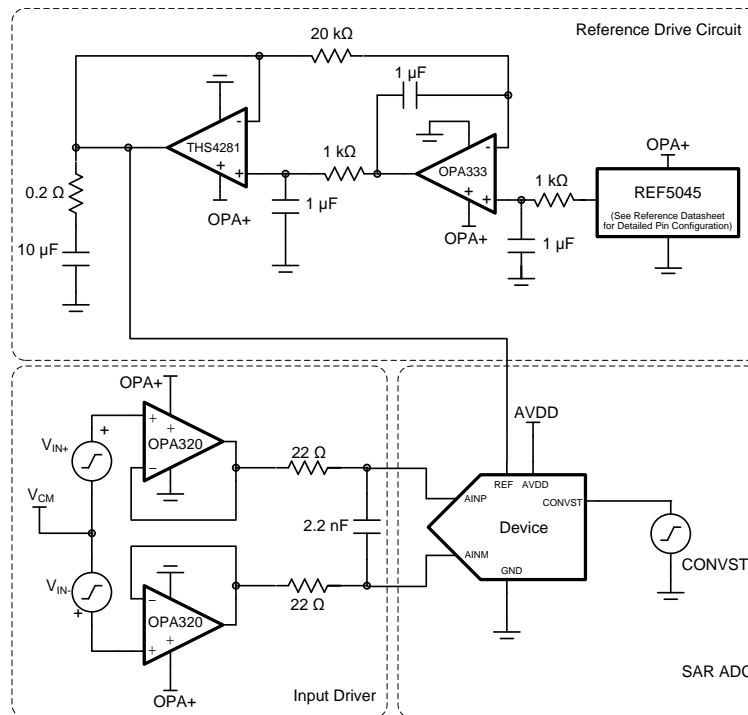
The reference buffer is designed with the [THS4281](#) and [OPA333](#) in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

For the input driving amplifiers, key specifications include rail-to-rail input and output swing, high bandwidth, high slew rate, and fast settling time. The [OPA350](#) CMOS amplifier meets all these specification requirements for this circuit with a single-supply and low quiescent current. The component values of the antialiasing filter are selected to meet the settling requirements of the system as well as to maintain the stability of the input driving amplifiers.

**10.2.1.3 Application Curve**



## 10.2.2 Low-Power DAQ Circuit for Excellent Dynamic Performance at 1 MSPS



**Figure 67. DAQ Circuit for Lowest Power and Excellent Dynamic Performance at 1 MSPS**

### 10.2.2.1 Design Requirements

Design an application circuit optimized for using the ADS8881 to achieve

- ENOB > 17 bits and
- < 35 mW of total power consumption and
- maximum specified throughput of 1 MSPS

### 10.2.2.2 Detailed Design Procedure

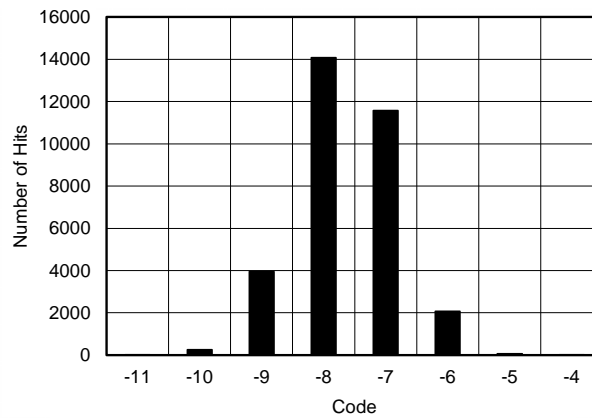
The application circuit in [Figure 67](#) shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1  $\Omega$  at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

In such applications, the input driver must be low in power and noise as well as able to support rail-to-rail input and output swing with a single supply. A high amplifier bandwidth is also preferred to help attenuate high-frequency distortion. However, oftentimes bandwidth and noise are traded off with the power consumption of the amplifier. This circuit uses the OPA320 as the front-end driving amplifier because this device has a relatively low noise density of 7 nV/ $\sqrt{\text{Hz}}$  for a maximum-specified quiescent current of 1.45 mA per channel.

The noise contribution from the front-end amplifier is band-limited by the 3-dB bandwidth of the RC filter and is designed to be 1.65 MHz in this application. Again, the component values of the antialiasing filter are carefully selected to maintain the stability of the input driving amplifiers.

**10.2.2.3 Application Curve**



$V_{diff}$  close to 0 V, 32768 data points, standard deviation = 0.82 bits,  
ENOB (dc) = 17.18 bits

**Figure 68. DC Input Histogram**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see [18-Bit, 1-MSPS Data Acquisition \(DAQ\) Block Optimized for Lowest Power \(SLAU513\)](#).

10.2.3 DAQ Circuit for Lowest Distortion and Noise Performance at 1 MSPS

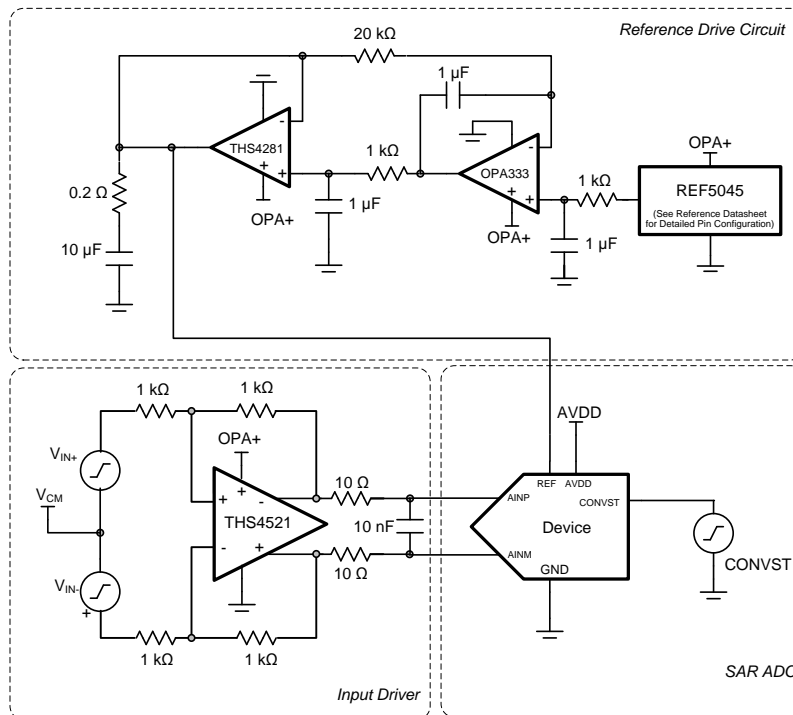


Figure 69. Differential Input DAQ Circuit for Lowest Distortion and Noise at 1 MSPS

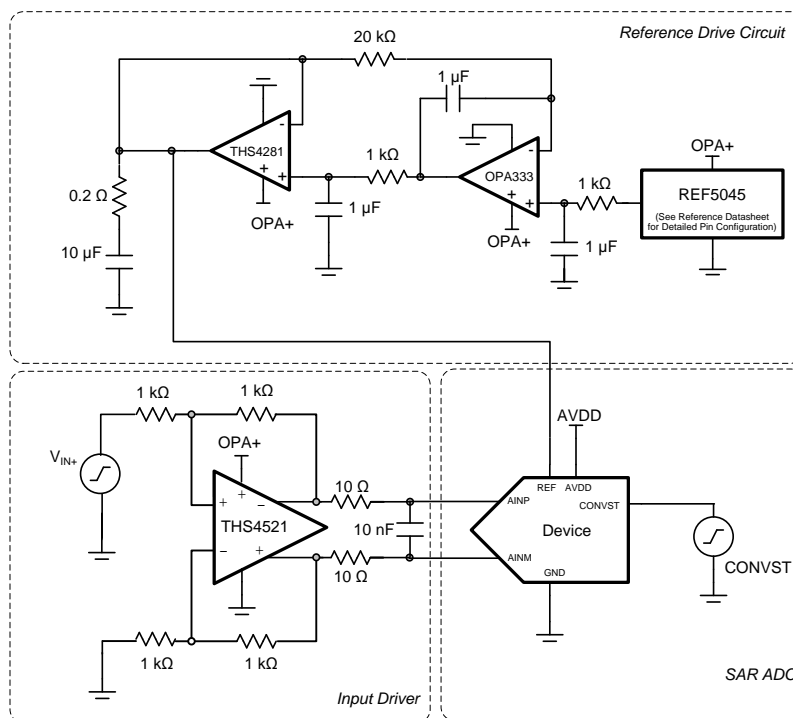


Figure 70. Single-Ended to Differential DAQ Circuit for Lowest Distortion and Noise at 1 MSPS



### 10.2.3.1 Design Requirements

Design an application circuit optimized for using the ADS8881 to achieve

- > 98.5-dB SNR, < -110-dB THD and
- $\pm 1.5$ -LSB linearity and
- maximum specified throughput of 1 MSPS

### 10.2.3.2 Detailed Design Procedure

The application circuits are shown in [Figure 69](#) and [Figure 70](#). In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in an inverting gain configuration and a low-pass RC filter before being fed into the ADC.

The reference driver circuit, shown in [Figure 69](#) and [Figure 70](#), generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise [REF5045](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

The reference buffer is designed with the [THS4281](#) and [OPA333](#) in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1  $\Omega$  at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

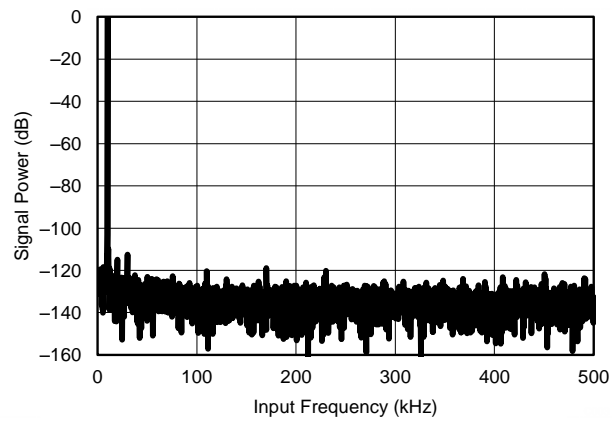
As a rule of thumb, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power [THS4521](#) as an input driver that provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

The circuit in [Figure 69](#) shows a fully-differential DAQ block optimized for low distortion and noise using the THS4521 and ADS8881. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4521 (not shown in [Figure 69](#)). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider. However, note that the ADS8881 allows the common-mode input voltage ( $V_{CM}$ ) to be set to any value in the range of 0 V to  $V_{REF}$ .

The circuit in [Figure 70](#) shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4521 and the ADS8881. This front-end circuit configuration requires a single-ended ac signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4521 (not shown in [Figure 70](#)). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider. However, note that the ADS8881 allows the common-mode input voltage ( $V_{CM}$ ) to be set to any value in the range of 0 V to  $V_{REF}$ .

10.2.3.3 Application Curve



$f_{IN} = 10 \text{ kHz}$ , SNR = 99 dB, THD = -112 dB

Figure 71. FFT Plot



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see [18-Bit, 1-MSPS Data Acquisition \(DAQ\) Block Optimized for Lowest Distortion and Noise \(SLAU515\)](#).

### 10.2.4 Ultralow-Power DAQ Circuit at 10 kSPS

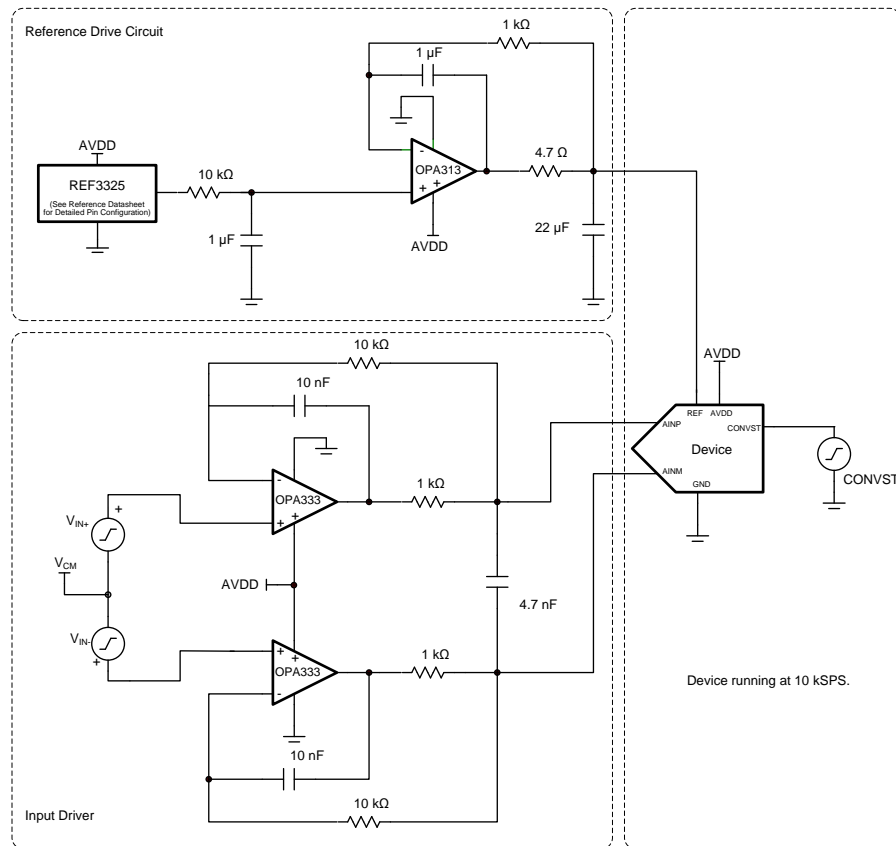


Figure 72. Ultralow-Power DAQ Circuit at 10 kSPS

#### 10.2.4.1 Design Requirements

Portable and battery-powered applications require ultralow-power consumption and do not need very high throughput from the ADC.

Design a single-supply, data acquisition circuit optimized for using the ADS8881 to achieve

- ENOB > 16 bits and
- Ultralow-power consumption of < 1 mW at throughput of 10 kSPS.

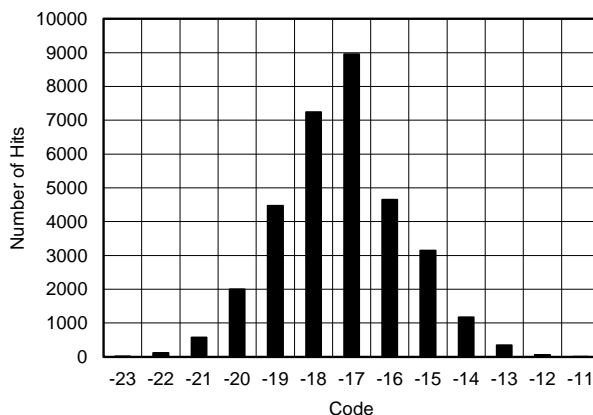
#### 10.2.4.2 Detailed Design Procedure

The application circuit in Figure 72 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5 V dc using a single 3.3-V supply. This ultralow power reference block is suitable to drive the ADS8881 for power-sensitive applications at a relatively lower throughput. This design uses the high-precision REF3325 circuit that provides an accurate 2.5-V reference voltage at an extremely low quiescent current of 5 μA. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

The reference buffer is designed with the low-power OPA313 that can operate from a 3.3-V supply at an extremely low quiescent current of 50 μA. The wideband noise contribution from the amplifier is limited by a lowpass filter of a cutoff frequency equal to 1.5 kHz, formed by a 4.7-Ω resistor in combination with a 22-μF capacitor. The 4.7-Ω series resistor creates an additional drop in the reference voltage that is corrected by a dual-feedback configuration.

The input driver circuit uses extremely low-power, dual amplifiers (such as the [OPA2333](#)) with a maximum quiescent current of 28  $\mu\text{A}$  per channel to drive the ADC inputs. The input amplifiers are configured in a modified unity-gain buffer configuration. The filter capacitor at the ADC inputs attenuates the sampling charge-injection noise from the ADC but effects the stability of the input amplifiers by degrading the phase margin. This attenuation requires a series isolation resistor to maintain amplifier stability. The value of the series resistor is directly proportional to the open-loop output impedance of the driving amplifier to maintain stability, which is high (in the order of  $\text{k}\Omega$ ) in the case of low-power amplifiers such as the [OPA333](#). Therefore, a high value of 1  $\text{k}\Omega$  is selected for the series resistor at the ADC inputs. However, this series resistor creates an additional voltage drop in the signal path, thereby leading to linearity and distortion issues. The dual-feedback configuration used in [Figure 72](#) corrects for this additional voltage drop and maintains system performance at ultralow-power consumption.

**10.2.4.3 Application Curve**



$V_{diff}$  close to 0 V, 32768 data points, standard deviation = 1.7 bits,  
ENOB (dc) = 16.3 bits

**Figure 73. DC Input Histogram**



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see [18-Bit, 10kSPS Data Acquisition \(DAQ\) Block Optimized for Ultra Low Power < 1mW \(SLAU514\)](#).

## 11 Power-Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

### 11.1 Power-Supply Decoupling

Decouple the AVDD and DVDD pins with GND, using individual 1- $\mu$ F decoupling capacitors placed in close proximity to the pin, as shown in Figure 74.

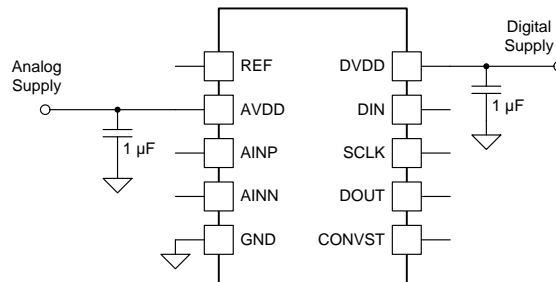


Figure 74. Supply Decoupling

### 11.2 Power Saving

The device has an auto power-down feature that powers down the internal circuitry at the end of every conversion. Referring to Figure 75, the input signal is acquired on the sampling capacitors when the device is in a power-down state ( $t_{acq}$ ); at the same time, the result for the previous conversion is available for reading. The device powers up on the start of the next conversion. During conversion phase ( $t_{conv}$ ), the device also consumes current from the reference source (connected to the REF pin).

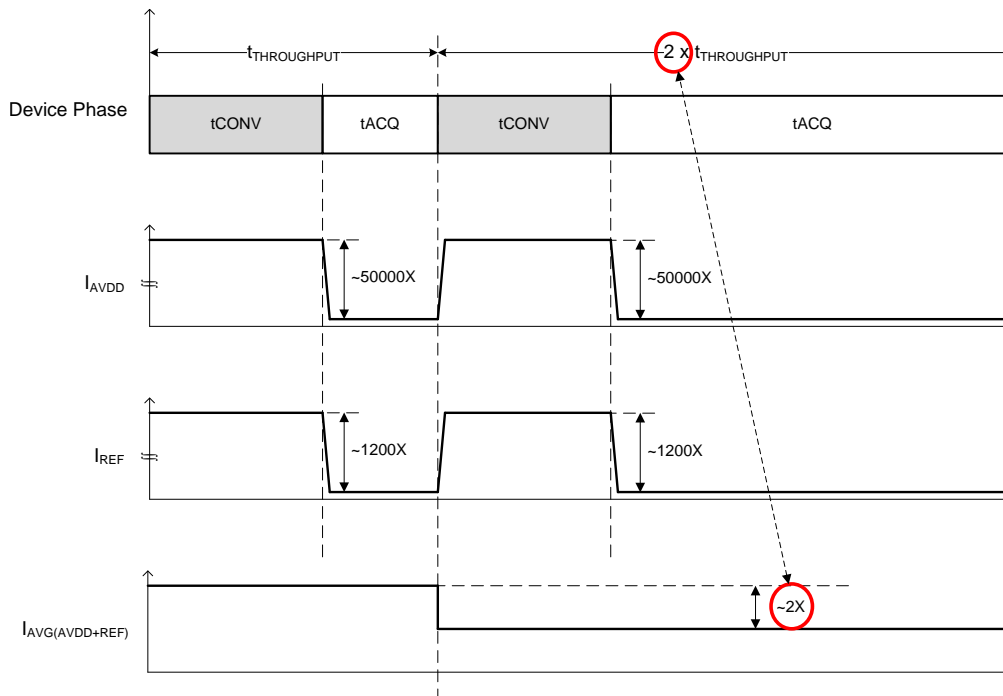
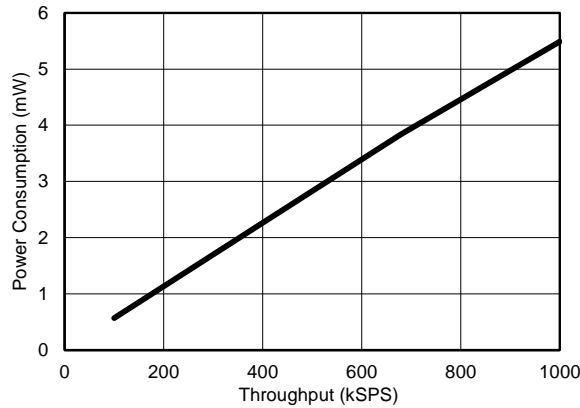


Figure 75. Power Scaling With Throughput

**Power Saving (continued)**

The conversion time,  $t_{conv}$ , is independent of the SCLK frequency. When operating the device at speeds lower than the maximum rated throughput, the conversion time,  $t_{conv}$ , does not change; the device spends more time in power-down state. Therefore, as shown in [Figure 76](#), the device power consumption from the AVDD supply and the external reference source is directly proportional to the speed of operation. Extremely low AVDD power-down current (50 nA, typical) and extremely low external reference leakage current (250 nA, typical), make this device ideal for very low throughput applications (such as pulsed measurements).



**Figure 76. Power Scaling With Throughput**

## 12 Layout

### 12.1 Layout Guidelines

Figure 77 shows a board layout example for the device. Appropriate layout that interconnects accompanying capacitors and converters with low inductance is critical for achieving optimum performance. Thus, a PCB board with at least four layers is recommended to keep all critical components on the top layer and interconnected to a solid (low inductance) analog ground plane at the subsequent inner layer using 15-mil vias. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 77, the analog input and reference input signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

As a result of dynamic currents during conversion and data transfer, each supply pin (AVDD and DVDD) must have a decoupling capacitor to keep the supply voltage stable. To maximize decoupling capabilities, inductance between each supply capacitor and the supply pin of the converter is kept less than 5 nH by placing the capacitor within 0.2-inches from the pin and connecting it with 20-mil traces and a 15-mil grounding via, as shown in Figure 77. TI recommends using one 1- $\mu$ F ceramic capacitor at each supply pin. Avoid placing vias between the supply pin and its decoupling capacitor.

Dynamic currents are also present at the REF pin during the conversion phase and very good decoupling is critical to achieve optimum performance. The inductance between the reference capacitor and the REF pin is kept less than 2 nH by placing the capacitor within 0.1-inches from the pin and connecting it with 20-mil traces and multiple 15-mil grounding vias, as shown in Figure 77. A single, 10- $\mu$ F, X7R-grade, 0805-size, ceramic capacitor with at least a 10-V rating is recommended for good performance over the rated temperature range. Avoid using additional lower value capacitors because the interactions between multiple capacitors may affect the ADC performance at higher sampling rates. A small, 0.1- $\Omega$  to 0.47- $\Omega$ , 0603-size resistor placed in series with the reference capacitor (as shown in Figure 77) keeps the overall impedance low and constant, especially at very high frequencies.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

### 12.2 Layout Example

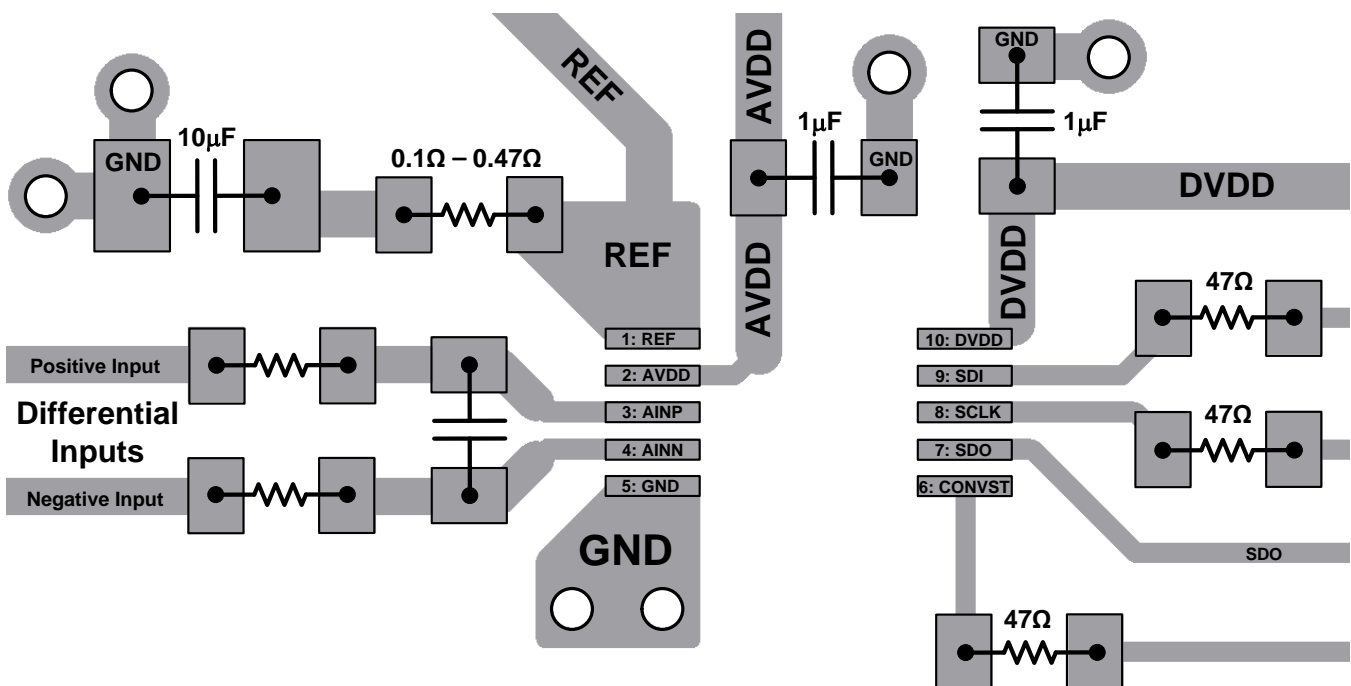


Figure 77. Recommended Layout

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

- TIPD117 验证设计参考指南: 《适用于多路复用器和步进输入的数据采集 (18 位、1 $\mu$ s 满量程响应) 参考设计》, [TIDU012](#)
- TIPD113 验证设计参考指南: 《数据采集参考设计 (10kHz 交流、35mW、18 位、1MSPS)》, [SLAU513](#)
- TIPD114 验证设计参考指南: 《数据采集参考设计 (1kHz 交流、1mW、18 位、1MSPS)》, [SLAU514](#)
- TIPD115 验证设计参考指南: 《针对最低失真和最低噪声进行优化的 18 位、1MSPS 数据采集参考设计》, [SLAU515](#)
- TIPD116 验证设计参考指南: 《适用于 ECG 系统的数据采集模块 (离散 LEAD I ECG 实施方案) 参考设计》, [SLAU516](#)
- 《OPA313 数据表》, [SBOS649](#)
- 《OPA333、OPA2333 数据表》, [SBOS351](#)
- 《OPA350 数据表》, [SBOS099](#)
- 《THS4521 数据表》, [SBOS458](#)
- 《THS4281 数据表》 (文献编号 [SLOS432](#))
- Precision Hub:
  - 使用 SAR ADC TINA 模型: 静态特性, 功率调节
  - 使用 SAR ADC TINA 模型: 关于稳定性的诸多问题
  - SAR ADC 响应时间: 迅速响应, 迅速控制
  - SAR ADC 输入的相关注意事项

### 13.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件, 并且可以快速访问样片或购买链接。

表 7. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS8881C	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
ADS8881I	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 商标

E2E is a trademark of Texas Instruments.

TINA is a trademark of Texas Instruments Inc..

SPI is a trademark of Motorola Inc.

All other trademarks are the property of their respective owners.



### 13.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8881CDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	<a href="#">Samples</a>
ADS8881CDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	<a href="#">Samples</a>
ADS8881CDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	<a href="#">Samples</a>
ADS8881CDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	<a href="#">Samples</a>
ADS8881IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	<a href="#">Samples</a>
ADS8881IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	<a href="#">Samples</a>
ADS8881IDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	<a href="#">Samples</a>
ADS8881IDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8881CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8881DRRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8881CDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8881CDRCT	VSON	DRC	10	250	210.0	185.0	35.0
ADS8881IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8881IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8881IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

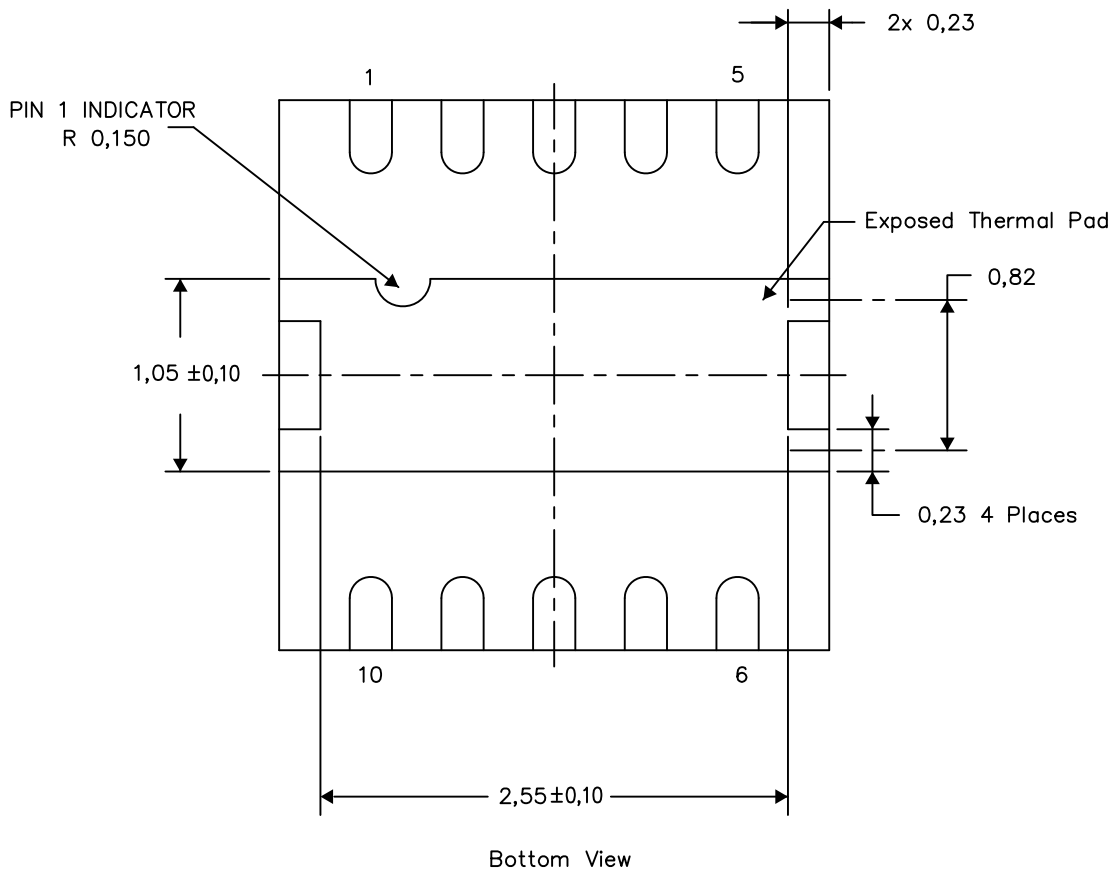
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206565-6/Y 08/15

NOTE: A. All linear dimensions are in millimeters



DGS (S-PDSO-G10)

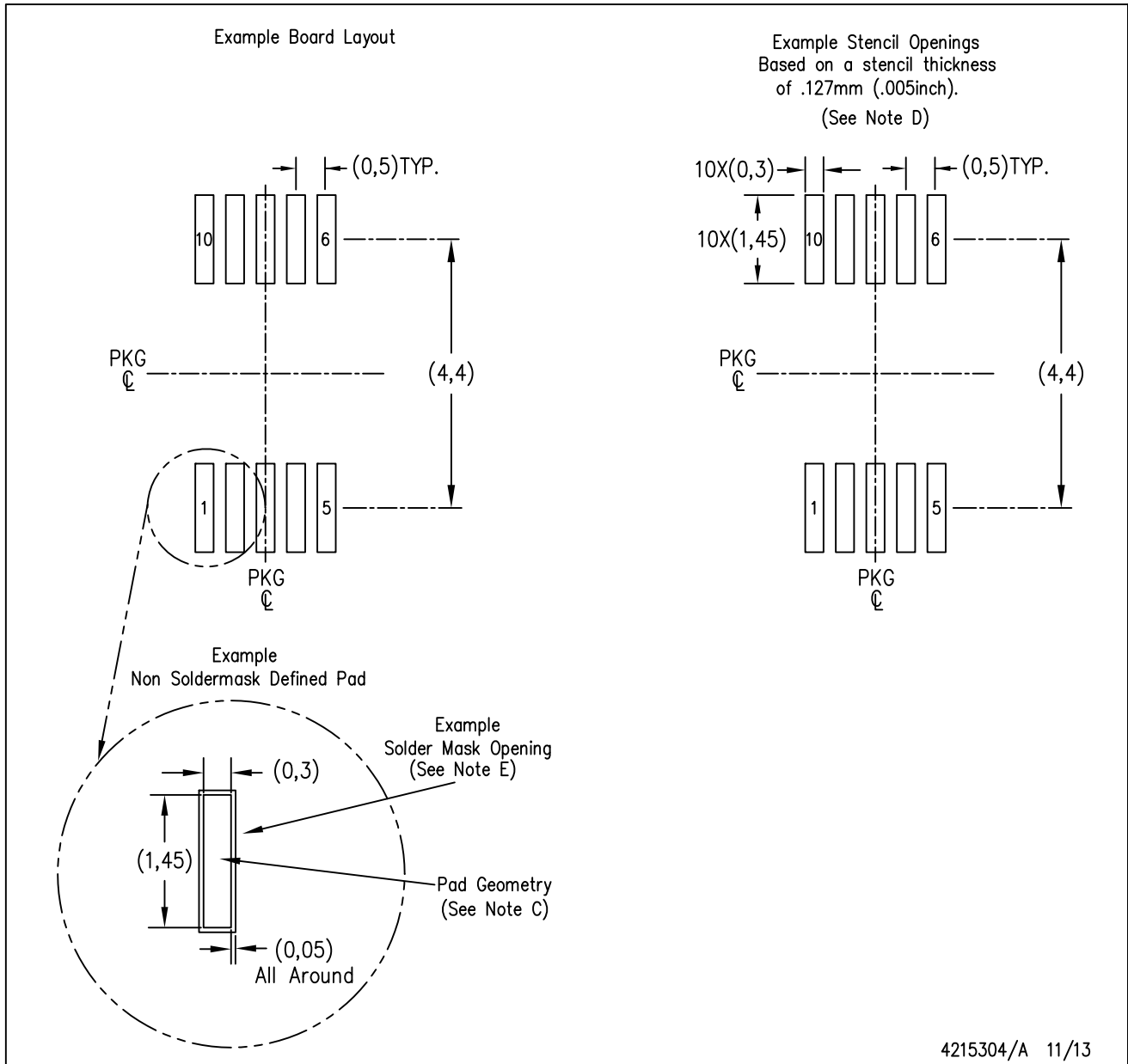
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或暗示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与美国 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认为的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2017 德州仪器半导体技术（上海）有限公司