

# ADS7041 超低功耗、超小尺寸、10 位、1MSPS、SAR ADC

## 1 特性

- 业界第一款具有毫微瓦功耗的逐次逼近寄存器 (SAR) 模数转换器 (ADC):
  - 1MSPS 和 1.8V AVDD 时为 189 $\mu$ W
  - 1MSPS 和 3V AVDD 时为 600 $\mu$ W
  - 100kSPS 和 3V AVDD 时为 60 $\mu$ W
  - 1kSPS 和 3V AVDD 时低于 1 $\mu$ W
- 业界最小的 SAR ADC:
  - 采用 X2QFN-8 封装, 封装尺寸为 2.25mm<sup>2</sup>
- 1MSPS 吞吐量且零延迟
- 宽工作范围:
  - AVDD: 1.65V 到 3.6V
  - DVDD: 1.65V 至 3.6V (与 AVDD 无关)
  - 温度范围: -40°C 至 125°C
- 出色的性能:
  - 10 位分辨率且无丢码 (NMC)
  - 最大  $\pm 0.8$  最低有效位 (LSB) 的积分非线性 (INL), 最大  $\pm 0.7$  最低有效位 (LSB) 的差分非线性 (DNL)
  - 61dB 的信噪比 (SNR) (3V AVDD 时)
  - 75dB 的总谐波失真 (THD) (3V AVDD 时)
- 单极输入范围: 0V 至 AVDD
- 集成偏移校准
- 串行外设接口 (SPI)<sup>™</sup>- 兼容串口: 14MHz
- 符合 JESD8-7A 标准的数字 I/O

## 2 应用

- 低功耗数据采集
- 电池供电类手持设备
- 液位传感器
- 超声波流量计
- 电机控制
- 可穿戴健身器
- 便携式医疗设备
- 硬盘
- 血糖仪

## 3 说明

ADS7041 是一款 10 位、1MSPS、模数转换器 (ADC)。该器件支持较宽的模拟输入电压范围 (1.65V 到 3.6V), 并包含一个基于电容且内置采样保持电路的逐次逼近寄存器 (SAR) ADC。串行外设接口 (SPI) 兼容串口由  $\overline{CS}$  和 SCLK 信号控制。输入信号在  $\overline{CS}$  下降沿进行采样, SCLK 用于转换和串行数据输出。此器件支持宽范围的数字电源 (1.65V 至 3.6V), 可直接连接到各类主机控制器。ADS7041 符合 JESD8-7A 标准的标称 DVDD 范围 (1.65V 至 1.95V)。

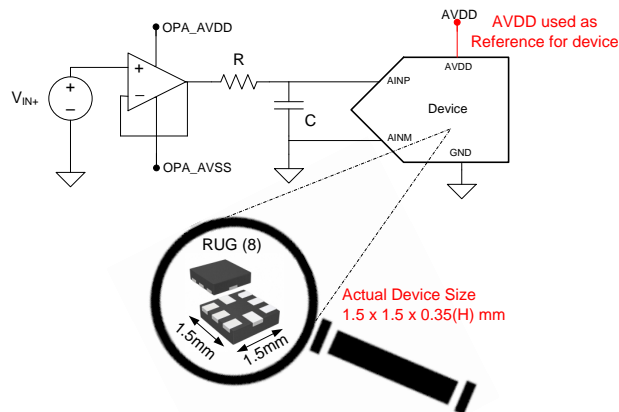
ADS7041 采用 8 引脚微型引线 X2QFN 封装, 额定工作温度范围为 -40°C 至 125°C。此器件尺寸微小且功耗极低, 非常适合空间受限类电池供电应用。

器件信息(1)

部件名称	封装	封装尺寸 (标称值)
ADS7041	X2QFN (8)	1.50mm x 1.50mm
	超薄小外形尺寸封装 (VSSOP)(8)	2.30mm x 2.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

## 典型应用



注: ADS7041 比 0805 (2012 公制) SMD 元件小。



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (February 2015) to Revision C	Page
• Updated <a href="#">Figure 1</a> .....	7
• Changed <i>Serial Interface</i> section: changed last half of first paragraph, changed <a href="#">Figure 35</a> .....	18
• Changed <a href="#">Figure 38</a> .....	21
• 添加了社区资源部分 .....	32

Changes from Revision A (November 2014) to Revision B	Page
• 已更改 宽工作电压范围 特性 要点：已将 AVDD 的值从 1.8V 改为 1.65V .....	1
• 已更改 宽模拟输入电压范围下限至 1.65V（说明部分第 1 段） .....	1
• Changed <i>ESD Ratings</i> table to latest standards .....	5
• Changed AVDD parameter minimum specification in <i>Recommended Operating Conditions</i> table to 1.65 V .....	5
• Changed AVDD range in conditions of <i>Electrical Characteristics</i> table .....	6
• Changed INL and DNL parameter test conditions in <i>Electrical Characteristics</i> table .....	6
• Changed E <sub>O</sub> parameter calibrated test conditions in <i>Electrical Characteristics</i> table .....	6
• Changed maximum throughput rate parameter test conditions in <i>Electrical Characteristics</i> table .....	6
• Changed AVDD parameter minimum specification in <i>Electrical Characteristics</i> table .....	6
• Changed conditions for <i>Timing Characteristics</i> table: changed range of AVDD and added C <sub>LOAD</sub> condition .....	7
• Changed t <sub>D_CKDO</sub> parameter in <i>Timing Characteristics</i> table .....	7
• Added f <sub>SCLK</sub> minimum specification to <i>Timing Characteristics</i> table .....	7
• Changed titles of <a href="#">Figure 26</a> to <a href="#">Figure 30</a> .....	11
• Changed <i>Reference</i> sub-section in <i>Feature Description</i> section .....	15
• Changed range of second f <sub>CLK-CAL</sub> parameter description in <a href="#">Table 2</a> .....	20
• Changed range of second f <sub>CLK-CAL</sub> parameter description in <a href="#">Table 3</a> .....	21
• Changed <i>Reference Circuit</i> section in <i>Application Information</i> .....	24

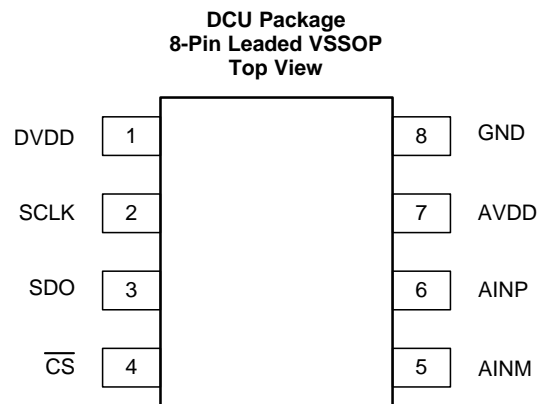
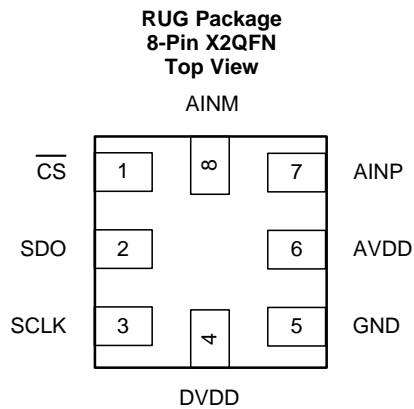
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- Added last two sentences to *AVDD and DVDD Supply Recommendations* section ..... 30
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**Changes from Original (November 2014) to Revision A**

**Page**

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- 已更改产品预览数据表..... 1
-

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	RUG	DCU		
AINM	8	5	Analog input	Analog signal input, negative
AINP	7	6	Analog input	Analog signal input, positive
AVDD	6	7	Supply	Analog power-supply input, also provides the reference voltage to the ADC
$\overline{\text{CS}}$	1	4	Digital input	Chip-select signal, active low
DVDD	4	1	Supply	Digital I/O supply voltage
GND	5	8	Supply	Ground for power supply, all analog and digital signals are referred to this pin
SCLK	3	2	Digital input	Serial clock
SDO	2	3	Digital output	Serial data out

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

	MIN	MAX	UNIT
AVDD to GND	−0.3	3.9	V
DVDD to GND	−0.3	3.9	V
AINP to GND	−0.3	AVDD + 0.3	V
AINM to GND	−0.3	0.3	V
Digital input voltage to GND	−0.3	DVDD + 0.3	V
Storage temperature, T <sub>stg</sub>	−60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
AVDD	Analog supply voltage range	1.65	3.6	V
DVDD	Digital supply voltage range	1.65	3.6	V
T <sub>A</sub>	Operating free-air temperature	−40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS7041		UNIT
		RUG (X2QFN)	DCU (VSSOP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	177.5	235.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	51.5	79.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	76.7	117.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.0	8.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	76.7	116.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

At  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 1.65\text{ V}$  to  $3.6\text{ V}$ ,  $DVDD = 1.65\text{ V}$  to  $3.6\text{ V}$ ,  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , and  $V_{\text{AINM}} = 0\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
Full-scale input voltage span <sup>(1)</sup>			0		AVDD	V
Absolute input voltage range	AINP to GND		-0.1		AVDD + 0.1	V
	AINM to GND		-0.1		0.1	
$C_S$	Sampling capacitance			15		pF
<b>SYSTEM PERFORMANCE</b>						
	Resolution			10		Bits
NMC	No missing codes		10			Bits
INL	Integral nonlinearity	AVDD = 1.8 V to 3.6 V	-0.8	±0.4	0.8	LSB <sup>(2)</sup>
DNL	Differential nonlinearity	AVDD = 1.8 V to 3.6 V	-0.7	±0.4	0.7	LSB
$E_O$	Offset error	Uncalibrated		±3		LSB
		Calibrated <sup>(3)</sup>	AVDD = 1.8 V to 3.6 V	-2	±0.5	
$dV_{OS}/dT$	Offset error drift with temperature			10		ppm/°C
$E_G$	Gain error		-0.2	±0.1	0.2	%FS
	Gain error drift with temperature			±10		ppm/°C
<b>SAMPLING DYNAMICS</b>						
$t_{ACQ}$	Acquisition time		235			ns
	Maximum throughput rate	14-MHz SCLK, AVDD = 1.65 V to 3.6 V			1	MHz
<b>DYNAMIC CHARACTERISTICS</b>						
SNR	Signal-to-noise ratio <sup>(4)</sup>	$f_{IN} = 2\text{ kHz}$ , AVDD = 3 V	60	61		dB
		$f_{IN} = 2\text{ kHz}$ , AVDD = 1.8 V		60		
THD	Total harmonic distortion <sup>(4)(5)</sup>	$f_{IN} = 2\text{ kHz}$ , AVDD = 3 V		-75		dB
SINAD	Signal-to-noise and distortion <sup>(4)</sup>	$f_{IN} = 2\text{ kHz}$ , AVDD = 3 V	60	61		dB
		$f_{IN} = 2\text{ kHz}$ , AVDD = 1.8 V		60		
SFDR	Spurious-free dynamic range <sup>(4)</sup>	$f_{IN} = 2\text{ kHz}$ , AVDD = 3 V		80		dB
$BW_{(fp)}$	Full-power bandwidth	At -3 dB, AVDD = 3 V		25		MHz
<b>DIGITAL INPUT/OUTPUT (CMOS Logic Family)</b>						
$V_{IH}$	High-level input voltage <sup>(6)</sup>		0.65 DVDD		DVDD + 0.3	V
$V_{IL}$	Low-level input voltage <sup>(6)</sup>		-0.3		0.35 DVDD	V
$V_{OH}$	High-level output voltage <sup>(6)</sup>	At $I_{source} = 500\ \mu\text{A}$	0.8 DVDD		DVDD	V
		At $I_{source} = 2\text{ mA}$	DVDD - 0.45		DVDD	
$V_{OL}$	Low-level output voltage <sup>(6)</sup>	At $I_{sink} = 500\ \mu\text{A}$	0		0.2 DVDD	V
		At $I_{sink} = 2\text{ mA}$	0		0.45	
<b>POWER-SUPPLY REQUIREMENTS</b>						
AVDD	Analog supply voltage		1.65	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
$I_{AVDD}$	Analog supply current	At 1 MSPS with AVDD = 3 V			200	μA
		At 100 kSPS with AVDD = 3 V			23	
		At 1 MSPS with AVDD = 1.8 V		105		
$P_D$	Power dissipation	At 1 MSPS with AVDD = 3 V			600	μW
		At 100 kSPS with AVDD = 3 V			60	
		At 1 MSPS with AVDD = 1.8 V		189		

(1) Ideal input span; does not include gain or offset error.

(2) LSB means least significant bit.

(3) Refer to the [Offset Calibration](#) section for more details.

(4) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.

(5) Calculated on the first nine harmonics of the input frequency.

(6) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. See the [Digital Voltage Levels](#) section for more details.

### 6.6 Timing Characteristics

All specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $AVDD = 1.65\text{ V}$  to  $3.6\text{ V}$ ,  $DVDD = 1.65\text{ V}$  to  $3.6\text{ V}$ , and  $C_{LOAD}$  on SDO =  $20\text{ pF}$ , unless otherwise specified.

		MIN	TYP	MAX	UNIT
<b>TIMING SPECIFICATIONS</b>					
$f_{\text{THROUGHPUT}}$	Throughput			1	MSPS
$t_{\text{CYCLE}}$	Cycle time	1			$\mu\text{s}$
$t_{\text{CONV}}$	Conversion time		$10.5 \times t_{\text{SCLK}} + t_{\text{SU\_CSCK}}$		ns
$t_{\text{DV\_CSDO}}$	Delay time: $\overline{\text{CS}}$ falling to data enable			10	ns
$t_{\text{D\_CKDO}}$	Delay time: SCLK falling to (next) data valid on DOUT, $AVDD = 1.8\text{ V}$ to $3.6\text{ V}$			30	ns
	Delay time: SCLK falling to (next) data valid on DOUT, $AVDD = 1.65\text{ V}$ to $1.8\text{ V}$			50	ns
$t_{\text{DZ\_CSDO}}$	Delay time: $\overline{\text{CS}}$ rising to DOUT going to 3-state	5			ns
<b>TIMING REQUIREMENTS</b>					
$t_{\text{ACQ}}$	Acquisition time	235			ns
$f_{\text{SCLK}}$	SCLK frequency	0.016		14	MHz
$t_{\text{SCLK}}$	SCLK period	71.43			ns
$t_{\text{PH\_CK}}$	SCLK high time	0.45		0.55	$t_{\text{SCLK}}$
$t_{\text{PL\_CK}}$	SCLK low time	0.45		0.55	$t_{\text{SCLK}}$
$t_{\text{PH\_CS}}$	$\overline{\text{CS}}$ high time	60			ns
$t_{\text{SU\_CSCK}}$	Setup time: $\overline{\text{CS}}$ falling to SCLK falling	15			ns
$t_{\text{D\_CKCS}}$	Delay time: last SCLK falling to $\overline{\text{CS}}$ rising	10			ns

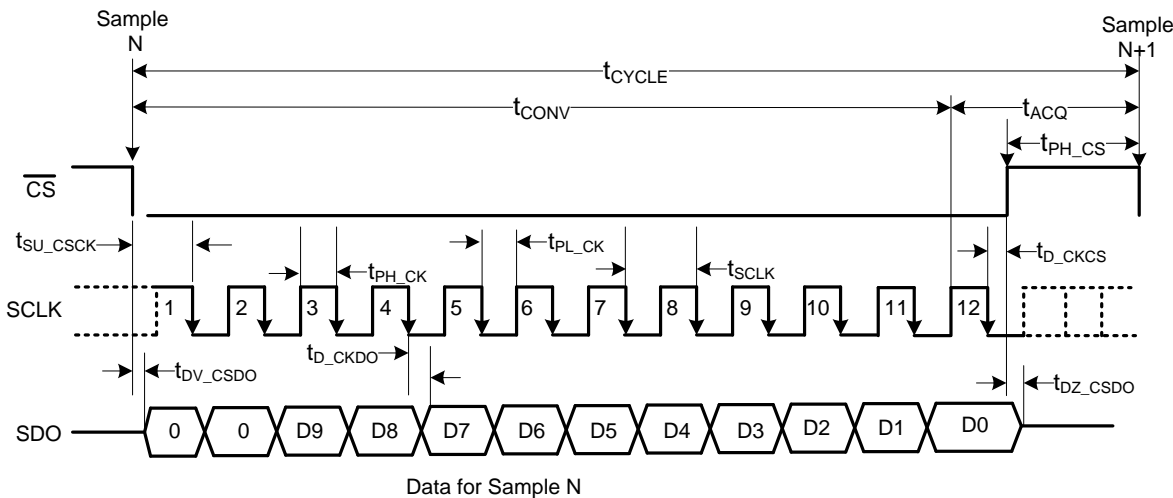
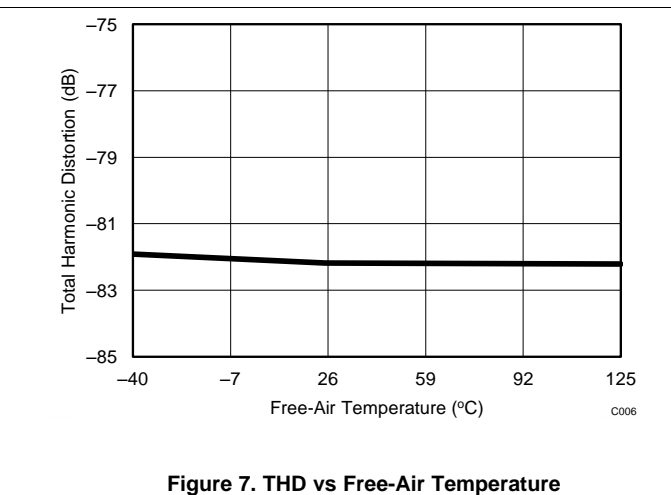
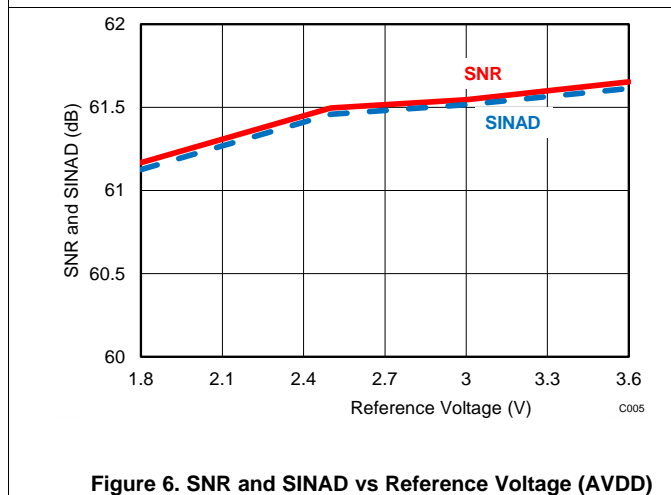
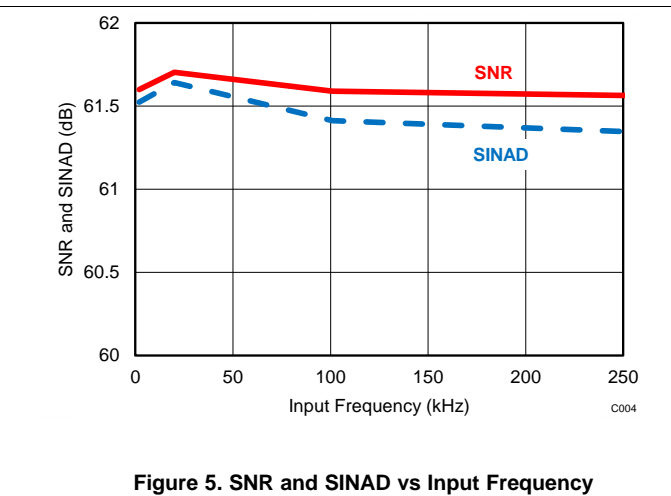
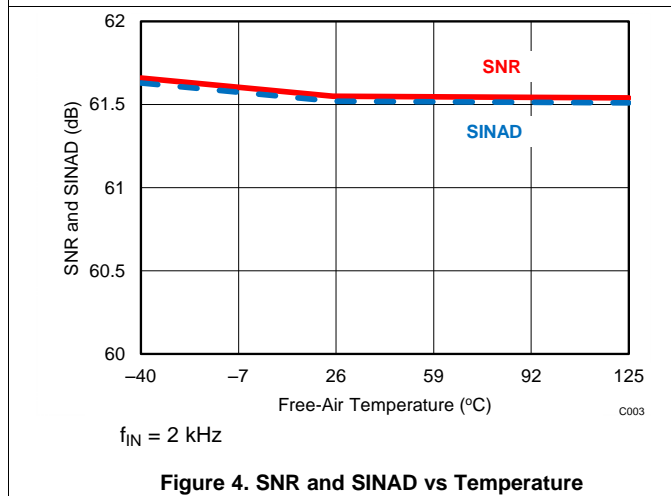
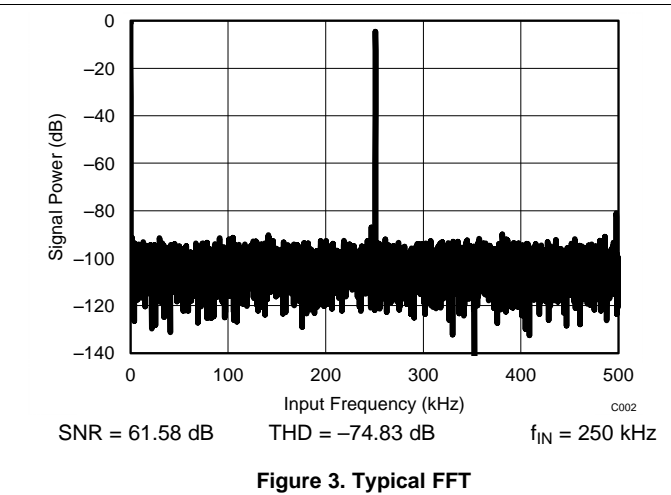
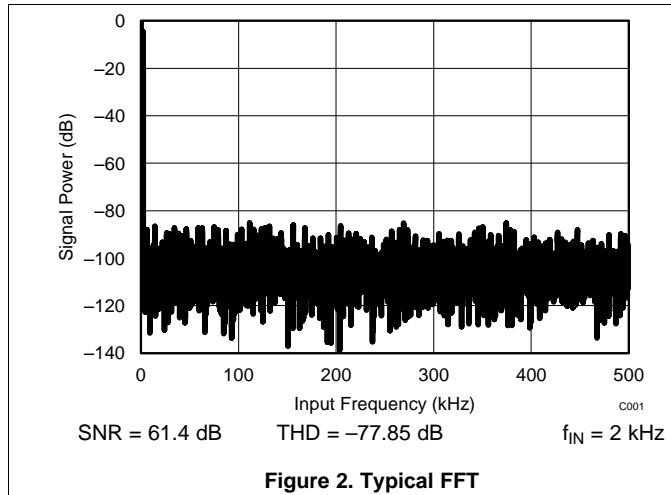


Figure 1. Timing Diagram

### 6.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , unless otherwise noted.





Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , unless otherwise noted.

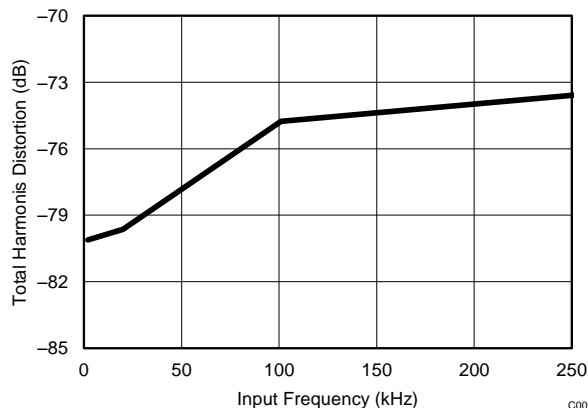


Figure 8. THD vs Input Frequency

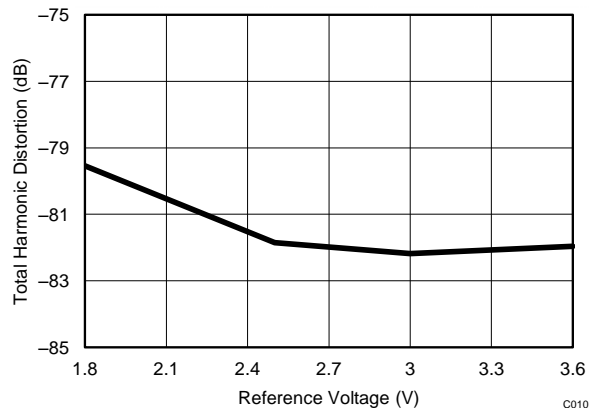


Figure 9. THD vs Reference Voltage

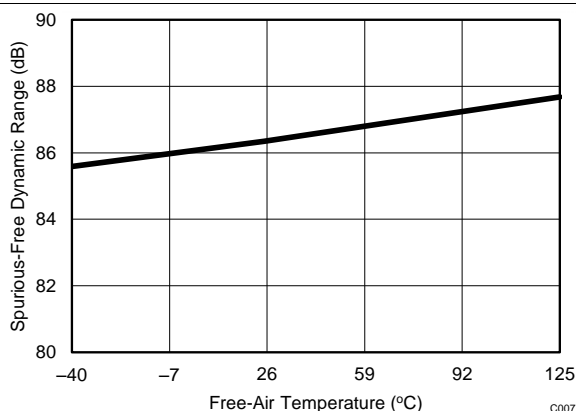


Figure 10. SFDR vs Free-Air Temperature

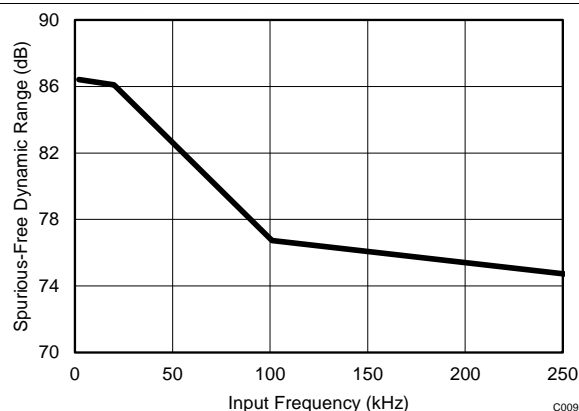


Figure 11. SFDR vs Input Frequency

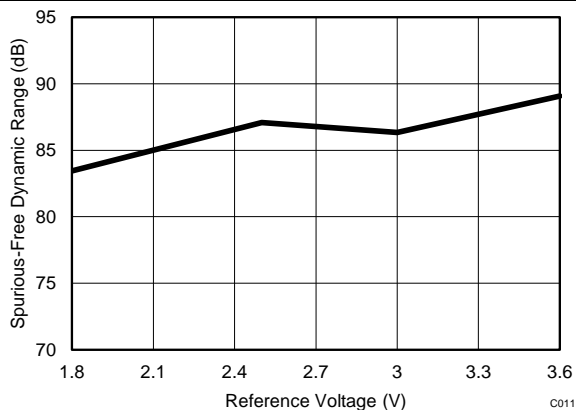


Figure 12. SFDR vs Reference Voltage (AVDD)

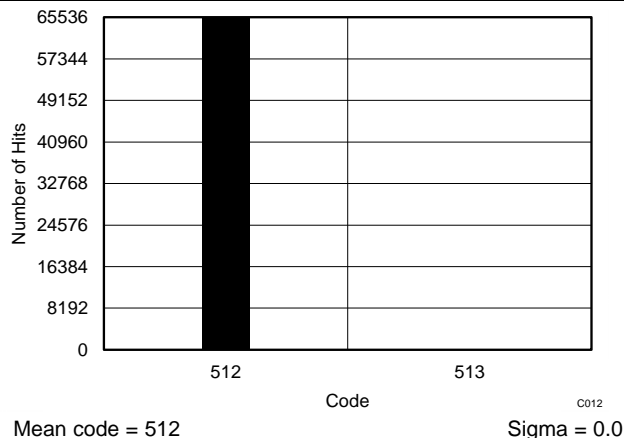


Figure 13. DC Input Histogram

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , unless otherwise noted.

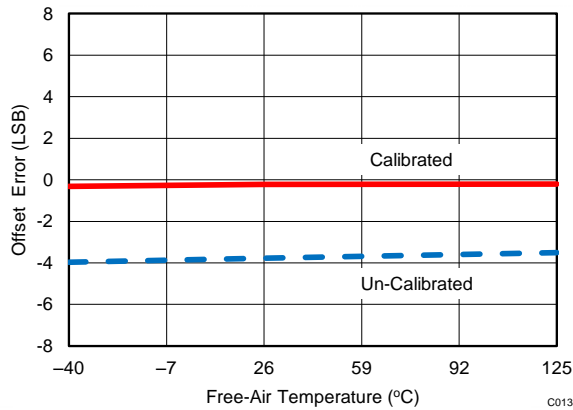


Figure 14. Offset Error vs Free-Air Temperature

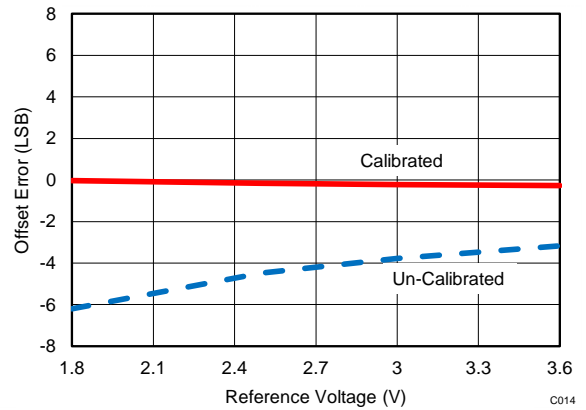


Figure 15. Offset Error vs Reference Voltage (AVDD)

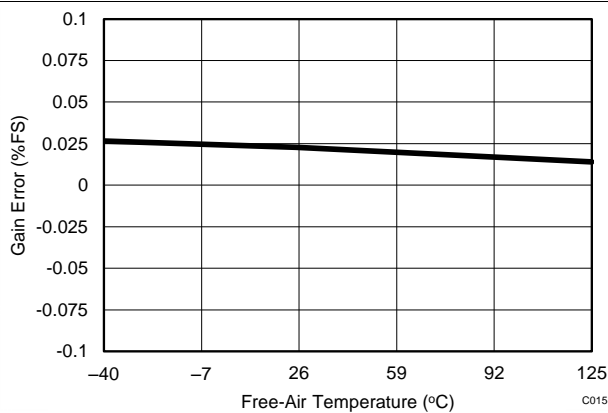


Figure 16. Gain Error vs Free-Air Temperature

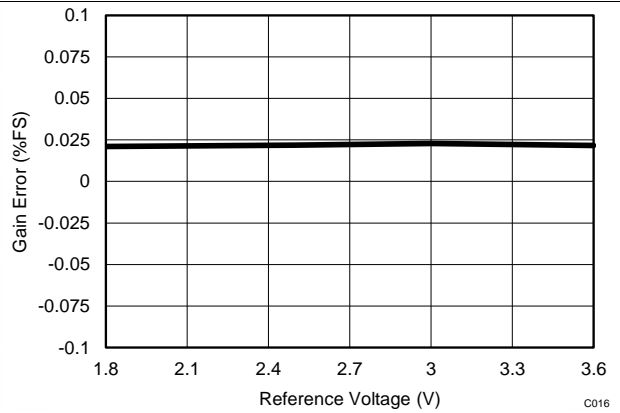


Figure 17. Gain Error vs Reference Voltage (AVDD)

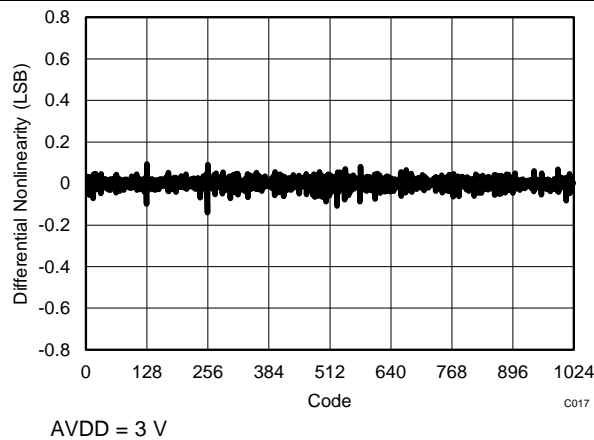


Figure 18. Typical DNL

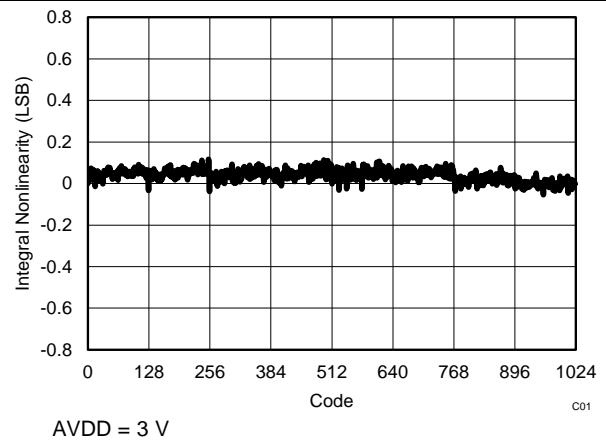


Figure 19. Typical INL

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , unless otherwise noted.

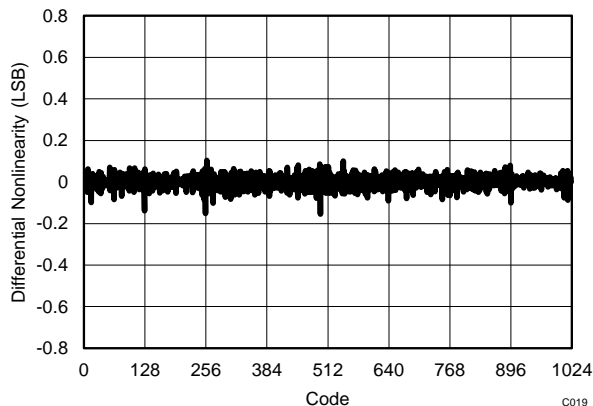


Figure 20. Typical DNL

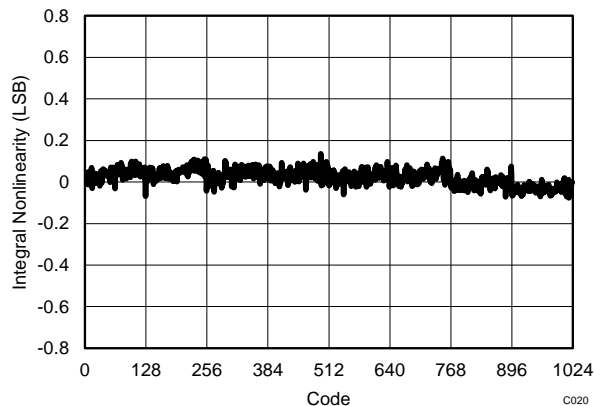


Figure 21. Typical INL

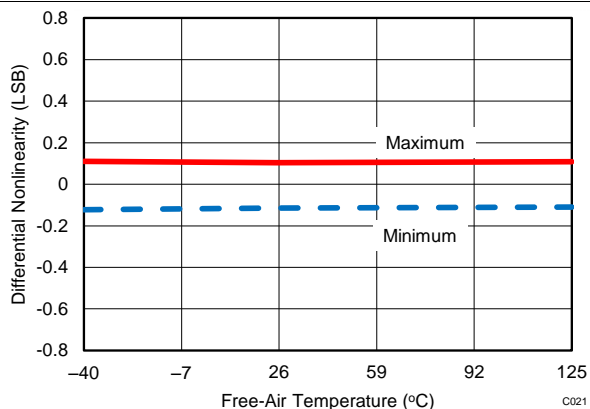


Figure 22. DNL vs Free-Air Temperature

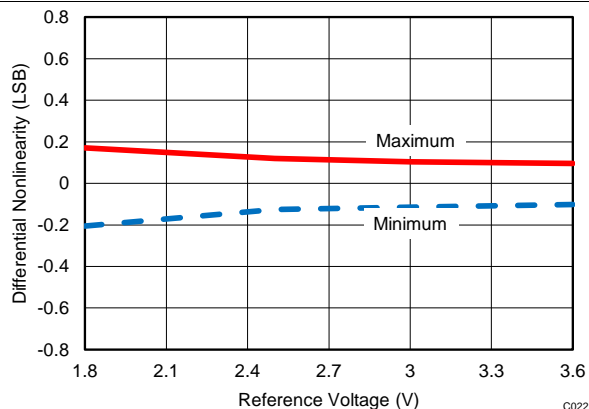


Figure 23. DNL vs Reference Voltage (AVDD)

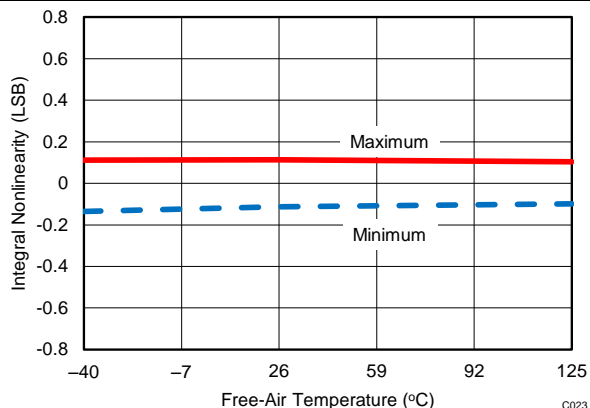


Figure 24. INL vs Free-Air Temperature

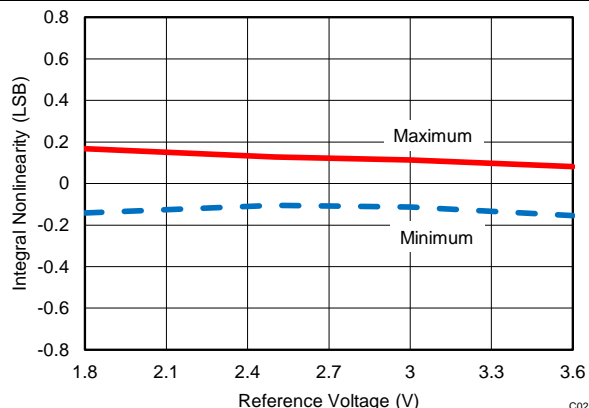
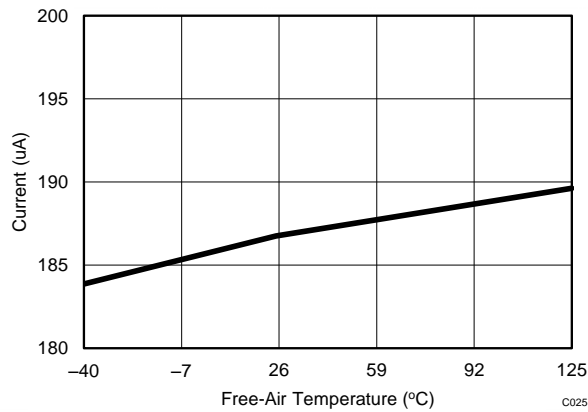


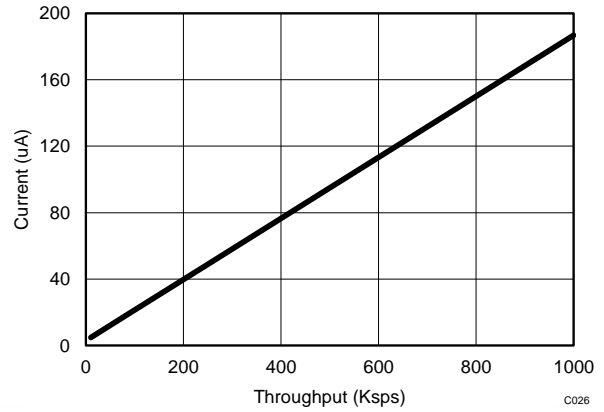
Figure 25. INL vs Reference Voltage (AVDD)

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3\text{ V}$ ,  $DVDD = 1.8\text{ V}$ , and  $f_{\text{SAMPLE}} = 1\text{ MSPS}$ , unless otherwise noted.

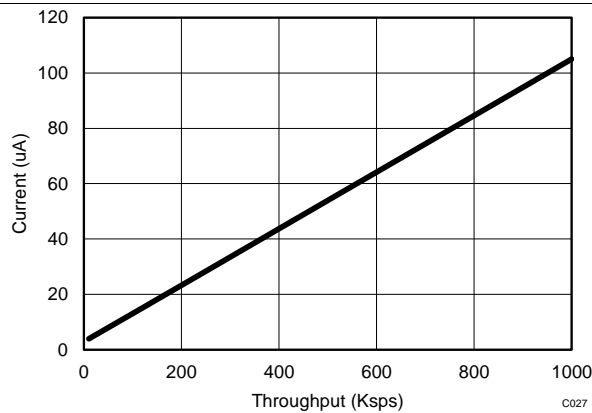


**Figure 26. AVDD Supply Current vs Free-Air Temperature**



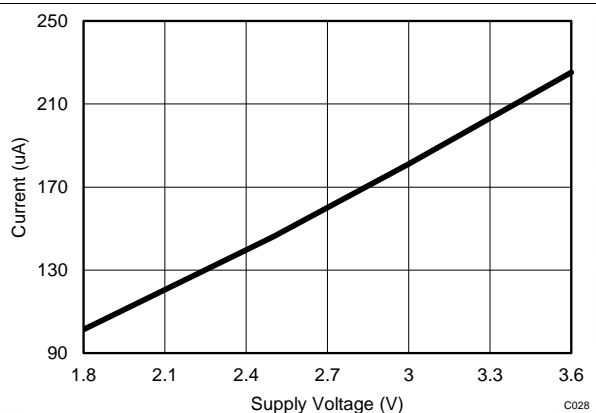
AVDD = 3 V

**Figure 27. AVDD Supply Current vs Throughput**

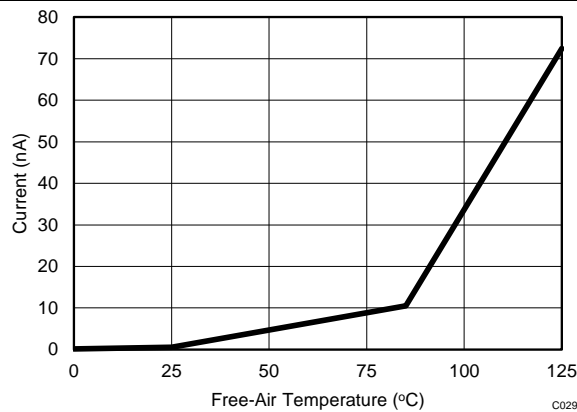


AVDD = 1.8 V

**Figure 28. AVDD Supply Current vs Throughput**



**Figure 29. AVDD Supply Current vs AVDD Voltage**



**Figure 30. AVDD Static Current vs Free-Air Temperature**

## 7 Parameter Measurement Information

### 7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 31 shows voltage levels for the digital input and output pins.

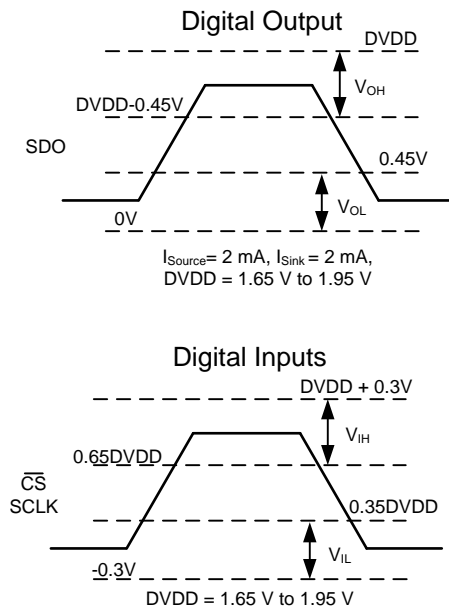


Figure 31. Digital Voltage Levels as per the JESD8-7A Standard

## 8 Detailed Description

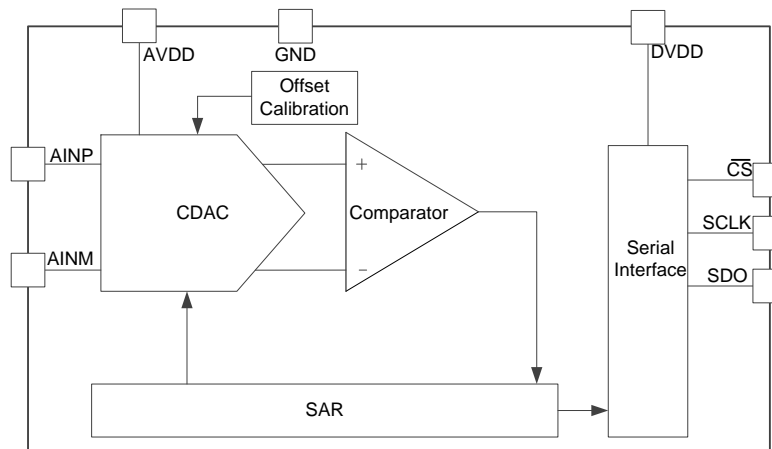
### 8.1 Overview

The ADS7041 is an ultralow-power, ultra-small analog-to-digital converter (ADC) that supports a wide analog input range. The analog input range for the device is defined by the AVDD supply voltage. The device samples the input voltage across the AINP and AINM pins on the  $\overline{CS}$  falling edge and starts the conversion. The clock provided on the SCLK pin is used for conversion and data transfer. During conversions, both the AINP and AINM pins are disconnected from the sampling circuit. After the conversion completes, the sampling capacitors are reconnected across the AINP and AINM pins and the ADS7041 enters acquisition phase.

The device has an internal offset calibration. The offset calibration can be initiated by the user either on power-up or during normal operation; see the [Offset Calibration](#) section for more details.

The device also provides a simple serial interface to the host controller and operates over a wide range of digital power supplies. The ADS7041 requires only a 14-MHz SCLK for supporting a throughput of 1 MSPS. The digital interface also complies with the JESD8-7A (normal range) standard. The [Functional Block Diagram](#) section provides a block diagram of the device.

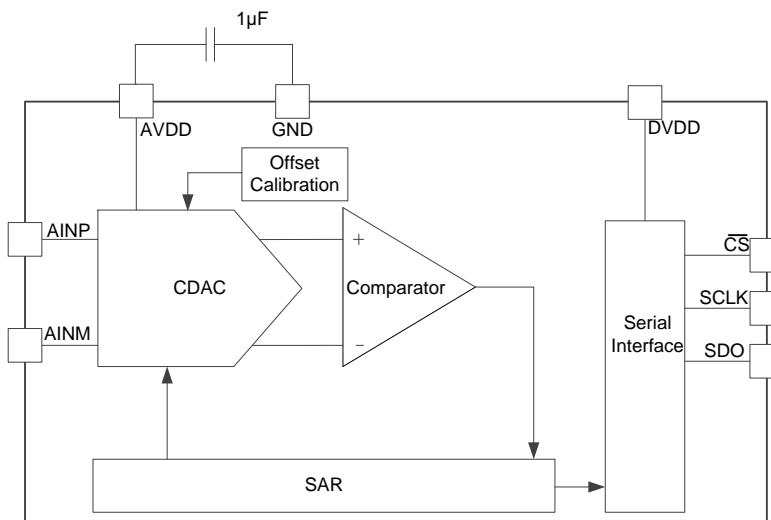
### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Reference

The device uses the analog supply voltage (AVDD) as a reference, as shown in [Figure 32](#). TI recommends decoupling the AVDD pin with a 1- $\mu$ F, low equivalent series resistance (ESR) ceramic capacitor. The minimum capacitor value required for AVDD is 200 nF. The AVDD pin functions as a switched capacitor load to the source powering AVDD. The decoupling capacitor provides the instantaneous charge required by the internal circuit and helps in maintaining a stable dc voltage on the AVDD pin. TI recommends powering the AVDD pin with a low output impedance and low-noise regulator (such as the [TPS79101](#)).

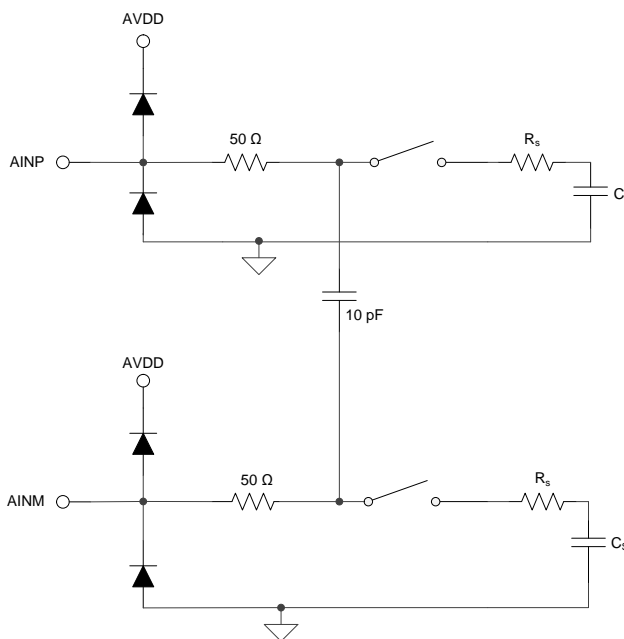


**Figure 32. Reference for the Device**

## Feature Description (continued)

### 8.3.2 Analog Input

The device supports single-ended analog inputs. The ADC samples the difference between AINP and AINM and converts for this voltage. The device is capable of accepting a signal from  $-100\text{ mV}$  to  $100\text{ mV}$  on the AINM input and is useful in systems where the sensor or signal-conditioning block is far from the ADC. In such a scenario, there can be a difference between the ground potential of the sensor or signal conditioner and the ADC ground. In such cases, use separate wires to connect the ground of the sensor or signal conditioner to the AINM pin. The AINP input is capable of accepting signals from  $0\text{ V}$  to  $\text{AVDD}$ . [Figure 33](#) represents the equivalent analog input circuits for the sampling stage. The device has a low-pass filter followed by the sampling switch and sampling capacitor. The sampling switch is represented by an  $R_s$  (typically  $50\ \Omega$ ) resistor in series with an ideal switch and  $C_s$  (typically  $15\text{ pF}$ ) is the sampling capacitor. The ESD diodes are connected from both analog inputs to  $\text{AVDD}$  and ground.



**Figure 33. Equivalent Input Circuit for the Sampling Stage**

The analog input full-scale range (FSR) is equal to the reference voltage of the ADC. The reference voltage for the device is equal to the analog supply voltage ( $\text{AVDD}$ ). Thus, the device FSR can be determined by [Equation 1](#):

$$\text{FSR} = V_{\text{REF}} = \text{AVDD} \quad (1)$$

### 8.3.3 ADC Transfer Function

The device output is in straight binary format. The device resolution for a single-ended input can be computed by [Equation 2](#):

$$1\text{ LSB} = V_{\text{REF}} / 2^N$$

where:

- $V_{\text{REF}} = \text{AVDD}$  and
- $N = 10$

(2)



Feature Description (continued)

Figure 34 and Table 1 show the ideal transfer characteristics for the device.

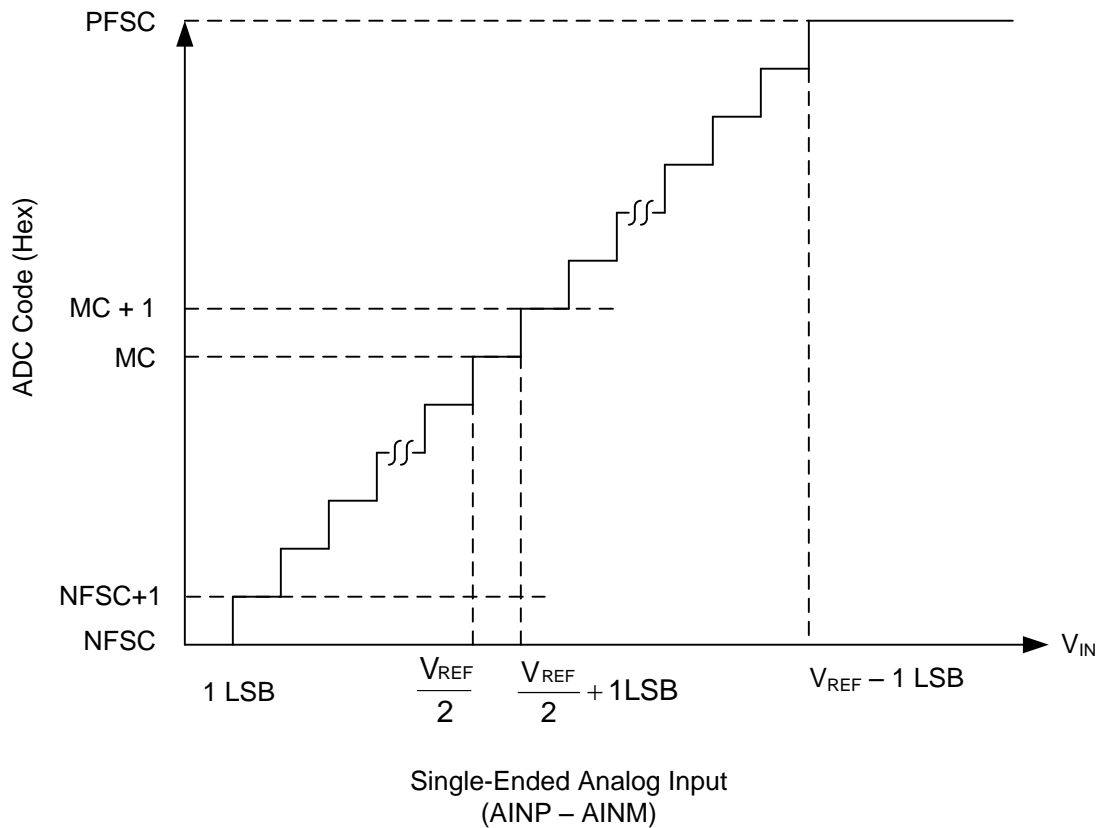


Figure 34. Ideal Transfer Characteristics

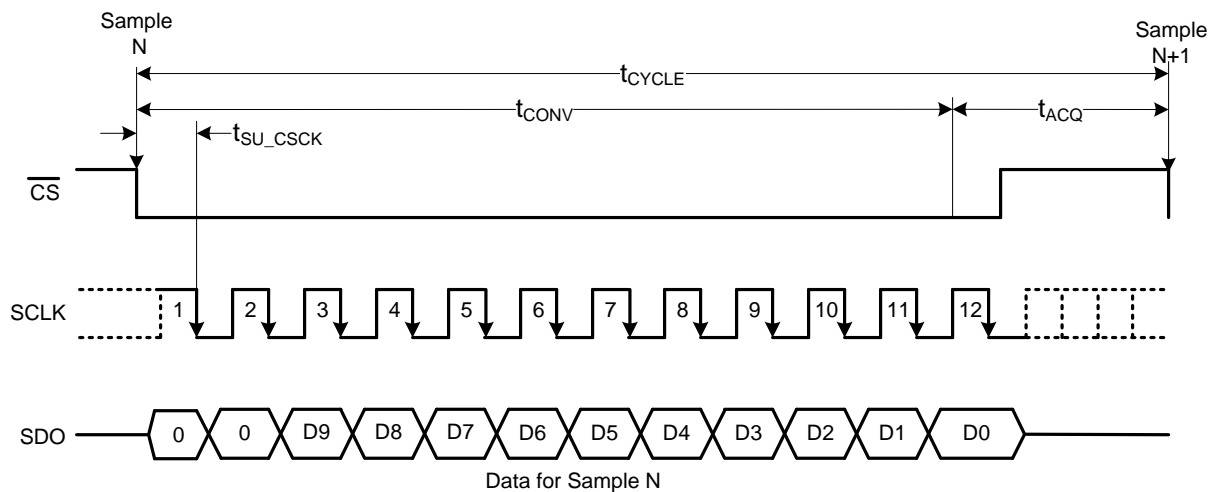
Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP - AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE
$\leq 1$ LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
$(V_{REF} / 2)$ to $(V_{REF} / 2) + 1$ LSB	MC	Mid code	200
$(V_{REF} / 2) + 1$ LSB to $(V_{REF} / 2) + 2$ LSBs	MC + 1	—	201
$\geq V_{REF} - 1$ LSB	PFSC	Positive full-scale code	3FF

### 8.3.4 Serial Interface

The device supports a simple, SPI-compatible interface to the external host. The  $\overline{\text{CS}}$  signal defines one conversion and serial transfer frame. A frame starts with a  $\overline{\text{CS}}$  falling edge and ends with a  $\overline{\text{CS}}$  rising edge. The SDO pin outputs the ADC conversion results. Figure 35 shows a detailed timing diagram for the serial interface. A minimum delay of  $t_{\text{SU\_CSCK}}$  must elapse between the  $\overline{\text{CS}}$  falling edge and the first SCLK falling edge. The device uses the clock provided on the SCLK pin for conversion and data transfer. The conversion result is available on the SDO pin with the first two bits set to 0, followed by 10 bits of the conversion result. The first zero is launched on the SDO pin on the  $\overline{\text{CS}}$  falling edge. Subsequent bits (starting with another 0 followed by the conversion result) are launched on the SDO pin on subsequent SCLK falling edges. The SDO output remains low after 12 SCLKs. A  $\overline{\text{CS}}$  rising edge ends the frame and brings the serial data bus to 3-state. For acquisition of the next sample, a minimum time of  $t_{\text{ACQ}}$  must be provided after the conversion of the current sample is completed. For details on timing specifications, see the [Timing Characteristics](#) table.

The device initiates an offset calibration on the first  $\overline{\text{CS}}$  falling edge after power-up and the SDO output remains low during the first serial transfer frame after power-up. For further details, refer to the [Offset Calibration](#) section.

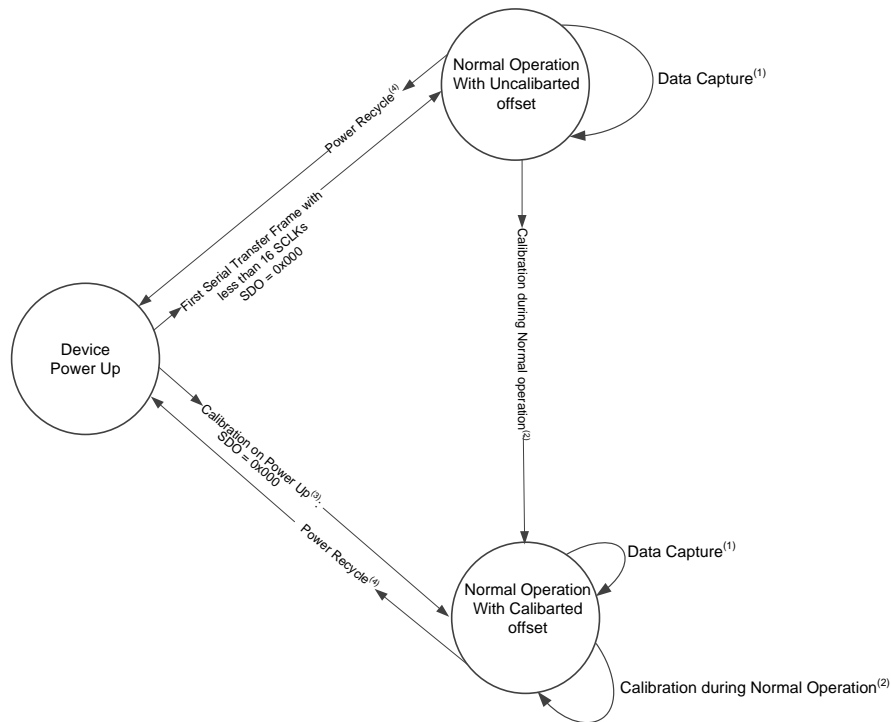


**Figure 35. Serial Interface Timing Diagram**

## 8.4 Device Functional Modes

### 8.4.1 Offset Calibration

The ADS7041 includes a feature to calibrate the device internal offset. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage. The device includes an internal offset calibration register (OCR) that stores the offset calibration result. The OCR is an internal register and cannot be accessed by the user through the serial interface. The OCR is reset to zero on power-up. Therefore, TI recommends calibrating the offset on power-up to bring the offset within the specified limits. If the operating temperature or analog supply voltage reflect a significant change, the offset can be recalibrated during normal operation. Figure 36 shows the offset calibration process.



- (1) See the [Timing Characteristics](#) section for timing specifications.
- (2) See the [Offset Calibration During Normal Operation](#) section for details.
- (3) See the [Offset Calibration on Power-Up](#) section for details.
- (4) The power recycle on the AVDD supply is required to reset the offset calibration and to bring the device to a power-up state.

**Figure 36. Offset Calibration**

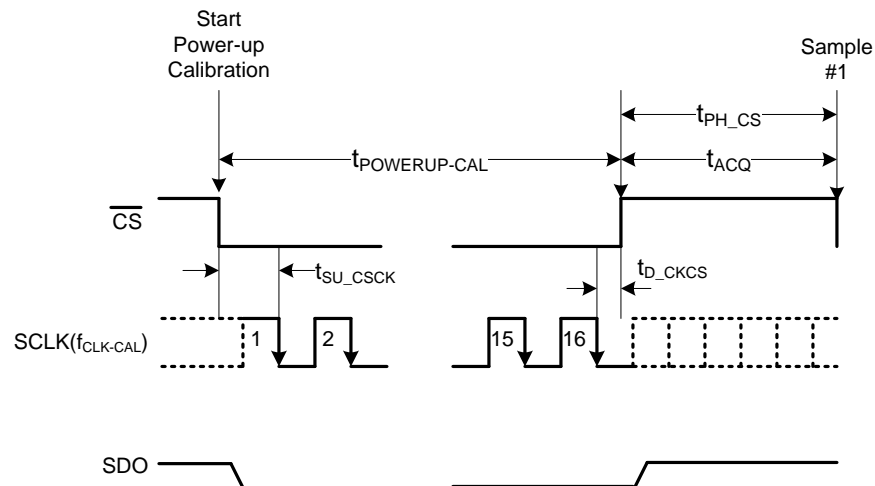
**Device Functional Modes (continued)**
**8.4.1.1 Offset Calibration on Power-Up**

The device initiates offset calibration on the first  $\overline{\text{CS}}$  falling edge after power-up and calibration completes if the  $\overline{\text{CS}}$  pin remains low for at least 16 SCLK falling edges after the first  $\overline{\text{CS}}$  falling edge. The SDO output remains low during calibration. The minimum acquisition time must be provided after calibration for acquiring the first sample. If the device is not provided with at least 16 SCLKs during the first serial transfer frame after power-up, the OCR is not updated. Table 2 provides the timing parameters for offset calibration on power-up.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in OCR is provided by the device on the SDO output. Figure 37 shows the timing diagram for offset calibration on power-up.

**Table 2. Offset Calibration on Power-Up**

		MIN	TYP	MAX	UNIT
$f_{\text{CLK-CAL}}$	SCLK frequency for calibration for 2.25 V < AVDD < 3.6 V			14	MHz
$f_{\text{CLK-CAL}}$	SCLK frequency for calibration for 1.65 V < AVDD < 2.25 V			12	MHz
$t_{\text{POWERUP-CAL}}$	Calibration time at power-up	15 $t_{\text{SCLK}}$			ns
$t_{\text{ACQ}}$	Acquisition time	235			ns
$t_{\text{PH-CS}}$	$\overline{\text{CS}}$ high time	$t_{\text{ACQ}}$			ns
$t_{\text{SU-CSCK}}$	Setup time: $\overline{\text{CS}}$ falling to SCLK falling	15			ns
$t_{\text{D-CKCS}}$	Delay time: last SCLK falling to $\overline{\text{CS}}$ rising	10			ns


**Figure 37. Offset Calibration on Power-Up Timing Diagram**

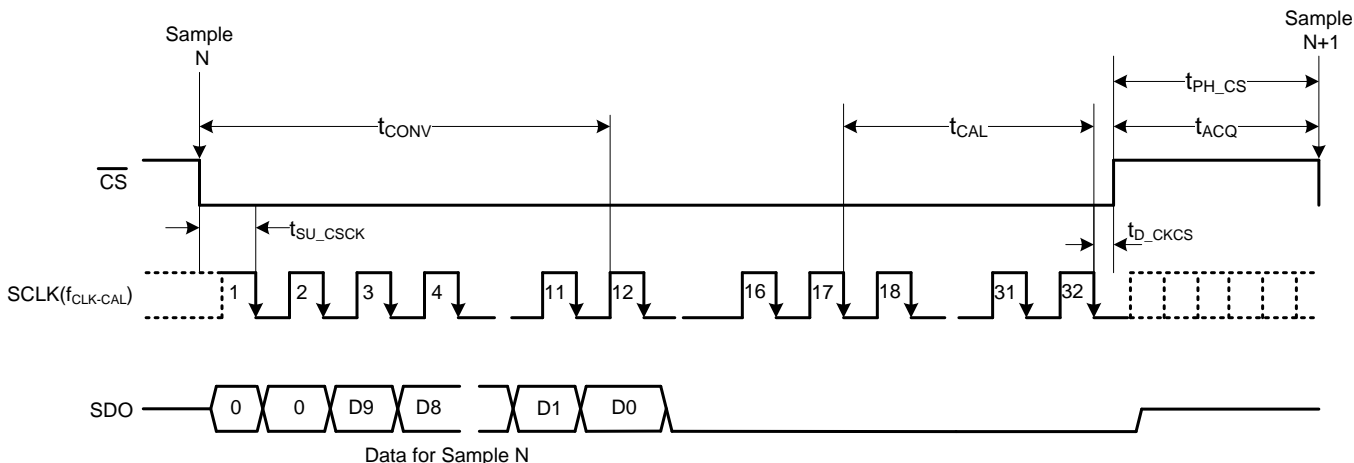
### 8.4.1.2 Offset Calibration During Normal Operation

Offset calibration can be done during normal device operation if at least 32 SCLK falling edges are provided in one serial transfer frame. During the first 12 SCLKs, the device converts the sample acquired on the CS falling edge and provides data on the SDO output. The device initiates the offset calibration on the 17th SCLK falling edge and calibration completes on the 32nd SCLK falling edge. The SDO output remains low after the 12th SCLK falling edge and SDO goes to 3-state after CS goes high. If the device is provided with less than 32 SCLKs during a serial transfer frame, the OCR is not updated. Table 3 provides the timing parameters for offset calibration during normal operation.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in the OCR is provided by the device on the SDO output. Figure 38 shows the timing diagram for offset calibration during normal operation.

**Table 3. Offset Calibration During Normal Operation**

		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration for 2.25 V < AVDD < 3.6 V			14	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration for 1.65 V < AVDD < 2.25 V			12	MHz
$t_{CAL}$	Calibration time during normal operation	15 $t_{SCLK}$			ns
$t_{ACQ}$	Acquisition time	235			ns
$t_{PH\_CS}$	$\overline{CS}$ high time	$t_{ACQ}$			ns
$t_{SU\_CSCK}$	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
$t_{D\_CKCS}$	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns



**Figure 38. Offset Calibration During Normal Operation Timing Diagram**

## 9 Application and Implementation

### NOTE

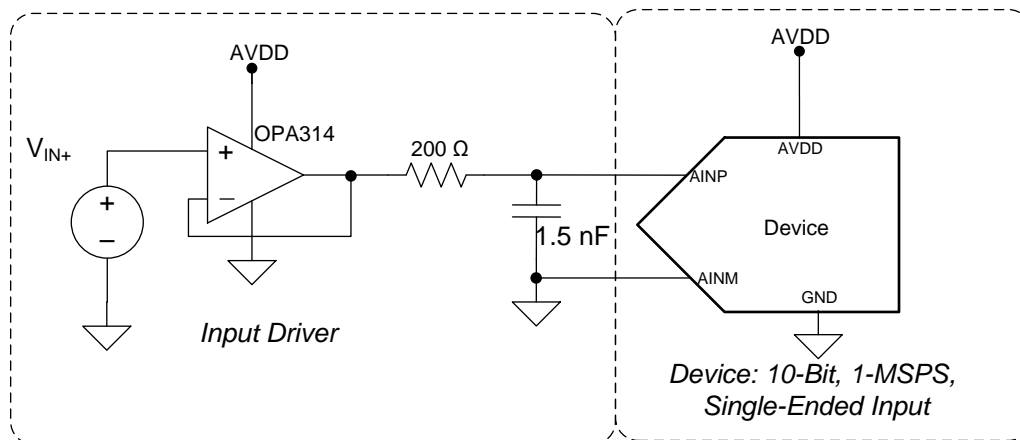
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7041.

### 9.2 Typical Applications

#### 9.2.1 Single-Supply DAQ with the ADS7041



**Figure 39. DAQ Circuit: Single-Supply DAQ**

##### 9.2.1.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7041 with SNR greater than 61 dB and THD less than  $-75$  dB for input frequencies of 2.5 kHz at a throughput of 1 MSPS.

##### 9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an antialiasing filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

## Typical Applications (continued)

### 9.2.1.2.1 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a rate greater than or equal to the Nyquist rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an external, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass RC filter, for which the 3-dB bandwidth is optimized for noise, response time, and throughput. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. Figure 40 provides the equation for determining the bandwidth of the antialiasing filter.

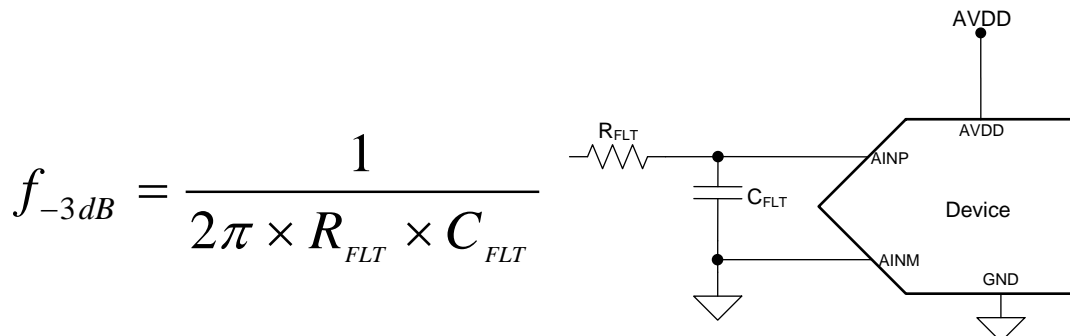


Figure 40. Antialiasing Filter

For ac signals, the filter bandwidth must be kept low to band limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor,  $C_{FLT}$ , is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor is at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 15 pF. Thus, the value of  $C_{FLT}$  is greater than 300 pF. Select a COG- or NPO-type capacitor because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{FLT}$ ) are used at the output of the amplifiers. A higher value of  $R_{FLT}$  is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{FLT}$  requires balancing the stability and distortion of the design.

The input amplifier bandwidth is typically much higher than the cutoff frequency of the antialiasing filter. Thus, TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers can require more bandwidth than others to drive similar filters.

## Typical Applications (continued)

### 9.2.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth:** Select the small-signal bandwidth of the input amplifiers to be high enough to settle the input signal in the acquisition time of the ADC. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the select the amplifier bandwidth as described in [Equation 3](#).

$$GBW \geq 4 \times \frac{1}{2\pi \times R_{FLT} \times C_{FLT}}$$

where:

- GBW = unity gain bandwidth (3)
- **Noise:** Noise contribution of the front-end amplifiers must be low enough to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band limited by designing a low cutoff frequency RC filter, as explained in [Equation 4](#).

$$N_G \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu VRMS$ ,
- $e_{n\_RMS}$  is the amplifier broadband noise,
- $f_{-3dB}$  is the  $-3$ -dB bandwidth of the RC filter, and
- $N_G$  is the noise gain of the front-end circuit, which is equal to 1 in the buffer configuration. (4)
- **Settling time:** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver with TINA™-SPICE simulations before selecting the amplifier.

The OPA314 is selected for this application for its rail-to-rail input and output swing, low-noise ( $14 \text{ nV}/\sqrt{\text{Hz}}$ ), and low-power ( $150 \mu\text{A}$ ) performance to support a single-supply data acquisition circuit.

### 9.2.1.2.3 Reference Circuit

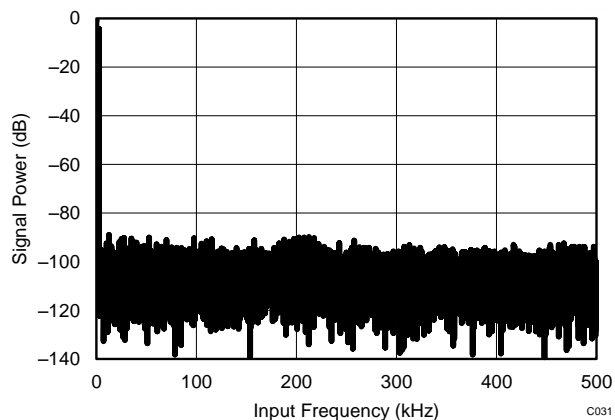
The analog supply voltage of the device is also used as a voltage reference for conversion. TI recommends decoupling the AVDD pin with a  $1\text{-}\mu\text{F}$ , low-ESR ceramic capacitor. The minimum capacitor value required for AVDD is  $200 \text{ nF}$ .



**Typical Applications (continued)**

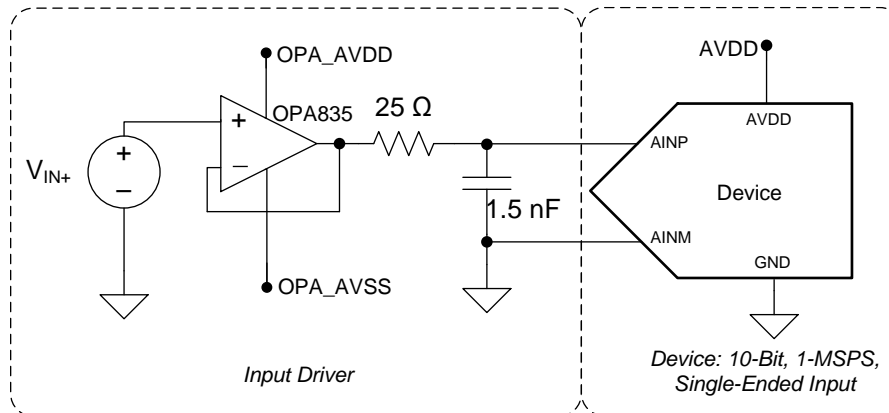
**9.2.1.3 Application Curve**

Figure 41 shows the FFT plot for the ADS7041 with a 2.5-kHz input frequency used for the circuit in Figure 39.



SNR = 61.1 dB      THD = -79.8 dB      SINAD = 61 dB  
 Number of samples = 32768

**Figure 41. Test Results for the ADS7041 and OPA314 for a 2.5-kHz Input**

**Typical Applications (continued)**
**9.2.2 DAQ Circuit with the ADS7041 for Maximum SINAD**


**Figure 42. ADS7041 DAQ Circuit: Maximum SINAD for Input Frequencies up to 250 kHz**

**9.2.2.1 Design Requirements**

The goal of this application is to design a data acquisition circuit based on the ADS7041 with SINAD greater than 61 dB for input frequencies up to 250 kHz.

**9.2.2.2 Detailed Design Procedure**

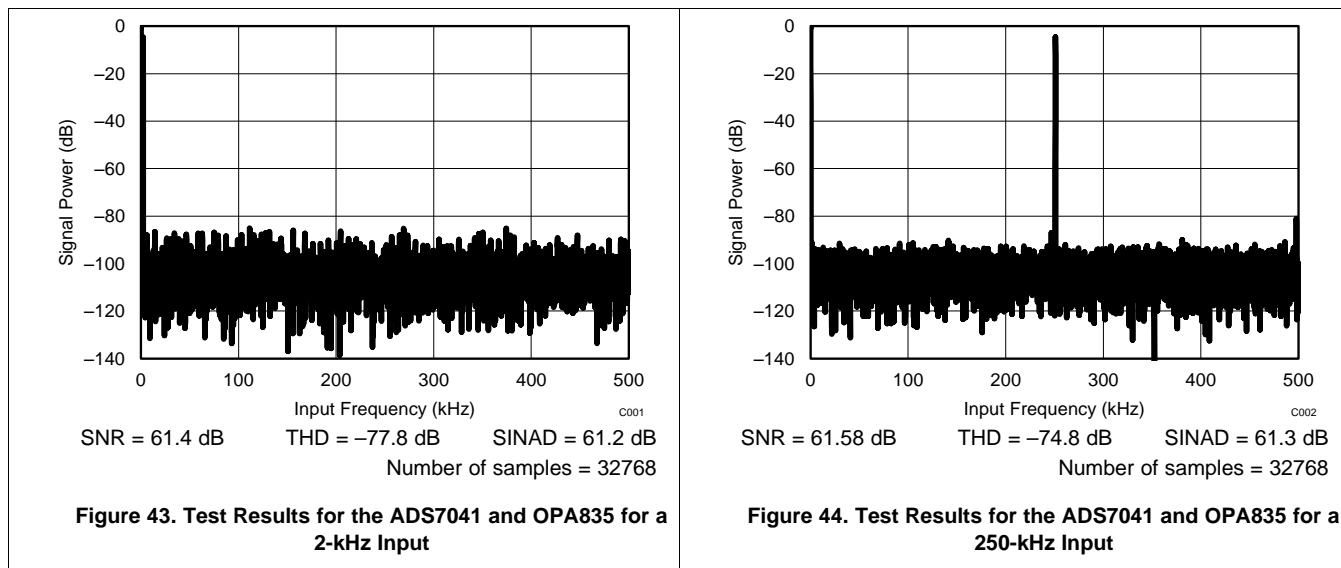
To achieve a SINAD of 61 dB, the operational amplifier must have high bandwidth in order to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in [Figure 42](#), the [OPA835](#) is selected for its high bandwidth (56 MHz) and low noise (9.3 nV/ $\sqrt{\text{Hz}}$ ).



For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIPD168, Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor \(TIDU390\)](#).

**9.2.2.3 Application Curves**

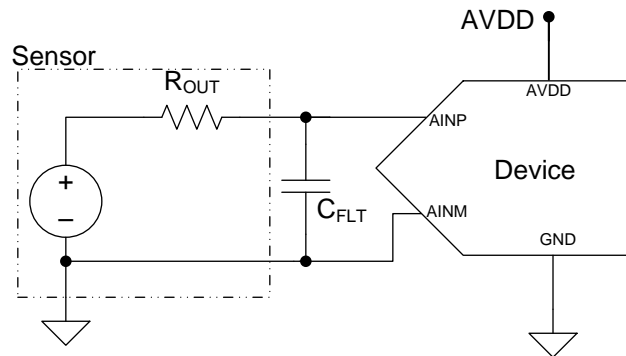
Figure 43 shows the FFT plot for the ADS7041 with a 2-kHz input frequency used for the circuit in Figure 42. Figure 44 shows the FFT plot for the ADS7041 with a 250-kHz input frequency used for the circuit in Figure 42.



**Figure 43. Test Results for the ADS7041 and OPA835 for a 2-kHz Input**

**Figure 44. Test Results for the ADS7041 and OPA835 for a 250-kHz Input**

### 9.2.3 10-Bit, 10-kSPS DAQ Circuit Optimized for DC Sensor Measurements



**Figure 45. Interfacing the Device Directly with Sensors**

In applications where the input is very slow moving and the overall system ENOB is not a critical parameter, a DAQ circuit can be designed without the input driver for the ADC. This type of a use case is of particular interest for applications in which the primary goal is to achieve the absolute lowest power possible. Typical applications that fall into this category are low-power sensor applications (such as temperature, pressure, humidity, gas, and chemical).

#### 9.2.3.1 Design Requirements

For this design example, use the parameters listed in [Table 4](#) as the input parameters.

**Table 4. Design Parameters**

DESIGN PARAMETER	GOAL VALUE
Throughput	10 kSPS
SNR at 100 Hz	60.5 dB
THD at 100 Hz	70dB
SINAD at 100 Hz	60 dB
ENOB	9
Power	10 $\mu$ W

#### 9.2.3.2 Detailed Design Procedure

The ADS7041 can be directly interfaced with sensors at lower throughputs without the need of an amplifier buffer. The analog input source drive must be capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal within the acquisition time of the SAR ADC. However, the output impedance of the sensor must be taken into account when interfacing a SAR ADC directly with sensors. Drive the analog input of the SAR ADC with a low impedance source. The input signal requires more acquisition time to settle to the desired accuracy because of the higher output impedance of the sensor. The simplified circuit for a sensor as a voltage source with output impedance ( $R_{OUT}$ ) is shown in [Figure 45](#).

The acquisition time of a SAR ADC (such as the ADS7041) can be increased by reducing throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput, or
2. Keeping the SCLK fixed at the highest permissible value (that is, 14 MHz for the device) and increasing the CS high time.

Table 5 lists the acquisition time for the above two cases for a throughput of 100 kSPS. Clearly, case 2 provides more acquisition time for the input signal to settle.

**Table 5. Acquisition Time with Different SCLK Frequencies**

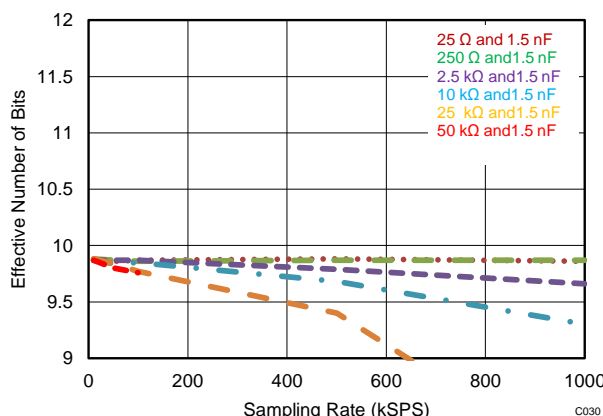
CASE	SCLK	t <sub>cycle</sub>	CONVERSION TIME (= 10.5 × t <sub>SCLK</sub> + t <sub>SU_CSCK</sub> )	ACQUISITION TIME (= t <sub>cycle</sub> - t <sub>conv</sub> )
1	1.4 MHz	10 μs	7.65 μs	2.35 μs
2	14 MHz	10 μs	0.765 μs	9.235 μs



For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIPD168, Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor \(TIDU390\)](#).

**9.2.3.3 Application Curve**

When the output impedance of the sensor increases, the time required for the input signal to settle increases and the performance of the SAR ADC starts degrading if the input signal does not settle within the acquisition time of the ADC. The performance of the SAR ADC can be improved by reducing the throughput to provide enough time for the input signal to settle. Figure 46 provides the results for ENOB achieved from the ADS7041 for case 2 at different throughputs with different input impedances at the device input.



**Figure 46. ENOB (Effective Number of Bits) Achieved from the ADS7041 at Different Throughputs**

Table 6 shows the results and performance summary for this 12-bit, 10-kSPS DAQ circuit application.

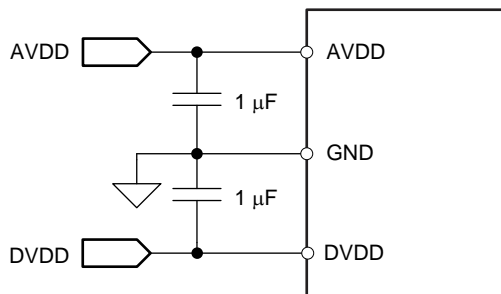
**Table 6. Results and Performance Summary for 10-Bit, 10-kSPS DAQ Circuit for DC Sensor Measurements**

DESIGN PARAMETER	GOAL VALUE	ACHIEVED RESULT
Throughput	10 kSPS	10 kSPS
SNR at 100 Hz	60.5 dB	61.3 dB
THD at 100 Hz	70dB	75 dB
SINAD at 100 Hz	60dB	61.1 dB
ENOB	9	9.87
Power	10 μW	6 μW

## 10 Power-Supply Recommendations

### 10.1 AVDD and DVDD Supply Recommendations

The ADS7041 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins individually with 1- $\mu$ F ceramic decoupling capacitors, as shown in Figure 47. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.



**Figure 47. Power-Supply Decoupling**

### 10.2 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, load capacitance on the SDO line, and the output code. The load capacitance on the SDO line is charged by the current from the SDO pin on every rising edge of the data output and is discharged on every falling edge of the data output. The current consumed by the device from the DVDD supply can be calculated by Equation 5:

$$I_{DVDD} = C \times V \times f$$

where:

- C = Load capacitance on the SDO line,
- V = DVDD supply voltage, and
- f = Number of transitions on the SDO output. (5)

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK. SDO changing on every SCLK results in an output code of 3AAh or 155h. For an output code of 3AAh or 155h at a 1-MSPS throughput, the frequency of transitions on the SDO output is 5MHz.

For the current consumption to remain at the lowest possible value, keep the DVDD supply at the lowest permissible value and keep the capacitance on the SDO line as low as possible.

### 10.3 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) as close as possible to the analog input voltage. Set AVDD to be greater than or equal to the analog input voltage of the device.
- Keep the digital supply voltage (DVDD) at the lowest permissible value.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces with throughput.



## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

相关文档如下：

- 《OPA314 数据表》（文献编号 [SBOS563](#)）
- 《OPA835 数据表》（文献编号 [SLOS713](#)）
- 《TPS79101 数据表》（文献编号 [SLVS325](#)）
- 《TIPD168 参考指南》（文献编号 [TIDU390](#)）

### 12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.



### 13 机械、封装和可订购信息

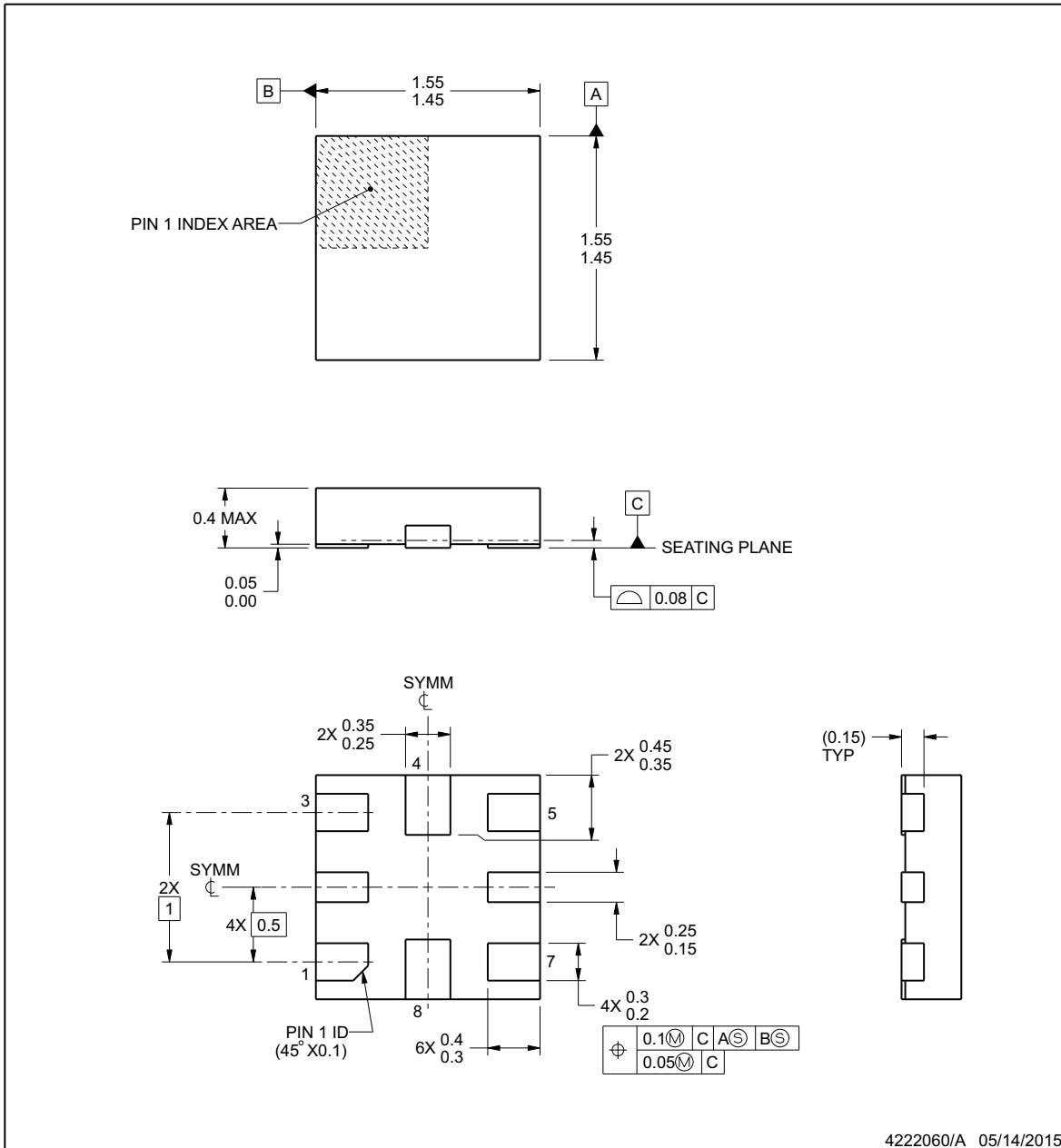
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。



**RUG0008A**

**PACKAGE OUTLINE**  
**X2QFN - 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

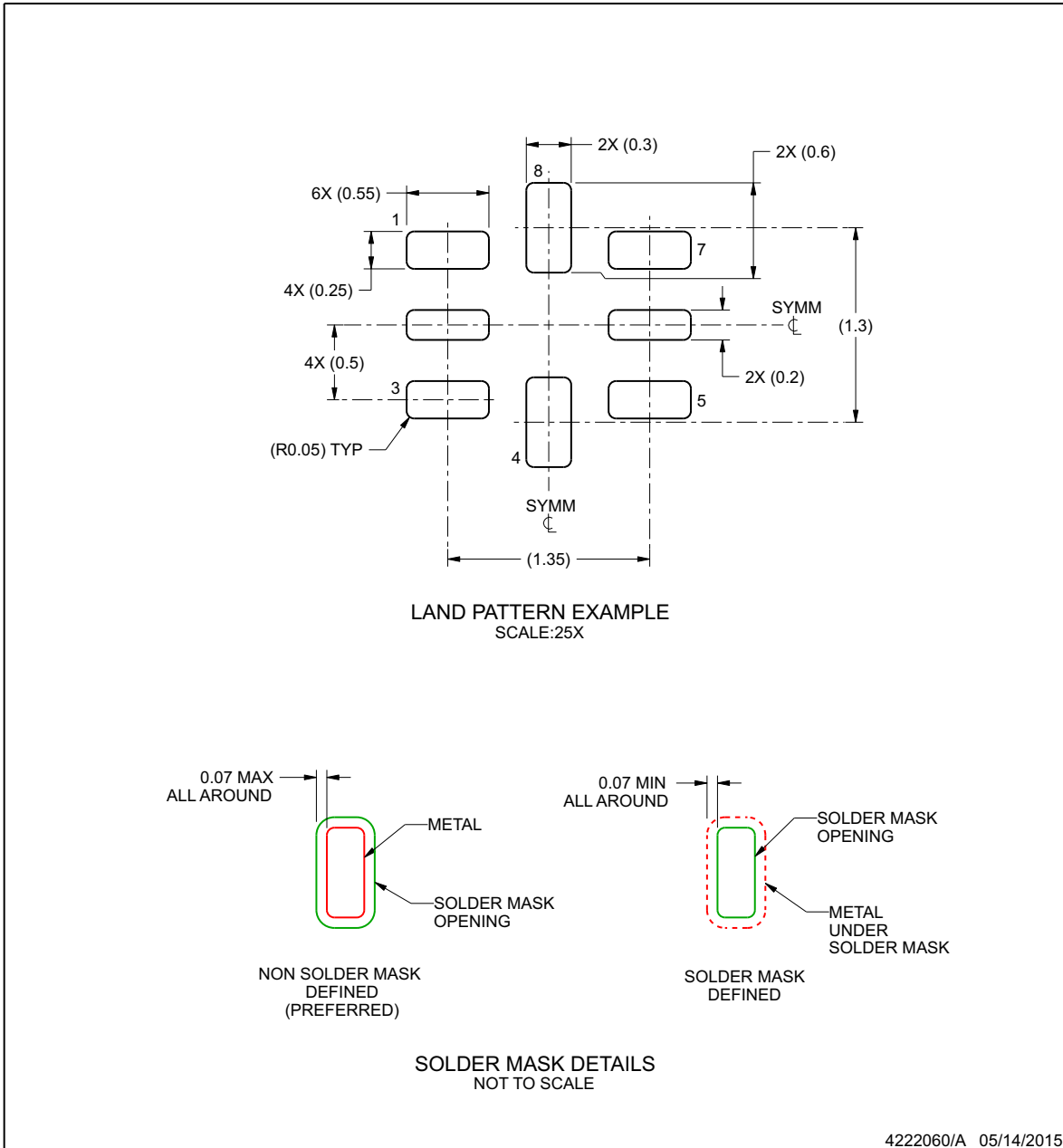
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222060/A 05/14/2015

NOTES: (continued)

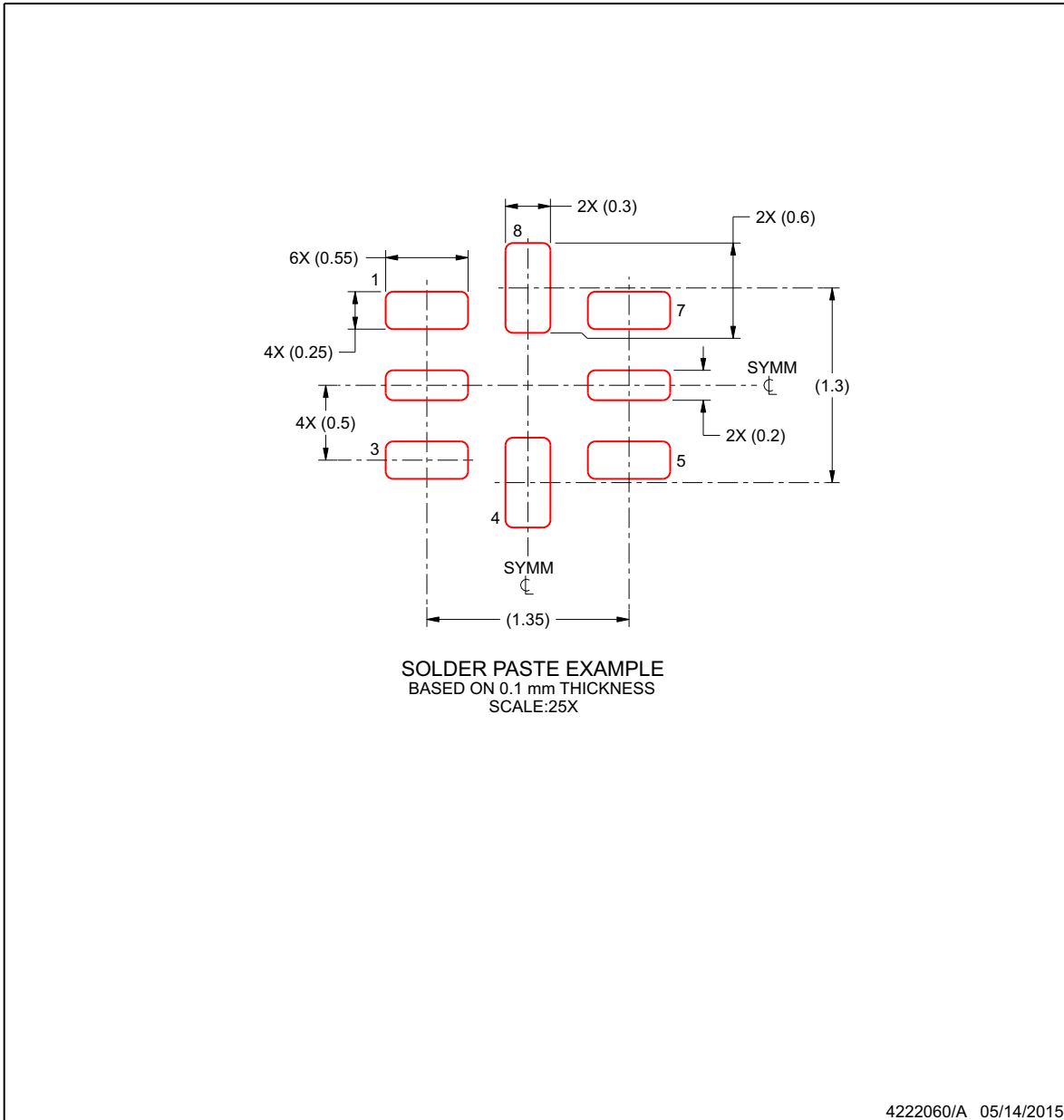
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

**EXAMPLE STENCIL DESIGN**

**RUG0008A**

**X2QFN - 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
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OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7041IDCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041	<a href="#">Samples</a>
ADS7041IDCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041	<a href="#">Samples</a>
ADS7041IRUGR	ACTIVE	X2QFN	RUG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	FU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7041IDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
ADS7041IDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
ADS7041IRUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7041IDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
ADS7041IDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
ADS7041IRUGR	X2QFN	RUG	8	3000	202.0	201.0	28.0



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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