CMOS, 8-Bit, Buffered Multiplying DAC

Enhanced Product

AD7524-EP

FEATURES

- Microprocessor compatible (6800, 8085, Z80)
- TTL-/CMOS-compatible inputs
- On-chip data latches
- Endpoint linearity
- Low power consumption
- Monotonicity guaranteed (full temperature range)
- Latch free (no protection Schottky required)

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Microprocessor controlled gain circuits
- Microprocessor controlled attenuator circuits
- Microprocessor controlled function generation
- Precision AGC circuits
- Bus structured instruments

FUNCTIONAL BLOCK DIAGRAM

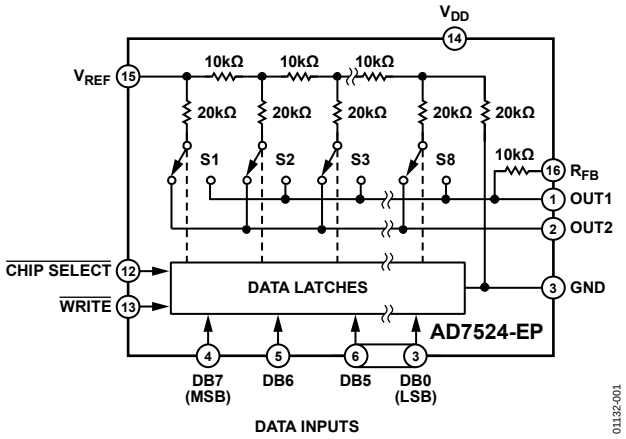

Figure 1.

GENERAL DESCRIPTION

The AD7524-EP is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

An 8-bit DAC with input latches, the load cycle of the AD7524-EP is similar to the write cycle of the random access memory. Using an advanced thin-film on the CMOS fabrication process, the AD7524-EP provides accuracy to ⅛ LSB with a typical power dissipation of less than 10 mW.

An improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a 5 V supply. The loading speed has also been increased for compatibility with most microprocessors.

Featuring operation from 5 V to 15 V, the AD7524-EP interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524-EP an ideal choice for many microprocessor controlled gain setting and signal control applications.

Additional application and technical information can be found in the AD7524 data sheet.

Rev. 0

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REVISION HISTORY

1/12—Revision 0: Initial Version

SPECIFICATIONS

V_{REF} = 10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise noted. Temperature range goes from −55°C to +125°C.

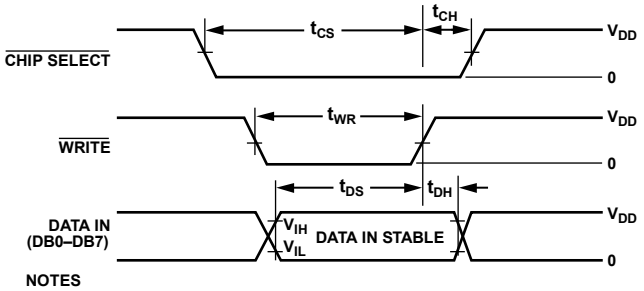
Table 1.

Parameter	Limit, T_A = 25°C		Limit, T_{MIN}, T_{MAX}[1]		Unit	Test Conditions/ Comments
	V_{DD} = 5 V	V_{DD} = 15 V	V_{DD} = 5 V	V_{DD} = 15 V		
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy	±1/2	±1/2	±1/2	±1/2	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error[2]	±2½	±1¼	±3½	±1½	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC measured from 25°C to T_{MIN} or from 25°C to T_{MAX}
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$[3]	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0 to DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0 to DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
DYNAMIC PERFORMANCE						
Output Current Settling Time (to ½ LSB)[3]	400	250	500	350	ns max	OUT1 load = 100 Ω, C_{EXT} = 13 pF; $\overline{WR}$, $\overline{CS}$ = 0 V; DB0 to DB7 = 0 V to V_{DD} to 0 V
AC Feedthrough[3]						
At OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10 V, 100 kHz sine wave; DB0 to DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
At OUT2	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10 V, 100 kHz sine wave; DB0 to DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
REFERENCE INPUT						
R_{IN} (Pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (Pin 1)	120	120	120	120	pF max	DB0 to DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	30	30	30	30	pF max	
C_{OUT1} (Pin 1)	30	30	30	30	pF max	DB0 to DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input High Voltage Requirement, V_{IH}	2.4	13.5	2.4	13.5	V min	
Input Low Voltage Requirement, V_{IL}	0.8	1.5	0.5	1.5	V max	
Input Current, I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]						
DB0 to DB7	5	5	5	5	pF max	V_{IN} = 0 V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0 V

Parameter	Limit, T_A = 25°C V_{DD} = 5 V	Limit, T_A = 25°C V_{DD} = 15 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = 5 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = 15 V	Unit	Test Conditions/ Comments
SWITCHING CHARACTERISTICS						See Figure 2
Chip Select to Write Setup Time, t_{CS}[5]	170	100	240	150	ns min	$t_{WR} = t_{CS}$
Chip Select to Write Hold Time, t_{CH}	0	0	0	0	ns min	
Write Pulse Width, t_{WR}	170	100	240	150	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
Data Setup Time, t_{DS}	135	60	170	100	ns min	
Data Hold Time, t_{DH}	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All digital inputs V_{IL} or V_{IH}
	100	100	500	500	µA max	All digital inputs 0 V or V_{DD}

[1] Temperature range is as follows: −55°C to +125°C.
[2] Gain error is measured using internal feedback resistor. Full-scale range (FSR) = V_{REF}.
[3] Guaranteed not tested.
[4] DAC thin-film resistor temperature coefficient is approximately −300 ppm/°C.
[5] AC parameter, sample tested @ 25°C to ensure conformance to specification.

WRITE CYCLE TIMING DIAGRAM



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = 5V, $t_R = t_F$ = 20ns; V_{DD} = 15V, $t_R = t_F$ = 40ns.

2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

3. $t_{DS} + t_{DH}$ IS APPROXIMATELY CONSTANT AT 145ns MIN AT 25°C, V_{DD} = 5V AND t_{WR} 170ns MIN. THE AD7524 IS SPECIFIED FOR A MINIMUM t_{DH} OF 10ns. HOWEVER, IN APPLICATIONS WHERE t_{DH} > 10ns, t_{DS} MAY BE REDUCED ACCORDINGLY UP TO THE LIMIT t_{DS} = 65ns, t_{DH} = 80ns.

01132-002

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +17 V
$V_{R_{FEEDBACK}}$ to GND	±25 V
V_{REF} to GND	±25 V
Digital Input Voltage to GND	−0.3 V to V_{DD} +0.3 V
OUT1, OUT2 to GND	−0.3 V to V_{DD} +0.3 V
Power Dissipation (Any Package)	
To 75°C	450 mW
Derates above 75°C by	6 mW/°C
Operating Temperature, Extended	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

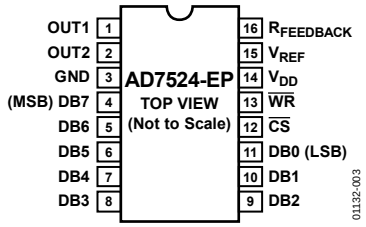


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	DAC Current Output.
2	OUT2	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	GND	Ground.
4	DB7 (MSB) to DB0 (LSB)	Parallel Data Bit 7 to Data Bit 0.
12	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with $\overline{WR}$ to load parallel data to the input latch.
13	$\overline{WR}$	Write. When low, use in conjunction with $\overline{CS}$ to load parallel data.
14	V_{DD}	Positive Power Supply Input. These parts can be operated with a supply of 5 V.
15	V_{REF}	DAC Reference Voltage Input Terminal.
16	$R_{FEEDBACK}$	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.

OUTLINE DIMENSIONS

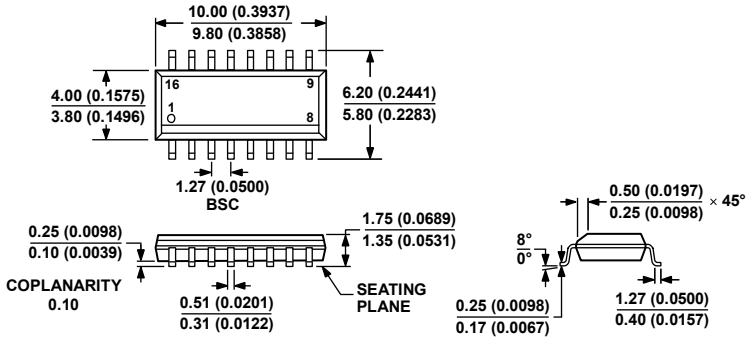


Figure 4. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Nonlinearity (V_{DD} = 15 V)	Temperature Range	Package Description	Package Option
AD7524SR-EP	±0.5 LSB	−55°C to +125°C	16-Lead SOIC_N	R-16
AD7524SR-EP-RL7	±0.5 LSB	−55°C to +125°C	16-Lead SOIC_N	R-16

NOTES