100 mA, Low Quiescent Current, CMOS Linear Regulator

ADP120

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- Output voltage range: 1.2 V to 3.3 V
- Output current: 100 mA
- Low quiescent current
  - I_{GND} = 11 µA with zero load
  - I_{GND} = 22 µA with 100 mA load
- Low shutdown current: <1 µA
- Low dropout voltage
  - 60 mV @ 100 mA load
- High PSRR
  - 73 dB @ 1 kHz at V_{OUT} = 1.2 V
  - 70 dB @ 10 kHz at V_{OUT} = 1.2 V
- Low noise: 40 µV rms at V_{OUT} = 1.2 V
- No noise bypass capacitor required
- Initial accuracy: ±1%
- Stable with small 1 µF ceramic output capacitor
- Current-limit and thermal overload protection
- Logic controlled enable
- 5-lead TSOT package
- 4-ball 0.4 mm pitch WLCSP

APPLICATIONS

- Mobile phones
- Digital camera and audio devices
- Portable and battery-powered equipment
- Post regulation

TYPICAL APPLICATIONS CIRCUITS

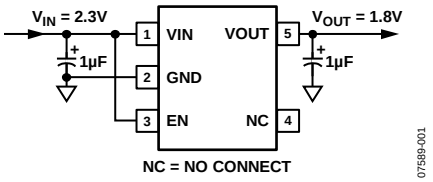

Figure 1. ADP120 TSOT with Fixed Output Voltage, 1.8 V

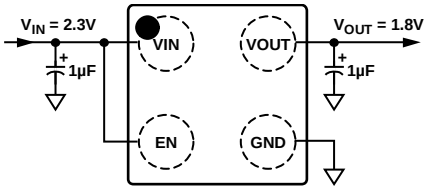

Figure 2. ADP120 WLCSP with Fixed Output Voltage, 1.8 V

GENERAL DESCRIPTION

The ADP120 is a low quiescent current, low dropout, linear regulator that operates from 2.3 V to 5.5 V and provides up to 100 mA of output current. The low 60 mV dropout voltage at 100 mA load improves efficiency and allows operation over a wide input voltage range. The low 22 µA of quiescent current at full load makes the ADP120 ideal for battery-operated portable equipment.

The ADP120 is available in output voltages ranging from 1.2 V to 3.3 V. The part is optimized for stable operation with small 1 µF ceramic output capacitors. The ADP120 delivers good transient performance with minimal board area.

Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP120 is available in a tiny 5-lead TSOT and a 4-ball 0.4 mm pitch WLCSP and utilizes the smallest footprint solution for use in a variety of portable applications.

Rev. B

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ADP120* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1072: How to Successfully Apply Low Dropout Regulators

Data Sheet

- ADP120: 100mA, Low Quiescent Current, CMOS Linear Regulator Data Sheet

TOOLS AND SIMULATIONS

- ADI Linear Regulator Design Tool and Parametric Search
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE DESIGNS

- CN0214

DESIGN RESOURCES

- ADP120 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP120 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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Added Figure 50 17
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7/08—Rev. 0 to Rev. A

Deleted ADP120-1 ..... Universal
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6/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 2.3 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.3		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		11		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			21	µA
		I_{OUT} = 10 mA		15		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			29	µA
		I_{OUT} = 100 mA		22		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			35	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.5	µA
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 100 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−2		+2	%
		100 µA < I_{OUT} < 100 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−2.5		+2.5	%
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, I_{OUT} = 1 mA, T_J = −40°C to +125°C	−0.03		+0.03	%/V
Load Regulation[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 100 mA		0.001		%/mA
		I_{OUT} = 1 mA to 100 mA, T_J = −40°C to +125°C			0.005	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	V_{OUT} = 3.3 V				
TSOT		I_{OUT} = 10 mA		8		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			12	mV
		I_{OUT} = 100 mA		80		mV
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			120	mV
WLCSP		I_{OUT} = 10 mA		6		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			9	mV
		I_{OUT} = 100 mA		60		mV
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			90	mV
START-UP TIME[3]	$t_{START-UP}$	V_{OUT} = 3.3 V		120		µs
CURRENT LIMIT THRESHOLD[4]	I_{LIMIT}		110	180	350	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.3 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.3 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = V_{IN} or GND		0.05		µA
		EN = V_{IN} or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			2.25	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	1.5			V
Hysteresis	$UVLO_{HYS}$			120		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		65		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		52		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 1.2 V		40		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	10 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		60		dB
		10 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		66		dB
		10 kHz, V_{IN} = 5 V, V_{OUT} = 1.2 V		70		dB

[1] Based on an endpoint calculation using 1 mA and 100 mA loads. See Figure 6 for typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.3 V.
[3] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 90% of its nominal value.
[4] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

RECOMMENDED SPECIFICATIONS: INPUT AND OUTPUT CAPACITORS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended, Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP120 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a four-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a four-layer, 4" × 3" PCB. Refer to JESD 51-7 and JESD 51-9 for detailed information regarding board construction. For additional information, see Application Note AN-617, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a four-layer board. JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8, JESD51-9, and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
4-Ball, 0.4 mm Pitch WLCSP	260	58	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

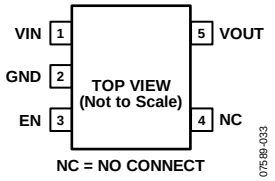

Figure 3. 5-Lead TSOT Pin Configuration

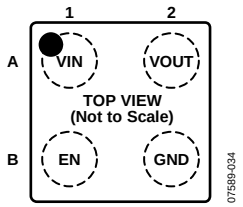

Figure 4. 4-Ball WLCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSOT	**WLCSP**	**Mnemonic**	**Description**
1	A1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	B2	GND	Ground.
3	B1	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	N/A	NC	No Connect. Not connected internally.
5	A2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

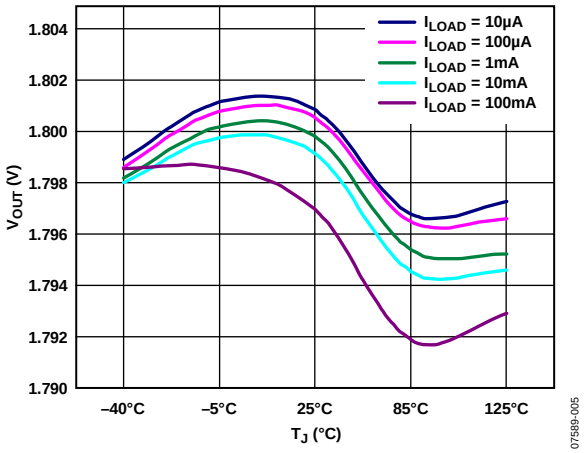

Figure 5. Output Voltage vs. Junction Temperature

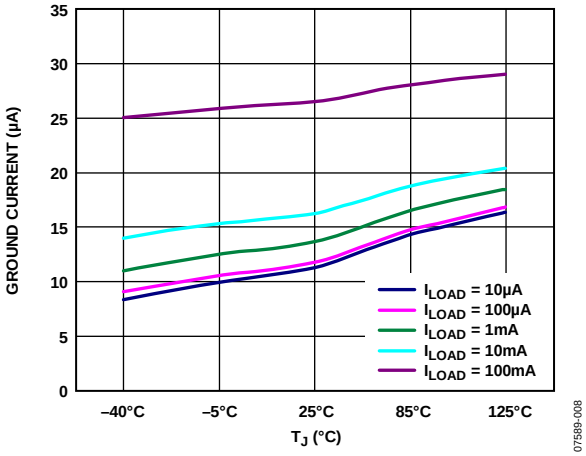

Figure 8. Ground Current vs. Junction Temperature

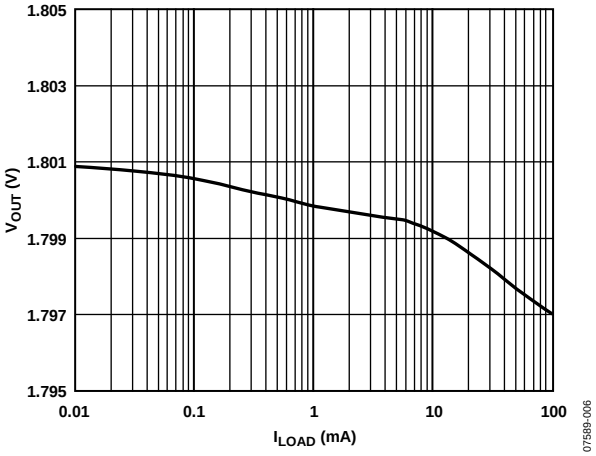

Figure 6. Output Voltage vs. Load Current

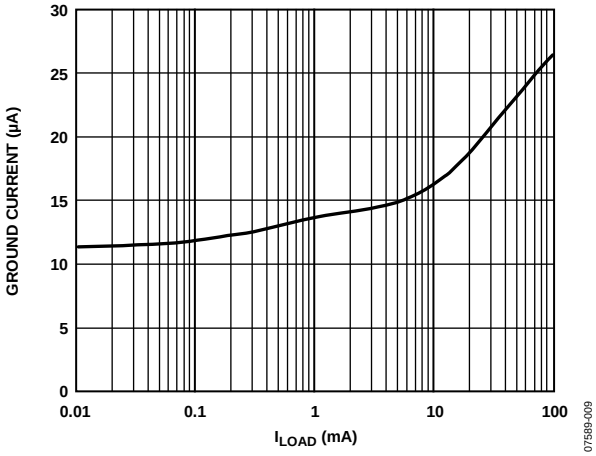

Figure 9. Ground Current vs. Load Current

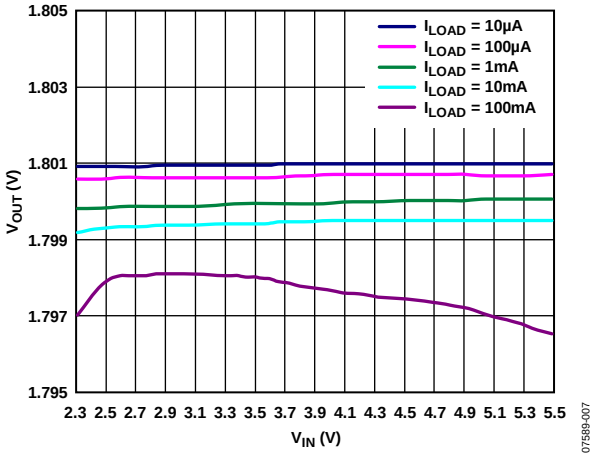

Figure 7. Output Voltage vs. Input Voltage

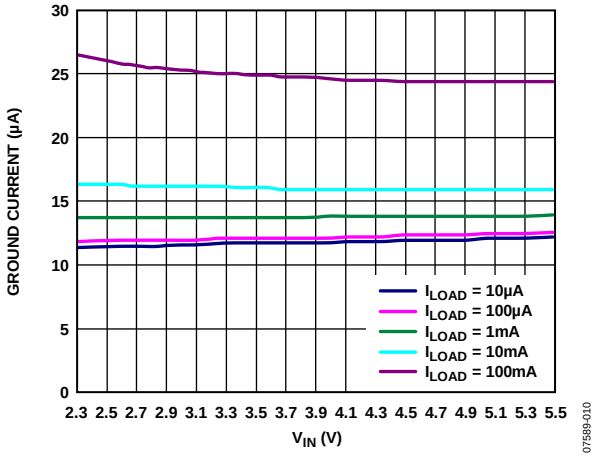

Figure 10. Ground Current vs. Input Voltage

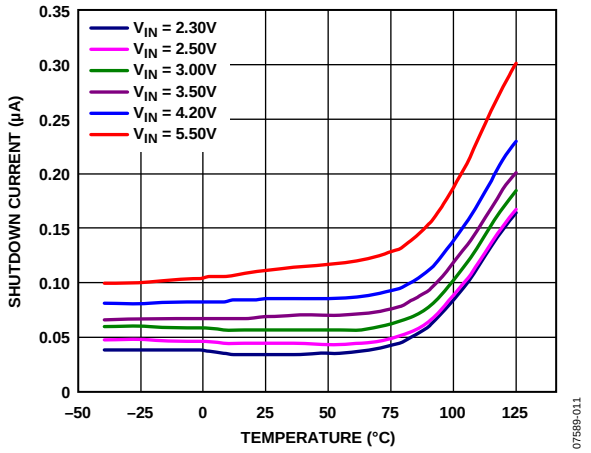

Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

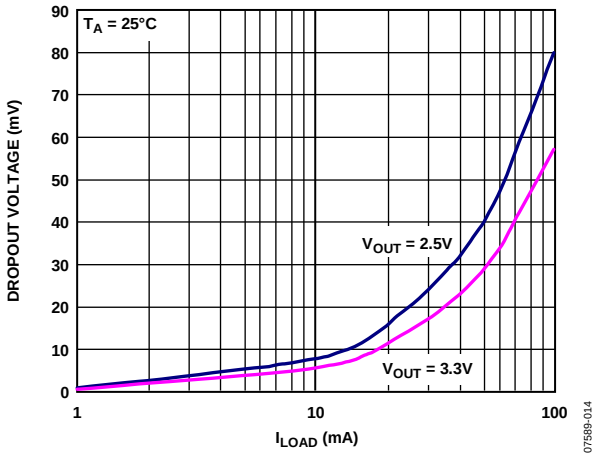

Figure 14. Dropout Voltage vs. Load Current, WLCSP, V_{OUT} = 2.5 V and 3.3 V

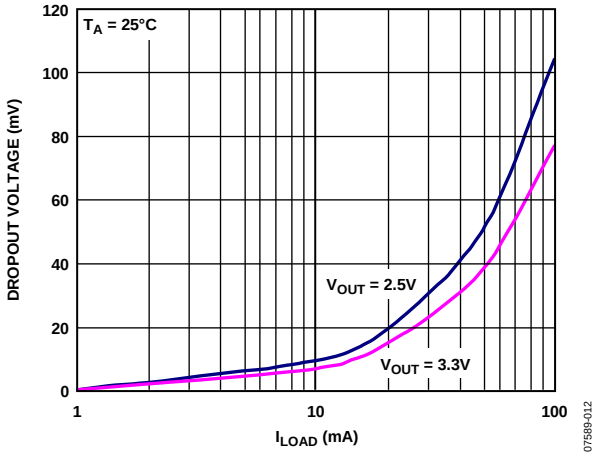

Figure 12. Dropout Voltage vs. Load Current, TSOT, V_{OUT} = 2.5 V and 3.3 V

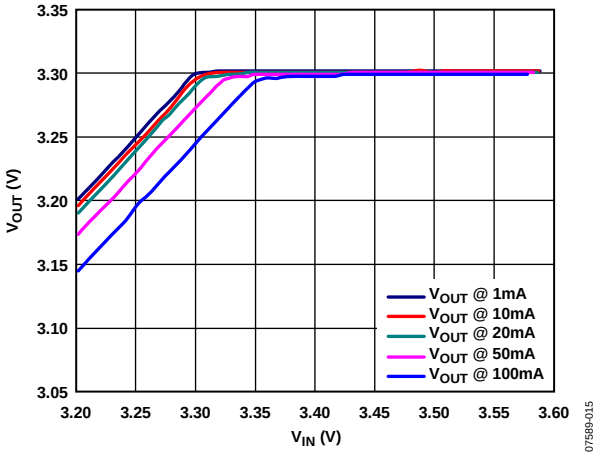

Figure 15. Output Voltage vs. Input Voltage (in Dropout), WLCSP, V_{OUT} = 3.3 V

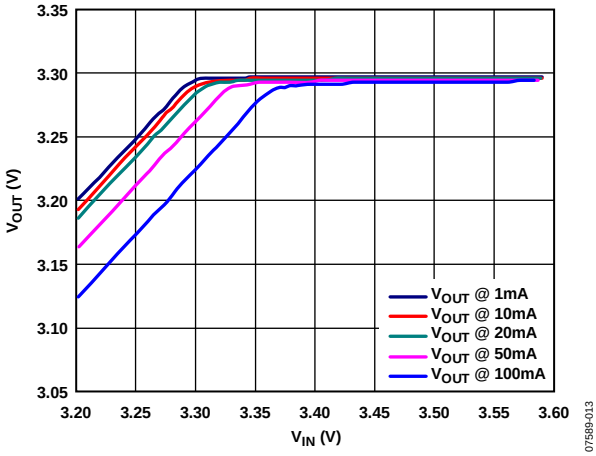

Figure 13. Output Voltage vs. Input Voltage (in Dropout), TSOT, V_{OUT} = 3.3 V

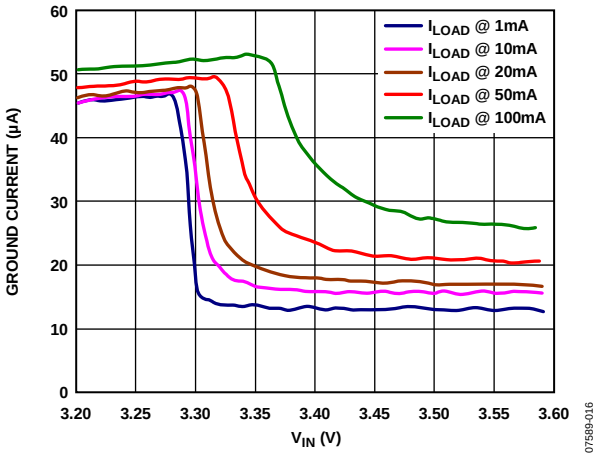

Figure 16. Ground Current vs. Input Voltage (in Dropout)

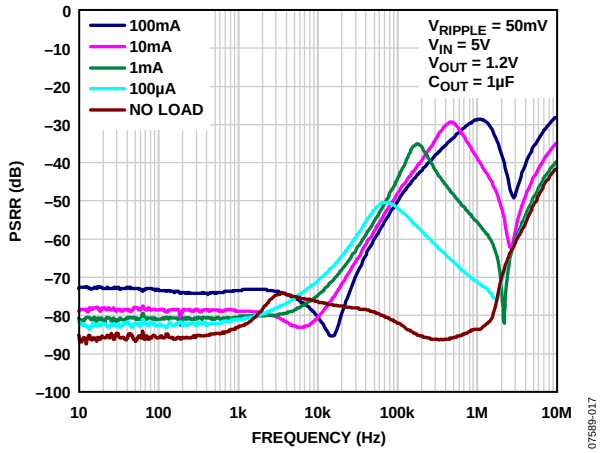

Figure 17. Power Supply Rejection Ratio vs. Frequency

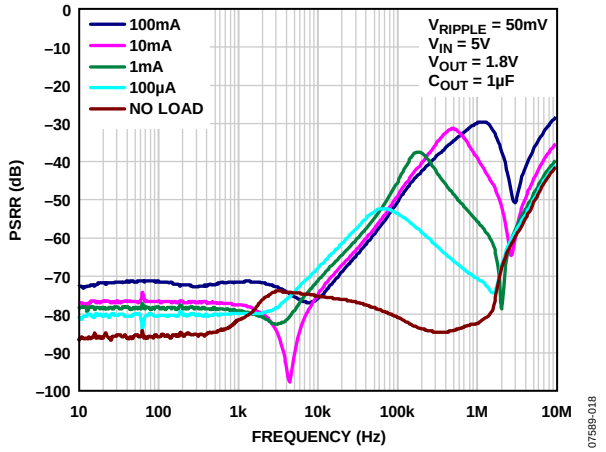

Figure 18. Power Supply Rejection Ratio vs. Frequency

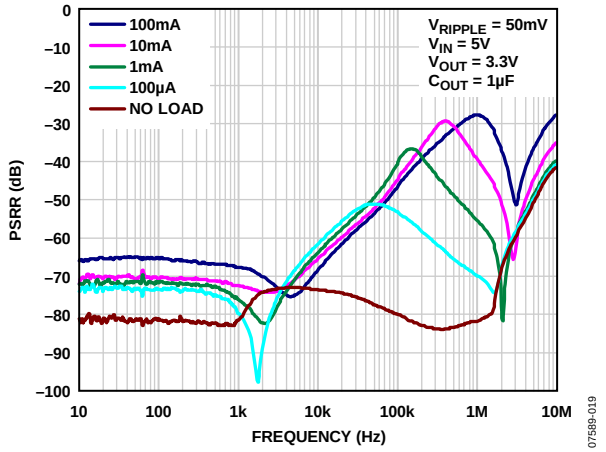

Figure 19. Power Supply Rejection Ratio vs. Frequency

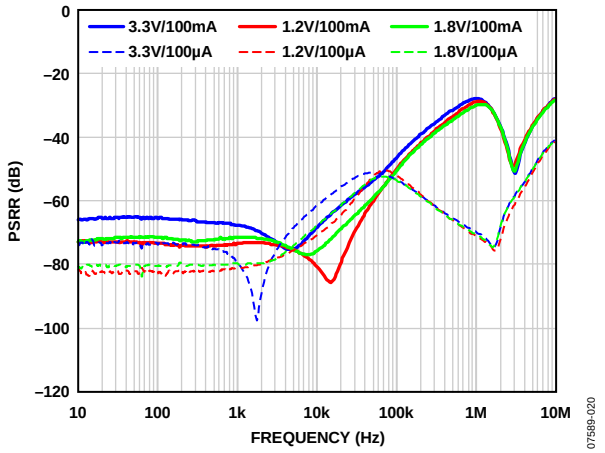

Figure 20. Power Supply Rejection Ratio vs. Frequency, Various Output Voltages and Load Currents

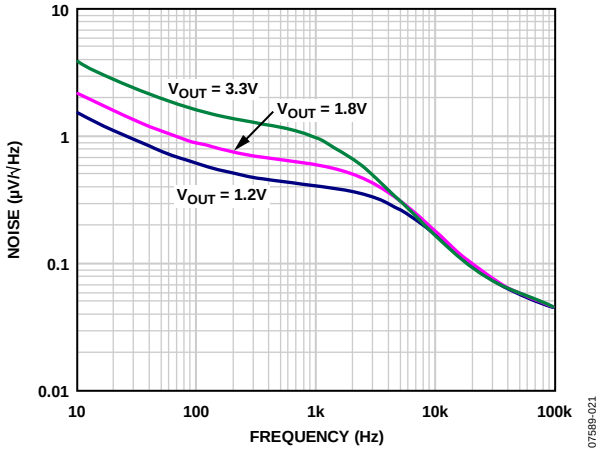

Figure 21. Output Noise Spectrum, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

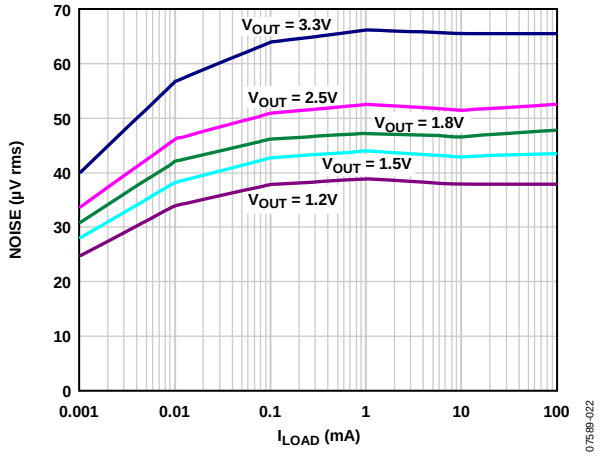

Figure 22. Output Noise vs. Load Current and Output Voltage
V_{IN} = 5 V, C_{OUT} = 1 µF

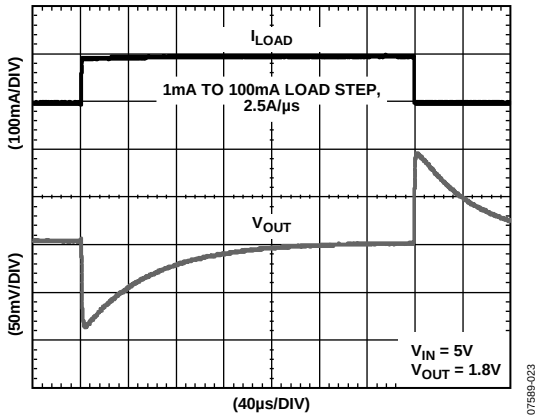

Figure 23. Load Transient Response, C_{IN} and C_{OUT} = 1 µF

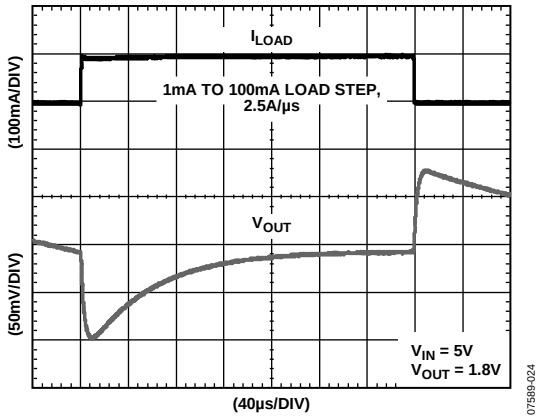

Figure 24. Load Transient Response, C_{IN} and C_{OUT} = 4.7 µF

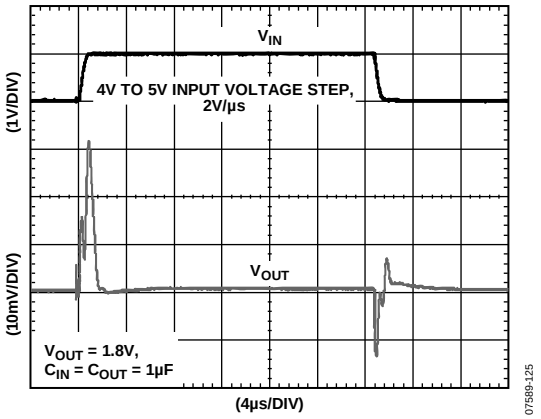

Figure 25. Line Transient Response, Load Current = 100 mA

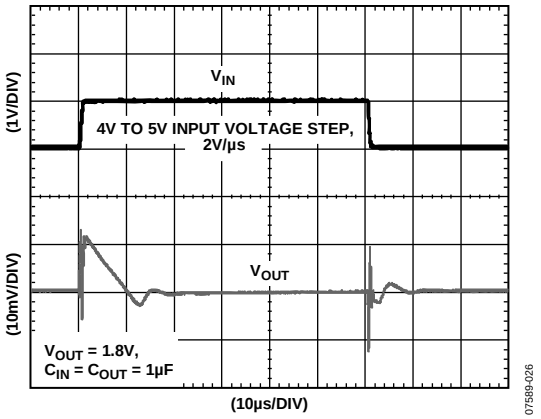

Figure 26. Line Transient Response, Load Current = 1 mA

THEORY OF OPERATION

The ADP120 is a low quiescent current, low dropout linear regulator that operates from 2.3 V to 5.5 V and provides up to 100 mA of output current. Drawing a low 22 µA of quiescent current (typical) at full load makes the ADP120 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP120 provides excellent transient performance.

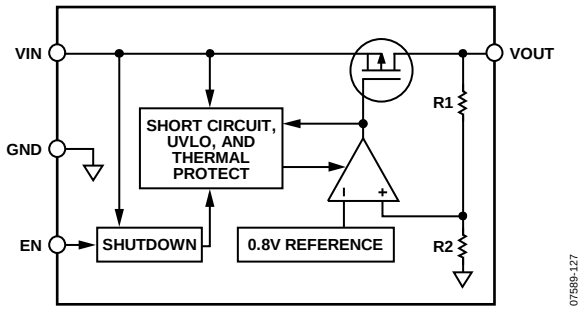

Figure 27. Internal Block Diagram

Internally, the ADP120 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP120 is available in output voltages ranging from 1.2 V to 3.3 V. The ADP120 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP120 is designed for operation with small, space-saving ceramic capacitors, but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP120. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP120 to large changes in load current. Figure 28 and Figure 29 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

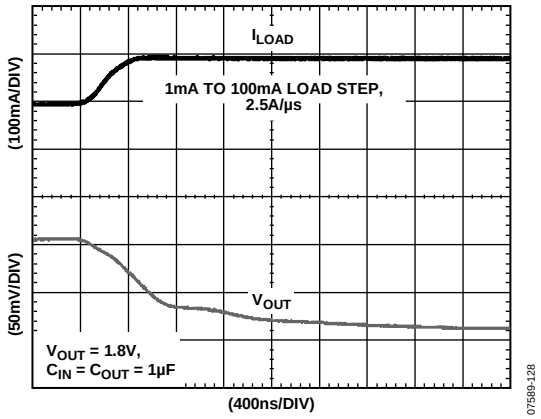

Figure 28. Output Transient Response, C_{OUT} = 1 µF

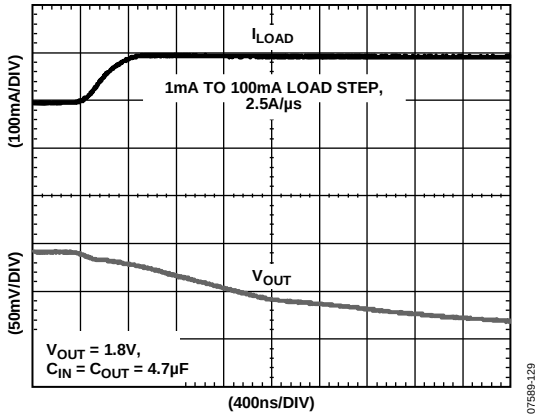

Figure 29. Output Transient Response, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP120, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 30 depicts the capacitance vs. voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

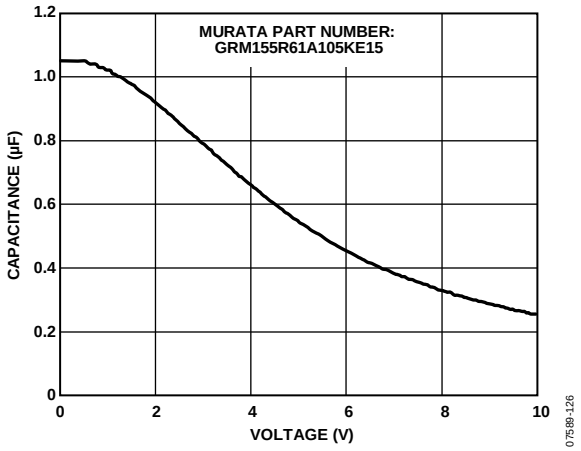

Figure 30. Capacitance vs. Voltage Characteristic

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, TEMPCO over −40°C to +85°C is assumed to be 15% for an X5R dielectric. TOL is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 30.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP120, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP120 has an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 2.2 V. This ensures that the inputs and the output of the ADP120 behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP120 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. Figure 31 shows a rising voltage on EN crossing the active threshold, and VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

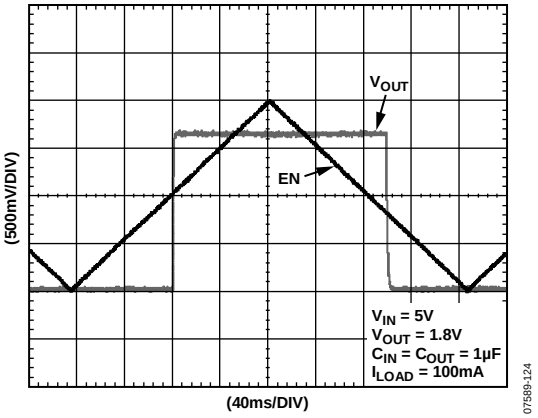

Figure 31. Typical EN Pin Operation

As shown in Figure 31, the EN pin has hysteresis built-in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage; therefore, these thresholds vary with changing input voltage. Figure 32 shows typical EN active/inactive thresholds when the input voltage varies from 2.3 V to 5.5 V.

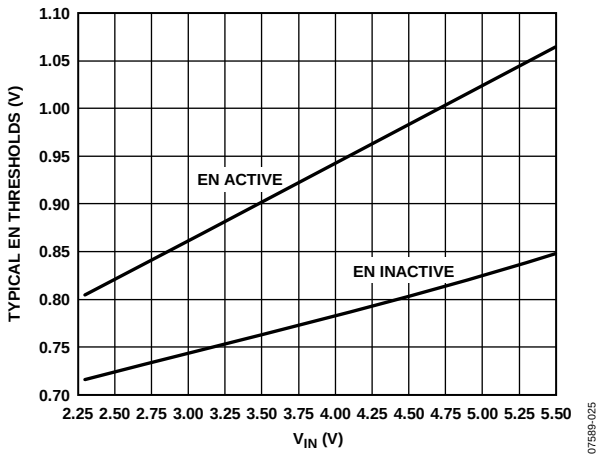

Figure 32. Typical EN Pin Thresholds vs. Input Voltage

The ADP120 utilizes an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 1.8 V option is approximately 120 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases.

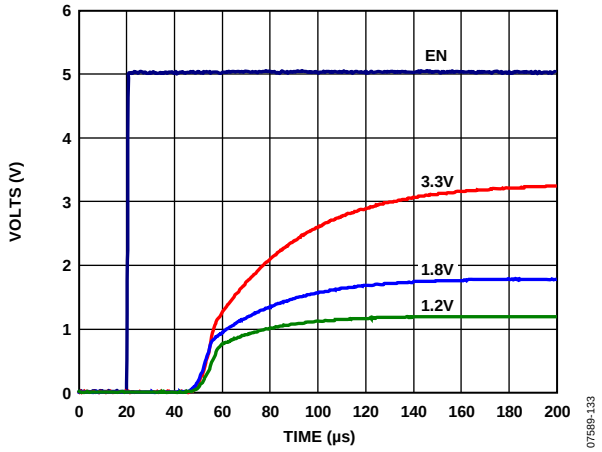

Figure 33. Typical Start-Up Time

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP120 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP120 is designed to current limit when the output load reaches 150 mA (typical). When the output load exceeds 150 mA, the output voltage reduces to maintain a constant current limit.

Thermal overload protection is built-in, limiting the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output turns off, reducing the output current to zero. When the junction temperature drops below 135°C, the output turns on again thereby restoring output current to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP120 current limits, conducting only 150 mA into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 150 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 150 mA and 0 mA that continues as long as the short remains at the output.

Current- and thermal-limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited to prevent junction temperatures from exceeding 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP120 does not dissipate much heat due to its high efficiency. However, in applications with high ambient temperature and high supply voltage-to-output voltage differential, the heat dissipated in the package is large enough to cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP120 must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB. Table 6 shows typical θ_{JA} values of the 5-lead TSOT and 4-ball WLCSP packages for various PCB copper sizes. Table 7 shows the typical Ψ_{JB} value of the 5-lead TSOT and 4-ball WLCSP.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	TSOT (°C/W)	WLCSP (°C/W)
0[1]	170	260
50	152	159
100	146	157
300	134	153
500	131	151

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

TSOT (°C/W)	WLCSP (°C/W)
42.8	58.4

The junction temperature of the ADP120 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. Figure 34 to Figure 47 show junction temperature calculations for different ambient temperatures, load currents, V_{IN}-to-V_{OUT} differentials, and areas of PCB copper.

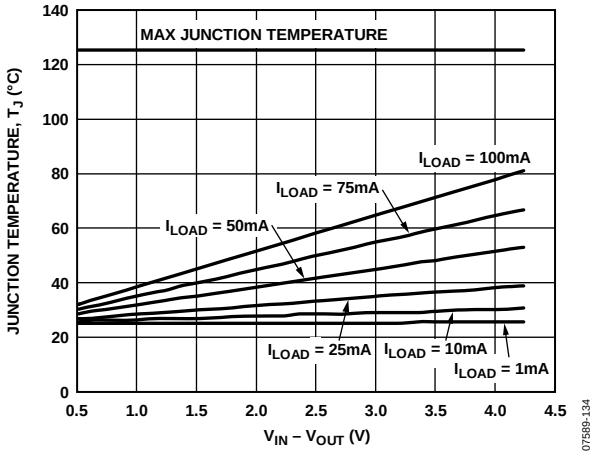

Figure 34. TSOT, 500 mm² of PCB Copper, T_A = 25°C

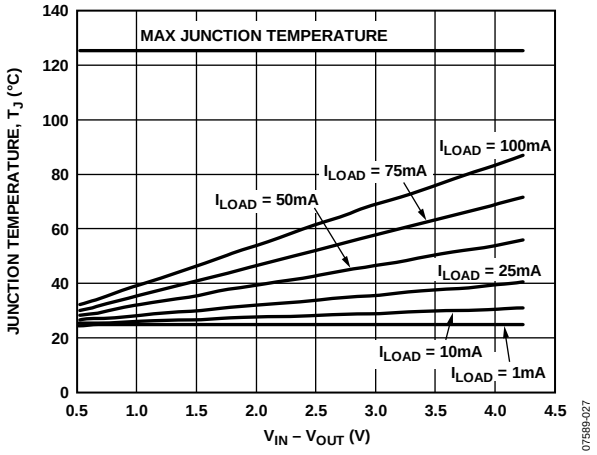

Figure 35. TSOT, 100 mm² of PCB Copper, T_A = 25°C

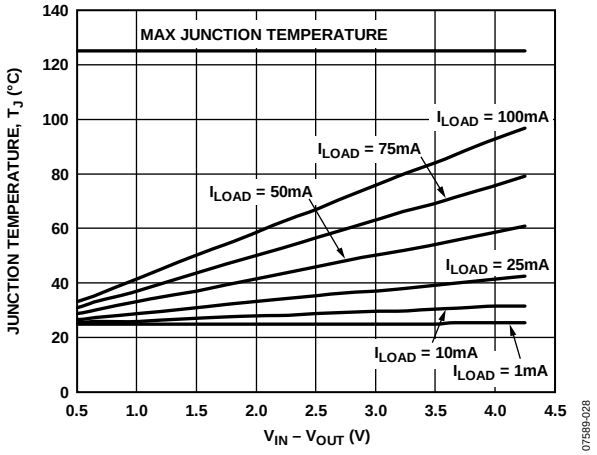

Figure 36. TSOT, 0 mm² of PCB Copper, T_A = 25°C

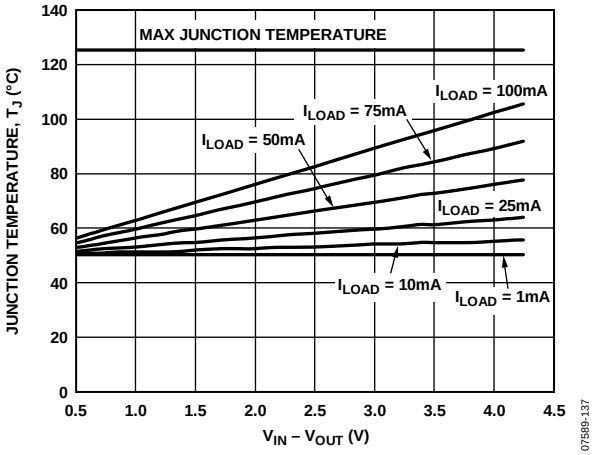

Figure 37. TSOT, 500 mm² of PCB Copper, T_A = 50°C

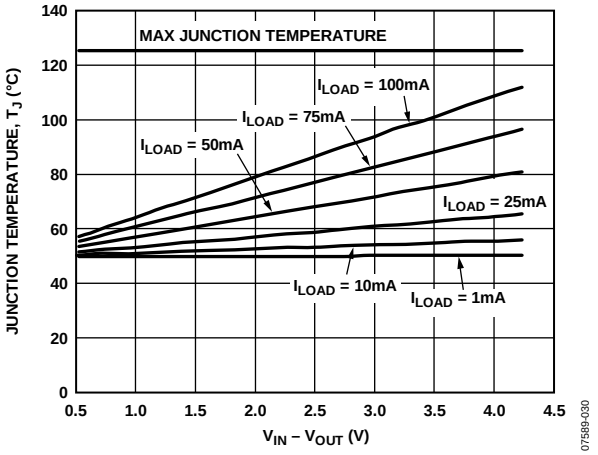

Figure 38. TSOT, 100 mm² of PCB Copper, T_A = 50°C

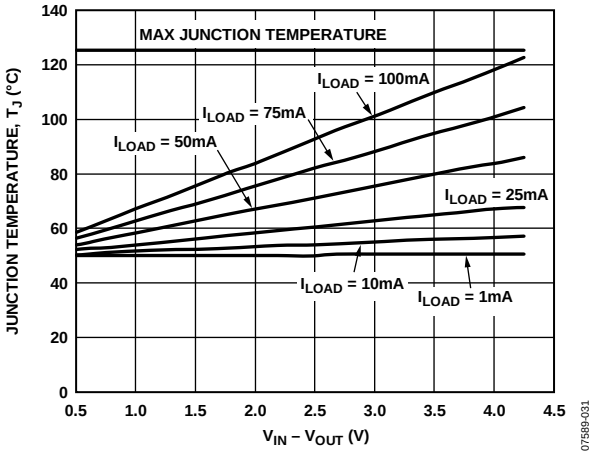

Figure 39. TSOT, 0 mm² of PCB Copper, T_A = 50°C

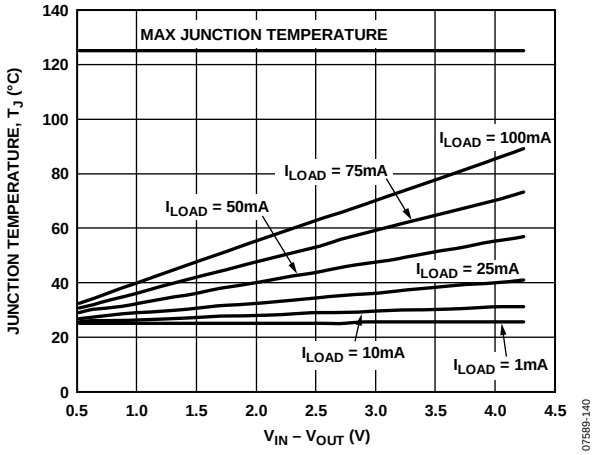

Figure 40. WLCSP, 500 mm² of PCB Copper, T_A = 25°C

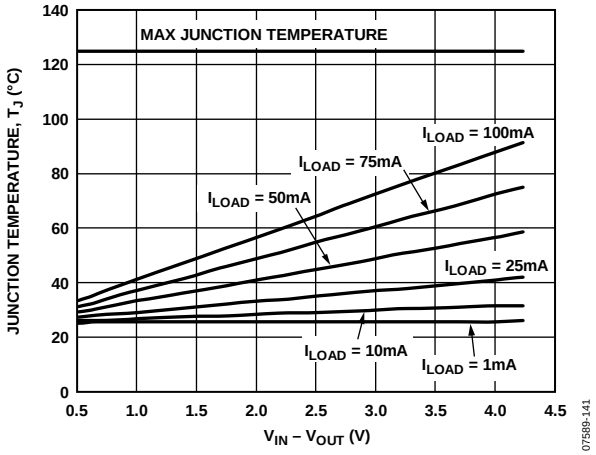

Figure 41. WLCSP, 100 mm² of PCB Copper, T_A = 25°C

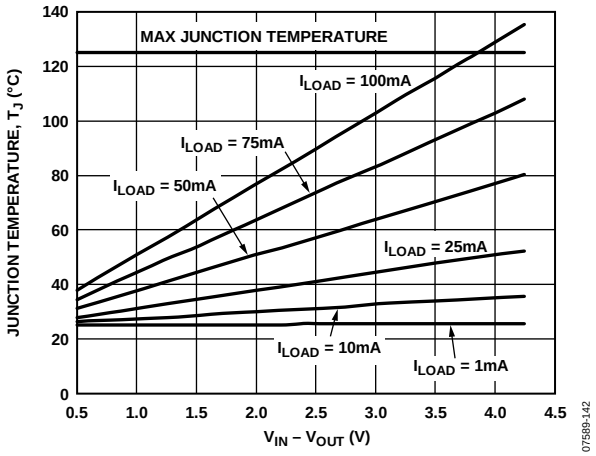

Figure 42. WLCSP, 0 mm² of PCB Copper, T_A = 25°C

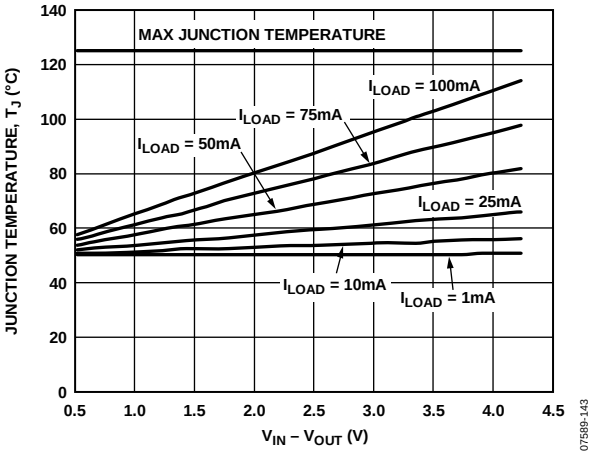

Figure 43. WLCSP, 500 mm² of PCB Copper, T_A = 50°C

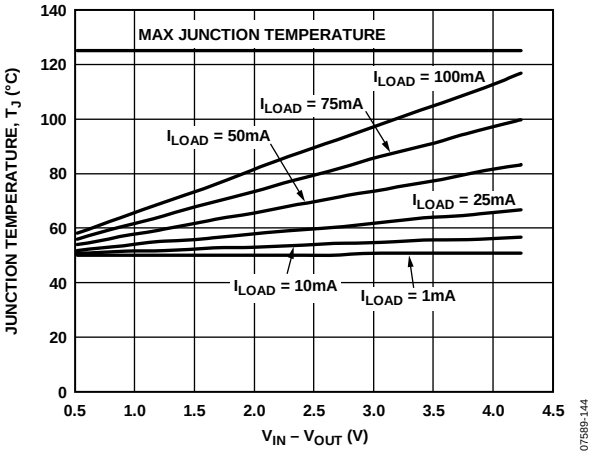

Figure 44. WLCSP, 100 mm² of PCB Copper, T_A = 50°C

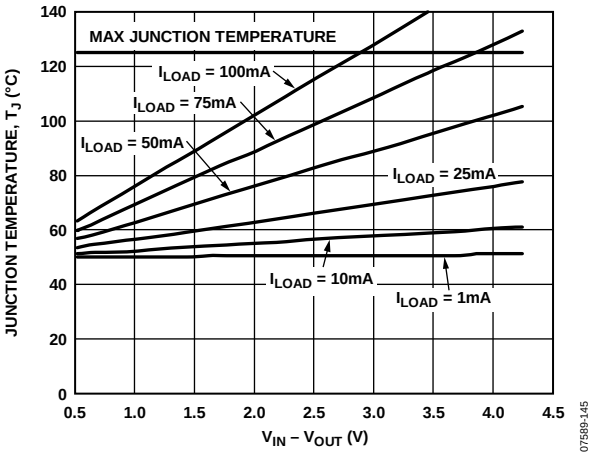

Figure 45. WLCSP, 0 mm² of PCB Copper, T_A = 50°C

In cases where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

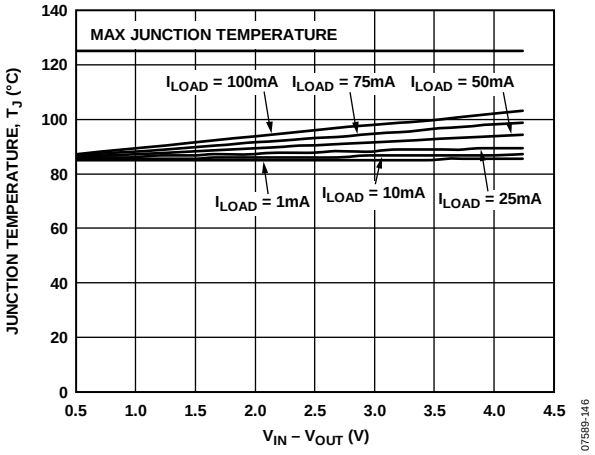

Figure 46. TSOT, T_B = 85°C

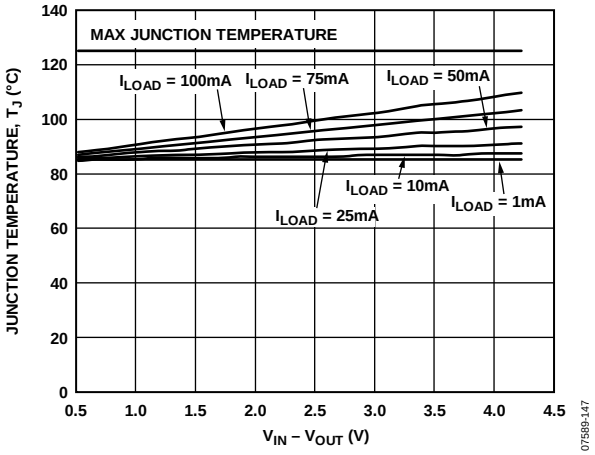

Figure 47. WLCSP, T_B = 85°C

PCB LAYOUT CONSIDERATIONS

Improve heat dissipation from the package by increasing the amount of copper attached to the pins of the ADP120. However, as listed in Table 6, a point of diminishing return is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402- or 0603-size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

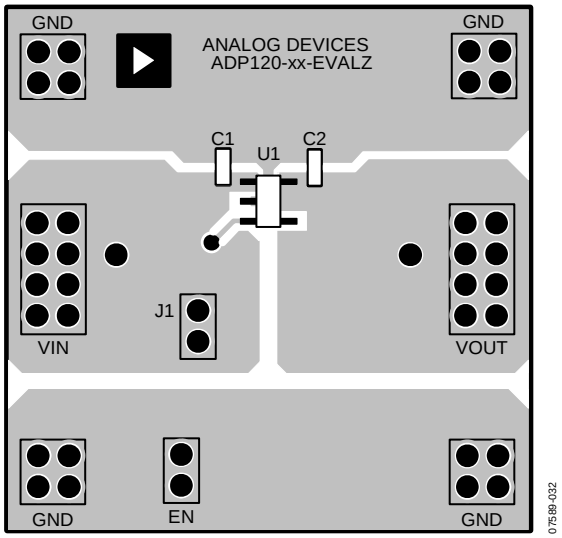

Figure 48. TSOT PCB Layout

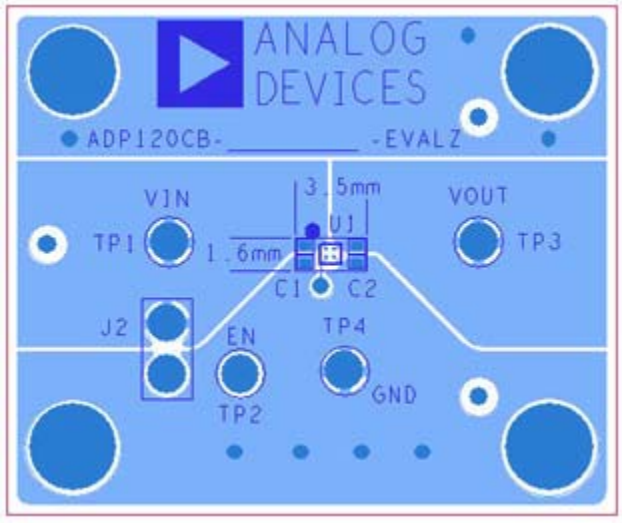

Figure 49. WLCSP PCB Layout—Top Side

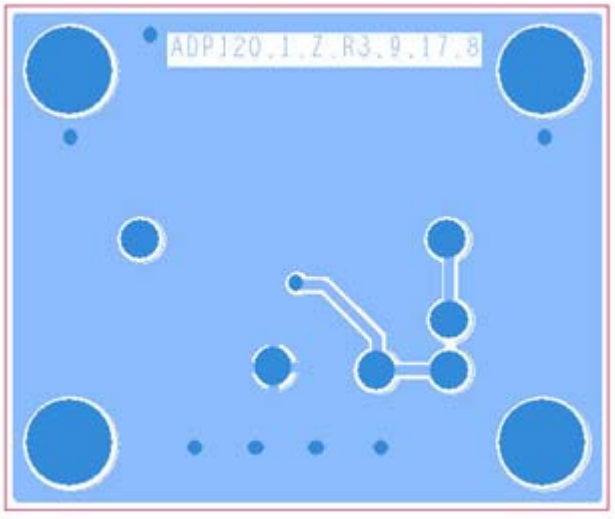

Figure 50. WLCSP PCB Layout—Bottom Side

OUTLINE DIMENSIONS

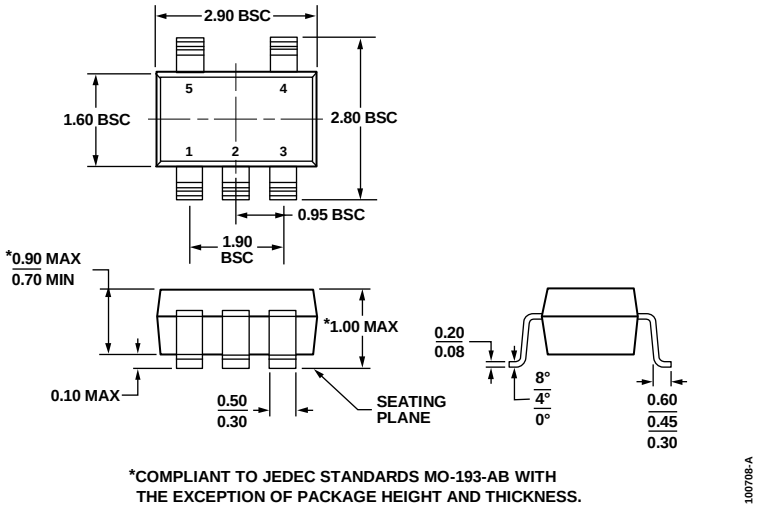

Figure 51. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

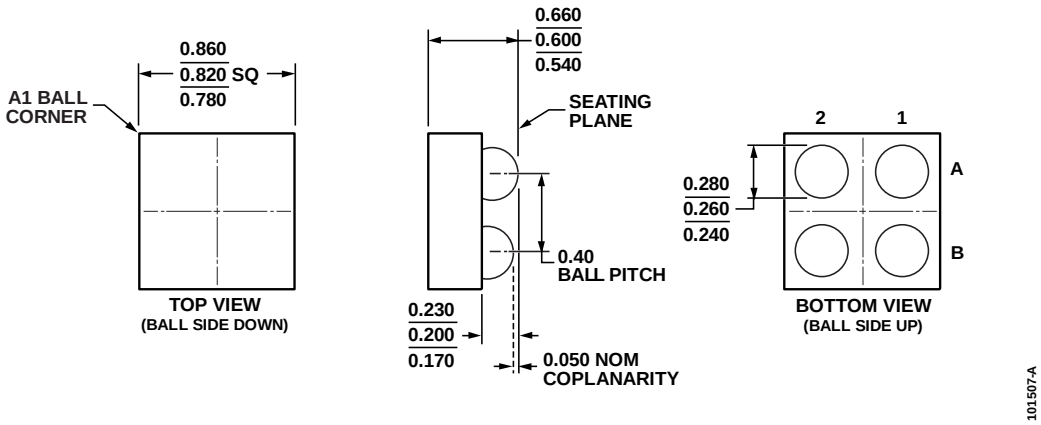

Figure 52. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP120-AUJZ12R7[3]	−40°C to +125°C	1.2	5-Lead TSOT	UJ-5	L9R
ADP120-AUJZ15R7[3]	−40°C to +125°C	1.5	5-Lead TSOT	UJ-5	L9Q
ADP120-AUJZ18R7[3]	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	L9P
ADP120-AUJZ33R7[3]	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	L9N
ADP120-ACBZ12R7[3]	−40°C to +125°C	1.2	4-Ball WLCSP	CB-4-2	LBJ
ADP120-ACBZ15R7[3]	−40°C to +125°C	1.5	4-Ball WLCSP	CB-4-2	LBK
ADP120-ACBZ25R7[3]	−40°C to +125°C	2.5	4-Ball WLCSP	CB-4-2	LBU
ADP120-ACBZ28R7[3]	−40°C to +125°C	2.8	4-Ball WLCSP	CB-4-2	LBW
ADP120-ACBZ30R7[3]	−40°C to +125°C	3.0	4-Ball WLCSP	CB-4-2	LBY
ADP120-18-EVALZ[3]		1.8	ADP120 1.8 V Output Evaluation Board		
ADP120-15-EVALZ[3]		1.5	ADP120 1.5 V Output Evaluation Board		
ADP120-12-EVALZ[3]		1.2	ADP120 1.2 V Output Evaluation Board		
ADP120CB-2.8-EVALZ[3]		2.8	ADP120 WLCSP 2.8 V Output Evaluation Board		
ADP120CB-2.5-EVALZ[3]		2.5	ADP120 WLCSP 2.5 V Output Evaluation Board		
ADP120CB-1.8-EVALZ[3]		1.8	ADP120 WLCSP 1.8 V Output Evaluation Board		
ADP120CB-1.5-EVALZ[3]		1.5	ADP120 WLCSP 1.5 V Output Evaluation Board		
ADP120CB-1.2-EVALZ[3]		1.2	ADP120 WLCSP 1.2 V Output Evaluation Board		
ADP120-BL1-EVZ[3]			Blank Evaluation Board		

[1] For new designs, see the ADP121.
[2] For additional voltage options, contact your local Analog Devices, Inc., sales or distribution representative.
[3] Z = RoHS Compliant Part.

NOTES

D07589-0-4/09(B)