6.0 GHz, Ultrahigh Dynamic Range, Differential Amplifier

Preliminary Technical Data

ADL5569

FEATURES

- –3 dB bandwidth of 6.0 GHz
- Preset 20 dB gain, can be reduced by adding external resistors
- Differential or single-ended input to differential output
- Internally dc-coupled inputs and outputs
- Low noise input stage: 7.9 dB noise figure at 2 GHz
- Low distortion at 5 V supply and 2 V p-p output with 100 Ω load
  - 500 MHz: –78 dBc (HD2), –70 dBc (HD3), –80 dBc (IMD3)
  - 2 GHz: –61 dBc (HD2), –52 dBc (HD3), –64 dBc (IMD3)
- Slew rate: 23 V/ns at 2 V p-p output
- DC power consumption: 86 mA per amplifier at 5 V

APPLICATIONS

- Differential ADC drivers
- Single-ended to differential conversion
- RF/IF gain blocks
- SAW filter interfacing
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

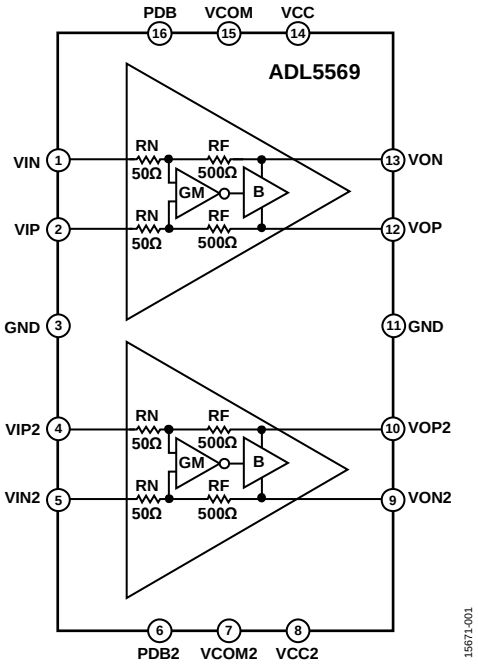

Figure 1.

GENERAL DESCRIPTION

The ADL5569 is a high performance, dual, differential amplifier with 20 dB of voltage gain, optimized for applications spanning from dc to 6.0 GHz. The amplifier is available in a dual format, and it offers a low referred to input (RTI) noise of 1.0 nV/√Hz (at 500 MHz) and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 12-bit to 16-bit analog-to-digital converters (ADCs). The ADL5569 is ideally suited for use in high performance zero intermediate frequency (IF) and complex IF receiver designs. In addition, this device has excellent low distortion for single-ended input driver applications.

Using two external series resistors for each amplifier expands the gain flexibility of the amplifier and allows any gain selection from 6 dB to 20 dB for a differential input. For a single-ended input, the gain can be adjusted from 6 dB to 17 dB. In addition, this device maintains low distortion through its output common-mode range of 2 V to 3 V, providing a flexible capability for driving ADCs with ac levels up to 2 V p-p.

Operating from a single 5 V supply, the quiescent current of the ADL5569 is typically 86 mA per amplifier. When disabled, the amplifiers consumes only 16 mA for both amplifiers.

The device is optimized for wideband, low distortion, and low noise operation, giving it unprecedented spurious-free dynamic range (SFDR) from dc to 4 GHz. These attributes, together with its adjustable gain capability, make this device the amplifier of choice for driving a wide variety of ADCs, mixers, pin diode attenuators, surface acoustic wave (SAW) filters, and a multiplicity of discrete RF devices.

Fabricated on an Analog Devices, Inc., high speed silicon germanium (SiGe) process, the ADL5569 is supplied in a compact 2.5 mm × 3 mm, 16-lead LFCSP package, and operates over the −40°C to +85°C temperature range.

Rev. PrB Document Feedback

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SPECIFICATIONS

Supply voltage (V_S) = 5 V, output common-mode voltage (V_{COMx}) = V_S/2, source impedance (R_S) = 100 Ω differential, load impedance (R_L) = 100 Ω differential, output voltage (V_{OUT}) = 2 V p-p composite, frequency = 500 MHz, T_A = 25°C, parameters specified for differential input and differential output, signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} ≤ 0.5 V p-p		6.0		GHz
Bandwidth, 1.0 dB Flatness	V_{OUT} ≤ 1.0 V p-p		TBD		MHz
Voltage Gain (A_V)					
Differential Input	R_L = open		20		dB
	R_L = 100 Ω differential	6	19		dB
Single-Ended Input	R_L = 100 Ω differential	6	17		dB
Gain Accuracy			±0.2		dB
Gain Supply Sensitivity	V_S ± 5%				mdB/V
Gain Temperature Sensitivity	T_A = −40°C to +85°C				mdB/°C
Slew Rate	Rising, V_{OUT} = 2 V p-p step		23.5		V/ns
	Falling, V_{OUT} = 2 V p-p step		23.5		V/ns
Settling Time	2 V step to 1%		500		ps
Overdrive Recovery Time	Differential input voltage step from 2 V to 0 V, for V_{OUT} ≤ ±10 mV		TBD		ns
Reverse Isolation (SDD12)			TBD		dB
Input to Output Isolation When Disabled	100 MHz; PDBx = low				dB
INPUT/OUTPUT CHARACTERISTICS					
Input Common-Mode Range		1.3		3.5	V
Input Resistance					
Differential			100		Ω
Single-Ended			91.7		Ω
Input Capacitance (Single-Ended)					pF
Common-Mode Rejection Ratio (CMRR)	Frequency = 500 MHz		TBD		dB
Output Common-Mode Range	VCOMx	2.0		3.0	V
VCOM, VCOM2 Input Impedance			TBD		
Output, Common Mode	Referenced to V_{COMx} (V_S/2)		TBD		mV
Offset					
Drift	T_A = −40°C to +85°C		TBD		mV/°C
Output Differential Offset			TBD		mV
Voltage					
Drift	T_A = −40°C to +85°C		TBD		µV/°C
Output Resistance (Differential)			0.51		Ω
Maximum Output Voltage Swing	1 dB compression point		6.5		Vp-p
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Digital Input Voltage	PDB, PDB2				
Logic High (V_{IH})		2.1		3.45	V
Logic Low (V_{IL})		0		1.0	V
PDB Input Current	PDB = 3 V		−7		µA
	PDB = 0 V		−70		µA
Supply Current (I_{SUPPLY})	Each amplifier				
Quiescent, each amplifier	PDB = high		86		mA
Disabled (Power Down), Each Amplifier	PDB = low		8		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE/HARMONIC PERFORMANCE					
100 MHz					
Second Harmonic Distortion (HD2)			–83		dBc
Third Harmonic Distortion (HD3)			–80		dBc
Output Third-Order Intercept (OIP3)			42		dBm
Third-Order Intermodulation Distortion (IMD3)			–82		dBc
Output Second-Order Intercept (OIP2)			TBD		dBm
Second-Order Intermodulation Distortion (IMD2)			TBD		dBc
Output 1 dB Compression Point (OP1dB)			TBD		dBm
Noise Figure (NF)			5.3		dB
Noise Spectral Density (NSD), RTI[1]					nV/√Hz
500 MHz					
HD2			–78		dBc
HD3			–70		dBc
OIP3			41		dBm
IMD3			–80		dBc
OIP2			TBD		dBm
IMD2			TBD		dBc
NF			5.3		dB
NSD, RTI			1.0		nV/√Hz
1000 MHz					
HD2			–72		dBc
HD3			–58		dBc
OIP3			38		dBm
IMD3			–74		dBc
OIP2			TBD		dBm
IMD2			TBD		dBc
NF			5.6		dB
NSD, RTI					nV/√Hz
2000 MHz					
HD2			–61		dBc
HD3			–52		dBc
OIP3			33		dBm
IMD3			–64		dBc
OIP2			TBD		dBm
IMD2			TBD		dBc
NF			7.9		dB
NSD, RTI			TBD		nV/√Hz
3000 MHz					
HD2			-56		dBc
HD3			-45		dBc
OIP3			28		dBm
IMD3			–54		dBc
OIP2			TBD		dBm
IMD2			TBD		dBc
NF			9.8		dB
NSD, RTI			TBD		nV/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
4000 MHz					
HD2			-50		dBc
HD3			-50		dBc
OIP3			21		dBm
IMD3			−40		dBc
OIP2			TBD		dBm
IMD2			TBD		dBc
NF			11.2		dB
NSD, RTI			TBD		nV/√Hz

[1] NSD RTI is calculated from NF, as follows:

$$NSD\ (RTI) = ½ \times \sqrt{4kT \times (10^{NF/10} - 1) \times R_{IN}}$$

where:
k is Boltzmann's constant, which equals 1.381×10^{-23} J/K.
T is the standard absolute temperature for evaluating noise figure, which equals 290 K.
R_{IN} is the differential input impedance of each amplifier, which equals 100 Ω.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Output Voltage Swing × Bandwidth Product	5 V-GHz
Supply Voltage (V_S) at VCC, VCC2	5.25 V
VIPx, VINx	V_S + 0.5 V
Maximum Output Current, I_{OUT} (VIPx and VINx Pins)	±30 mA
Internal Power Dissipation	1 W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-16-44	90.5	20.9	°C/W

[1] Measured on Analog Devices evaluation board.
[2] Based on simulation with JEDEC standard JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

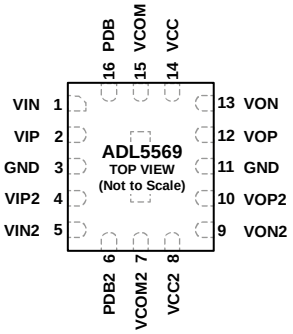

Figure 2 .Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Negative side of Balanced Differential Inputs for Amplifier 1. This pin is biased to $V_{VCC1}/2$, and is typically ac-coupled.
2	VIP	Positive side of Balanced Differential Inputs for Amplifier 1. This pin is biased to $V_{VCC1}/2$, and is typically ac-coupled.
3,11	GND	Ground. Ground Reference for the whole chip, and must be soldered to a low impedance ground plane.
4	VIP2	Positive Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to $V_{VCC2}/2$, and is typically ac-coupled.
5	VIN2	Negative Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to $V_{VCC2}/2$, and is typically ac-coupled.
6	PDB2	Power Down Control (active low) for Amplifier 2. This pin is internally pulled up to about 2.8 V. A logic high on this pin ($2.1\ V < V_{PDB2} < 3.3\ V$) enables the device.
7	VCOM2	Common-Mode Voltage Input for Amplifier 2. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of the amplifier. If left open, $V_{VCOM2} = V_{CC2}/2$. Decouple this pin to ground with a 0.1 µF capacitor.
8	VCC2	Positive Supply for Amplifier 2.
9	VON2	Negative side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2}, and is typically ac-coupled.
10	VOP2	Positive side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2}, and is typically ac-coupled.
12	VOP	Positive side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM}, and is typically ac-coupled.
13	VON	Negative side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM}, and is typically ac-coupled.
14	VCC	Positive Supply for the Amplifier 1.
15	VCOM	Common-Mode Voltage Input for Amplifier 1. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of the amplifier. If left open, $V_{VCOM} = V_{CC}/2$. Decouple this pin to ground with a 0.1 µF capacitor.
16	PDB	Power Down Control (Active Low) for Amplifier 1. This pin is internally pulled up to about 2.8 V. A logic high on this pin ($2.1\ V < V_{PDB} < 3.3\ V$) enables the device.
EP	GND	Exposed Pad. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

THEORY OF OPERATION

The ADL5569 is a high gain, fully differential dual amplifier/ADC driver that operates on a single power supply voltage (V_S) of 5 V. Internal resistors preset the gain to 20 dB, and external resistors can be added to reduce this gain. The −3 dB bandwidth is 6.0 GHz, and it has a differential input impedance of 100 Ω. It has a differential output impedance of 0.5 Ω and an operating output common-mode voltage range of 2.0 V to 3.0 V with 5 V supply.

The ADL5569 is composed of a pair of fully differential amplifiers with on-chip feedback and feedforward resistors. The gain is fixed at 20 dB, but it can be reduced by adding two resistors in series with the two inputs. The amplifier provides a high differential open-loop gain and has an output common-mode circuit that enables the user to change the output common-mode voltage by applying a voltage to the VCOM or VCOM2 pin.

Each amplifier provides superior low distortion for frequencies near dc to beyond 2000 MHz, with low noise and low power consumption. This amplifier achieves an IMD3 of −82 dBc at 100 MHz, and −80 dBc IMD3 at 500 MHz for 2 V p-p operation. In addition, the ADL5569 can deliver 5 V p-p operation under heavy loads. The internal gain is set at 20 dB, and the device has a noise figure of 7.9 dB at 2 GHz. When comparing noise figure and distortion performance, this amplifier delivers the best in category SFDR.

The ADL5569 is very flexible in terms of input/output coupling. It can be ac-coupled or dc-coupled. For dc coupling, the output common-mode voltage can be adjusted (using the VCOM and VCOM2 pins) from 2.5 V to 0.5 V for VS at 3.3 V, and ground at −2.0 V.

The distortion performance as a function of output common-mode voltage is shown in TBD. Note that the VCOMx pins set the common-mode voltage at the outputs of the amplifier, the VOPx/VONx pins, when configured for ac-coupled applications.

For ac-coupled applications with series capacitors at the inputs, as shown in Figure 3, the input common-mode level is set to be the same as the voltage at VCOM or VCOM2.

Due to the wide input common-mode range, this device can easily be dc-coupled to many types of mixers, demodulators, and amplifiers. If the outputs are ac-coupled, no external VCOM/VCOM2 voltage adjustment is required because the amplifier output common-mode level is set to $V_S/2$.

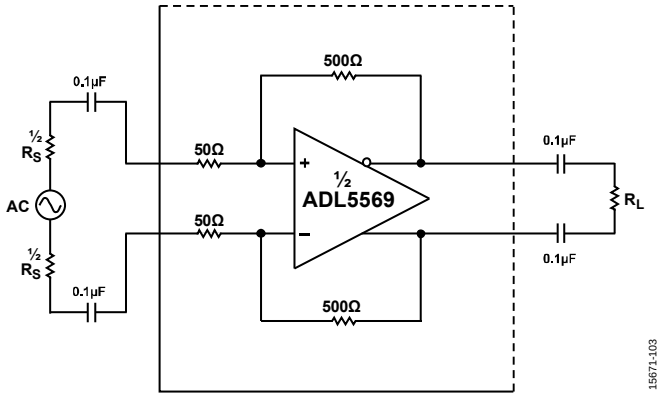

Figure 3. Basic Structure

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 4 shows the basic connections for operating the ADL5569. Apply 5 V to the VCC and VCC2 pins and decouple with 0.1 µF and 10 µF surface-mount ceramic capacitors in parallel to ground.

Decouple the VCOM and VCOM2 pins (Pin 7 and Pin 15) using a 0.1 µF capacitor. The PDB and PDB2 pins (Pin 6 and Pin 16) are tied to logic high, respectively, to enable each amplifier. A differential signal is applied to Amplifier 1 through Pin 1 (VIN) and Pin 2 (VIP) and to Amplifier 2 through Pin 4 (VIP2) and Pin 5 (VIN2). Each amplifier has a gain of 20 dB.

The Amplifier 1 input pins, Pin 1 (VIN) and Pin 2 (VIP), and output pins, Pin 13 (VON) and Pin 12 (VOP), are biased by applying a voltage to Pin 15 (VCOM). If VCOM is left open, VCOM equals ½ of V_S. The Amplifier 2 input pins, Pin 4 (VIP2) and Pin 5 (VIN2), and the output pins, Pin 9 (VON2) and Pin 10 (VOP2), are biased by applying a voltage to Pin 7 (VCOM2). If VCOM2 is left open, VCOM2 equals ½ of V_S.

The ADL5569 can be ac-coupled, as shown in Figure 4, or it can be dc-coupled if within the specified input and output common-mode voltage ranges. Pulling the PDB/PDB2 pins low puts the ADL5569 in sleep mode, reducing the current consumption to 16 mA at ambient temperature.

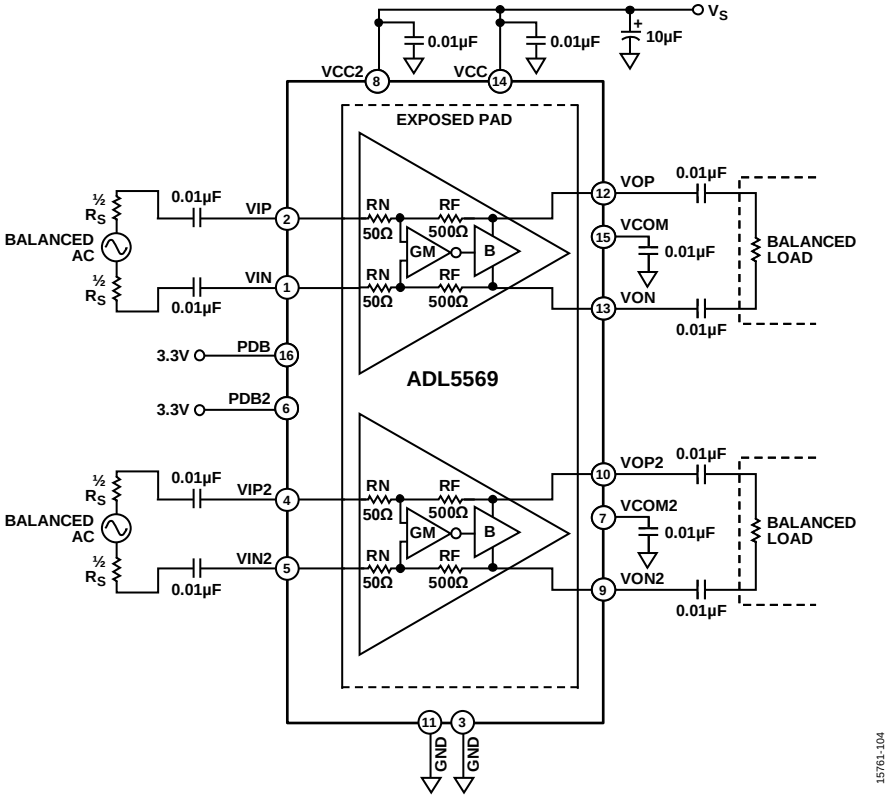

Figure 4. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5569 can be configured as a differential input to differential output driver, as shown in Figure 5. The 50 Ω resistors, R1 and R2, combined with the input balun, provide a 50 Ω input match for the 100 Ω input impedance. The input and output 0.1 µF capacitors isolate the $V_{CCx}/2$ bias from the source and balanced load. The load equals 200 Ω to provide the expected ac performance (see the Specifications section).

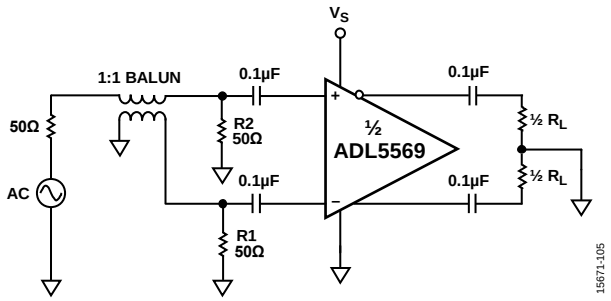

Figure 5. Differential Input to Differential Output Configuration

The differential gain of the ADL5569 is dependent on the source impedance and load, as shown in Figure 6. The differential gain (A_V) can be determined by

$$A_V = \frac{500}{50} \quad (1)$$

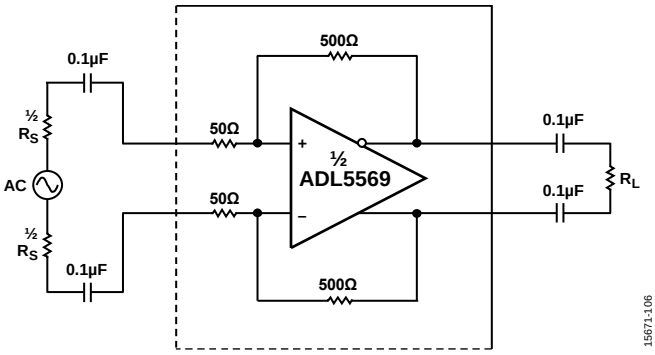

Figure 6. Differential Input Loading Circuit

Single-Ended Input to Differential Output

The ADL5569 can also be configured in a single-ended input to differential output driver, as shown in Figure 7. In this configuration, the gain of the device is reduced due to the application of the signal to only one side of the amplifier. The input and output 0.1 µF capacitors isolate the $V_{CCx}/2$ bias from the source and the balanced load.

The single-ended circuit configuration can be accomplished in three steps (see Figure 7), assuming a 50 Ω R_S source. First, calculate the input impedance (R_{IN}) of the amplifier using the following formula:

$$R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 \times (R_G + R_F)} \right)} \quad (2)$$

Thus, R_{IN} = 91.7 Ω.

The next step is to calculate the termination of Resistor R2 (see Figure 7). Because R_S must be equal to the parallel equivalent resistance of R2 and R_{IN},

$$R_S = \frac{R2 \times R_{IN}}{R2 + R_{IN}}$$

Thus,

$$R2 = R_{IN} \times R_S/(R_{IN} - R_S) \quad (3)$$

When R_S = 50 Ω and R_{IN} = 91.7 Ω, R2 = 109 Ω.

The last step is to calculate the gain path rebalancing resistor, R1 (see Figure 7), using the following formula:

$$R1 = \frac{RS \times R2}{R_S + R2}$$

Thus, R1 = 34.0 Ω.

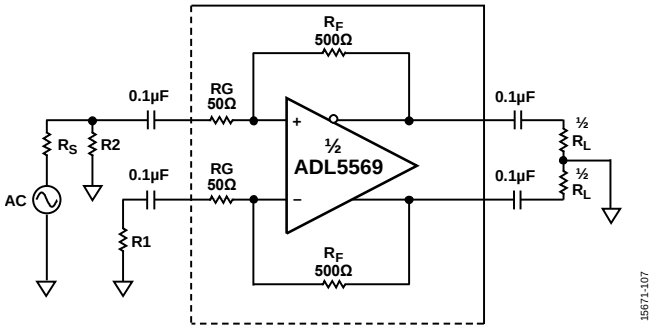

Figure 7. Single-Ended Input to Differential Output Configuration

See the AN-0990 Application Note, *Terminating a Differential Amplifier in Single-Ended Applications*, for more information on terminating single-ended inputs. The single-ended gain configuration of the ADL5569 is dependent on the source impedance and load, as shown in Figure 8.

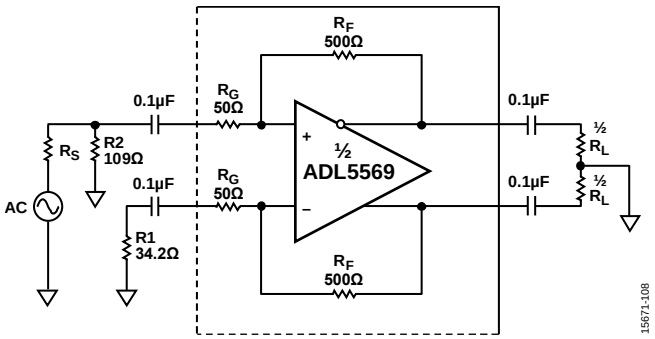

Figure 8. Single-Ended Input Loading Circuit

Determine the single-ended gain (A_{V1}) using the following two equations:

$$R_{MATCH} = \frac{R2 \times R_{IN}}{R2 + R_{IN}} \quad (4)$$

where R_{MATCH} is the input resistance value that matches R_S, calculated as follows:

$$A_{V1} = \frac{500}{50 + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_{MATCH} + R_S}{R_{MATCH}} \times \frac{R_L}{10 + R_L} \quad (5)$$

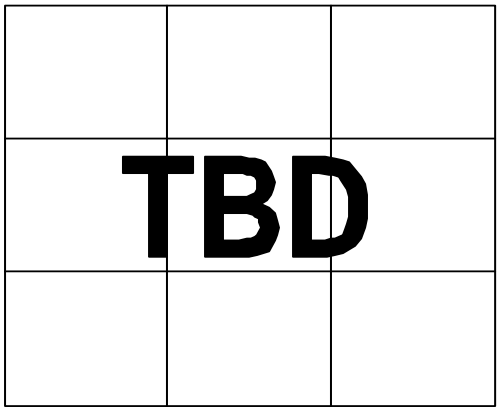

Figure 9. HD2 for Single-Ended (SE) and Differential (DIFF) Configurations vs. Frequency, V_{OUT} = 2 V p-p, R_L = 200 Ω

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5569 can be reduced by adding two resistors in series with the inputs to reduce the gain.

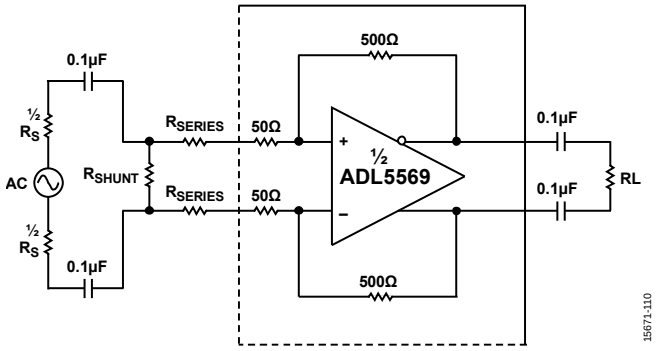

Figure 10. Gain Adjustment Using a Series Resistor

To find R_{SERIES} for a given A_V gain and RL, use the following equation:

$$R_{SERIES} = \frac{500}{A_V} - 50 \quad (6)$$

The necessary shunt component, R_{SHUNT}, to match to the source impedance, R_S, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{2R_{SERIES} + 100}} \quad (7)$$

The shunt resistor values for multiple target voltage gains are listed in Table 5. The source resistance and input impedance need careful attention when using Equation 5. The input impedance of the ADL5569 and the reactance of the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

To calculate the gain (A_V) for a given R_{SERIES} and RL, use the following equation:

$$A_V = \left(\frac{500}{R_{SERIES} + 50}\right) \quad (8)$$

Table 5. Differential Gain Adjustment Using Series Resistor

Target Voltage Gain (dB)	RS (Ω)	R_{SERIES} (Ω)	R_{SHUNT} (Ω)
6	50	188.6	55.8
7	50	162.7	56.6
8	50	139.5	57.5
9	50	118.9	58.6
10	50	100.5	59.9
11	50	84.2	61.4
12	50	69.6	63.2
13	50	56.6	65.3
14	50	45	67.8
15	50	34.6	70.9
16	50	25.4	74.7
17	50	17.2	79.5
18	50	9.9	85.7
19	50	3.4	93.7

EFFECT OF LOAD CAPACITANCE

Load capacitance, including stray capacitance from PCB traces, affect the bandwidth and flatness of the ADL5569 frequency response, resulting in excessive peaking. Adding external series resistors to each output isolates the load capacitance from the outputs, and reduces the peaking effectively. Respective frequency responses resulting from the addition of 1.5 pF and 3 pF differential load capacitance (C_{LD}) as well as series resistance (R_{SE}) of 15 Ω are shown in Figure 11.

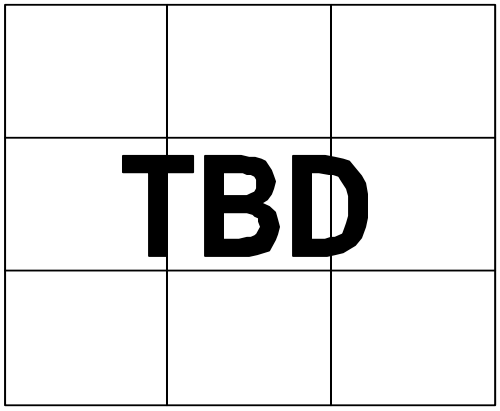

Figure 11. Frequency Response for Various Load Capacitances, V_S = 5 V, High Performance Mode, R_L = 200 Ω

ADC INTERFACING

A wideband data acquisition system (AD-FMCADC10-EBZ) using the ADL5569 together with the AD9208 14-bit ADC is shown in Figure 16. The RC filter after the amplifier works with the pole formed by the ADC input capacitance to attenuate the broadband noise and out of band harmonics generated by the amplifier, as well as blocking the sharp switching pulses, that is, charge injection from the ADC internal sampling circuitry, from reaching the amplifier outputs and creating nonlinear effects. An additional band-pass filter more specific to the system rejection requirements is also needed in front of the ADL5569 amplifier to prevent unwanted signals from compressing the amplifier as well as from reaching the ADC. This filter is usually added during bench testing. See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for additional testing information and setups.

The signal-to-noise ratios with respect to full scale of the ADC system (SNR FS), using various frontend circuit configurations on several circuit boards, are shown in Figure 12. Two-tone intermodulation distortion performance is shown in Figure 13, and the relative frequency responses for this ADC system with different antialiasing filter options, are shown in Figure 14.

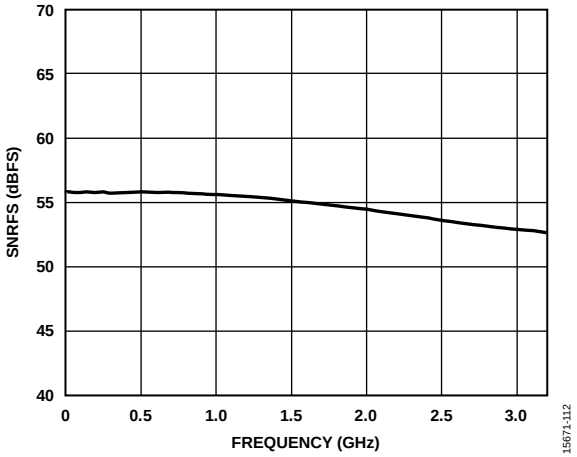

Figure 12. ADC System SNR (Referred to Full Scale)

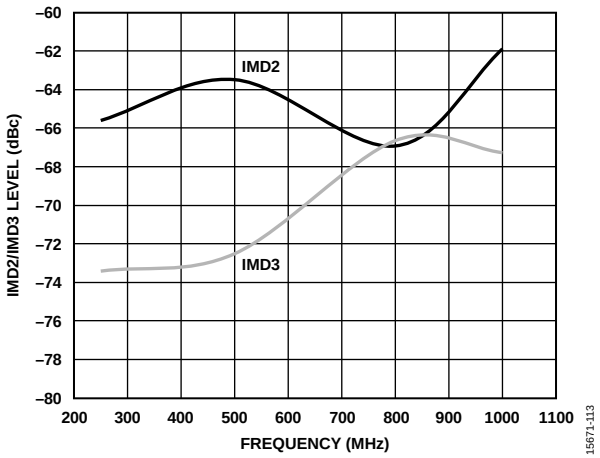

Figure 13. Measured Two-Tone IMD2/IMD3 Performance

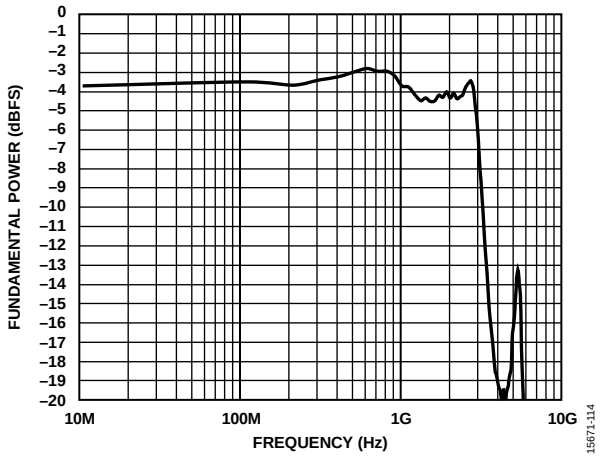

Figure 14. Measured Relative Frequency Response

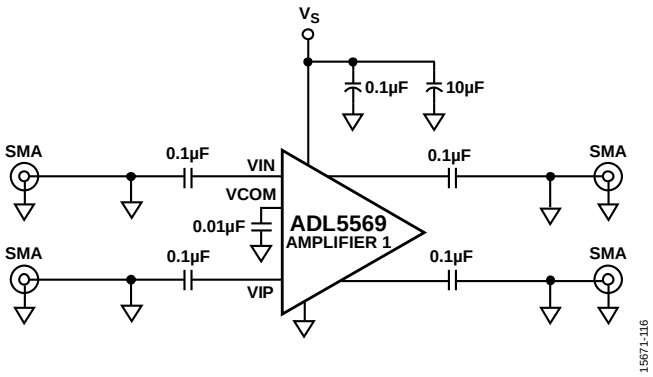

Figure 15. General-Purpose Characterization Circuit

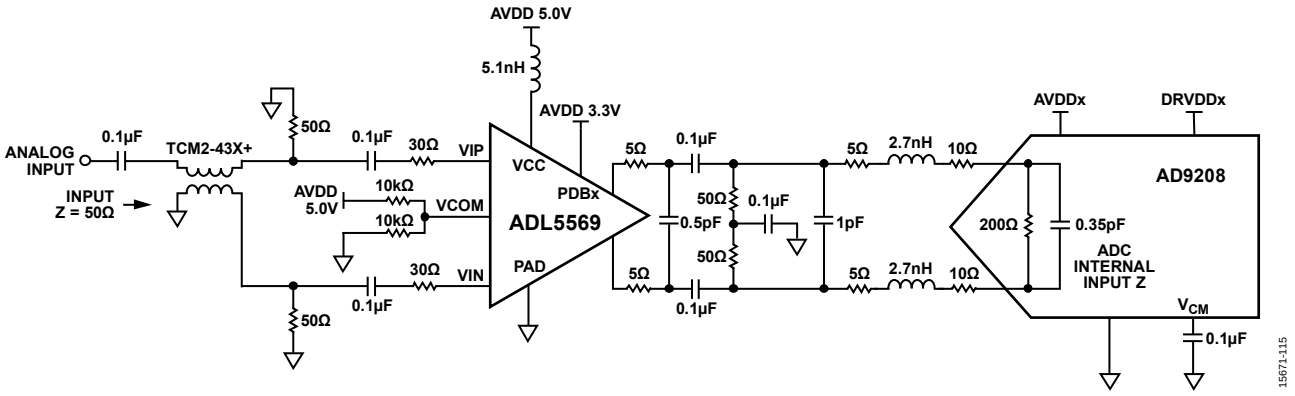

Figure 16. Wideband 3.2 GHz Bandwidth ADC Interfacing Example: ADL5569 Driving the AD9208

SOLDERING INFORMATION AND RECOMMENDED LAND PATTERN

Figure 17 shows the recommended land pattern for the ADL5569. The ADL5569 is contained in a 2.5 mm × 3 mm LFCSP package, which has an exposed ground pad (EP). This pad is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the pad to the low impedance ground plane on the PCB. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

The land pattern on the ADL5569 evaluation board provides a simulated thermal resistance (θ_{JA}) of 90.5 °C/W.

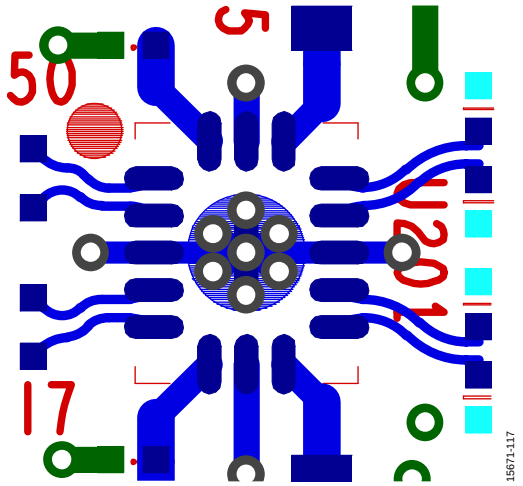

Figure 17. Recommended Land Pattern

EVALUATION BOARD

Figure 18 shows the schematic of the ADL5569 evaluation board. The evaluation board is powered by a single 5 V supply. The power supply is decoupled by 10 µF and 0.1 µF capacitors. On board regulators provide a 2.5 V common mode voltage and 3 V logic supply voltage to enable/disable the power-down feature.

Several termination options are also provided to allow the user to terminate unused inputs/outputs of the amplifier for single-ended applications.

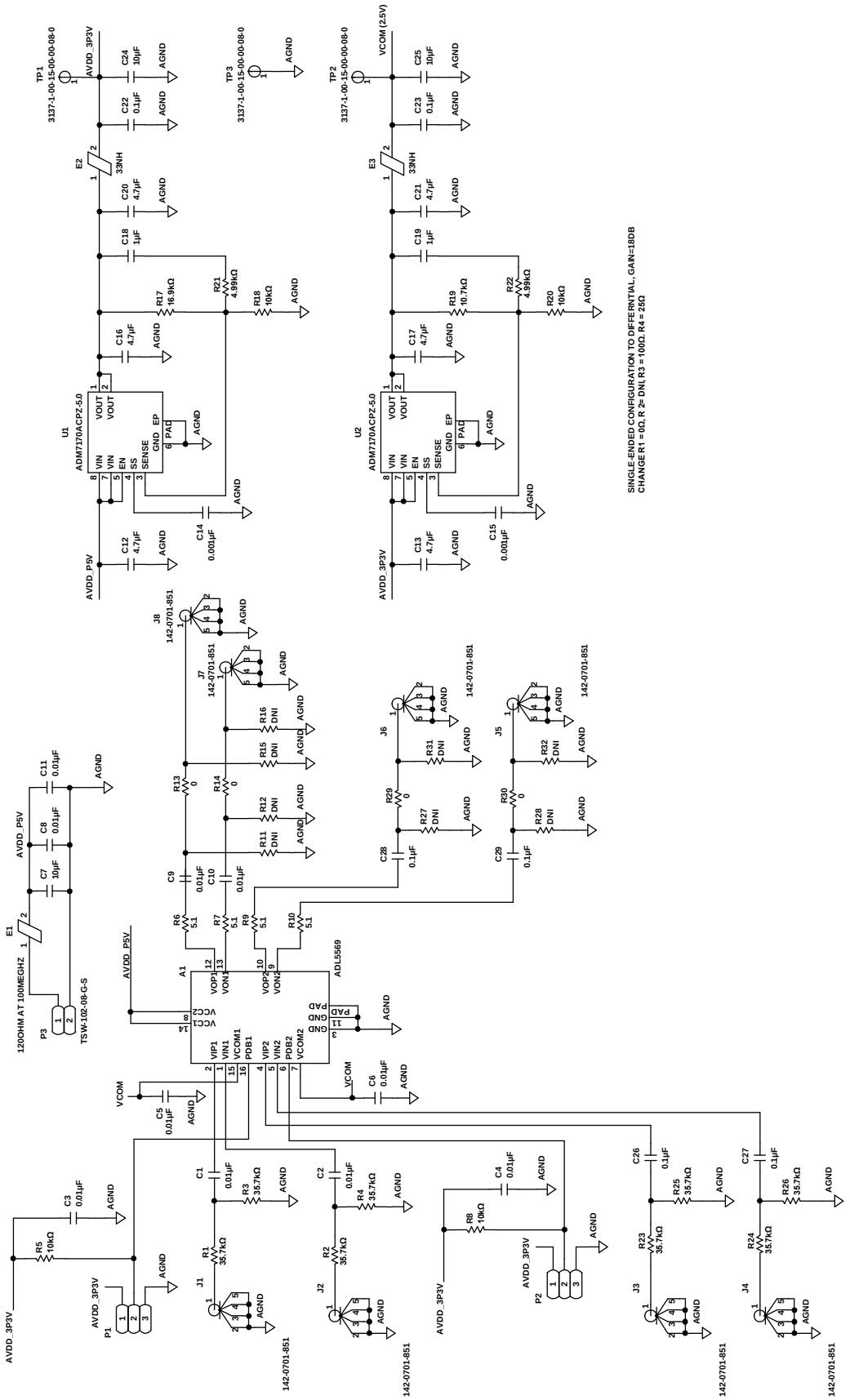

Figure 18. Evaluation Board Schematic

Table 6. Bill of Materials

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	A1	IC, dual channel amplifier	Analog Devices	ADL5569
10	C1, C2, C3, C4, C5, C6, C8, C9, C10, C11	0.01 µF capacitor, ceramic, X7R	Murata	GRM033R71A103KA01D
6	C12, C13, C16, C17, C20, C21	4.7 µF capacitor, ceramic, X5R	Murata	GRM155R60J475ME87D
2	C14, C15	0.001 µF capacitor, ceramic, X7R	Murata	GRM033R71E102KA01D
2	C18, C19	1 µF capacitor, ceramic, X5R	Taiyo Yuden	AMK063ABJ105MP-F
6	C22, C23, C26, C27, C28, C29	Capacitor ceramic, X5R	Murata	GRM033R60J104KE19D
2	C24, C25	10 µF capacitor, ceramic X5R	Taiyo Yuden	AMK105CBJ106MV-F
1	C7	10 µF capacitor ceramic, X5R	Murata	GRM21BR61C106KE15L
1	E1	120 Ω at 100 MHz, ferrite bead, 0.07 Ω, 1.5 A	Murata	BLM18SG121TN1D
2	E2, E3	33 nH, chip inductor, 0.06 Ω, 1.3 A	Coilcraft, Inc.	0402AF-330XJL
8	J1, J2, J3, J4, J5, J6, J7, J8	Connector PCB SMA 50 Ω end launch jack	CINCH	142-0701-851
2	P1, P2	Connector header, straight, three-position	Samtec	TSW-103-08-G-S
1	P3	Connector PCB header, two-position	Samtec	TSW-102-08-G-S
8	R1, R2, R3, R4, R23, R24, R25, R26	35.7 kΩ resistor, precision thick film chip	Panasonic	ERJ-1GEF3572C
4	R13, R14, R29, R30	0 Ω resistor, 0201	Panasonic	ERJ-1GE0R00C
1	R17	16.9 kΩ resistor, 0201	Panasonic	ERJ-1GEF1692C
1	R19	10.7 kΩ resistor, 0402	Vishay Precision Group	CRCW040210K7FKED
2	R21, R22	4.99 kΩ resistor, 0201	Samsung	RC0603F4991CS
4	R5, R8, R18, R20	10 kΩ resistor, 0201	Panasonic	ERJ-1GNF1002C
4	R6, R7, R9, R10	5.1 Ω resistor, 0201	Yageo	RC0201JR-075R1L
3	TP1, TP2, TP3	Connector PCB PC board pin	Mill-Max	3137-1-00-15-00-00-08-0
2	U1, U2	IC ultralow noise, high PSRR, low dropout (LDO) regulator	Analog Devices	ADM7170ACPZ-5.0

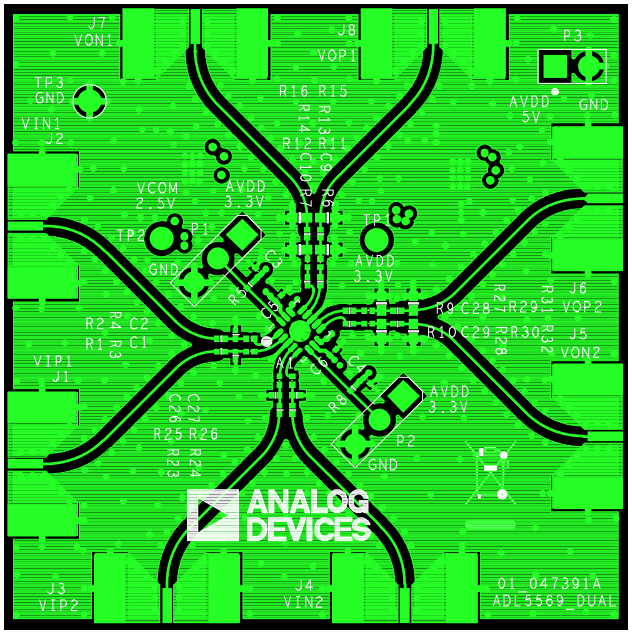

Figure 19. Layout of Evaluation Board, Component Side

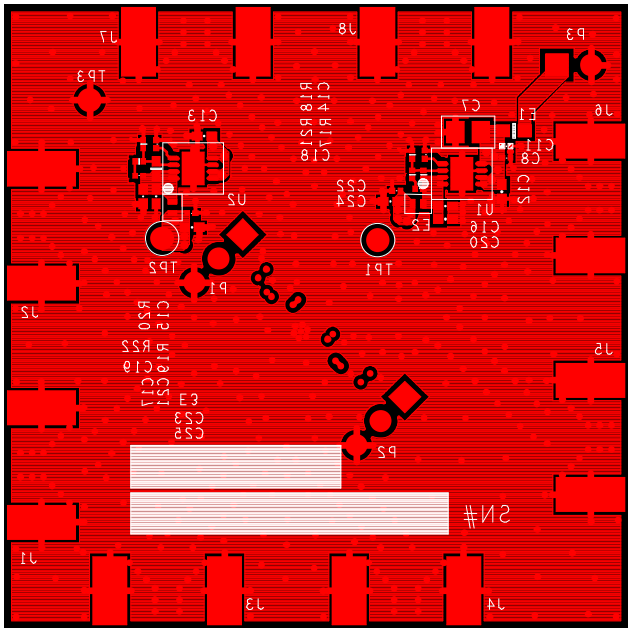

Figure 20. Layout of Evaluation Board, Circuit Side

OUTLINE DIMENSIONS

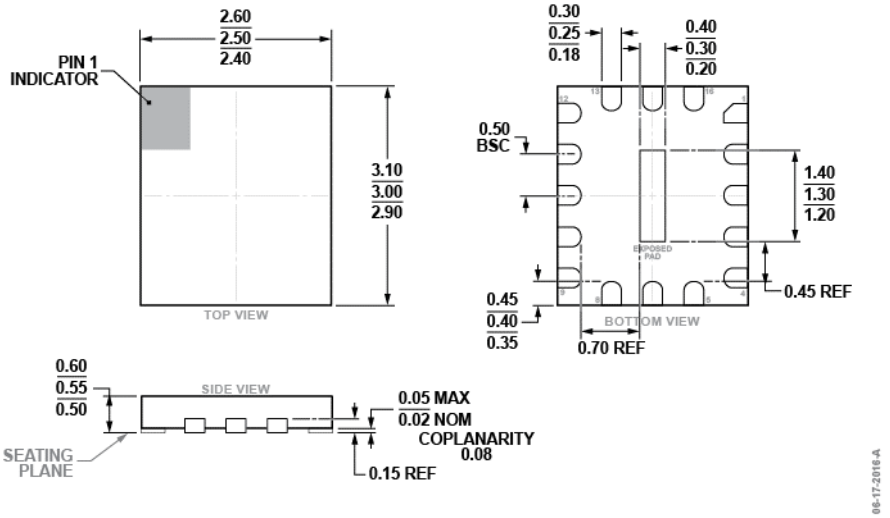

Figure 21. 16-Lead Lead Frame Chip Scale Package [LFCSP]
2.5 mm × 3 mm Body and 0.55 mm Package Height
(CP-16-44)
Dimensions shown in millimeters

PR15671-0-8/17(PrB)