

## FEATURES

- 7.5 GHz operating frequency
- 160 ps propagation delay
- 100 ps output rise/fall
- 110 fs random jitter
- On-chip input terminations
- Extended industrial temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 3.3 V power supply ( $V_{CC} - V_{EE}$ )

## APPLICATIONS

- Clock and data signal restoration
- High speed converter clocking
- Broadband communications
- Cellular infrastructure
- High speed line receivers
- ATE and high performance instrumentation
- Level shifting
- Threshold detection

## GENERAL DESCRIPTION

The ADCLK914 is an ultrafast clock/data buffer fabricated on the Analog Devices, Inc., proprietary, complementary bipolar (XFCB-3) silicon-germanium (SiGe) process. The ADCLK914 features high voltage differential signaling (HVDS) outputs suitable for driving the latest Analog Devices high speed digital-to-analog converters (DACs). The ADCLK914 has a single, differential open-collector output.

The ADCLK914 buffer operates up to 7.5 GHz with a 160 ps propagation delay and adds only 110 fs random jitter (RJ).

## FUNCTIONAL BLOCK DIAGRAM

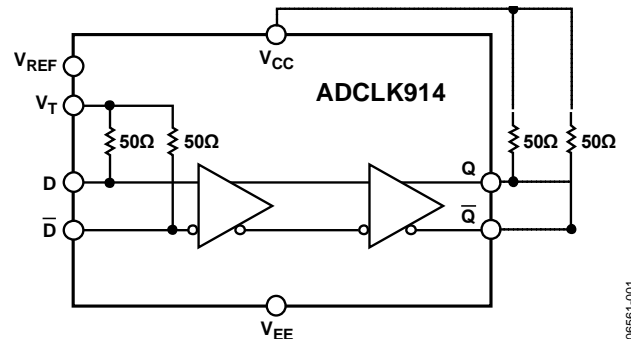


Figure 1.

06561-001

The input has a center tapped, 100  $\Omega$ , on-chip termination resistor and accepts LVPECL, CML, CMOS, LVTTTL, or LVDS (ac-coupled only). A  $V_{REF}$  pin is available for biasing ac-coupled inputs.

The HVDS output stage is designed to directly drive 1.9 V each side into 50  $\Omega$  terminated to  $V_{CC}$  for a total differential output swing of 3.8 V.

The ADCLK914 is available in a 16-lead LFCSP. It is specified for operation over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

# ADCLK914\* PRODUCT PAGE QUICK LINKS

Last Content Update: 09/08/2017

---

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADCLK914 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-501: Aperture Uncertainty and ADC System Performance
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

### Data Sheet

- ADCLK914: Ultrafast, SiGe, Open-Collector HVDS Clock/Data Buffer Data Sheet

### User Guides

- UG-058: Setting Up the Evaluation Board for the ADCLK914

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9739A Native FMC Card / Xilinx Reference Designs

## TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- ADCLK914 IBIS Model

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Solutions Bulletins & Brochures

- Digital-to-Analog Converter ICs Solutions Bulletin, Volume 10, Issue 1

### Technical Articles

- Design A Clock-Distribution Strategy With Confidence
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

### Tutorials

- MT-008: Converting Oscillator Phase Noise to Time Jitter

## DESIGN RESOURCES

- ADCLK914 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADCLK914 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

---

## TABLE OF CONTENTS

Features .....	1	Typical Performance Characteristics .....	7
Applications .....	1	Applications Information .....	9
Functional Block Diagram .....	1	Power/Ground Layout and Bypassing .....	9
General Description .....	1	HVDS Output Stage .....	9
Table of Contents .....	2	Interfacing to High Speed DACs .....	9
Revision History .....	2	Optimizing High Speed Performance .....	9
Specifications .....	3	Random Jitter .....	9
Electrical Characteristics .....	3	Typical Application Circuits .....	10
Absolute Maximum Ratings .....	5	Outline Dimensions .....	11
Thermal Performance .....	5	Ordering Guide .....	11
ESD Caution .....	5		
Pin Configuration and Function Descriptions .....	6		

## REVISION HISTORY

### 9/2017—Rev. A to Rev. B

Updated Outline Dimensions .....	11
Changes to Ordering Guide .....	11

### 10/2008—Rev. 0 to Rev. A

Changes to Input Low Voltage Parameter, Table 1 .....	3
Changes to Output High Voltage Parameter, Table 1 .....	3
Changes to Output Low Voltage Parameter, Table 1 .....	3
Output Differential Range Parameter, Table 1 .....	3
Changes to Absolute Maximum Ratings Section .....	5

### 7/2008—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . All outputs terminated through  $50\ \Omega$  to  $V_{CC}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS						
Input High Voltage	$V_{IH}$	$V_{EE} + 1.65$		$V_{CC}$	V	
Input Low Voltage	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V	
Input Differential Range	$V_{ID}$	0.2		3.4	V p-p	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ( $\pm 1.7\text{ V}$ between input pins)
		0.2		2.8	V p-p	$T_A = 85^\circ\text{C}$ to $125^\circ\text{C}$ ( $\pm 1.4\text{ V}$ between input pins)
Input Capacitance	$C_{IN}$		0.4		pF	
Input Resistance			50		$\Omega$	
Differential Mode			100		$\Omega$	
Common Mode			50		k $\Omega$	Open termination
Input Bias Current			20		$\mu\text{A}$	
DC OUTPUT CHARACTERISTICS						
Output High Voltage	$V_{OH}$	$V_{CC} - 0.55$	$V_{CC} - 0.40$	$V_{CC} - 0.25$	V	
Output Low Voltage	$V_{OL}$	$V_{CC} - 2.75$	$V_{CC} - 2.35$	$V_{CC} - 1.9$	V	
Output Differential Range	$V_{OD}$	1.54	1.95	2.22	V	
Reference Voltage	$V_{REF}$				V	
Output Voltage			$(V_{CC} + 1)/2$		V	$-500\ \mu\text{A}$ to $+500\ \mu\text{A}$
Output Resistance			250		$\Omega$	
AC PERFORMANCE						
Operating Frequency			7.5		GHz	$> 1.1\text{ V}$ differential output swing, $V_{CC} = 3.3\text{ V} \pm 10\%$
Propagation Delay	$t_{PD}$	127	158	202	ps	$V_{CC} = 3.3\text{ V} \pm 10\%$ , $V_{ICM} = V_{REF}$ , $V_{ID} = 1.6\text{ V p-p}$
Propagation Delay Temperature Coefficient			140		fs/ $^\circ\text{C}$	
Propagation Delay Skew (Device to Device)				65	ps	$V_{ID} = 1.6\text{ V p-p}$
Output Rise Time	$t_R$		100	125	ps	20%/80%
Output Fall Time	$t_F$		80	95	ps	80%/20%
Wideband Random Jitter <sup>1</sup>	RJ		110		fs rms	$V_{ID} = 1.6\text{ V p-p}$ , $6\text{ V/ns}$ , $V_{ICM} = 1.85\text{ V}$
Additive Phase Noise						
622.08 MHz			-132		dBc/Hz	@10 Hz offset
			-143		dBc/Hz	@100 Hz offset
			-151		dBc/Hz	@1 kHz offset
			-156		dBc/Hz	@10 kHz offset
			-157		dBc/Hz	@100 kHz offset
			-156		dBc/Hz	>1 MHz offset
245.76 MHz			-133		dBc/Hz	@10 Hz offset
			-143		dBc/Hz	@100 Hz offset
			-153		dBc/Hz	@1 kHz offset
			-158		dBc/Hz	@10 kHz offset
			-159		dBc/Hz	@100 kHz offset
			-158		dBc/Hz	>1 MHz offset

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
122.88 MHz			-150		dBc/Hz	@10 Hz offset
			-156		dBc/Hz	@100 Hz offset
			-160		dBc/Hz	@1 kHz offset
			-161		dBc/Hz	@10 kHz offset
			-161		dBc/Hz	@100 kHz offset
			-160		dBc/Hz	>1 MHz offset
<b>POWER SUPPLY</b>						
Supply Voltage Requirement	$V_{CC}$	2.97		3.63	V	
Power Supply Current						
Negative Supply Current	$I_{VEE}$	66	111	150	mA	Includes output current
Positive Supply Current	$I_{VCC}$	34	55	73	mA	
Power Supply Rejection <sup>2</sup>	$PSR_{VCC}$		13		ps/V	$V_{CC} = 3.3\text{ V} \pm 10\%$
Output Swing Supply Rejection <sup>3</sup>			-15		dB	$V_{CC} = 3.3\text{ V} \pm 10\%$

<sup>1</sup> Calculated from SNR of ADC method. See Figure 8 for rms jitter vs. input slew rate.

<sup>2</sup> Change in  $t_{PD}$  per change in  $V_{CC}$ .

<sup>3</sup> Change in output swing per change in  $V_{CC}$ .

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage ( $V_{CC}$ to GND)	6.0 V
Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
Maximum Output Voltage	$V_{CC} + 0.5$ V
Minimum Output Voltage	$V_{EE} - 0.5$ V
Input Termination	$\pm 2$ V
Voltage Reference	$V_{CC} - V_{EE}$
Operating Temperature Range, Ambient	-40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL PERFORMANCE

The ADCLK914 is specified for a case temperature ( $T_{CASE}$ ). To ensure that  $T_{CASE}$  is not exceeded, use an airflow source.

To determine the junction temperature on the application PCB

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:

$T_J$  is the junction temperature (°C).

$T_{CASE}$  is the case temperature (°C) measured by the customer at top center of package.

$\Psi_{JT}$  is determined by the values listed in Table 3.

PD is the power dissipation.

Values of  $\theta_{JA}$  are provided for package comparison and PCB design considerations.  $\theta_{JA}$  can be used for a first-order approximation of  $T_J$  by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where  $T_A$  is the ambient temperature (°C).

Values of  $\theta_{JB}$  are provided for package comparison and PCB design considerations.

Table 3. Thermal Parameters for ADCLK914 16-Lead LFCSP

Symbol	Description <sup>1</sup>	Value	Units
$\theta_{JA}$	Junction-to-ambient thermal resistance, 0.0 meters per sec air flow per JEDEC JESD51-2 (still air)	78.4	°C/W
$\theta_{JMA}$	Junction-to-ambient thermal resistance, 1.0 meter per sec air flow per JEDEC JESD51-6 (moving air)	68.5	°C/W
$\theta_{JMA}$	Junction-to-ambient thermal resistance, 2.5 m/s air flow per JEDEC JESD51-6 (moving air)	61.4	°C/W
$\theta_{JB}$	Junction-to-board thermal resistance, 1.0 meter per sec air flow per JEDEC JESD51-8 (moving air)	48.8	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance (die-to-heatsink) per MIL-Std 883, Method 1012.1	1.5	°C/W
$\Psi_{JT}$	Junction-to-top-of-package characterization parameter, 0 meters per sec air flow per JEDEC JESD51-2 (still air)	2.0	°C/W

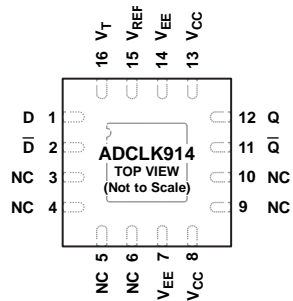
<sup>1</sup> Descriptions based on using a 2s2p test board.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NC = NO CONNECT. NO PHYSICAL CONNECTION TO THE DIE.
2. EXPOSED PAD. NO CONNECT. THE METALLIC BACK SURFACE OF THE PACKAGE IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO GROUND ON THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS NEEDED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS BACK SURFACE. ALLOW SUFFICIENT CLEARANCE FOR VIAS AND OTHER COMPONENTS.

08581-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Noninverting Input.
2	$\overline{D}$	Inverting Input.
3, 4, 5, 6, 9, 10	NC	No Connect. No physical connection to the die.
7, 14	$V_{EE}$	Negative Supply Voltage.
8, 13	$V_{CC}$	Positive Supply Voltage.
11	$\overline{Q}$	Inverting Output.
12	Q	Noninverting Output.
15	$V_{REF}$	Reference Voltage. Reference voltage for biasing ac-coupled inputs.
16	$V_T$	Center Tap. Center tap of 100 $\Omega$ input resistor.
Heat Sink/ Exposed Pad	NC	No Connect. The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to ground on the application board if improved thermal and/or mechanical stability is needed. Exposed metal at the corners of the package is connected to this back surface. Allow sufficient clearance for vias and other components.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . All outputs terminated through  $50\ \Omega$  to  $V_{CC}$ , unless otherwise noted.

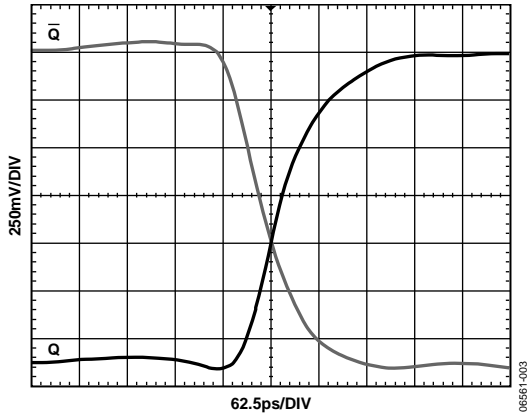


Figure 3. Output Waveform at 1 GHz,  $V_{CC} = 3.3\text{ V}$

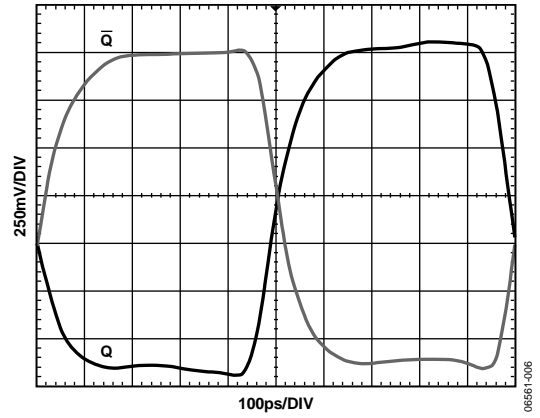


Figure 6. Output Waveform at 1 GHz,  $V_{CC} = 3.3\text{ V}$

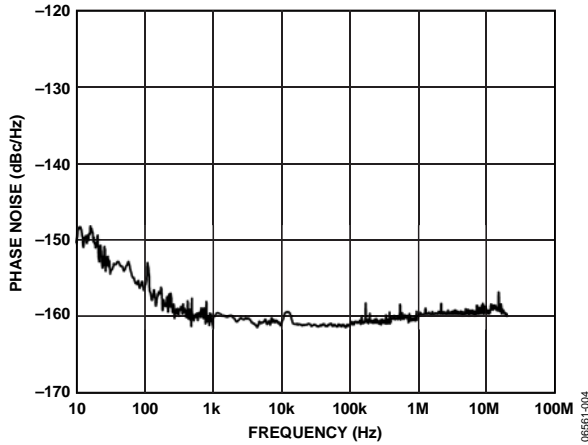


Figure 4. Phase Noise at 122.88 MHz

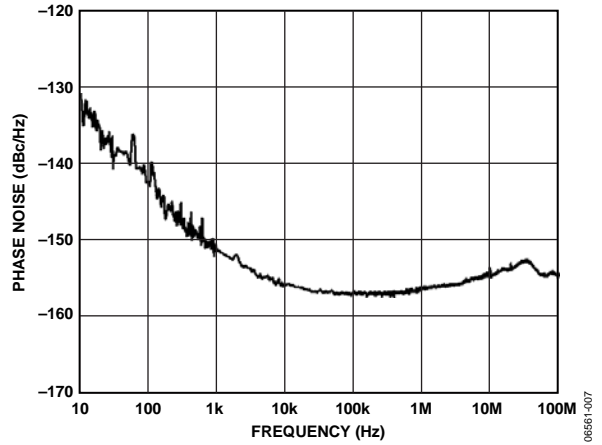


Figure 7. Phase Noise at 622.08 MHz

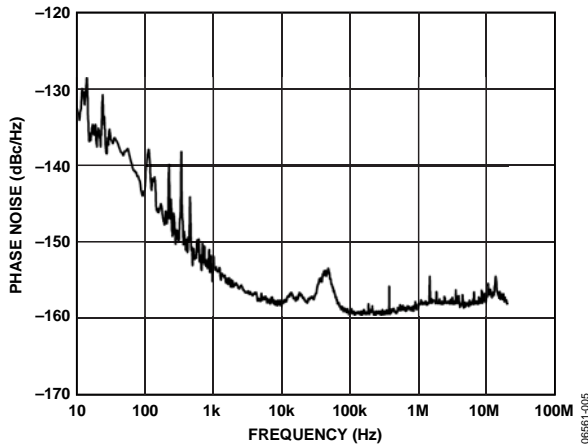


Figure 5. Phase Noise at 245.76 MHz

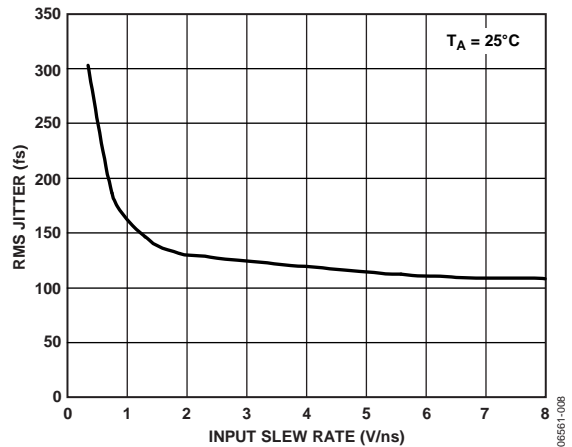


Figure 8. RMS Jitter vs. Input Slew Rate



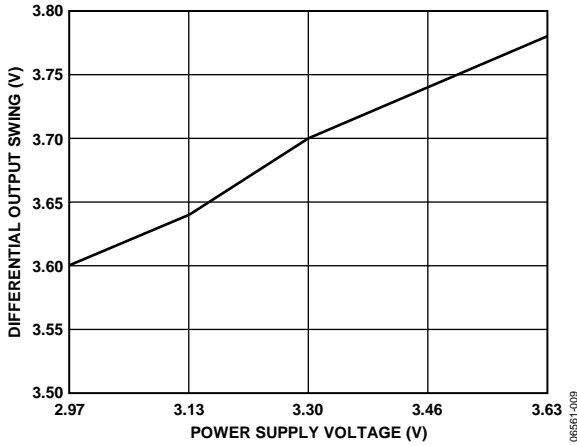


Figure 9. Differential Output Swing vs. Power Supply Voltage

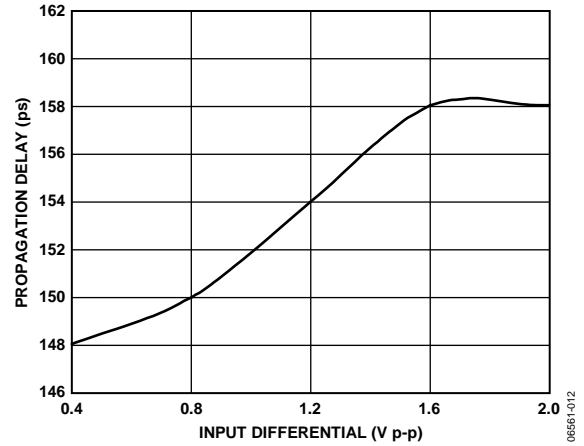


Figure 12. Propagation Delay vs.  $V_{ID}$ ;  $V_{ICM} = 2.15 V$

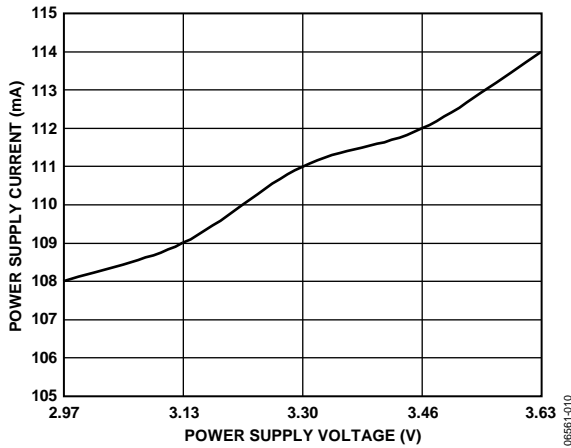


Figure 10. Power Supply Current vs. Power Supply Voltage

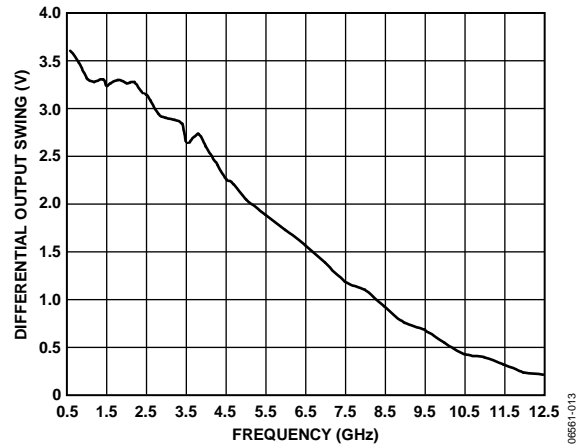


Figure 13. Toggle Rate, Differential Output Swing vs. Frequency

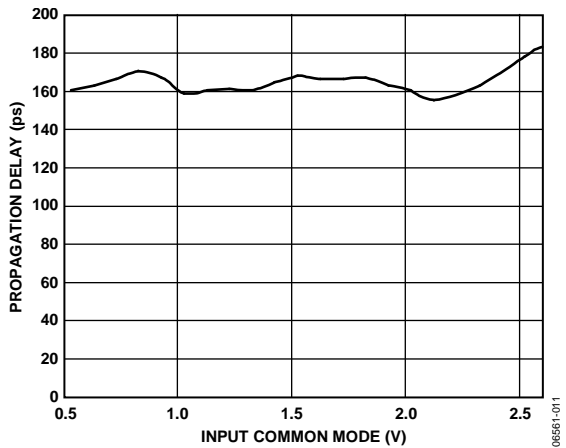


Figure 11. Propagation Delay vs.  $V_{ICM}$ ;  $V_{ID} = 1.6 V p-p$

## APPLICATIONS INFORMATION

### POWER/GROUND LAYOUT AND BYPASSING

The ADCLK914 buffer is designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes for both the negative supply ( $V_{EE}$ ) and the positive supply ( $V_{CC}$ ) planes as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Place a 1  $\mu\text{F}$  electrolytic bypass capacitor within several inches of each power supply pin to ground. In addition, place multiple high quality 0.001  $\mu\text{F}$  bypass capacitors as close as possible to each  $V_{EE}$  and  $V_{CC}$  supply pin and connect these capacitors to the GND plane with redundant vias. Carefully select high frequency bypass capacitors for minimum inductance and ESR. To maximize the effectiveness of the bypass capacitors at high frequencies, strictly avoid parasitic layout inductance.

Slew currents may also appear at the  $V_{DD}$  and  $V_{SS}$  pins of the device being driven by the ADCLK914.

### HVDS OUTPUT STAGE

The ADCLK914 has been developed to provide a bipolar interface to any CMOS device that requires extremely low jitter, high amplitude clocks. It is intended to be placed as close as possible to the receiving device and allows the rest of the clock distribution to run at standard CML or PECL levels.

Interconnects must be short and very carefully designed because the single terminated design provides much less margin for error than lower voltage, double terminated transmission techniques.

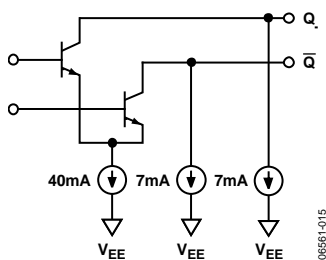


Figure 14. Simplified Schematic Diagram of the ADCLK914 HVDS Output Stage

### INTERFACING TO HIGH SPEED DACs

The ADCLK914 is designed to drive high amplitude, low jitter clock signals into high speed, multi-GSPS DACs. The ADCLK914 should be placed as close as possible to the clock input of the DAC so that the high slew rate and high amplitude clock signal that these devices require do not cause routing difficulties, generate EMI, or become degraded by dielectric and other

losses. The ADCLK914, in turn, may be driven directly by standard or low swing PECL, CML, CMOS, or LVTTTL sources, or by LVDS with simple ac coupling, as illustrated in Figure 15 through Figure 19.

### OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed circuit, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power, and ground impedances, as well as other layout issues, can severely limit performance and can cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified jitter performance by reducing the effective input slew rate.

Input and output matching have a significant impact on performance. The ADCLK914 buffer provides internal 50  $\Omega$  termination resistors for both D and  $\bar{D}$  inputs. The return side can be connected to the reference pin provided or to a current sink at  $V_{CC} - 2\text{V}$  for use with differential PECL, or to  $V_{CC}$  for direct coupled CML. The  $V_{REF}$  pin should be left floating any time that it is not used to minimize power consumption.

Note that the ADCLK914  $V_{REF}$  source is current-limited to resist damage from momentary shorts to  $V_{EE}$  or  $V_{CC}$  and from capacitor charging currents; for this reason, the  $V_{REF}$  source cannot be used as a PECL termination supply.

Carefully bypass the termination potential using ceramic capacitors to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If the inputs are directly coupled to a source, care must be taken to ensure that the pins remain within the rated input differential and common-mode ranges.

If the return is floated, the device exhibits 100  $\Omega$  cross-termination, but the source must then control the common-mode voltage and supply the input bias currents.

ESD/clamp diodes between the input pins prevent the application of excessive offsets to the input transistors. ESD diodes are not optimized for best ac performance. If a clamp is needed, it is recommended that appropriate external diodes be used.

### RANDOM JITTER

The ADCLK914 buffer has been specifically designed to minimize random jitter over a wide input range. Provided that sufficient voltage swing is present, random jitter is affected most by the slew rate of the input signal. Whenever possible, clamp excessively large input signals with fast Schottky diodes because attenuators reduce the slew rate. Input signal runs of more than a few centimeters should be over low loss dielectrics or cables with good high frequency characteristics.

TYPICAL APPLICATION CIRCUITS

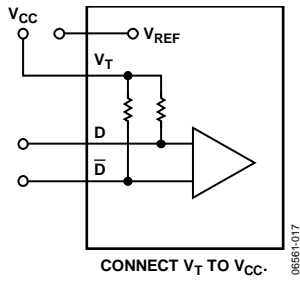


Figure 15. Interfacing to CML Inputs

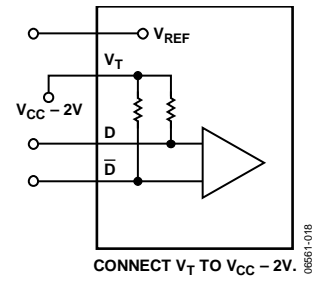
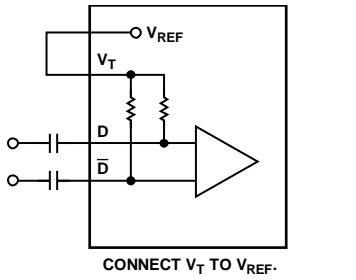


Figure 18. Interfacing to ECL Inputs



NOTES  
1. PLACING A BYPASS CAPACITOR FROM  $V_T$  TO GROUND CAN IMPROVE THE NOISE PERFORMANCE.

Figure 16. AC Coupling Differential Signals

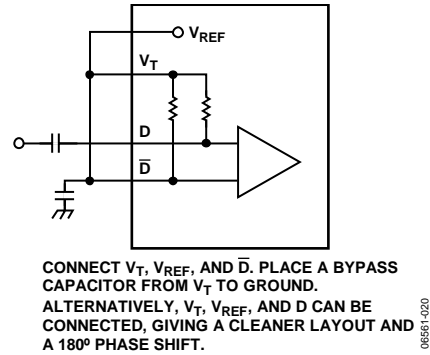


Figure 19. Interfacing to AC-Coupled, Single-Ended Inputs

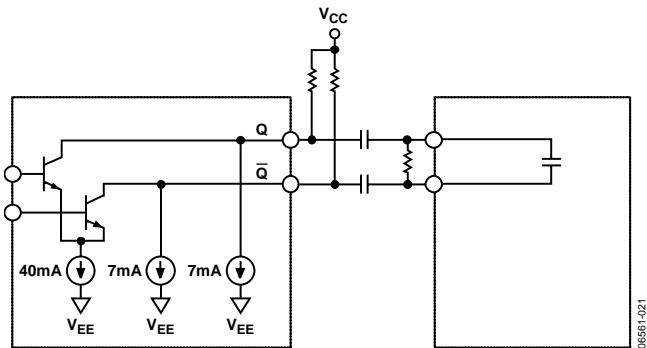
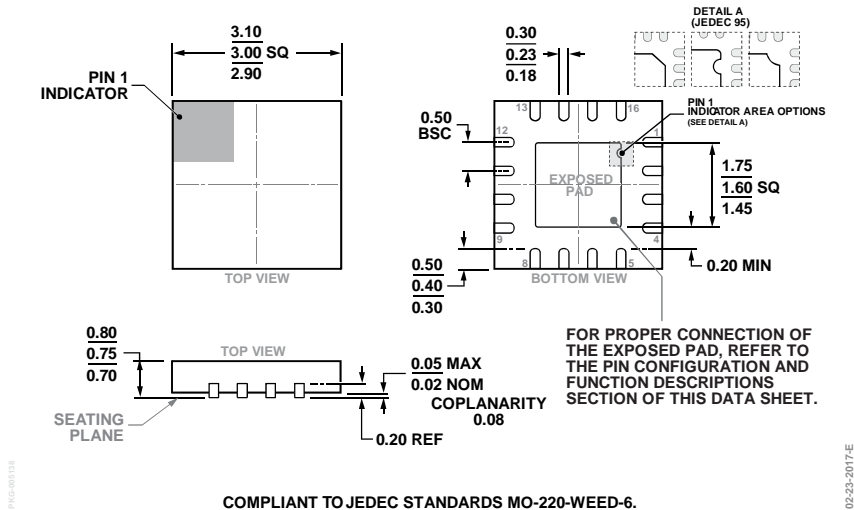


Figure 17. Interfacing to High Speed DAC

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 20. 16-Lead Lead Frame Chip Scale Package [LFCSP]  
3 mm × 3 mm Body and 0.75 mm Package Height  
(CP-16-22)

Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADCLK914BCPZ-WP	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914BCPZ-R7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914BCPZ-R2	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADCLK914/PCBZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.