9 KHz - 7 GHz Directional Bridge and Dual RMS Detector

Preliminary Technical Data

ADL5920

FEATURES

Frequency Range: 9 KHz to 7 GHz
Insertion Loss: 0.9 dB @1GHz
1.9 dB @6 GHz
Input and Output Return Loss/VSWR:
<1 GHz: >15 dB (<1:1.4)
1 to 3 GHz: 15 dB (1:1.4)
3 to 6 GHz: 13 dB (1:1.6)
OIP3: +70.5 dBm
Directivity:
23 dB @ 1 GHz
14 dB @ 3 GHz
6 dB @ 6 GHz
Max Input Power: +30 dBm
Forward Power Measurement range: 50 dB at 1 GHz
Linear-in-dB Outputs for RMS and Return Loss Measurement

Applications
Broadband In-Line Power and Return Loss Measurement in Wireless Transmitters, Signal Generators, Network Analyzers and Wireless Communications Testers

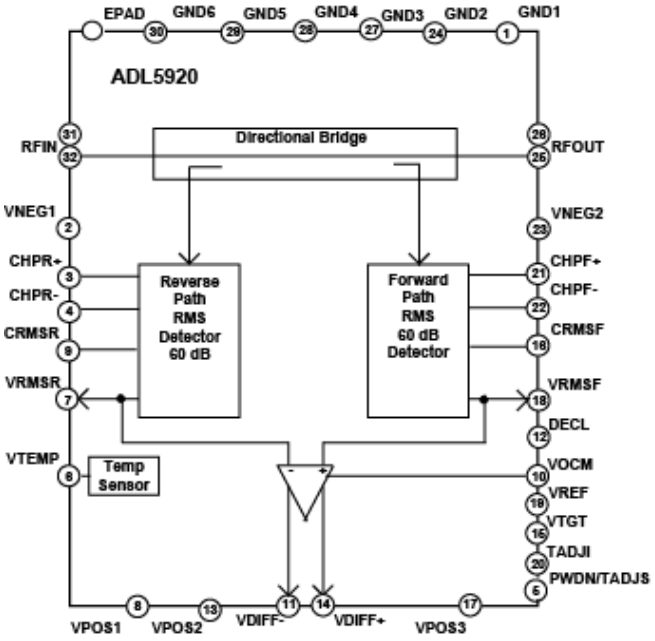

Figure 1. ADL5920 Block Diagram

GENERAL DESCRIPTION

The ADL5920 is an ultra-wide band bi-directional bridge detector that can simultaneously measure forward and reverse RMS power levels in a signal path along with return loss.

The forward and reverse power in the bridge is measured using two high range RMS detectors. The ratio of the forward and reverse power levels is also measured and provided as a differential output voltage with an adjustable common mode level.

The bridge and detector circuitry is internally DC coupled to allow for frequency measurements down to 9 KHz. By applying an optional -2.5V negative supply, ground referenced dc-coupled signals can be applied.

The maximum input signal on each of the RF ports (RFIP and RFOP) is +30 dBm with handling capability for open and shorted loads.

The ADL5920 requires a 5V supply and draws 150 mA. It can be powered down via a PWDN pin.

The ADL5920 is supplied in a 32-lead, 5 mm x 5 mm LFCSP, for the operating temperature range of -40°C to +85°C.

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ADL5920* PRODUCT PAGE QUICK LINKS

Last Content Update: 08/15/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADL5920 Evaluation Board

DOCUMENTATION

Data Sheet

- ADL5920: 9 KHz - 7 GHz Directional Bridge and Dual RMS Detector Preliminary Data Sheet

DESIGN RESOURCES

- ADL5920 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADL5920 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

SPECIFICATIONS

VPOS1, VPOS2, VPOS3 = 5 V, T_A = 25°C, Z_O = 50 Ω.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.009		6000	MHz
Input & Output Impedance	RFIN, RFOUT terminated with 50 Ω		50		Ω
GENERAL PARAMETERS					
Insertion Loss	frequency 9 KHz to 1 GHz		1		dB
	frequency 1 GHz to 3 GHz		1.5		dB
	frequency 3 GHz to 6 GHz		1.9		dB
Directivity	frequency 9 KHz to 1 GHz		>23		dB
	frequency 1 GHz to 3 GHz		14		dB
	frequency 3 GHz to 6 GHz		6		dB
VSWR (RFIN, RFOUT)	frequency 9 KHz to 1 GHz		<1.4:1		
	frequency 1 GHz to 3 GHz		1.4:1		
	frequency 3 GHz to 6 GHz		1.6:1		
Return Loss (RFIN, RFOUT)	frequency 9 KHz to 1 GHz		>15		dB
	frequency 1 GHz to 3 GHz		15		dB
	frequency 3 GHz to 6 GHz		13		dB
Max Input Power			30		dBm
±1 dB Input Range	1 GHz		50		dB
OIP3	900 MHz, +27 dBm per tone 1 MHz tone spacing		70.5		dBm
ENABLE INTERFACE	Pin PWDN				
Voltage Level to Enable	PWDN decreasing			1.3	V
Voltage Level to Disable	PWDN Increasing	1.4			V
Enable Time			2		µs
Disable Time			2		ns
POWER SUPPLY					
Supply Voltage			5		V
Quiescent Current	PWDN low		150		mA
Power Dissipation	PWDN high		1		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Average RF Power	30 dBm
Equivalent Voltage, Sine Wave Input	20 V p-p
Internal Power Dissipation	TBD mW
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	TBD°C
Thermal Impedance	TBD

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

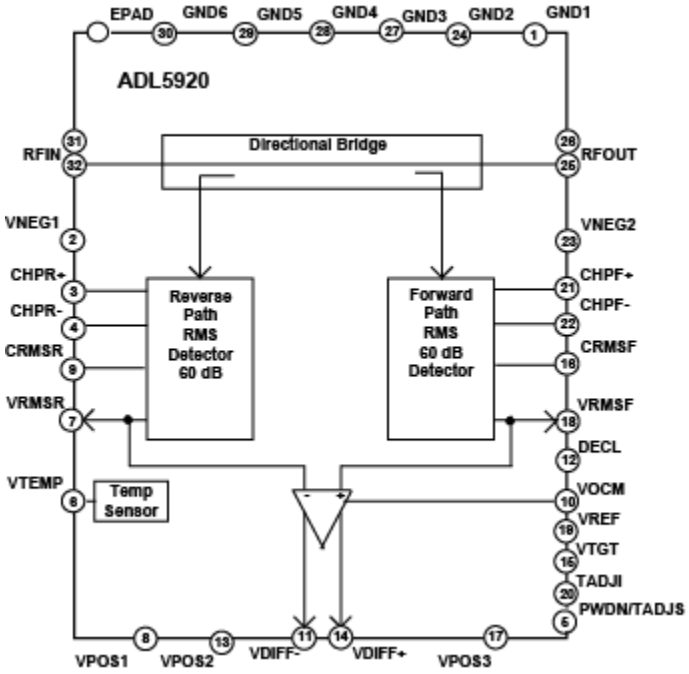

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1,24,27, 28,29,30	GND1, GND2,GND3 GND4, GND5, GND6	RF Ground: Connect all ground pins to a low-impedance ground plane
2,23	VNEG1, VNEG2	Negative supply pins. For normal single-supply operation, these pins should be connected to ground. In applications where the RF input and output are dc-coupled, a -2.5 V supply voltage should be applied to these pins along with a 5 V power supply on VPOS1, VPOS2 and VPOS3.
8, 13, 17	VPOS1, VPOS2, VPOS3	Power Supply: Each power supply pin should be separately decoupled using 100 pF and 0.1µF capacitors. The nominal supply voltage on these pins is 5V.
3,4, 21,22	CHPR+, CHPR- CHPF+, CHPF-	Offset Compensation Loop Control: The capacitances on these pin pairs set the high-pass corner frequency of internal offset compensation loops, which in turn sets the minimum operating frequency of the RMS detectors in the forward and reverse paths. A single capacitor should be connected across each pair of pins. These capacitors should be located as close to the pins as possible (0201 size components should be used to allow the capacitors to straddle the two pins). With no capacitance present, the internal offset compensation loops will have a high-pass corner of approximately 450 KHz. This would limit the minimum input frequency to approximately ten times this value. The default value for these capacitors is 0.1 uF. This sets up a high pass corner frequency of 1 KHz which enables operation down to 9 KHz, assuming at the RF input pins are either dc coupled or have large ac-coupling capacitor values.
5	TADJS/PWDN	Temperature Compensation/Shutdown. This is a dual function pin used for controlling temperature slope compensation at voltages <1.0 V and/or for shutting down the device at voltages >1.4 V. The temperature compensation voltage is generally set by connecting this pin to VREF through a resistor divider.
6	VTEMP	Temperature Sensor Output of 1.4 V at 25°C with a Coefficient of 5 mV/°C.
7,18	VRMSR, VRMSF	Reverse and Forward RMS Voltage Measurement: The voltages on these pins are proportional to the dB power of the incident signal to the RFOUT and RFIN pins
9,16	CRMSR, CRMSF	RMS Averaging Capacitor for Reverse and Forward Path Detectors. Connect RMS averaging capacitors between CRMSR and ground and between CRMSF and ground to set the averaging time constant of the forward and reverse rms detectors. For normal operation, the values of these two capacitors should be equal. The value depends on the lowest frequency of interest, i.e. as low as 9 kHz.

10	VOCM	Common Mode Input Voltage for VDIFF+ and VDIFF-: The input voltage applied to VOCM sets the common mode voltage for the VDIFF+ and VDIFF- differential pair. The nominal voltage on this pin should be 2.5 V. This input requires a bias current of +/- 1 mA. VOCM can be conveniently biased by connecting it directly VREF and connecting a 1 kohm resistor from VOCM to ground.
11,14	VDIFF-, VDIFF+:	Return Loss/VSWR Output: The differential voltage on these pins is proportional to the dB return loss of the load connected to the RFOUT port when the device is driven through the RFIN port. This differential voltage has a bias level which is equal to the voltage applied to VOCM, nominally 2 V.
12	DECL	Internal decoupling node. This pin should be decoupled with at 4.7 μF capacitor to ground. The voltage on this pin, nominally 3.2 V, should not be used externally to set any bias levels.
15	VTGT	RMS Target Voltage. The voltage applied to this pin sets the target RF level at the output of the internal VGAs that drive the internal squaring cells of the rms detectors. The recommended voltage for VTGT is 1 V. Increasing V_{TGT} above 1 V degrades the rms accuracy of the ADL5920 but slightly extends the top-end detection range . Reducing V_{TGT} below 1 V can improve the rms accuracy for signals with very high crest factors. The voltage on this pin can be derived from a resistor divider circuit that is driven by the VREF pin (pin 19).
19	VREF	Reference Voltage Output. This voltage reference has a nominal value of 2.5 V. This reference output voltage can be used to set the voltage to the TADJ and VTGT and VOCM pins.
20	TADJI	RMS Detector Temperature Compensation. This pin used to fine-tune the temperature intercept stability of the rms detectors. The voltage that is applied to this pin can be derived from VREF using a simple resistor divider. Nominally grounded.
25,26, 31,32	RFOUT, RFOUT, RFIN, RFIN	RF Inputs and Outputs: The two RFIN pins are common inputs and should always be connected together. Likewise the two RFOUT pins should always be connected together. The power of the incident signal on RFIN and is measured on the VRMSF pin while the power on the incident signal into RFOUT is measured on the VRMSR pin. The ratio of the incident signals on RFIN and RFOUT is measured on the VDIFF+ and VDIFF- pins. The RFIN and RFOUT pins are interchangeable, allowing the source signal to be driven into RFOUT with the load connected to RFIN. RFIN and RFOUT are normally ac-coupled to the source and load. RFIN and RFOUT can be dc-coupled by connecting by connecting a -2.5 V supply to the two VNEG pins and by connecting the DECL pin to ground.
	EPAD	Exposed Pad: The exposed pad should be connected to a ground plane with low thermal and electrical impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

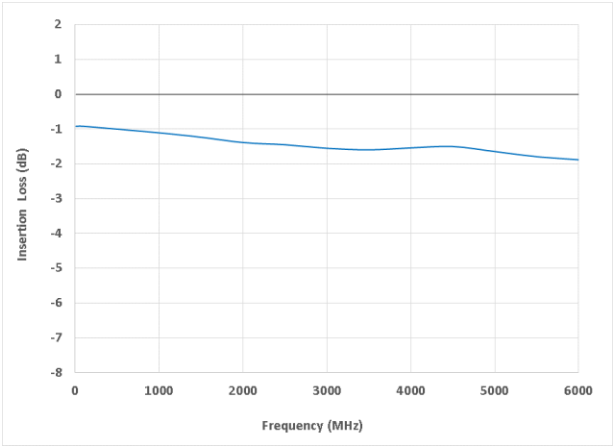

Figure 3. RFIN, RFOUT Typical Insertion Loss

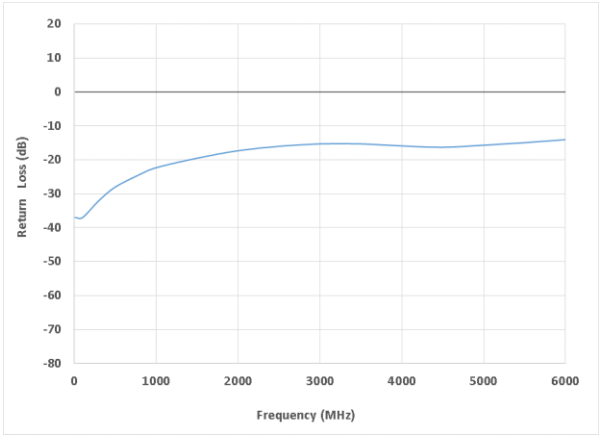

Figure 6. RFIN, RFOUT Typical Return Loss

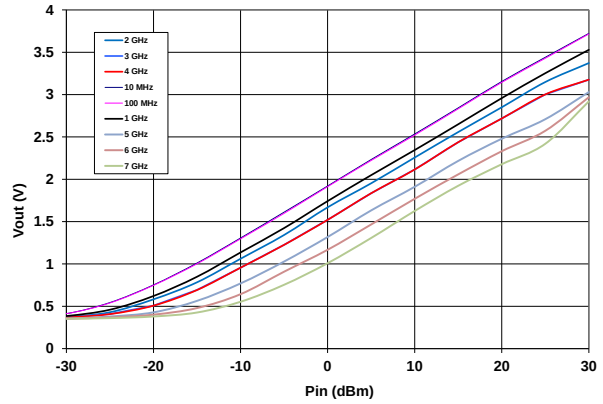

Figure 4. VRMSF vs. Input Power (dBm) and Frequency with Bridge driven from RFIN (RFOUT terminated with 50 Ohms).

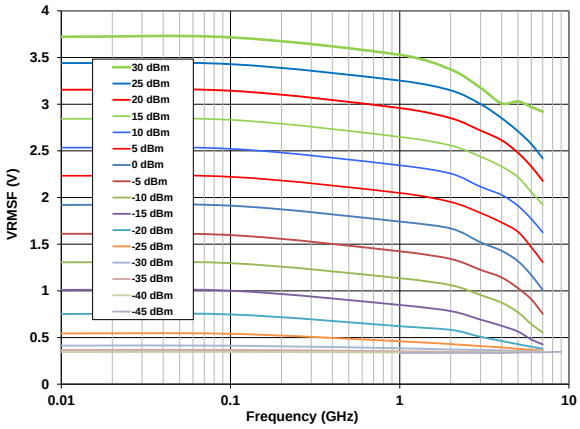

Figure 7. Typical VRMSF vs. Frequency at multiple input power levels from -25 dBm to +30 dBm (RFOUT terminated with 50 Ohms)

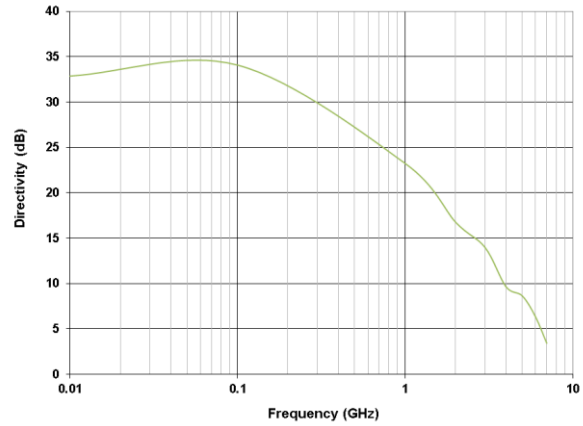

Figure 5. Bridge Directivity vs. Frequency with Bridge driven from RFIN at +20 dBm and RFOUT is terminated with 50 Ohms

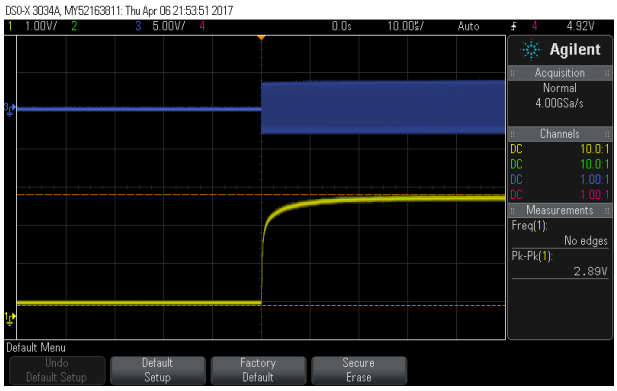

Figure 8. VRMSF Pulse Response to a 20 dBm RF Burst at 1 GHz Carrier Frequency. CRMS = 10 nF. Time base is 10 uS/div

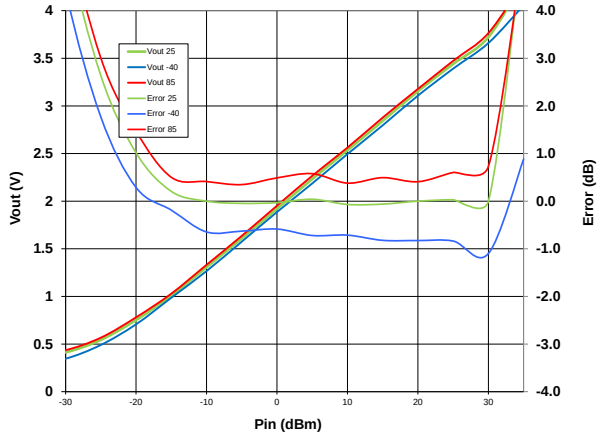

Figure 9. VRMSF vs. Input on RFIN at 10 MHz, 50 Ohm termination on RFOUT, 3-Point calibration at -10 dBm, +20 dBm and +30 dBm, TADJI=0V, TADJS=0V

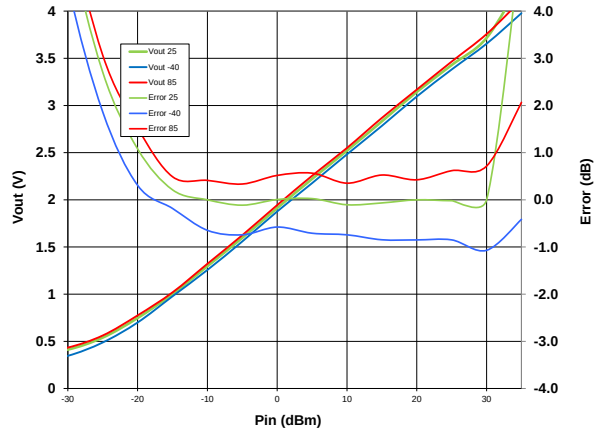

Figure 10. VRMSF vs. Input on RFIN at 100 MHz, 50 Ohm termination on RFOUT, 3-Point calibration at -10 dBm, +20 dBm and +30 dBm, TADJI=0V, TADJS=0V

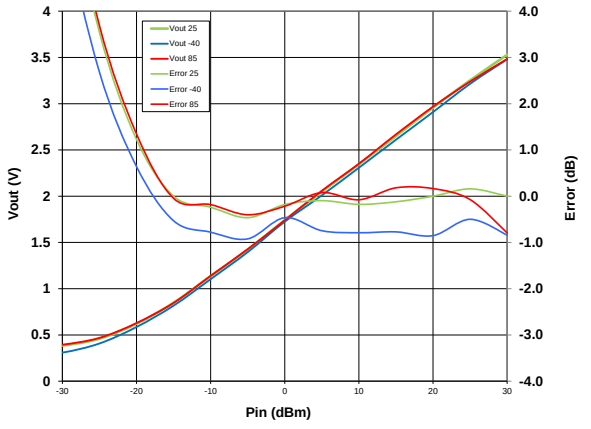

Figure 11. VRMSF vs. Input on RFIN at 1 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -15 dBm, +20 dBm and +30 dBm, TADJI=0V, TADJS=0V

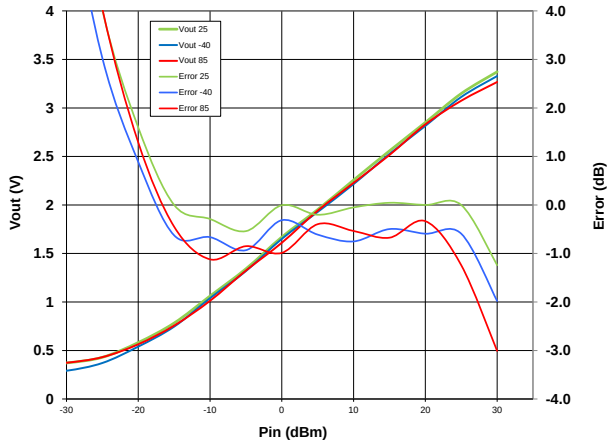

Figure 12. VRMSF vs. Input on RFIN at 2 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -15 dBm, +20 dBm and +25 dBm, TADJI=0V, TADJS=0V

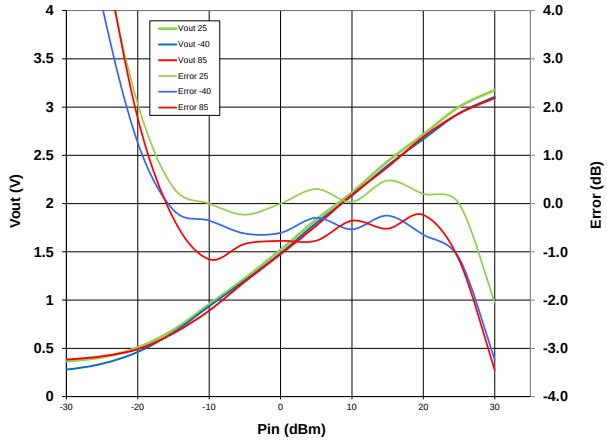

Figure 13. VRMSF vs. Input on RFIN at 3 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -10 dBm, +0 dBm and +25 dBm, TADJI=0V, TADJS=0.2 V

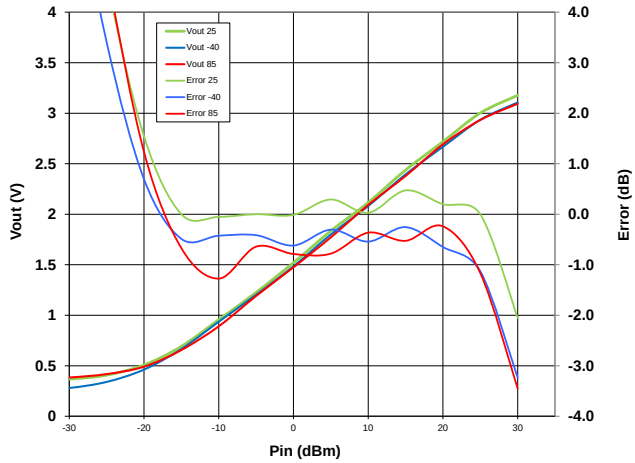

Figure 14. VRMSF vs. Input on RFIN at 4 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -15 dBm, -5 dBm and +25 dBm, TADJI=0V, TADJS=0.2 V

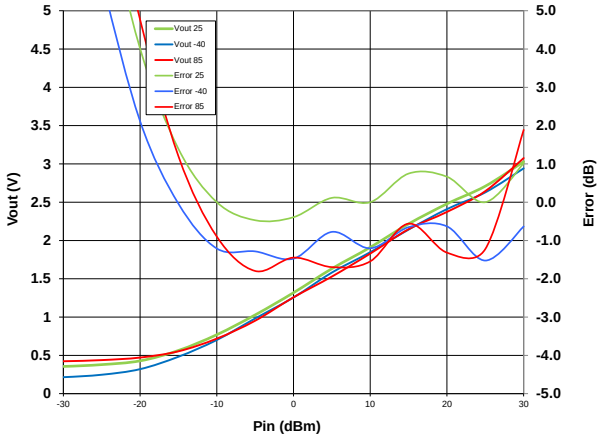

Figure 15. VRMSF vs. Input on RFIN at 5 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -10 dBm, +10 dBm and +25 dBm, TADJI=0.2V, TADJS=0 V

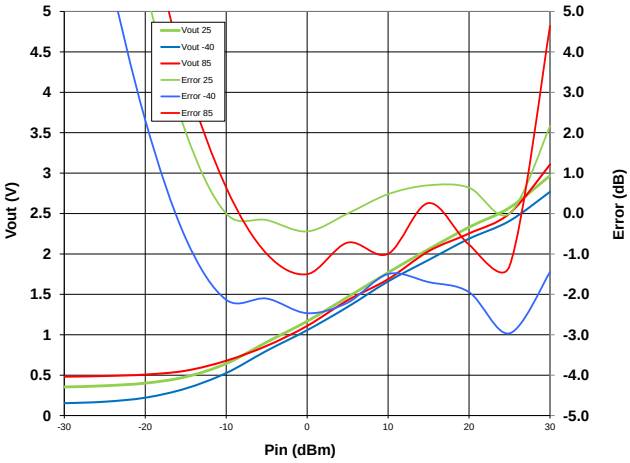

Figure 16. VRMSF vs. Input on RFIN at 6 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -10 dBm, +5 dBm and +25 dBm, TADJI=0.4V, TADJS=0 V

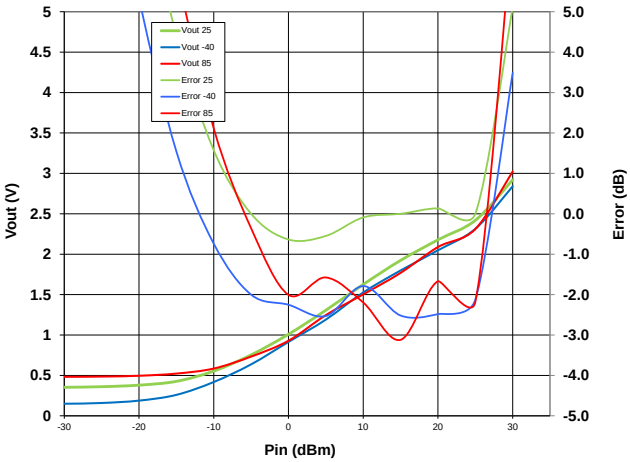

Figure 17. VRMSF vs. Input on RFIN at 7 GHz, 50 Ohm termination on RFOUT, 3-Point calibration at -5 dBm, +15 dBm and +25 dBm, TADJI=0.4V, TADJS=0 V

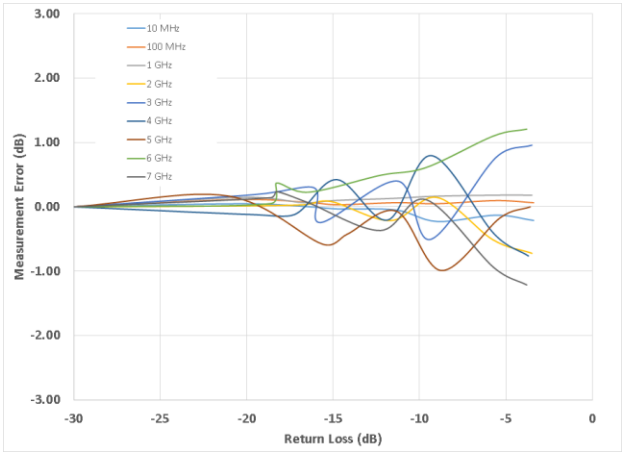

Figure 18. Power Measurement Error vs. Return Loss, Bridge Driven from RFIN with Varying Return Loss on RFOUT. VRMSF Output Voltage Calibrated with 50 ohm load on RFOUT

THEORY OF OPERATION

The ADL5920 contains a symmetric and bi-directional resistive bridge plus two identical RMS detectors that provide both forward and reverse power indications at pins VRMSF and VRMSR respectively. The device provides return loss and VSWR indication at the VDIFF+ and VDIFF- outputs, where

$$VDIFF = (VDIFF+) - (VDIFF-) = VRMSF - VRMSR \quad (1)$$

The bridge has an insertion loss of 0.9 dB below about 1 GHz when the source and load impedances are 50 Ω. The insertion loss increases with increasing frequency to about 1.9 dB at 6 GHz. Note that *insertion loss, L_I, in dB* is

$$IL = -20log_{10}|S21| = -20log_{10}\left|\frac{V_{RFOUT}}{V_{RFIN}}\right| = -20log_{10}L_I$$

in the case of equal reference impedance, Z_0, on both the input and output ports, which is the case for most systems; i.e. 50 Ohm systems. The ADL5920 is intended to be used in a 50 Ohm system.

As the source or load impedance deviates from 50 Ω, the VRMSF and VRMSR outputs indicate this via a reduction in the separation of these two voltages. For example, with a fixed signal level applied to the RFIN port and the load resistance that connected to the RFOUT port varied from a short to an open, only the VRMSR signal will change as the R_{LOAD} is changed. The VRMSF output will stay constant. The voltage difference indicates the return loss and reflection coefficient of the load and will indicate the directivity of the structure when $R_{LOAD} = R_{SOURCE} = 50\ \Omega$

The two RMS detectors are architecturally similar to the ADL5906 but are internally DC coupled to operate down to DC. They provide linear-in-dB outputs and thereby give a direct indication in dBm of the applied forward and reverse signals. Due to their linear-in-dB response, the output voltages represent the coupled and isolated port voltages in dB and thereby their difference directly indicates directivity or return loss. This is an advantage over simple diode detectors, which produce a linear-in-Volt output. The detector slope of each detector output voltage verses input power, P_{IN}, is approximately V_{SLP} = 60 mV/dB. Since both detectors are identical, the difference in output voltage with a perfectly matched source and load (50 Ω R_{SOURCE} and R_{LOAD}) is the *directivity* of the directional bridge, and is calculated as follows:

$$Directivity = \left(\frac{(VRMSF - VRMSR)}{V_{SLP}}\right) dB$$

In general directivity is defined as

$$Directivity(dB) = Coupling\ (dB) - Isolation\ (dB)$$
$$= 20log_{10}\left(\frac{C}{I}\right)$$

Where the isolation, *I*, and coupling, *C*, factors are positive numbers, and isolation is a smaller number than *C*.

In the default, single-supply and AC coupled connection (see Figure 19), the ADL5920 device directivity is about 30 dB for frequencies below 500 MHz which shows up as a constant difference voltage for the largest input powers. In the case where the signal is applied to the RFIN port (by definition the forward direction), the resulting difference voltage, VDIFF, VRMSF minus VRMSR is approximately +2 V at frequencies less than 500 MHz. However, as the input signal level is reduced, eventually the 'rejected' side will limit at the noise and offset floor and the VRMSR output will stay constant, while the VRMSF output will keep decreasing until it also reaches the noise and offset floor. Once the VRMSR output voltage is constant, one can only say that the 'directivity is greater than X' - the value calculated by the equation above. Therefore, to determine the inherent directivity of the ADL5920 measurement system it is important to apply a large enough input signal level such that one can reliably determine the isolated port voltage. This is best achieved through a P_{IN} sweep around 100 MHz.

Basic Connections

The ADL5920 requires a single supply of 5 V. The supply is connected to the VPOS1, VPOS2 and VPOS3 supply pins. Decouple each of these pins using two capacitors with values equal or similar to those shown. Place these capacitors as close as possible to the VPOS pins.

The RF input and output pins are ac-coupled using broadband 0.01 uF capacitors (recommended part number: ATC550Z103PT from ATC). This allows operation down to approximately 600 KHz. Larger value capacitors can be used to reduce the minimum input frequency further.

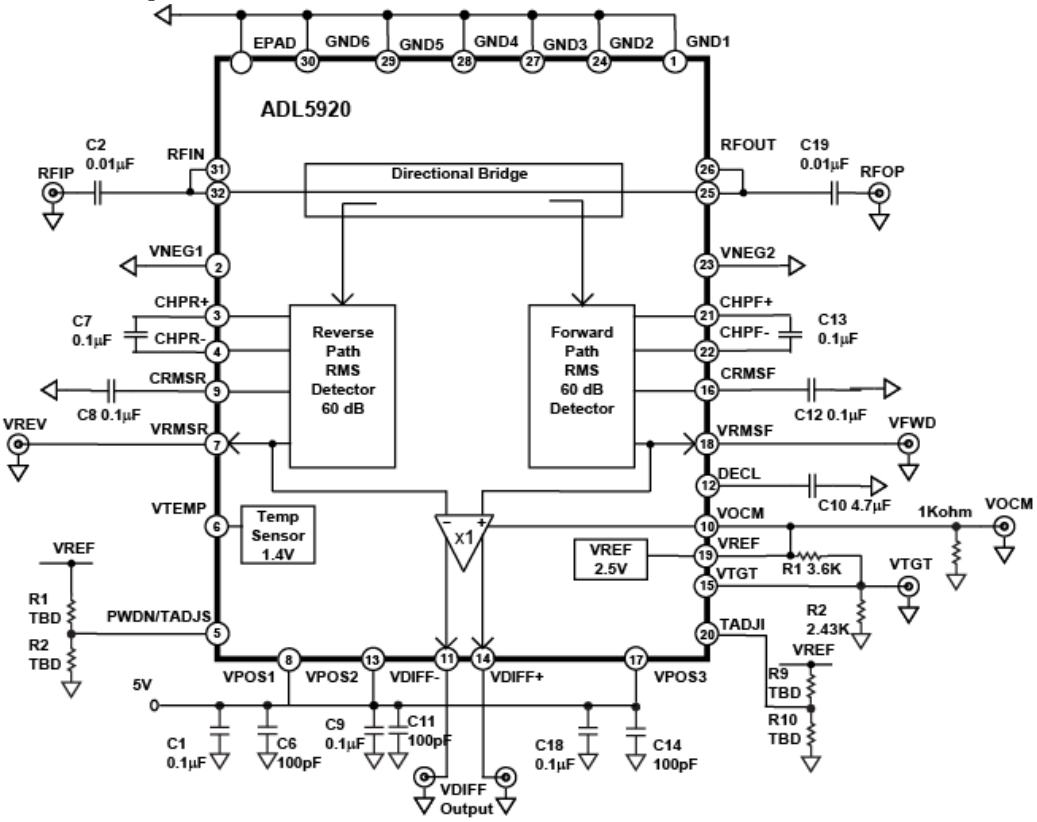

Figure 19. Basic Connections for single-supply AC-Coupled operation

RF POWER AND RETURN LOSS CALCULATION

Figure 20 shows the voltage measured on VRMSF and VRMSR when RFIN is swept across its power range at 100 MHz with a 50 ohm termination on RFOUT.As the input level varies from −25 dBm to +30 dBm, the output voltage on VRMSF varies from ~0.5 V to ~3.7 V.

The VRMSR output should ideally only respond to power reflected from the load. However because of the finite directivity of the ADL5920's bridge circuit, the VRMSR voltage starts to increase as the RF power at RFIN exceeds approximately 10 dBm. Thereafter, the VRMSR voltage follows a similar linear-in-dB response as VRMSF, albeit at a much lower level. The difference in output voltage between VRMSF and VRMSR where both voltages are following this linear-in-dB characteristic is proportional to the directivity in dB of the bridge circuit when the load is 50 ohms.

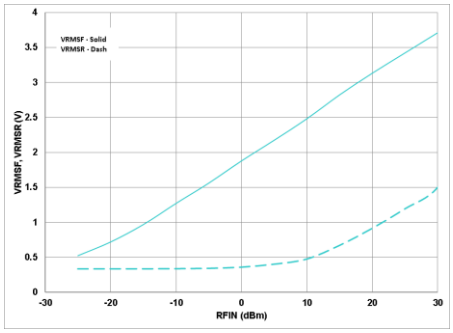

Figure 20.. VRMSF and VRMSR Output Voltage vs. Input Power at 100 MHz when Bridge is driven from RFIN and RFOUT is terminated with 50 Ohms

RETURN LOSS AND DIRECTIVITY MEAUREMENT AND CALCULATION

The equation for the idealized output voltage on VRMSF can be written as

$$V_{RMSF(IDEAL)} = Slope \times (P_{INF} - Intercept) \quad (19)$$

where:
Slope is the change in output voltage divided by the dB change in input power.
Intercept is the calculated input power level (in dBm) at which the output voltage would be equal to 0 V (note that *Intercept* is an extrapolated theoretical value not a measured value).

PINF is the power level applied to the RFIN pin.

The equation for $V_{RMSR(IDEAL)}$ will be similar with P_{INR} substituted in for P_{INF}

$$V_{RMSR(IDEAL)} = Slope \times (P_{INR} - Intercept) \quad (19)$$

Because *Slope* and *Intercept* vary from device to device and vs. frequency, calibration must be performed to achieve high accuracy.

In general, calibration is performed by applying two or more known signal levels (P_{IN1} and P_{IN2} in this case) to the input of the ADL5920 and measuring the corresponding output voltages (V_{RMSF1} and V_{RMSF2}). The calibration points should be within the linear operating range of the device.

With a two-point calibration, the slope and intercept are calculated as follows:

$$Slope = (V_{RMSF1} - V_{RMSF2})/(P_{RFIN1} - P_{RFIN2}) \quad (20)$$

$$Intercept = P_{RFIN1} - (V_{RMSF1}/Slope) \quad (21)$$

After the slope and intercept are calculated and stored in nonvolatile memory during equipment calibration, an equation can be used to calculate an unknown input power based on the output voltage of the detector.

$$P_{RFIN}(Unknown) = (V_{RMSF(MEASURED)}/Slope) + Intercept \quad (22)$$

A separate calibration can be performed to establish the slope and intercept of the reverse path. Alternatively, because the forward and reverse path bridge circuits and rms detectors are closely matched, the slope and intercept from the forward path calibration can be used to convert the VRMSR voltage into equivalent dBm RF power. Using this methodology, the following equations can be used to calculate forward power, reverse power and Return Loss.

$$P_{FWD}(dBm) = (V_{RMSF}/Slope) + Intercept \quad (22)$$

$$P_{REV}(dBm) = (V_{RMSR}/Slope) + Intercept \quad (22)$$

$$Return\ Loss(dB) = (P_{FWD} - P_{REV}) + Insertion\ Loss(dB)$$

with *Insertion Loss* having a negative sign for a passive load.

Return loss can also be calculated using the VDIFF+ and VDIFF- differential outputs using the equation:

$$Return\ Loss(dB) = (V_{DIFF+} - V_{DIFF-})Slope + Insertion\ Loss(dB) \quad (22)$$

The directivity of the bridge circuit can be calculated by putting a 50 ohm load on RFOUT and measuring VDIFF+ and VDIFF-. Directivity in dB is then given by the equation

$$Directivity(dB) = (V_{DIFF+} - V_{DIFF-})/Slope \quad (22)$$

EVALUATION BOARD

ADL5920-EVALZ is a fully populated, 4-layer, FR4- based evaluation board. For normal operation, it requires a 5 V/200 mA power supply. The 5 V power supply should be connected to the VPOS and GND test loops. The RF input and load should be applied to the RFIN and RFOUT 2.92 mm connectors respectively (since the ADL5920 is fully bi-directional, the input signal can also be applied to RFOUT with the load on RFIN). The output voltages are available on the VRMSR, VRMSF, VDIFF+ and VDIFF- SMA connectors or on the adjacent test loops. Configuration options for the evaluation board are listed in Table 8.

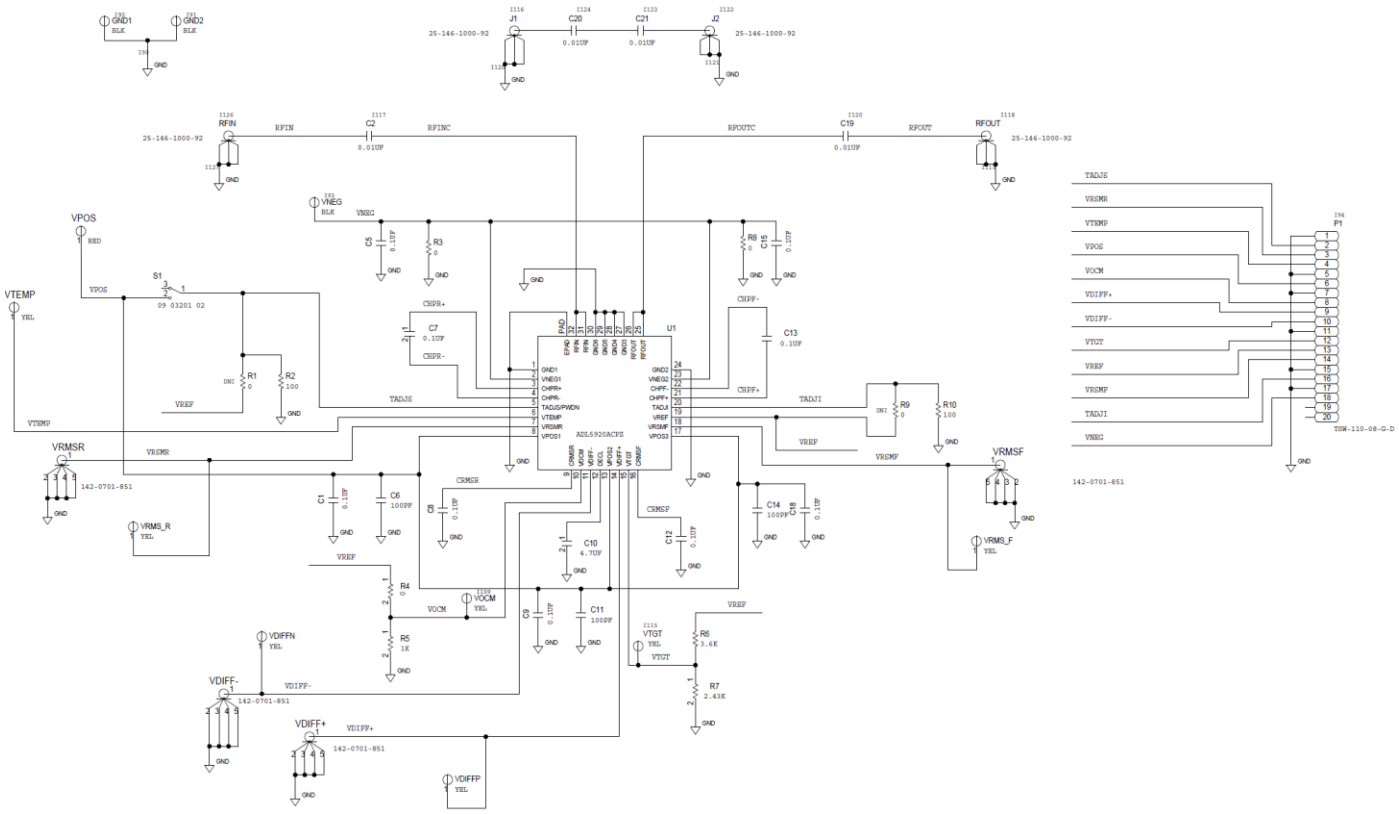

Figure 21. Evaluation Board Schematic

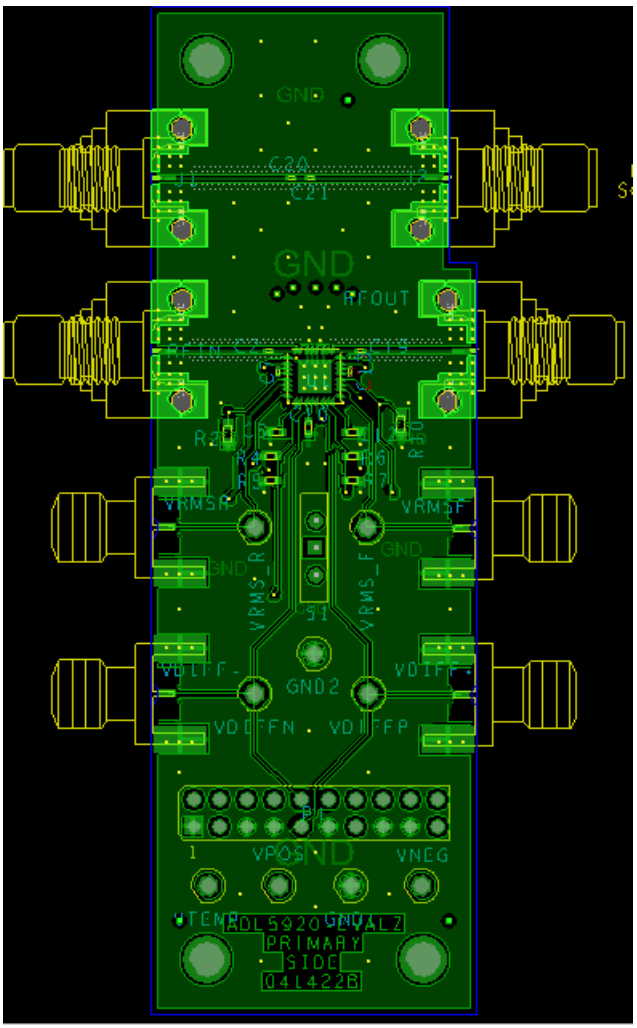

Figure 22. Evaluation Board Layout, Component Side

Table 4. Evaluation Board Configuration and Operation

Component	Function/Notes	Default Value
VPOS,GND1, GND2 C1,C6,C9, C11,C14,C18	**Power supply interface and decoupling.** Apply a 5V power supply for the evaluation board to the VPOS and GND1/GND2 test loops (GND1 and GND2 are connected to a common ground). The nominal supply decoupling on pins VPOS1, VPOS2 and VPOS3 consists of a 100 pF capacitor and a 0.1 µF capacitor on each power supply pin, with the 100 pF capacitor placed closer to the pin.	VPOS=5V GND1=GND2=0V C1,C9, C18 =0.1uF (0402) C6,C11,C14=100 pF(0402)
RFIN, RFOUT, C2, C19 28,29,30	**RF Inputs and Outputs to bridge Circuit:** The main signal path is ac-coupled by 10 nF 0201 capacitors. This sets the input corner frequency to approximately 600 KHz. For operation at lower frequencies, larger capacitor values can be installed. The RFIN and RFOUT connectors are interchangeable, allowing the source signal to be driven into RFOUT with the load connected to RFIN. The RFIN and RFOUT connectors are 2.92 mm. Care should be taken when attaching to these connectors because of their mechanical fragility.	C2=C19=10 nF (0201) RFIN, RFOUT = 2.92 mm End Launch Connector
J1, J2, C20, C21	**Calibration Path:** This path can be used to calibrate out the insertion loss of the RFIN and RFOUT traces. This signal path is ac-coupled by 10 nF 0201 capacitors. The J1 and J2 connectors are 2.92 mm. Care should be taken when connecting to these connectors because of their mechanical fragility.	C20=C21=10 nF (0201) J1, J2 = 2.92 mm End Launch Connector
VNEG, C5, C15, R3, R8, C10	**Negative Supply.** The main signal path from RFIN and RFOUT can be dc-coupled by connecting a -2.5 V supply to the VNEG test loop and replacing ac coupling caps C2 and C19 with 0 ohm resistors. R3 and R8 should be removed and replaced with 100 pF	VNEG = 0V R3=R8=0 ohms (0603) C15=C5=0.1uF (0402)

	capacitors pins. Connect the DECL pin to ground by removing C10 and replacing it with a 0 ohm resistor). In this mode the voltage on VPOS should remain at 5V.	C10 = 0.1uF (04020
R6, R7	**VTGT interface**. R7 and R6 are driven from VREF (2.5V) and provide 1 V to VTGT. If R6 and R7 are removed, an external voltage can be applied on the VTGT test point.	R7 = 2.4 kohms R6 = 3.6 kohms VTGT=1V
C7, C13	**RMS Detector Offset Compensation Loop:** The capacitances on these pins set the corner frequency of internal offset compensation loops of the two RMS detectors. These loops limit the minimum input frequency that can be sensed by the ADL5920. The default values for these capacitors set minimum input frequencies which are well below the frequency corner set by the ac-coupling capacitors in the main signal path. These capacitors should be located as close to pins 3 and 4 and pins 22 and 22	C7,C13=0.1uF (0201)
S1, R1, R2	**Device Enable and Slope Temperature Compensation.** S1 is used to disable the ADL5920 by connecting the TADJ/PWDN pin to VPOS. In its other position, S1 is open and the voltage on TADJ/PWDN is set by VREF(2.5V) and the R1,R2 resistor divider. This voltage is used to fine tune the temperature stability of the slope of the RMS detectors.	S1= open position R1= open (0603) R2= 100 ohms TADJ/PWDN = 0V
VTEMP	**Temperature Sensor Output**: This yellow test loop is connected directly to Pin 6 of the ADL5920 (VTEMP).	
VRMSF, RMSR VRMS_F, RMS_R	**Reverse and Forward RMS Voltage Measurement**: The voltages on these connectors are proportional to the dB power of the forward and reverse signals in the bridge circuit	VRMSF, VRMSR = SMA End Launch Connector VRMS_F, VRMS_R = Yellow Test Loops
C8, C12	**RMS Averaging Capacitors**. The value of the rms averaging capacitor should be set based on the peak-to-average ratio of the input signal and based on the desired output response time and residual output noise on the RMS detector outputs.	C8=C12=0.1uF (0402)
VOCM, R4, R5	**Common Mode Voltage for VDIFF+ and VDIFF-.** The voltage on VOCM pin (Pin 10) sets the common mode level for the VDIFF+ and VDIFF- differential pair. The nominal voltage on this pin should be 2.5 V. This input requires a bias current of +/- 1 mA and should be driven from a low impedance source. The nominal biasing method for VOCM is to connect it to VREF and connecting a 1 kohm resistor from VOCM to ground. An external voltage can be applied VOCM through Pin 8 of the P1 Connector.	R4= 0 ohms (0402) R5= 1 kohm (0402) VOCM = 2.5 V
VDIFF+, VDIFF- VDIFFN, VDIFFP	**Return Loss Measurement**: The output voltage from this differential pair is proportion to the ratio of the forward and reverse power in the bridge circuit. The common mode level is set by the voltage on VOCM and should be set to 2.5V	VDIFF+, VDIFF- = SMA End Launch Connector VDIFFN,VDIFFP = Yellow Test Loops
R9, R10	**TADJI Interface**: R9 and R10 set the voltage on the TADJI which is derived from VREF. This voltage is used to fine tune the temperature stability of the Intercept of the RMS detectors.	R9= open (0402) R10= 100 ohms (0402) TADJI=0V
P1	**P1 Header:** The P1 header can be used to access all of the dc levels on the evaluation board.	

OUTLINE DIMENSIONS

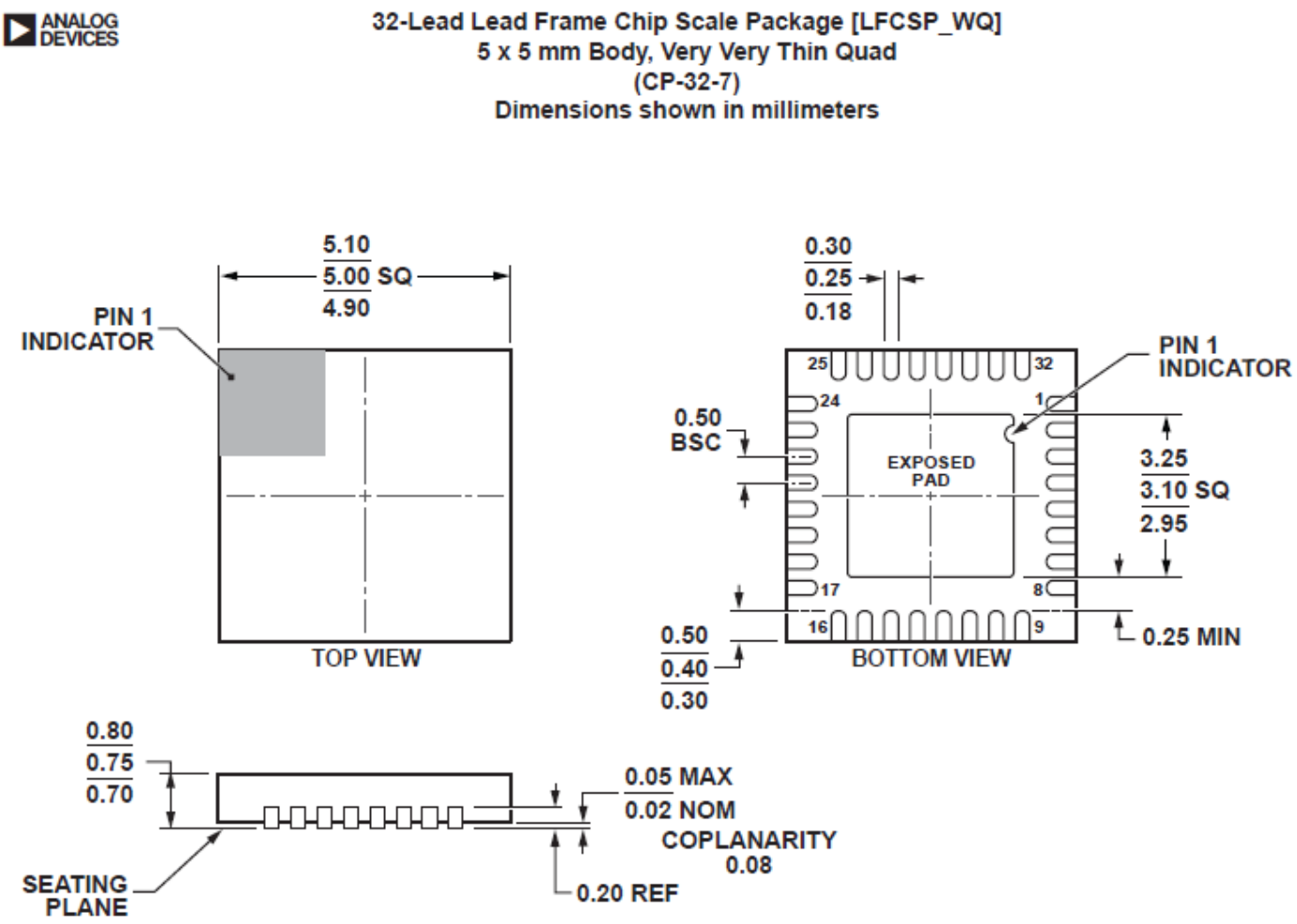

Figure 23. 5 mm x 5 mm x 0.75 mm 16-Lead Lead Frame Chip Scale Package [LFCSP CP-32-7]

NOTES

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