ANALOG DEVICES

HMC1086

v04.0714

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25 WATT GaN MMIC POWER AMPLIFIER, 2 - 6 GHz

Typical Applications

The HMC1086 is ideal for:

- Test Instrumentation
- General Communications
- Radar

Features

High Psat: +44.5 dBm

Power Gain at Psat: 14 dB

High Output IP3: +48 dBm

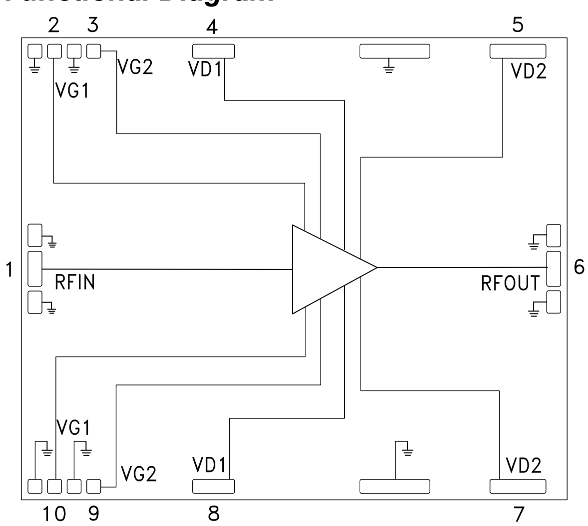
Small Signal Gain: 22 dB

Supply Voltage: +28 V @ 1.1 A

50 Ohm Matched Input/Output

Die Size: 3.4 x 4 x 0.1 mm^2

Functional Diagram



General Description

The HMC1086 is a 25W Gallium Nitride (GaN) Power Amplifier MMIC which operates between 2 and 6 GHz. The amplifier typically provides 22 dB of small signal gain, +44.5 dBm of saturated output power, and +48 dBm output IP3 at +33 dBm output power per tone. The HMC1086 draws 1100 mA quiescent current from a +28V DC supply. The RF I/Os are DC blocked and matched to 50 Ohms for ease of integration into Multi-Chip-Modules (MCM). All electrical performance data was acquired with die eutectically attached to 1.02 mm (40 mil) thick CuMo carrier with multiple 1.0 mil diameter ball bonds connecting the die to 50 Ohm transmission lines on alumina.

Electrical Specifications, T_A = +25 °C, Vdd = VD1 = VD2 = +28V, Idd = 1100 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		2 - 3.5			3.5 - 5			5 - 6		GHz
Small Signal Gain	21	22		22	23		21	22		dB
Gain Flatness		±0.5			±0.5			±0.5		dB
Gain Variation Over Temperature		0.012			0.016			0.024		dB/ °C
Input Return Loss		10			15			15		dB
Output Return Loss		8			8			8		dB
Power Gain (Pin @ 25 dBm)		18			18			18		dB
Saturated Output Power (Psat)		44.5			45			44.5		dBm
Output Third Order Intercept (IP3) [2]		48			48			48		dBm
Power Added Efficiency		42			37			34		%
Quiescent Supply Current (Idd @ Vdd = +28V)		1100			1100			1100		mA

[1] Assumes eutectic attach of die to a 40 mil CuMo carrier, and 25 °C is maintained at the back of the carrier.

[2] Measurement taken at Pout / tone = +33 dBm.

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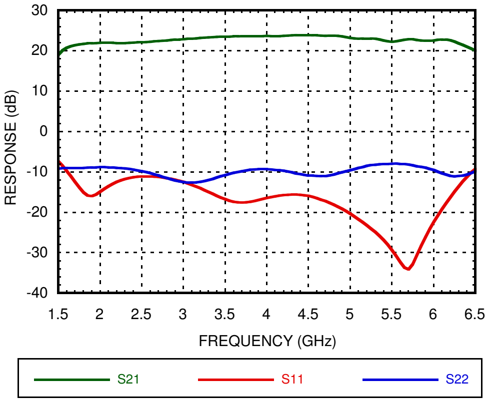
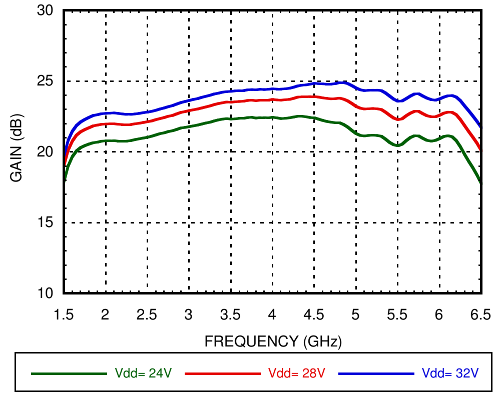
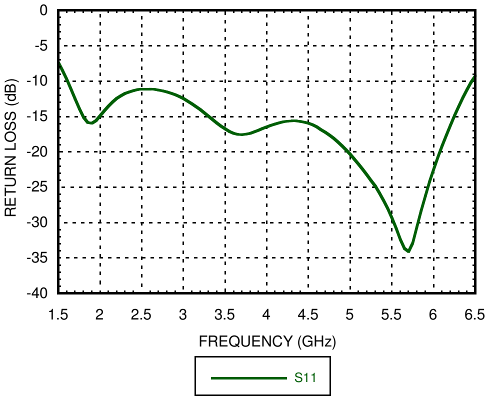
Gain and Return Loss



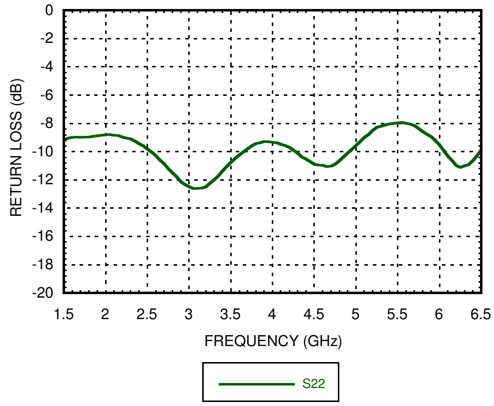
Gain vs. Vdd



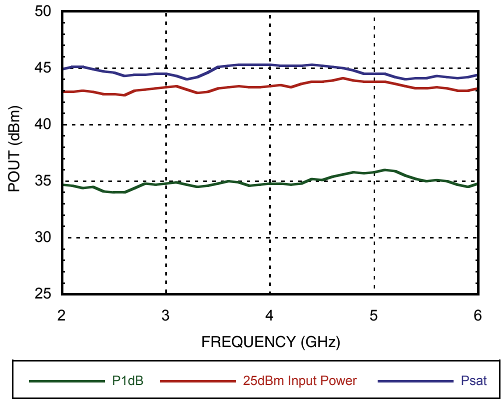
Input Return Loss



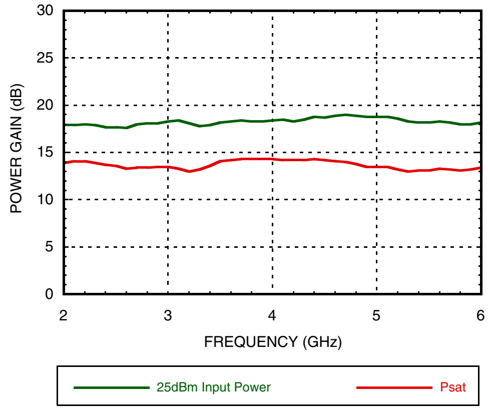
Output Return Loss



Pout vs. Frequency



Power Gain vs. Frequency



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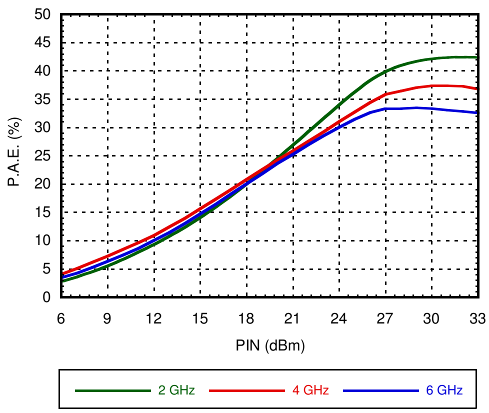
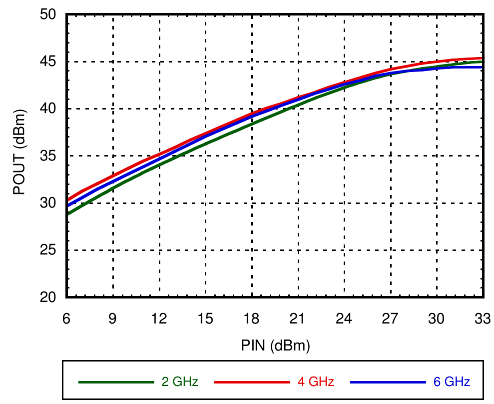
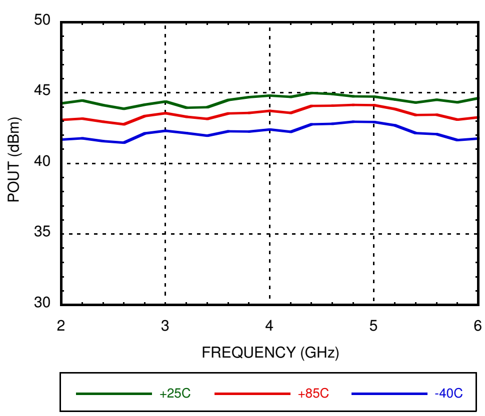
Power Added Efficiency vs. Pin



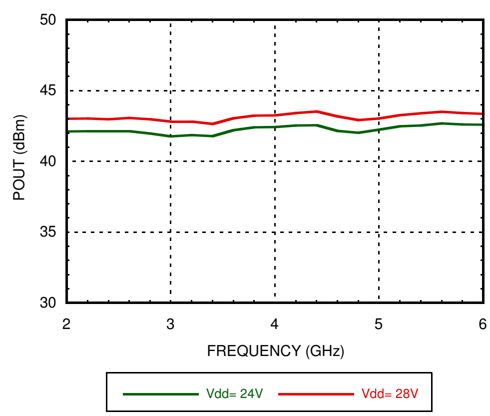
Pout vs. Pin



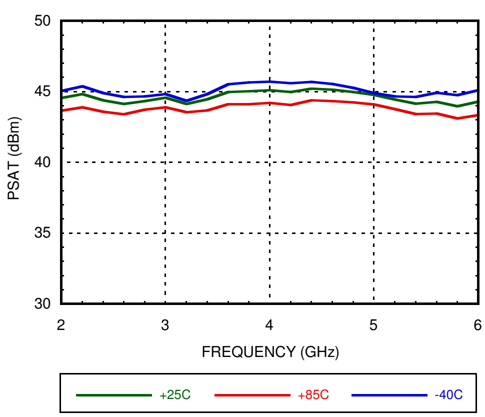
Pout vs. Temperature at Pin= 25dBm



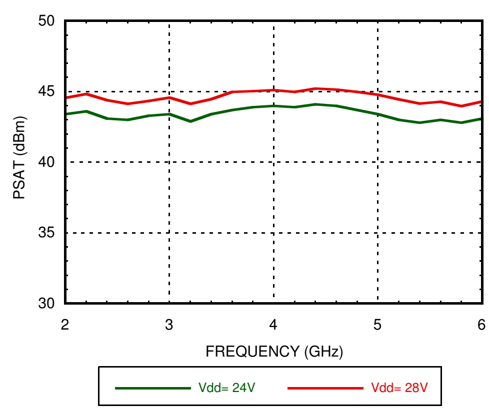
Pout vs. Vdd at Pin= 25dBm



Psat vs. Temperature



Psat vs. Vdd



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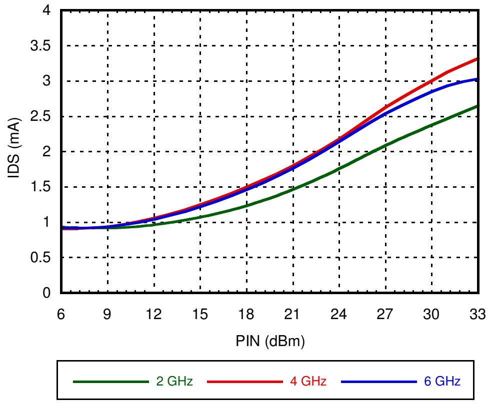
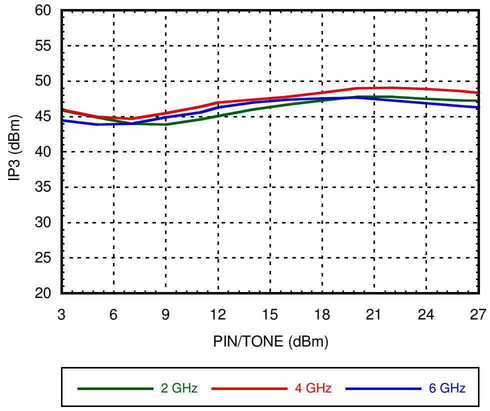
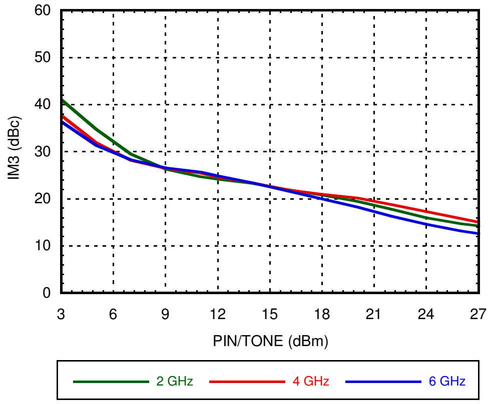
Drain Current vs. Pin



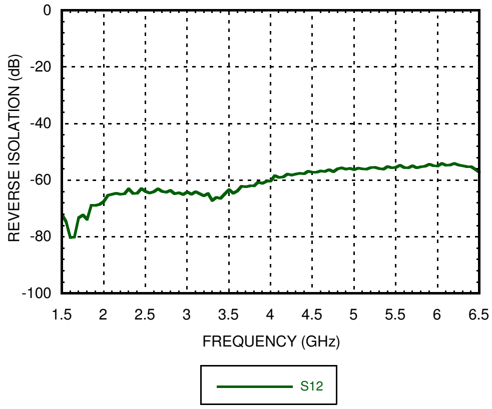
OIP3 vs Pin/Tone



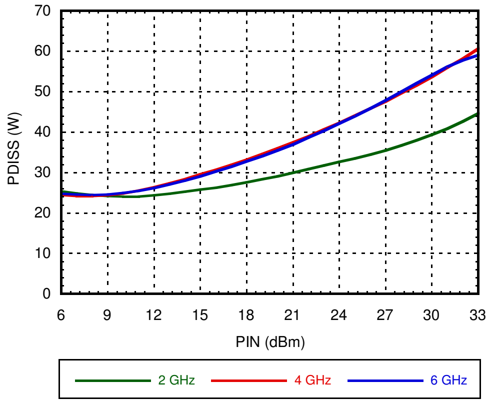
IM3 vs. Pin/Tone



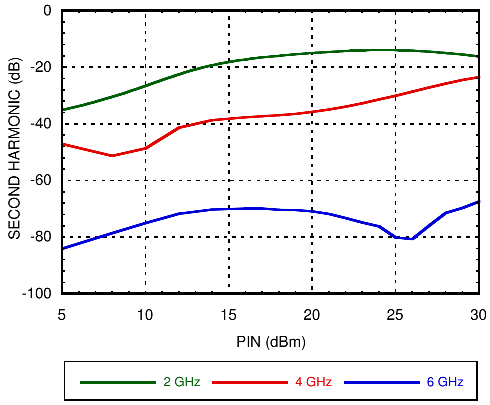
Reverse Isolation



Power Dissipation vs. Pin



Second Harmonic vs. Pin



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Absolute Maximum Ratings[1]

Drain Bias Voltage (Vdd)	+32V
Gate Bias Voltage (Vgg)	-8 V to 0V
Maximum Forward Gate Current	11 mA
Maximum RF Input Power (RFIN)	33 dBm
Maximum VSWR[2]	6:1
Maximum Junction Temperature (Tj)	225 °C
Maximum Pdiss (T = 85 °C) (Derate 455 mW/°C above 85 °C)	63.6W
Thermal Resistance (R_{TH})[3]	2.2°C/W
Operating Temperature	-40 °C to +85°C
Storage Temperature	-55 °C to 150 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

[1] Operation outside parameter ranges above can cause permanent damage to the device. These are maximum stress ratings only. Continuous operation of the device at these conditions is not implied.
[2] Assumes 0.5 mil AuSn die attach to a 40 mil CuMo Carrier with 85°C at the back of the carrier.
[3] Restricted by maximum power dissipation

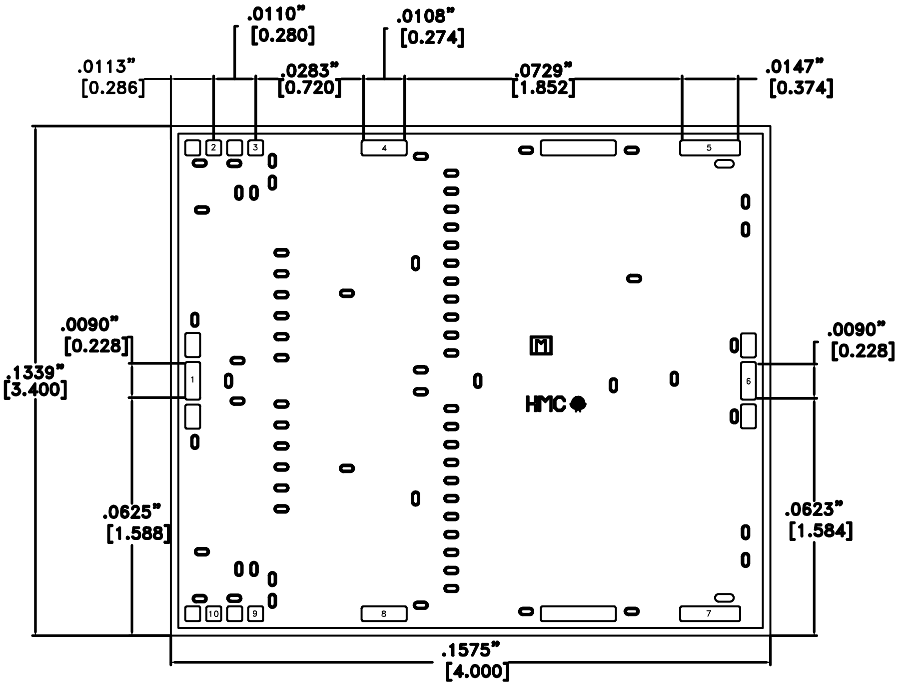
Die Packaging Information [1]

Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] Refer to the “Packaging Information” section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .004”
3. TYPICAL BOND PAD IS 0.0026” [0.066] SQUARE
4. BACKSIDE METALLIZATION: GOLD
5. BOND PAD METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND.
7. CONNECTION NOT REQUIRED FOR UNLABELED BOND PADS.
8. OVERALL DIE SIZE ± .002

Outline Drawing



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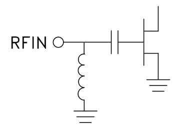
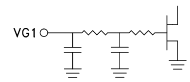
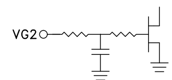
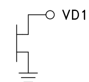
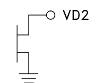
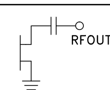
Pad Descriptions

Pad Number	Function	Description	Pin Schematic
1	RFIN	This Pad is RF coupled and is matched to 50 Ohms. The pad has zero Ohms DC resistance.	
2, 10	VG1	Gate control voltage for first stage.	
3, 9	VG2	Gate control voltage for second stage.	
4,8	VD1	Drain bias for first stage.	
5, 7	VD2	Drain bias for second stage.	
6	RFOUT	This Pad is RF coupled and is matched to 50 Ohms.	
Die Bottom	GND	Die Bottom must be connected to RF/DC ground.	

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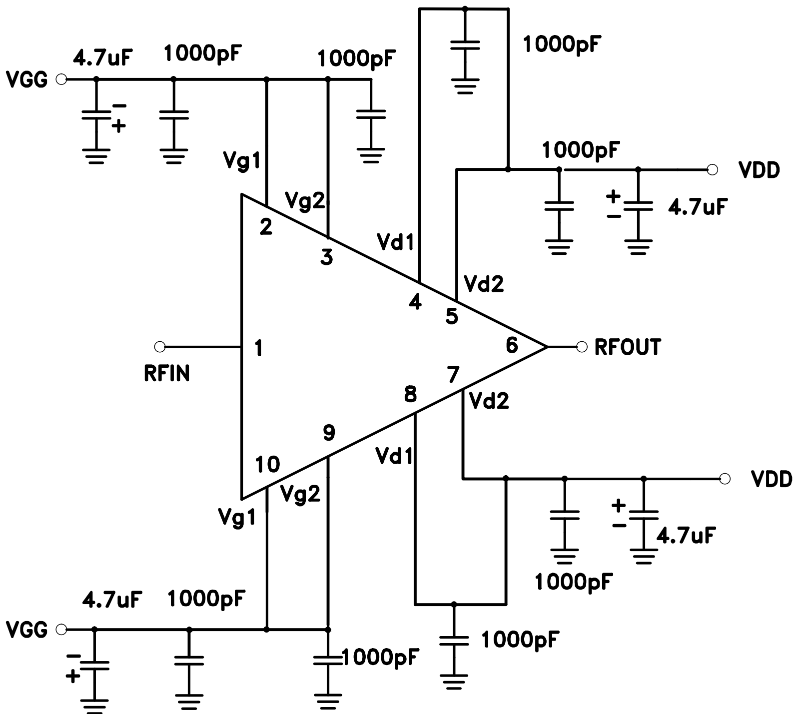
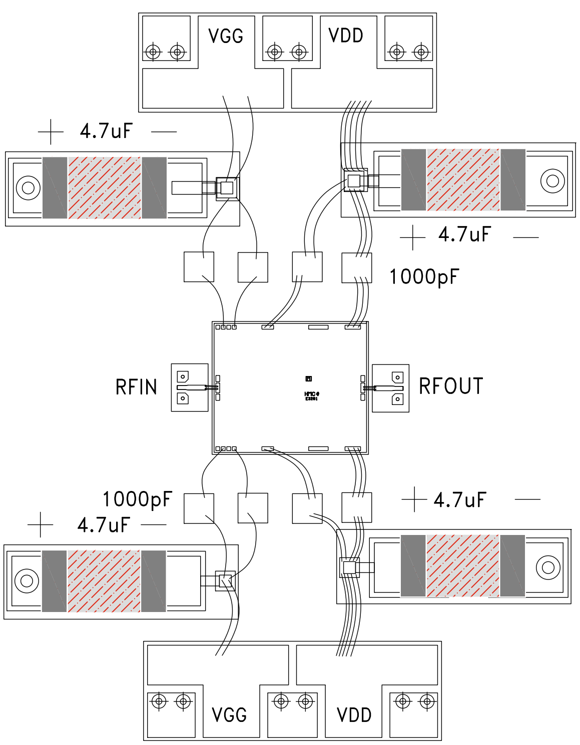
Application Circuit



Assembly Diagram



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Mounting & Bonding Techniques for GaN MMICs

The die should be eutectically attached directly to the ground plane (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254 mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150 mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102 mm (4 mil) thick die to a copper tungsten or CuMo heat spreader which is then attached to the thermally conductive ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076 mm to 0.152 mm (3 to 6 mils).

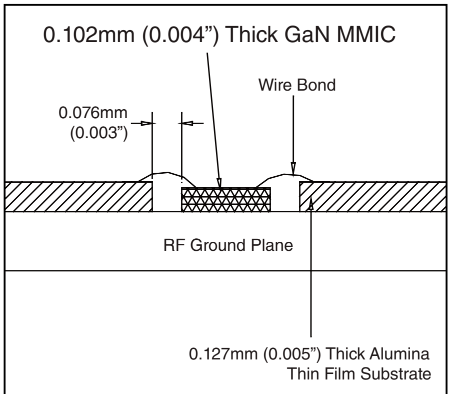

Figure 1.

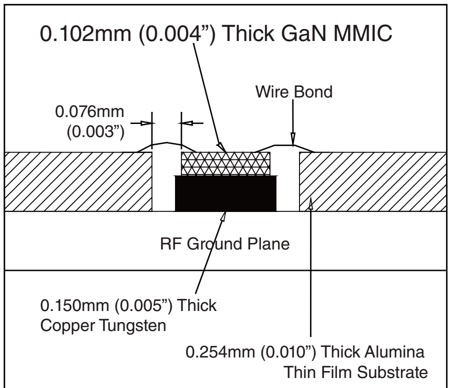

Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

Die placement: A heated vacuum collect (180 °C) is the preferred method of pick up. Ensure that the area of vacuum contact on the die is minimized to prevent cracking under differential pressure. All air bridges (if applicable) must be avoided during placement. Minimize impact forces applied to the die during auto-placement.

Mounting

The chip is back-metallized with a minimum of 5 microns of gold and is the RF ground and thermal interface. It is recommended that the chip be die mounted with AuSn eutectic preforms. The mounting surface should be clean and flat.

Eutectic Reflow Process: An 80/20 gold tin 0.5 mil (13 um) thick preform is recommended with a work surface temperature of 280 °C. Limit exposure to temperatures above 300 °C to 30 seconds maximum. A die bonder or furnace with 95 % N_2 / 5 % H_2 reducing atmosphere should be used. No organic flux should be used. Coefficient of thermal expansion matching is critical for long term reliability.

Die Attach Inspection: X-ray or acoustic scan is recommended.

Wire Bonding

Thermosonic ball or wedge bonding is the preferred interconnect technique. Gold wire must be used in a diameter appropriate for the pad size and number of bonds applied. Force, time and ultrasonics are critical parameters: optimize for a repeatable, high bond pull strength. Limit the die bond pad surface temperature to 200 °C maximum.

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