Isolated Synchronous Forward Controller with Active Clamp and *i*Coupler

Preliminary Technical Data

ADP1074

FEATURES

- Current Mode Controller for active clamp forward topology
- Integrated 5 kV isolation with Analog Devices *i*Coupler technology
- Wide voltage supply range
  - Primary V_{DD}: Up to 60 V
  - Secondary V_{DD2}: Up to 36 V
- Integrated 1A primary side MOSFET driver for power switch and active clamp reset switch
- Integrated 1A secondary side MOSFET driver for synchronous rectification
- Integrated error amplifier and < 1% accurate reference voltage
- Programmable slope compensation
- Programmable frequency range: 50 kHz – 600 kHz
- Frequency synchronization
- Programmable maximum duty cycle limit
- Programmable soft start
- Smooth soft start from pre-charged load
- Programmable dead time
- Power saving light load mode using MODE pin
- Protection features such as short circuit, output overvoltage, and over temperature protection
- Cycle-by-cycle input overcurrent protection
- Precision enable UVLO with hysteresis
- Power Good pin for system flagging
- Tracking function from secondary side
- Remote (secondary side) shutdown/reset function
- Available in 24-pin SOIC_W package

APPLICATIONS

- Isolated DC/DC Power conversion
- Intermediate Bus Voltage Generation
- Telecom, Industrial
- Base station and Antenna RF power
- Small Cell
- PoE Powered Device
- Enterprise Switches/Routers
- Core/Edge/Metro/Optical Routing
- Power Modules

GENERAL DESCRIPTION

The ADP1074[1] is a current mode fixed frequency active-clamp synchronous forward controller designed for isolated DC-to-DC power supplies. Analog Devices, Inc., proprietary *i*Coupler® devices are integrated in the ADP1074 to eliminate the bulky signal transformers and opto-couplers that transmit signals over the isolation boundary. This reduces system design complexity, cost, component count, and improves overall system reliability. With the integrated isolators and MOSFET drivers on both the primary and the secondary, the ADP1074 offers a compact system level design and yields a higher efficiency than a non-synchronous forward converter at heavy loads.

The primary side pins provide functions for programming the switching frequency and maximum duty cycle, external frequency synchronization and slope compensation.

The secondary side pins provide functions for differential output voltage sensing, over voltage, power good, and programmable light load mode setting.

The feedback signal and timing of synchronous rectifier PWMs are transmitted between the primary and secondary or secondary to primary through the *i*Couplers using a proprietary transmission scheme.

The ADP1074 also offers features such as input current protection, under voltage lockout (UVLO), precision enable with adjustable hysteresis, and over temperature protection (OTP) and light load power saving mode (LLM).

[1] Protected by U.S. Patent US 7,075,329 B2.

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TYPICAL APPLICATION CIRCUITS

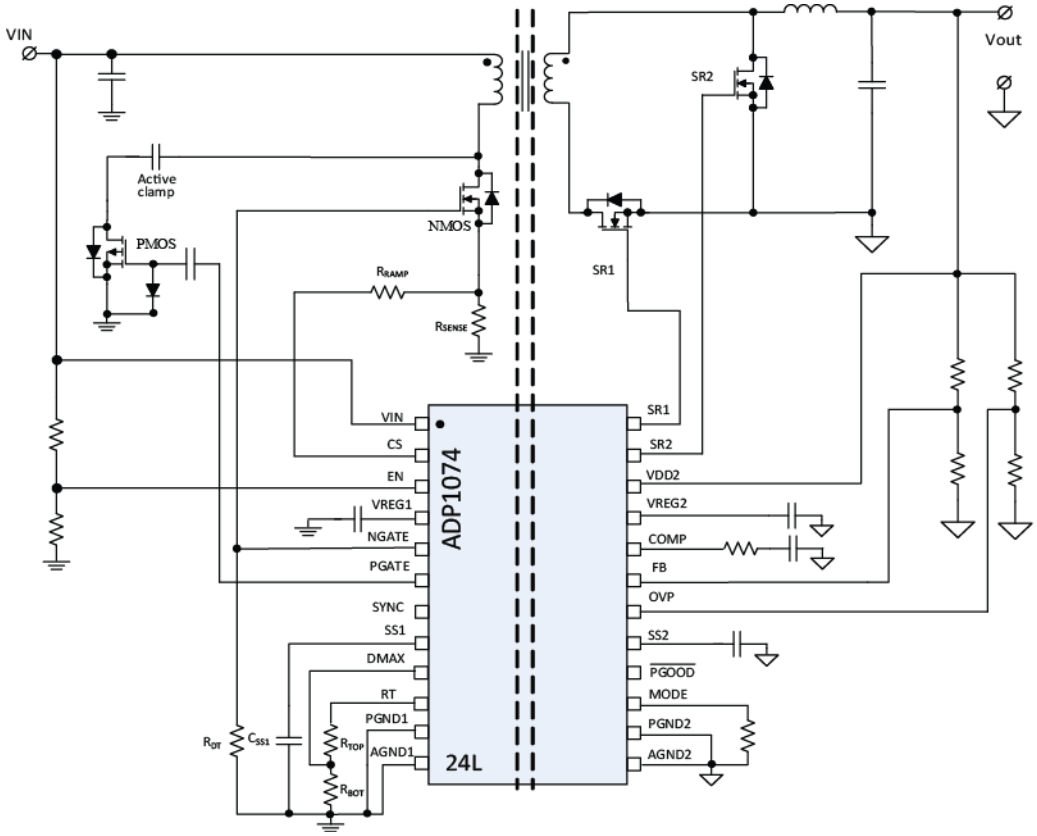

Figure 1. Typical Application Circuit for Active Clamp Forward Topology

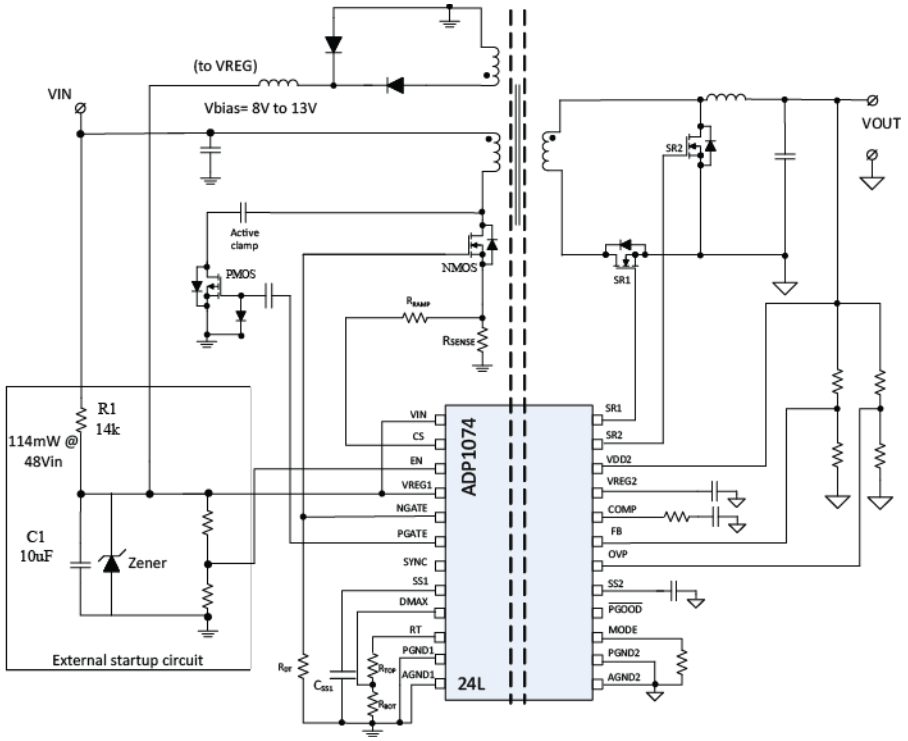

Figure 2. Typical Application Circuit for Active Clamp Forward Topology with Simple Startup Circuit and Bias Winding

SPECIFICATIONS

V_{IN} =24V, V_{DD2} = 12 V, T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY (primary)						
Supply Voltage	V_{IN}	4.7 µF capacitor from Vin to PGND1 1 µF capacitor from VREG1 to PGND1	4.7	24	60	V
Quiescent Supply Current	I_{VIN}	$V_{IN} > V_{IN\_UVLO}$, NGATE and PGATE unloaded At 100kHz				
		At 300kHz		3.8		mA
		At 600kHz		4.4		mA
				6.8		mA
	I_{VIN}	$V_{IN} > V_{IN\_UVLO}$, NGATE and PGATE loaded with 2.2nF and 410pF respectively				
		At 100kHz				
		At 300kHz		6		mA
		At 600kHz		1w2		mA
		V_{EN} < 1.2 V, VREG1= 0V, VIN= 60 V		24		mA
VIN shutdown current					35	µA
(VIN + VREG1) startup current	$I_{VIN\_startup}$	V_{EN} < 1.2 V, VREG1= 12 V, VIN= 12 V			160	µA
VIN UVLO		VIN rising	4.3	4.5	4.7	V
		VIN falling		4.3		V
UVLO hysteresis		EN>1.2 V, 1 µF capacitor on VREG1		-0.1		V
Time from EN high to PGATE output switching					1	ms
Time from EN low to SR1/2 output stops switching		EN<1.0 V, 1 µF capacitor on VREG1			1	µs
SUPPLY (secondary)						
Supply Voltage	V_{DD2}	4.7 µF capacitor from VDD2 to PGND2 1 µF capacitor from VREG2 to PGND2	4.5	12	36	V
Quiescent supply current	I_{DD2}	SR1 and SR2 unloaded At 100kHz		6.3		mA
		At 300kHz		6.4		mA
		At 600kHz		6.9		mA
	I_{DD2}	SR1 and SR2 loaded with 2.2nF				
		At 100kHz		9		mA
		At 300kHz		13.5		mA
		At 600kHz		20		mA
UVLO threshold		V_{DD2} rising		3.5		V
		V_{DD2} falling		3.45		V
UVLO Hysteresis				50		mV
Secondary UVLO hiccup time				225		ms
OSCILLATOR						
Switching frequency (f_s)		R_{RT} = 480 kΩ (±1%)	-10%	50	+10%	kHz
		R_{RT} = 240 kΩ (±1%)	-10%	100	+10%	kHz
		R_{RT} = 120 kΩ (±1%)	-10%	200	+10%	kHz
		R_{RT} = 80 kΩ (±1%)	-10%	300	+10%	kHz
		R_{RT} = 60 kΩ (±1%)	-10%	400	+10%	kHz
		R_{RT} = 40 kΩ (±1%)	-10%	600	+10%	kHz
VREG1 pin						
VREG1 voltage clamp		I_{VREG} = 3mA, V_{EN} < 1.2 V	13.5	14.3	15.2	V
VREG1 clamp series resistance		VREG1 current 5mA and 15mA		16		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GATE drivers (primary)						
NGATE and PGATE high voltage		I_{VREG1} = 20mA, VIN > 9V	7.6	8	8.4	V
Gate short circuit peak current[1]		8 V on VREG1		1.0		A
NGATE Rise Time		C_{NGATE} = 2.2 nF, 10% to 90%		16		ns
NGATE Fall Time		C_{NGATE} = 2.2 nF, 90% to 10%		16		ns
PGATE Rise Time		C_{PGATE} = 410 pF, 10% to 90%		8		ns
PGATE Fall Time		C_{PGATE} = 410 pF, 90% to 10%		8		ns
NGATE R_{ON}	R_{ON_SOURCE}	Source 100mA		6		Ω
NGATE R_{ON}	R_{ON_SINK}	Sink 100mA		4		Ω
NGATE Max Duty Cycle	D_{MAX}	R_{BOT}= 0 Ω	45	50	55	%
		R_{TOP}= R_{BOT}, 1% resistors		75		%
NGATE minimum on time		At 300 kHz, includes blanking time		170		ns
PGATE R_{ON}	R_{ON_SOURCE}	Source 100mA		10		Ω
PGATE R_{ON}	R_{ON_SINK}	Sink 100mA		8		Ω
SRx drivers (secondary)						
SR1 and SR2 high voltage		I_{VREG2} = 15mA, VDD2 > 5.5V	4.7	5	5.3	V
Gate short circuit peak current[2]		5 V on VREG2		1.0		A
SRx Rise Time		C_{SRx} = 2.2 nF, 10% to 90%		14		ns
SRx Fall Time		C_{SRx} = 2.2 nF, 90% to 10%		11		ns
SRx minimum on time		At 300 kHz		220		ns
SR1, SR2 R_{ON}	$R_{ON\_SR\_SOURCE}$	Source 100mA		6		Ω
	$R_{ON\_SR\_SINK}$	Sink 100mA		4		Ω
GATE Delay (SR1 rising to NGATE rising)				40		ns
Delay between NGATE falling edge and SR1 falling edge				14		ns
SR Dead time (PGATE rising to SR2 falling)		Resistor (±5%) at NGATE				
		R_{DT} = 10 kΩ		150		ns
		R_{DT} = 22 kΩ		100		ns
		R_{DT} = 47 kΩ		60		ns
		R_{DT} = open		30		ns
SR1 and SR2 dead time		Dead time between SR1 and SR2		25		ns
CURRENT LIMIT SENSE (primary)						
CS limit threshold	V_{CS_LIM}	Over current sense limit threshold		120		mV
CS leading edge blanking time				150		ns
Current source di/dt for slope compensation				20		µA/Ts
OCP comparator delay				20		ns
Time in OCP before entering hiccup mode				1.25		ms
OCP hiccup time				45		ms
FB PIN AND ERROR AMPLIFIER						
Feedback Accuracy Voltage	V_{FB}	T_J = –40°C to +85°C	–0.85%	+1.2	+0.85%	V
		T_J = –40°C to +125°C	–1.5%	+1.2	+1.5%	V
FB Input Bias Current			-100	1	+100	nA
Transconductance	gm		212	250	287	µS
Output current clamp minimum				-65		µA
Output current clamp maximum				40		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
COMP clamp maximum voltage		20uA sourcing current to COMP pin		2.52		V
COMP clamp minimum voltage		20uA sinking current from COMP pin		0.6		V
Open loop gain				80		dB
Output shunt resistance				5		GΩ
Gain Bandwidth Product				1		MHz
PRECISION ENABLE THRESHOLD						
EN threshold	V_{EN}	EN rising	1.14	1.2	1.26	V
EN hysteresis		V_{EN} < 1.2 V	3	4	5	mA
		V_{EN} > 1.2 V		1		µA
EN Hysteresis current				3		µA
MODE pin						
Light Load Mode current		Connect a resistor from MODE to AGND2	5	6	7	µA
Temperature						
Thermal shutdown				155		°C
Hysteresis				-15		°C
SOFT START SS1 and SS2 pins						
Primary side SS1 current source		During soft start only		8		µA
Secondary side SS2 current source		During soft start only, post-handover		20		µA
			15		25	µA
SS2 discharging current		During a fault condition or soft stop		30		µA
SYNC pin						
Synchronization Range			50		600	kHz
Input Pulse Width			100			ns
Number of cycles before synchronization				7		
Input low voltage					0.4	V
Input high voltage			3			V
Leakage Current					1	µA
COMP signal delay through *i*Coupler				600		ns
*i*COUPLER						
Rated Dielectric Insulation Voltage		1 minute duration		5		kV
Minimum External Air Gap (Clearance)		Measured from input terminals to output terminals, shortest distance through air		7.6 min		mm
Minimum External Air Gap (Creepage)		Measured from input terminals to output terminals, shortest distance path along body		7.6 min		mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation		0.030		mm
Tracking Resistance (Comparative Tracking Index)	CTI	Material Group (DIN VDE 0110, 1/89, Table		>400		V
Isolation Group				II		
Common mode Transient Immunity, Dynamic			-25		25	kV/µs
FB, OVP, AND $\overline{\text{PGOOD}}$ THRESHOLDS		Over-voltage threshold for $\overline{\text{PGOOD}}$ to toggle for FB and OVP pin	1.3	1.36	1.42	V
FB pin OV Hysteresis				25		mV
FB pin UV threshold		Under-voltage threshold for $\overline{\text{PGOOD}}$ to toggle	1.04	1.11	1.16	V
FB pin UV Hysteresis				25		mV
OVP comparator delay (includes *i*Coupler delay)				250		ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Time from fault condition to $\overline{\text{PGOOD}}$ toggling		OVP pin fault to $\overline{\text{PGOOD}}$ toggling		50		µs
		FB pin OV/UV to $_V$ toggling		5		µs
OVP pin leakage current				1		µA
$\overline{\text{PGOOD}}$ pin leakage current				1		µA
OVP hiccup		Time before entering OVP hiccup mode		200		ms
		Hiccup time trigged by OVP event		200		ms

[1] Short-circuit duration less than 1 µs. Average power must conform to the limit shown under the Absolute Maximum Ratings.

[2] Short-circuit duration less than 1 µs. Average power must conform to the limit shown under the Absolute Maximum Ratings.

REGULATORY INFORMATION

See Table 5 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 2.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified by CQC11-471543-2012, GB4943.1-2011:
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (1 MOPP)), 490 V rms (686 V peak) Reinforced insulation (2 MOPP), 238 V rms (325 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 780 V secondary (1103 V peak)	Reinforced insulation, V_{IORM} = 849 peak, V_{IOTM} = 8000 V peak	Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 389 V rms (552 V peak), tropical climate, altitude ≤5000 meters
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each product is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN, EN	-0.3V to 66 V
VDD2	-0.3V to 42 V
VREG1	-0.3V to 16V
NGATE, PGATE	-0.3V to 16V
RT, CS, SYNC, SS1, SS2, $\overline{\text{PGOOD}}$, FB, COMP, OVP, MODE, DMAX, SR1, SR2, VREG2	-0.3V to 6V
AGND1, PGND1, AGND2, PGND2	±0.3 V
Common mode Transients[1]	±25 kV/µs
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD	
Charged Device Model	250 V
Human Body Model	1 kV

[1] Refers to common mode transients across the insulation barrier. Common mode transients exceeding the absolute maximum rating can cause latch up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. JEDEC thermal resistance values (θ_{JA} & θ_{JC}) and thermal characterization parameter (Ψ_{JT}) shown in Table 4 should be used in compliance with JEDEC standards for thermal reporting (JESD51-12).

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}
SOIC_W 24-Lead	65.4 °C/W	43.8 °C/W	9.1 °C/W

Table 5. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
WAVEFORM			
AC Voltage			
Bipolar	560	V peak	50-year minimum lifetime
Unipolar	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

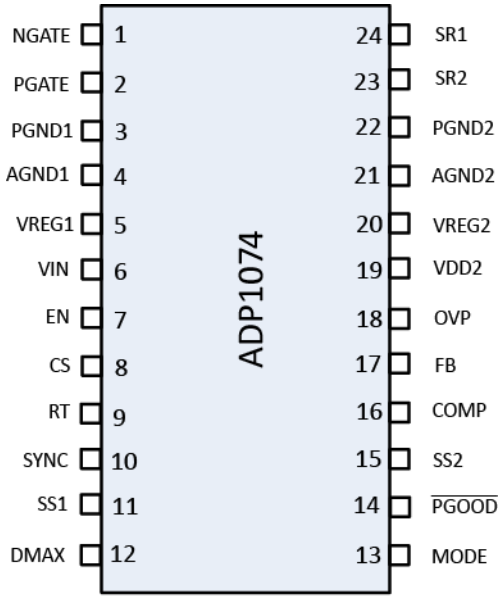

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NGATE	Driver output for main power MOSFET on the primary side. Multiple function pin. Connect a resistor from NGATE to PGND1 to setup the predetermined dead time between PGATE and SR2.
2	PGATE	Driver for the active clamp MOSFET of the forward topology. This pin is referenced to PGND1.
3	PGND1	Power ground on primary side. Star connect this pin to AGND1.
4	AGND1	Analog ground on primary. Star connect this pin to PGND1. Use this pin to differentially sense the primary current sensed with the sense resistor between the CS and AGND1 pins.
5	VREG1	8 V output for MOSFET drivers. Connect 1uF or greater at this pin. It is recommended to not put an external load on this pin in any way. This pin is referenced to PGND1.
6	VIN	Input voltage. Connect a 4.7µF capacitor at this pin. The size of this capacitor can be reduced if the input voltage to this pin is guaranteed to be stable. This pin is referenced to PGND1.
7	EN	Precision enable input. The controller is enabled when the voltage at EN pin is above the EN threshold voltage. Soft stop is enabled when EN drops below the EN threshold voltage. This pin also has a programmable EN hysteresis. This pin is referenced to AGND1.
8	CS	Input current sensing. This pin senses the input pulse width modulated current. Place a current sense resistor between the source terminal of the power MOSFET and PGND1. This current sense resistor sets up the input current limit. This pin is also used for external slope compensator. Connect a resistor from CS to the current sense resistor to generate a voltage ramp for the slope compensation. This pin is referenced to AGND1. It is recommended to connect a 33-100pF capacitor at this pin which acts as an RC filter along with the slope compensation resistor.
9	RT	Connect two resistors in series that sum up to the appropriate resistor from RT to AGND1 to set the switching frequency. Also see DMAX pin. See RT and duty cycle section for formula.
10	SYNC	Connect an external clock to the SYNC pin to synchronize the internal oscillator to this external clock frequency. Connect SYNC to AGND1 if this feature is not used. It is recommended that the SYNC frequency be within 10% of the frequency set by the RT pin.
11	SS1	Connect a capacitor at this pin to set up the open loop soft start time. This pin is referenced to AGND1.
12	DMAX	Maximum duty cycle control. Connect DMAX to the center tap of the resistor divider at the RT pin to setup the maximum duty cycle. See RT and duty cycle section for formula.
13	MODE	Light load mode setting. Connect MODE to AGND2 to disable discontinuous conduction mode (DCM) operation, or to a high logic (2.5 V or higher such as VREG2 pin) to force a LLM operation, or to a resistor to setup a fixed light load mode (LLM) threshold voltage.
14	$\overline{\text{PGOOD}}$	Power Good bar. Open drain output. Connect a pull-up resistor from $\overline{\text{PGOOD}}$ to VREG2.
15	SS2	Soft start on secondary. Connect a capacitor from SS2 to AGND2 to setup the soft start time on the secondary.
16	COMP	Compensation node on the secondary. This pin is the output of the gm amplifier. This pin is referenced to AGND2.

Pin No.	Mnemonic	Description
17	FB	Feedback node on the secondary. Set up the resistor divider from the output voltage such that the nominal voltage when the power supply is in regulation is 1.2 Volts. This pin is referenced to AGND2.
18	OVP	Output overvoltage protection (OVP). The OVP threshold is set at 1.36 Volts. Connect a resistive divider from OVP to the output and AGND2.
19	VDD2	Input supply on the secondary. Connect VDD2 to the output voltage for a self-driven configuration. Connect a 4.7µF capacitor from this pin to AGND2. The size of this capacitor can be reduced if the input voltage to this pin is guaranteed to be stable.
20	VREG2	5V regulated LDO output for internal bias and powering the drivers of the synchronous rectifiers. Do not use this pin as a reference or load this pin in any way. Connect a 1µF capacitor from this pin to AGND2.
21	AGND2	Analog ground on secondary. Star connect this pin to PGND2. Use this pin for differential sensing of the output voltage between the FB pin and AGND2.
22	PGND2	Power ground on secondary. Star connect this pin to AGND2.
23	SR2	MOSFET driver output for the synchronous rectifier MOSFET. This PWM controls the free-wheeling switch.
24	SR1	MOSFET driver output for the synchronous rectifier MOSFET. This PWM is in phase with NGATE.

SIMPLIFIED BLOCK DIAGRAM

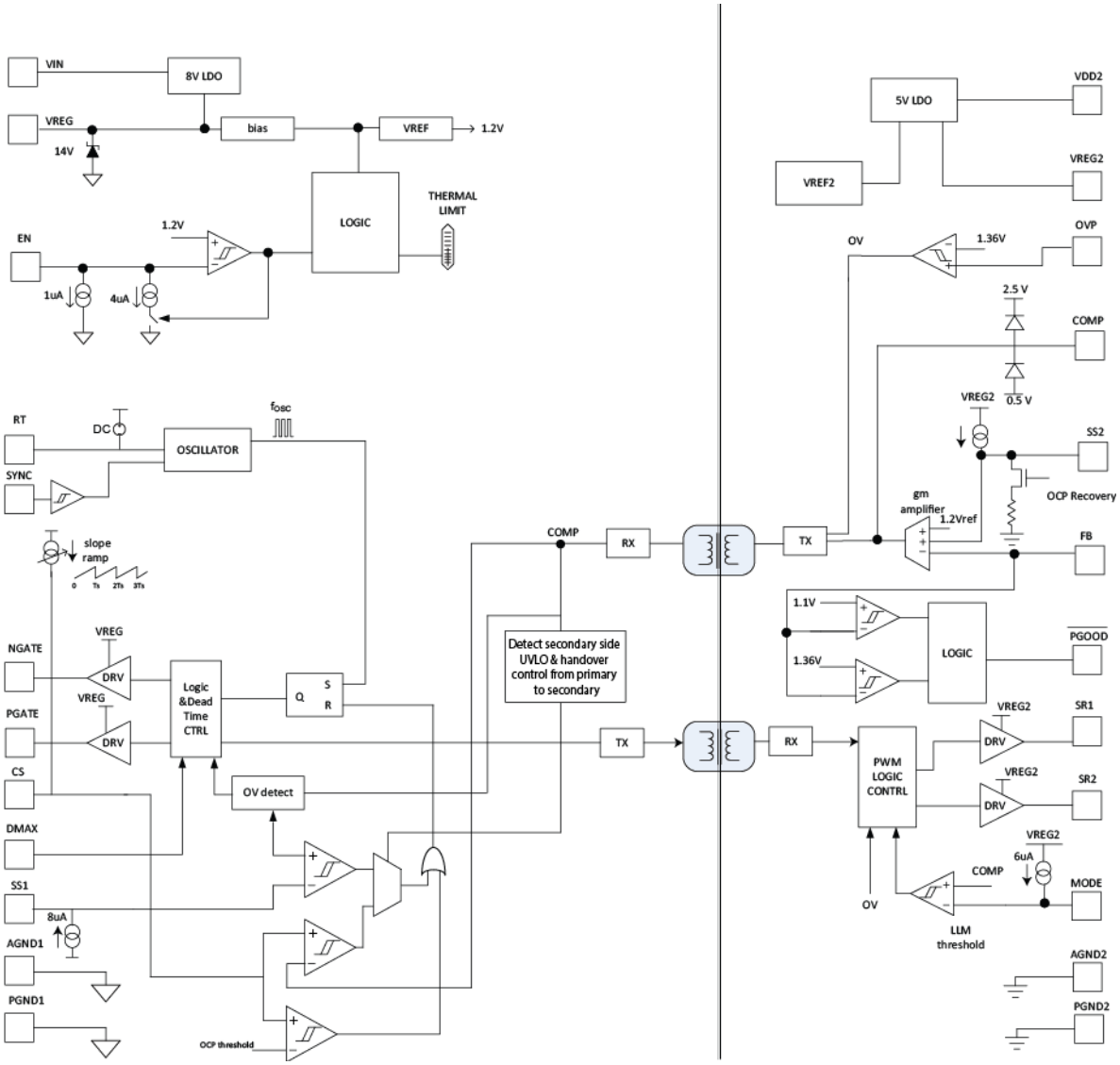

Figure 4. Simplified Block Diagram

APPLICATIONS INFORMATION

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADP1074.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 5 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The ADP1074.insulation lifetime depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 5, Figure 6, and Figure 7 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products yet meets the 50-year operating lifetime recommended by Analog Devices for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. Treat any cross-insulation voltage waveform that does not conform to Figure 6 or Figure 7 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 5.

Note that the voltage presented in Figure 6 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

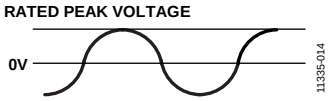

Figure 5. Bipolar AC Waveform

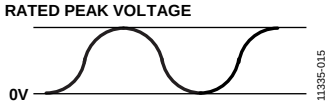

Figure 6. Unipolar AC Waveform

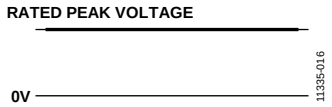

Figure 7. DC Waveform

OUTLINE DIMENSIONS

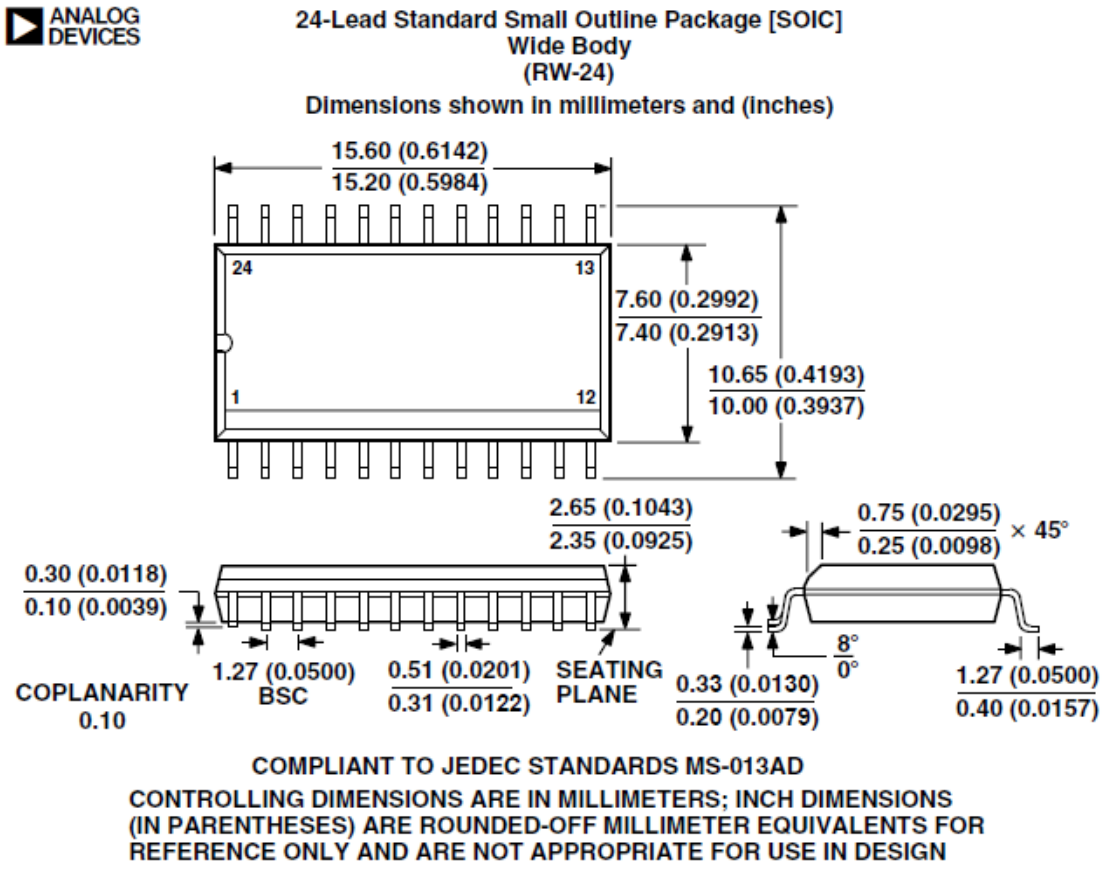

Figure 8. 24-Lead SOIC Wide Body Package