Precision Analog Microcontroller
ARM7TDMI MCU with 12-Bit ADC and DDS DAC

Silicon Anomaly

ADuC7128/ADuC7129

This anomaly list describes the known bugs, anomalies and workarounds for the ADuC7128/ADuC7129 MicroConverter®. The anomalies listed apply to all ADuC7128/ADuC7129 packaged material branded as follows:

First Line ADuC7128 or ADuC7129
Second Line BCPZ126

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7128/ADuC7129 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded ADuC7128 BCPZ126 or ADuC7129 BCPZ126	Release	Rev. 0	2

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

FUNCTIONALITY ISSUES

Table 1. ADC Conversion Start Mode [er001]

Background	ADCCON[2:0] allow the user to select one of the following seven ADC conversion start modes of operation: • External Pin **CONVST** triggered ADC conversion. • Timer1 overflow. • Timer0 overflow. • Single software conversion. • Continuous software conversion. • PLA triggered ADC conversion. • PWM triggered ADC conversion.
Issue	The active low, external pin (P0.4) triggered conversion is always active, even if it is not selected via ADCCON[2:0]. This is the case if the function of P0.4 is configured as a CONVST input or if P0.4 is configured as any other function, for example, MS1, PLAO[1], or GPIO. This means that if a falling edge is seen on P0.4 and ADCCON[7] is enabled, a single ADC conversion is triggered. If an ADC conversion cycle is already in progress, this conversion stops, and a new ADC conversion cycle begins in response to a falling edge on P0.4.
Workaround	Pending.
Related Issues	ADCCON[7], the ADC enable conversion mode bit, is fully functional, allowing the user to disable any of the active ADC conversion modes except continuous conversion (see the ADuC7128/ADuC7129 data sheet).

Table 2. I²C® Slave Not Releasing the Bus [er002]

Background	During a read from the master to the slave, if the FIFO of the slave is empty, the slave should NACK the request from the master. Then, it should release the bus, allowing the master to generate a stop condition.
Issue	Following the generation of a NACK, the ADuC7128/ADuC7129 may not release the bus due to the generation of a FIFO transmit empty interrupt.
Workaround	Following the generation of a transmit FIFO empty interrupt, the bus can be released by any of the following: • Placing valid data in the transmit FIFO. • Placing dummy data in the transmit FIFO followed by a transmit FIFO flush. • Resetting the slave interface by disabling/enabling the slave.
Related Issues	None.

SECTION 1. ADuC7128/ADuC7129 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	ADC conversion start mode	Open
er002	I²C slave not releasing the bus	Open

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).