8 kV Peak, High Working Voltage, 150 Mbps, Dual-Channel LVDS Isolator

Preliminary Technical Data

ADN4711

FEATURES

- 8000 V peak dual channel LVDS isolator
- LVDS compliant (TIA/EIA-644-A) over full operating range
- Any data rate up to 150 Mbps with low jitter
  - 5.3 ns maximum propagation delay
  - 330 ps maximum peak-to-peak jitter at 150 Mbps
  - 270 ps maximum pulse skew
  - 1 ns maximum channel-to-channel skew across parts
- 2.5 V or 3.3 V supplies
- -75 dBc power supply ripple rejection & glitch immunity
- ±8 kV IEC 61000-4-2 ESD protection across isolation
- High common-mode transient immunity: >25 kV/µs
- Low radiated emissions for passing EN55022 Class A with
  - 150 Mbps PRBS or 75 MHz clock
- Safety and regulatory approvals
  - UL (pending): 5700 V rms for 1 minute per UL 1577
  - VDE certificate of conformity, VDE 0884-11 (pending)
    - V_{IORM} = 1250 V peak reinforced
- Fail-safe output high for open and short/terminated inputs
- Operating temperature range: −40°C to +105°C
- 20-lead SOIC-IC with 8 mm creepage/clearance

APPLICATIONS

- Motor Control Safety Isolation
- Analog front end (AFE) isolation
- Data-plane isolation
- Isolated high-speed clock and data links

FUNCTIONAL BLOCK DIAGRAM

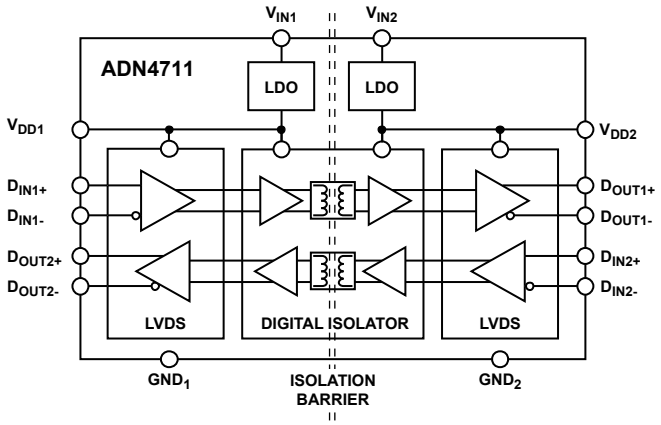

Figure 1. Dual-channel, transmit and receive

GENERAL DESCRIPTION

The ADN4711 is a signal isolated, low voltage differential signaling (LVDS) buffers that operates at up to 150 Mbps with very low jitter (<5% unit interval).

The ADN4711 comprises TIA/EIA-644-A compliant LVDS drivers and receivers integrated with iCoupler technology, enhanced for high-speed operation and for high working voltages of 1250Vpk. This allows drop-in galvanic isolation of an LVDS signal chain for high-bandwidth communication across an electrical safety isolation barrier.

The LVDS receivers on ADN4711 includes a failsafe mechanism to ensure a logic 1 on the corresponding LVDS driver output when the inputs are floating, short circuit or not driven but terminated.

For high-speed operation with low jitter, the LVDS and isolator circuits rely on a 2.5V supply. An integrated on-chip LDO can provide the required 2.5V from an external 3.3V power supply. The ADN4711 is fully specified over a wide industrial temperature range and is available in 20-lead wide-body SOIC-IC package with increased creepage guaranteeing 8 mm.

Rev. PrC

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Last Content Update: 02/23/2017

COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- ADN4711: 8 kV Peak, High Working Voltage, 150 Mbps, Dual-Channel LVDS Isolator Preliminary Data Sheet

DESIGN RESOURCES

- ADN4711 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADN4711 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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DOCUMENT FEEDBACK

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SPECIFICATIONS

For all minimum/maximum specifications, $V_{DD1} = V_{DD2} = 2.375$ V to 2.625 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. For all typical specifications, $V_{DD1} = V_{DD2} = 2.5$ V, $T_A = 25°C$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
INPUTS (RECEIVERS)						
Input Threshold						See Figure 5, Table 2
High	V_{TH}			100	mV	
Low	V_{TL}	−100			mV	
Differential Input Voltage	$\|V_{ID}\|$	100			mV	See Figure 5, Table 2
Input Common-Mode Voltage	V_{IC}	$0.5\|V_{ID}\|$		$2.4 - 0.5\|V_{ID}\|$	V	See Figure 5, Table 2
Input Current	I_{IH}, I_{IL}	−5		+5	µA	$V_I = V_{DD}$ or $V_I = 0$ V, $V_{DD} = 2.5$ V or 0 V
Differential Input Capacitance[1]	$C_{INx\pm}$		2		pF	$D_{INx\pm} = 0.4 \sin(30 \times 10^6 \pi t)$ V + 0.5 V, other input = 1.2 V
OUTPUTS (DRIVERS)						
Differential Output Voltage	$\|V_{OD}\|$	250	310	450	mV	See Figure 3, Figure 4, $R_L = 100\ \Omega$
V_{OD} Magnitude Change	$\|\Delta V_{OD}\|$			50	mV	See Figure 3, Figure 4, $R_L = 100\ \Omega$
Offset Voltage	V_{OS}	1.125	1.17	1.375	V	See Figure 3, $R_L = 100\ \Omega$
V_{OS} Magnitude Change	ΔV_{OS}			50	mV	See Figure 3, $R_L = 100\ \Omega$
V_{OS} Peak to Peak[1]	$V_{OS(PP)}$			150	mV	See Figure 3, $R_L = 100\ \Omega$
Output Short Circuit Current	I_{OS}			−20	mA	$D_{OUTx\pm} = 0$ V
				12	mA	$\|V_{OD}\| = 0$ V
Differential Output Capacitance[1]	$C_{OUTx\pm}$		5		pF	$D_{OUTx\pm} = 0.4 \sin(30 \times 10^6 \pi t)$ V + 0.5 V, other input = 1.2 V, V_{DD1} or $V_{DD2} = 0$ V
POWER SUPPLY						
Supply Current	I_{DD1}, I_{IN1}, I_{DD2} or I_{IN2}			TBD	mA	No output load, inputs with 100 Ω, no applied $\|V_{ID}\|$
				80	mA	All outputs loaded, $R_L = 100\ \Omega$, f = 75 MHz
				70	mA	All outputs loaded, $R_L = 100\ \Omega$, f = 75 MHz, $T_A \geq 85°C$
LDO Input Range	V_{IN1}/V_{IN2}	3.0	3.3	3.6	V	No external supply on V_{DD1} or V_{DD2}
LDO Output Range	V_{DD1}/V_{DD2}	2.375	2.5	2.625		
Power Supply Ripple Rejection, Phase Spur Level	PSRR		-75		dBc	Phase spur level on $D_{OUTx\pm}$ with 75 MHz clock on $D_{INx\pm}$ and applied ripple of 100 kHz, 100 mV p-p on a 2.5 V supply to V_{DD1} or V_{DD2}
COMMON-MODE TRANSIENT IMMUNITY[2]	|CM|	TBC	50		kV/µs	$V_{CM} = 1000$ V, transient magnitude = 800 V

[1] These specifications are guaranteed by design and characterization.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining any D_{OUTx+}/D_{OUTx-} pin in the same state as the corresponding D_{INx+}/D_{INx-} pin (no change on output), or producing the expected transition on any D_{OUTx+}/D_{OUTx-} pin if the applied common-mode transient edge is coincident with a data transition on the corresponding D_{INx+}/D_{INx-} pin. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

RECEIVER INPUT THRESHOLD TEST VOLTAGES

Table 2. Test Voltages for Receiver Operation

Applied Voltages		Input Voltage, Differential	Input Voltage, Common Mode	Driver Output
V_{IN+} (V)	V_{IN-} (V)	V_{ID} (V)	V_{IC} (V)	V_{OD} (V)
+1.25	+1.15	+0.1	+1.2	>+250 mV
+1.15	+1.25	-0.1	+1.2	<-250 mV
+2.4	+2.3	+0.1	+2.35	>+250 mV
+2.3	+2.4	-0.1	+2.35	<-250 mV
+0.1	0	+0.1	+0.05	>+250 mV
0	+0.1	-0.1	+0.05	<-250 mV
+1.5	+0.9	+0.6	+1.2	>+250 mV
+0.9	+1.5	-0.6	+1.2	<-250 mV
+2.4	+1.8	+0.6	+2.1	>+250 mV
+1.8	+2.4	-0.6	+2.1	<-250 mV
+0.6	0	+0.6	+0.3	>+250 mV
0	+0.6	-0.6	+0.3	<-250 mV

TIMING SPECIFICATIONS

V_{DD1}, V_{DD2} = 2.375 V to 2.625 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted. All typicals, $V_{DD1} = V_{DD2}$ = 2.5V, T_A = 25°C.

Table 3.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Conditions/Comments
PROPAGATION DELAY	t_{PLH}, t_{PHL}		4	5.3	ns	See Figure 6, From any D_{IN+}/D_{IN-} to D_{OUT+}/D_{OUT-}
SKEW						See Figure 6, Across all D_{OUT+}/D_{OUT-}
Duty Cycle[2]	$t_{SK(D)}$			250	ps	
Channel-to-Channel[3]	$t_{SK(CH)}$		TBD	TBD	ps	
Part-to-Part[4]	$t_{SK(PP)}$			1	ns	
JITTER[5]						See Figure 6, From any D_{IN+}/D_{IN-} to D_{OUT+}/D_{OUT-}
Random Jitter, RMS[6] (1σ)	$t_{RJ(RMS)}$		3	TBD	ps rms	75 MHz clock input
Deterministic Jitter[7, 8]	$t_{DJ(PP)}$		TBD	TBD	ps	150 Mbps 2^{23} – 1 PRBS
With Crosstalk	$t_{DJC(PP)}$		TBD			150 Mbps 2^{23} – 1 PRBS
Total Jitter at BER 1 × 10^{-12}	$t_{TJ(PP)}$		TBD	330	ps	75 MHz/150 Mbps 2^{23} – 1 PRBS[9]
RISE/FALL TIME	t_r, t_f			350	ps	See Figure 6, any D_{OUTx+}/D_{OUTx-}, 20% to 80%, R_L = 100 Ω, C_L = 5 pF
FAIL-SAFE DELAY[10]	t_{FSH}, t_{FSL}		TBD	1	µs	See Figure 6, Figure 7, Any D_{OUT+}/D_{OUT-}, R_L = 100 Ω
MAXIMUM DATA RATE		150			Mbps	

[1] These specifications are guaranteed by design and characterization.
[2] Duty cycle or pulse skew is defined as the magnitude of the maximum difference between t_{PLH} and t_{PHL} for any channel of a device, that is, $|t_{PHLx} - t_{HLPx}|$.
[3] Channel-to-channel or output skew is defined as the difference between the largest and smallest values of t_{PLHx} within a device or the difference between the largest and smallest values of T_{PHLx} within a device, whichever of the two is greater.
[4] Part-to-part output skew is defined as the difference between the largest and smallest values of t_{PLHx} across multiple devices or the difference between the largest and smallest values of t_{PHLx} across multiple devices, whichever of the two is greater.
[5] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter. V_{ID} = 400 mV p-p, $t_R = t_F$ = 0.3 ns (20% to 80%).
[6] This specification is measured over a population of ~7,000,000 edges.
[7] Peak-to-peak jitter specifications include jitter due to pulse skew ($t_{SK(D)}$).
[8] This specification is measured over a population of ~3,000,000 edges.
[9] Using the formula $t_{TJ(PP)} = 14 \times t_{RJ(RMS)} + t_{DJ(PP)}$.
[10] The fail-safe delay is the delay before $D_{OUTx\pm}$ is switched high to reflect idle input to $D_{INx\pm}$ ($|V_{ID}| < 100$ mV, open or short/terminated input condition).

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		34	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		3.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

UL (Pending)	VDE (Pending)
To be recognized Under UL 1577 Component Recognition Program[1] Single Protection, 5700 V rms Isolation Voltage	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11)[2] Reinforced insulation, 1250 V peak, V_{IOSM} = 8000 V peak

[1] In accordance with UL 1577, each ADN4711 is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-11, each ADN4711 is proof tested by applying an insulation test voltage ≥ 2344 V peak for 1 sec (partial discharge detection limit = 5 pC).

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1250	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	2344	V peak
Input to Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1875	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1500	V peak
Highest Allowable Overvoltage		V_{IOTM}	8000	V peak
Surge Isolation Voltage				
Reinforced	$V_{PEAK} = 12.8$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

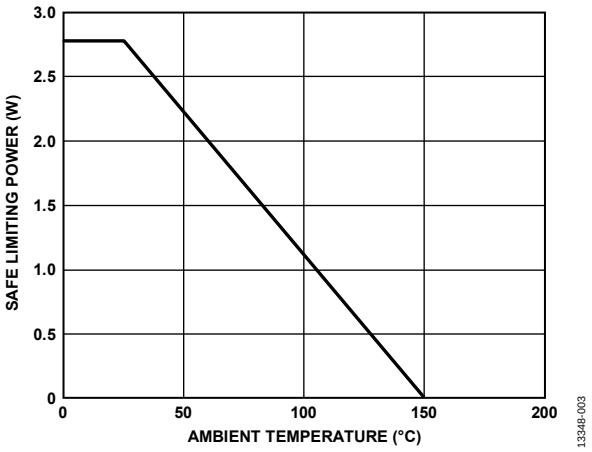

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +105°C
Supply Voltages		
Supply to LDO	V_{IN1}, V_{IN2}	3.0 V to 3.6 V
LDO bypass, V_{IN} shorted to V_{DD}	V_{DD1}, V_{DD2}	2.375 V to 2.625 V

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

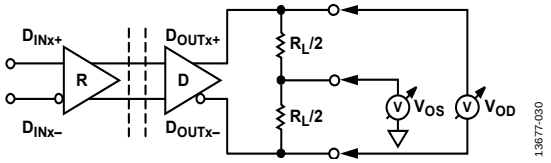

Figure 3. Driver Test Circuit

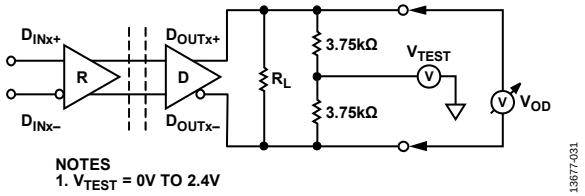

Figure 4. Driver Test Circuit (Full Load Across Common-Mode Range)

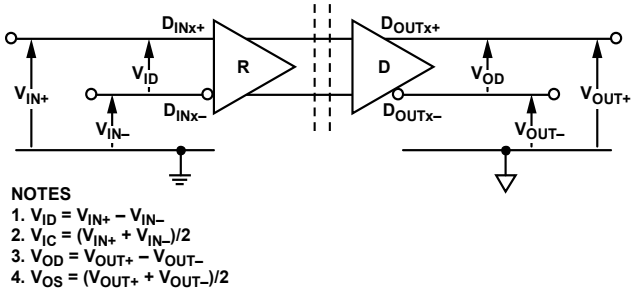

Figure 5. Voltage Definitions

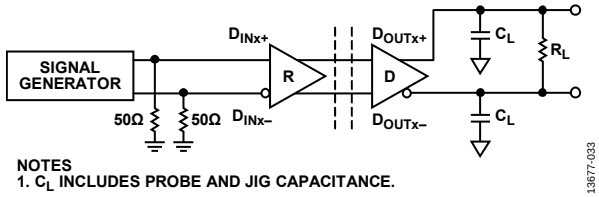

Figure 6. Timing Test Circuit

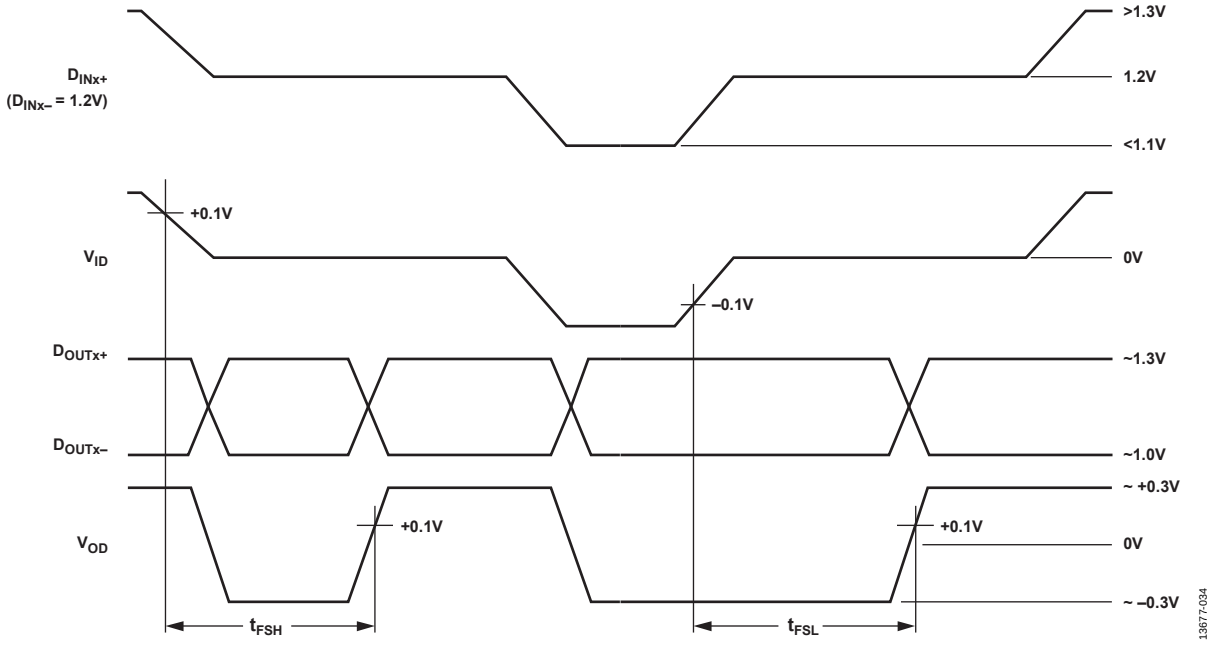

Figure 7. Fail-safe Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
V_{IN1} to GND1/ V_{IN2} to GND2	−0.3 V to +6.5 V
V_{DD1} to GND1/ V_{DD2} to GND2	−0.3 V to +2.8 V
Input Voltage (D_{IN+}, D_{IN-}) to GND	−0.3 V to 3.6 V
Output Voltage (D_{OUT+}, D_{OUT-}) to GND	−0.3 V to 3.6 V
Short-Circuit Duration (D_{OUT+}, D_{OUT-}) to GND	Continuous
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
ESD, Human Body Model (All pins to respective GND, 1.5 kΩ 100 pF)	TBD
ESD, IEC 61000-4-2 (All pins to isolated GND across isolation barrier)	8 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	θ_{JA}	Unit
20-lead SOIC-IC	45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

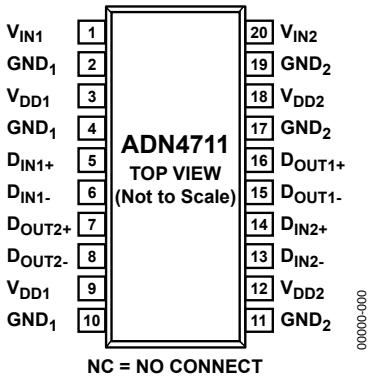

Figure 8.

Table 10. Pin Function Descriptions

ADN4711 Pin No.	Mnemonic	Description
1	V_{IN1}	Optional 3.3V power supply/LDO input for side 1, bypass to GND_1 using a 1µF capacitor. Alternatively, if using a 2.5V supply, connect V_{IN1} directly to V_{DD1}.
2, 4, 10	GND_1	Ground, Side 1.
3, 9	V_{DD1}	2.5V power supply for side 1, connect both pins externally and bypass to GND_1 with 0.1 µF capacitors. If supplying 3.3V to V_{IN1}, connect a 1µF capacitor between pin 3 and GND_1 for proper regulation of the internal LDO's 2.5V output.
5	D_{IN1+}	Noninverted Differential Input 1.
6	D_{IN1-}	Inverted Differential Input 1.
14	D_{IN2+}	Noninverted Differential Input 2.
13	D_{IN2-}	Inverted Differential Input 2.
11, 17, 19	GND_2	Ground, Side 2.
12, 18	V_{DD2}	2.5V power supply for side 2, connect both pins externally and bypass to GND_2 with 0.1 µF capacitors. If supplying 3.3V to V_{IN2}, connect a 1µF capacitor between pin 18 and GND_2 for proper regulation of the internal LDO's 2.5V output.
8	D_{OUT2-}	Inverted Differential Output 2.
7	D_{OUT2+}	Noninverted Differential Output 2.
15	D_{OUT1-}	Inverted Differential Output 1.
16	D_{OUT1+}	Noninverted Differential Output 1.
20	V_{IN2}	Optional 3.3V power supply/LDO input for side 2, bypass to GND_2 using a 1µF capacitor. Alternatively, if using a 2.5V supply, connect V_{IN2} directly to V_{DD2}.

THEORY OF OPERATION

The ADN4711 is an TIA/EIA-644-A LVDS compliant isolated buffer. LVDS signals applied to the inputs are transmitted on the outputs of the buffer, and galvanic isolation is integrated between the two sides of the device. This allows drop-in isolation of LVDS signal chains.

The LVDS receiver detects the differential voltage present across a termination resistor on an LVDS input. An integrated digital isolator transmits the input state across the isolation barrier, and an LVDS driver outputs the same state as the input.

With a positive differential voltage ≥100 mV across any D_{IN+}, D_{IN-}, the corresponding D_{OUT+} sources current. This flows across the connected transmission line and termination at the receiver at the far end of the bus, while D_{OUT-} sinks the return current. With a negative differential voltage ≤100 mV across any D_{IN+}, D_{IN-}, the corresponding D_{OUT+} sinks current, with D_{OUT-} sourcing the current. Table 11 shows these input/output combinations.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.1 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor (R_T). The received voltage is centered about 1.2 V. Note that because the differential voltage V_{ID} reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage magnitude $|V_{ID}|$.

TRUTH TABLE AND FAIL-SAFE RECEIVER

The LVDS standard, TIA/EIA-644-A defines normal receiver operation under two conditions, an input differential voltage of ≥+100 mV corresponding to one logic state, and a voltage of ≤–100 mV for the other logic state. Between these thresholds, standard LVDS receiver operation is undefined (it may detect either state). The ADN4711 incorporates a failsafe circuit, to ensure the LVDS outputs are in a known state (logic high) when the input state is undefined (–100 mV < V_{ID} < +100 mV), as shown in Table 11.

This input state can occur when the inputs are floating (unconnected, no termination resistor), when the inputs are shorted, and when there is no active driver connected to the inputs (but with a termination resistor). Open-circuit, short-circuit and terminated/idle bus failsafe respectively ensure a known output state for these conditions, as implemented by the ADN4711.

After the fail-safe circuit is triggered by these input states (–100 mV < V_{ID} < +100 mV), there is a delay of up to 1.2 µs before the output is guaranteed to be high (V_{OD} ≥ 250 mV). During this time, the output may transition to or stay in a logic low state (V_{OD} ≤ –250 mV).

The fail-safe circuit triggers as soon as the input differential voltage remains between +100 mV and –100 mV for some nanoseconds. This means that very slow rise and fall times on the input signal, outside typical LVDS operation (350 ps maximum t_R/t_F), can potentially trigger the fail-safe circuit on a high to low crossover.

At the minimum $|V_{ID}|$ of 100 mV for normal operation, the rise/fall time must be ≤5 ns to avoid triggering a fail-safe state. Increasing $|V_{ID}|$ to 200 mV correspondingly allows an input rise/fall time of up to 10 ns without triggering a fail-safe state. For very low speed applications where slow high to low transitions in excess of this limit are expected, using external biasing resistors is an option to introduce a minimum $|V_{ID}|$ of 100 mV (that is, the fail-safe cannot trigger).

Table 11. ADN4711 Operation

Input ($D_{INx±}$)			Output ($D_{OUTx±}$)		
Powered On	**V_{ID} (mV)**	**Logic**	**Powered On**	**V_{OD} (mV)**	**Logic**
Yes	≥100	High	Yes	≥250	High
Yes	≤–100	Low	Yes	≤–250	Low
Yes	–100 < V_{ID} < +100	Indeterminate	Yes	≥250	High
No	Don't care	Don't care	Yes	≥250	High

ISOLATION

In response to any change in the input state detected by the integrated LVDS receiver, an encoder circuit sends narrow (~1 ns) pulses to a decoder circuit using integrated transformer coils. The decoder is bi-stable and is, therefore, either set or reset by the pulses that indicate input transitions. The decoder state determines the LVDS driver output state in normal operation, and this in turn reflects the isolated LVDS buffer input state.

In the absence of input transitions for more than approximately 1 µs, a periodic set of refresh pulses, indicative of the correct input state, ensures dc correctness at the output (including the failsafe output state if applicable). This will also correct the output state within 1 µs in the event of a fault condition (e.g. common mode transient slew rate >TBC kV/µs), or set the output to the failsafe state on ADN4711 if applicable.

On power-up, the output state may initially be in the incorrect DC state if there are no input transitions. The output state will be corrected within 1 µs by the refresh pulses.

If the decoder receives no internal pulses for more than approximately 1 µs, the device assumes that the input side is unpowered or nonfunctional, in which case, the output is set to a positive differential voltage (logic high).

PCB LAYOUT

The ADN4711 can operate with high-speed LVDS signals up to 75 MHz clock, or 150 Mbps NRZ data. With such high frequencies, it is particularly important to apply best practice for LVDS trace layout and termination. A 100 Ω termination resistor should be located as close as possible to the receiver, across the D_{INx+} and D_{INx-} pins.

Controlled 50 Ω impedance traces are needed on LVDS signal lines for full signal integrity, reduced system jitter and minimizing EMI from the PCB. Trace widths, lateral distance within each pair and distance to the ground plane underneath all have to be chosen appropriately. Via fencing to PCB ground between pairs is also best practice to minimize crosstalk between adjacent pairs.

The ADN4711 passes EN55022 Class A emissions limits without any special considerations required for the isolator. Best practice for high-speed PCB design, as summarized above, should avoid any other emissions from PCBs in applications using ADN4711. Special care is still recommended for off-board connections, where switching transients from high-speed LVDS signals (and clocks in particular) may conduct onto cabling, resulting in radiated emissions. Use common mode chokes, ferrites, or other filters as appropriate at LVDS connectors, as well as cable shield or PCB ground connections to earth/chassis.

The ADN4711 requires appropriate decoupling of the V_{DD} pins with 100 nF capacitors. If the integrated LDO is not used, and a 2.5V supply is connected directly, then the appropriate V_{IN} pin should be connected to the supply as well, as shown in Figure 9.

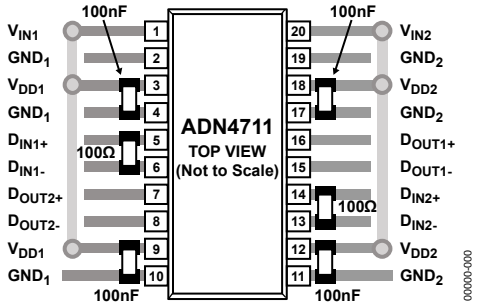

Figure 9. Required PCB Layout when not using LDO (2.5V supply)

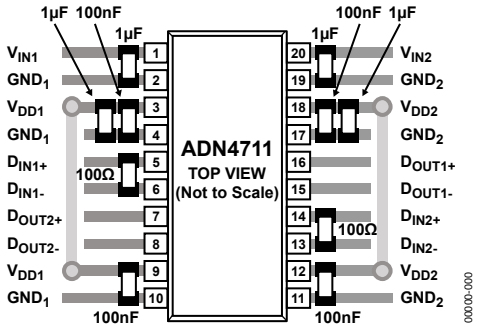

Figure 10. Required PCB Layout when using LDO (3.3V supply)

When the integrated LDO is used, bypass capacitors of 1 uF are required on the V_{IN} pins, and the nearest V_{DD} pins (LDO output), as shown in Figure 10.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the device is set by the condition in which, induced voltage in the transformer receiving coil is sufficiently large, to either falsely set or reset the decoder. The following analysis defines such conditions. The ADN4711 is examined in a 2.375 V operating condition, because it represents the most susceptible mode of operation for these products.

The pulses at the transformer output have an amplitude greater than 0.5 V. The decoder has a sensing threshold of about 0.25 V, therefore establishing a 0.25 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADN4711, and an imposed requirement that the induced voltage be, at most, 50%

of the 0.25 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 11.

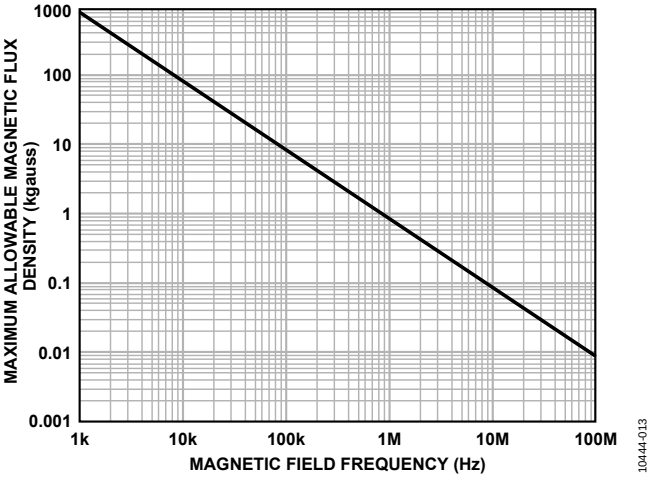

Figure 11. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.92 kgauss induces a voltage of 0.125 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst case polarity, during a transmitted pulse, it would reduce the received pulse from >0.5 V to 0.375 V. This is still higher than the 0.25 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADN4711 transformers. Figure 12 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADN4711 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component, could potentially be a concern. For the 1 MHz example noted, the user would have to place a 2.29 kA current 5 mm away from the ADN4711 to affect component operation.

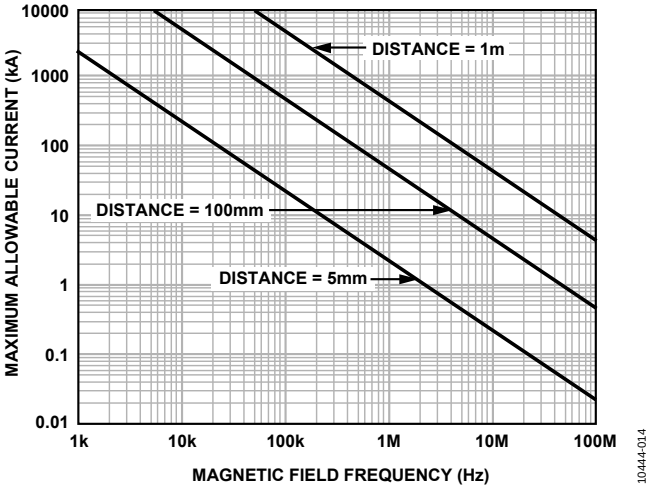

Figure 12. Maximum Allowable Current for Various Currents to ADN4711 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Avoid PCB structures that form loops.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADN4711 is presented in Table 3.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line

voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{RMS} is the total rms working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 13 and the following equations.

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\ RMS}$ = 240 V rms

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

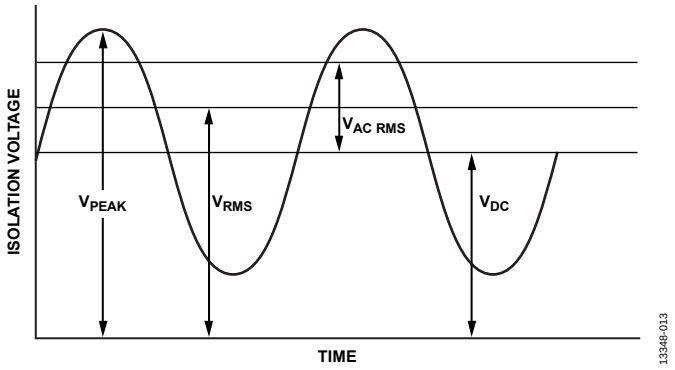

Figure 13. Critical Voltage Example

OUTLINE DIMENSIONS

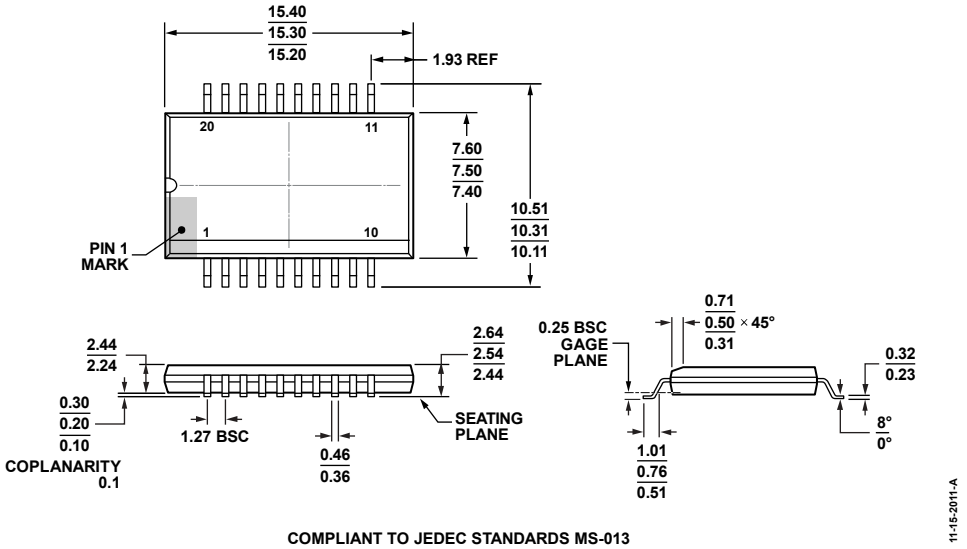

Figure 14. 20-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body (RI-20-1)
Dimensions shown in millimeters

PR15269-0-11/16(PrC)