# **Power MOSFET**

# 60 V, 1.6 m $\Omega$ , 230 A, Single N-Channel

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

## **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit	
Drain-to-Source Voltage			$V_{DSS}$	60	V	
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	V	
Continuous Drain		T <sub>C</sub> = 25°C	I <sub>D</sub>	230	Α	
Current R <sub>θJC</sub> (Notes 1, 3)	Steady State	T <sub>C</sub> = 100°C		160		
Power Dissipation		$T_C = 25^{\circ}C$	P <sub>D</sub>	170	W	
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		84		
Continuous Drain		$T_A = 25^{\circ}C$	$I_D$	35	Α	
Current R <sub>0JA</sub> (Notes 1, 2, 3)	Steady	T <sub>A</sub> = 100°C		25		
Power Dissipation	State	$T_A = 25^{\circ}C$	$P_{D}$	3.8	W	
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C		1.9		
Pulsed Drain Current	$T_A = 25$	°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	900	Α	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Source Current (Body Diode)			I <sub>S</sub>	190	Α	
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 17 A)			E <sub>AS</sub>	451	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.9	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{ heta JA}$	39	

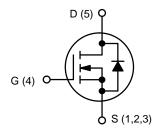
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



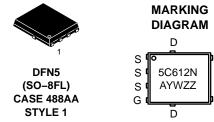
#### ON Semiconductor®

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V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
60 V	1.6 mΩ @ 10 V	230 A



**N-CHANNEL MOSFET** 



D

5C612N = Specific Device Code A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> / T <sub>J</sub>				12.8		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$ , $V_{J} = 25^{\circ}C$				10	^
		$V_{DS} = 60 \text{ V}$ $T_{J} = 125^{\circ}$	T <sub>J</sub> = 125°C			250	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2.0		4.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-9.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 50 A		1.4	1.6	mΩ
CHARGES, CAPACITANCES & GATE RE	SISTANCE						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V			4830		pF
Output Capacitance	C <sub>OSS</sub>				3180		
Reverse Transfer Capacitance	C <sub>RSS</sub>				22		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V; I <sub>D</sub> = 50 A			60.2		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				14.2		
Gate-to-Source Charge	Q <sub>GS</sub>				23.3		
Gate-to-Drain Charge	$Q_{GD}$				6.3		
Plateau Voltage	V <sub>GP</sub>				4.9		V
SWITCHING CHARACTERISTICS (Note 5	5)						
Turn-On Delay Time	t <sub>d(ON)</sub>				14.2		
Rise Time	t <sub>r</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 48 \text{ V},$ $I_{D} = 50 \text{ A}, R_{G} = 2.5 \Omega$			46.9		ns ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>				38.9		
Fall Time	t <sub>f</sub>				11.9		
DRAIN-SOURCE DIODE CHARACTERIS	STICS						
Forward Diode Voltage V <sub>SD</sub>	$V_{SD}$	V <sub>GS</sub> = 0 V,	$T_J = 25^{\circ}C$		0.81	1.0	V
		T <sub>J</sub> = 125°C		0.67		<b>1</b> '	
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dI}_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 50 \text{ A}$			82.4		ns
Charge Time	t <sub>a</sub>				40.8		
Discharge Time	t <sub>b</sub>				41.6		
Reverse Recovery Charge	$Q_{RR}$				139		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

#### TYPICAL CHARACTERISTICS

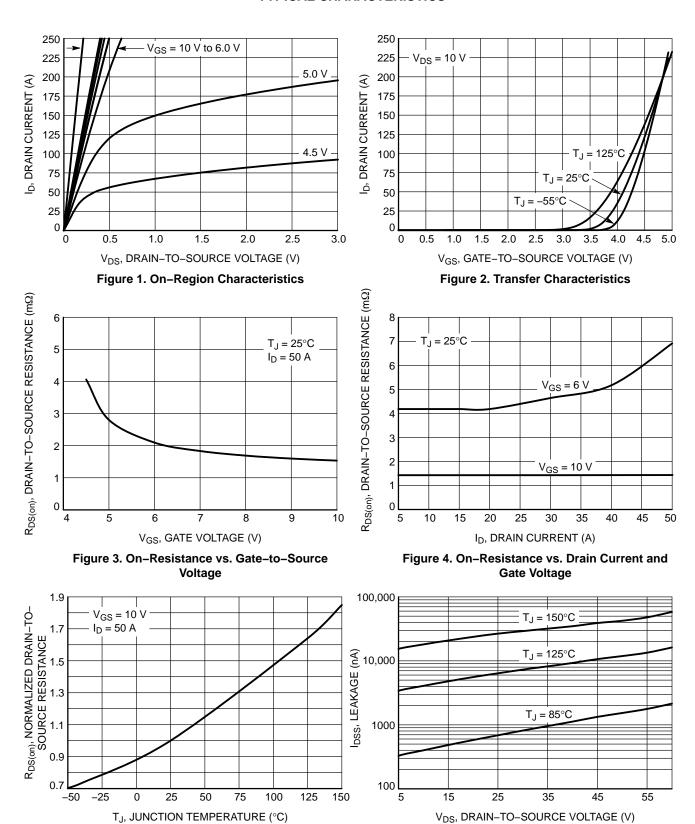


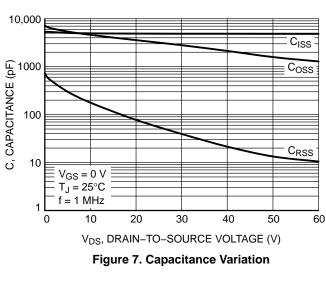
Figure 6. Drain-to-Source Leakage Current

vs. Voltage

Figure 5. On-Resistance Variation with

**Temperature** 

#### TYPICAL CHARACTERISTICS



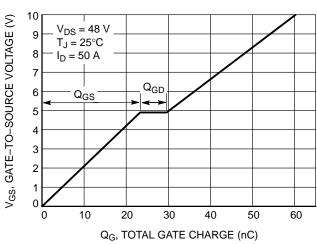


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

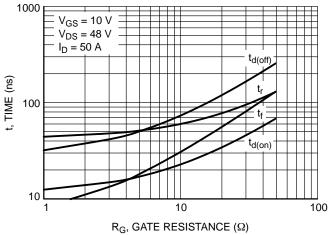


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

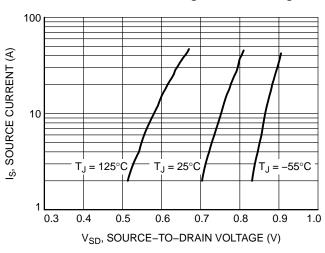


Figure 10. Diode Forward Voltage vs. Current

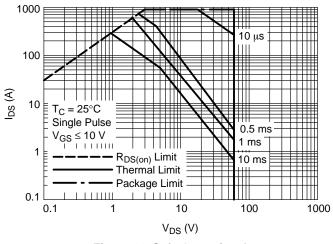


Figure 11. Safe Operating Area

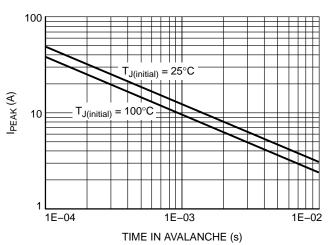


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

## **TYPICAL CHARACTERISTICS**

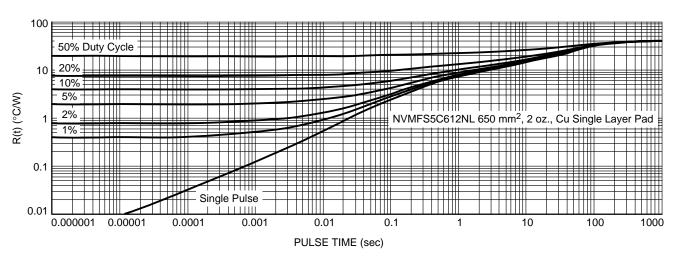


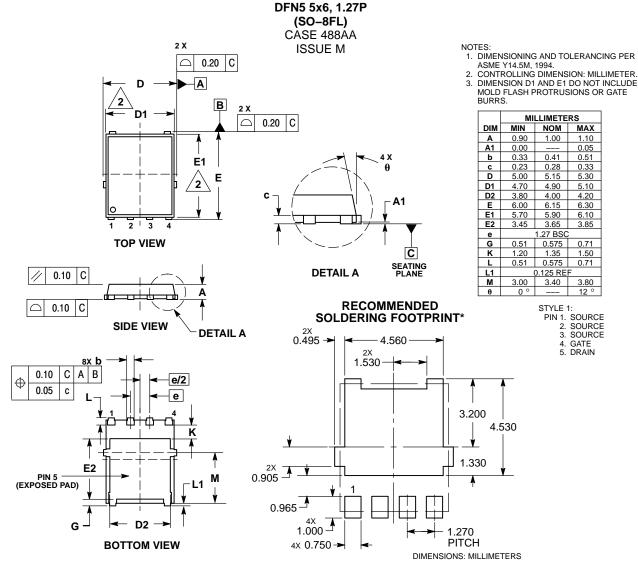
Figure 13. Thermal Characteristics

## **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTMFS5C612NT1G	5C612	DFN5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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