LC06111TMT

1-Cell Lithium-Ion Battery Protection IC with integrated Power MOSFET

ON Semiconductor®

www.onsemi.com

WDFN6 2.6x4.0, 0.65P, Dual Flag
CASE 511BZ

Overview

The LC06111TMT is a protection IC for 1−cell lithium−ion batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over−charging, over−discharging, over−current discharging and over−current charging.

A battery protection system can be made by only LC06111TMT and few external parts.

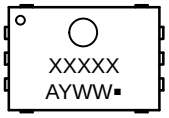
Features

- Charge−and−discharge power MOSFET are integrated at T_A = 25°C, V_{CC} = 4.5 V
  - ON resistance (total of charge and discharge) 8.4 mΩ (typ)
- Highly accurate detection voltage/current at T_A = 25°C, V_{CC} = 3.7 V
  - Over−charge detection: ±25 mV
  - Over−discharge detection: ±50 mV
  - Charge over−current detection: −1.5 A/ +0.4 A (2.0 A to 5.7 A)
    −26%/ +0.4 A (5.8 A to 8.0 A)
  - Discharge over−current detection: −1.5A/ +0.4 A (2.0 A to 5.7 A)
    −26%/ +0.4 A (5.8 A to 8.0 A)
- Delay time for detection and release (fixed internally)
- Discharge/Charge over−current detection is compensated for temperature dependency of power FET
- 0 V battery charging: “Permission”
- Auto wake−up function battery charging: “Permission”
- Over charge detection voltage: 4.1 V to 4.6 V (5 mV steps)
- Over charge release hysteresis: 0 V to 0.3 V (100 mV steps)
- Over discharge detection voltage: 2.2 V to 2.8 V (50 mV steps)
- Over discharge release hysteresis: 0 V to 0.075 V (25 mV steps)

Typical Applications

- Smart phone
- Tablet
- Wearable device

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

ORDERING INFORMATION

Device	Package	Shipping†
LC06111TMTTTG	WDFN6 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SPECIFICATIONS

Table 1. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	VCC	−0.3 to 12.0	V	Between PAC+ and VCC : R1=680 Ω
S1 − S2 voltage	VS1−S2	12.0	V	
CS terminal Input voltage	CS	VCC−12.0	V	
Charge or discharge current	BAT−, PAC−	12.0	A	
TST Input voltage	TST	−0.3 to 7	V	
Storage temperature	Tstg	−55 to +125	°C	
Current between S1 and S2(DC)	ID	12.0	A	VCC = 3.7 V
Current between S1 and S2 (continuous pulse)	IDP	40	A	Pulse Width<10μs, duty cycle<1%
Operating ambient temperature	Topr	−40 to +85	°C	At pulse current
Allowable power dissipation	Pd	450	mW	
Junction temperature	Tj	125	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum ratings represent the values which cannot be exceeded at any given time.
2. If you intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for confirmation.

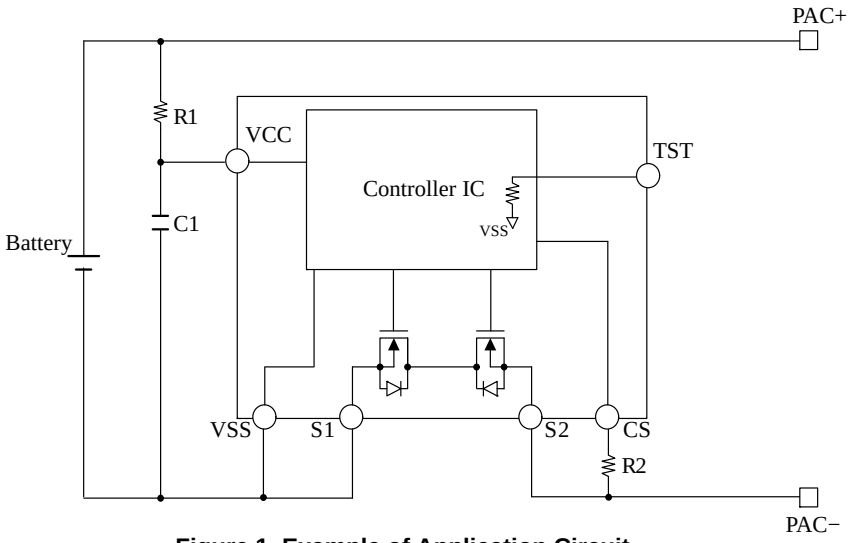


Figure 1. Example of Application Circuit

Table 2.

Components	Recommended value	Max	unit	Description
R1	680	1k	Ω	
R2	1k	2k	Ω	
C1	1μ	−	F	

3. We don't guarantee the characteristics of the circuit shown above.

ELECTRICAL CHARACTERISTICS (Note 4, 5)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Detection voltage							
Over−charge detection voltage	Vov	R1=680 Ω	25°C	Vov_set −25	Vov_set	Vov_set +25	mV
			−30 to 70°C	Vov_set −30	Vov_set	Vov_set +30	
Over−charge release voltage	Vovr	R1=680 Ω	25°C	Vovr_set −40	Vovr_set	Vovr_set +40	mV
			−30 to 70°C	Vovr_set −70	Vovr_set	Vovr_set +70	
Over−discharge detection voltage	Vuv	R1=680 Ω	25°C	Vuv_set −50	Vuv_set	Vuv_set +50	mV
			−30 to 70°C	Vuv_set −80	Vuv_set	Vuv_set +80	
Over−discharge release voltage	Vuvr	R1=680 Ω CS=0V	25°C	Vuv_set −100	Vuvr_set	Vuvr_set +100	mV
			−30 to 70°C	Vuv_set −120	Vuvr_set	Vuvr_set +120	
Over−discharge release voltage2	Vuvr2	R1=680 Ω CS=open	25°C	Vuv2_set −100	Vuvr2_set	Vuvr2_set +100	mV
			−30 to 070°C	Vuv2_set −120	Vuvr2_set	Vuvr2_set +120	
Discharge over−current detection current	Ioc	R2=1kΩ	25°C VCC=3.7V At pulse current Ioc_set=2.0A to 5.7A	Ioc_set−1.5	Ioc_set	Ioc_set +0.4	A
			25°C VCC=3.7V At pulse current Ioc_set=5.8A to 8.0A	Ioc_set*0.74			
			−30 to 70°C VCC=2.6 to 4.3 V At pulse current Ioc_set=2.0A to 5.7A	Ioc_set−2.2	Ioc_set	Ioc_set +1.1	
			−30 to 70°C VCC=2.6 to 4.3 V At pulse current Ioc_set=5.8A to 8.0A	Ioc_set*0.6			
Discharge over−current mode release voltage	Vrel_CS	R2=1 kΩ	25°C VCC=3.7V	VCC−0.95	VCC−0.65	VCC−0.35	V
			−30 to 70°C VCC=2.6 to 4.3 V	VCC−1.15	VCC−0.65	VCC−0.15	
Discharge over−current detection current2 (Short circuit)	Ioc2	R2=1 kΩ	25°C VCC=3.7 V At pulse current	Ioc2_set*0.6	Ioc2_set	Ioc2_set*1.3	A
Charge over−current detection current	Ioch	R2=1 kΩ	25°C VCC=3.7 V At pulse current Ioch_set=2.0A to 5.7 A	Ioch_set−1.5	Ioch_set	Ioch_set +0.4	A
			25°C VCC=3.7 V At pulse current Ioch_set=5.8 A to 8.0 A	Ioch_set*0.74			
			−30 to 70°C VCC=2.6 to 4.3 V At pulse current Ioch_set=2.0 A to 5.7 A	Ioch_set−2.2	Ioch_set	Ioch_set +1.1	
			−30 to 70°C VCC=2.6 to 4.3 V At pulse current Ioch_set=5.8 A to 8.0 A	Ioch_set*0.6			

ELECTRICAL CHARACTERISTICS (Note 4, 5)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Detection voltage							
Charge over−current release current	Iochr	R2=1 kΩ	25°C VCC=3.7V At pulse current Iochr_set=2.0A to 5.7A	Iochr_set−1.5	Iochr_set	Iochr_set +0.4	A
			25°C VCC=3.7V At pulse current Iochr_set=5.8 A to 8.0 A	Iochr_set*0.74			
			−30 to 70°C VCC=2.6 to 4.3V At pulse current Iochr_set=2.0 A to 5.7 A	Iochr_set−2.2	Iochr_set	Iochr_set+1.1	
			−30 to 70°C VCC=2.6 to 4.3V At pulse current Iochr_set=5.8 A to 8.0 A	Iochr_set*0.6			
Input voltage							
Operating Voltage for 0V charging	Vchg	Vcc−CS Vcc−GND=0V	25°C			1.4	V
Current consumption							
Operating current	Icc	At normal state	25°C VCC=3.7V		3	6	μA
Stand−by current	Istb	At Stand−by state	25C° VCC=2.0V			0.95	μA
		Auto wake−up =enable					
Resistance							
ON resistance 1 of integrated power MOS FET	Ron1	VCC = 3.1V I = ±2.0A	25°C	8.6	10.8	15.2	mΩ
ON resistance 2 of integrated power MOS FET	Ron2	VCC = 3.7V I = ±2.0A	25°C	7.6	9.5	12.8	mΩ
ON resistance 3 of integrated power MOS FET	Ron3	VCC = 4.0V I = ±2.0A	25°C	7.2	9.0	11.8	mΩ
ON resistance 4 of integrated power MOS FET	Ron4	VCC = 4.5V I = ±2.0A	25°C	6.6	8.4	10.6	mΩ
Internal resistance (VCC−CS)	Rcsu	VCC = 2.0V CS = 0V	25°C		300		kΩ
Internal resistance (VSS−CS)	Rcsd	VCC = 3.7V CS = 3.5V	25°C		15		kΩ

ELECTRICAL CHARACTERISTICS (Note 4, 5)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Detection and Release delay time							
Over−charge detection delay time	Tov		25°C	0.8	1	1.2	sec
			−30 to 70°C	0.6	1	1.5	
Over−charge release delay time	Tovr		25°C	12.8	16	19.2	ms
			−30 to 70°C	9.6	16	24	
Over−discharge detection delay time	Tuv		25°C	14	20	26	ms
			−30 to 70°C	12	20	30	
Over−discharge release delay time	Tuvr		25°C	0.9	1.1	1.3	ms
			−30 to 70°C	0.6	1.1	1.5	
Discharge over−current detection delay time 1	Toc1	VCC = 3.7V	25°C	9.6	12	14.4	ms
			−30 to 70°C	7.2	12	18	
Discharge over−current release delay time 1	Tocr1	VCC = 3.7V	25°C	3.2	4	4.8	ms
			−30 to 70°C	2.4	4	6	
Discharge over−current detection delay time 2 (Short circuit)	Toc2	VCC = 3.7V	25°C	280	400	560	μs
			−30 to 70°C	180	400	800	
Charge Over−current detection delay time	Toch	VCC = 3.7V	25°C	12.8	16	19.2	ms
			−30 to 70°C	9.6	16	24	
Charge Over−current release delay time	Tochr	VCC = 3.7V	25°C	3.2	4	4.8	ms
			−30 to 70°C	2.4	4	6	

4. Product parametric performance indicated in the Electrical Characteristics fir the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. The specification in this parameter and all specification at high and low temperature on this page are guaranteed by design.

RECOMMENDED BOARD LAYOUT

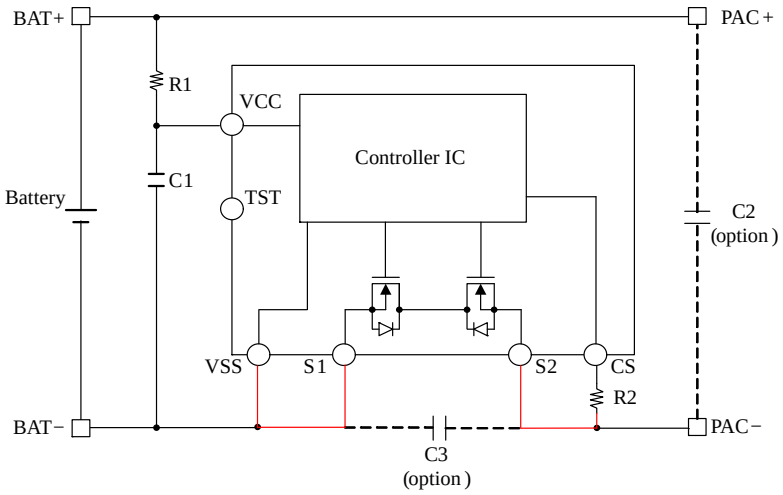


Figure 2. Board Schematic

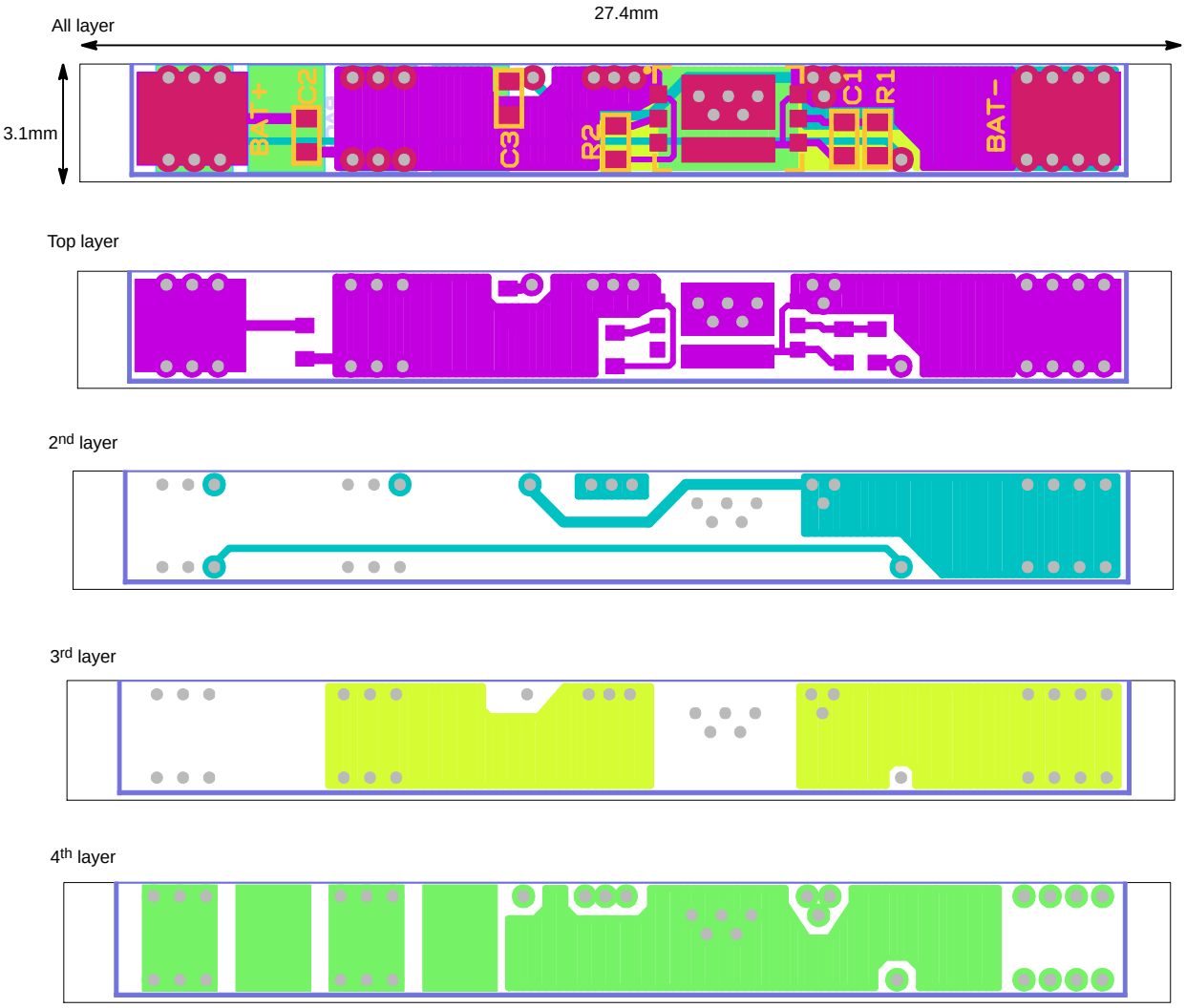


Figure 3. Board size L = 27.4 mm W = 3.1 mm H = 0.8 mm glass−epoxy 4 layers

NOTES:

1.Please connect the VSS line to a pin of S1 directly.
2.Please connect the resistance of R2 to a pin of S2 directly.

It can perform the detection of the overcurrent exactly by performing these.
It can get rid of influence of the wiring impedance caused by a severe electric current flowing through S1 and S2.
Red line of schematic is very important line.

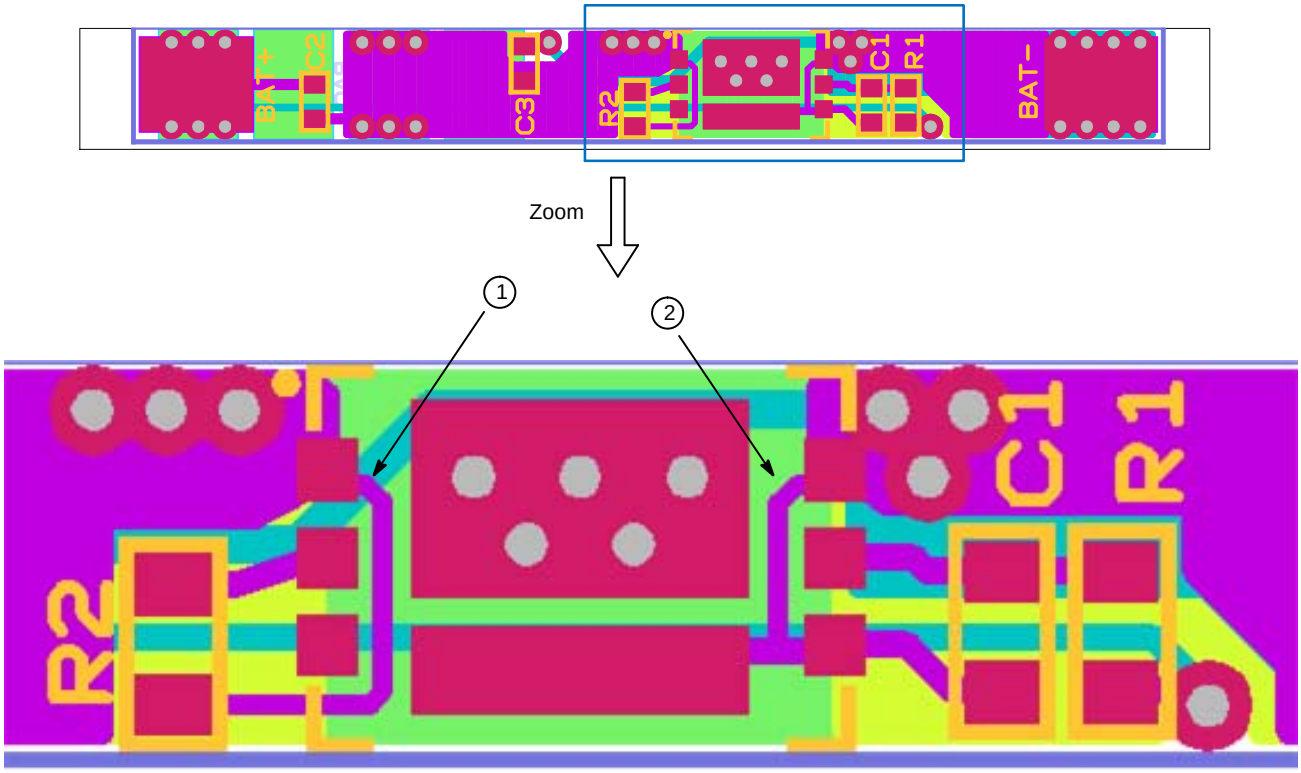


Figure 4. 4nd Layer

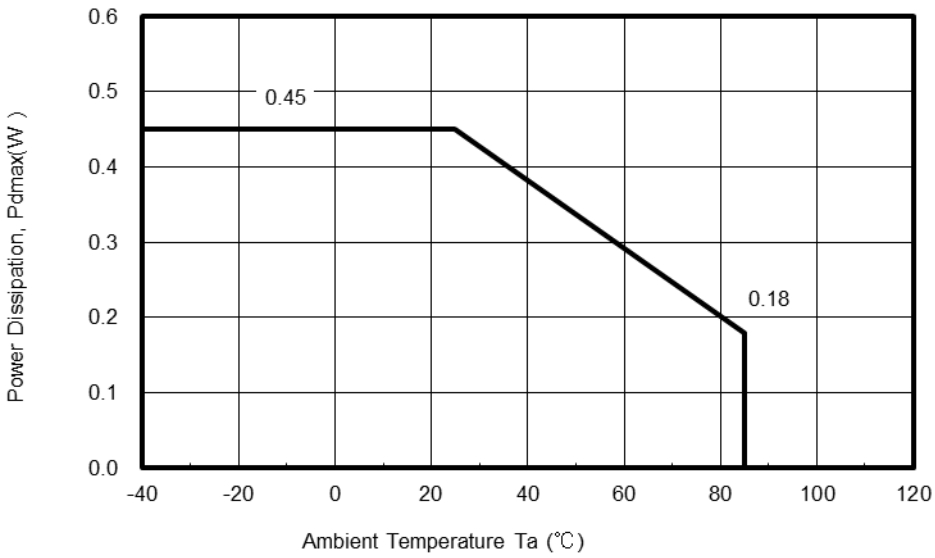


Figure 5. Pdmax−Ta graph

Table 3. PIN FUNCTIONS

Pin No.	Symbol	Pin Function	Description
1	S2	Charger minus voltage input pin	
2	CS	Charger minus voltage input pin	
3	TST	Package trimming Terminal	Connected to VSS with 100kΩ
4	VSS	Negative power Input	
5	VCC	VCC terminal	
6	S1	Negative power input	
7	Drain	Drain of FET	Exposed pad
8	Sub	IC Sub (VSS)	Exposed pad

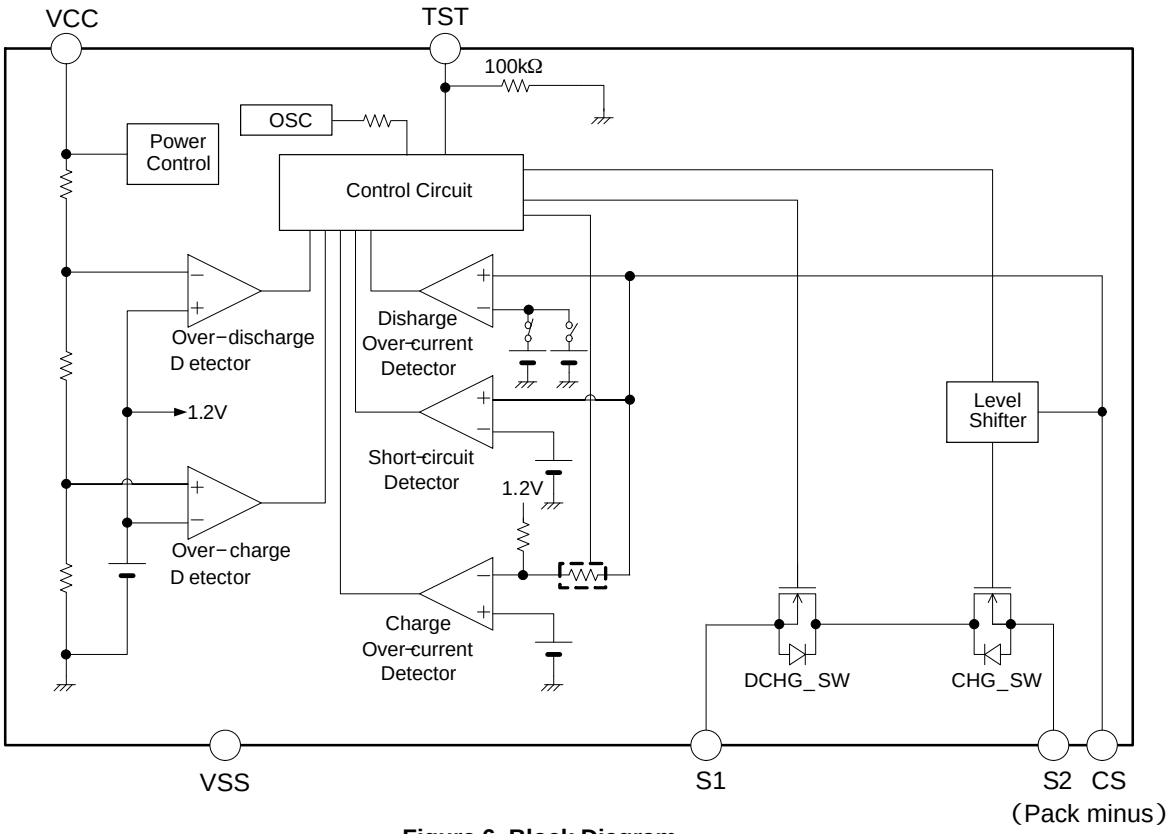


Figure 6. Block Diagram

Description of operation

Normal Mode

- LC06111TMT controls charging and discharging by detecting cell voltage (VCC) and controls S2−S1 current. In case that cell voltage is between over−discharge detection voltage (Vuv) and over−charge detection voltage (Vov), and S2−S1 current is between charge over−current detection current (Ioch) and discharge over−current detection current (Ioc), internal power MOS FETs as CHG_SW, DCHG_SW are both turned ON.

This is the normal mode, and it is possible to be charged and discharged.

Over−Charging Mode

- Internal power MOS FETCHG_SW turns off if cell voltage becomes greater than or equal to over−charge detection voltage (Vov) over the delay time of over−charging (Tov).
  This is the over−charging detection mode.
- The recovery from over−charging will be made after the following two conditions are satisfied.
  1. Charger is removed from IC.
  2. Cell voltage decreases under over−charge release voltage (Vovr) over the delay time of over−charging releasing (Tovr) due to discharging through a load.

Consequently, internal power MOS FET as CHG_SW will be turned on and normal mode will be resumed.

- In over−charging mode, discharging over−current detection is made only when CS pin increases more than discharging over−current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG_SW FET.

If CS pin voltage increases more than discharging over−current detection current 2 (Ioc2) over the delay time of discharging over−current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG_SW is turned off. (short−circuit detection mode)

After detecting short−circuit, CS pin will be pulled down to Vss by internal resistor Rcsd.

The recovery from short circuit detection in over−charging mode will be made after the following two conditions are satisfied.

- 1. Load is removed from IC.
- 2. CS pin voltage becomes less than or equal to discharging over−current release voltage(Vrel_CS) over the delay time of discharging over−current release (Tocr1) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and over−charging detection mode will be resumed.

Over−discharging mode

- If cell voltage drops lower than over−discharge detection voltage (Vuv) over the delay time of over−discharging (Tuv), discharging will be shut off, internal power FETs as DCHG_SW is turned off.

This is the over−discharging mode.

After detecting over−discharging, CS pin will be pulled up to Vcc by an internal resistor Rcsu and the bias of internal circuits will be shut off. (Stand−by mode)

In shut−down mode, operating current is suppressed under 0.95uA (max).

- The recovery from stand−by mode will be made by internal circuits biased after the following two conditions are satisfied.

1. Charger is connected.
2. VCC level rise more than Over−discharge release voltage2(Vuvr2) without charger.(Auto wake−up function)

- By continuing to be charged, if cell voltage increases more than over−discharge detection voltage (Vuvr) over the delay time of over−discharging (Tuvr), internal power MOS FETs as DCHG_SW is turned on and normal mode will be resumed.
- In over−discharge detection mode, charging over−current detection does not operate.

By continuing to be charged, charging over−current detection starts to operate after cell voltage goes up more than over−discharge release voltage (Vuvr).

Discharging over−current detection mode 1

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over−current detection current (Ioc) over the delay time of discharging over−current (Toc1).

This is the discharging over−current detection mode 1.

In discharging over−current detection mode 1, CS pin will be pulled down to Vss with internal resistor Rcsd.

- The recovery from discharging over−current detection mode will be made after the following two conditions are satisfied.

1. Load is removed from IC.

2. CS pin voltage becomes less than or equal to discharging over−current release current (Iocr) over the delay time of discharging over−current release (Tocr1) due to CS pin pulled down through Rcsd.

- Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

Discharging over−current detection mode 2 (short circuit detection)

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over−current detection current2 (Ioc2) over the delay time of discharging over−current 2 (Toc2).
  This is the short circuit detection mode.
- In short circuit detection mode, CS pin will be pulled down to Vss by internal resistor Rcsd.

The recovery from short circuit detection mode will be made after the following two conditions are satisfied.

1. Load is removed from IC.

2. CS pin voltage becomes less than or equal to discharging over−current release voltage(Vrel_CS) over the delay time of discharging over−current release (Tocr1) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

Charging over−current detection mode

- Internal power MOS FET as CHG_SW will be turned off and charging current will be shut off if CS pin voltage becomes less than or equal to charging over−current detection current (Ioch) over the delay time of charging over−current (Toch).
  This is the charging over−current detection mode.
- The recoveries from charging over−current detection mode will be made after the following two conditions are satisfied.

1. Charger is removed from IC and CS pin will increase by load connection.

2. CS pin voltage becomes greater than or equal to charging over−current release current (Iochr) over the delay time of charging over−current release (Tocrh).

Consequently, internal power MOS FET as CHG_SW will be turned on, and normal mode will be resumed.

*Internal current flows out through CS and S2 terminals.

After charger is removed, it flows through parasitic diode of CHG_SW FET.

Therefore, CS pin voltage will go up more than charging over−current release current (Iochr).

So CS pin voltage is not an indispensable condition for recovery from charging over−current detection.

Available Voltage for 0V charging

It is the function that the voltage of a connected battery can charge from the state that became 0V by self−discharge. The 0V battery charge start battery charger voltage (Vchg), it fix a gate of the charge system order FET to the VDD terminal voltage when it connect a battery charger of the above−mentioned voltage to PAC+ terminal between PAC− terminals.

Gate−source voltage of the charge control FET becomes equal to the turn−on voltage or more due to the charger voltage, the charging control FET To start charging row is turned on.

Discharge control FET is off at this time, the charge current flows through the internal parasitic diode in the discharging control FET. It is the normal state battery voltage becomes the overdischarge release voltage (Vuvr) or more.

TIMING CHART

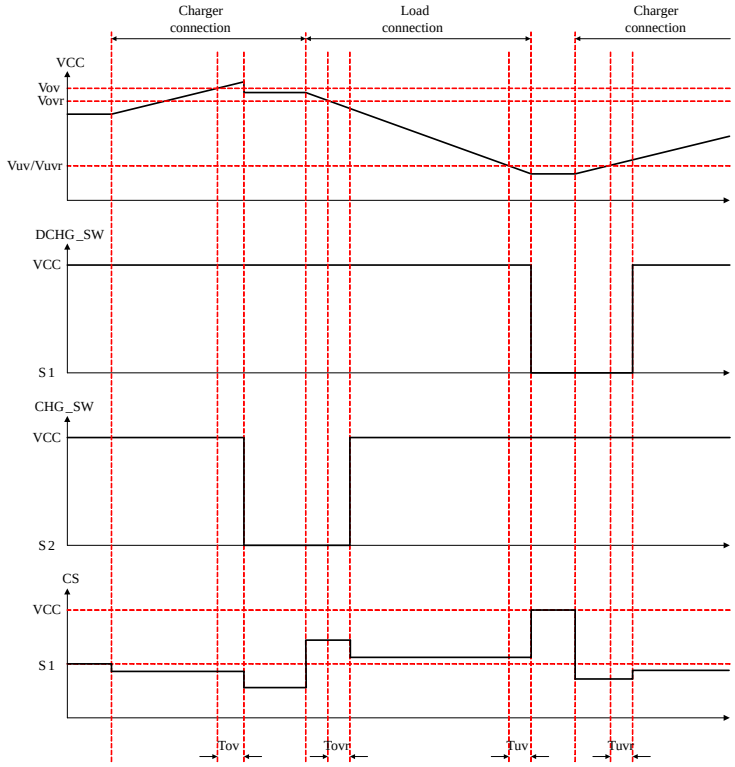


Figure 7. Over−charged detection/release, Over−discharge detection/release (Connect charger)

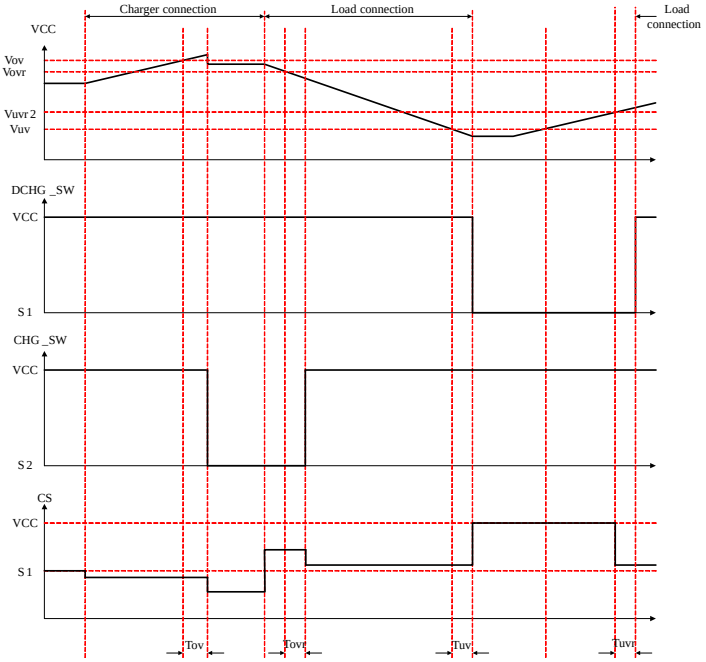


Figure 8. Over−charge detection/release, Over−discharged detection/release (Non−connect charger)

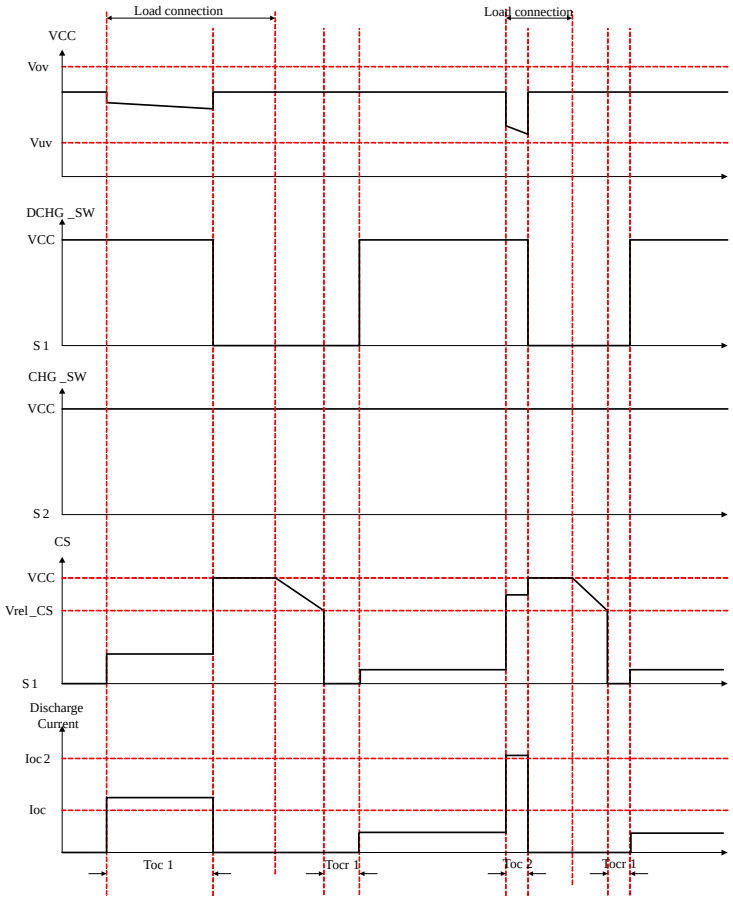


Figure 9. Discharge over−current detection1, Discharge over−current detection2 (Short circuit)

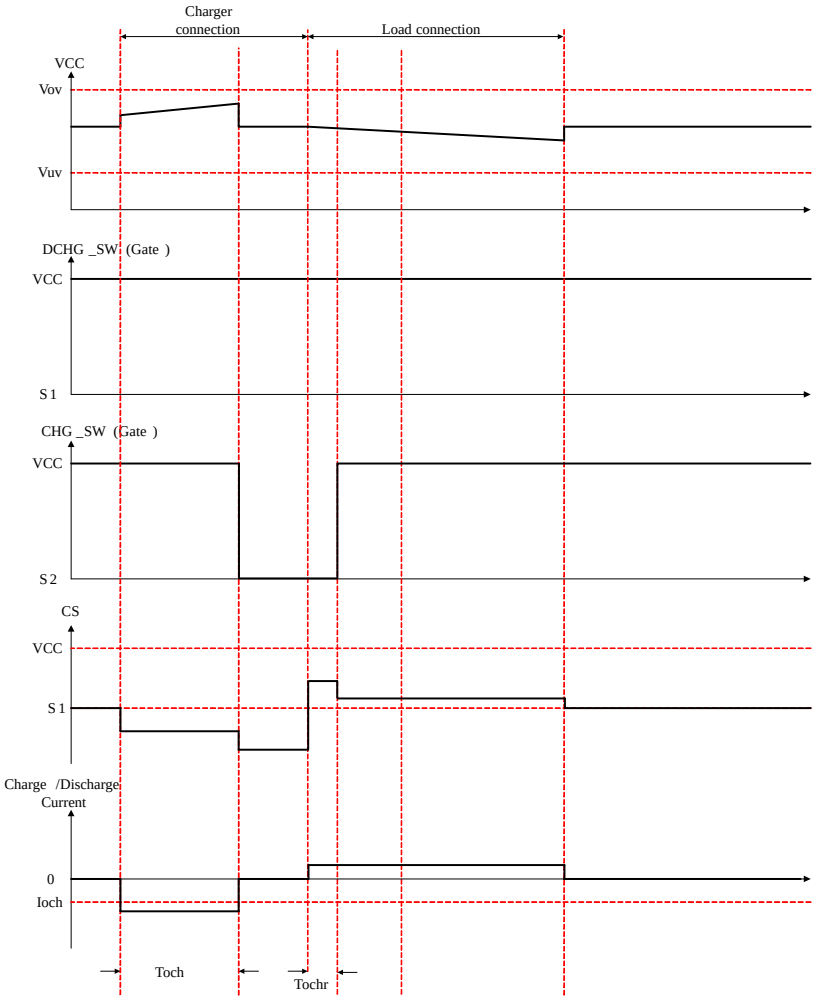
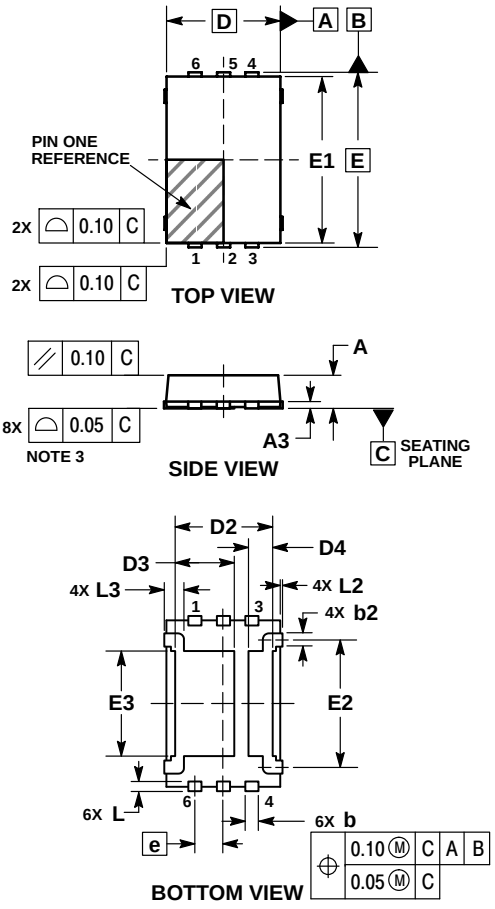


Figure 10. Charge over−current detection

LC06111TMT

PACKAGE DIMENSIONS

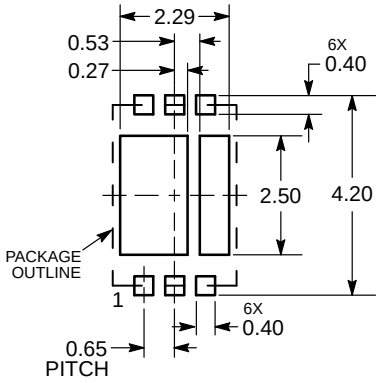
WDFN6 2.6x4.0, 0.65P, Dual Flag
CASE 511BZ
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. PROFILE TOLERANCE APPLIES TO THE EXPOSED PADS AS WELL AS THE LEADS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.80
A3	0.10	0.25
b	0.25	0.40
b2	0.15	0.30
D	2.60 BSC	
D2	2.075	2.375
D3	1.20	1.50
D4	0.40	0.70
E	4.00 BSC	
E1	3.80 REF	
E2	2.95	3.05
E3	2.25	2.55
e	0.65 BSC	
L	0.12	0.32
L2	---	0.10
L3	---	0.55

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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