



ON Semiconductor®

# NTH027N65S3F

## N-Channel SuperFET® III FRFET® MOSFET 650 V, 75 A, 27.4 mΩ

### Features

- 700 V @  $T_J = 150\text{ }^\circ\text{C}$
- Typ.  $R_{DS(on)} = 23\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 259\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 1972\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

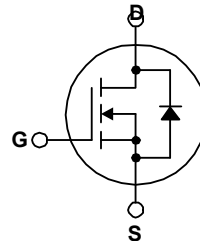
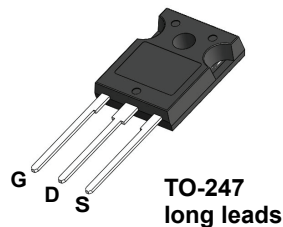
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

### Description

SuperFET® III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SuperFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SuperFET III FRFET® MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		NTH027N65S3F-F155 (Note 1)	Unit
$V_{DSS}$	Drain to Source Voltage		650	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 30$	V
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	75	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	60	
$I_{DM}$	Drain Current	- Pulsed (Note 2)	187.5	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 3)		1610	mJ
$I_{AS}$	Avalanche Current (Note 2)		15	A
$E_{AR}$	Repetitive Avalanche Energy (Note 2)		5.95	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 4)		50	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	595	W
		- Derate Above $25^\circ\text{C}$	4.76	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	NTH027N65S3F-F155	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
NTH027N65S3F-F155	NTH027N65S3F	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 150°C	700	-	-	V
$\Delta\text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 15 mA, Referenced to 25°C	-	0.61	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	-	-	10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	-	361	-	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 7.5 mA	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 35 A	-	23	27.4	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 37.5 A	-	56	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	7690	-	pF
C <sub>oss</sub>	Output Capacitance		-	200	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	1972	-	pF
C <sub>oss(er.)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	352	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 37.5 A, V <sub>GS</sub> = 10 V	-	259	-	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	72	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		(Note 5)	-	99	-
ESR	Equivalent Series Resistance	f = 1 MHz	-	1.2	-	Ω

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 37.5 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 2 Ω	-	49	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	47	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	131	-	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 5)	-	34	-

### Source-Drain Diode Characteristics

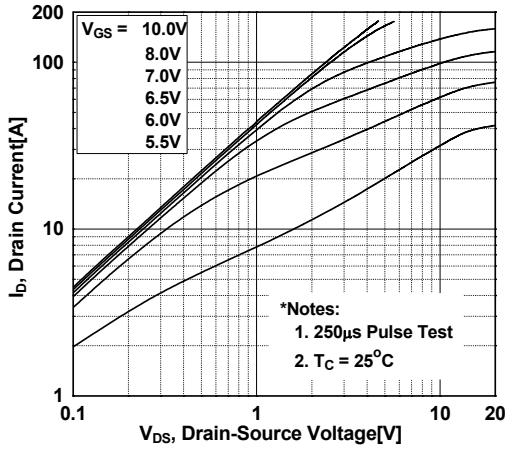
I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current	-	-	75	A	
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current	-	-	187.5	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 37.5 A	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 37.5 A, dI <sub>F</sub> /dt = 100 A/μs	-	168	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	1014	-	nC

#### Notes:

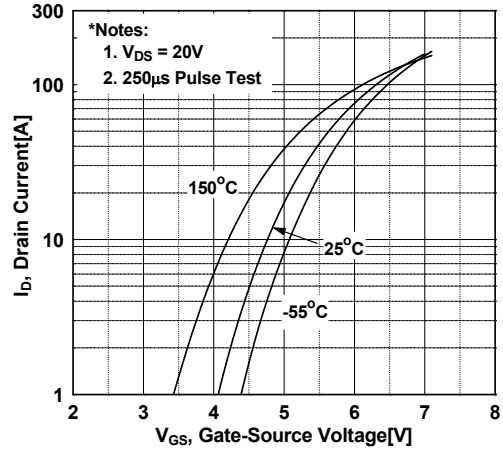
1. Due to system integration constraints between Fairchild and ON semiconductor, as of November 1, 2017 any product part number with a underscore will be replaced with a dash. This is a notification.
2. Repetitive rating: pulse-width limited by maximum junction temperature.
3. I<sub>AS</sub> = 15 A, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
4. I<sub>SD</sub> ≤ 37.5 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ 400 V, starting T<sub>J</sub> = 25°C.
5. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

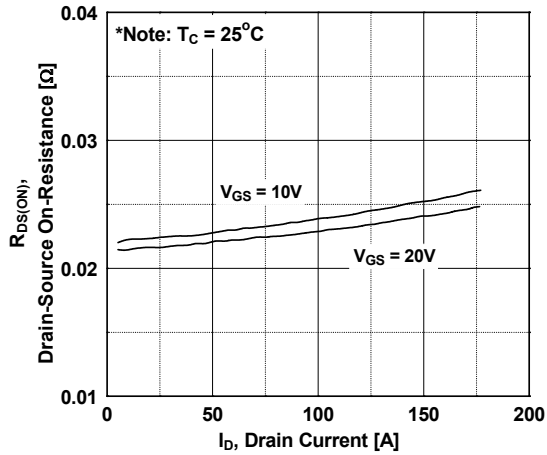
**Figure 1. On-Region Characteristics**



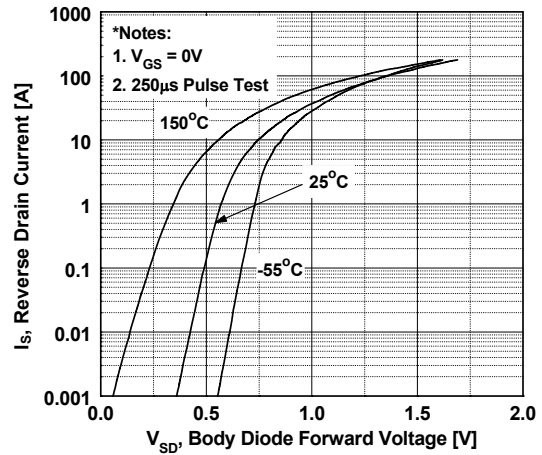
**Figure 2. Transfer Characteristics**



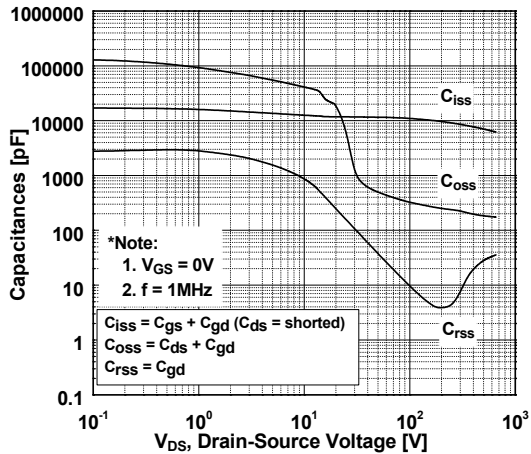
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



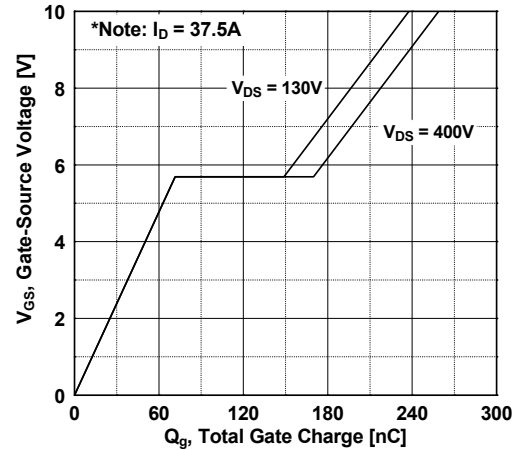
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

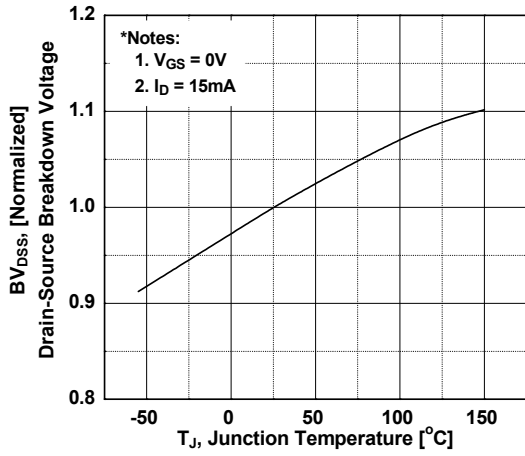


Figure 8. On-Resistance Variation vs. Temperature

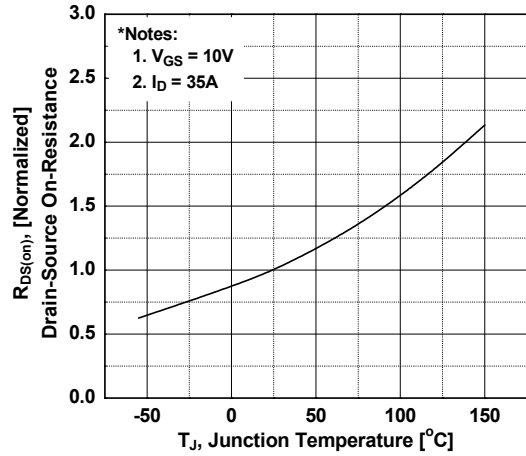


Figure 9. Maximum Safe Operating Area

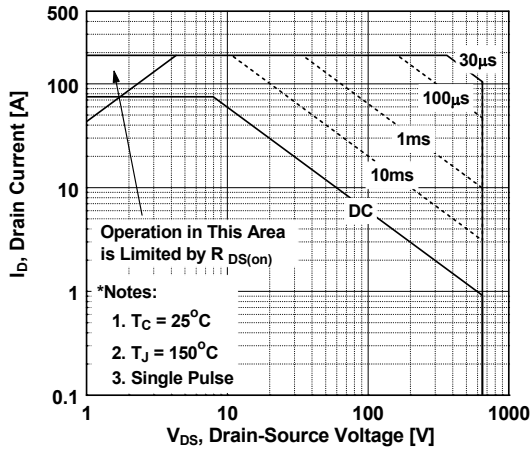


Figure 10. Maximum Drain Current vs. Case Temperature

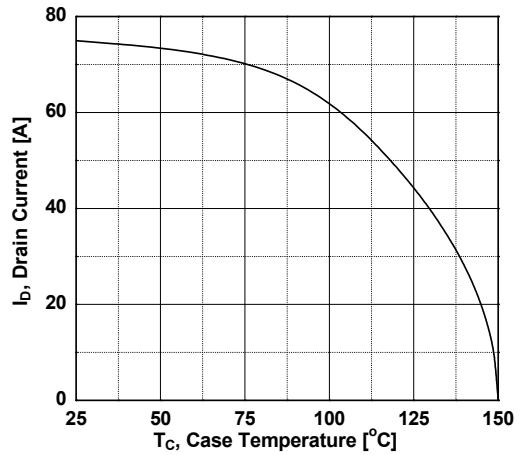
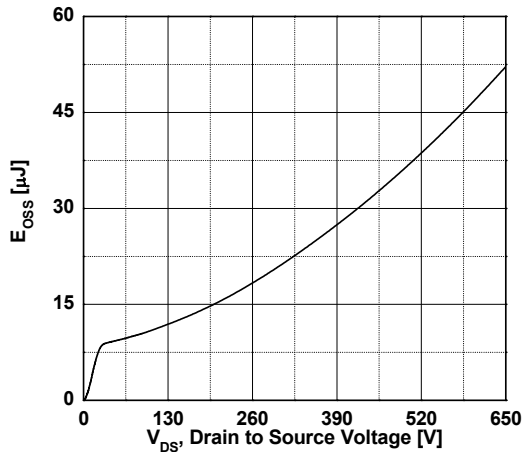
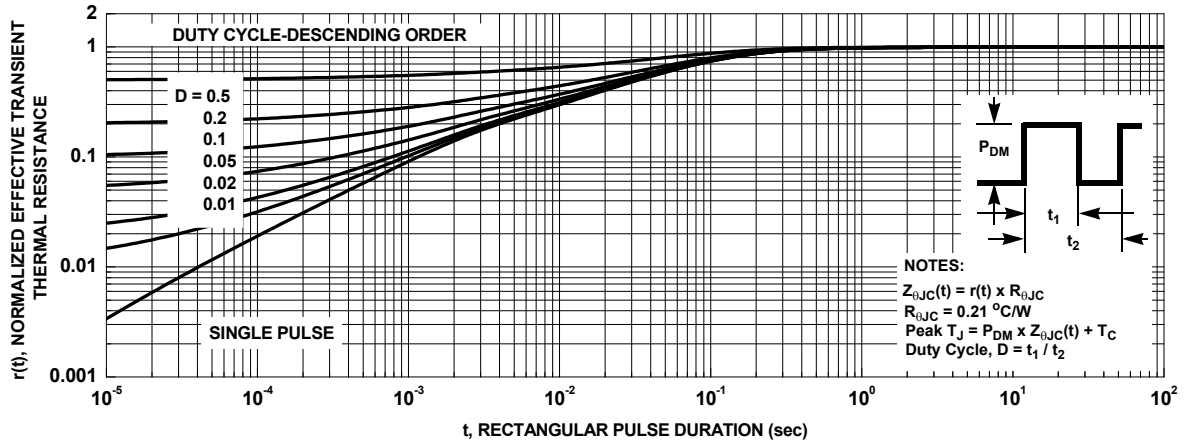


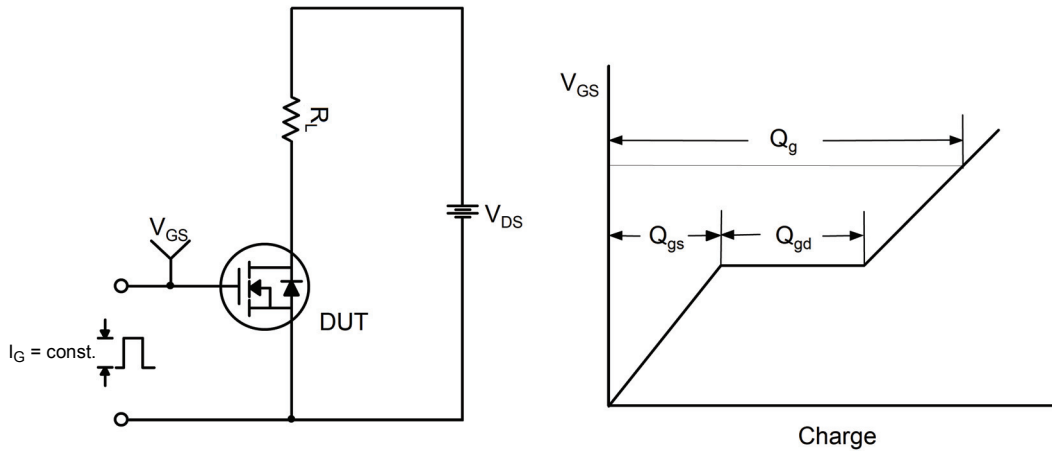
Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve





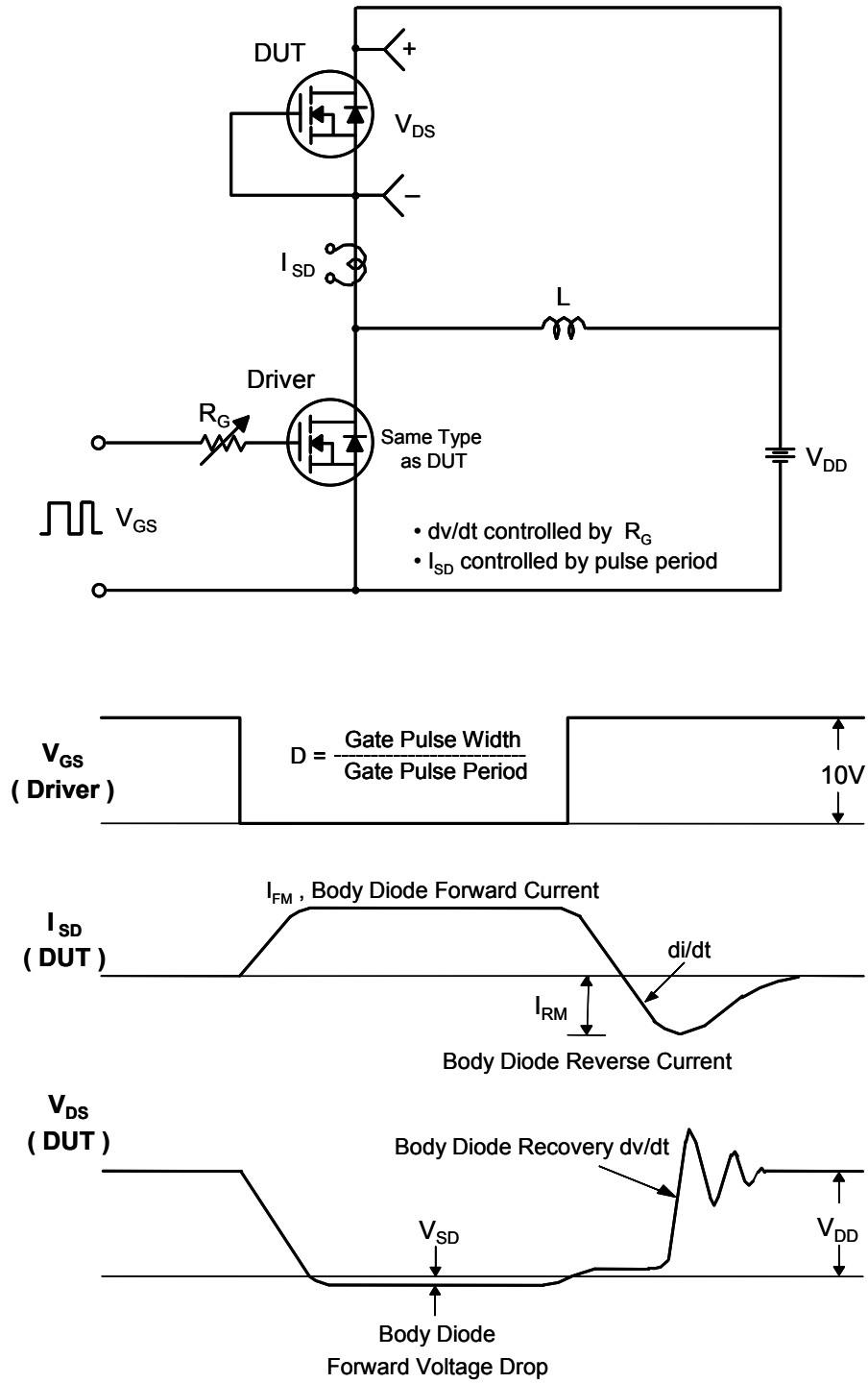
**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**

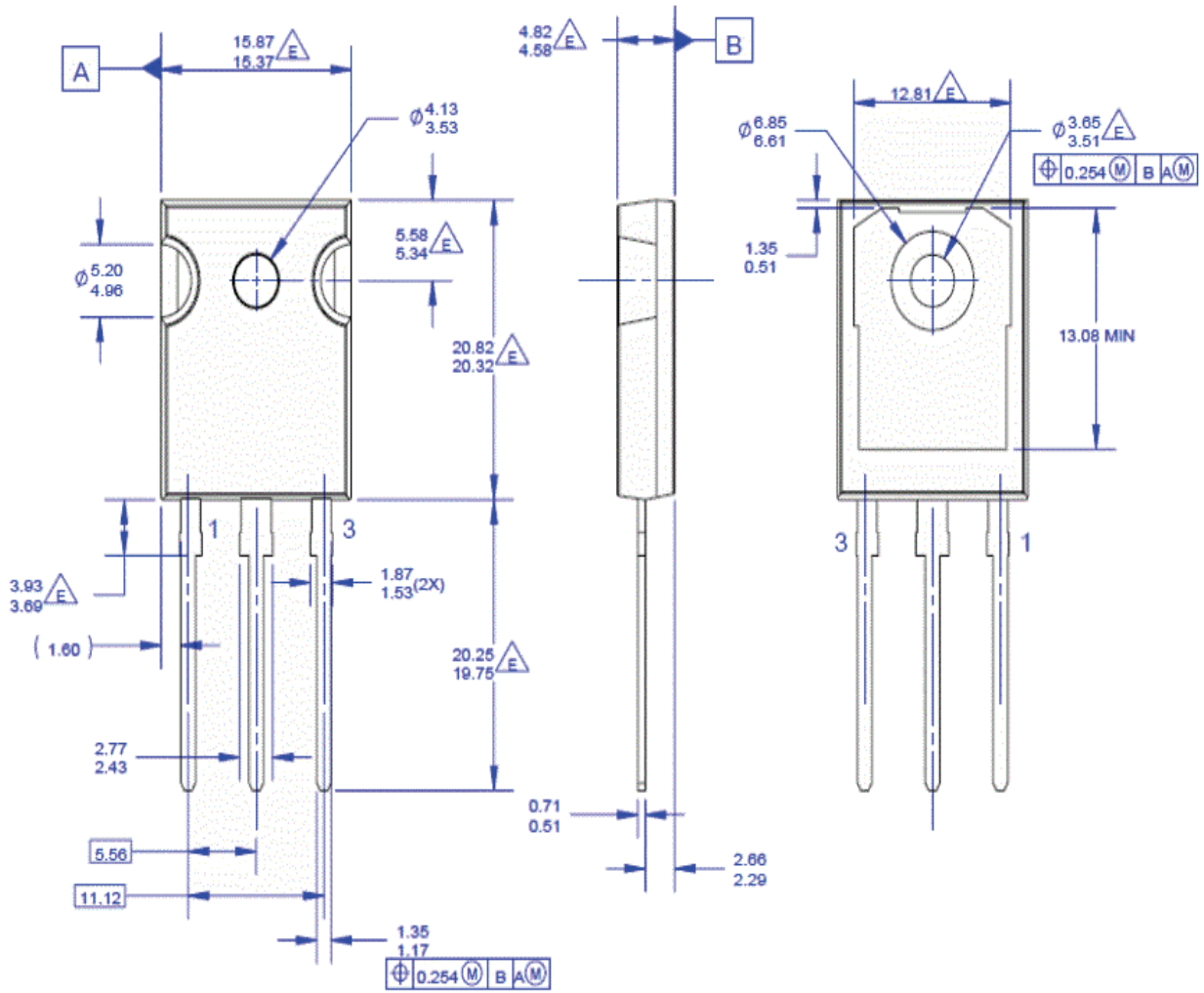


**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**



**Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

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 F. DRAWING FILENAME: MKT-TO247G03\_REV02



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